

TVS1800 18Vフラットクランプ・サージ保護デバイス

1 特長

- 産業用信号ライン向け $\pm 1\text{kV}$ 、 42Ω のIEC 61000-4-5サージ・テストに耐える保護機能
- 最大クランプ電圧: サージ電流(8/20 μs) 40Aで24.7V
- スタンドオフ電圧: 18V
- 4mm²の小さい占有面積
- 125°Cで35Aのサージ電流(8/20 μs)の反復ストライクを5,000回吸収
- 強力なサージ保護:
 - IEC61000-4-5 (8/20 μs): 40A
 - IEC61643-321 (10/1000 μs): 6A
- 低リーク電流
 - 27°Cで1.2nA (標準値)
 - 85°Cで9nA (標準値)
- 低容量: 116pF
- レベル4 IEC 61000-4-2に準拠したESD保護機能を内蔵

2 アプリケーション

- 産業用センサI/O
- ソリッド・ステート・ドライブ
- PLC I/Oモジュール
- 医療用機器
- 12V電カライン
- 15Vアナログ信号入力
- 家電製品

3 概要

TVS1800は、最大40AのIEC 61000-4-5フォルト電流を確実にシャントして、システムを高電力過渡事象や落雷から保護します。一般的な産業用信号ラインのEMC要件向けのソリューションとして、 42Ω のインピーダンスにより結合される、最大 $\pm 1\text{kV}$ のIEC 61000-4-5開路電圧に耐えられます。TVS1800は、独自の帰還メカニズムの採用により、フォルト時に高精度のフラット・クランプングを実現し、システムがさらされる電圧を25V未満に抑えます。電圧レギュレーションが正確であるため、許容電圧の低いシステム部品を安心して選択でき、堅牢性を犠牲にすることなくシステムのコストと複雑さを抑えることができます。

また、TVS1800は占有面積が小さい2mm \times 2mmのSONパッケージで供給されるため、スペースの制約があるアプリケーションに最適であり、業界標準のSMA/SMBパッケージに比べて占有面積を70%削減できます。リーク電流と容量が極めて低いことから、保護するラインへの影響も最小限に抑えられます。製品のライフサイクル全体にわたる堅牢な保護を保証するために、TIはTVS1800に対して高温で5,000回の反復サージが発生するテストを実施し、性能に変化がないことを確認しています。

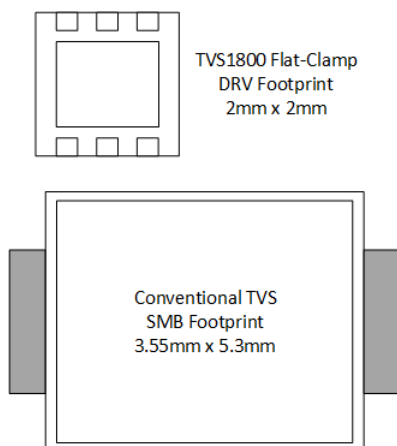
TVS1800はTIのフラットクランプ・サージ・デバイス・ファミリの製品です。このファミリに含まれる他のデバイスの詳細については、「[デバイス比較表](#)」を参照してください。

製品情報⁽¹⁾

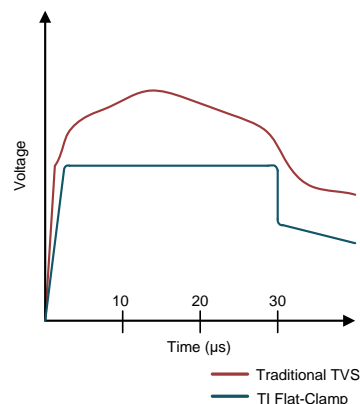
型番	パッケージ	本体サイズ(公称)
TVS1800	SON (6)	2.00mm \times 2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

占有面積の比較



8/20 μs のサージ・イベントに対する電圧クランプの応答



目次

1	特長	1	8.3	Feature Description.....	9
2	アプリケーション	1	8.4	Reliability Testing	9
3	概要	1	8.5	Device Functional Modes.....	10
4	改訂履歴.....	2	9	Application and Implementation	11
5	Device Comparison Table	3	9.1	Application Information.....	11
6	Pin Configuration and Functions	4	9.2	Typical Application	11
7	Specifications	5	10	Power Supply Recommendations	12
7.1	Absolute Maximum Ratings	5	11	Layout	13
7.2	ESD Ratings - JEDEC	5	11.1	Layout Guidelines	13
7.3	ESD Ratings - IEC	5	11.2	Layout Example	13
7.4	Recommended Operating Conditions.....	5	12	デバイスおよびドキュメントのサポート	14
7.5	Thermal Information	5	12.1	ドキュメントの更新通知を受け取る方法.....	14
7.6	Electrical Characteristics.....	6	12.2	コミュニティ・リソース	14
7.7	Typical Characteristics	7	12.3	商標	14
8	Detailed Description	9	12.4	静電気放電に関する注意事項	14
8.1	Overview	9	12.5	Glossary	14
8.2	Functional Block Diagram	9	13	メカニカル、パッケージ、および注文情報	14

4 改訂履歴

2017年12月発行のものから更新

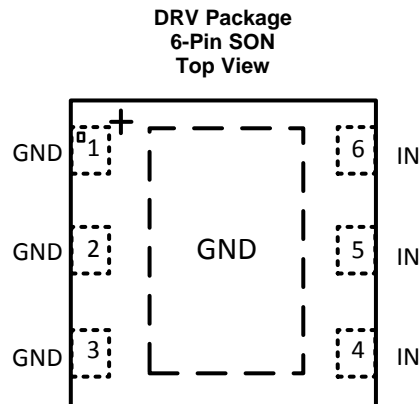
Page

•	製品のステータスを「事前情報」から「量産データ」に変更	1
---	-----------------------------------	---

5 Device Comparison Table

Device	V_{rwm}	V_{clamp} at I_{pp}	I_{pp} (8/20 μ s)	V_{rwm} leakage (nA)	Package Options	Polarity
TVS0500	5	9.2	43	0.07	SON	Unidirectional
TVS1400	14	18.4	43	2	SON	Unidirectional
TVS1800	18	22.8	40	0.5	SON	Unidirectional
TVS2200	22	27.7	40	3.2	SON	Unidirectional
TVS2700	27	32.5	40	1.7	SON	Unidirectional
TVS3300	33	38	35	19	WCSP, SON	Unidirectional

6 Pin Configuration and Functions



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	No.		
IN	4, 5, 6	I	ESD and surge protected channel
GND	1, 2, 3, exposed thermal pad	GND	Ground

7 Specifications

7.1 Absolute Maximum Ratings

 $T_A = 27^\circ\text{C}$ (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Maximum Surge	IEC 61000-4-5 Current (8/20 μs)		40	A
	IEC 61000-4-5 Power (8/20 μs)		960	W
	IEC 61643-321 Current (10/1000 μs)		6	A
	IEC 61643-321 Power (10/1000 μs)		120	W
Maximum Forward Surge	IEC 61000-4-5 Current (8/20 μs)		50	A
	IEC 61000-4-5 Power (8/20 μs)		80	W
	IEC 61643-321 Current (10/1000 μs)		23	A
	IEC 61643-321 Power (10/1000 μs)		60	W
EFT	IEC 61000-4-4 EFT Protection		80	A
I_{br}	DC Breakdown current		18	mA
I_F	DC Forward Current		500	mA
T_A	Ambient Operating Temperature	-40	125	$^\circ\text{C}$
T_{stg}	Storage Temperature	-65	150	$^\circ\text{C}$

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings - JEDEC

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	± 2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	± 500

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings - IEC

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	± 18
		IEC 61000-4-2 air-gap discharge	± 30

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{RWM}	Reverse Stand-off Voltage		18		V

7.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TVS1800	UNIT
		DRV (SON)	
		6 PINS	
R_{qJA}	Junction-to-ambient thermal resistance	70.4	$^\circ\text{C/W}$
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	73.7	$^\circ\text{C/W}$
R_{qJB}	Junction-to-board thermal resistance	40	$^\circ\text{C/W}$
Y_{JT}	Junction-to-top characterization parameter	2.2	$^\circ\text{C/W}$

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

Thermal Information (continued)

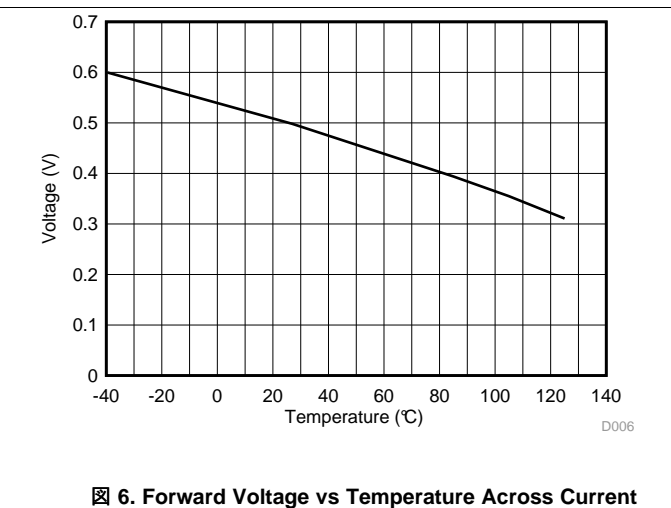
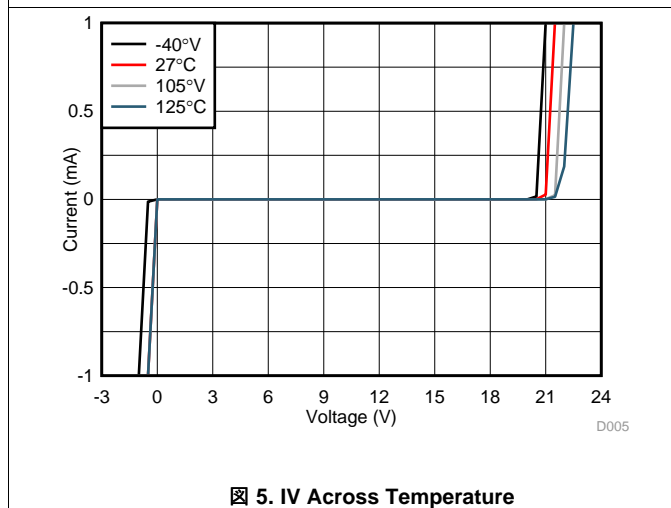
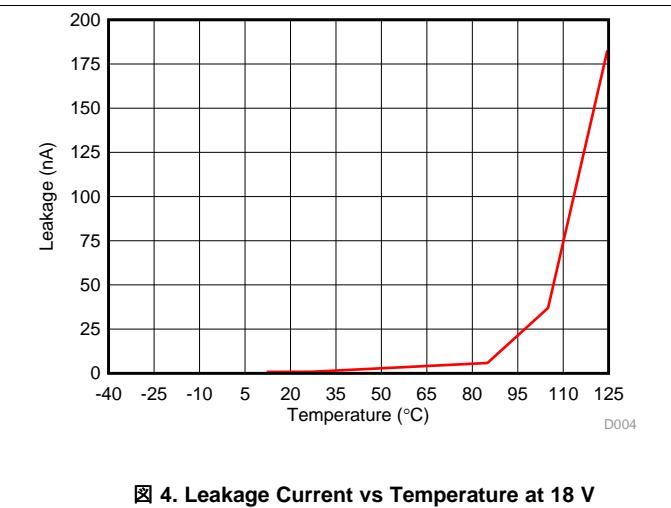
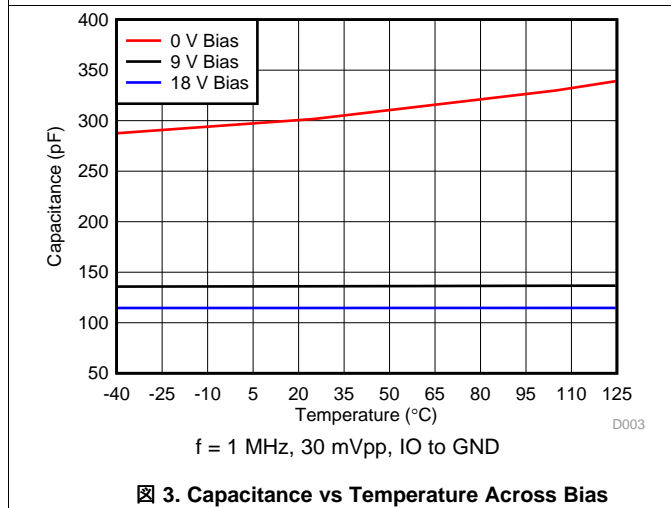
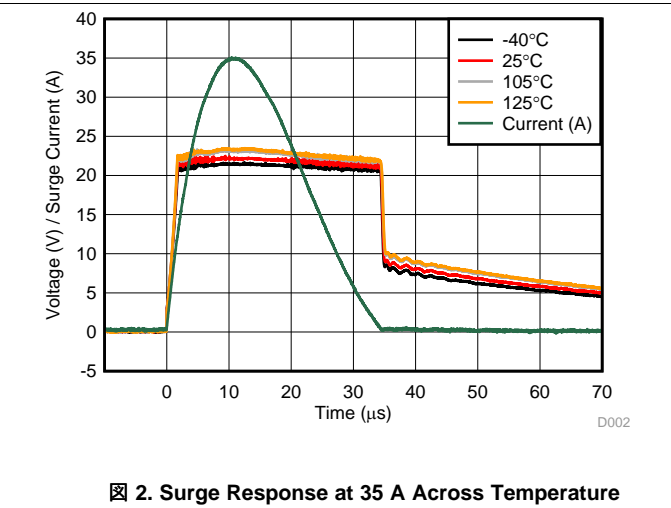
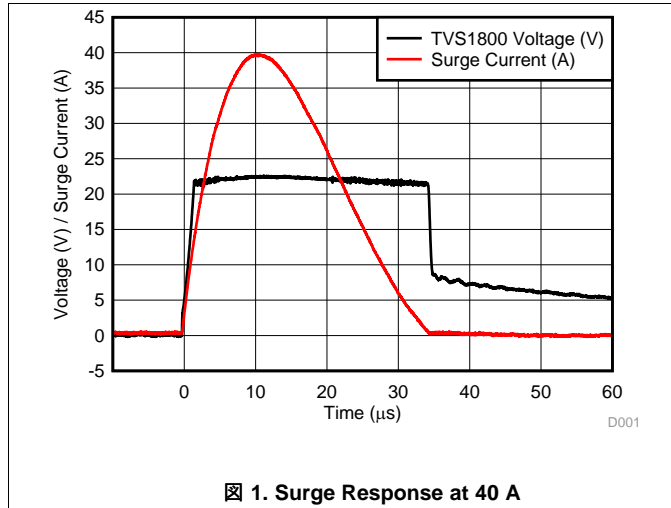
THERMAL METRIC ⁽¹⁾		TVS1800	UNIT
		DRV (SON)	
		6 PINS	
Y_{JB}	Junction-to-board characterization parameter	40.3	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	11	°C/W

7.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse Stand-off Voltage		-0.5		18	V
I_{LEAK}	Leakage Current	Measured at $V_{IN} = V_{RWM}$, $T_A = 27^\circ\text{C}$		1.2	13	nA
		Measured at $V_{IN} = V_{RWM}$, $T_A = 85^\circ\text{C}$		9	330	nA
		Measured at $V_{IN} = V_{RWM}$, $T_A = 105^\circ\text{C}$		52	1150	nA
V_F	Forward Voltage	$I_{IN} = 1\text{ mA}$ from GND to IO	0.25	0.5	0.65	V
V_{BR}	Break-down Voltage	$I_{IN} = 1\text{ mA}$ from IO to GND	19.5	21.3	23.8	V
V_{FCLAMP}	Forward Clamp Voltage	40 A IEC 61000-4-5 Surge (8/20 μs) from GND to IO, 27°C	1	2	5	V
V_{CLAMP}	Clamp Voltage	24 A IEC 61000-4-5 Surge (8/20 μs) from IO to GND, $V_{IN} = 0\text{ V}$ before surge, 27°C		22.5	23	V
		40 A IEC 61000-4-5 Surge (8/20 μs) from IO to GND, $V_{IN} = 0\text{ V}$ before surge, 27°C		22.7	23.4	V
		35 A IEC 61000-4-5 Surge (8/20 μs) from IO to GND, $V_{IN} = V_{RWM}$ before surge, $T_A = 125^\circ\text{C}$		23.7	24.7	V
R_{DYN}	8/20 μs surge dynamic resistance	Calculated from V_{CLAMP} at $.5 \cdot I_{pp}$ and I_{pp} surge current levels, 27°C		30		m Ω
C_{IN}	Input pin capacitance	$V_{IN} = V_{RWM}$, $f = 1\text{ MHz}$, 30 mV $_{pp}$, IO to GND		116		pF
SR	Maximum Slew Rate	0- V_{RWM} rising edge, sweep rise time and measure slew rate when $I_{PK} = 1\text{ mA}$, 27°C		2.5		V/ μs
		0- V_{RWM} rising edge, sweep rise time and measure slew rate when $I_{PK} = 1\text{ mA}$, 105°C		0.7		V/ μs

7.7 Typical Characteristics



Typical Characteristics (continued)

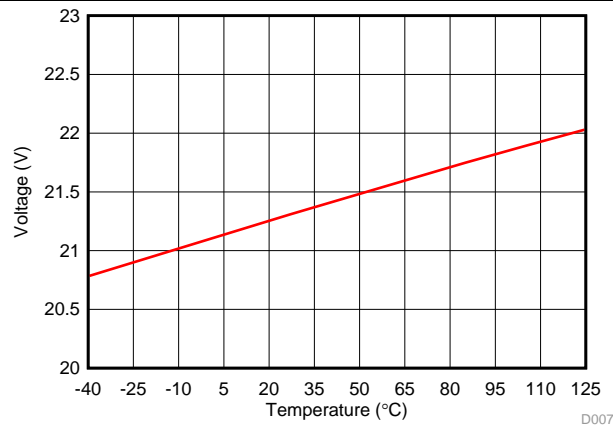


Figure 7. Breakdown Voltage at 1 mA vs Temperature

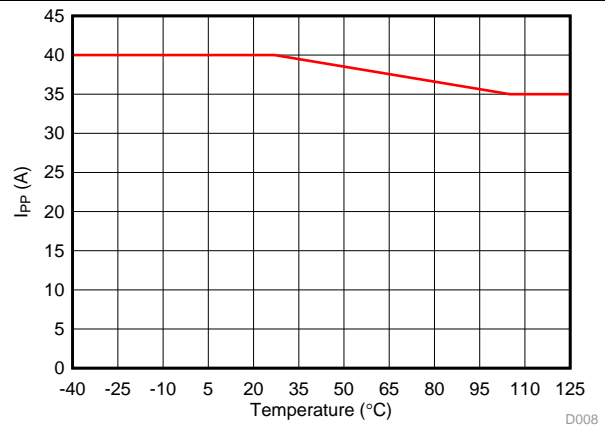


Figure 8. Max Surge Current (8/20 μs) vs Temperature

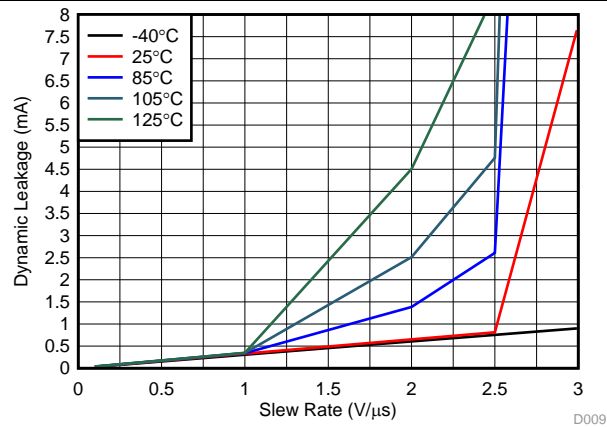


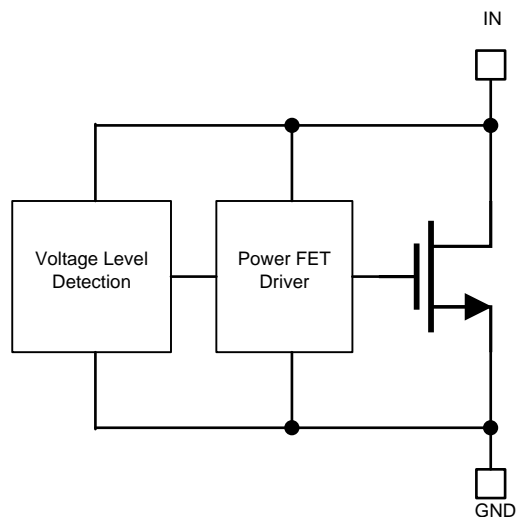
Figure 9. Maximum Leakage vs Signal Slew Rate Across Temperature

8 Detailed Description

8.1 Overview

The TVS1800 is a precision clamp with a low, flat clamping voltage during transient overvoltage events like surge and protecting the system with zero voltage overshoot. For a detailed overview of the Flat-Clamp family of devices, please reference TI's [Flat-Clamp surge protection technology for efficient system protection](#) white paper. This document explains in detail the functional operation of the devices and how they impact and improve system design.

8.2 Functional Block Diagram



Copyright © 2017, Texas Instruments Incorporated

8.3 Feature Description

The TVS1800 is a precision clamp that handles 40 A of IEC 61000-4-5 8/20 μ s surge pulse. The flat clamping feature helps keep the clamping voltage very low to keep the downstream circuits from being stressed. The flat clamping feature can also help end-equipment designers save cost by opening up the possibility to use lower-cost lower voltage tolerant downstream ICs. The TVS1800 has minimal leakage under the standoff voltage of 18 V, making it an ideal candidate for applications where low leakage and power dissipation is a necessity. IEC 61000-4-2 and IEC 61000-4-4 ratings make it a robust protection solution for ESD and EFT events. Wide ambient temperature range of -40°C to $+125^{\circ}\text{C}$ makes it a good candidate for most applications. Compact packages enable it to be used in small devices and save board area.

8.4 Reliability Testing

To ensure device reliability, the TVS1800 is characterized against 5000 repetitive pulses of 35 A IEC 61000-4-5 8/20 μ s surge pulses at 125°C . The test is performed with less than 10 seconds between each pulse at high temperature to simulate worst case scenarios for fault regulation. After each surge pulse, the TVS1800 clamping voltage, breakdown voltage, and leakage are recorded to ensure that there is no variation or performance degradation. By ensuring robust, reliable, high temperature protection, the TVS1800 enables fault protection in applications that must withstand years of continuous operation with no performance change.

8.5 Device Functional Modes

8.5.1 Protection Specifications

The TVS1800 is specified according to both the IEC 61000-4-5 and IEC 61643-321 standards. This enables usage in systems regardless of which standard is required in relevant product standards or best matches measured fault conditions. The IEC 61000-4-5 standard requires protection against a pulse with a rise time of 8 μs and a half length of 20 μs while the IEC 61643-321 standard requires protection against a much longer pulse with a rise time of 10 μs and a half length of 1000 μs .

The positive and negative surges are imposed to the TVS1800 by a combinational waveform generator (CWG) with a 2- Ω coupling resistor at different peak voltage levels. For powered on transient tests that need power supply bias, inductances are usually used to decouple the transient stress and protect the power supply. The TVS1800 is post tested by assuring that there is no shift in device breakdown or leakage at V_{rwm} .

In addition, the TVS1800 has been tested according to IEC 61000-4-5 to pass a ± 1 kV surge test through a 42- Ω coupling resistor and a 0.5 μF capacitor. This test is a common test requirement for industrial signal I/O lines and the TVS1800 will serve as an ideal protection solution for applications with that requirement.

The TVS1800 also integrates IEC 61000-4-2 Level 4 ESD Protection and 80 A of IEC 61000-4-4 EFT Protection. These combine to ensure that the device is able to protect against all transient conditions regardless of length or type.

For more information on TI's test methods for Surge, ESD, and EFT testing, reference [TI's IEC 61000-4-x Testing Application Note](#).

8.5.2 Minimal Derating

Unlike traditional diodes the TVS1800 has very little derating of max power dissipation and ensures robust performance up to 125°C as shown in [Figure 8](#). Traditional TVS diodes lose up to 50% of their current carrying capability when at high temperatures, so a surge pulse above 85°C ambient can cause failures that are not seen at room temperature. The TVS1800 prevents this and ensures that you will see the same level of protection regardless of temperature.

8.5.3 Transient Performance

During large transient swings, the TVS1800 will begin clamping the input signal to protect downstream conditions. While this prevents damage during fault conditions, it can cause leakage when the intended input signal has a fast slew rate. In order to keep power dissipation low and remove the chance of signal distortion, it is recommended to keep the slew rate of any input signal on the TVS1800 below 2.5 V/ μs at room temperature and below 0.7 V/ μs at 125°C as shown in [Figure 9](#). Faster slew rates will cause the device to clamp the input signal and draw current through the device for a few microseconds, increasing the rise time of the signal. This will not cause any harm to the system or to the device, however if the fast input voltage swings occur regularly it can cause device overheating.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TVS1800 can be used to protect any power, analog, or digital signal from transient fault conditions caused by the environment or other electrical components.

9.2 Typical Application

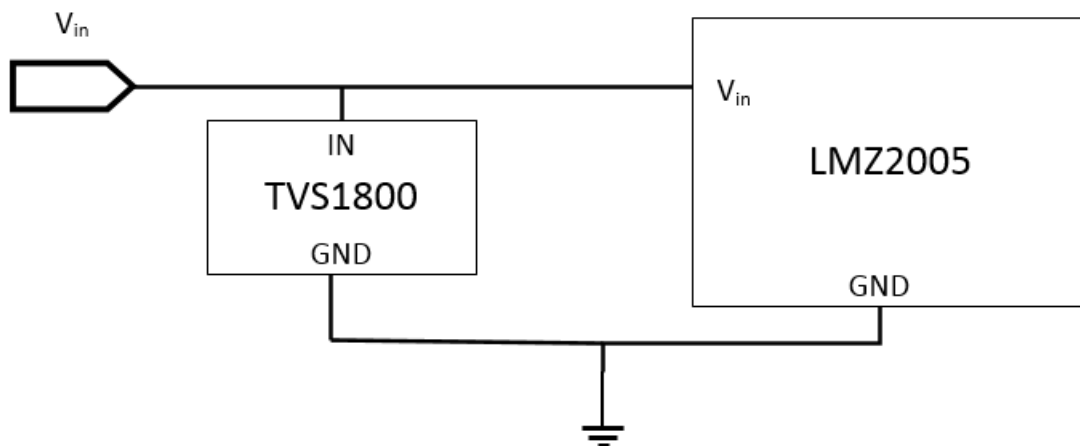


图 10. TVS1800 Application Schematic

9.2.1 Design Requirements

A typical operation for the TVS1800 would be protecting a 12 V input voltage line with a wide variance requiring extra standoff from the nominal voltage, as shown in 图 10. In this example, a TVS1800 is protecting the input to an LMZ2005, a power module with an input voltage range of 20 V and an absolute maximum input voltage of 25 V. Without any input protection, if a surge event is caused by lightning, coupling, ringing, or any other fault condition this input voltage will rise to hundreds of volts for multiple microseconds, violating the absolute maximum input voltage and harming the device. An ideal surge protection diode will maximize the useable voltage range while still clamping at a safe level for the system, so TI's Flat-Clamp technology provides the best protection solution.

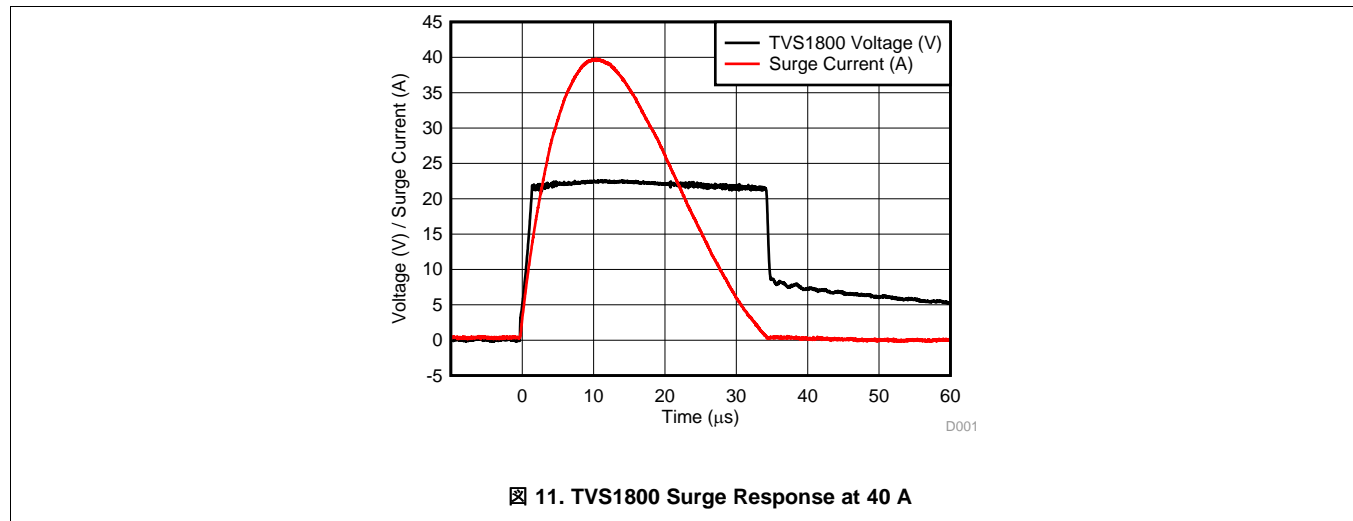
9.2.2 Detailed Design Procedure

If the TVS1800 is in place to protect the device, during a surge event the voltage will rise to the breakdown of the diode at 21 V, and then the TVS1800 will turn on, shunting the surge current to ground. With the low dynamic resistance of the TVS1800, even large amounts of surge current will have minimal impact on the clamping voltage. The dynamic resistance of the TVS1800 is around 30 m Ω , which means 40 A of surge current will cause a voltage raise of 40 A \times 30 m Ω = 1.2 V. Because the device turns on at 21.3 V, this means the module input will be exposed to a maximum of 21.3 V + 1.2 V = 22.5 V during surge pulses, well within the LMZ2005 absolute maximum. This pulse is shown in Figure 11 and ensures robust protection of your circuit.

Typical Application (continued)

Finally, the small size of the device also improves fault protection by lowering the effect of fault current coupling onto neighboring traces. The small form factor of the TVS1800 allows the device to be placed extremely close to the input connector, lowering the length of the path fault current will take through the system compared to larger protection solutions.

9.2.3 Application Curves



9.2.4 Configuration Options

The TVS1800 can be used in either unidirectional or bidirectional configuration. The TVS1800 shows unidirectional usage to protect an input. By placing two TVS1800's in series with reverse orientation, bidirectional operation can be utilized which will allow a working voltage of ± 18 V. The TVS1800 operation in bidirectional will be similar to unidirectional operation, with a minor increase in breakdown voltage and clamping voltage. The TVS3300 bidirectional performance has been characterized in the [TVS3300 Configurations Characterization](#). While the TVS1800 in bidirectional configuration has not specifically been characterized, it will have similar relative changes to the TVS3300 in bidirectional configuration.

10 Power Supply Recommendations

The TVS1800 is a clamping device so there is no need to power it. Be careful not to violate the recommended V_{IN} voltage range (0 V to 18 V) to ensure the device functions properly.

11 Layout

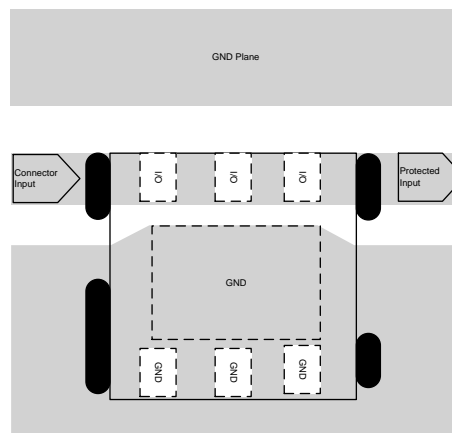
11.1 Layout Guidelines

The optimum placement is as close to the connector as possible. EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures. The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.

Route the protected traces as straight as possible.

Eliminate any sharp corners on the protected traces between the TVS1800 and the connector by using rounded corners with the largest radii possible. Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Example



☒ 12. TVS1800 Layout

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™オンライン・コミュニティ *TIのE2E (Engineer-to-Engineer) コミュニティ*。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.3 商標

E2E is a trademark of Texas Instruments.

12.4 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TVS1800DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1HUH	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TVS1800DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

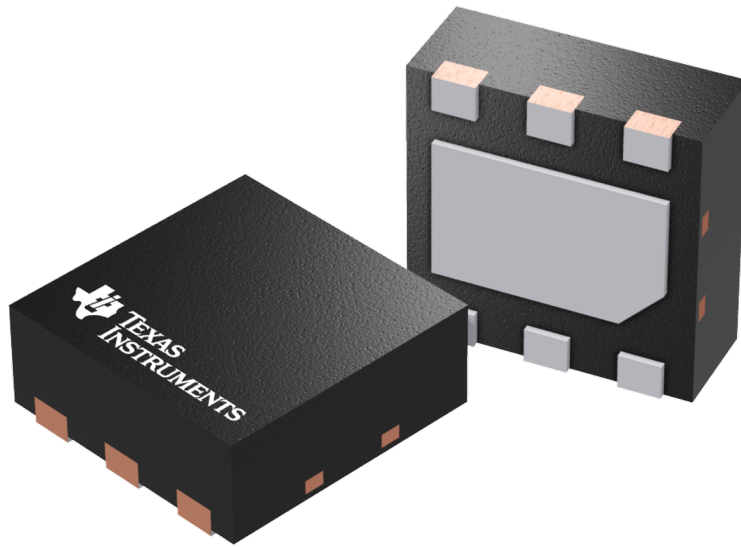
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TVS1800DRVR	WSON	DRV	6	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DRV 6

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4206925/F



4222173/B 04/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

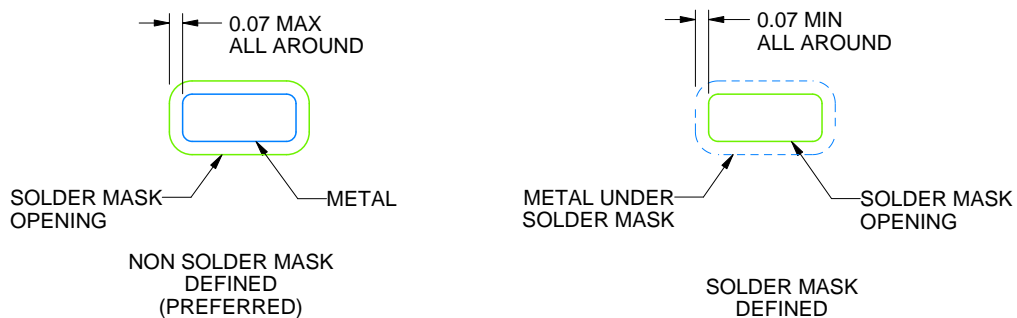
DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売約款 (<https://www.tij.co.jp/ja-jp/legal/terms-of-sale.html>)、または [ti.com](https://www.ti.com) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

日本語版 日本テキサス・インスツルメンツ合同会社
Copyright © 2021, Texas Instruments Incorporated