

TXV0106-Q1 車載用 6 ビット、固定方向、低スキュー、 低ジッタ電圧トランスレータまたはバッファ

1 特長

- 車載アプリケーション向けに AEC-Q100 認定済み
- ダンピング出力抵抗を内蔵
- 汎用とスキューの影響を受けやすいアプリケーション向けの固定方向電圧レベル・シフトとバッファ
- RGMII 2.0 標準タイミング仕様に適合:
 - 立ち上がり時間と立ち下がり時間: 750ps 未満
 - チャネル間スキュー: 400ps 未満
 - デューティ・サイクル歪み: $\pm 5\%$ 未満
- 完全に構成可能な対称型デュアル・レール設計により、各ポートは 1.65V~3.6V で動作可能
- 1.65V~3.6V で最大 320Mbps をサポート
 - RGMII タイミング仕様を満たす最大 250Mbps
- 高い駆動能力 (3.6V で最大 12mA)
- 低消費電力:
 - 最大 10 μ A (25°C)
 - 最大 20 μ A (-40°C~125°C)
- V_{CC} 絶縁および V_{CC} 切断 (I_{off} -float) 機能
 - どちらかの V_{CC} 電源が 100mV 未満になった場合または切断された場合、すべての I/O がプルダウンされた後に高インピーダンス状態に移行
- I_{off} により部分的パワーダウン・モードでの動作をサポート
- 動作温度範囲: -40°C~+125°C
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護:
 - 人体モデルで 2000V
 - 荷電デバイス・モデルで 1000V

2 アプリケーション

- 中距離 / 短距離レーダー
- ADAS ドメイン・コントローラ
- HVAC コントローラ設計
- マシン・ビジョン・カメラ
- ラック・サーバー向けマザーボード
- IP 電話

3 概要

TXV0106-Q1 は、6 ビット、デュアル電源、固定方向、低スキュー、低ジッタの電圧変換デバイスです。このデバイスは、MAC と PHY の間の RGMII 信号など、スキューの影響を受けやすいインターフェイスでのバッファリング、リドライブ、電圧変換、パワーアップ絶縁に使用できます。Ax ピンおよびイネーブル・ピン (\overline{OE}) は V_{CCA} ロジック・レベルを基準とし、Bx ピンは V_{CCB} ロジック・レベルを基準としています。このデバイスは、チャネル間スキュー、デューティ・サイクル歪み、対称型の立ち上がり / 立ち下がりタイミングを改善しており、厳格なタイミング条件を必要とするアプリケーションに適しています。

このデバイスは、 I_{off} を使った部分的パワーダウン・アプリケーション向けに完全に動作が規定されています。 I_{off} 回路が出力をディセーブルにするため、電源切断時にデバイスに電流が逆流して損傷に至ることを回避できます。

V_{CC} 絶縁機能は、いずれかの V_{CC} 電源が 0V 付近になると、両方のポートが高インピーダンス状態になるよう設計されています。この機能により、複数の MAC と PHY にまたがる通信で電力を絶縁でき、MAC と PHY の電源が非同期にオンになり、デバイス間の電流の逆流を防止する状況に有益です。

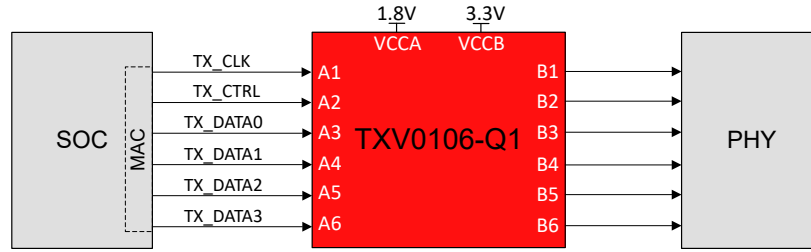
電源投入または電源切断時に高インピーダンス状態を確保するため、 \overline{OE} はプルアップ抵抗経由で V_{CC} に結線します。この抵抗の最小値は、ドライバの電流シンク能力によって決定されます。制御ロジックの動作の概要については、「[デバイスの機能モード](#)」を参照してください。

パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ(2)
TXV0106-Q1	BQB (WQFN, 16)	3.5mm × 2.5mm

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- (2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。





RGMII アプリケーションの TXV010x-Q1

ADVANCE INFORMATION

Table of Contents

1 特長	1	8.3 Feature Description.....	14
2 アプリケーション	1	8.4 Device Functional Modes.....	15
3 概要	1	9 Application and Implementation	16
4 Revision History	3	9.1 Application Information.....	16
5 Pin Configuration and Functions	4	9.2 Typical Application.....	16
6 Specifications	5	9.3 Power Supply Recommendations.....	17
6.1 Absolute Maximum Ratings.....	5	9.4 Layout.....	18
6.2 ESD Ratings.....	5	10 Device and Documentation Support	19
6.3 Recommended Operating Conditions.....	6	10.1 Documentation Support.....	19
6.4 Thermal Information.....	6	10.2 ドキュメントの更新通知を受け取る方法.....	19
6.5 Electrical Characteristics.....	7	10.3 サポート・リソース.....	19
6.6 Switching Characteristics, $V_{CCA} = 1.8 \pm 0.15 \text{ V}$	8	10.4 Trademarks.....	19
6.7 Switching Characteristics, $V_{CCA} = 2.5 \pm 0.2 \text{ V}$	9	10.5 静電気放電に関する注意事項.....	19
6.8 Switching Characteristics, $V_{CCA} = 3.3 \pm 0.3 \text{ V}$	10	10.6 用語集.....	19
7 Parameter Measurement Information	11	11 Mechanical, Packaging, and Orderable Information	19
7.1 Load Circuit and Voltage Waveforms.....	11	11.1 Tape and Reel Information.....	20
8 Detailed Description	13	11.2 Mechanical Data.....	22
8.1 Overview.....	13		
8.2 Functional Block Diagram.....	13		

4 Revision History

DATE	REVISION	NOTES
July 2023	*	Initial Release

5 Pin Configuration and Functions

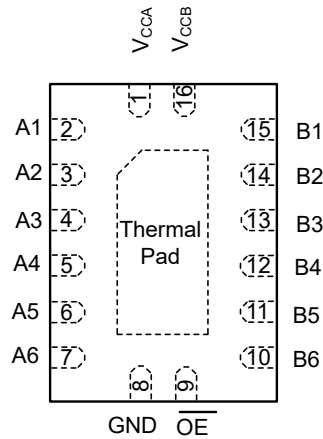


图 5-1. BQB Package, 16-Pin WQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
V _{CCA}	1	—	A-port supply voltage. 1.8 V ≤ V _{CCA} ≤ 3.6 V.
A1	2	I/O	Input/output A1. Referenced to V _{CCA} .
A2	3	I/O	Input/output A2. Referenced to V _{CCA} .
A3	4	I/O	Input/output A3. Referenced to V _{CCA} .
A4	5	I/O	Input/output A4. Referenced to V _{CCA} .
A5	6	I/O	Input/output A5. Referenced to V _{CCA} .
A6	7	I/O	Input/output A6. Referenced to V _{CCA} .
GND	8	—	Ground.
OE	9	I	Output Enable. Pull to GND to enable all outputs. Pull to V _{CCA} to place all outputs in high-impedance mode. Referenced to V _{CCA} .
B6	10	I/O	Input/output B6. Referenced to V _{CCB} .
B5	11	I/O	Input/output B5. Referenced to V _{CCB} .
B4	12	I/O	Input/output B4. Referenced to V _{CCB} .
B3	13	I/O	Input/output B3. Referenced to V _{CCB} .
B2	14	I/O	Input/output B2. Referenced to V _{CCB} .
B1	15	I/O	Input/output B1. Referenced to V _{CCB} .
V _{CCB}	16	—	B-port supply voltage. 1.8 V ≤ V _{CCB} ≤ 3.6 V.
Thermal pad		—	Thermal pad. Can be grounded (recommended) or left floating.

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CCA}	Supply voltage A		-0.5	4.6	V
V _{CCB}	Supply voltage B		-0.5	4.6	V
V _I	Input Voltage ⁽²⁾	I/O Ports (A Port)	-0.5	4.6	V
		I/O Ports (B Port)	-0.5	4.6	
		Control Inputs	-0.5	4.6	
V _O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	A Port	-0.5	4.6	V
		B Port	-0.5	4.6	
V _O	Voltage applied to any output in the high or low state ^{(2) (3)}	A Port	-0.5	V _{CCA} + 0.5	V
		B Port	-0.5	V _{CCB} + 0.5	
I _{IK}	Input clamp current	V _I < 0	-50		mA
I _{OK}	Output clamp current	V _O < 0	-50		mA
I _O	Continuous output current		-50	50	mA
	Continuous current through V _{CC} or GND		-100	100	
T _j	Junction Temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

- (1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C3	±1000	V

- (1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

			MIN	MAX	UNIT	
V _{CCA}	Supply voltage A		1.65	3.6	V	
V _{CCB}	Supply voltage B		1.65	3.6	V	
V _{IH}	High-level input voltage	Data Inputs (Ax, Bx), OE (Referenced to V _{CCI})	V _{CCI} = 1.65 V to 3.6 V		V _{CCI} × 0.7	V
V _{IL}	Low-level input voltage	Data Inputs (Ax, Bx), OE (Referenced to V _{CCI})	V _{CCI} = 1.65 V to 3.6 V		V _{CCI} × 0.3	V
I _{OH}	High-level output current		V _{CCO} = 1.65 V – 1.95 V		–8	mA
	High-level output current		V _{CCO} = 2.3 V – 2.7 V		–9	mA
	High-level output current		V _{CCO} = 3 V – 3.6 V		–12	mA
I _{OL}	Low-level output current		V _{CCO} = 1.65 V – 1.95 V		8	mA
	Low-level output current		V _{CCO} = 2.3 V – 2.7 V		9	mA
	Low-level output current		V _{CCO} = 3 V – 3.6 V		12	mA
V _I	Input voltage		0	3.6	V	
V _O	Output voltage	Active State	0	V _{CCO}	V	
		Tri-State	0	3.6	V	
Δt/Δv	Input transition rise and fall time			5	ns/V	
T _A	Operating free-air temperature		–40	125	°C	

(1) V_{CCI} is the V_{CC} associated with the input port. V_{CCO} is the V_{CC} associated with the output port.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TXV0106-Q1	UNIT
		BQB (WQFN)	
		16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	TBD	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	TBD	°C/W
R _{θJB}	Junction-to-board thermal resistance	TBD	°C/W
Y _{JT}	Junction-to-top characterization parameter	TBD	°C/W
Y _{JB}	Junction-to-board characterization parameter	TBD	°C/W
R _{θJC(bottom)}	Junction-to-case (bottom) thermal resistance	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) app report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)^{(1) (2)}

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	Operating free-air temperature (T _A)			UNIT	
					–40°C to 125°C				
					MIN	TYP	MAX		
V _{IL}	Data Input_Negative threshold	Data inputs, \overline{OE}	1.65 V – 3.6 V	1.65 V – 3.6 V			0.3× V _{CCA}	V	
V _{IH}	Data Input_Positive threshold	Data inputs, \overline{OE}	1.65 V – 3.6 V	1.65 V – 3.6 V			0.7× V _{CCA}	V	
V _{OH}	High-level output voltage ⁽³⁾	I _{OH} = –8 mA	1.65 V	1.65 V			1.2	V	
		I _{OH} = –9 mA	2.3 V	2.3 V			1.8	V	
		I _{OH} = –12 mA	3 V	3 V			2.4	V	
V _{OL}	Low-level output voltage ⁽⁴⁾	I _{OL} = 8 mA	1.65 V	1.65 V			0.27	V	
		I _{OL} = 9 mA	2.3 V	2.3 V			0.23	V	
		I _{OL} = 12 mA	3 V	3 V			0.26	V	
I _I	Input leakage current	Data Inputs (Ax, Bx) V _I = V _{CCI} or GND	1.65 V – 3.6 V	1.65 V – 3.6 V			–0.16	0.35	μA
I _{off}	Partial power down current	A Port or B Port V _I or V _O = 0 V – 3.6 V	0 V	0 V – 3.6 V			–5	3.6	μA
		A Port or B Port V _I or V _O = 0 V – 3.6 V	0 V – 3.6 V	0 V			–5	3.6	
I _{OZ}	Tri-state output current ⁽⁵⁾	A or B Port: V _I = V _{CCI} or GND V _O = V _{CCO} or GND \overline{OE} = V _{IH}	3.6 V	3.6 V			–0.16	0.35	μA
I _{CCA}	V _{CCA} supply current	V _I = V _{CCI} or GND I _O = 0	1.65 V – 3.6 V	1.65 V – 3.6 V				14	μA
			0 V	3.6 V			–0.036		
			3.6 V	0 V				11	
I _{CCB}	V _{CCB} supply current	V _I = V _{CCI} or GND I _O = 0	1.65 V – 3.6 V	1.65 V – 3.6 V				12	μA
			0 V	3.6 V				8.6	
			3.6 V	0 V			–0.036		
I _{CCA} + I _{CCB}	Combined supply current	V _I = V _{CCI} or GND I _O = 0	1.65 V – 3.6 V	1.65 V – 3.6 V				22	μA
C _i	Control Input Capacitance	V _I = 3.3 V or GND	3.3 V	3.3 V				3.9	pF
C _{io}	Data I/O Capacitance	\overline{OE} = V _{CCA} , V _O = 1.65 V DC +1 MHz -16 dBm sine wave	3.3 V	3.3 V				2.7	pF

- (1) V_{CCI} is the V_{CC} associated with the input port.
- (2) V_{CCO} is the V_{CC} associated with the output port.
- (3) Tested at V_I = V_{IH}.
- (4) Tested at V_I = V_{IL}.
- (5) For I/O ports, the parameter I_{OZ} includes the input leakage current.

6.6 Switching Characteristics, $V_{CCA} = 1.8 \pm 0.15 \text{ V}$

Minimum and maximum limits apply over the recommended temperature range at $C_L = 15 \text{ pF}$ and 250Mbps, unless otherwise indicated.

PARAMETER	FROM	TO	B-Port Supply Voltage (V_{CCB})									Unit	
			$1.8 \pm 0.15 \text{ V}$			$2.5 \pm 0.2 \text{ V}$			$3.3 \pm 0.3 \text{ V}$				
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{pd}	Propagation delay	A	B			5			3.7			3.1	ns
t_{dis}	Disable time	\overline{OE}	B			7.6			5.7			6.7	ns
t_{en}	Enable time	\overline{OE}	B			4.4			3.2			2.9	ns
t_{SKO}	Output Channel-to-channel skew	A	B			490			320			360	ps
T_R	Rise time (20% to 80%)	A	B			1.42			1			0.87	ns
T_F	Fall time (20% to 80%)	A	B			1.42			1			0.9	ns
Duty Cycle	Duty cycle variation	A	B	46	50	56	48	50	54	48	50	54	%
$T_{R_5 \text{ pF}}$	Rise time (20% to 80%) ⁽¹⁾	A	B			0.83			0.59			0.47	ns
$T_{F_5 \text{ pF}}$	Fall time (20% to 80%) ⁽¹⁾	A	B			0.83			0.61			0.48	ns
$t_{SKO_5 \text{ pF}}$	Output Channel-to-channel skew ⁽¹⁾	A	B			320			290			335	ps
Duty Cycle _{5 pF}	Duty cycle variation ⁽¹⁾	A	B	48	50	54	49	50	54	49	50	54	%

(1) Parameters tested under RGMII input transition rise and fall time. $C_{LOAD} = 5 \text{ pF}$

6.7 Switching Characteristics, $V_{CCA} = 2.5 \pm 0.2 \text{ V}$

Minimum and maximum limits apply over the recommended temperature range at $C_L = 15 \text{ pF}$ and 250Mbps, unless otherwise indicated.

PARAMETER	FROM	TO	B-Port Supply Voltage (V_{CCB})									Unit	
			1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V				
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{pd}	Propagation delay	A	B	5			3.6			3			ns
t_{dis}	Disable time	\overline{OE}	B	6.8			5.2			6.3			ns
t_{en}	Enable time	\overline{OE}	B	3.8			2.6			2.2			ns
t_{SKO}	Output Channel-to-channel skew	A	B	480			320			360			ps
T_R	Rise time (20% to 80%)	A	B	1.4			1			0.85			ns
T_F	Fall time (20% to 80%)	A	B	1.4			1			0.84			ns
Duty Cycle	Duty cycle variation	A	B	46	50	56	48	50	54	48	50	54	%
T_{R_5pF}	Rise time (20% to 80%) ⁽¹⁾	A	B	0.82			0.59			0.47			ns
T_{F_5pF}	Fall time (20% to 80%) ⁽¹⁾	A	B	0.83			0.61			0.48			ns
t_{SKO_5pF}	Output Channel-to-channel skew ⁽¹⁾	A	B	321			290			334			ps
Duty Cycle _{5 pF}	Duty cycle variation ⁽¹⁾	A	B	48	50	54	49	50	54	49	50	54	%

(1) Parameters tested under RGMII input transition rise and fall time. $C_{LOAD} = 5 \text{ pF}$

6.8 Switching Characteristics, $V_{CCA} = 3.3 \pm 0.3 \text{ V}$

Minimum and maximum limits apply over the recommended temperature range at $C_L = 15 \text{ pF}$ and 250Mbps, unless otherwise indicated.

PARAMETER	FROM	TO	B-Port Supply Voltage (V_{CCB})									Unit	
			1.8 ± 0.15 V			2.5 ± 0.2 V			3.3 ± 0.3 V				
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{pd}	Propagation delay	A	B	4.1			2.8			2.3			ns
t_{dis}	Disable time	\overline{OE}	A	7.6			7.6			7.6			ns
t_{en}	Enable time	\overline{OE}	A	4.4			4.4			4.4			ns
t_{SKO}	Output Channel-to-channel skew	A	B	310			190			150			ps
T_R	Rise time (20% to 80%)	A	B	1.4			1			0.84			ns
T_F	Fall time (20% to 80%)	A	B	1.4			1			0.84			ns
Duty Cycle	Duty cycle variation	A	B	46	50	54	48	50	53	48	50	52	%
T_{R_5pF}	Rise time (20% to 80%) ⁽¹⁾	A	B	0.83			0.59			0.47			ns
T_{F_5pF}	Fall time (20% to 80%) ⁽¹⁾	A	B	0.83			0.61			0.48			ns
t_{SKO_5pF}	Output Channel-to-channel skew ⁽¹⁾	A	B	180			130			120			ps
Duty Cycle _{5 pF}	Duty cycle variation ⁽¹⁾	A	B	48	50	53	49	50	52	49	50	52	%

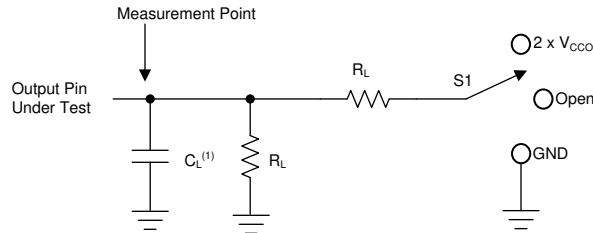
(1) Parameters tested under RGMII input transition rise and fall time. $C_{LOAD} = 5 \text{ pF}$

7 Parameter Measurement Information

7.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- $f = 1 \text{ MHz}$
- $Z_O = 50 \Omega$
- $\Delta t/\Delta V \leq 1 \text{ ns/V}$

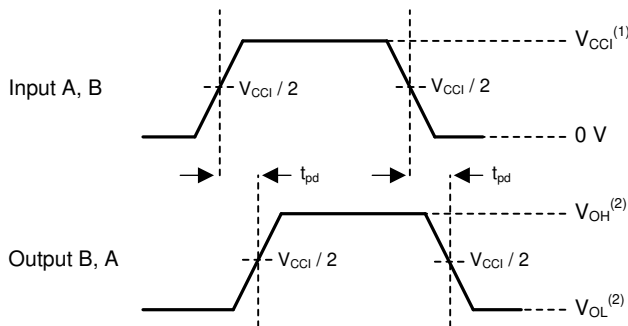


A. C_L includes probe and jig capacitance.

图 7-1. Load Circuit

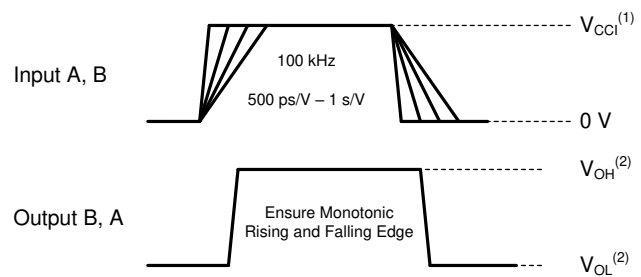
表 7-1. Load Circuit Conditions

Parameter	V_{CCO}	R_L	C_L	S_1	V_{TP}
t_{pd} Propagation (delay) time	1.65 V – 3.6 V	2 k Ω	15 pF	Open	N/A
t_{en} , t_{dis} Enable time, disable time	1.65 V – 3.6 V	2 k Ω	15 pF	$2 \times V_{CCO}$	0.15 V
t_{en} , t_{dis} Enable time, disable time	1.65 V – 3.6 V	2 k Ω	15 pF	GND	0.15 V



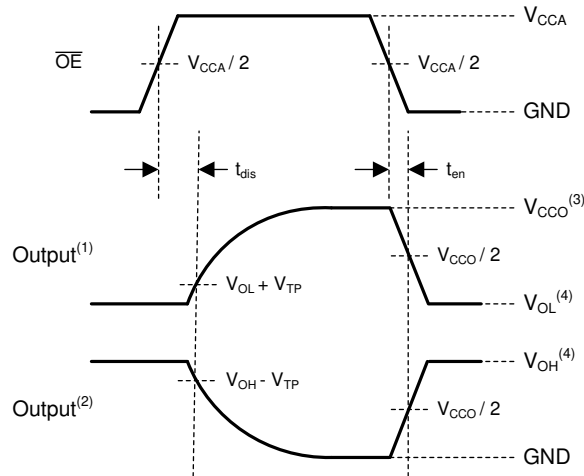
1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L , C_L , and S_1

图 7-2. Propagation Delay



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L , C_L , and S_1

图 7-3. Input Transition Rise and Fall Rate



- A. Output waveform on the condition that input is driven to a valid Logic Low.
- B. Output waveform on the condition that input is driven to a valid Logic High.
- C. V_{CCO} is the supply pin associated with the output port.
- D. V_{OH} and V_{OL} are typical output voltage levels with specified R_L , C_L , and S_1 .

7-4. Enable Time and Disable Time

8 Detailed Description

8.1 Overview

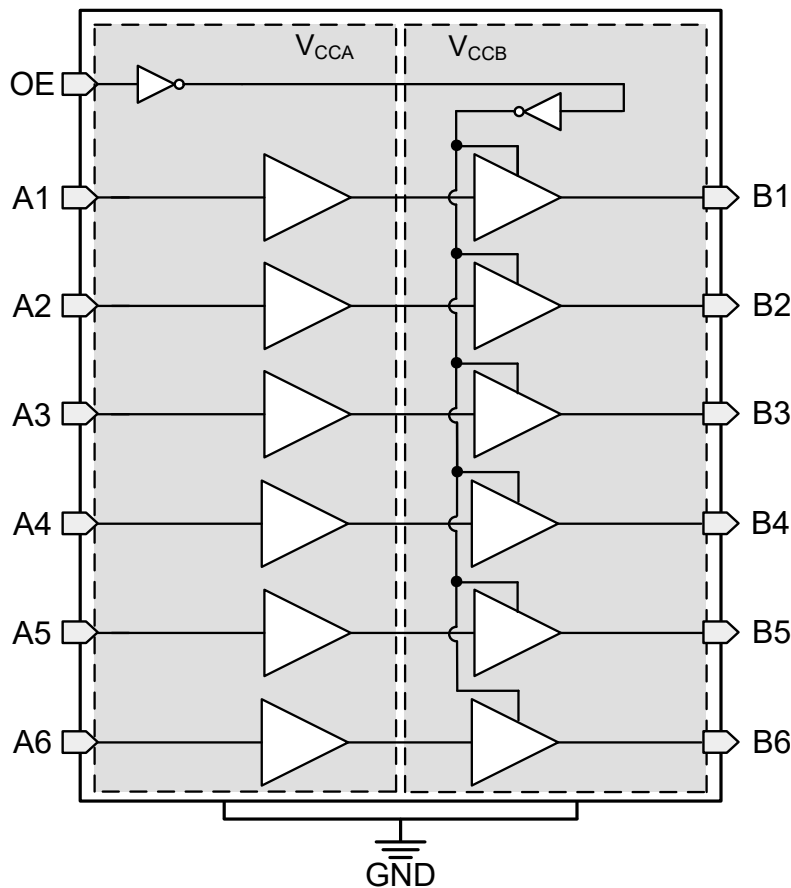
The TXV0106-Q1 is a 6-bit translating transceiver that uses two individually configurable power-supply rails. The device is operational with both V_{CCA} and V_{CCB} supplies as low as 1.65 V and as high as 3.6 V. Additionally, the device can be operated with $V_{CCA} = V_{CCB}$. The Ax port is designed to track V_{CCA} , and the Bx port is designed to track V_{CCB} .

The TXV0106-Q1 device is designed for asynchronous communication between data buses, and transmits data in a fixed direction from the A bus to the B bus. The output-enable input (\overline{OE}) is used to disable the outputs so the buses are effectively isolated. The output-enable pin (\overline{OE}) of the TXV0106-Q1 is referenced to V_{CCA} . To enable the high-impedance state of the level shifter I/Os during power up or power down, the \overline{OE} pin should be tied to V_{CCA} through a pullup resistor.

This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry prevents excessive current from being drawn from or sourced into an input, output, or I/O while the device is powered down.

The V_{CC} isolation or V_{CC} disconnect feature is designed so that if either V_{CC} is less than 100 mV or disconnected with the complementary supply within the recommended operating conditions, both I/O ports are weakly pulled-down and then set to the high-impedance state by disabling their outputs while the supply current is maintained. The $I_{off-float}$ circuitry prevents excessive current from being drawn from or sourced into an input, output, or I/O while the supply is floating.

8.2 Functional Block Diagram




8-1. Functional Block Diagram of the TXV0106-Q1

8.3 Feature Description

8.3.1 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the [Absolute Maximum Ratings](#) must be followed at all times.

8.3.2 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the [Electrical Characteristics](#).

8.3.3 V_{CC} Isolation and V_{CC} Disconnect ($I_{off(float)}$)

This device has 2 features (V_{CC} Isolation and V_{CC} Disconnect) which helps in preventing current backflow in case the device is powered down unexpectedly. V_{CC} Isolation: when one of the supplies is kept at (or goes to) zero during normal operation, no current will be consumed by the supply that is maintained. This scenario forces all I/Os to be High-Z. V_{CC} Disconnect: when one of the supplies is left floating (disconnect) after ramping up, the I/Os are forced into High-Z without consuming any current from the maintained supply. In both cases, the I/Os will enter a high-impedance state when either supply (V_{CCA} or V_{CCB}) is <100 mV or left floating, while the other supply is still connected to the device. The following figure shows more information.

The maximum supply current is specified by I_{CCx} , while V_{CCx} is floating, in the [Electrical Characteristics](#). The maximum leakage into or out of any input or output pin on the device is specified by $I_{off(float)}$ in the [Electrical Characteristics](#).

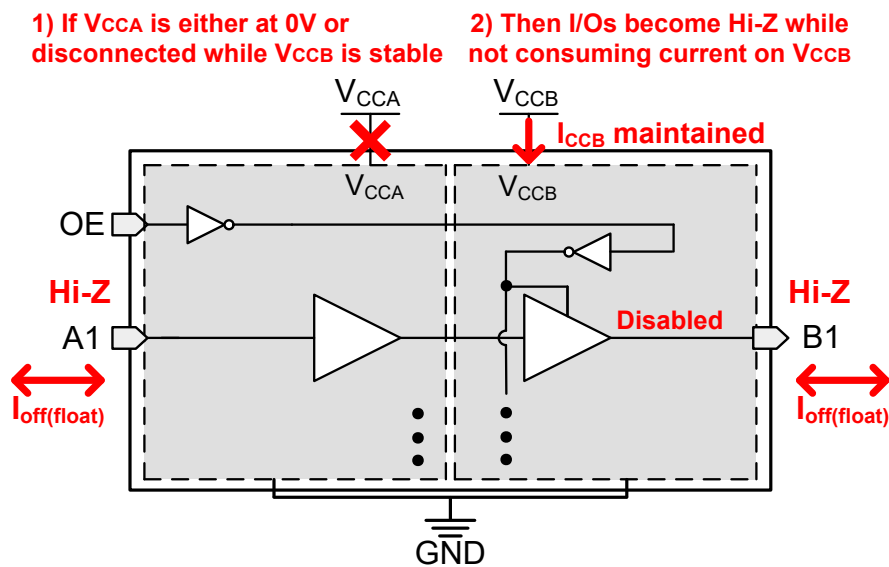


图 8-2. V_{CC} Disconnect and V_{CC} Isolation Feature

8.3.4 Over-Voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the [Recommended Operating Conditions](#).

8.3.5 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in [Figure 8-3](#)

注意

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

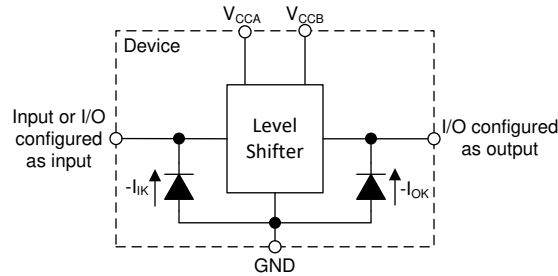


Figure 8-3. Electrical Placement of Clamping Diodes for Each Input and Output

8.3.6 Fully Configurable Dual-Rail Design

Both the V_{CCA} and V_{CCB} pins can be supplied at any voltage from 1.65 V to 3.6 V, making the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, and 3.3 V).

8.3.7 Supports High-Speed Translation

The TXV0106-Q1 device can support high data rate applications. The translated signal data rate can support up to 320Mbps when the signal is translated from 1.8 V to 3.3 V. For the device to meet RGMII 2.0 timing specifications (rise or fall time, skew, and duty cycle distortion) the data rate will need to be lowered to 250Mbps.

8.4 Device Functional Modes

Table 8-1. Function Table

CONTROL INPUTS (1)	PORT STATUS		OPERATION
	A PORT	B PORT	
L	Input (Hi-Z)	Output (Enabled)	A data to B bus
H	Input (Hi-Z)	Input (Hi-Z)	Isolation

(1) Input circuits of the data I/Os are always active and should be kept at a valid logic level.

9 Application and Implementation

注

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9.1 Application Information

The TXV0106-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The TXV0106-Q1 device is an excellent choice for use in applications where a push-pull driver is connected to the data I/Os. The maximum data rate can be up to 320Mbps when device translates a signal from 1.8 V to 3.3 V.

9.2 Typical Application

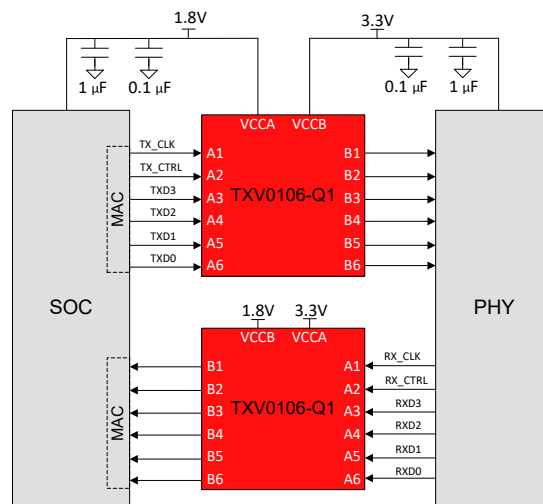


図 9-1. RGMII Application (Interfacing Between MAC and PHY)

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	1.8 V to 3.3 V
Output voltage range	1.8 V to 3.3 V
Frequency	125 MHz
Load Capacitance	5 pF
Input Transition Rise/Fall Time	< 2 ns/V

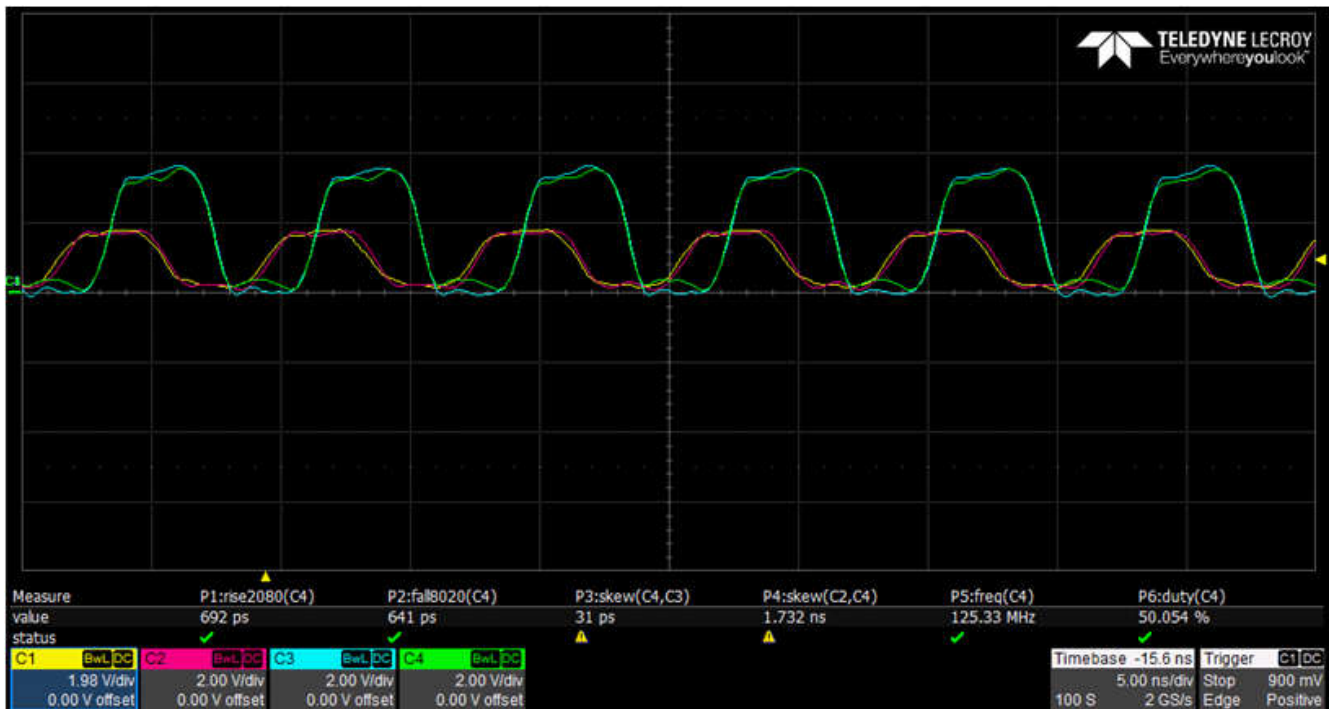
9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
 - Use the supply voltage of the device that is driving the TXV0106-Q1 device to determine the input voltage range. For a valid logic-high, the value must exceed the positive-going input-threshold voltage (V_{t+}) of the input port. For a valid logic low the value must be less than the negative-going input-threshold voltage (V_{t-}) of the input port.

- Output voltage range
 - Use the supply voltage of the device that the TXV0106-Q1 device is driving to determine the output voltage range.
- RGMII Compliant
 - For the TXV0106-Q1 to meet RGMII timing specifications, parameters like frequency, C_{LOAD} and input rise or fall transition have to be met. Make sure each channel does not exceed a maximum frequency of 125 MHz, use a C_{LOAD} no greater than 5 pF, and use an input rise or fall translation no greater than 2 ns/V.

9.2.3 Application Curves



9-2. TXV0106-Q1 Timing Measurements

9.3 Power Supply Recommendations

The TXV0106-Q1 uses two separate configurable power supply rails, V_{CCA} and V_{CCB} . The A port and B port are designed to track V_{CCA} and V_{CCB} , respectively, allowing for low-voltage fixed translation between any of the 1.8-V, 2.5-V and 3.3-V voltage nodes.

The output-enable \overline{OE} input circuit is designed to be supplied by V_{CCA} . When the \overline{OE} input is high, all outputs are placed in the high-impedance state. To make sure a high-impedance state of the outputs occurs during power up or power down, the \overline{OE} input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

ADVANCE INFORMATION

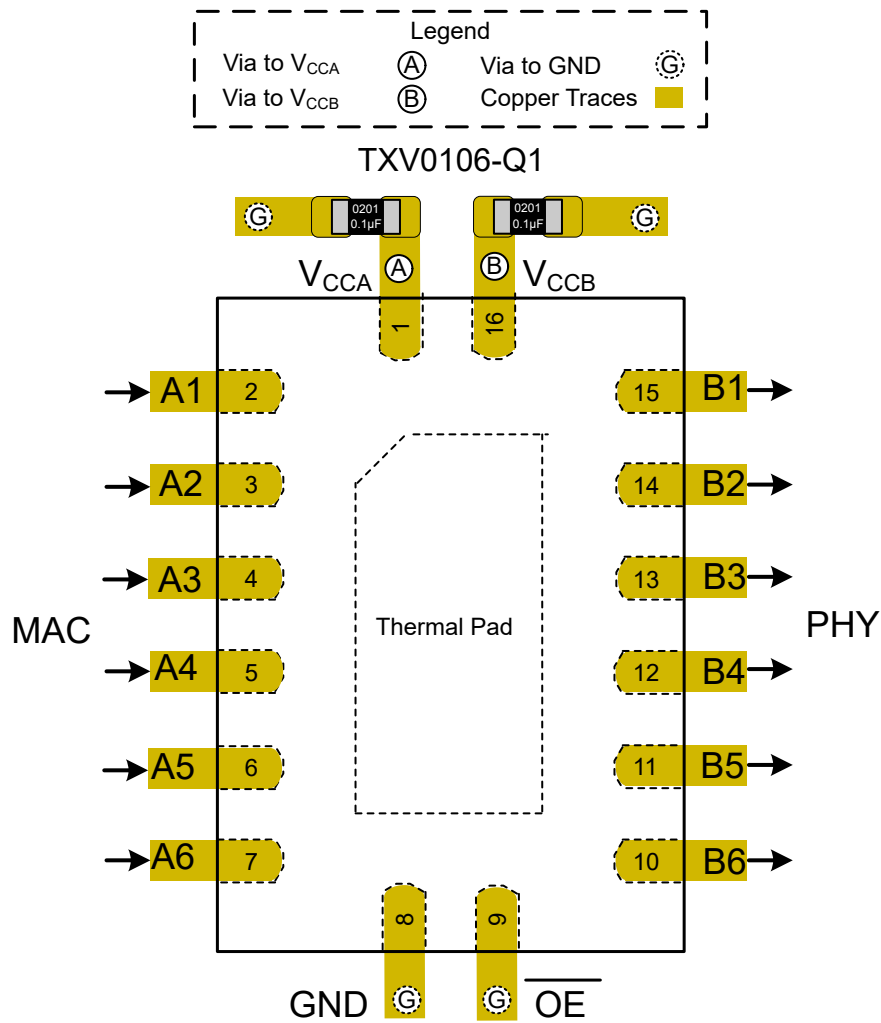
9.4 Layout

9.4.1 Layout Guidelines

For device reliability, follow common printed-circuit board layout guidelines such as the following:

- Use short trace lengths to avoid excessive.
- Use bypass capacitors on the power supply pins and place them as close to the device as possible.
- A 0.1- μ F bypass capacitor is recommended, but transient performance can be improved by having both 1- μ F and 0.1- μ F capacitors in parallel with the smallest value capacitor placed closest to the power pin.
- The high drive capability of this device creates fast edges into light loads. Routing and load conditions should be considered to prevent ringing.

9.4.2 Layout Example



9-3. Layout Example – TXV0106-Q1

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Understanding Schmitt-Triggers application brief](#)

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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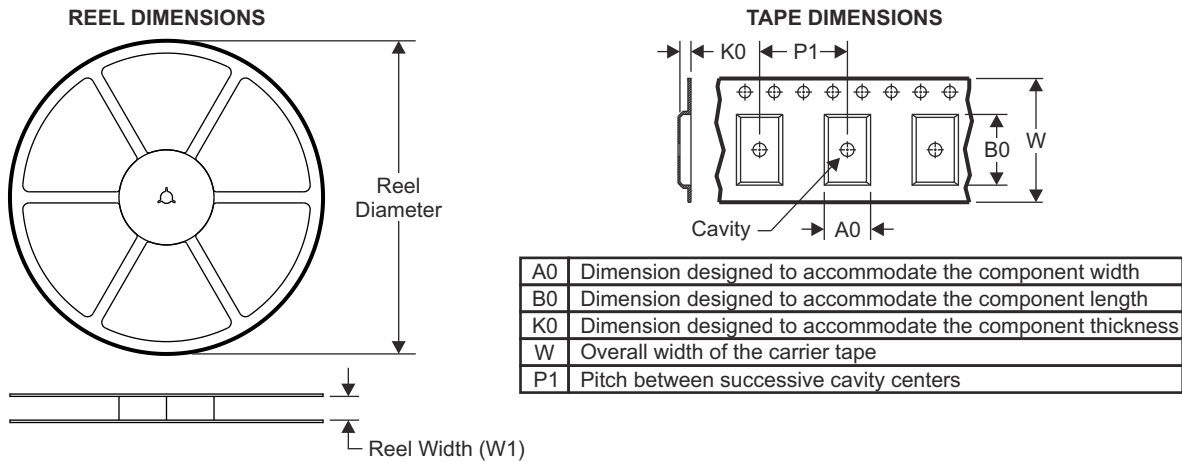
10.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

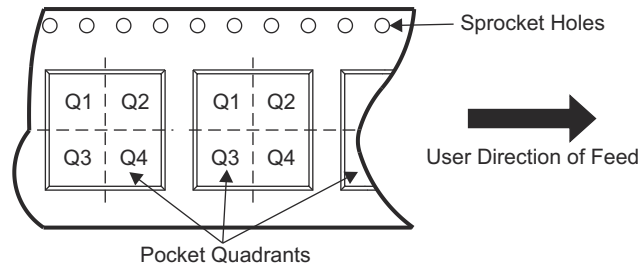
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

11.1 Tape and Reel Information



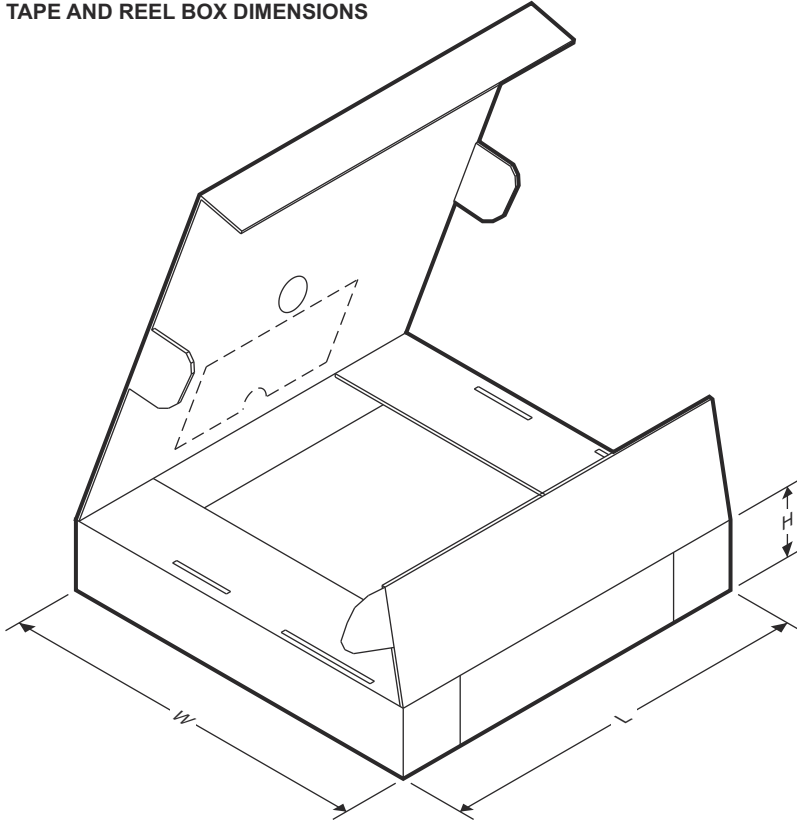
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTXV0106QWBQBRQ1	WQFN	BQB	16	3000	180	12.4	2.8	3.8	1.2	4	12	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTXV0106QWBQBRQ1	WQFN	BQB	16	3000	210	185	35

ADVANCE INFORMATION

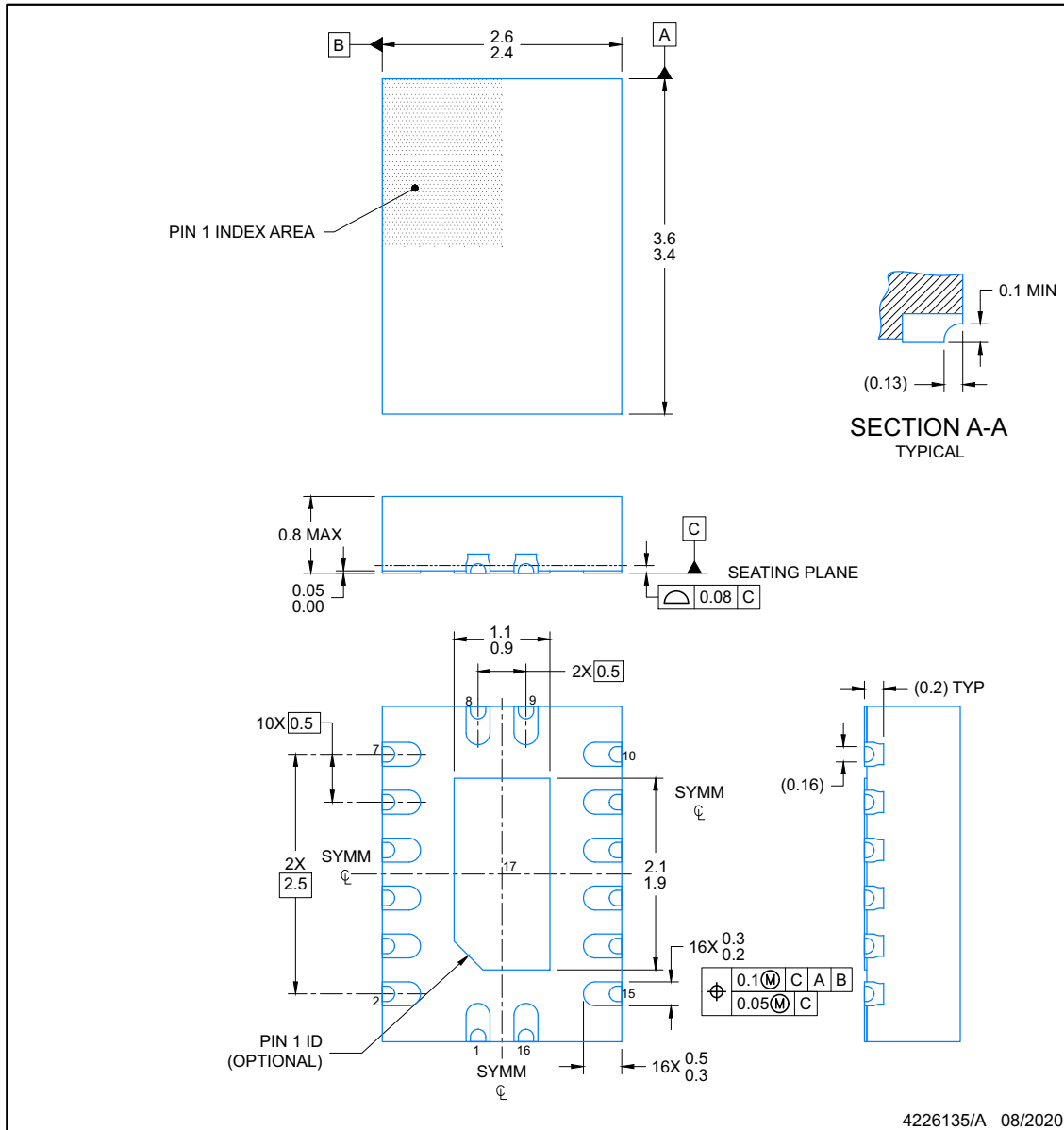
11.2 Mechanical Data

PACKAGE OUTLINE
WQFN - 0.8 mm max height

BQB0016B

INDSTNAME

ADVANCE INFORMATION



NOTES:

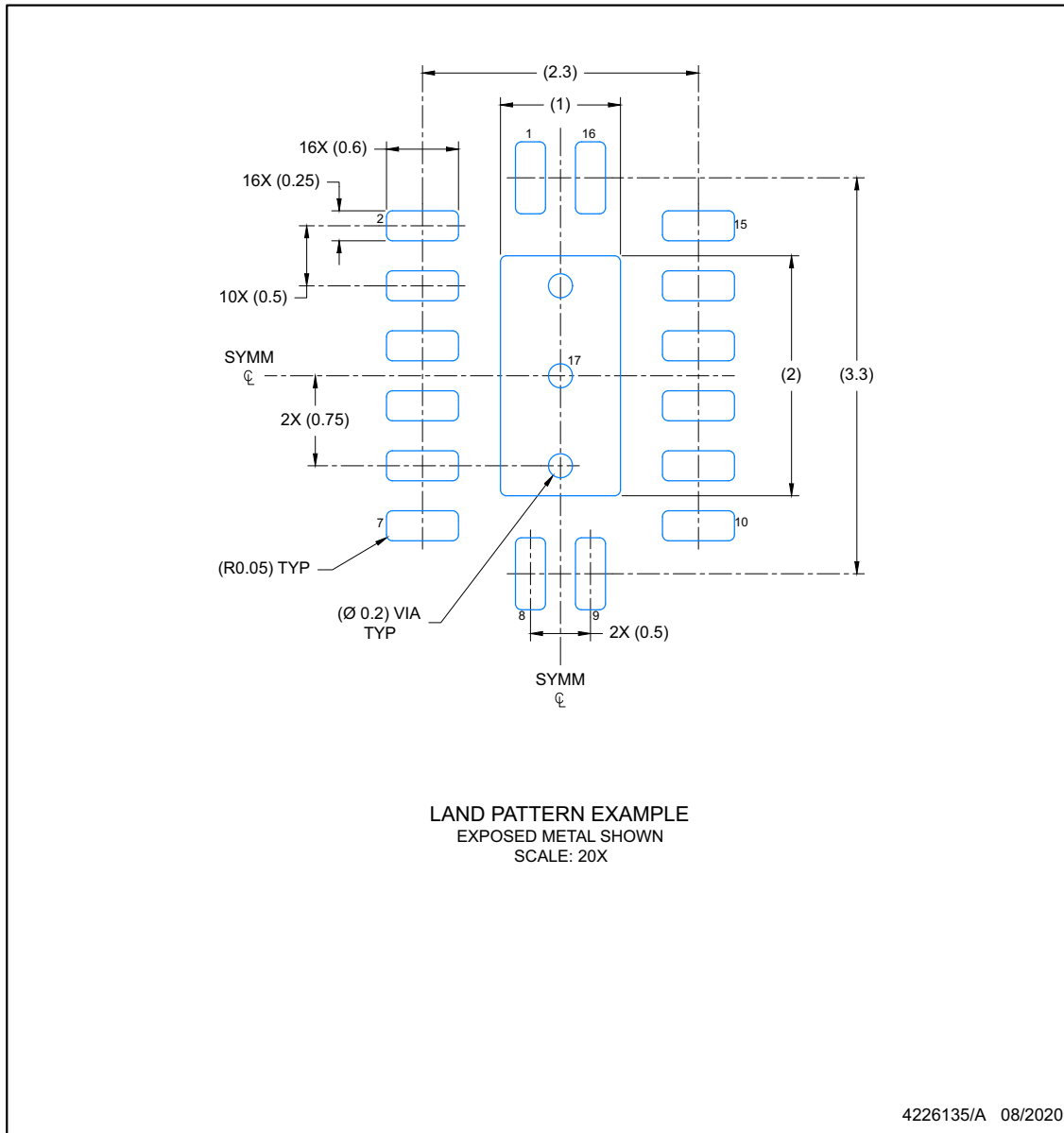
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

BQB0016B

WQFN - 0.8 mm max height

INDSTNAME



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sl原因271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

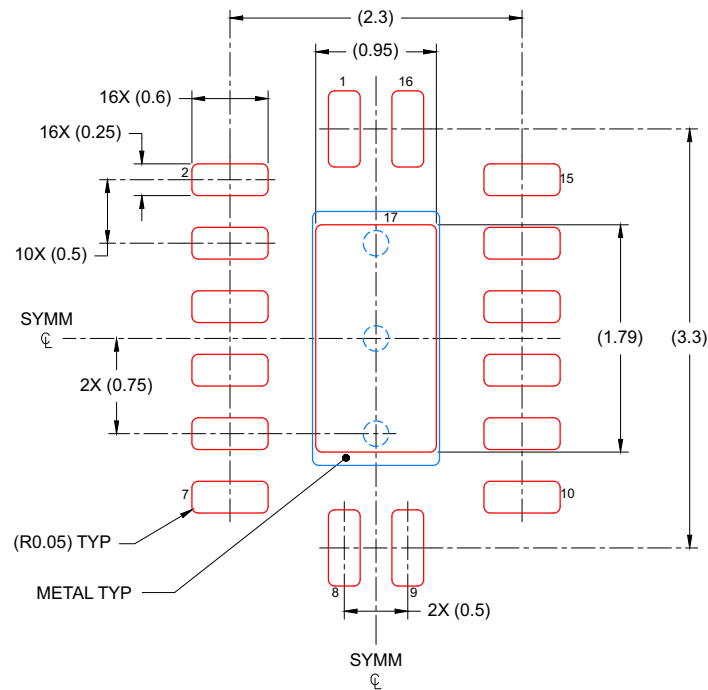
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

BQB0016B

WQFN - 0.8 mm max height

INDSTNAME



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXV0106QWBQRQ1	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TV106Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TXV0106-Q1 :

- Catalog : [TXV0106](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

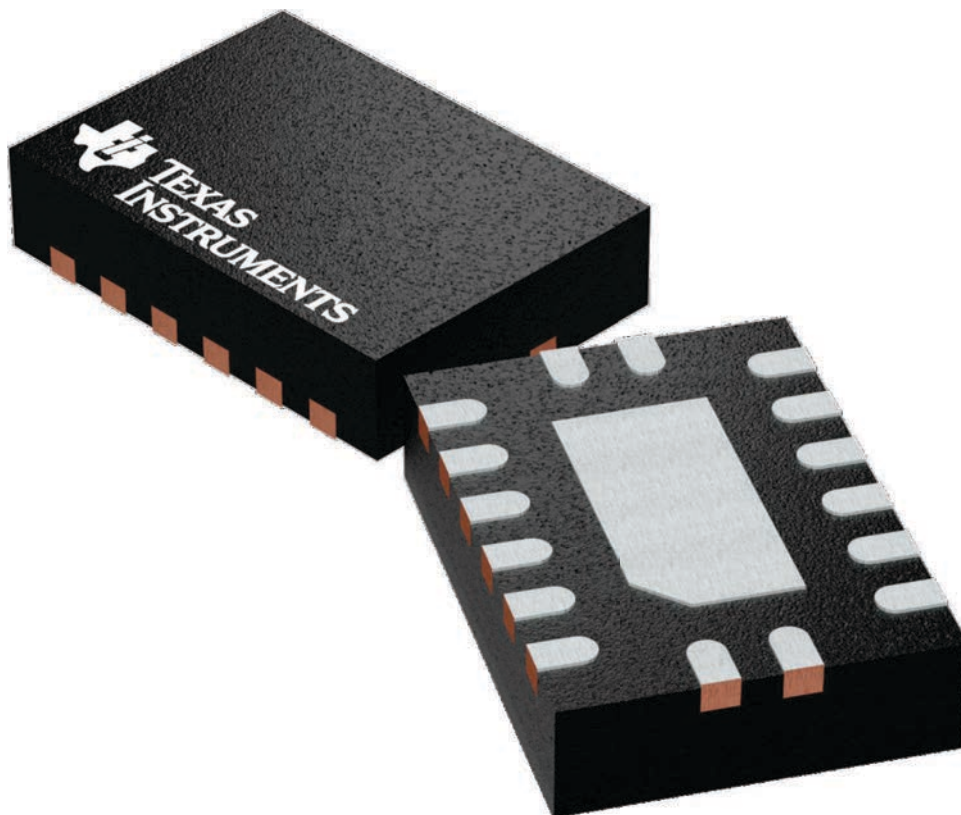
BQB 16

WQFN - 0.8 mm max height

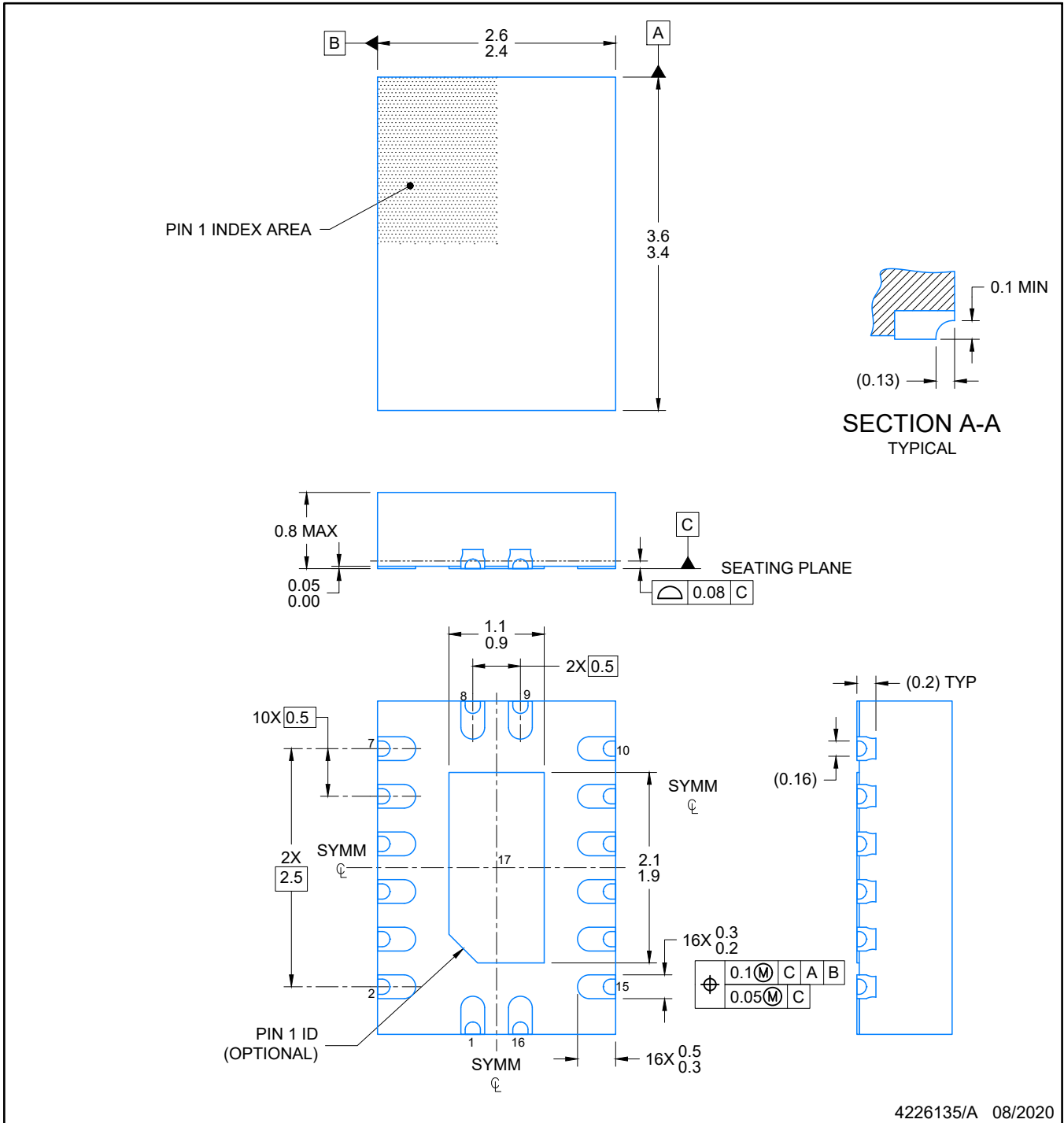
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



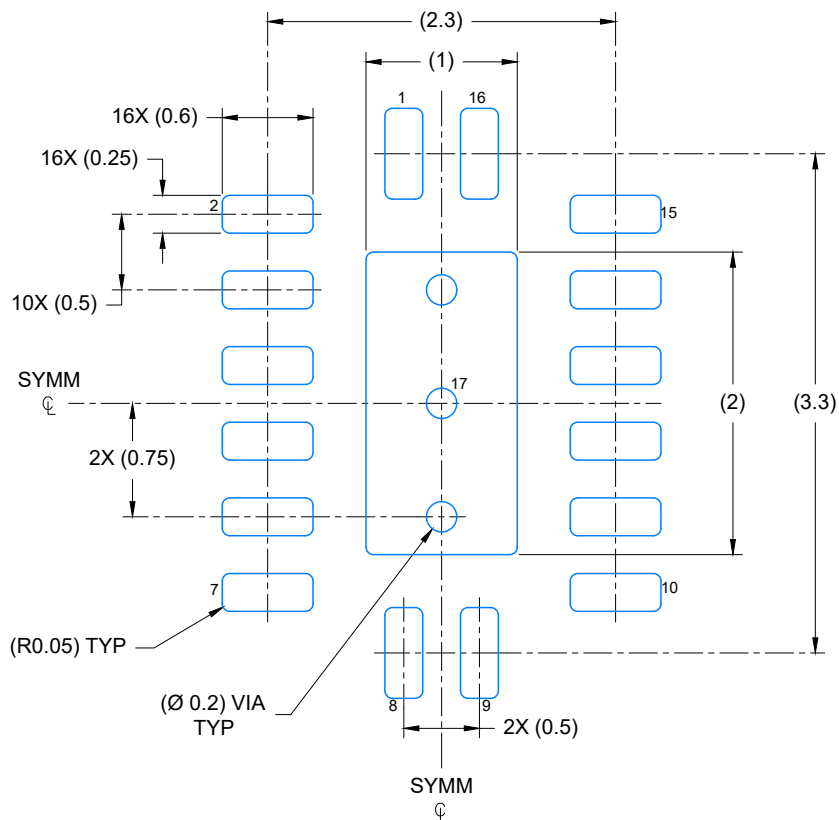
4226161/A



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

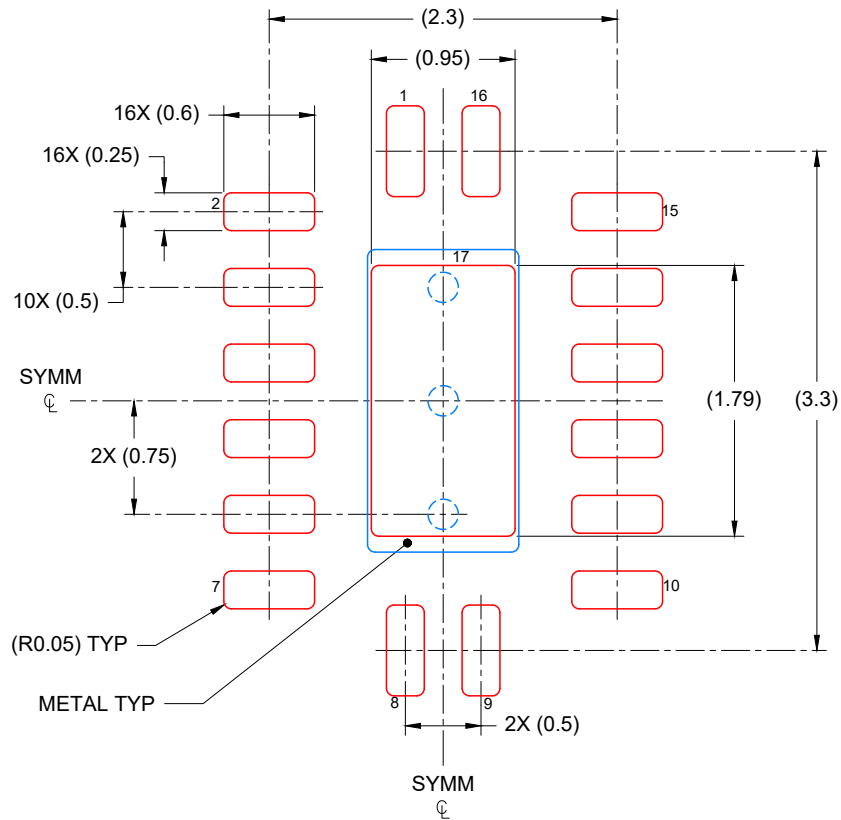


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 85% PRINTED COVERAGE BY AREA
 SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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