UCC14240-Q1 車載用 2.0W、24V V_{IN}、25V V_{OUT}、高密度、>3kV_{RMS}、絶縁型 DC/DC モジュール

1 特長

- 絶縁トランス付きの統合型高密度絶縁型 DC/DC モジュール
- 以下のものを駆動する絶縁型 DC/DC：IGBT、SiC FET
- 入力電圧範囲：21V～27V、絶対最大定格 32V
- T_A ≤ 85℃ で 2.0W、T_A = 105℃ で 1.5W を超える出力電力
- 可変 (VDD – VEE) 出力電圧 (外付け抵抗による)：すべての温度範囲にわたって 18V～25V、±1.3% のレギュレーション精度
- 可変 (COM – VEE) 出力電圧 (外部抵抗による)：すべての温度範囲にわたって 2.5V～(VDD – VEE)、±1.3% のレギュレーション精度
- スペクトラム拡散変調とトランス内蔵の設計により、低い電磁放射を実現
- イネーブル、パワー・グッド、UVLO、OVLO、ソフトスタート、短絡、電力制限、低電圧、過電圧、過熱からの保護
- CMTI > 150kV/μs
- 車載アプリケーション向けに AEC-Q100 認定済み
  - 温度グレード 1：-40℃ ≤ T_J ≤ 150℃
  - 温度グレード 1：-40℃ ≤ T_A ≤ 125℃
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 安全関連の認証計画：
  - DIN EN IEC 60747-17 (VDE 0884-17) に準拠した基本絶縁耐圧：4243V_{PK}
  - UL1577 に準拠した絶縁耐圧：3000V_{RMS} (1 分間)
  - CQC GB4943.1 準拠の基本絶縁
- 36 ピンのワイド SSOP パッケージ

2 アプリケーション

- ハイブリッド、電気自動車、およびパワー・トレーン・システム (EV/HEV)
  - インバータおよびモーター制御
  - オンボード・チャージャ (OBC) およびワイヤレス・チャージャ
  - DC/DC コンバータ
- グリッド・インフラ
  - EV 充電ステーション向け電源モジュール
  - DC 充電 (バッテリ) ステーション
  - ストリング・インバータ
- モーター・ドライブ
  - AC インバータと VF ドライブ、ロボット・サーボ・ドライブ
- 産業用輸送
  - オフハイウェイ車両向け電気式ドライブ

3 概要

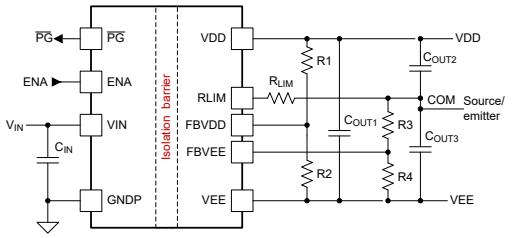
UCC14240-Q1 は、IGBT または SiC ゲート・ドライバへの電力供給を目的として設計された車載用高絶縁電圧 DC/DC 電源モジュールです。UCC14240-Q1 は、独自のアーキテクチャを採用したトランスと DC/DC コントローラを統合しており、非常に低い放射で高効率を実現します。高精度の出力電圧により優れたチャネル拡張を実現し、パワー・デバイスのゲートに過大なストレスを与えずにシステム効率を向上します。

UCC14240-Q1 は、高効率で、最大 2.0W (標準値) の絶縁出力電力を供給します。必要な外付け部品が最小限で、オンチップのデバイス保護機能が内蔵されており、入力低電圧誤動作防止、過電圧誤動作防止、出力電圧パワーグッド・コンパレータ、過熱シャットダウン、ソフトスタート・タイミング、調整可能で絶縁された正負出力電圧、イネーブル・ピン、オープン・ドレイン出力パワーグッド・ピンなどの追加機能を備えています。

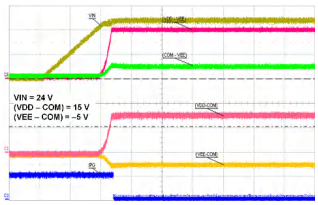
パッケージ情報

発注型番(1)	パッケージ	本体サイズ (公称)
UCC14240QDWNRQ1	DWN (SSOP、36)	12.83mm × 7.50mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション概略



標準的な電源オン・シーケンス

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (December 2022) to Revision C (December 2022)	Page
• Updated table notes	5

Changes from Revision A (November 2021) to Revision B (December 2022)	Page
• ステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

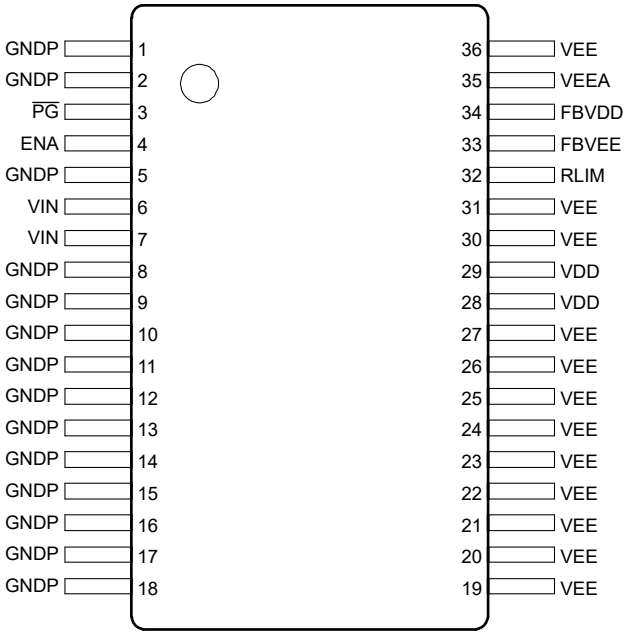


図 5-1. DWN Package, 36-Pin SSOP (Top View)

表 5-1. Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
GNDP	1, 2, 5, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18	G	Primary-side ground connection for VIN. PIN 1,2, and 5 are analog ground. PIN 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, and 18 are power ground. Place several vias to copper pours for thermal relief. See *Layout Guidelines*.
$\overline{PG}$	3	O	Active low power-good open-drain output pin. $\overline{PG}$ remains low when (UVLO ≤ V_{VIN} ≤ OVLO); (UVP1 ≤ (VDD – VEE) ≤ OVP1); (UVP2 ≤ (COM – VEE) ≤ OVP2); $T_{J\_Primary}$ ≤ $TSHUTP_{PRIMARY\_RISE}$; and $T_{J\_secondary}$ ≤ $TSHUT_{SECONDARY\_RISE}$
ENA	4	I	Enable pin. Forcing ENA LOW disables the device. Pull HIGH to enable normal device functionality. 5.5-V recommended maximum.
VIN	6, 7	P	Primary input voltage. PIN 6 is for analog input, and PIN 7 is for power input. For PIN 7, connect one 10-µF ceramic capacitor from power VIN PIN 7 to power GNDP PIN 8. Connect a 0.1-µF high-frequency bypass ceramic capacitor close to PIN 7 and PIN 8. Optionally, connect a 330pF 0402 size high-frequency bypass ceramic capacitor close to analog VIN PIN 6 and GNDP PIN 5.
VEE	19, 20, 21, 22, 23, 24, 25,26, 27, 30,31, 36	G	Secondary-side reference connection for VDD and COM. The VEE pins are used for the high current return paths.
VDD	28, 29	P	Secondary-side isolated output voltage from transformer. Connect a 2.2-µF and a parallel 0.1-µF ceramic capacitor from VDD to VEE. The 0.1-µF ceramic capacitor is the high frequency bypass and must be next to the IC pins. A 4.7-µF or 10-µF ceramic capacitor can be used instead of 2.2 to further reduce the output ripple voltage.
RLIM	32	P	Secondary-side second isolated output voltage resistor to limit the source current from VDD to COM node, and the sink current from COM to VEE. Connect a resistor from RLIM to COM to regulate the (COM – VEE) voltage. See R_{LIM} *Resistor Selection* for more detail.
FBVEE	33	I	Feedback (COM – VEE) output voltage sense pin used to adjust the output (COM – VEE) voltage. Connect a resistor divider from COM to VEE so that the midpoint is connected to FBVEE, and the equivalent FBVEE voltage when regulating is 2.5 V. Add a 330-pF ceramic capacitor for high frequency decoupling in parallel with the low-side feedback resistor. The 330-pF ceramic capacitor for high frequency bypass must be next to the FBVEE and VEEA IC pins on top layer or back layer connected with vias.

表 5-1. Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
FBVDD	34	I	Feedback (VDD – VEE) output voltage sense pin and to adjust the output (VDD – VEE) voltage. Connect a resistor divider from VDD to VEE so that the midpoint is connected to FBVDD, and the equivalent FBVDD voltage when regulating is 2.5 V. Add a 330-pF ceramic capacitor for high frequency decoupling in parallel with the low-side feedback resistor. The 330-pF ceramic capacitor for high frequency bypass must be next to the FBVDD and VEEA IC pins on top layer or back layer connected with vias.
VEEA	35	G	Secondary-side analog sense reference connection for the noise sensitive analog feedback inputs, FBVDD and FBVEE. Connect the low-side feedback resistors and high frequency decoupling filter capacitor close to the VEEA pin and respective feedback pin FBVDD or FBVEE. Connect to secondary-side gate drive lowest voltage reference, VEE. Use a single point connection and place the high frequency decoupling ceramic capacitor close to the VEEA pin. See *Layout Guidelines*.

(1) P = power, G = ground, I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		MIN	TYP	MAX	UNIT
	VIN to GNDP	–0.3		32	V
	ENA, $\overline{PG}$ to GNDP	–0.3		7	V
	VDD, RLIM, FBVDD, FBVEE to VEE	–0.3		32	V
P_{LOSS_MAX}	Total power loss at T_A=25°C			2.45	W
$P_{OUT\_VDD\_MAX}$	Total (VDD – VEE) output power at T_A=25°C			2.5	W
$I_{RLIM\_MAX\_RMS\_SOURCE}$	Max RLIM pin rms current sourcing from VDD to RLIM. (16% average run time over lifetime of 24,500 hr)			0.125	A_{RMS}
$I_{RLIM\_MAX\_RMS\_SINK}$	Max RLIM pin rms current sinking from RLIM to VEE. (16% average run time over lifetime of 24,500 hr)			0.125	A_{RMS}
T_J	Operating junction temperature range	–40		150	°C
T_{stg}	Storage temperature	–65		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011 Section 7.2	±500	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PIN		MIN	TYP	MAX	UNIT
V_{VIN}	Primary-side input voltage to GNDP	21	24	27	V
V_{ENA}	Enable to GNDP	0		5.5	V
$V_{\overline{PG}}$	Powergood to GNDP	0		5.5	V
V_{VDD}	VDD to VEE	18		25	V
V_{VEE}	COM to VEE	2.5		VDD – VEE	V
V_{FBVDD}, V_{FBVEE}	FBVDD, FBVEE to VEE	0	2.5	5.5	V
T_A	Ambient temperature	–40		125	°C
T_J	Junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		DWN (SSOP) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.9	°C/W

THERMAL METRIC(1)		DWN (SSOP) 36 PINS	UNIT
Ψ_{JT}	Junction-to-top characterization parameter	16.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	25.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

V_{VIN} = 24 V, C_{IN} = 10µF, C_{OUT} = 2.2 uF, T_J = 150 °C, V_{ENA} = 5 V

PARAMETER		TEST CONDITIONS	TYP VALUE	UNIT
P_D	Power dissipation	(VDD – VEE) = 25 V, $P_{VDD-VEE}$ = 2 W; (COM – VEE) = 5 V, No Load from (VDD - COM) or (COM - VEE)	1.65	W

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
General				
CLR	External clearance (1)	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External creepage (1)	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance – transformer power isolation)	> 120	µm
		Minimum internal gap (internal clearance – capacitive signal isolation)	> 8.6	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 300 VRMS	I-IV	
		Rated mains voltage ≤ 600 VRMS	I-IV	
		Rated mains voltage ≤ 1000 VRMS	I-III	
DIN EN IEC 60747-17 (VDE 0884-17) (Planned Certification Targets) (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1202	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	850	V_{RMS}
		DC voltage	1202	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60s (qualification);V_{TEST} = 1.2 × V_{IOTM} , t = 1 s (100% production)	4243	V_{PK}
V_{IMP}	Maximum impulse voltage (3)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (3)	Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	6500	V_{PK}
qpd	Apparent charge (4)	Method a, After Input/Output safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method a, After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.3 × V_{IORM}, t_m = 10 s	≤ 5	pC
		Method b1: At routine test (100% production) and preconditioning (type test); V_{ini} = 1.2 x V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.5 x V_{IORM}, t_m = 1 s	≤ 5	pC
C_{IO}	Barrier capacitance, input to output (5)	V_{IO} = 0.4 sin (2πft), f = 1 MHz	< 3.5	pF

PARAMETER		TEST CONDITIONS	VALUE	UNIT
R_{IO}	Isolation resistance, input to output (5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	> 10^{11}	Ω
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577 (Planned Certification Target)				
V_{ISO}	Withstand isolation voltage	Withstand isolation voltage V_{TEST} = V_{ISO} = 3000 V_{RMS}, t = 60s (qualification) V_{TEST} = 1.2 × V_{ISO} = 3600 V_{RMS}, t = 1 s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed-circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device

6.7 Safety-Related Certifications

VDE	UL	CQC
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify under UL 1577 Component Recognition Program	Plan to certify according to GB4943.1
Basic insulation Maximum transient isolation voltage, 4243 V_{PK}; Maximum repetitive peak isolation voltage, 1202 V_{PK}; Maximum surge isolation voltage, 6500 V_{PK}	Single protection, 3000 V_{RMS}	Basic insulation, Altitude ≤ 5000 m, Tropical Climate, 595 V_{RMS} maximum working voltage
Certificate number: (planned)	File number: (planned)	Certificate number: (planned)

6.8 Electrical Characteristics

Over operating temperature range (–40 °C ≤ T_J ≤ 150 °C, 21 V ≤ V_{VIN} ≤ 27 V, C_{IN} = 10µF, C_{OUT} = 2.2 µF, V_{ENA} = 5 V, R_{LIM} = 1 kΩ, unless otherwise noted. All typical values at T_A = 25 °C and V_{VIN} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY (Primary-side. All voltages with respect to GNDP)						
V_{VIN}	Input voltage range	Primary-side input voltage to GNDP	21	24	27	V
I_{VINQ_OFF}	VIN quiescent current, disabled	V_{ENA}=0 V; V_{VIN} = 21 V - 27 V			700	µA
$I_{VIN\_ON\_NO\_LOAD}$	VIN operating current, enabled, No Load	V_{ENA} = 5 V; V_{VIN} = 21 V - 27 V; (VDD – VEE) = 25-V regulating; $I_{VDD-VEE}$ = 0 mA			35	mA
$I_{VIN\_ON\_FULL\_LOAD}$	VIN operating current, enabled, Full Load	V_{ENA}=5 V; V_{VIN} = 21 V - 27 V; (VDD – VEE) = 25-V regulating; $I_{VDD-VEE}$ = 60 mA			250	mA
UVLOP COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VIN\_ANALOG\_UVLOP\_RISING}$	VIN analog undervoltage lockout rising threshold		8	9	10	V
$V_{VIN\_ANALOG\_UVLOP\_FALLING}$	VIN analog undervoltage lockout falling threshold		7	8	9	V
$V_{VIN\_UVLOP\_RISING}$	VIN undervoltage lockout rising threshold		19	20	21	V
$V_{VIN\_UVLOP\_FALLING}$	VIN undervoltage lockout falling threshold		17.1	18	18.9	V

Over operating temperature range (–40 °C ≤ T_J ≤ 150 °C, 21 V ≤ V_{VIN} ≤ 27 V, C_{IN} = 10µF, C_{OUT} = 2.2 µF, V_{ENA} = 5 V, R_{LIM} = 1 kΩ, unless otherwise noted. All typical values at T_A = 25 °C and V_{VIN} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVLO COMPARATOR (Primary-side. All voltages with respect to GNDP)						
$V_{VIN\_OVLO\_RISE}$	VIN overvoltage lockout rising threshold		29.45	31	32.55	V
$V_{VIN\_OVLO\_FALLING}$	VIN overvoltage lockout falling threshold		27.55	29	30.45	V
THERMAL SHUTDOWN COMPARATOR (Primary-side)						
$TSHUTP_{PRIMARY\_RISE}$	Primary-side over-temperature shutdown rising threshold (1)	First time at power-up Tj needs to be < 130 °C to turn on	140	150	160	°C
$TSHUTP_{PRIMARY\_HYST}$	Primary-side over-temperature shutdown hysteresis (1)		15	20	25	°C
ENA INPUT PIN (Primary-side. All voltages with respect to GNDP)						
V_{EN_IR}	Input voltage rising threshold, logic HIGH	Rising edge			2.1	V
V_{EN_IF}	Input voltage falling threshold, logic LOW	Falling edge	0.8			V
I_{EN}	Enable Pin Input Current	V_{ENA} = 5.0 V		5	10	µA
$\overline{PG}$ OPEN-DRAIN OUTPUT PIN (Primary-side. All voltages with respect to GNDP)						
$V_{\overline{PG}\_OUT\_LO}$	$\overline{PG}$ output-low saturation voltage	Sink Current = 5 mA, power good			0.5	V
$I_{\overline{PG}\_OUT\_HI}$	$\overline{PG}$ Leakage current	$V_{\overline{PG}}$ = 5.5 V, power not good			5	µA
F_{SW}	Switching frequency	V_{VIN} = 24 V; V_{ENA} = 5 V; (VDD-VEE) = 25 V	11	13	15	MHz
F_{SSM}	Frequency of Spread Spectrum Modulation (SSM) triangle waveform	Only during primary-side startup starting after VIN > UVLOP, and ENA = HIGH; $F_{SS\_BURST\_P}$ = 1/8 µs = 125 kHz		90		kHz
SSM Percentage change of $F_{CARRIER}$	SSM Percent change of carrier frequency during Spread Spectrum Modulation (SSM) by triangle waveform	Only during primary-side startup starting after VIN > UVLOP, and ENA = HIGH; $F_{SS\_BURST\_P}$ = 1/8 µs = 125 kHz		5		%
$t_{SOFT\_START\_TIME\_OUT}$	Primary-side soft-start time-out	Timer begins when VIN > UVLOP and ENA = High and reset when Powergood pin indicates Good		16		ms
VDD OUTPUT VOLTAGE (Secondary-side. All voltages with respect to VEE)						
V_{VDD_RANGE}	(VDD – VEE) Output voltage range		18		25	V
$V_{VDD\_DC\_ACCURACY}$	(VDD – VEE) Output voltage DC regulation accuracy	Secondary-side (VDD – VEE) output voltage, over load, line and temperature range, externally adjust with external resistor divider	-1.3		1.3	%
VDD REGULATION HYSTERETIC COMPARATOR (Secondary-side. All voltages with respect to VEE)						
V_{FBVDD_REF}	Feedback regulation reference voltage for (VDD – VEE)	(VDD – VEE) output in regulation	2.4675	2.5	2.5325	V
V_{FBVDD_HYST}	FBVDD Hysteresis comparator hysteresis settings. Hysteresis at the FBVDD pin. [The (VDD-VEE) hysteresis would amplify this FBVDD hysteresis by the feedback resistor divider gain.]		9	10	12.3	mV
COM OUTPUT VOLTAGE (Secondary-side. All voltages with respect to VEE)						
V_{VEE_RANGE}	(COM – VEE) Output voltage range		2.5		(VDD – VEE)	V

Over operating temperature range (–40 °C ≤ T_J ≤ 150 °C, 21 V ≤ V_{VIN} ≤ 27 V, C_{IN} = 10µF, C_{OUT} = 2.2 µF, V_{ENA} = 5 V, R_{LIM} = 1 kΩ, unless otherwise noted. All typical values at T_A = 25 °C and V_{VIN} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VEE\_DC\_ACCURACY}$	(COM – VEE) Output voltage DC regulation accuracy	Secondary-side (COM – VEE) output voltage, over load, line and temperature range, externally adjust with external resistor divider	–1.3		1.3	%
COM REGULATION HYSTERETIC COMPARATOR (Secondary-side. All voltages with respect to VEE)						
V_{FBVEE_REF}	Feedback regulation reference voltage for (COM – VEE)	(COM – VEE) output in regulation	2.4675	2.5	2.5325	V
$V_{RLIM\_SHORT\_CHRG\_CMP\_RISE}$	RLIM pin Short Charge comparator rising threshold to exit PWM	Rising threshold		0.73		V
$t_{RLIM\_SHORT\_CHRG\_ON\_TIME}$	On-Time during RLIM pin Short Charge PWM mode	RLIM pin < 0.645 V, while FBVEE pin < 2.48 V		1.2		us
$t_{RLIM\_SHORT\_CHRG\_OFF\_TIME}$	Off-Time during RLIM pin Short Charge PWM mode	RLIM pin < 0.645 V, while FBVEE pin < 2.48 V		5		us
UVLOS COMPARATOR (Secondary-side. All voltages with respect to VEE)						
$V_{VDD\_UVLO\_RISE}$	(VDD – VEE) undervoltage lockout rising threshold	Voltage at FBVDD		0.9		V
$V_{VDD\_UVLO\_HYST}$	(VDD – VEE) undervoltage lockout hysteresis	Voltage at FBVDD		0.2		V
OVLOS COMPARATOR (Secondary-side. All voltages with respect to VEE)						
$V_{VDD\_OVLOS\_RISE}$	(VDD – VEE) overvoltage lockout rising threshold	Voltage from VDD to VEE, rising	29.45	31	32.55	V
$V_{VDD\_OVLOS\_FALLING}$	(VDD – VEE) overvoltage lockout falling threshold	Voltage from VDD to VEE, falling	27.55	29	30.45	V
SOFT-START (Secondary-side. All voltages with respect to VEE)						
VREF_Voltage_per_Steps	Voltage per step	7 Steps of 200mV each, starting from 1.3V and ending at 2.5V.		0.2		V
VREF_Voltage_Start	VREF voltage at Start of secondary-side soft-start	7 Steps of 200mV each, starting from 1.3V and ending at 2.5V.		1.3		V
VREF_Voltage_End	VREF voltage at End of secondary-side soft-start	7 Steps of 200mV each, starting from 1.3V and ending at 2.5V.		2.5		V
UVP1, (VDD – VEE) UNDER -VOLTAGE PROTECTION COMPARATOR (Secondary-side. All voltages with respect to VEE)						
$V_{VDD\_UVP\_RISE}$	(VDD – VEE) under-voltage protection rising threshold, $V_{UVP} = V_{REF} \times 90\%$		2.175	2.25	2.35	V
$V_{VDD\_UVP\_HYST}$	(VDD – VEE) undervoltage protection hysteresis			20		mV
OVP1, (VDD – VEE) OVER-VOLTAGE PROTECTION COMPARATOR (Secondary-side. All voltages with respect to VEE)						
$V_{VDD\_OVP\_RISE}$	(VDD – VEE) over-voltage protection rising threshold, $V_{OVP} = V_{REF} \times 110\%$		2.7	2.75	2.825	V
$V_{VDD\_OVP\_HYST}$	(VDD – VEE) overvoltage protection hysteresis			20		mV
UVP2, (COM – VEE) UNDER -VOLTAGE PROTECTION COMPARATOR (Secondary-side. All voltages with respect to VEE)						
$V_{VEE\_UVP\_RISE}$	(COM – VEE) under-voltage protection rising threshold, $V_{UVP} = V_{REF} \times 90\%$		2.1	2.25	2.4	V
$V_{VEE\_UVP\_HYST}$	(COM – VEE) undervoltage protection hysteresis			20		mV
OVP2, (COM – VEE) OVER-VOLTAGE PROTECTION COMPARATOR (Secondary-side. All voltages with respect to VEE)						
$V_{VEE\_OVP\_RISE}$	(COM – VEE) over-voltage protection rising threshold, $V_{OVP} = V_{REF} \times 110\%$		2.7	2.75	2.825	V
$V_{VEE\_OVP\_HYST}$	(COM – VEE) over-voltage protection hysteresis			20		mV
THERMAL SHUTDOWN COMPARATOR (Secondary-side)						

Over operating temperature range (–40 °C ≤ T_J ≤ 150 °C, 21 V ≤ V_{VIN} ≤ 27 V, C_{IN} = 10µF, C_{OUT} = 2.2 µF, V_{ENA} = 5 V, R_{LIM} = 1 kΩ, unless otherwise noted. All typical values at T_A = 25 °C and V_{VIN} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$TSHUTS_{SECONDARY\_RISE}$	Secondary -side over-temperature shutdown rising threshold (1)	First time at power-up Tj needs to be < 130ºC to turnon.	145	150	155	°C
$TSHUTS_{SECONDARY\_HYST}$	Secondary-side over-temperature shutdown hysteresis (1)		15	20	25	°C
CMTI (Common Mode Transient Immunity)						
CMTI	Common Mode Transient Immunity	Positive VEE with respect to GNDP	150			V/ns
		Negative VEE with respect to GNDP			–150	V/ns
INTEGRATED TRANSFORMER (Primary-side to Secondary-side)						
N	Transformer effective turns ratio	Secondary side to primary side		1.18		-

(1) Functionality tested in production. MIN, TYP, MAX ensured by characterization.

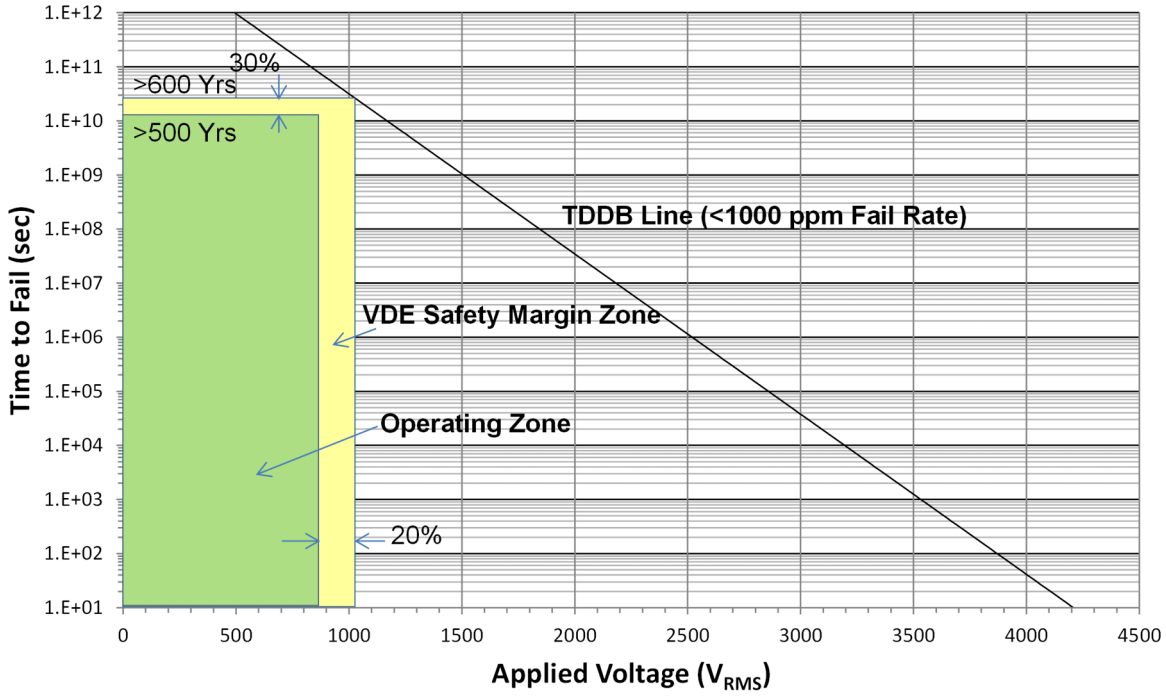
6.9 Safety Limiting Values

PARAMETER		TEST CONDITIONS	MAX	UNIT
I_S	Safety input rms current (VDD-VEE)	$R_{\theta JA}$ = 52.3 °C/W, V_{VIN} = 27 V, T_J = 150 °C, T_A = 25 °C, P_{OUT} = 2 W (1) (2)	150	mA
		$R_{\theta JA}$ = 52.3 °C/W, V_{VIN} = 21 V, T_J = 150 °C, T_A = 25 °C, P_{OUT} = 2 W (1) (2)	200	mA
P_S	Safety power dissipation (input power - output power)	$R_{\theta JA}$ = 52.3 °C/W, T_J = 150 °C, T_A = 25 °C (1) (2)	2.39	W
T_S	Safety temperature	(1) (2)	150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and PS should not be exceeded. These limits vary with the ambient temperature, T_A.

(2) The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: $T_J = T_A + R_{qJA} \times P$, where P is the power dissipated in the device. $T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature. $P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.10 Insulation Characteristics



Working Isolation Voltage = 850V_{RMS}
T_A up to 150 °C

Projected Insulation Lifetime = 270 Years
Applied Voltage Frequency = 60 Hz

図 6-1. TDDB: Insulation Lifetime Projection for 850 Vrms Working Voltage.

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For basic insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1000 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE basic certification requires additional safety margin of 20% for working voltage and 30% for lifetime which translates into minimum required insulation lifetime of 26 years at a working voltage that's 20% higher than the specified value. The TDDB projection line shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 850 V_{RMS} with a lifetime of 270 years.

6.11 Typical Characteristics

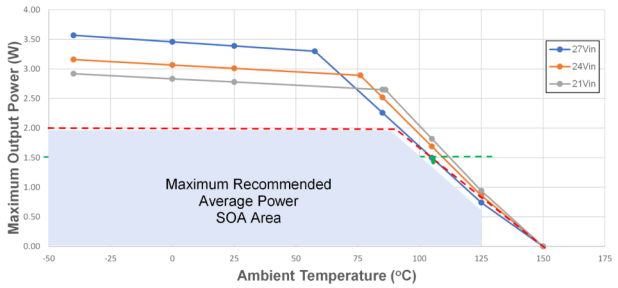


図 6-2. SOA Derating Curves: $V_{VDD-VEE}$ = 18 V, $V_{COM-VEE}$ = 5 V, No Load.

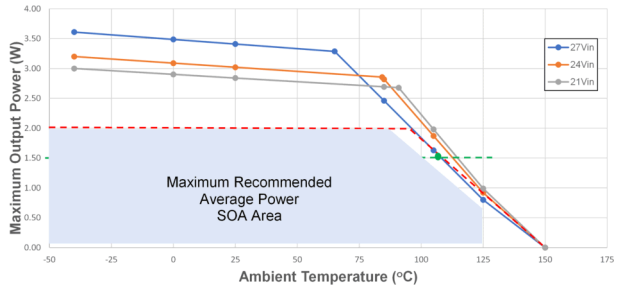


図 6-3. SOA Derating Curves: $V_{VDD-VEE}$ = 20 V, $V_{COM-VEE}$ = 5 V, No Load

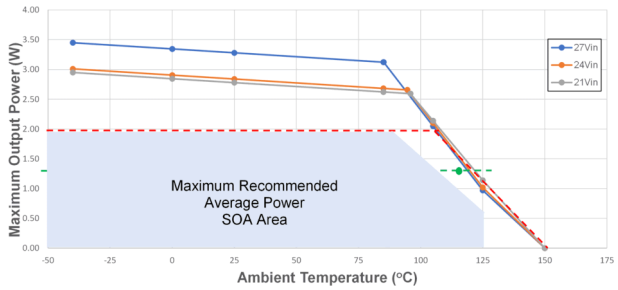


図 6-4. SOA Derating Curves: $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V, No Load

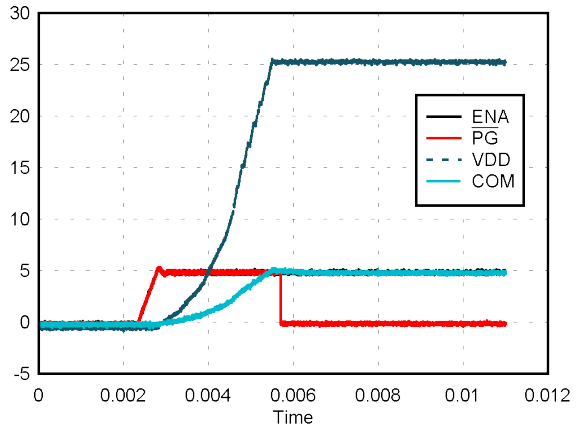


図 6-5. Start-up: VIN = 24 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V, No Load

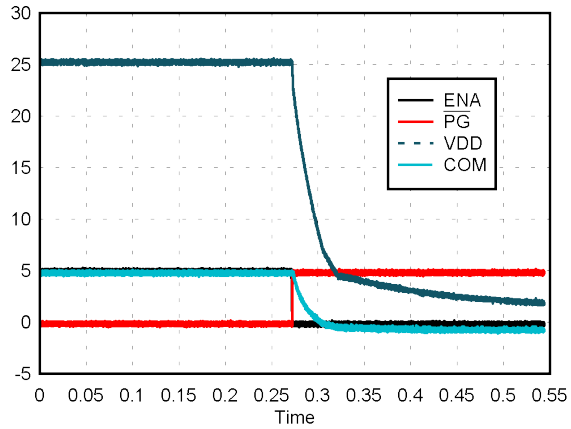


図 6-6. Shutdown: VIN = 24 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V, No Load

6.11 Typical Characteristics (continued)

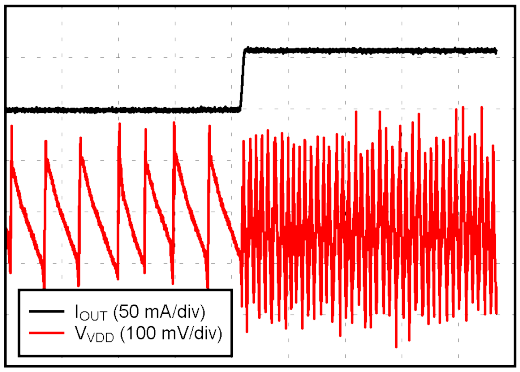


図 6-7. Load Transient Response: No Load to 1 W, VIN = 24 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V

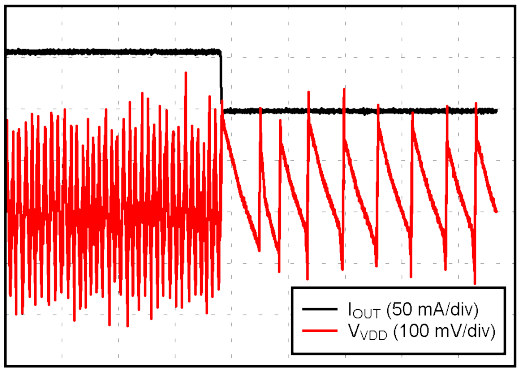


図 6-8. Load Transient Response: 1 W to No Load, VIN = 24 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V

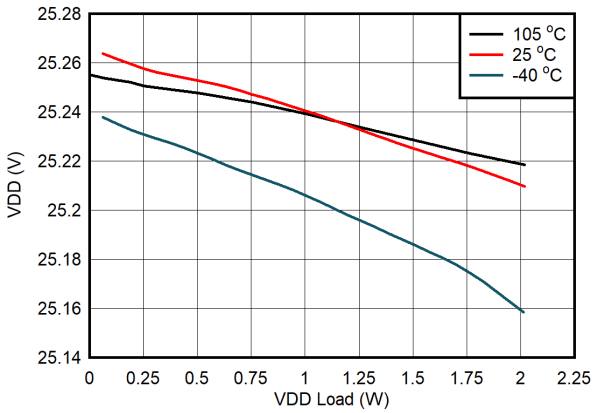


図 6-9. $V_{VDD-VEE}$ Load Regulation: VIN = 21 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V

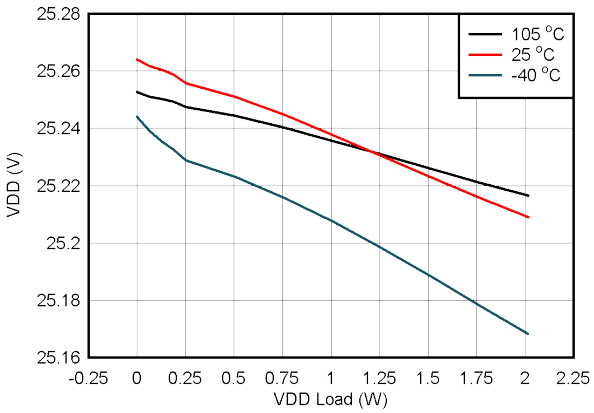


図 6-10. $V_{VDD-VEE}$ Load Regulation: VIN = 24 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V

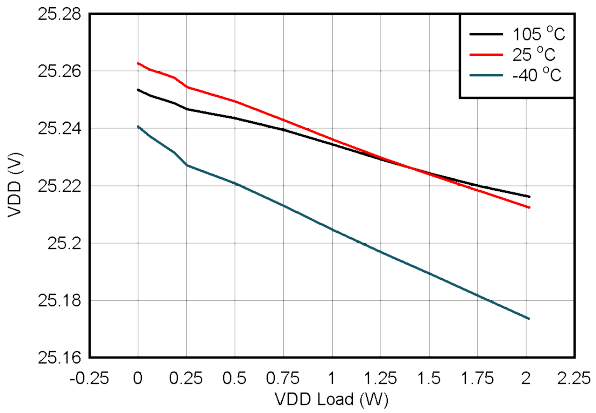


図 6-11. $V_{VDD-VEE}$ Load Regulation: VIN = 27 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V

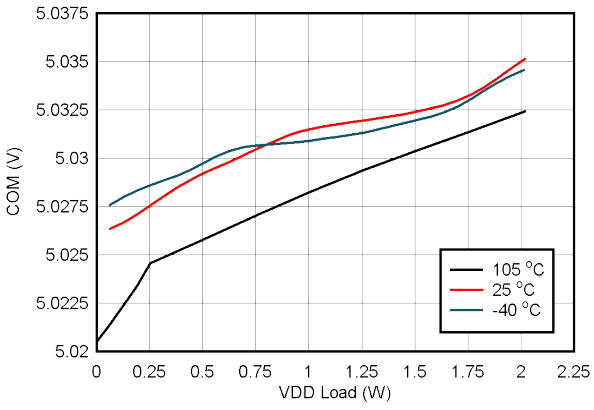


図 6-12. $V_{COM-VEE}$ Load Regulation: VIN = 21 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V

6.11 Typical Characteristics (continued)

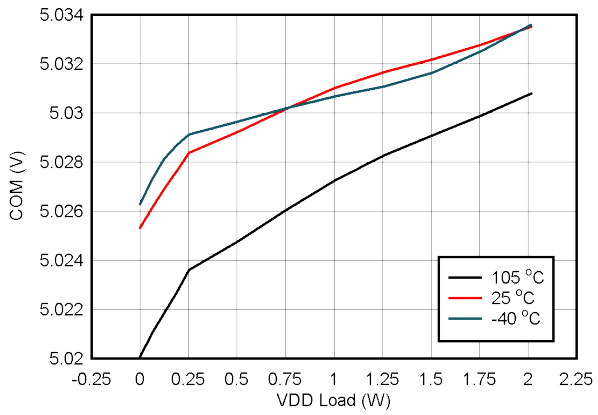


図 6-13. $V_{COM-VEE}$ Load Regulation: VIN = 24 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V

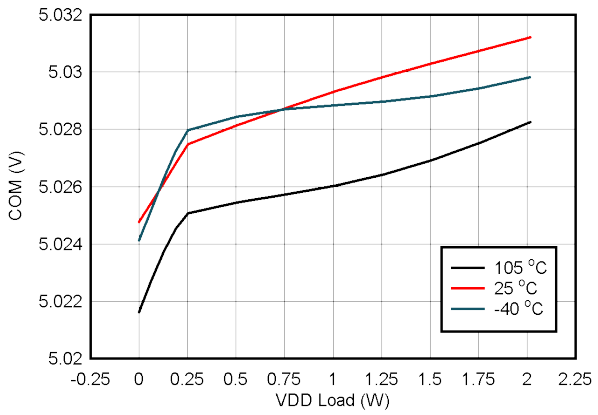


図 6-14. $V_{COM-VEE}$ Load Regulation: VIN = 27 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V

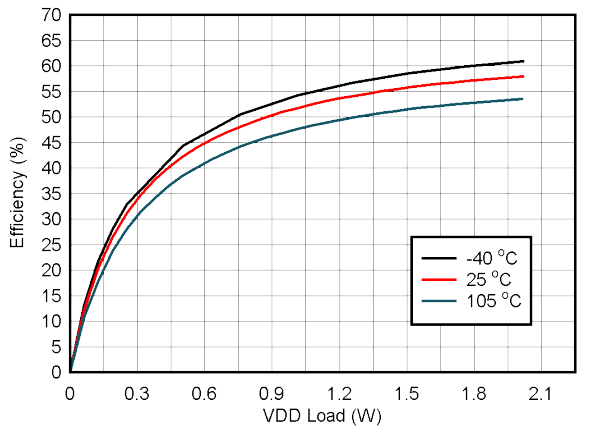


図 6-15. Efficiency vs Load on $V_{VDD-VEE}$: VIN = 21 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V, No Load on $V_{COM-VEE}$

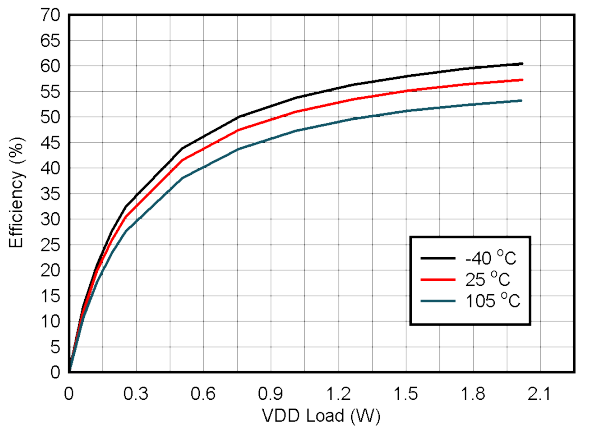


図 6-16. Efficiency vs Load on $V_{VDD-VEE}$: VIN = 24 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V, No Load on $V_{COM-VEE}$

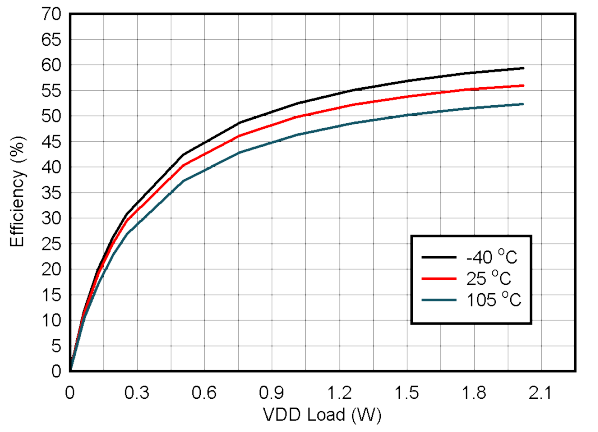


図 6-17. Efficiency vs Load on $V_{VDD-VEE}$: VIN = 27 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V, No Load on $V_{COM-VEE}$

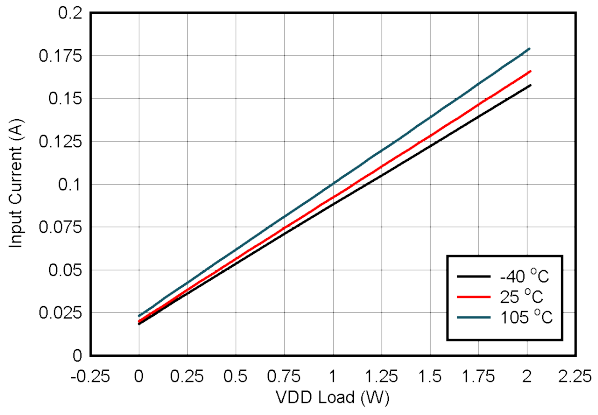


図 6-18. Input Current vs Load on $V_{VDD-VEE}$: VIN = 21 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V, No Load on $V_{COM-VEE}$

6.11 Typical Characteristics (continued)

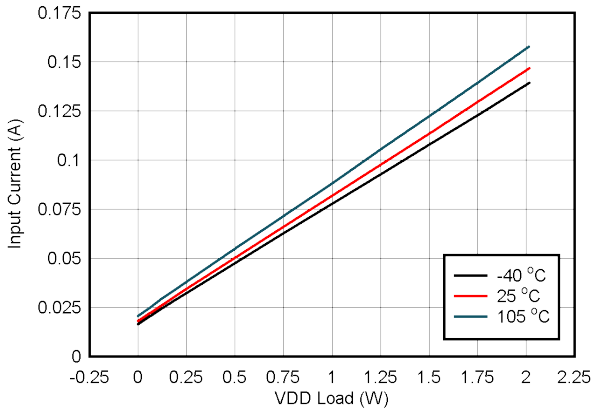


図 6-19. Input Current vs Load on $V_{VDD-VEE}$: VIN = 24 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V, No Load on $V_{COM-VEE}$

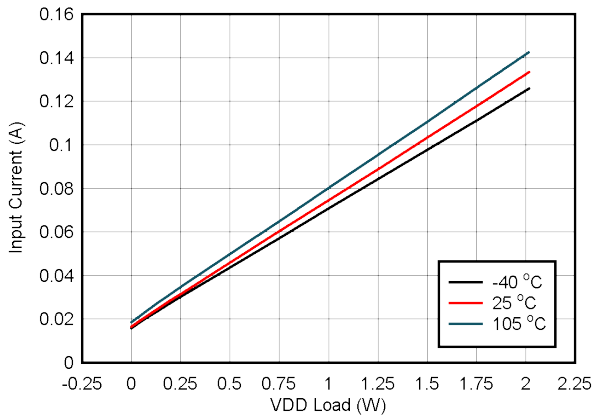


図 6-20. Input Current vs Load on $V_{VDD-VEE}$: VIN = 27 V, $V_{VDD-VEE}$ = 25 V, $V_{COM-VEE}$ = 5 V, No Load on $V_{COM-VEE}$

7 Detailed Description

7.1 Overview

UCC14240-Q1 device is suitable for applications that have limited board space and require more integration. These devices are also suitable for very-high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive. The low-profile, low-center of gravity, and low weight provides a higher vibration tolerance than systems using large bulky transformers. The device is easy-to-use and provides flexibility to adjust both positive and negative output voltages as needed when optimizing the gate voltage for maximum efficiency while protecting gate oxide from over-stress with its tight voltage regulation accuracy.

The device integrates a high-efficiency, low-emissions isolated DC/DC converter for powering the gate drive of SiC or IGBT power devices in traction inverter motor drives, industrial motor drives, or other high voltage DC/DC converters. This DC/DC converter provides greater than 1.5 W of power.

The integrated DC/DC converter uses switched mode operation and proprietary circuit techniques to reduce power losses and boost efficiency. Specialized control mechanisms, clocking schemes, and the use of an on-chip transformer provide high efficiency and low radiated emissions.

The integrated transformer provides power delivery throughout a wide temperature range while maintaining a 3000-V_{RMS} isolation, and an 850-V_{RMS} continuous working voltage. The low isolation capacitance of the transformer provides high CMTI allowing fast dv/dt switching and higher switching frequencies, while emitting less noise.

The V_{VIN} supply is provided to the primary-side power controller that switches the input stage connected to the integrated transformer. Power is transferred to the secondary-side output stage, and regulated to a level set by the resistor divider connected between the (VDD – VEE) pin and the FBVDD pin with respect to the VEE pin. The output voltage is adjustable with external resistor divider allowing a wide (VDD – VEE) range.

For optimal performance ensure to maintain the V_{VIN} input voltage within the recommended operating voltage range. Do not exceed the absolute maximum voltage rating to avoid over-stressing the input pins.

A fast hysteretic feedback burst control loop monitors (VDD – VEE) and ensures the output voltage is kept within the hysteresis with low overshoots and undershoots during load and line transients. The burst control loop enables efficient operation across full load and allows a wide VOUT adjustability throughout the whole V_{VIN} range. The undervoltage lockout (UVLO) protection monitors the input voltage pin, VIN, with hysteresis and input filter ensuring robust system performance under noisy conditions. The overvoltage lockout (OVLO) protection monitors the input voltage pin, VIN, protects against over-voltage stress by disabling switching and reducing the internal peak voltage. Controlled soft-start timing, provided throughout the full power-up time, limits the peak input inrush current while charging the output capacitor and load.

The UCC14240-Q1 also provides a second output rail, (COM – VEE), that is used as a negative bias for the gate drivers, allowing quicker turn-off switching for the IGBTs, and also to protect from unwanted turn-on during fast switching of SiC devices. (COM – VEE) has a simple, yet fast and efficient bias controller to ensure the positive and negative rails are regulated during the PWM switching. The COM pin can be connected from the source of SiC device or emitter of an IGBT device. An external current limiting resistor allows the designer to program the sink and source current peak according to the needs of the gate drive system.

A fault protection and powergood status pin provides a mechanism for the host controller to monitor the status of the DC/DC converter and provide proper sequencing of power and PWM control signals to the gate driver. Fault protection includes undervoltage, overvoltage, over-temperature shutdown, and a 100 µs isolated channel communication interface watchdog timer.

A typical soft-start ramp-up time is approximately 3 ms, but varies based on input voltage, output voltage, output capacitance, and load. If either output is shorted or over-loaded, the device is not able to power-up within the 16-ms soft-start watch-dog-timer protection time, so the device latches off for protection. The latch can be reset by toggling the ENA pin or powering VIN down and up.

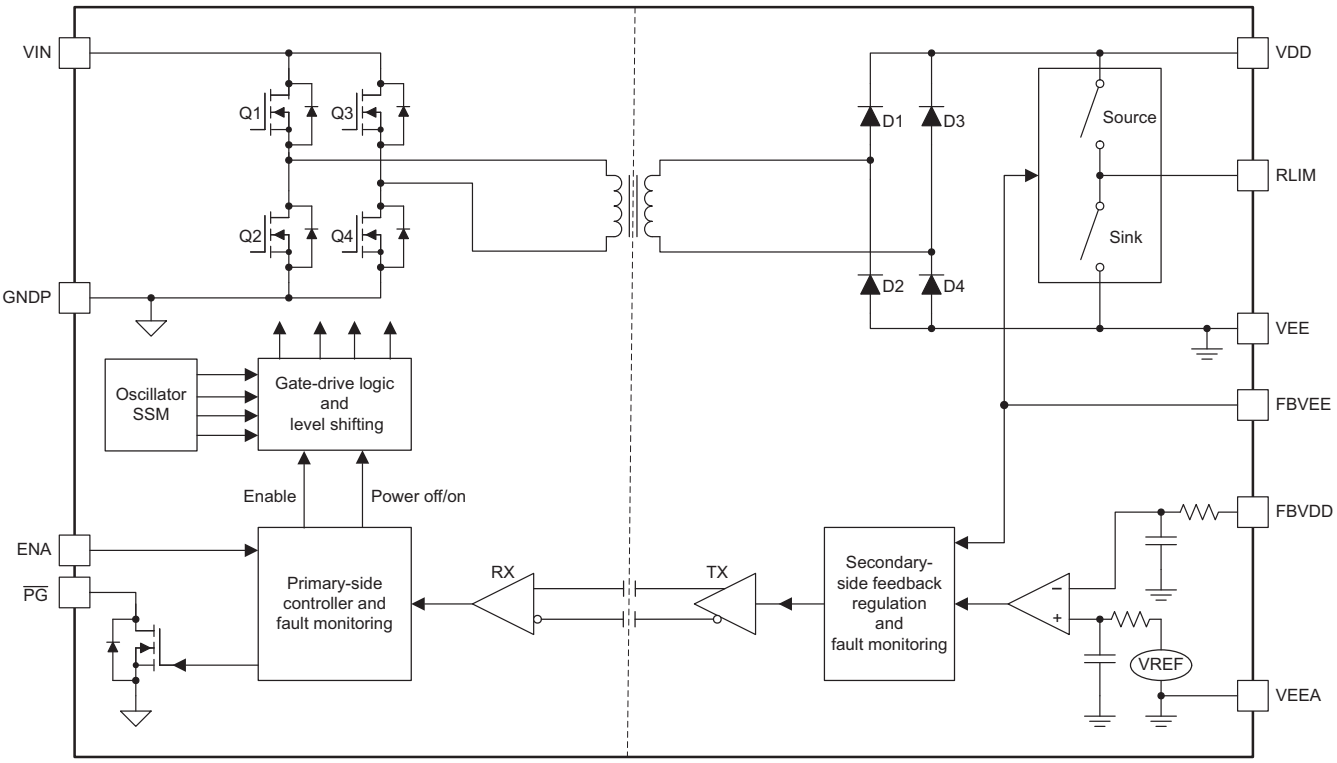
The output load must be kept low until start-up is complete and $\overline{PG}$ pin is low. When powering up, do not apply a heavy load to (VDD – VEE) or (COM – VEE) outputs until the /PG pin has indicated power is good (pulling logic low) to avoid problems providing the power to ramp-up the voltage.

TI recommends to use the $\overline{PG}$ status indicator as a trigger point to start the PWM signal into the gate driver. $\overline{PG}$ output removes any ambiguity as to when the outputs are ready by providing a robust closed loop indication of when both (VDD –VEE) and (COM – VEE) outputs have reached their regulation threshold within ±10%.

Do not allow the host to begin PWM to gate driver until after $\overline{PG}$ goes low. This action typically occurs less than 16 ms after $V_{VIN} > V_{VIN\_UVLOP}$ and ENA goes high. The /PG status output indicates the power is good after soft start of (VDD – VEE) and (COM – VEE) and are within ±10% of regulation.

If the host is not monitoring $\overline{PG}$, then ensure that the host does not begin PWM to gate driver until 20 ms after $V_{VIN} > V_{VIN\_UVLOP}$ and ENA goes high to allow enough time for power to be good after soft start of VDD and VEE.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Stage Operation

The UCC14240-Q1 module uses an active full-bridge inverter on the primary-side and a passive full-bridge rectifier on the secondary-side. The small integrated transformer has a relatively high carrier frequency to reduce the size for integrating into the 36-pin SOIC package. The power stage carrier frequency operates within 10 MHz to 16 MHz. The power stage carrier frequency is determined by input voltage with a feed-forward control: when V_{VIN} is less than 21 V, the frequency is clamped at 16 MHz; when V_{VIN} is higher than 27 V, the frequency is clamped at 10 MHz; when V_{VIN} is between 21 V and 27 V, the frequency reduces gradually from 16 MHz to 10 MHz as V_{VIN} voltage rises. Spread spectrum modulation, SSM, is used to reduce emissions. ZVS operation is maintained to reduce switching power losses.

The UCC14240-Q1 module creates two regulated outputs. It can be configured as a single output converter, VDD to VEE only, or a dual-output converter, VDD to VEE and COM to VEE. Even though the module uses VEE as the reference point to create two positive output voltages, the outputs can use COM as the reference point and become a positive and a negative output.

These two outputs are controlled independently through hysteresis control. Furthermore, the VDD-VEE is the main output, and COM to VEE uses the main output as its input to created a second regulated output voltage.

7.3.1.1 VDD-VEE Voltage Regulation

The VDD-VEE output is the main output of the module. The power stage operation is determined by the sensed VDD-VEE voltage on FBVDD pin. As shown in 図 7-1, the VDD-VEE voltage is sensed through a voltage divider R_{FBVDD_TOP} and R_{FBVDD_BOT}. When FBVDD voltage stays below the turn-off threshold, roughly 10 mV above the V_{FBVDD_REF}, the power stage operates, delivers power to the secondary side and makes the VDD-VEE output voltage rise. After the output reaches the turn-off threshold, the power stage turns off. Output voltage drops because of the load current. After the output voltage drops below the turn-on threshold, roughly 10 mV below the V_{FBVDD_REF}, the power stage is turned on again. With the accurate voltage reference and hysteresis control, the VDD-VEE output voltage can be regulated with high accuracy. To improve the noise immunity, a small capacitor of 330 pF should be added between FBVDD and VEE pins. Excessive capacitor slows down the hysteresis loop and can cause excessive output voltage ripple or even stability issue.

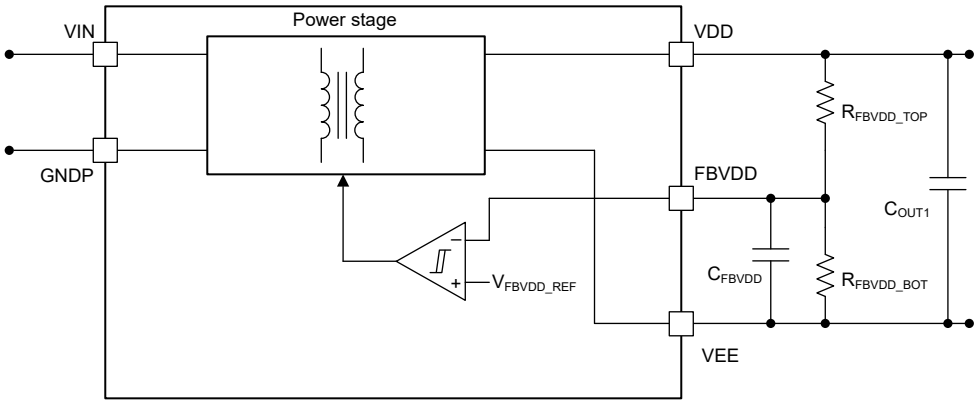


図 7-1. VDD-VEE Voltage Regulation

7.3.1.2 COM-VEE Voltage Regulation

COM-VEE output takes VDD-VEE output as its input and creates a regulated output voltage. It can be considered as an LDO output from VDD-VEE, though the operation principle is not quite the same. Given its input voltage is VDD-VEE, the maximum output voltage from COM to VEE is the voltage between VDD and VEE.

The COM-VEE output regulator stage uses the internal high-side or low-side FETs in series with the external current-limit resistor (R_{LIM}) to charge or discharge the COM-VEE output voltage. The hysteresis control is used to control the switching instance of the two FETs, to achieve an accurately regulated COM-VEE voltage. As shown in 図 7-2, the COM-VEE output voltage is sensed through the voltage divider R_{FBVEE_TOP} and R_{FBVEE_BOT} on FBVEE pin. TI recommends a 330-pF capacitor on FBVEE pin to filter out the switching frequency noise. When the voltage on FBVEE is below the charging threshold, 20 mV below the V_{FBVEE_REF}, the charging resistor is kept on and discharging resistor is kept off. COM-VEE output voltage rises. After FBVEE voltage reaches the stop charging threshold, 20 mV above the V_{FBVEE_REF}, the charging resistor is turned off. Output voltage rise stops. When the charging resistor is turned off, the discharge resistor is controlled by another hysteresis controller, based on FBVEE pin voltage, with the same reference voltage V_{FBVEE_REF}, and 20-mV of hysteresis.

The COM-VEE output regulator stage will protect from having the high-side FET stay ON for a long time during a COM to VEE short. This protection feature is implemented by monitoring the RLIM-pin voltage and controlling the high-side FET duty-ratio. When the COM pin voltage is lower than 0.645 V while the FBVEE voltage is below 2.48 V, the hysteretic control of the COM-VEE regulator is overridden by an approximately 20 % duty-ratio control on high-side FET, with a typical on-time of 1.2 µs and off-time of 5 µs in each duty cycle. When the COM pin voltage is higher than 0.73 V, the duty ratio control is disabled and the hysteretic control resumes to normal operation.

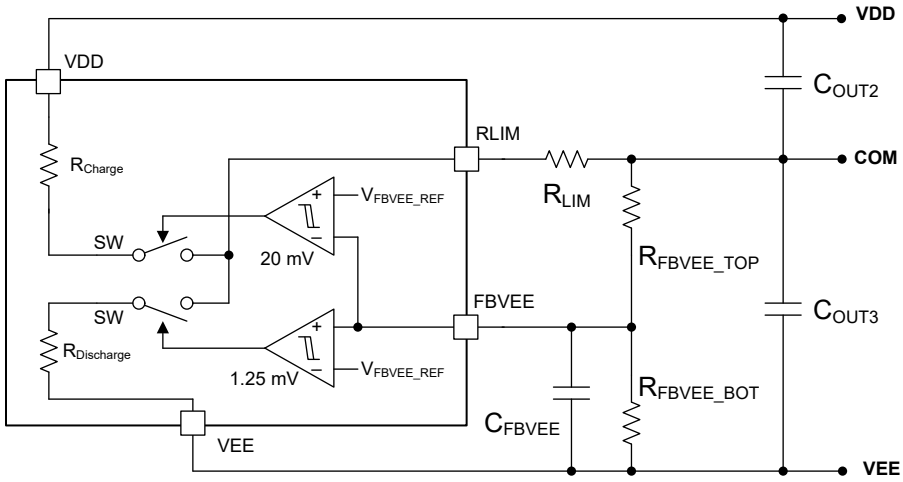


図 7-2. COM-VEE Voltage Regulation

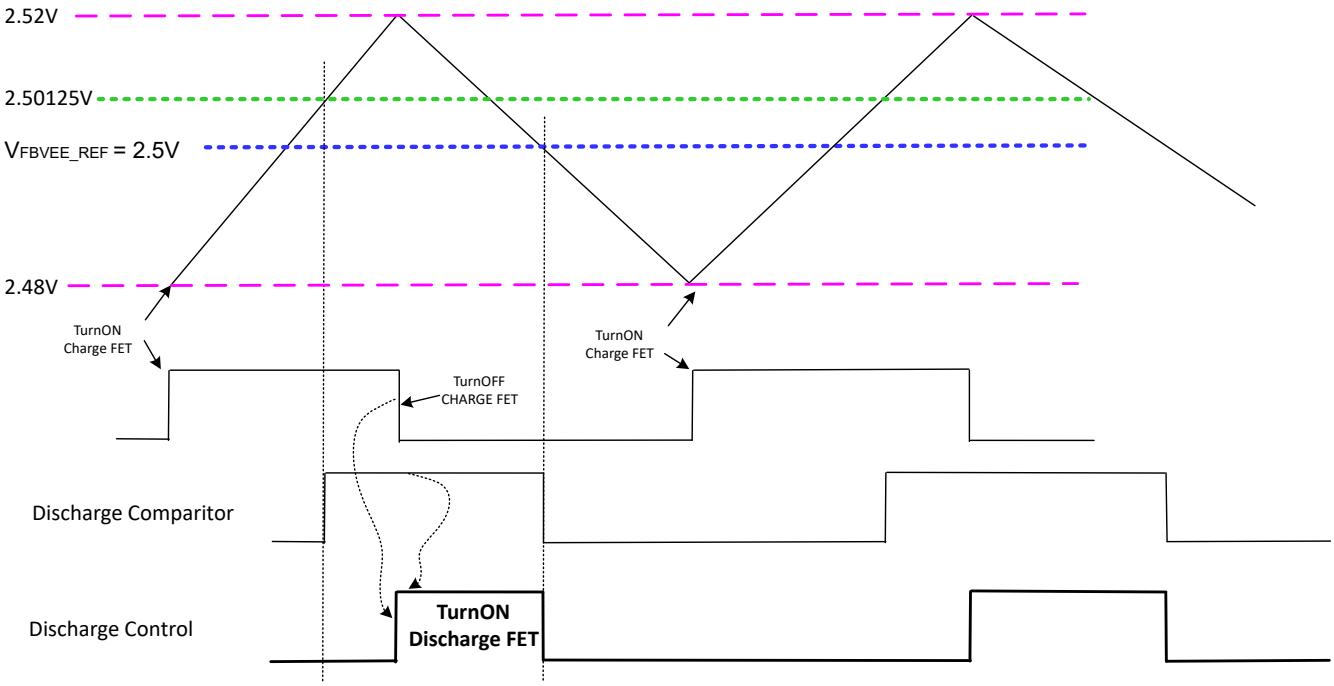


図 7-3. COM-VEE Voltage Regulation Diagram

7.3.1.3 Power Handling Capability

The maximum power handling capability is determined by both circuit operation and thermal condition. For a given output voltage, the maximum power increases with input voltage before triggering the thermal protection. An over-power-protection (OPP) is implemented to limit maximum output power and reduces power stage RMS current at high input voltage. The OPP is implemented by a feed-forward control from the input voltage to the OPP burst duty cycle (D_{OPP}). The D_{OPP} adds a "baby" burst within the on-time of "Mama" burst from the main feedback loop for the (VDD-VEE) regulation. When the input voltage increases, the D_{OPP} reduces automatically to limit the averaged output power.

At high ambient temperature, the thermal performance determines the maximum power and safe operating area (SOA). A protective thermal shut-down is triggered after overtemperature is detected. The high-efficiency and optimized thermal design for transformer and silicon provide a high power handling capability at high ambient temperature in a small package (2W for 85ºC and 1.5 W for 105ºC).

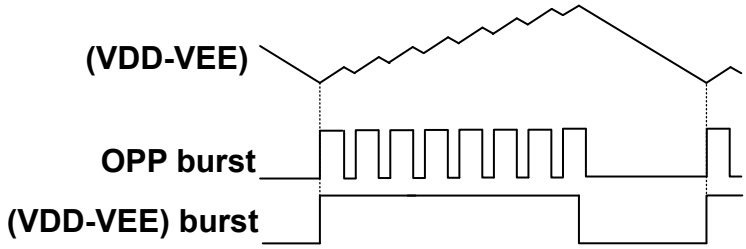


図 7-4. Diagram of Over-Power-Protection with baby burst

7.3.2 Output Voltage Soft Start

UCC14240-Q1 power-up diagram of two output rails with soft start is shown in 図 7-5. After V_{VIN} > V_{VIN_UVLOP} and ENA is pulled high, the soft-start sequence starts with burst duty cycle control with soft duty cycle increment. The burst duty cycle gradually increases from 12.5% to 50% over time by the primary-side control signal (D_{SS_PRI}), so both $V_{VDD-VEE}$ and $V_{COM-VEE}$ increase ratiometrically with a controlled shallow rising slope. When $V_{VDD-VEE}$ is increased above V_{VDD_UVLOS}, there is a sufficient bias voltage for the feedback-loop communication channel, so the burst feedback control on the secondary side takes over. As a result, the D_{SS_PRI} is pulled high and does not affect burst duty cycle anymore. The burst duty cycle is determined by comparing V_{FBVDD} and V_{REF}. V_{REF} increases from 1.1V to 2.5 V with seven increment steps, where each 0.2-V step lasts 128 µs. After $V_{VDD-VEE}$ > V_{VDD_UVP}, /PG is pulled low and the RLIM source-sink regulator for $V_{COM-VEE}$ is enabled. The polarity of source or sink current of RLIM pin is determined by comparing V_{FBVEE} and V_{REF} so as to keep $V_{COM-VEE}$ in tight regulation. The soft-start feature greatly reduces the input inrush current during power-up. In addition, if $V_{VDD-VEE}$ cannot reach to V_{VDD_UVLOS} within 16 ms, then the device shuts down in a safe-state. The 16-ms soft-start time-out protects the module under output short circuit condition before power up.

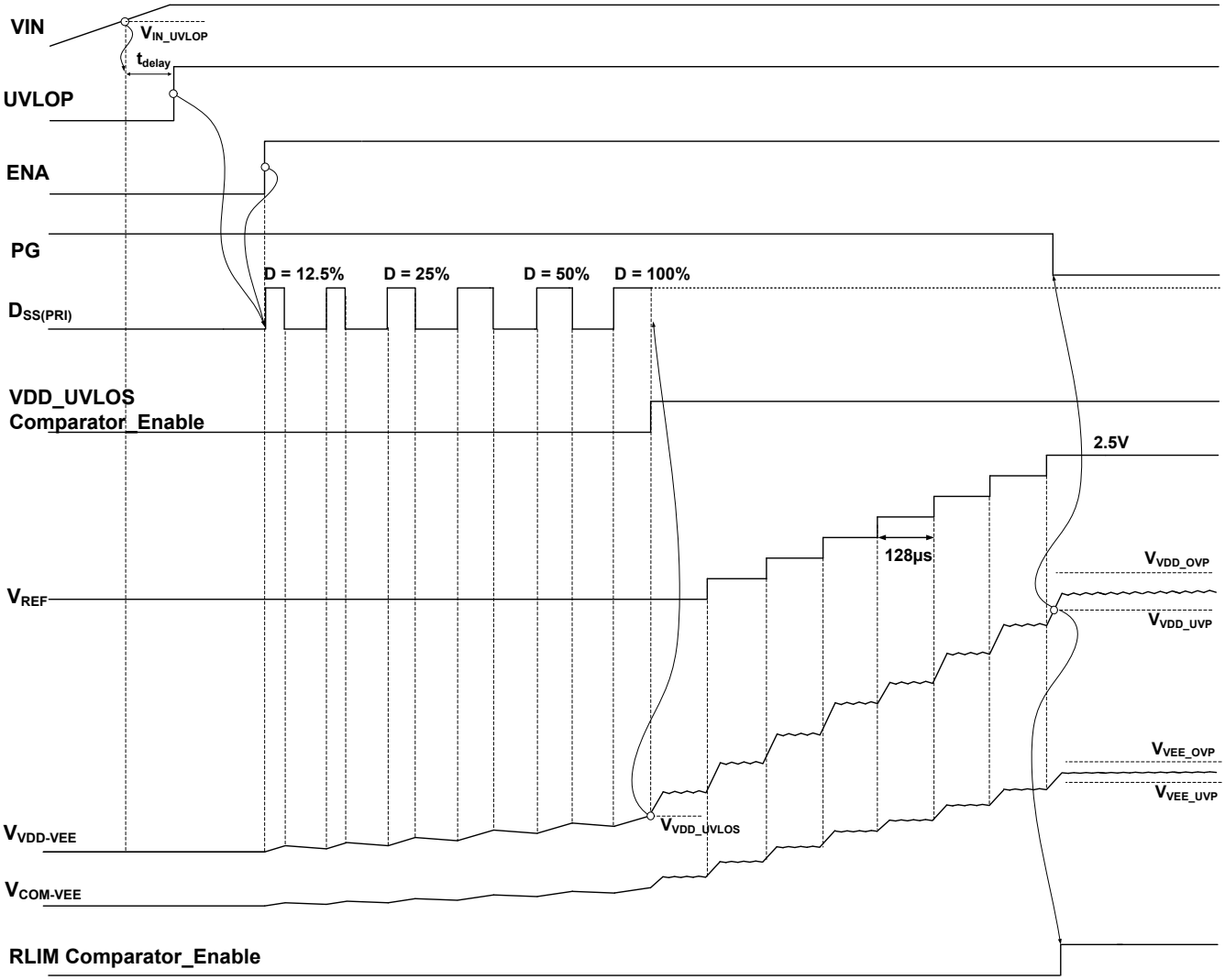


図 7-5. Output voltage Soft-Start Diagram

7.3.3 ENA and $\overline{PG}$

The ENA input pin and $\overline{PG}$ output pin on the primary-side use 5-V TTL and 3.3-V LVTTL level logic thresholds.

The active-high enable input (ENA) pin is used to turn-on the isolated DC/DC converter of the module. Either 3.3-V or 5-V logic rails can be used. Maintain the ENA pin voltage below 5.5 V. After ENA pin voltage becomes above the enable threshold VEN_IR, UCC14240-Q1 enables, starts switching, goes through the soft-start process and delivers power to the secondary side. After ENA pin voltage falls below the disable threshold V_{EN_IF}, UCC14240-Q1 disables, stops switching.

The ENA pin can also be used to reset the UCC14240-Q1 device after it enters the protection safe-state mode. After a detected fault, the protection logic will latch off and place the device into a safe state. When all the faults are cleared, the ENA-pin can be used to clear the UCC14240-Q1 latch by toggling the ENA pin voltage below V_{EN_IF} for longer than 150 µs, then toggling back up to 3.3 V or 5 V. The device will then exit the latch-off mode and we initiate a soft-start. 図 7-6 illustrates the latch-off reset timing.

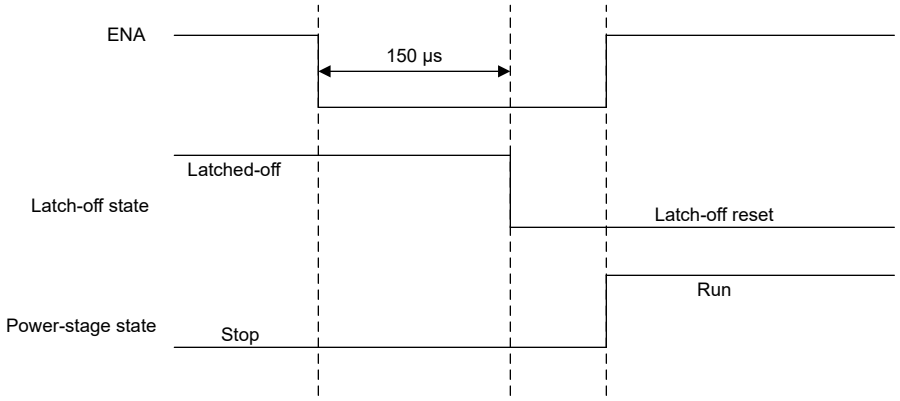


図 7-6. Latch-off Reset Using ENA Pin

The active-low power-good ($\overline{PG}$) pin is an open-drain output that indicates (short) when the module has no fault and the output voltages are within ±10% of the output voltage regulation setpoints. Connect a pull-up resistor (> 1 kΩ) from $\overline{PG}$ pin to either a 5-V or 3.3-V logic rail. Maintain the $\overline{PG}$ pin voltage below 5.5 V without exceeding its recommended operating voltage. The logic of $\overline{PG}$ pin can be illustrated using 図 7-7.

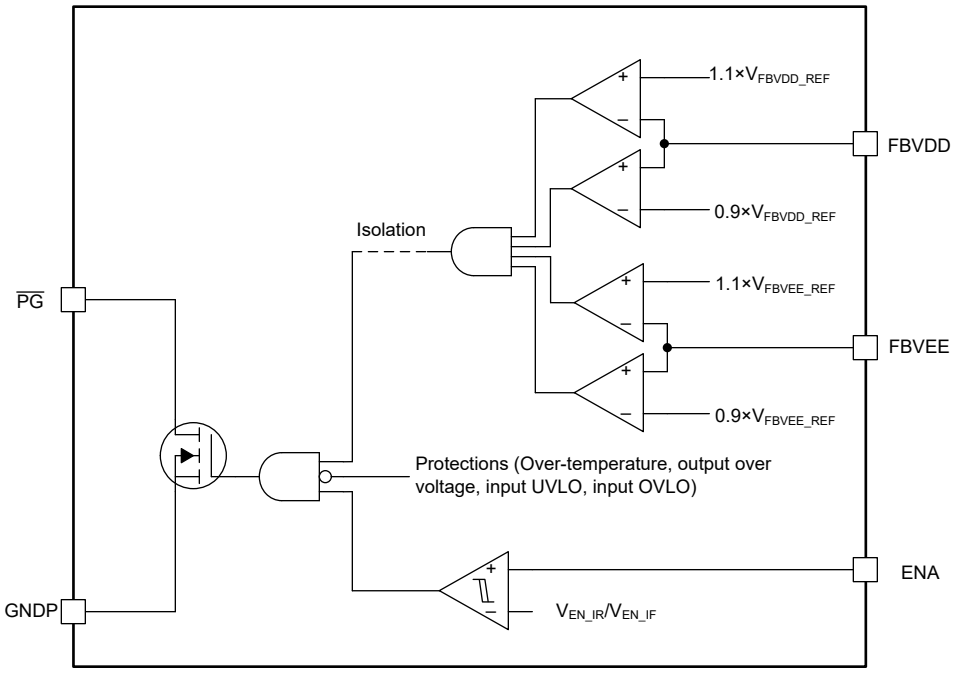


図 7-7. $\overline{PG}$ Pin Logic

7.3.4 Protection Functions

UCC14240-Q1 devices are equipped with a full feature of protection functions, include input undervoltage lockout, overvoltage lockout protections, output undervoltage protection, overvoltage protection, overpower protection, and over-temperature protection. The input undervoltage and overvoltage lockout protections have the auto recovery response. All other protections have the latch-off response. After the latch-off-response protections are triggered, the converter enters a latch off state, stops switching until the latch is reset by either toggling the ENA pin Off then On, or by lowering the V_{VIN} voltage below the $V_{VIN\_ANALOG\_UVLOP\_FALLING}$ threshold, and then above the $V_{VIN\_UVLOP\_RISING}$ threshold.

7.3.4.1 Input Undervoltage Lockout

UCC14240-Q1 can take wide input voltage range, from 21 V to 27 V. When the input voltage becomes too low, the output either cannot be regulated due to the transformer turns ratio limitation, or the converter operates with too much current stress. Either way, the converter must shut down to protect the system.

The UCC14240-Q1 enters input undervoltage lockout when V_{VIN} voltage becomes lower than the UVLO threshold $V_{VIN\_UVLOP\_FALLING}$. In UVLO mode, the converter stops switching. After VIN pin voltage becomes lower than the VIN analog undervoltage lockout falling threshold $V_{VIN\_VULOP\_FALLING}$, UCC14240-Q1 resets all the protections. After that, after the V_{VIN} voltage becomes above the UVLO threshold $V_{VIN\_UVLOP\_RISING}$, the converter is enabled. Depending on the ENA pin voltage, the converter can start switching, go through the soft-start process, or in the disable mode, waiting for ENA pin voltage becomes high.

7.3.4.2 Input Overvoltage Lockout

The input overvoltage lockout protection is used to protect the UCC14240-Q1 devices from overvoltage damage. It has an auto-recovery response. When the V_{VIN} pin voltage becomes higher than the input overvoltage lockout threshold $V_{VIN\_OVLO\_RISE}$, switching stops, converter stops sending energy to the secondary side. After input overvoltage lockout protection, after V_{VIN} pin voltage drop below the recovery threshold $V_{VIN\_OVLO\_FALLING}$, depending on the ENA pin voltage status, the converter can either resuming operation, go through the full soft-start process, or in the disabled mode, wait for ENA pin becomes high. The input overvoltage lockout does not reset other latch-off protections.

7.3.4.3 Output Overvoltage Protection

The UCC14240-Q1 devices sense the output voltage through FBVDD and FBVEE pins to control the output voltage. To prevent the output voltage becomes too high, damages the load or UCC14240-Q1 device itself, the UCC14240-Q1 devices are equipped with the output overvoltage protection. There are two levels of overvoltage protection, based on the feedback pin voltage, and the output voltage.

During the normal operation, because of load transient, or load unbalancing between two outputs, the output voltages can exceed its regulation level. Based on the pin voltages on FBVDD and FBVEE, after the voltage exceeds the threshold, $V_{VDD\_OVP\_RISE}$, or $V_{VEE\_OVP\_RISE}$ (10% above the target regulation voltage), the converter stops switching immediately.

In rare cases, the voltage divider becomes malfunction and gives the wrong output voltage information. In turn, the control loop can regulate the output voltages at a wrong voltage level. The UCC14240-Q1 device is also equipped with a fail-safe overvoltage protection. After the VDD-VEE voltage becomes higher than the overvoltage protection threshold $V_{VDD\_OVLOS\_RISE}$, the converter shuts down immediately. This fail-safe protection level is set at 31 V. It is meant to protect UCC14240-Q1 devices, instead of the load. The design must ensure the voltage feedback divider normal operation at all conditions.

The output overvoltage protections have the latch-off response.

7.3.4.4 Overpower Protection

The Over Power Protection, OPP, limits the maximum average output power. When the output is overloaded, it is important to shutdown the module to prevent it from further damage, or propagating the fault into other portion of the entire system. Given the extremely high switching frequency, it is not practical to implement the traditional cycle-by-cycle current limit. Instead, the UCC14240-Q1 device relies on the Over Power Protection (OPP) working together with the output undervoltage protection.

As discussed in Power Handling Capability, with the input voltage feedforward, and the "baby" burst duty cycle adjustment, the maximum power delivery capability of the UCC14240-Q1 is well controlled. The impact of OPP on the relationship between Vin and maximum output power is shown in 図 7-8.

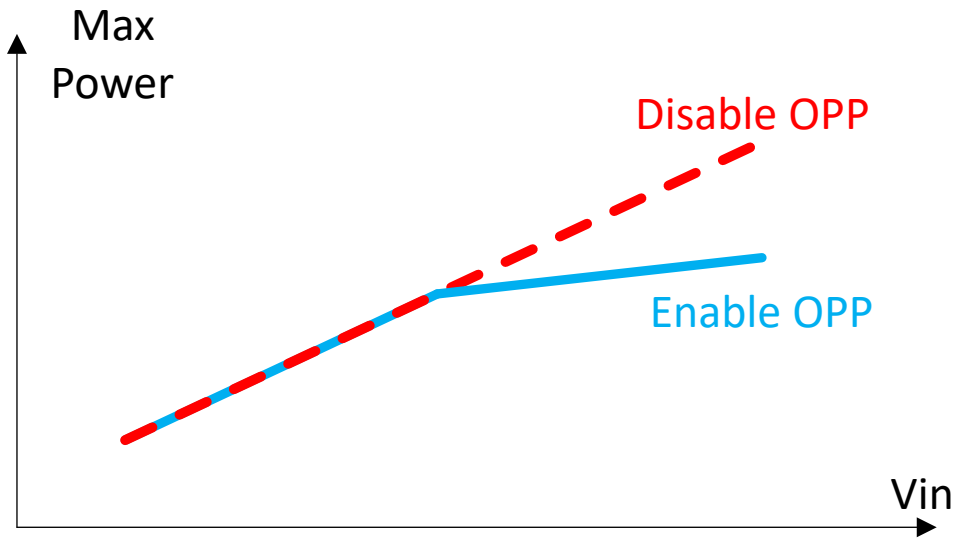


図 7-8. Maximum Output Power Under Different Input Voltage Condition

When the load exceeds the maximum power delivery capability, the output voltage starts to droop. When the output voltage falls below the Under Voltage Protection threshold, the output undervoltage protection is triggered and the parts latches off into a safe state.

7.3.4.4.1 Output Undervoltage Protection

The output voltage under voltage protection is based on the FBVDD and FBVEE pin voltages. When the FBVDD pin voltage becomes lower than its UVP threshold $V_{VDD\_UVP\_FALL}$, or the FBVEE pin voltage becomes lower than its UVP threshold $V_{VEE\_UVP\_FALL}$, the undervoltage protection is activated. The UCC14240-Q1 stops switching, and the PG pin becomes open.

During soft start, the output voltages rise from zero. Both FBVDD and FBVEE pin voltage are below the UVP thresholds. The UVP is disabled during the soft start. If the pin voltage cannot reach the UVP recovery thresholds ($V_{VDD\_UVP\_RISE}$, $V_{VEE\_UVP\_RISE}$) after the soft start completes, undervoltage protection is activated. The UCC14240-Q1 stops switching, and the PG pin becomes open.

The undervoltage protection has a latched-off response. After it is activated, the latch-off state can be cleared by recycling V_{VIN}. Toggling ENA pin can also reset the latch-off state. Refer to ENA and $\overline{PG}$ for details.

7.3.4.5 Overtemperature Protection

UCC14240-Q1 integrates the primary-side, secondary-side power stages, as well as the isolation transformer. The power loss caused by the power conversion causes the module temperature higher than the ambient temperature. To ensure the safe operation of the power module, the UCC14240-Q1 device is equipped with over-temperature protection. Both the primary-side power stage, and the secondary-side power stage temperatures are sensed and compared with the over-temperature protection threshold. If the primary-side power stage temperature becomes higher than $TSHUTP_{PRIMARY\_RISE}$, or the secondary-side power stage temperature becomes higher than $TSHUTS_{SECONDARY\_RISE}$, the module enters over-temperature protection mode. The module stops switching; $\overline{PG}$ pin becomes open. After protection, the module enters latch-off mode. When the power stage temperature drops below the over-temperature recovery threshold, recycling V_{VIN}, or toggling ENA pin voltage brings the model out of latch-off mode. Depending on ENA pin voltage, the module either starts switching, delivering power to the secondary side, or in the standby mode waiting for ENA pin voltage becomes high.

7.4 Device Functional Modes

Depending on the input and output conditions, ENA pin voltage, as well as the device temperature, the UCC14240-Q1 operates in one of the below operation modes.

1. Disable mode. In this mode, the module is off, but waiting for ENA pin becoming high to start operate.

2. Soft-start mode. In this mode, the module starts to deliver power to the secondary side. The primary-side operation duty cycle and secondary-side references are raised gradually to reduce the stress to the module.
3. Normal operation mode. In this mode, the module operates normally, delivers power to the secondary side.
4. Protection mode, auto-recovery. In this mode, the module is off, due to the input UVLO or OVLO protection. After the input voltage fault is cleared, depending on the ENA pin voltage condition, it either becomes disabled mode if the ENA pin voltage is low, or it goes through soft-start mode to the normal operation mode.
5. Protection mode, latched-off. In this mode, the module is off, due to other protections. The module remains off even the fault causing the protection is cleared. Recycling V_{VIN} operation must ensure the input voltage goes below the analog UVLO falling threshold ($V_{VIN\_ ANALOG\_UVLOP\_FALLING}$) first to reset the latch-off state, or the ENA pin is toggled Low (OFF) then High (ON).

表 7-1 lists the supply functional modes for this device. The ENA pin has an internal weak pull-down resistance to ground, but TI does not recommend leaving this pin open.

表 7-1. Device Functional Modes

INPUT			OUTPUTS			Operation Mode
V_{VIN}	ENA	FAULT	$V_{(VDD - VEE)}$ Isolated Output1	$V_{(COM - VEE)}$ Isolated Output2	PG Open Drain	
$V_{VIN} < V_{VIN\_UVLOP\_RISING}$	X	X	OFF	OFF	High	Protection mode, auto-recovery
$V_{VIN\_UVLOP\_RISING} < V_{VIN} < V_{VIN\_OVLO\_RISING}$	LOW	X	OFF	OFF	High	Disable mode
$V_{VIN\_UVLOP\_RISING} < V_{VIN} < V_{VIN\_OVLO\_RISING}$	HIGH	NO FAULT	Regulating at Setpoint	Regulating at Setpoint	Low	Normal operation
$V_{VIN\_UVLOP\_RISING} < V_{VIN} < V_{VIN\_OVLO\_RISING}$	HIGH	YES FAULT	OFF	OFF	High	Protection mode, latched-off
$V_{VIN} > V_{VIN\_OVLO\_RISING}$	X	X	OFF	OFF	High	Protection mode, auto-recovery

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The UCC14240-Q1 device is suitable for applications that have limited board space and desire more integration. This device is also suitable for very high voltage applications, where power transformers meeting the required isolation specifications are bulky and expensive.

8.2 Typical Application

The following figures show the typical application schematics for the UCC14240-Q1 device configurations supplying an isolated load.

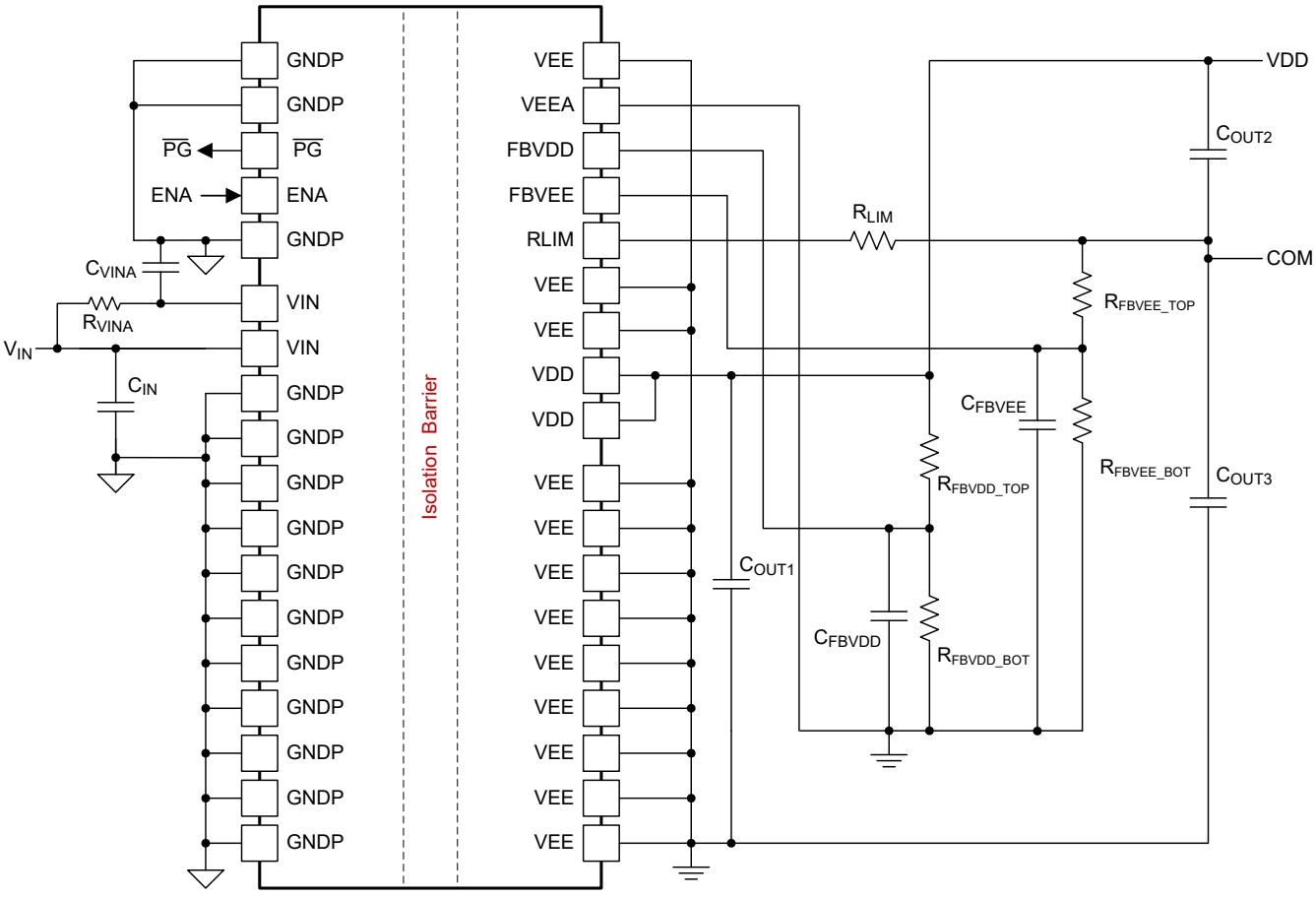


図 8-1. Dual Adjustable Output Configuration

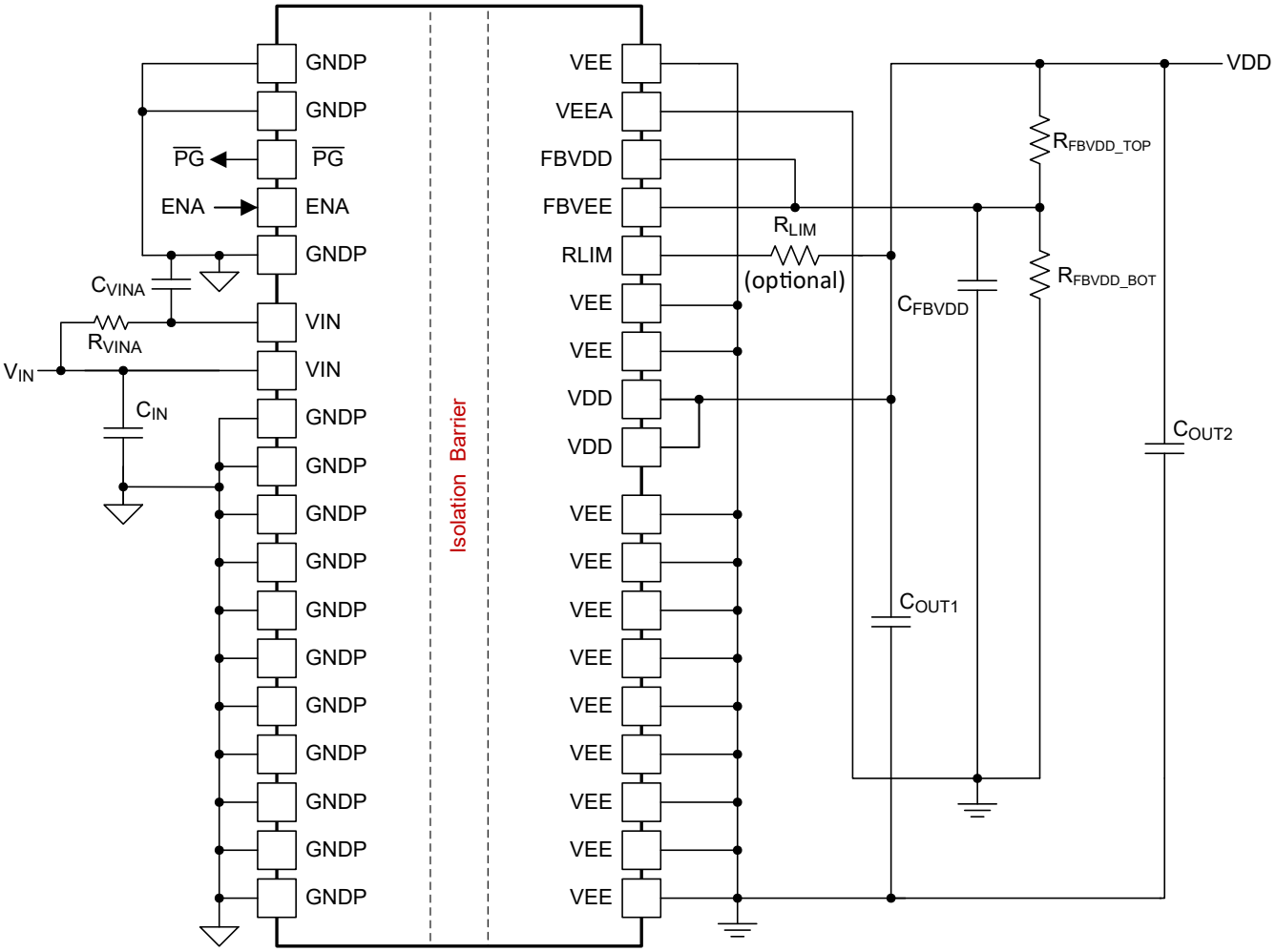


図 8-2. Single Adjustable Output Configuration

8.2.1 Design Requirements

Designing with the UCC14240-Q1 module is simple. First, choose single output or dual output. Determine the voltage for each output and then set the regulation through resistor dividers. The gate charge of the power device determines the amount of output decoupling capacitance needed at the gate driver input. Calculate the RLIM resistor value for regulating the (COM – VEE) voltage rail for a dual output. Finally, add the recommended input and output capacitors according to the procedure below.

8.2.2 Detailed Design Procedure

Place ceramic decoupling capacitors as close as possible to the device pins. For the input supply, place the capacitors between pins 6 to 7 (VIN) and pins 8 to 9 (GNDP). For the isolated output supply, (VDD – VEE), place the capacitors between pins 28 to 29 (VDD) and pins 30 to 31 (VEE). For the isolated output supply, (COM – VEE), place an RLIM resistor between the RLIM pin and the gate driver COM supply input. Also place decoupling capacitors at the gate driver supply pins (COM and VEE) and at gate driver supply pins (VDD and VEE) with values according to the following component calculation sections. These locations are of particular importance to all the decoupling capacitors because the capacitors supply the transient current associated with the fast switching waveforms of the power drive circuits. Ensure the capacitor dielectric material is compatible with the target application temperature.

8.2.2.1 Capacitor Selection

The UCC14240-Q1 device creates an isolated output VDD-VEE as its main output. The device also creates a second output COM-VEE, using VDD-VEE as its power source. Because both outputs are isolated from the

input, and sharing VEE as the common reference point, the UCC14240-Q1 outputs can be configured as dual-output two-positive, dual-output two-negative, or dual-output one-positive and one-negative. UCC14240-Q1 output can also be used as a single positive output or single negative output.

When the module is configured as dual-output, one-positive output, one-negative output; it is very important to properly select the output capacitor ratios C_{OUT2} and C_{OUT3} to optimize the regulation and avoid causing an over-voltage or under-voltage fault.

表 8-1. Calculated Capacitor Values

CAPACITOR	VALUE (µF)	NOTES
C_{IN}	10 + 0.1	Place a 10-µF and a 0.1-µF high-frequency decoupling capacitor in parallel close to VIN pins. A capacitance greater than 10uF can be used to reduce the voltage ripple when the series impedance from the voltage source to the VIN pins is large. Optionally, connect a 330pF 0402 size high-frequency bypass ceramic capacitor close to analog VIN PIN 6 and GNDP PIN 5 when the input voltage ripple is large enough to interfere with the internal input voltage sense signal and the normal startup operation. For extreme input ripple voltage cases, connect a 4.75-ohm filter resistor to power input, PIN7, and connect a 10-µF ceramic capacitor from analog VIN PIN 6, to power analog GNDP. In most cases, the RC input filter is not needed. If the filter resistor is not placed, make sure both PIN 6 and PIN 7 are connected to input voltage.
C_{OUT1}	2.2 + 0.1	Add a 2.2-µF and a 0.1-µF capacitor for high-frequency decoupling of (VDD – VEE). Place close to the VDD and VEE pins. A capacitance greater than 2.2uF can be used to reduce the output voltage ripple.
C_{OUT2}	See below	Bulk charge, decoupling output capacitors are required at the gate driver pins. The C_{OUT2} and C_{OUT3} capacitance ratio is important to optimize the dual output voltage divider accuracy during charge or discharge switching cycles.
C_{OUT3}	See below	

The selection of C_{OUT2} and C_{OUT3} is based on the gate charge requirement for the gate driver load, the charge balancing during the start-up, and the expected maximum current loading.

During the startup, the ratio between C_{OUT2} and C_{OUT3} must be equal to the ratio between (COM−VEE) and (VDD−COM) and offset by the loading current from VDD-COM and COM-VEE, to allow both COM to VEE and VDD to VEE voltages reaches steady state at the same time, as shown in 式 1.

First calculate the C_{OUT2} value based on the Gate charge of the power device Q_{G_Total}, whether IGBT or SiC power MOSFET, and the percent of voltage droop wanted during the turn-on of the gate with respect to the positive gate voltage applied, VDD to COM.

$$C_{OUT2} = \frac{Q_{G\_Total}}{\left(\frac{Percent\_Cdroop}{100}\right) \times (V_{VDD-COM})} \quad (1)$$

where

- Q_{G_Total} is the total gate charge of the power switch

Then calculate the C_{OUT3} value based on the output voltage ratios, the load current expected, and the variation of the output capacitors.

$$C_{OUT3} = \frac{C_{OUT2} \times (V_{VDD-COM}) \times \left(I_{MAX\_POWER} - I_{(COM-VEE)}\right)}{(V_{COM-VEE}) \times \left(I_{MAX\_POWER} - I_{(VDD-COM)}\right)} \quad (2)$$

where the load $I_{VDD\text{-}COM}$ and $I_{COM\text{-}VEE}$ are the load currents respectively, and the I_{MAX_POWER} is the SOA Maximum Power (P_{MAX_SOA}) divided by the $V_{VDD\text{-}VEE}$ output voltage.

$$I_{(VDD-COM)} = I_{Q\_Driver\_VDD-COM} + I_{Other\_load\_VDD-COM} \quad (3)$$

$$I_{(COM-VEE)} = I_{Q\_Driver\_COM-VEE} + I_{Other\_load\_COM-VEE} \quad (4)$$

where

- $I_{(VDD-COM)}$ is the total current from VDD to COM, excluding average gate drive current.
- $I_{(COM-VEE)}$ is the total current from COM to VEE, excluding average gate drive current.
- $I_{Q\_DRIVER\_VDD-COM}$ is the maximum quiescent current of the gate driver from (VDD – COM), and any current pulled from VDD by external logic must be included.
- $I_{Q\_DRIVER\_COM-VEE}$ is the maximum quiescent current of the gate driver from (COM – VEE),
- $I_{Other\_load\_VDD-COM}$ is the maximum current pulled from VDD to COM by external logic.
- $I_{Other\_load\_COM-VEE}$ is the maximum current pulled from COM to VEE by external logic.

and

$$I_{POWER} = \frac{P_{MAX}}{V_{VDD-VEE}} \quad (5)$$

The approximate P_{MAX} value can be extracted from the provided SOA curves at the respective ambient temperature.

Calculate C_{OUT3} using worst case capacitor values based on expected variation, $C_{OUT3\_maximum}$, and $C_{OUT3\_Minimum}$. This action makes sure the capacitor ratio tends to push the COM-VEE voltage to a slightly lower value than the target regulation value during startup.

注

C_{OUT2} and C_{OUT3} are the total capacitance on the VDD and VEE outputs. They include the capacitors from both the isolated bias supply and the gate driver circuit.

The sizes of C_{OUT2} and C_{OUT3} are determined by the gate driver load gate charge and ripple voltage requirement. C_{OUT1} can then be used to reduce the total ripple voltage and to soften the start-up time.

8.2.2.2 R_{LIM} Resistor Selection

When the module is configured as dual-positive or dual-negative outputs, the RLIM resistor is a true current limiting resistor. Set up the RLIM resistor value as the maximum load current needed for $V_{COM-VEE}$, using 式 6. I_{VOUT2_max} is the maximum load current for $V_{COM-VEE}$ output.

$$R_{LIM} = \frac{V_{COM-VEE}}{I_{(VDD-COM)\_max}} - R_{LIM\_INT} \quad (6)$$

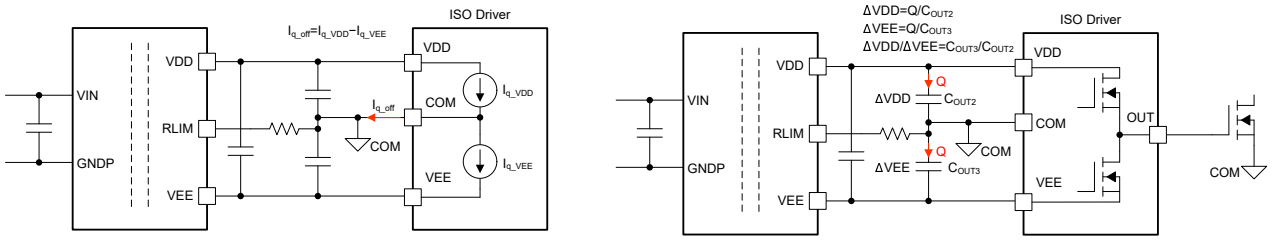
R_{LIM_INT} is the internal switch resistance value of 30 Ω typical.

For isolated gate driver applications, one positive and one negative outputs are needed. In this case, VDD-VEE is the total output voltage, and the middle point becomes the reference point. Because the total voltage between VDD and VEE is always regulated through the FBVDD feedback, the RLIM pin only must regulate the middle point voltage so that it can give the correct positive and negative voltages. The RLIM control is achieved through FBVEE pin as described in COM-VEE Voltage Regulation.

Based on Capacitor Selection, when selecting the output capacitor ratio proportional to the voltage ratio, the capacitors form a voltage divider. The middle point voltage must naturally give the correct positive and negative voltages. At the same time, for the gate driver circuit, the gate charge pulled out from the positive rail capacitor during turn-on is fed back to the negative rail capacitor during turn-off, the two output rail load must always be balanced. However, due to the gate driver circuit quiescent current unbalancing, and the two-rail capacitance tolerances, the middle point voltage can move away with time. The RLIM pin provides an opposite current to keep the middle point voltage at the correct level.

As illustrated in 図 8-3 (a), without considering the gate charge, the gate driver circuit quiescent current loads the positive rail and negative rail differently. The net current shows up as a DC offset current to the middle point.

As illustrated in 図 8-3 (b), every time the gate driver circuit turns-on the main power switch, it pulls the charge out of the positive and negative rail output capacitors. When the module power stage provides energy to the secondary side, refreshing those capacitors, the same charge is fed into both capacitors. If the capacitor values are perfect, the voltage rise in the capacitors will be proportional. The positive and negative voltages would not change. However, due to the capacitor tolerances, the capacitor values are not perfectly matched. The voltages will rise at different ratios with the smaller capacitor rising faster. Over time, the middle point voltage, COM, would pull to a different value. A load across one of the capacitors will pull towards a voltage imbalance. The RLIM function counteract the voltage imbalance and bring the COM voltage back into regulation.



(a) Load current unbalancing

(b) Capacitance unbalancing

図 8-3. Source of voltage unbalancing

Considering these two effects, the RLIM must provide enough current to compensate this offset current. The RLIM must be low enough to provide enough current, but not too low otherwise the middle point voltage is corrected at each turn on and turn off edge of the gate driver and excessive power loss is generated.

The R_{LIM} resistor chosen can provide enough current for the load using the following equations, whichever has lower R_{LIM} value. 式 7 shows source current due to capacitor variation and gate driver quiescent current (I_Q). 式 8 shows sink current due to capacitor variation and I_Q.

$$R_{LIM\_MAX} = \frac{(VDD - COM)}{\left[\frac{C_{OUT3} \times (1 - \Delta C_{OUT3})}{C_{OUT2} \times (1 - \Delta C_{OUT2}) + C_{OUT3} \times (1 - \Delta C_{OUT3})} - \frac{C_{OUT3}}{C_{OUT2} + C_{OUT3}}\right] \times Q_{G\_Total} \times f_{SW} + \left(I_{(COM - VEE)} - I_{(VDD - COM)}\right)} - R_{LIM\_INT} \quad (7)$$

$$R_{LIM\_MAX} = \frac{(VEE - COM)}{\left[\frac{C_{OUT2} \times (1 - \Delta C_{OUT2})}{C_{OUT2} \times (1 - \Delta C_{OUT2}) + C_{OUT3} \times (1 - \Delta C_{OUT3})} - \frac{C_{OUT2}}{C_{OUT2} + C_{OUT3}}\right] \times Q_{G\_Total} \times f_{SW} + \left(I_{(COM - VEE)} - I_{(VDD - COM)}\right)} - R_{LIM\_INT} \quad (8)$$

Select RLIM value to be the lowest of either 1) the RLIM needed for capacitor imbalance and the load, or 2) the RLIM needed to respond to a 10% overshoot of $V_{COM\text{-}VEE}$ within 1.5 ms with the given load current.

$$R_{LIM\_MAX\_for\_overshoot} = \frac{V_{COM - VEE}}{\left(C_{OUT3\_max} \times \frac{0.10 \times V_{VDD - COM}}{1.5\ ms}\right) + \left(I_{(VDD - COM)} - I_{(COM - VEE)}\right)} - R_{LIM\_INT} \quad (9)$$

where

- Q_{G_Total} is the total gate charge of power switch.
- f_{SW} is the switching frequency of gate drive load.

R_{LIM} value determines response time of (COM – VEE) regulation. Too low an R_{LIM} value can cause oscillation and can overload (VDD – VEE). Too high an R_{LIM} value can give offset errors, due to slow response. If R_{LIM} is greater than above calculations, then there is not enough current available to replenish the charge to the output capacitors, causing a charge imbalance where the voltage is not able to maintain regulation, and eventually exceeds the OVP2 or UVP2 FAULT thresholds and shutting down the device for protection. Choose R_{LIM} value to be 10% less than the smaller value of the two calculated results.

8.2.3 Application Curves

The PMP23223 is a reference design that pairs the complementary UCC14240-Q1 isolated DC/DC power module with the UCC21732-Q1 isolated gate driver for a SiC power MOSFET or IGBT power module. The following waveforms show the controlled soft start for both positive and negative rails. Also shown, is the fast and highly accurate voltage regulation during gate driver switching from 1 kHz to 35 kHz. See PMP23223 reference design test report for more details.

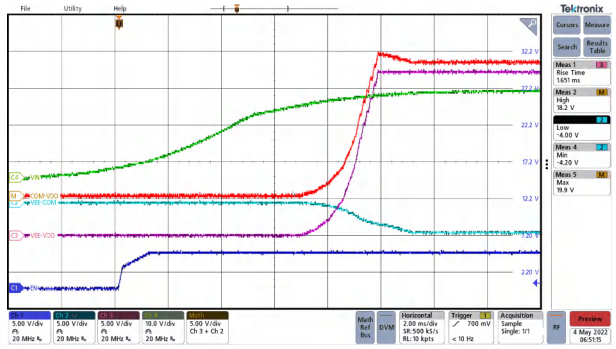


図 8-4. Power-Up Sequence.

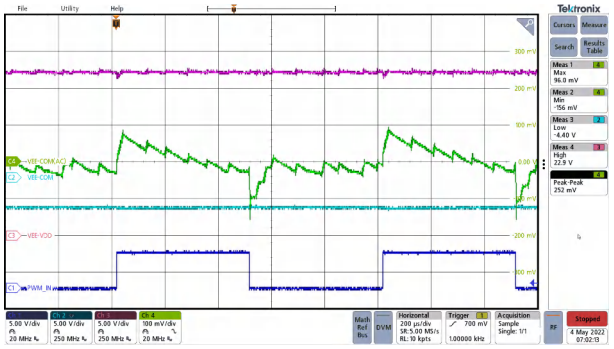


図 8-5. Ripple voltage: VEE-COM Switching 100-nF Load at 1 kHz.

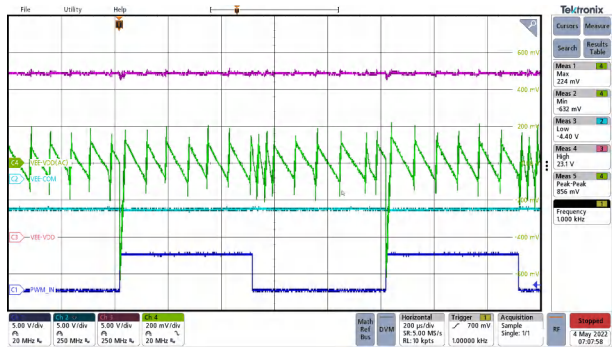


図 8-6. Ripple voltage: VDD-VEE Switching 100-nF Load at 1 kHz.

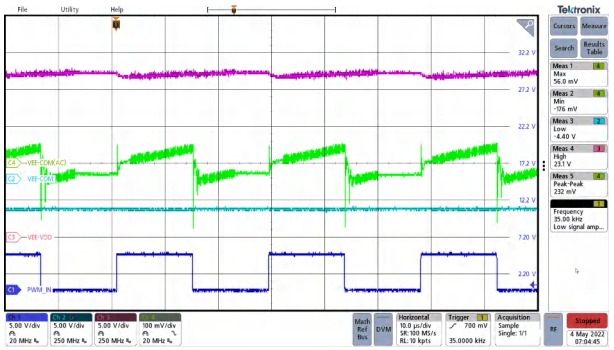


図 8-7. Ripple voltage: VEE-COM Switching 100-nF Load at 35 kHz.

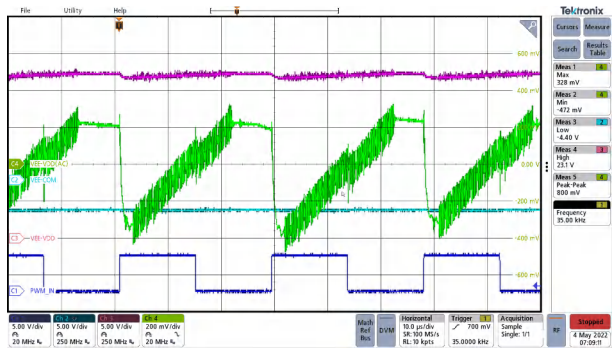


図 8-8. Ripple voltage: VDD-VEE Switching 100-nF Load at 35 kHz.

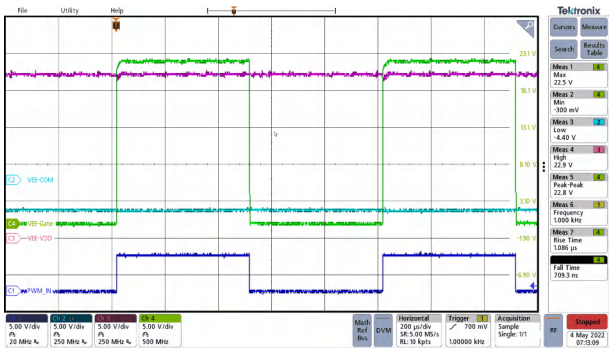


図 8-9. Gate Waveform Switching 100 nF at 1 kHz.

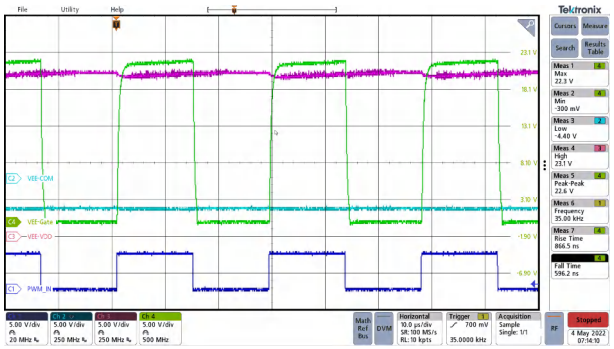


図 8-10. Gate Waveform Switching 100 nF at 35kHz.

8.3 System Examples

The UCC14240-Q1 module is designed to allow a microcontroller host to enable it with the ENA pin for proper system sequencing. The $\overline{PG}$ output also allows the host to monitor the status of the module. The /PG pin goes low when there are no faults and the output voltage is within ±10% of the set target output voltage. The output voltage is meant to power a gate driver for either IGBT or SiC FET power device. The host can start sending PWM control to the gate driver after the $\overline{PG}$ pin goes low to ensure proper sequencing. Shown below is the system diagram for the dual-output configuration and a system diagram for the single output configuration.

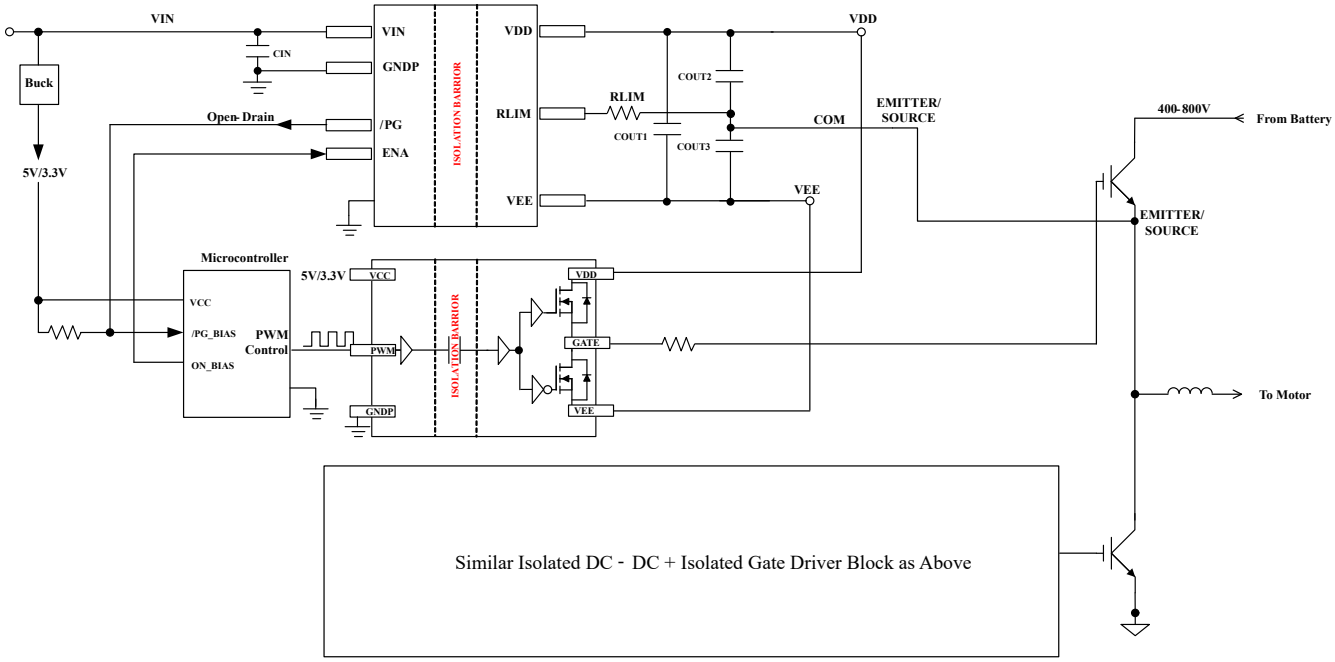


図 8-11. Dual Output System Configuration

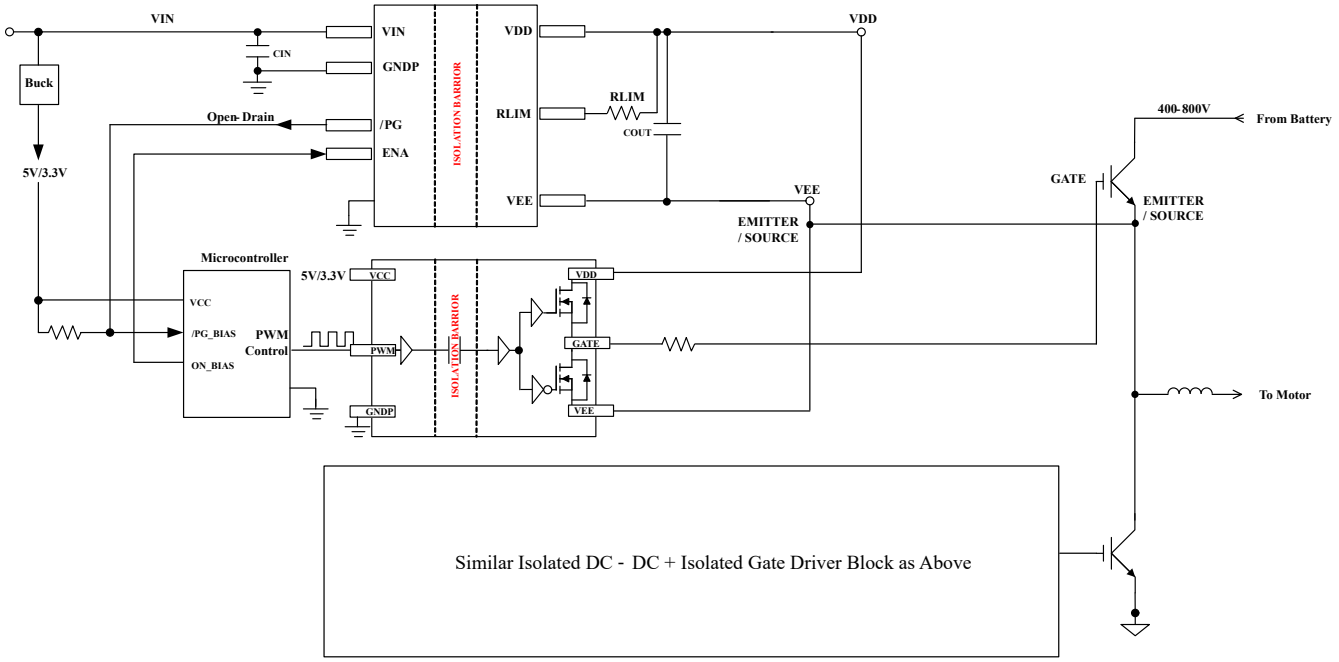


図 8-12. Single Output System Configuration

8.4 Power Supply Recommendations

The recommended input supply voltage (V_{VIN}) for UCC14240-Q1 is between 21 V and 27 V. To help ensure reliable operation, adequate decoupling capacitors must be located as close to supply pins as possible. Local bypass capacitors must be placed between the VIN and GNDP pins at the input; between VDD and VEE at the isolated output supply; and COM and VEE at the lower voltage output supply. TI recommends low ESR, ceramic surface mount capacitors. TI further suggests placing two such capacitors: one with a value of 2.2 µF for supply bypassing and an additional 0.1-µF capacitor in parallel for high frequency filtering. The input supply must have an appropriate current rating to support output load required by the end application.

8.5 Layout

8.5.1 Layout Guidelines

The UCC14240-Q1 integrated isolated power solution simplifies system design and reduces board area usage. Follow these guidelines for proper PCB layout to achieve optimum performance.

- Place decoupling capacitors as close as possible to the device pins. For the input supply, place the capacitors between pin 7 (power VIN) and pins 8–18 (power GNDP), and place the capacitors between pin 6 (analog VIN) and pins 1, 2, and 5 (analog GNDP). For the isolated output supply, place the capacitors between pin 28, 29 (VDD) and pins 19–25, 30–31, 35–36 (VEE). This location is of particular importance to the input decoupling capacitor because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.

  The capacitors between pin 6 (analog VIN) and pins 1, 2, and 5 (analog GNDP) are optional and recommended.
- Because the device does not have a thermal pad for heat-sinking, the device dissipates heat through the respective GND pins. Ensure that enough copper (preferably a connection to the ground plane) is present on GNDP and VEE pins for best heat-sinking.
- If space and layer count allow, TI recommends to connect the VIN, GNDP, VDD, and VEE pins to internal ground or power planes through multiple vias. Alternatively, make the traces that are connected to these pins as wide as possible to minimize losses.
- Minimize capacitive coupling between the RLIM pin and the FBVEE pin by separating the traces while routing, and if possible use a via near the FBVEE pin to route the feedback connection through a different layer.

- A minimum of four layers is recommended to accomplish a good thermal PCB design. Inner layers can be used to create a high-frequency bypass capacitor between GNDP and VEE, which in turn mitigates radiated emissions.
- Pay close attention to the spacing between primary ground plane (GNDP) and secondary ground plane (VEE) on the outer layers of the PCB. The effective creepage and clearance of the system is reduced if the two ground planes have a lower spacing than that of the UCC1413x-Q1 package.
- To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the UCC14240-Q1 module.

8.5.2 Layout Example

The layout example shown in the following figures is from the evaluation board UCC14240-Q1EVM, UCC14240EVM-052, and based on the 図 8-1 design.

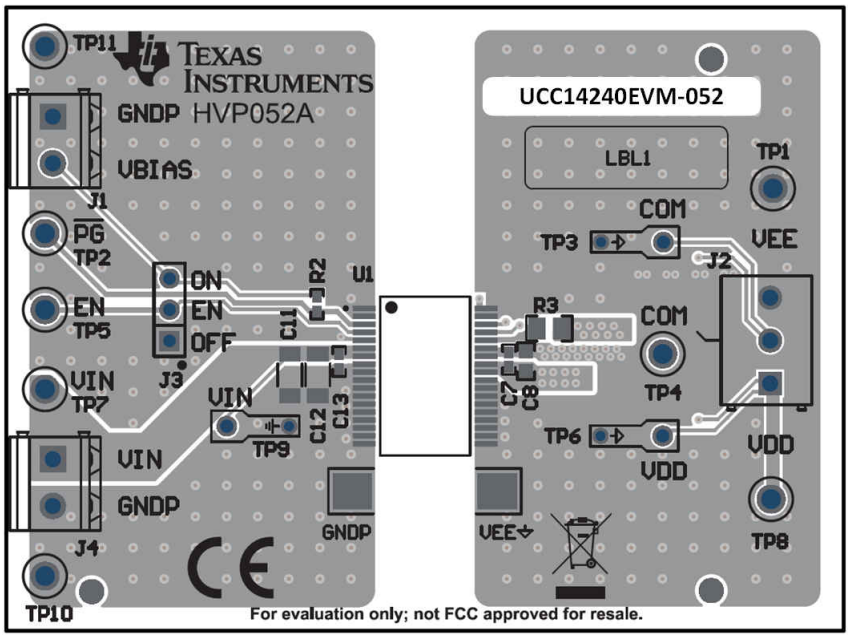


図 8-13. UCC14240-Q1EVM, PCB Top Layer, Assembly

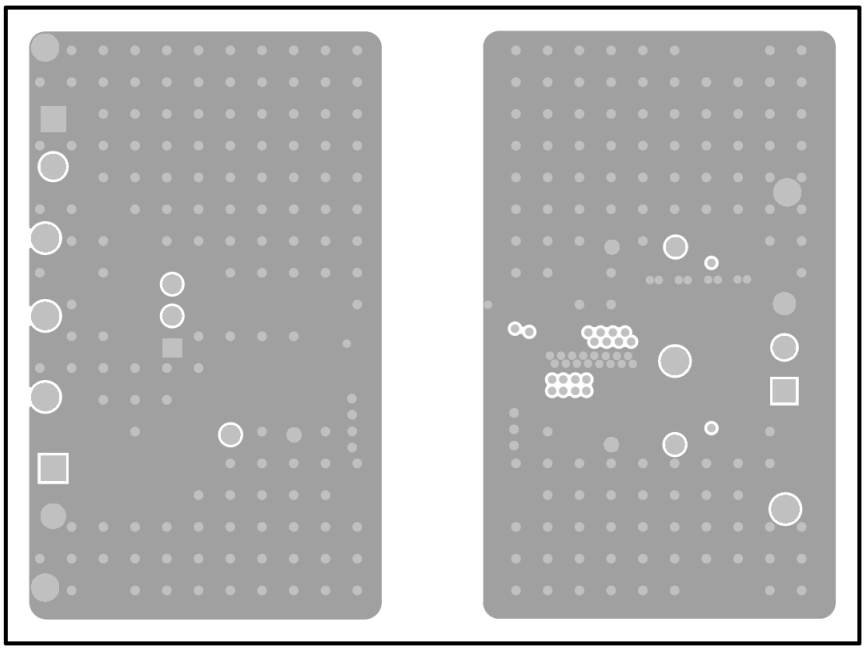


図 8-14. UCC14240-Q1EVM, Signal Layer 2 (Same as Layer 3)

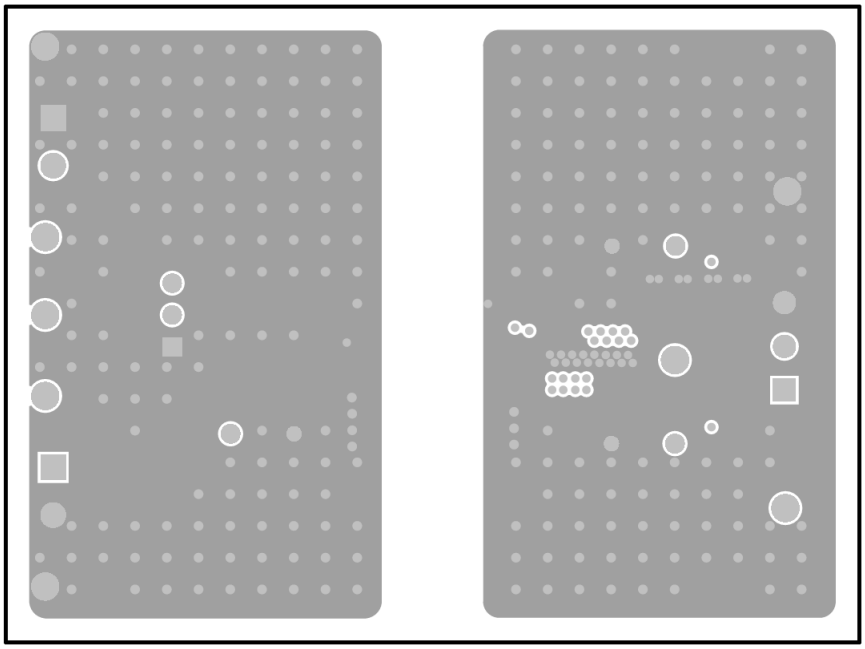


図 8-15. UCC14240-Q1EVM, Signal Layer 3 (Same as Layer 2)

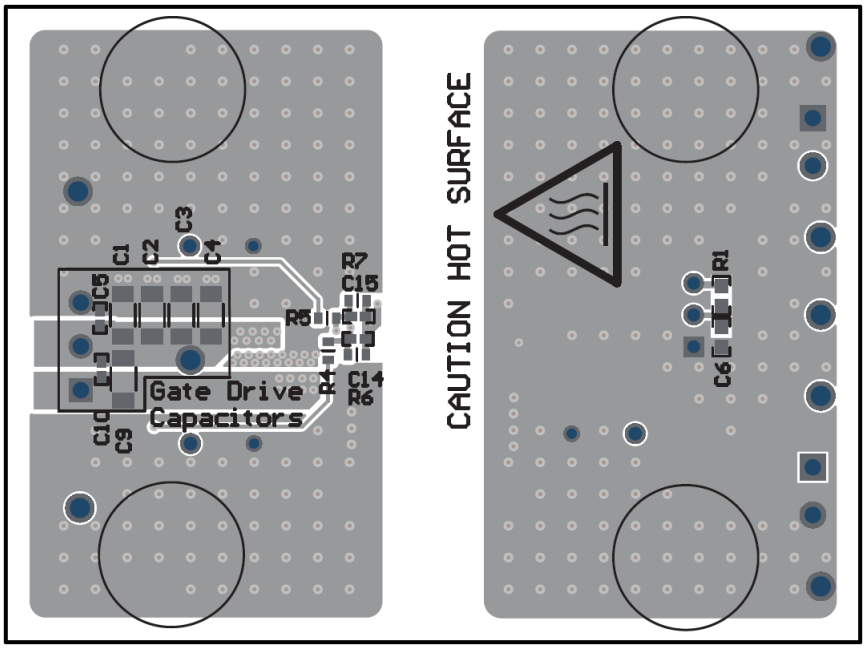


図 8-16. UCC14240-Q1EVM, PCB Bottom Layer, Assembly (Mirrored View)

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Using the UCC14240EVM-052 for Biasing Traction Inverter Gate Driver ICs Requiring Single, Positive or Dual, Positive/Negative Bias Power user's guide*
- Texas Instruments, *Isolation Glossary*

9.2 ドキュメントの更新通知を受け取る方法

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC14240QDWNRQ1	ACTIVE	SO-MOD	DWN	36	750	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC14240-Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

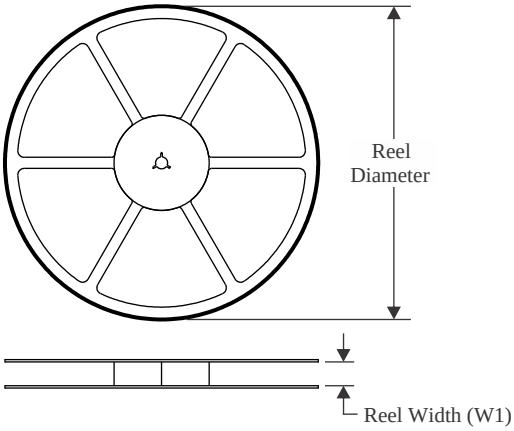
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

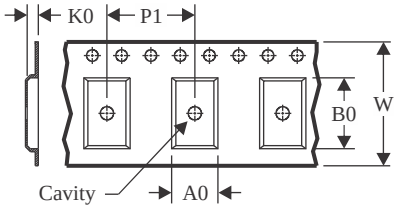
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

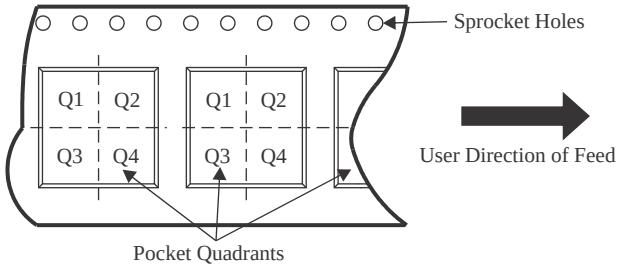


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

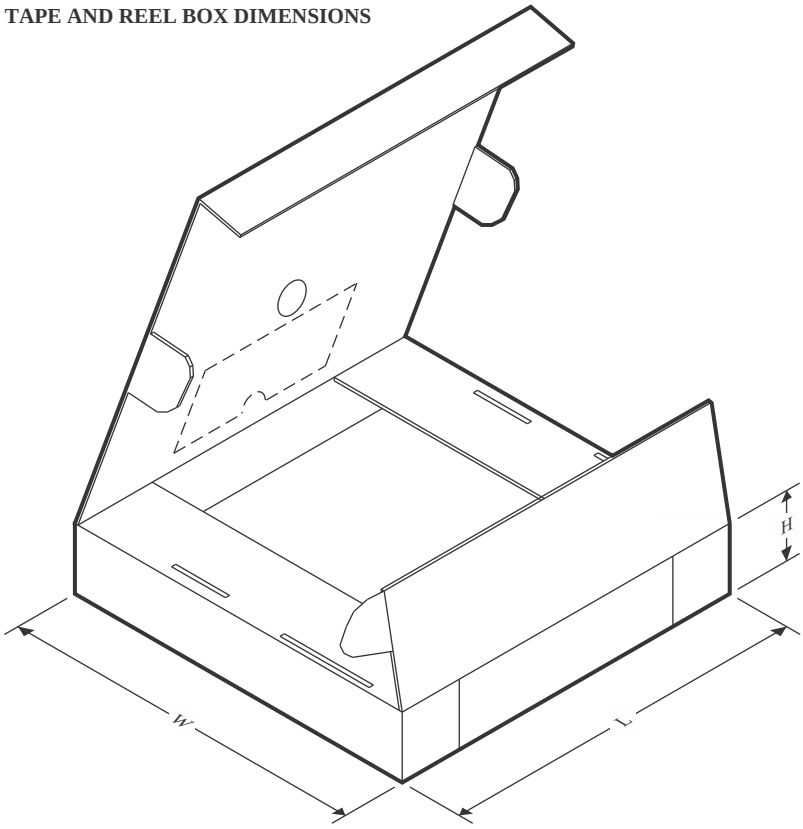
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC14240QDWNRQ1	SO-MOD	DWN	36	750	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

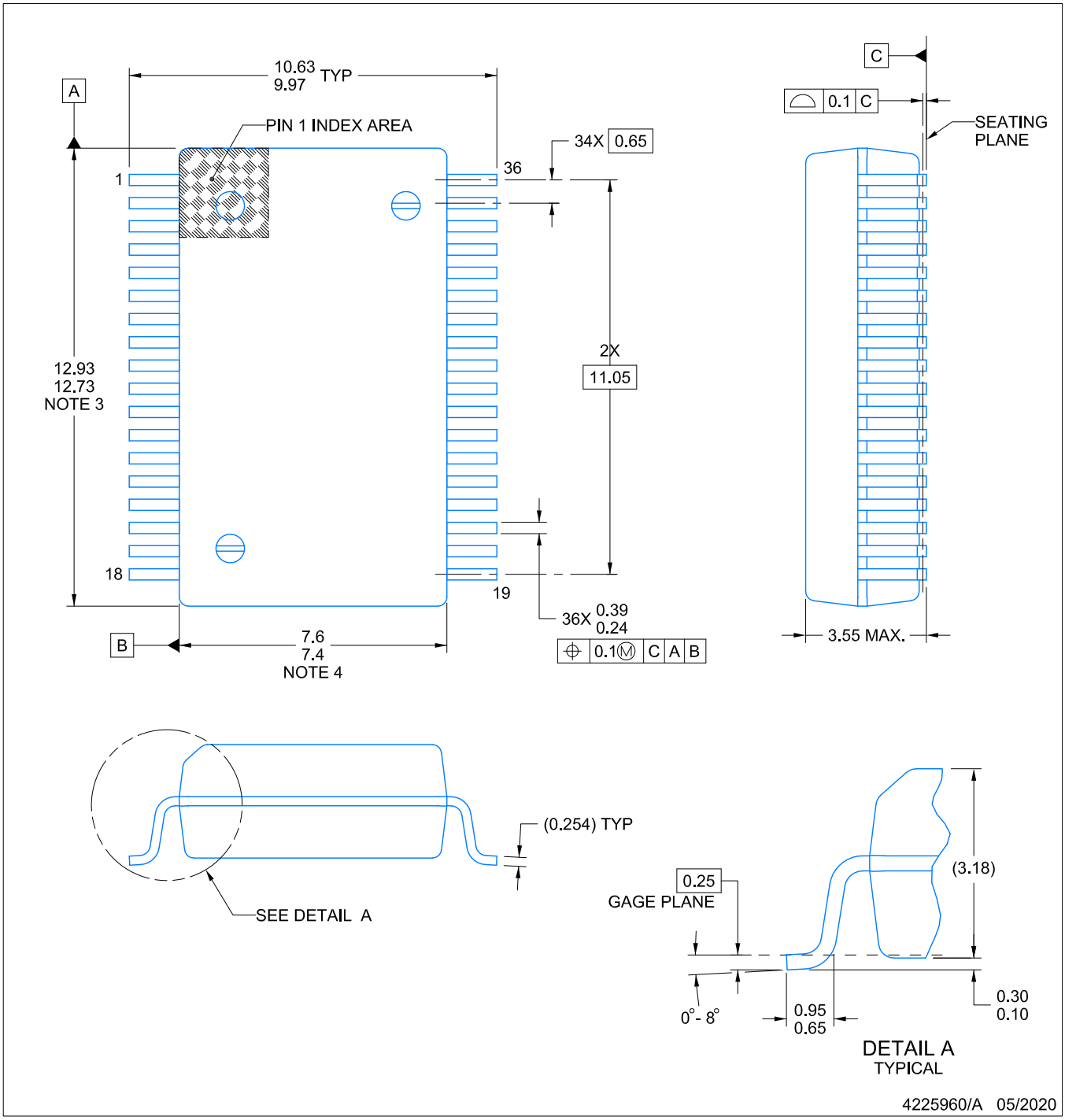
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC14240QDWNRQ1	SO-MOD	DWN	36	750	350.0	350.0	43.0

PACKAGE OUTLINE

DWN0036A

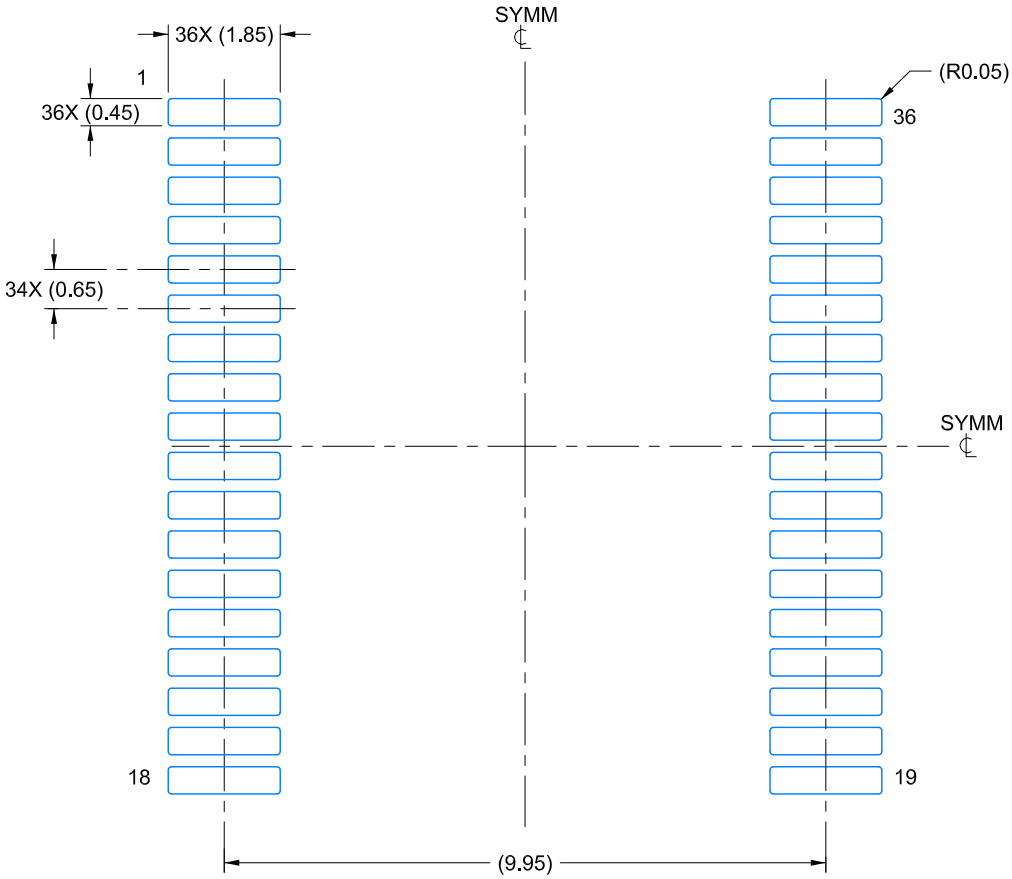
SSOP - 3.55 mm max height

SMALL OUTLINE PACKAGE

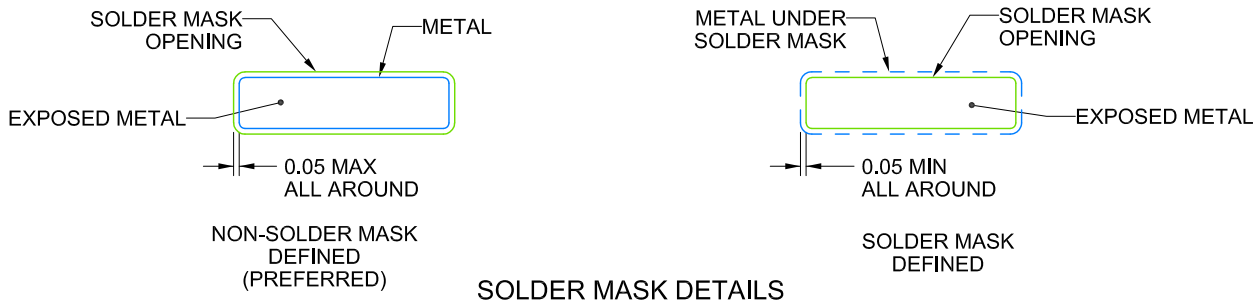


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

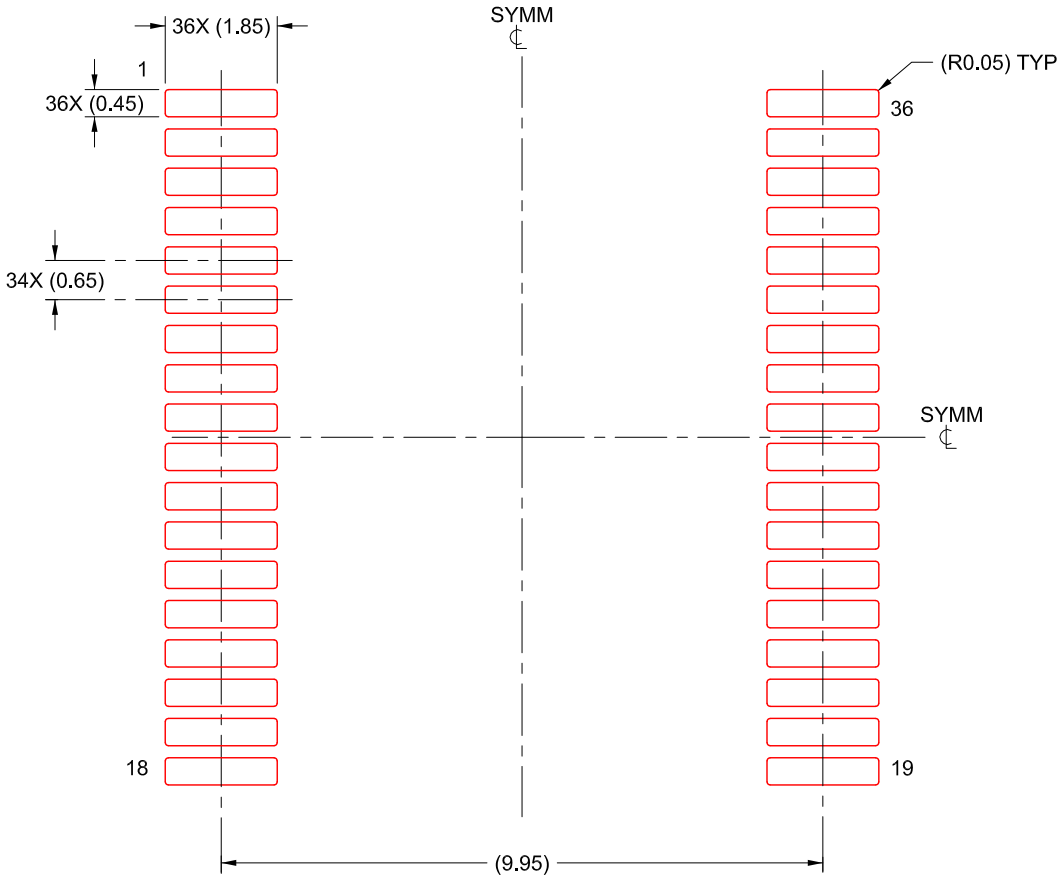


SOLDER MASK DETAILS

4225960/A 05/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4225960/A 05/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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