UCC21738-Q1 アクティブ保護機能と高 CMTI 搭載、SiC/IGBT 向け、車載用、10A ソース / シンク、強化絶縁型シングル・チャネル・ゲート・ドライバ

1 特長

- 5.7kV$_{RMS}$ のシングル・チャネル絶縁型ゲート・ドライバ
- 下記の内容で AEC-Q100 認定済み:
  - デバイス温度グレード 1:-40℃～+125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル 3A
  - デバイス CDM ESD 分類レベル C6
- 機能安全品質管理
  - 機能安全システムの設計に役立つ資料を利用可能
- 最高 2121V$_{pk}$ の SiC MOSFET および IGBT
- 最高出力駆動電圧 (VDD-VEE):33V
- ±10A の駆動能力と分割出力
- CMTI:150V/ns 以上
- 高速過電流保護、270ns の応答時間
- 外部アクティブ・ミラー・クランプ
- フォルト発生時の 900mA ソフト・ターンオフ
- システム・フォルト時にパワー・スイッチをオンにするための絶縁側 ASC 入力
- 過電流時の $\overline{\text{FLT}}$ アラームと $\overline{\text{RST}}$/EN からのリセット
- $\overline{\text{RST}}$/EN での高速イネーブル / ディスエーブル応答
- 入力ピンの 40ns 未満のノイズ過渡およびパルスを除去
- VDD の UVLO は 12V (RDY がパワー・グッドになる)
- 最大 5V のオーバー / アンダーシュート過渡電圧に耐える入力 / 出力
- 伝搬遅延時間:130ns 以下、パルス / 部品スキュー:30ns 以下
- 沿面距離と空間距離が 8mm を超える SOIC-16 DW パッケージ
- 動作時の接合部温度:-40℃～150℃

2 アプリケーション

- EV 用トラクション・インバータ
- オンボード・チャージャおよび充電ステーション
- HEV/EV 用 DC/DC コンバータ

3 概要

UCC21738-Q1 は、先進の保護機能、クラス最高の動的性能、堅牢性を持ち合わせ、最高 2121V (DC) で動作する SiC MOSFET および IGBT 用に設計されたガルバニック絶縁型シングル・チャネル・ゲート・ドライバです。本デバイスは最大±10A のピーク・ソース / シンク電流を供給できます。

入力側は SiO$_2$ 容量性絶縁技術によって出力側から絶縁されており、最大 1.5kV$_{RMS}$ の動作電圧、絶縁バリア寿命が 40 年を超える 12.8kV$_{PK}$ のサージ耐性を備えるとともに、小さい部品間スキューと 150V/ns を超える同相過渡耐性 (CMTI) を実現しています。

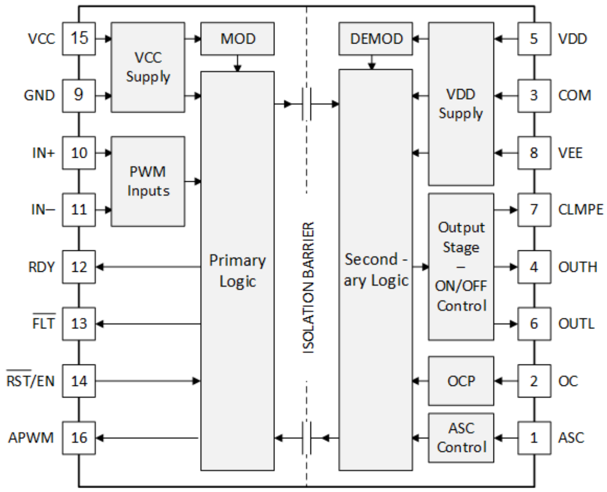
UCC21738-Q1 は、高速の過電流および短絡検出、シャント電流センシング、フォルト通知、アクティブ・ミラー・クランプ、入力側および出力側電源 UVLO などの最新の保護機能を備えているため、SiC および IGBT のスイッチング動作や堅牢性を最適化できます。ASC 機能を使用してシステム障害発生時にパワー・スイッチを強制的にオンにできるため、ドライバの汎用性をさらに高め、システム設計、サイズ、コストを簡素化できます。

製品情報

部品番号(1)	パッケージ	本体サイズ (公称)
UCC21738-Q1	DW SOIC-16	10.3mm × 7.5mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

デバイスのピン構成



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
September 2023	*	Initial Release

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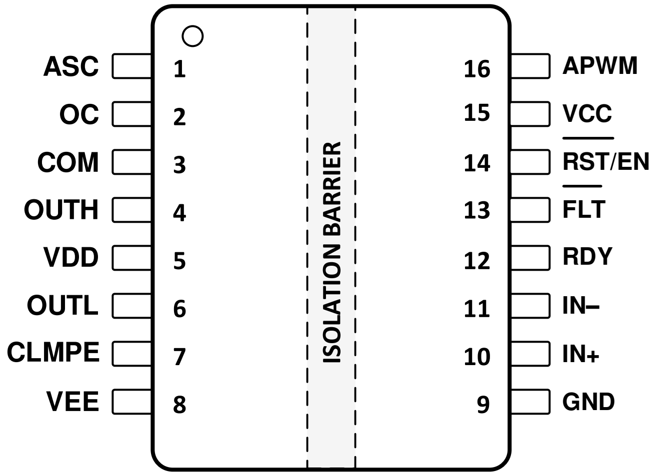
5 Pin Configuration and Functions



Not to scale

図 5-1. UCC21738-Q1 DW SOIC (16) Top View

表 5-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
ASC	1	I	Active high to enable active short circuit function to force output high during system failure events. Tie to COM if unused.
OC	2	I	Overcurrent detection pin for SenseFET, DESAT, and shunt resistor sensing. Tie to COM if unused.
COM	3	P	Common ground reference. Connect to emitter pin for IGBT and source pin for SiC-MOSFET
OUTH	4	O	Gate driver output pull up
VDD	5	P	Positive supply rail for gate drive voltage. Bypass with a >10-µF capacitor to COM to support specified gate driver source peak current capability. Place decoupling capacitor close to the pin.
OUTL	6	O	Gate driver output pull down
CLMPE	7	O	External active Miller clamp control. Connect this pin to the gate of the external Miller clamp MOSFET. Leave floating if unused.
VEE	8	P	Negative supply rail for gate drive voltage. Bypass with a >10-µF capacitor to COM to support specified gate driver sink peak current capability. Place decoupling capacitor close to the pin.
GND	9	P	Input power supply and logic ground reference
IN+	10	I	Noninverting gate driver control input. Tie to VCC if unused.
IN–	11	I	Inverting gate driver control input. Tie to GND if unused.
RDY	12	O	Power good for VCC-GND, VDD-COM. RDY is open drain configuration and can be paralleled with other RDY signals.
$\overline{\text{FLT}}$	13	O	Active low fault alarm output upon overcurrent or short circuit. $\overline{\text{FLT}}$ is in open drain configuration and can be paralleled with other faults.
$\overline{\text{RST}}$/EN	14	I	The $\overline{\text{RST}}$/EN serves two purposes: 1) Enable or shutdown the output side. The FET is turned off by a regular turn-off if EN is set to low; 2) Resets the OC condition signaled on $\overline{\text{FLT}}$ pin if $\overline{\text{RST}}$/EN is set to low for more than 1000 ns. A reset of signal $\overline{\text{FLT}}$ is asserted at the rising edge of $\overline{\text{RST}}$/EN. For automatic reset function, this pin only serves to enable or shutdown the output side. The FET is turned off by a regular turn-off, if terminal EN is set to low. Tie to IN+ for automatic reset.
VCC	15	P	Input power supply from 3 V to 5.5 V. Bypass with a >1-µF capacitor to GND. Place decoupling capacitor close to the pin.
APWM	16	O	Isolated PWM output monitoring ASC pin status. Leave floating if unused.

(1) P = Power, G = Ground, I = Input, O = Output

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VCC	VCC - GND	–0.3	6	V
VDD	VDD - COM	–0.3	36	V
VEE	VEE - COM	–17.5	0.3	V
V_{MAX}	VDD - VEE	–0.3	36	V
IN+, IN-, $\overline{\text{RST}}$/EN	DC	GND–0.3	VCC	V
	Transient, less than 100 ns (2)	GND–5.0	VCC+5.0	V
ASC	Reference to COM	–0.3	6	V
OC	Reference to COM	–0.3	6	V
OUTH, OUTL	DC	VEE–0.3	VDD	V
	Transient, less than 100 ns (2)	VEE–5.0	VDD+5.0	V
CLMPE	Reference to VEE	–0.3	5	V
RDY, $\overline{\text{FLT}}$, APWM		GND–0.3	VCC	V
$I_{\overline{FLT}}$, I_{RDY}	$\overline{\text{FLT}}$ and RDY pin input current		20	mA
I_{APWM}	APWM pin output current		20	mA
T_J	Junction Temperature	–40	150	°C
T_{stg}	Storage Temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime

(2) Values are verified by characterization on bench.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD classification level 3A	±4000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C6	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VCC	VCC-GND	3	5.5	V
VDD	VDD-COM	13	33	V
VEE	VEE-COM	-16	0	V
V_{MAX}	VDD-VEE		33	V
IN+, IN-, $\overline{\text{RST}}$/EN	Reference to GND, High level input voltage	0.7xVCC	VCC	V
	Reference to GND, Low level input voltage	0	0.3xVCC	V
ASC	Reference to COM	0	5	V
$t_{\overline{RST}/EN}$	Minimum pulse width that reset the fault	1000		ns
T_A	Ambient temperature	–40	125	°C

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6.3 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_J	Junction temperature	–40	150	°C

6.4 Thermal Information

THERMAL METRIC[1]		UCC21738-Q1	UNIT
		DW (SOIC)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	27.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	32.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	VCC = 5V, VDD-COM = 20V, COM-VEE = 5V, IN+/– = 5V, 150kHz, 50% Duty Cycle for 10nF load, T_a = 25℃			985	mW
P_{D1}	Maximum power dissipation (side-1)				20	mW
P_{D2}	Maximum power dissipation (side-2)				965	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material Group	According to IEC 60664–1	I	
	Overvoltage Category per IEC 60664–1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test	1500	V_{RMS}
		DC voltage	2121	V_{DC}
V_{IMP}	Maximum impulse voltage	Tested in air, 1.2/50-µs waveform per IEC 62368-1	8000	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM}, t = 60 s (qualification test)	8000	V_{PK}
		V_{TEST}= 1.2 × V_{IOTM}, t = 1 s (100% production test)	8000	V_{PK}

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6.6 Insulation Specifications (続き)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50 µs waveform	12800	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, V_{ini} =V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM} = 2545 V_{PK}, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1,V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM} = 3394 V_{PK}, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test), V_{ini} = V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM} = 3977 V_{PK}, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.5 × sin (2πft), f = 1 MHz	~ 1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	≥ 10^{12}	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	≥ 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	≥ 10^{9}	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	V_{TEST} = V_{ISO} = 5700 V_{RMS}, t = 60 s (qualification), V_{TEST} = 1.2 × V_{ISO} = 6840 V_{RMS}, t = 1 s (100% production)	5700	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-pin device.

6.7 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheatthe die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{θJA}$ = 68.3°C/W, V_{DD} = 15 V, V_{EE} = -5V, T_J = 150°C, T_A = 25°C			61	mA
		$R_{θJA}$ = 68.3°C/W, V_{DD} = 20 V, V_{EE} = -5V, T_J = 150°C, T_A = 25°C			49	
P_S	Safety input, output, or total power	$R_{θJA}$ = 68.3°C/W, V_{DD} = 20 V, V_{EE} = -5V, T_J = 150°C, T_A = 25°C			1220	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J , specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A. The junction-to-air thermal resistance, R_{qJA}, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter: $T_J = T_A + R_{qJA}$ ´ P, where P is the power dissipated in the device. $T_{J(max)} = T_S = T_A + R_{qJA}$ ´ P_S, where $T_{J(max)}$ is the maximum allowed junction temperature. $P_S = I_S$ ´ V_I , where VI is the maximum supply voltage.

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6.8 Electrical Characteristics

VCC = 3.3 V or 5.0 V, 1-µF capacitor from VCC to GND, VDD–COM = 20 V, 18 V or 15 V, COM–VEE = 5 V, 8 V or 15 V, C_L = 100pF, –40°C<T_J<150°C (unless otherwise noted)(1)(2).

Parameter		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC UVLO THRESHOLD AND DELAY						
V_{VCC_ON}	VCC - GND		2.55	2.7	2.85	V
V_{VCC_OFF}			2.35	2.5	2.65	V
V_{VCC_HYS}				0.2		V
t_{VCCFIL}	VCC UVLO deglitch time			10		µs
$t_{VCC+\ to\ OUT}$	VCC UVLO on delay to output high	IN+ = VCC, IN– = GND	28	37.8	55	µs
$t_{VCC-\ to\ OUT}$	VCC UVLO off delay to output low		5	10	15	µs
$t_{VCC+\ to\ RDY}$	VCC UVLO on delay to RDY high	$\overline{RST}$/EN = VCC	30	37.8	55	µs
$t_{VCC-\ to\ RDY}$	VCC UVLO off delay to RDY low		5	10	15	µs
VDD UVLO THRESHOLD AND DELAY						
V_{VDD_ON}	VDD - COM		10.5	11.4	12.8	V
V_{VDD_OFF}			9.9	10.6	11.8	V
V_{VDD_HYS}				0.8		V
t_{VDDFIL}	VDD UVLO deglitch time			5		µs
$t_{VDD+\ to\ OUT}$	VDD UVLO on delay to output high	IN+ = VCC, IN– = GND	2	5	15	µs
$t_{VDD-\ to\ OUT}$	VDD UVLO off delay to output low			5	15	µs
$t_{VDD+\ to\ RDY}$	VDD UVLO on delay to RDY high	$\overline{RST}$/EN = VCC		10	15	µs
$t_{VDD-\ to\ RDY}$	VDD UVLO off delay to RDY low			10	15	µs
VCC, VDD QUIESCENT CURRENT						
I_{VCCQ}	VCC quiescent current	OUT(H) = High, f_S = 0Hz	2.5	3	4	mA
		OUT(L) = Low, f_S = 0Hz	1.45	2	2.75	mA
I_{VDDQ}	VDD quiescent current	OUT(H) = High, f_S = 0Hz	2.4	3.1	5.3	mA
		OUT(L) = Low, f_S = 0Hz	2.2	2.9	4.7	mA
LOGIC INPUTS - IN+, IN- and $\overline{RST}$/EN						
V_{INH}	Input high threshold	VCC=3.3V		1.85	2.31	V
V_{INL}	Input low threshold		0.99	1.52		V
V_{INHYS}	Input threshold hysteresis			0.33		V
I_{IH}	Input high level input leakage current	V_{IN} = VCC		90		uA
I_{IL}	Input low level input leakage current	V_{IN} = GND		-90		uA
R_{IND}	Input pins pull down resistance			55		kΩ
R_{INU}	Input pins pull up resistance			55		kΩ
T_{INFIL}	IN+, IN– and $\overline{RST}$/EN deglitch (ON and OFF) filter time	f_S = 50kHz	28	40	60	ns
T_{RSTFIL}	Deglitch filter time to reset $\overline{FLT}$		500	650	800	ns
GATE DRIVER STAGE						
I_{OUTH}	Peak source current	C_L = 0.18µF, f_S = 1kHz		10		A
I_{OUTL}	Peak sink current			10		A
R_{OUTH} (3)	Output pull-up resistance	I_{OUTH} = -0.1A		2.5		Ω
R_{OUTL}	Output pull-down resistance	I_{OUTL} = 0.1A		0.3		Ω
V_{OUTH}	High level output voltage	I_{OUTH} = -0.2A, VDD = 18V		17.5		V
V_{OUTL}	Low level output voltage	I_{OUTL}= 0.2A		60		mV
ACTIVE PULLDOWN						

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6.8 Electrical Characteristics (続き)

VCC = 3.3 V or 5.0 V, 1-µF capacitor from VCC to GND, VDD–COM = 20 V, 18 V or 15 V, COM–VEE = 5 V, 8 V or 15 V, C_L = 100pF, –40°C<T_J<150°C (unless otherwise noted)(1)(2).

Parameter		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUTPD}	Output active pull down on OUTL	$I_{OUTL(typ)}$ = 0.1×$I_{OUTL(typ)}$, VDD=OPEN, VEE=COM	1.5	2.0	2.5	V
EXTERNAL ACTIVE MILLER CLAMP						
V_{CLMPTH}	Miller clamp threshold voltage	Reference to VEE	1.5	2.0	2.5	V
V_{CLMPE}	Output high voltage		4.8	5	5.3	V
I_{CLMPEH}	Peak source current	C_{CLMPE} = 10nF	0.12	0.25		A
I_{CLMPEL}	Peak sink current		0.12	0.25	0.37	A
t_{CLMPER}	Rising time	C_{CLMPE} = 330pF		20	40	ns
t_{DCLMPE}	Miller clamp ON delay time			40	70	ns
SHORT CIRCUIT CLAMPING						
$V_{CLP\text{-}OUT(H)}$	V_{OUTH}–VDD	OUT = High, $I_{OUT(H)}$ = 500mA, t_{CLP}=10µs		0.9		V
$V_{CLP\text{-}OUT(L)}$	V_{OUTL}–VDD	OUT = High, $I_{OUT(L)}$ = 500mA, t_{CLP}=10µs		1.8		V
OC PROTECTION						
I_{DCHG}	OC pull down current	V_{OC} = 1V		40		mA
V_{OCTH}	Detection threshold		0.63	0.7	0.77	V
V_{OCL}	Voltage when OUTL = Low	Reference to COM, I_{OC} = 5mA		0.13		V
t_{OCFIL}	OC fault deglitch filter		95	120	180	ns
t_{OCOFF}	OC propagation delay to OUTL 90%		150	270	400	ns
t_{OCFLT}	OC to $\overline{\text{FLT}}$ low delay		300	530	750	ns
INTERNAL SOFT TURN OFF						
I_{STO}	Soft turn-off current on fault condition	VDD-VEE = 20 V, OUTL = 8 V	500	900	1200	mA
ACTIVE SHORT CIRCUIT (ASC)						
V_{ASCL}	ASC input low threshold		1.35	1.5	1.71	V
V_{ASCH}	ASC input high threshold		2.7	2.9	3.17	V
t_{ASC_r}	ASC to output rising edge delay		390	660	1120	ns
t_{ASC_f}	ASC to output falling edge delay		152	300	477	ns
APWM Monitor						
f_{APWM}	APWM output frequency	V_{ASC}=2.5V	360	400	440	kHz
D_{APWM}	APWM duty cycle	V_{ASC}=0.6V	9	11.5	13.5	%
		V_{ASC}=2.5V	48.5	50	51.5	%
		V_{ASC}=4.5V	87.5	90	92.5	%
FLT AND RDY REPORTING						
t_{RDYHLD}	VDD UVLO RDY low minimum holding time		0.55		1	ms
$t_{FLTMUTE}$	Output mute time on fault	Reset fault through $\overline{\text{RST}}$/EN	0.55		1	ms
R_{ODON}	Open drain output on resistance	I_{ODON} = 5mA		30		Ω
V_{ODL}	Open drain low output voltage				0.3	V
COMMON MODE TRANSIENT IMMUNITY						
CMTI	Common-mode transient immunity	V_{CM} = 1500 V	150			V/ns

(1) Currents are positive into and negative out of the specified terminal.
(2) All voltages are referenced to COM unless otherwise notified.

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(3) For internal PMOS only. Refer to Driver Stage for effective pull-up resistance.

6.9 Switching Characteristics

VCC = 5.0 V, 1-µF capacitor from VCC to GND, VDD - COM = 20V, 18V or 15V, COM - VEE = 3 V, 5 V or 8 V, C_L = 100pF, -40℃<T_J<150℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PDLH}	Propagation delay time low-to-high		60	90	130	ns
t_{PDHL}	Propagation delay time low-to-high		60	90	130	ns
PWD	Pulse width distortion (t_{PDHL}-t_{PDLH})				30	ns
t_{sk-pp}	Part to part skew	Rising or falling propagation delay			30	ns
t_r	Driver output rise time	C_L = 10nF		33		ns
t_f	Driver output fall time	C_L = 10nF		27		ns
f_{MAX}	Maximum switching frequency				1	MHz

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6.10 Insulation Characteristics Curves

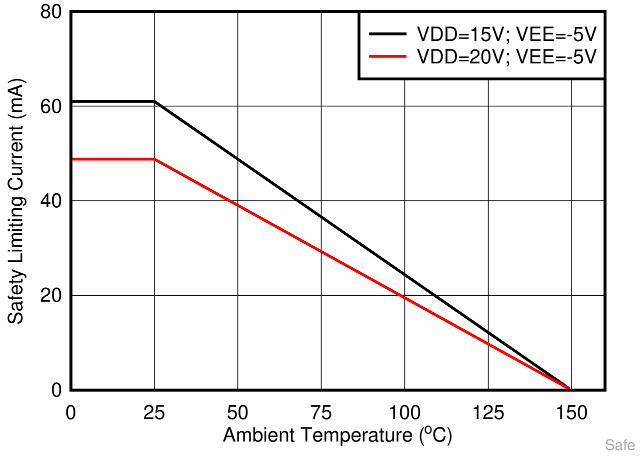

図 6-1. Thermal Derating Curve for Limiting Current per VDE

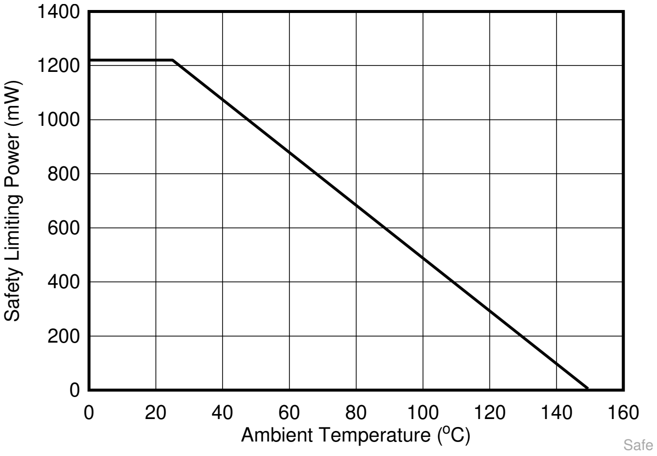

図 6-2. Thermal Derating Curve for Limiting Power per VDE

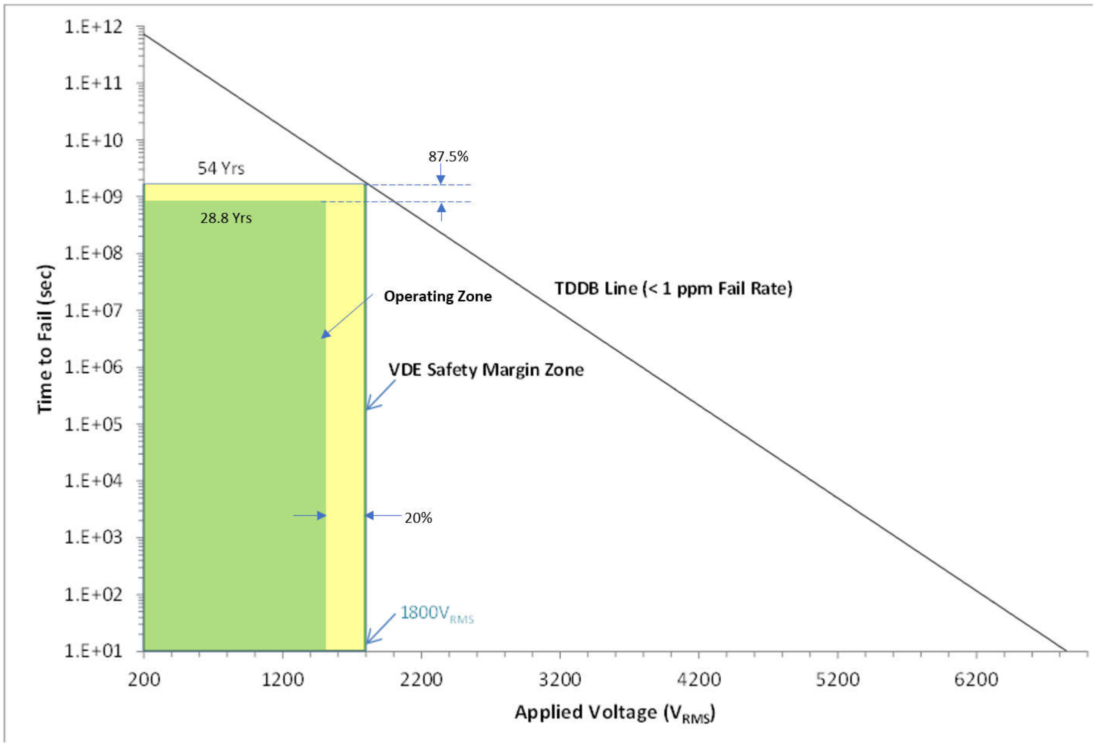

図 6-3. Reinforced Isolation Capacitor Lifetime Projection

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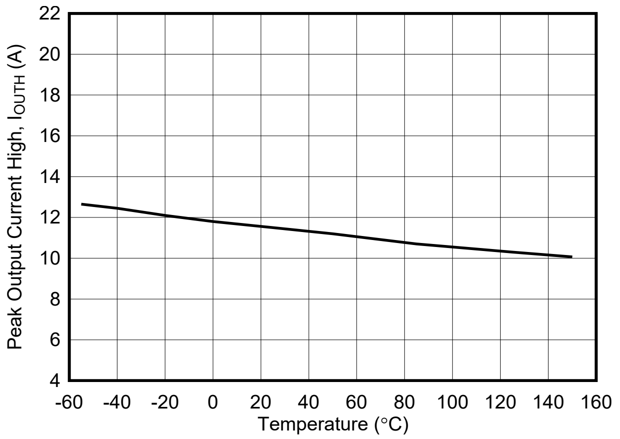
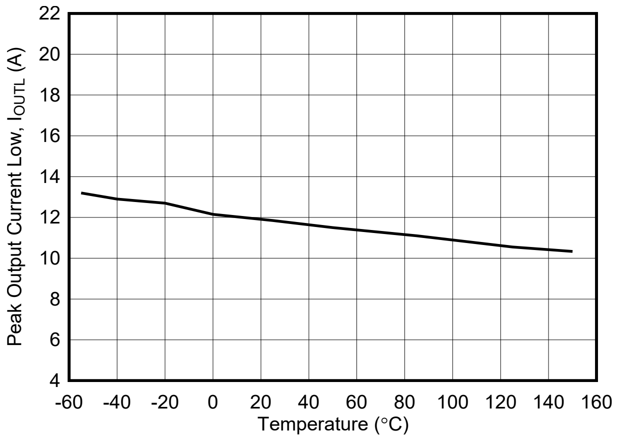
6.11 Typical Characteristics



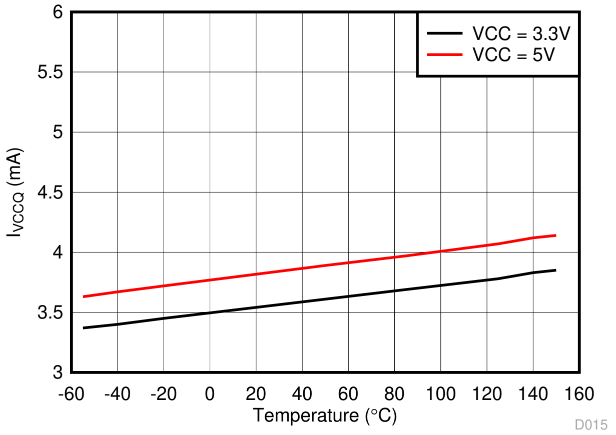
V_{DD} = 20 V, V_{EE} = –5 V

図 6-4. Output High Drive Current vs Temperature



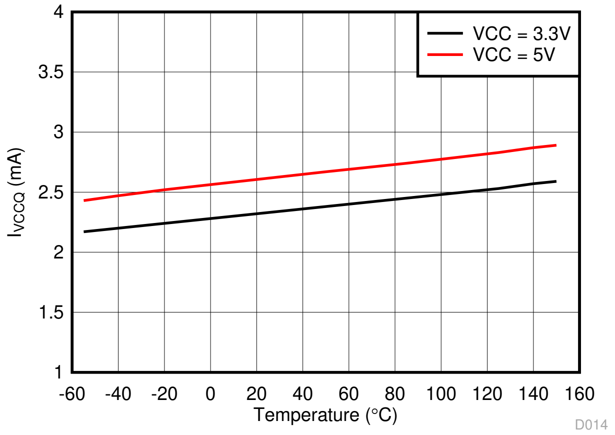
V_{DD} = 20 V, V_{EE} = –5 V

図 6-5. Output Low Driver Current vs Temperature



IN+ = High IN- = Low

図 6-6. I_{VCCQ} Supply Current vs Temperature



IN+ = Low IN- = Low

図 6-7. I_{VCCQ} Supply Current vs Temperature

6.11 Typical Characteristics

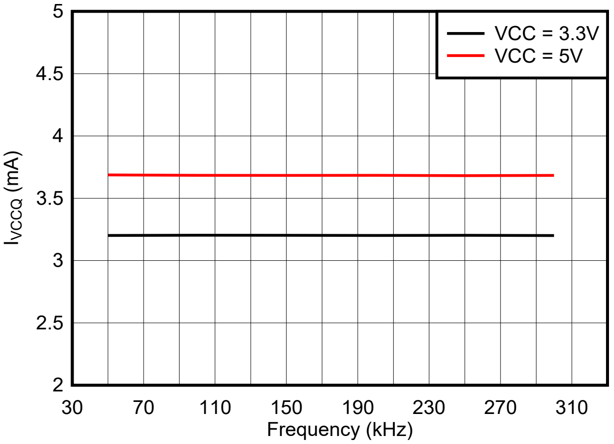
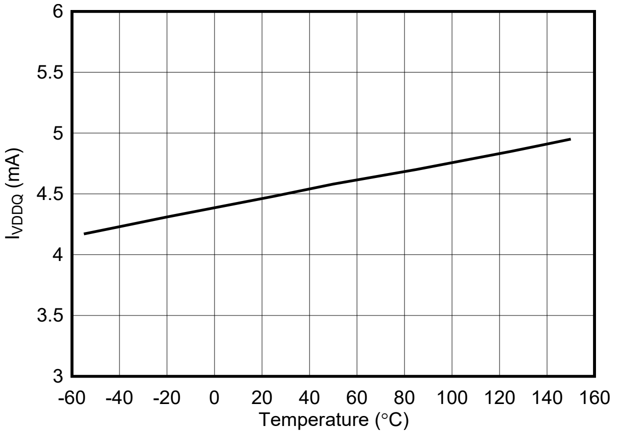
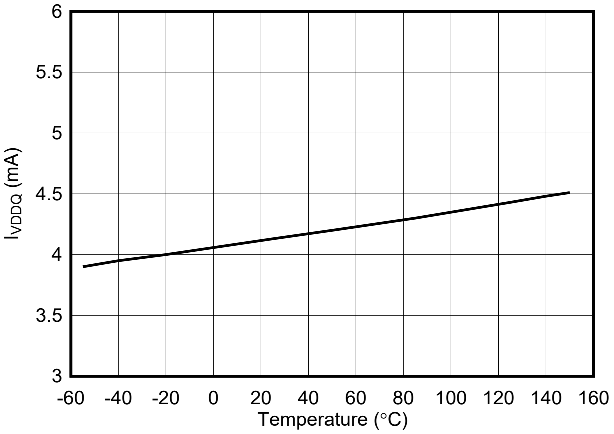


図 6-8. I_{VCCQ} Supply Current vs Input Frequency



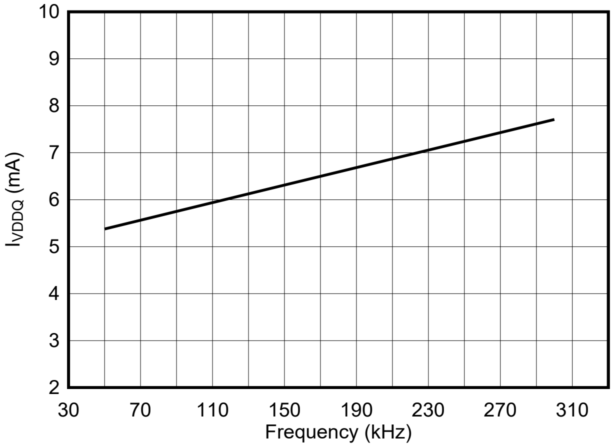
V_{DD} = 20 V, V_{EE} = –5 V IN+ = High, IN- = Low

図 6-9. I_{VDDQ} Supply Current vs Temperature



V_{DD} = 20 V, V_{EE} = –5 V IN+ = Low, IN- = Low

図 6-10. I_{VDDQ} Supply Current vs Temperature



VDD/VEE = 20 V/–5 V

図 6-11. I_{VDDQ} Supply Current vs Input Frequency

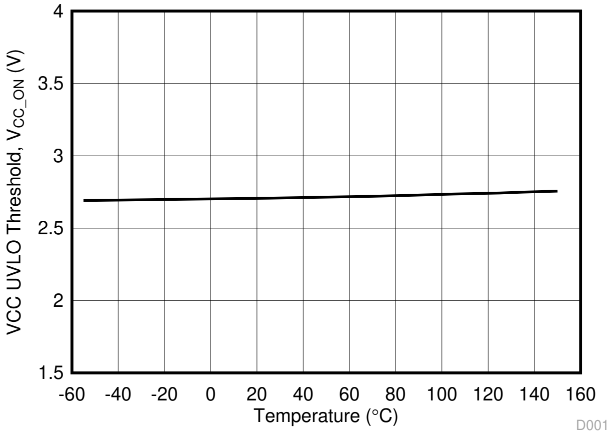


図 6-12. VCC UVLO vs Temperature

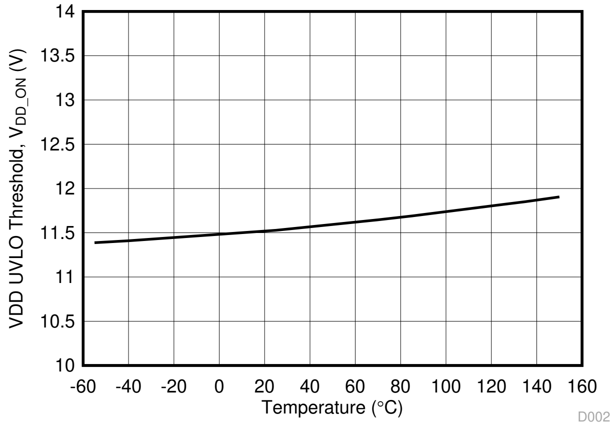
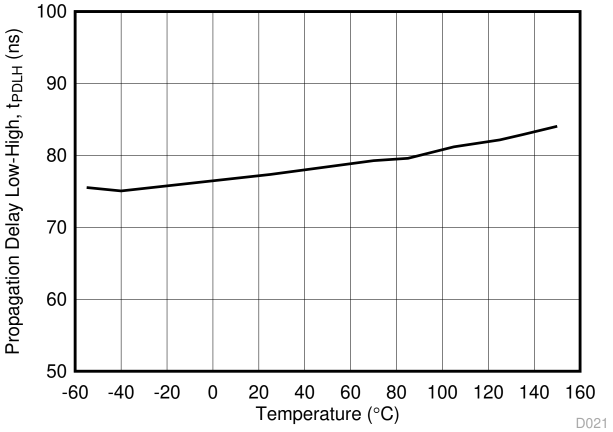


図 6-13. VDD UVLO vs Temperature

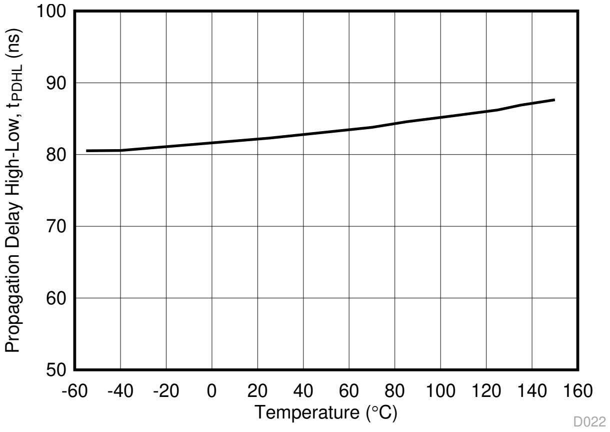
6.11 Typical Characteristics



V_{CC} = 3.3 V V_{DD} = 18 V C_L = 100 pF

R_{ON} = 0 Ω R_{OFF} = 0 Ω

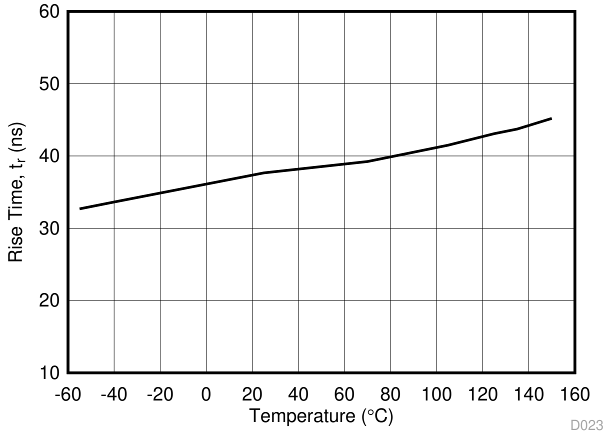
図 6-14. Propagation Delay t_{PDLH} vs Temperature



V_{CC} = 3.3 V V_{DD} = 18 V C_L = 100 pF

R_{ON} = 0 Ω R_{OFF} = 0 Ω

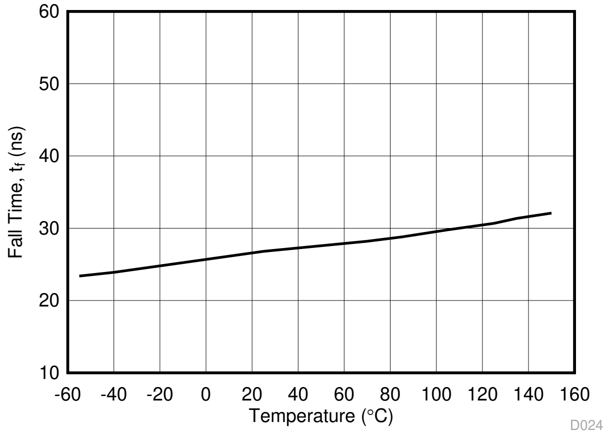
図 6-15. Propagation Delay t_{PDHL} vs Temperature



V_{CC} = 3.3 V V_{DD} = 18 V C_L = 10 nF

R_{ON} = 0 Ω R_{OFF} = 0 Ω

図 6-16. t_r Rise Time vs Temperature



V_{CC} = 3.3 V V_{DD} = 18 V C_L = 10 nF

R_{ON} = 0 Ω R_{OFF} = 0 Ω

図 6-17. t_f Fall Time vs Temperature

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6.11 Typical Characteristics

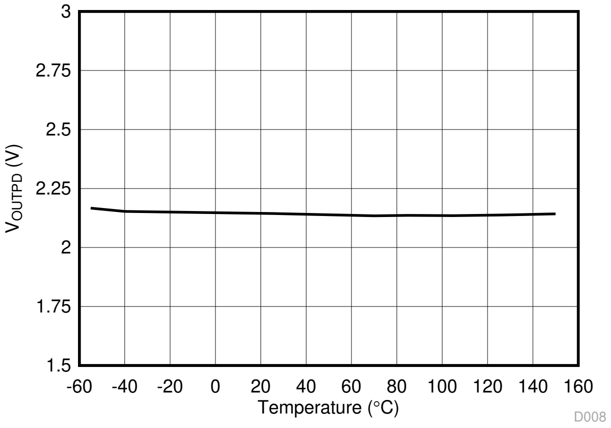

図 6-18. V_{OUTPD} Output Active Pulldown Voltage vs Temperature

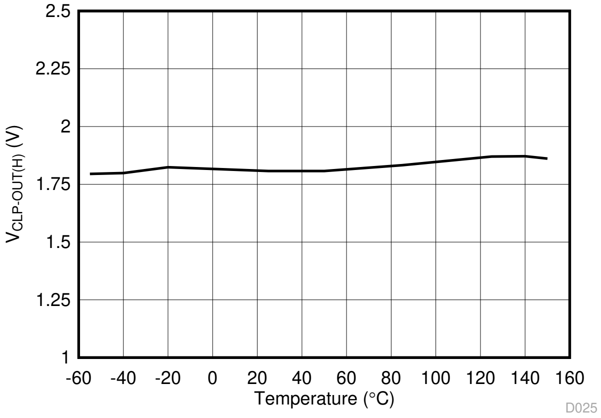

図 6-19. $V_{CLP-OUT(H)}$ Short Circuit Clamping Voltage vs Temperature

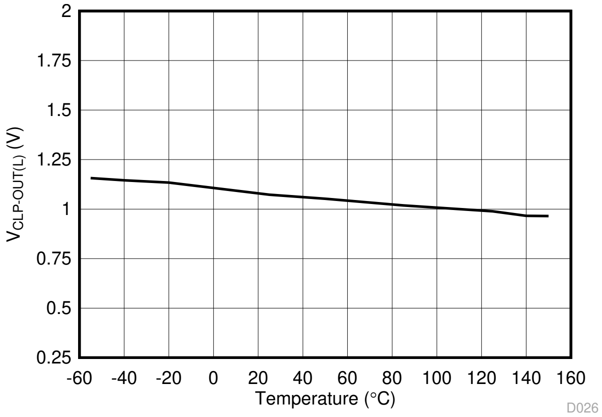

図 6-20. $V_{CLP-OUT(L)}$ Short Circuit Clamping Voltage vs Temperature

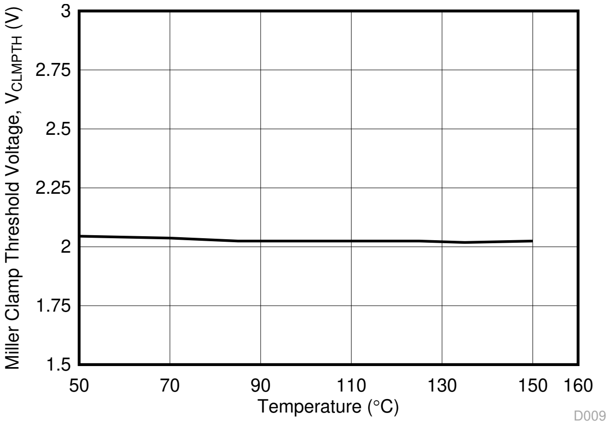

図 6-21. V_{CLMPTH} Miller Clamp Threshold Voltage vs Temperature

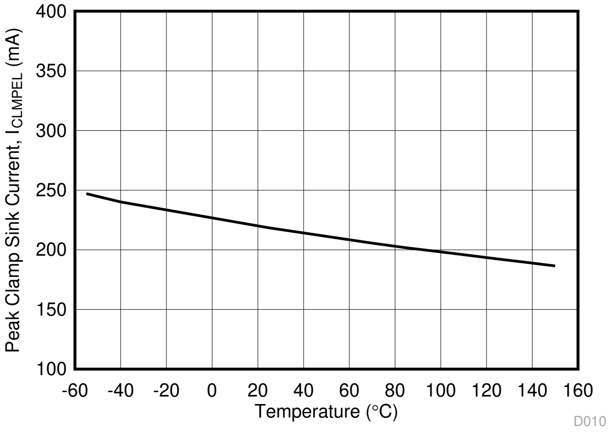

図 6-22. I_{CLMPEL} Miller Clamp Sink Current vs Temperature

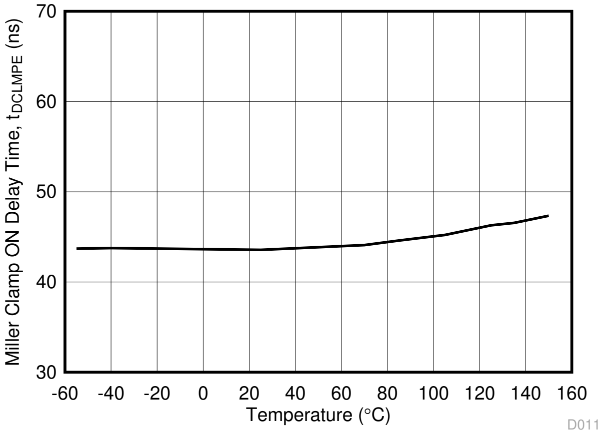

図 6-23. t_{DCLMPE} Miller Clamp ON Delay Time vs Temperature

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6.11 Typical Characteristics (continued)

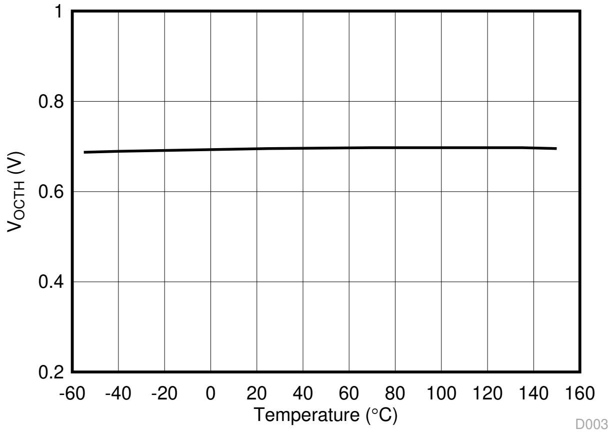

図 6-24. V_{OCTH} OC Detection Threshold vs Temperature

7 Parameter Measurement Information

7.1 Propagation Delay

7.1.1 Regular Turn-OFF

図 7-1 shows the propagation delay measurement for noninverting configurations. 図 7-2 shows the propagation delay measurement with the inverting configurations.

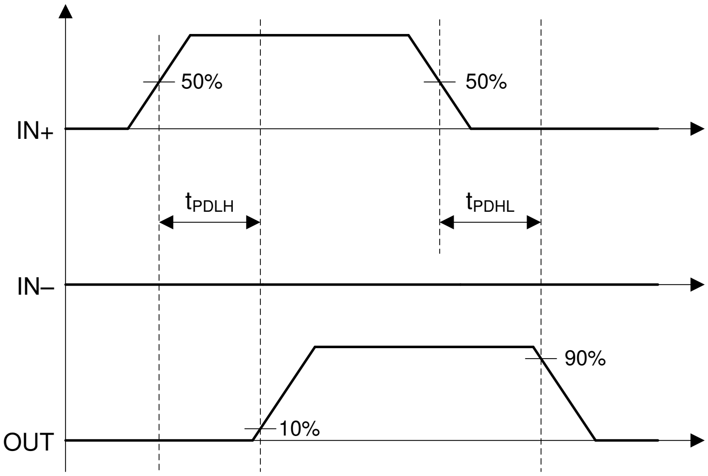

図 7-1. Noninverting Logic Propagation Delay Measurement

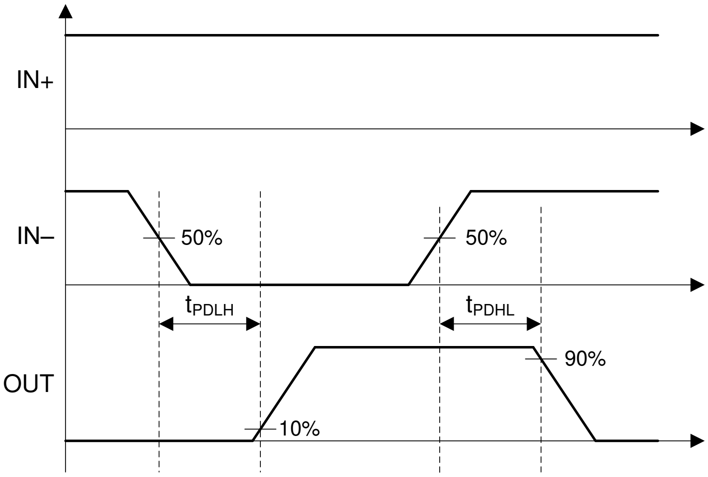

図 7-2. Inverting Logic Propagation Delay Measurement

7.2 Input Deglitch Filter

In order to increase the robustness of gate driver over noise transient and accidental small pulses on the input pins; that is, IN+, IN–, $\overline{\text{RST}}$/EN, a 40-ns deglitch filter is designed to filter out the transients and make sure there is no faulty output responses or accidental driver malfunctions. When the IN+ or IN– PWM pulse is smaller than the input deglitch filter width, T_{INFIL}, there will be no responses on OUT drive signal. 図 7-3 and 図 7-4 show the IN+ pin ON and OFF pulse deglitch filter effect. 図 7-5 and 図 7-6 show the IN– pin ON and OFF pulse deglitch filter effect.

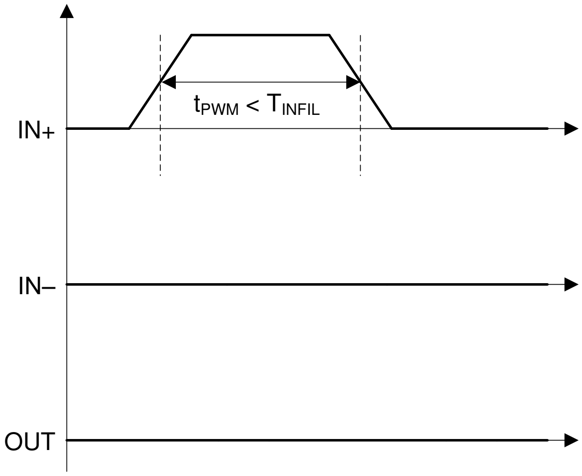

図 7-3. IN+ ON Deglitch Filter

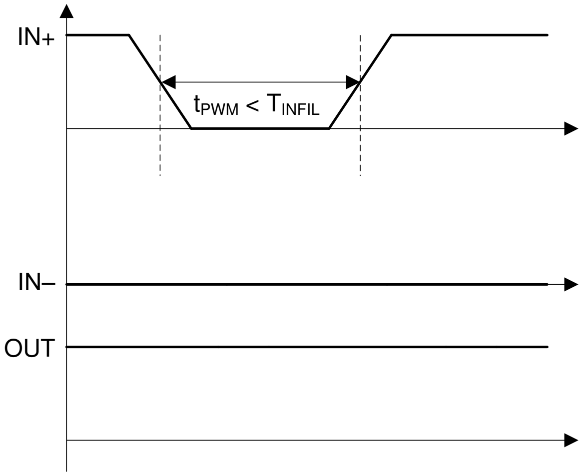

図 7-4. IN+ OFF Deglitch Filter

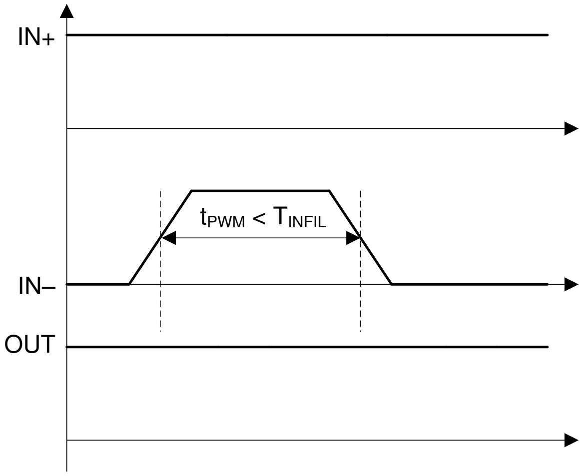

図 7-5. IN– ON Deglitch Filter

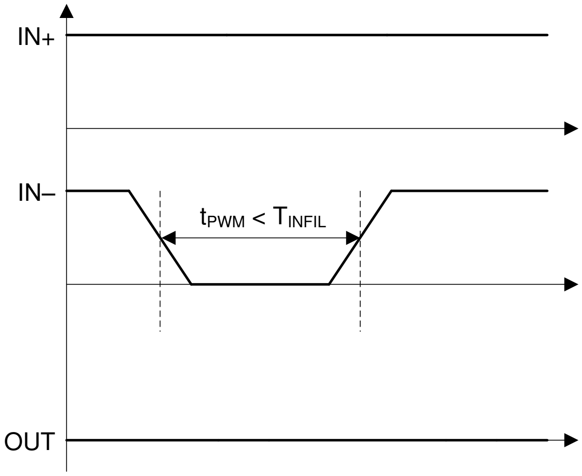

図 7-6. IN– OFF Deglitch Filter

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7.3 Active Miller Clamp

7.3.1 External Active Miller Clamp

An active Miller clamp can help add an additional low impedance path to bypass the Miller current and prevent the high dV/dt introduced unintentional turn-on through the Miller capacitance. Different from the internal active Miller clamp, an external active Miller clamp function is used for applications where the gate driver may not be close to the power device or power module due to system layout considerations. An external active Miller clamp function provides a 5-V gate drive signal to turn on the external Miller clamp FET when the gate driver voltage is less than the Miller clamp threshold, V_{CLMPTH}. 図 7-7 shows the timing diagram for the external active Miller clamp function.

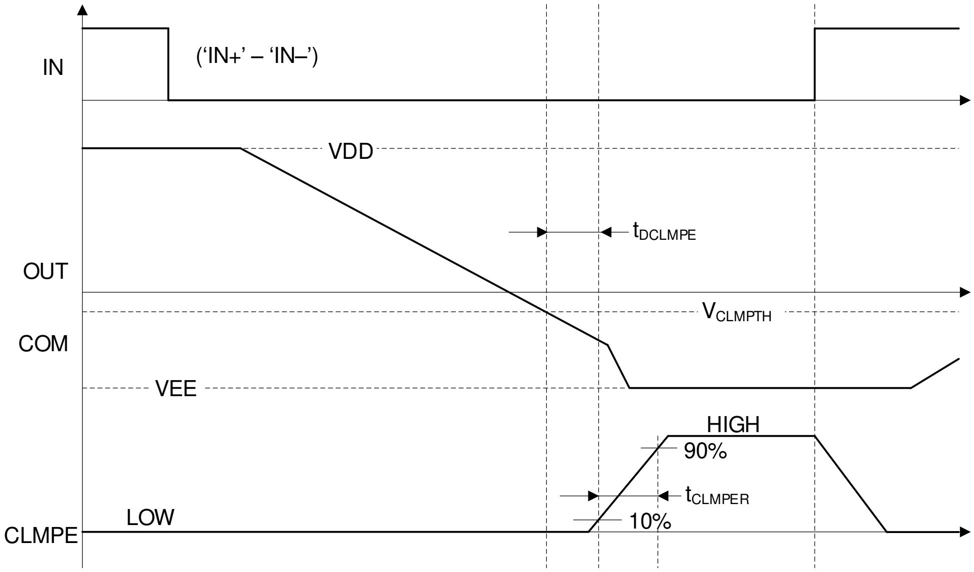

図 7-7. Timing Diagram for External Active Miller Clamp Function

7.4 Undervoltage Lockout (UVLO)

Undervoltage lockout (UVLO) is one of the key protection features designed to protect the system in case of bias supply failures on VCC, the primary side power supply, and VDD, the secondary side power supplies.

7.4.1 VCC UVLO

The VCC UVLO protection details are discussed in this section. 図 7-8 shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN–APWM.

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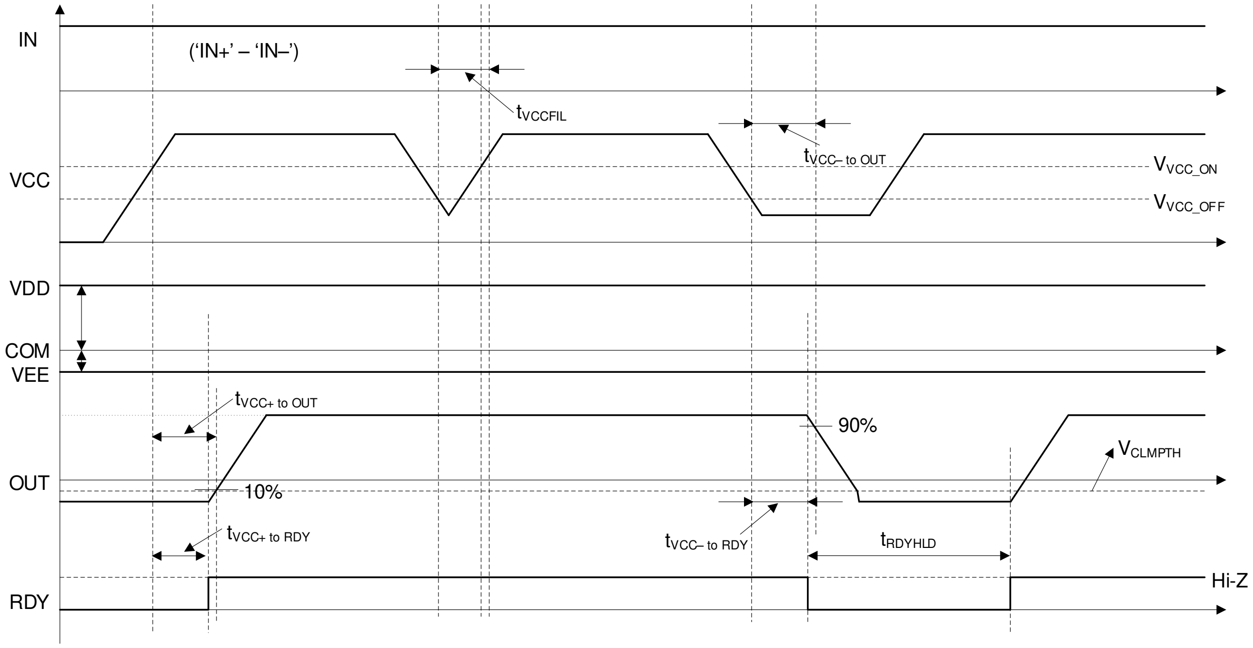

図 7-8. VCC UVLO Protection Timing Diagram

7.4.2 VDD UVLO

The VDD UVLO protection details are discussed in this section. 図 7-9 shows the timing diagram illustrating the definition of UVLO ON/OFF threshold, deglitch filter, response time, RDY and AIN–APWM.

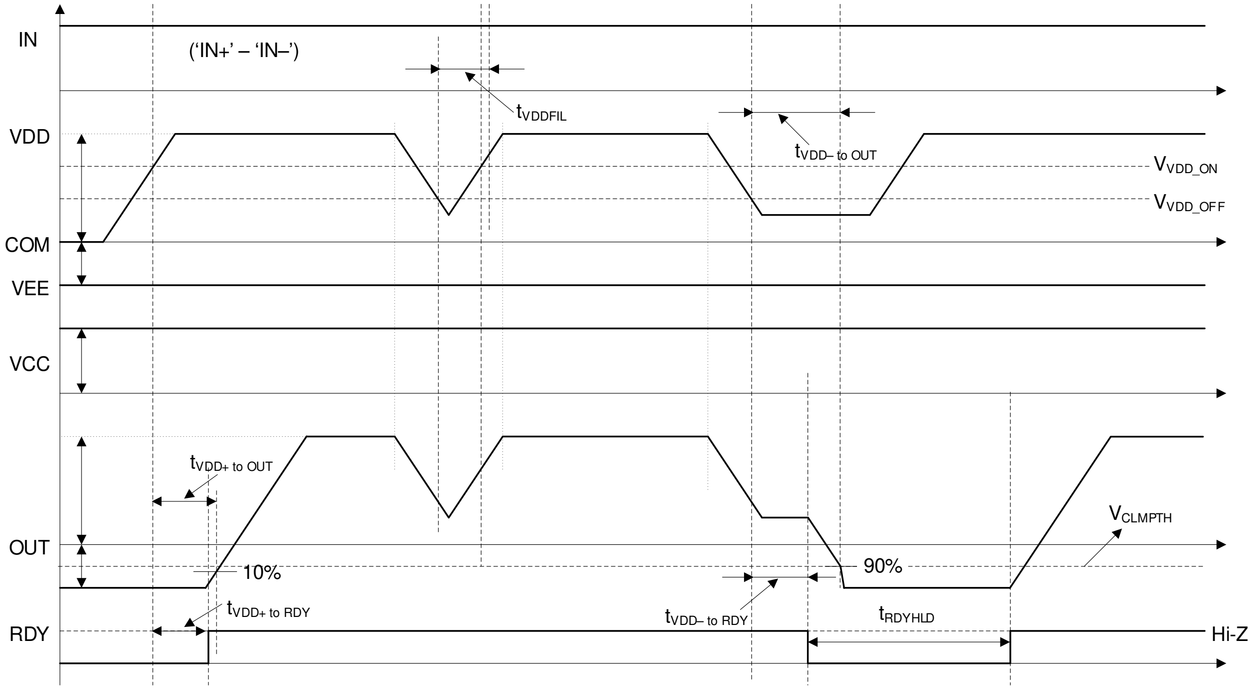

図 7-9. VDD UVLO Protection Timing Diagram

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7.5 Overcurrent (OC) Protection

7.5.1 OC Protection with Soft Turn-OFF

OC protection is used to sense the current of the SiC-MOSFETs and IGBTs under overcurrent or shoot-through condition. 図 7-10 shows the timing diagram of OC operation with soft turn-off.

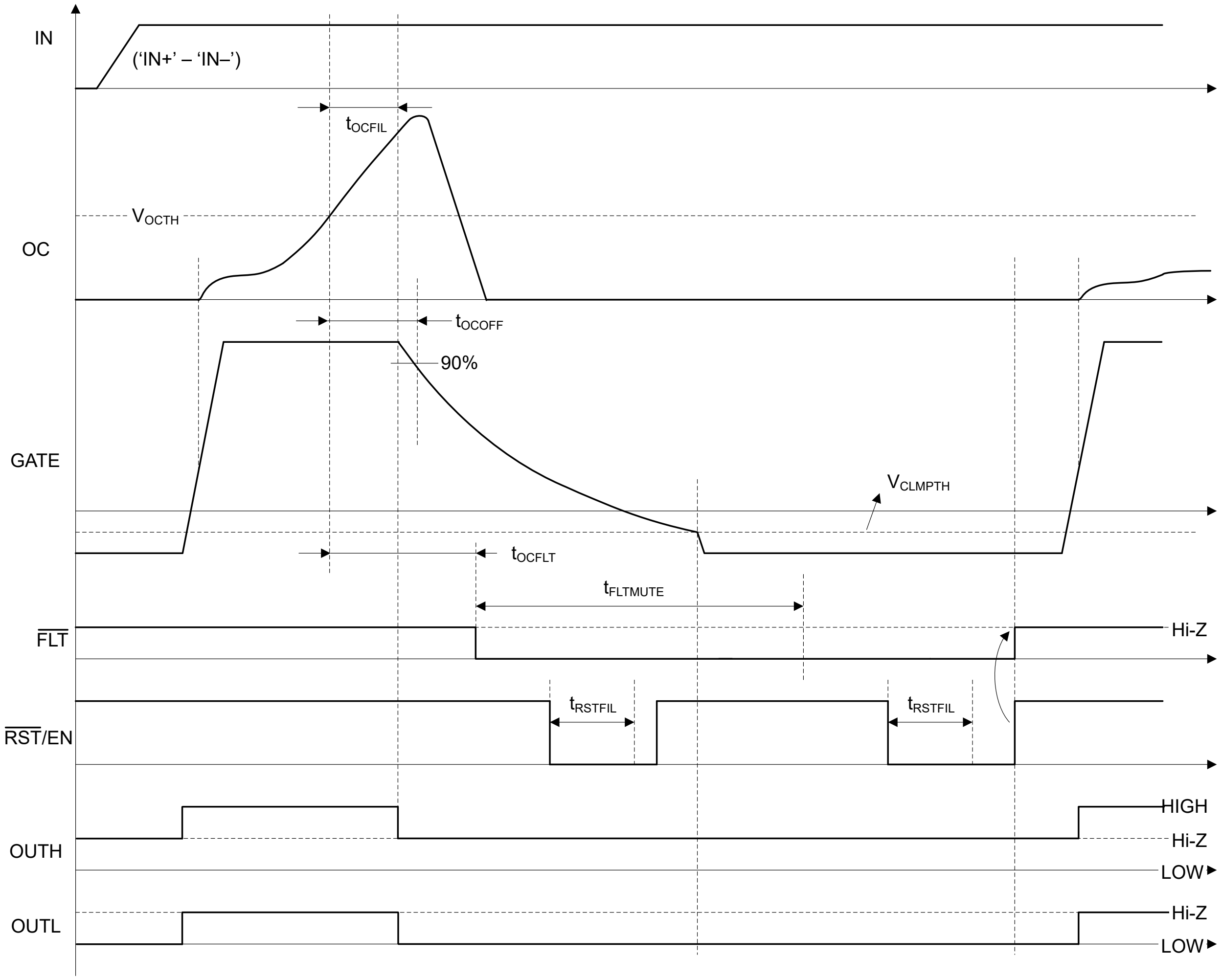

図 7-10. OC Protection with Soft Turn-OFF

7.6 ASC Support

When the ASC pin receives a logic high signal, the output is forced high regardless of the input side pin conditions. The ASC function has higher priority than the input signal and VCC UVLO. The priority of VDD UVLO, and the overcurrent fault event are higher than the ASC function.

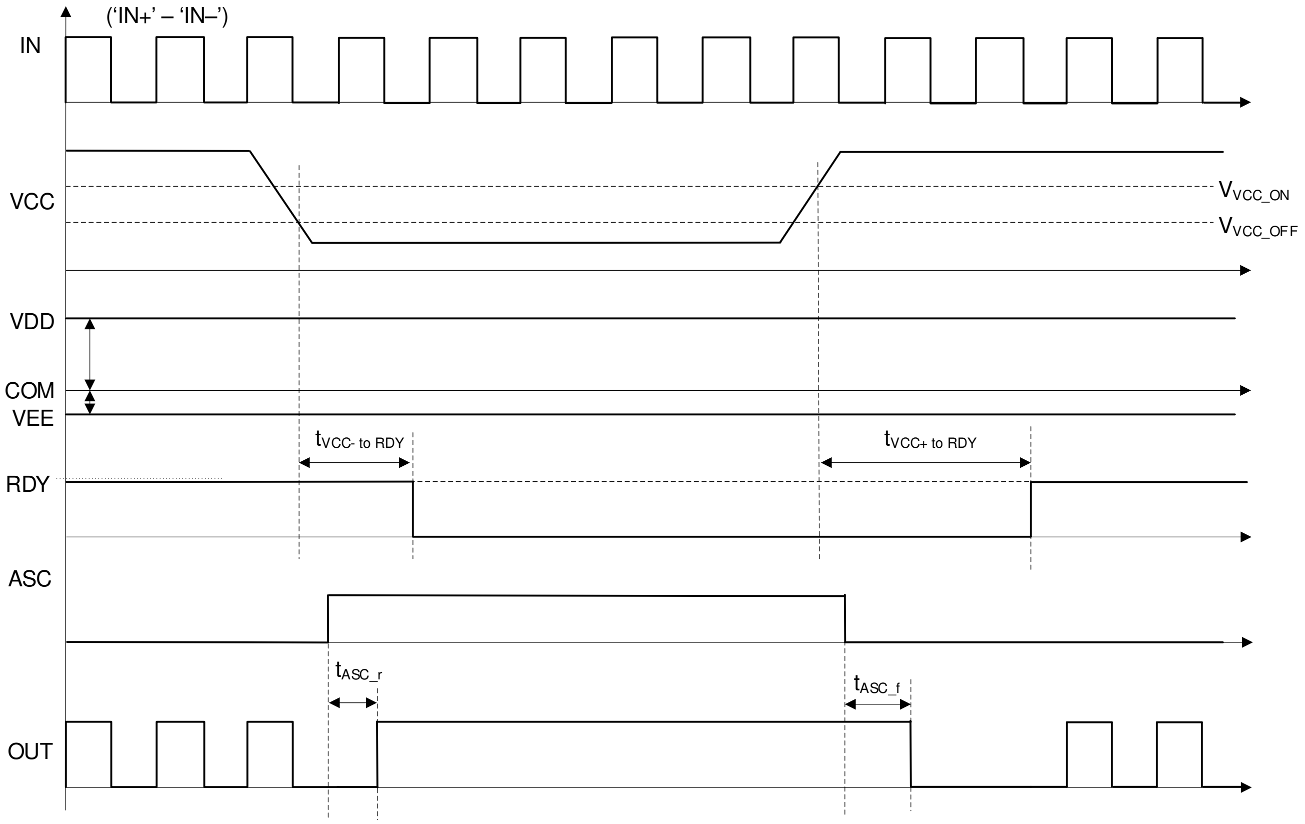

図 7-11. ASC Support with VCC UVLO

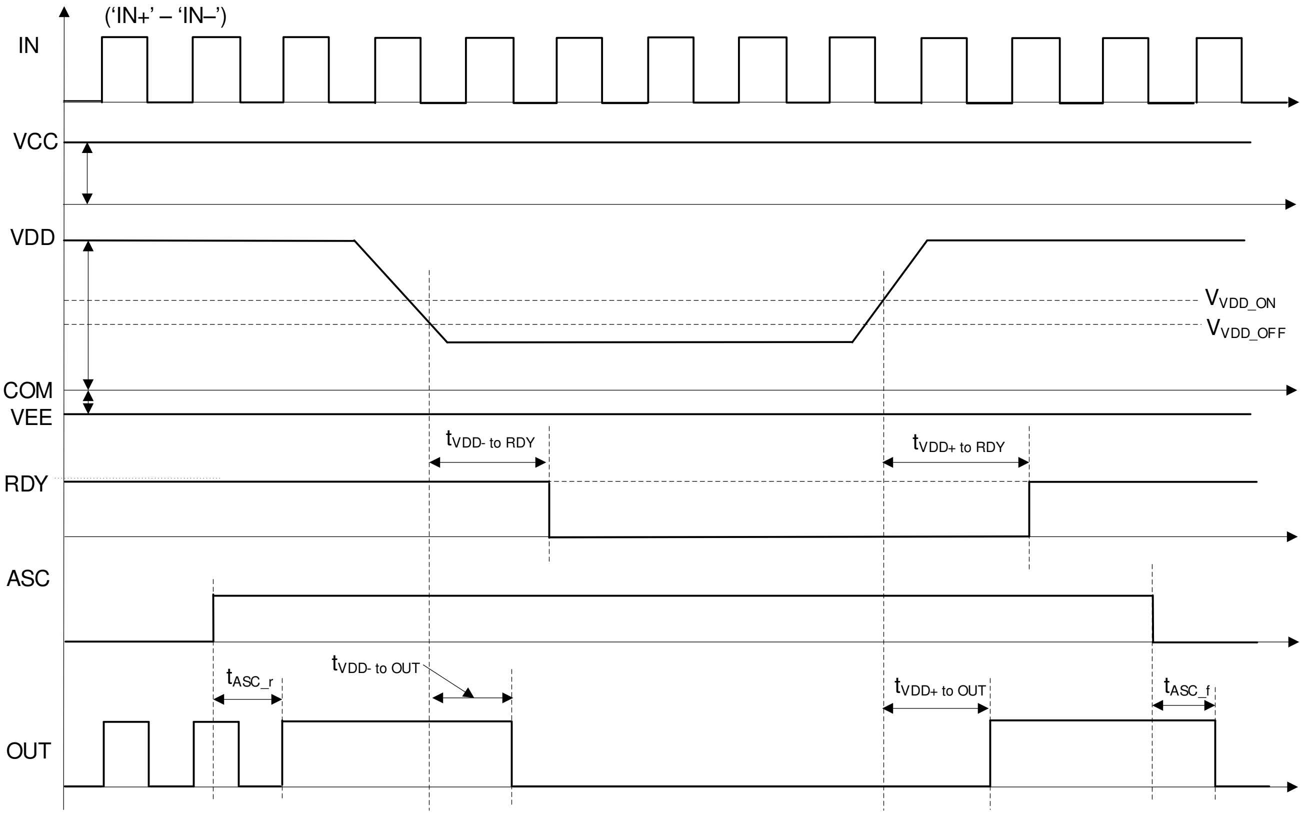

図 7-12. ASC Support with VDD UVLO

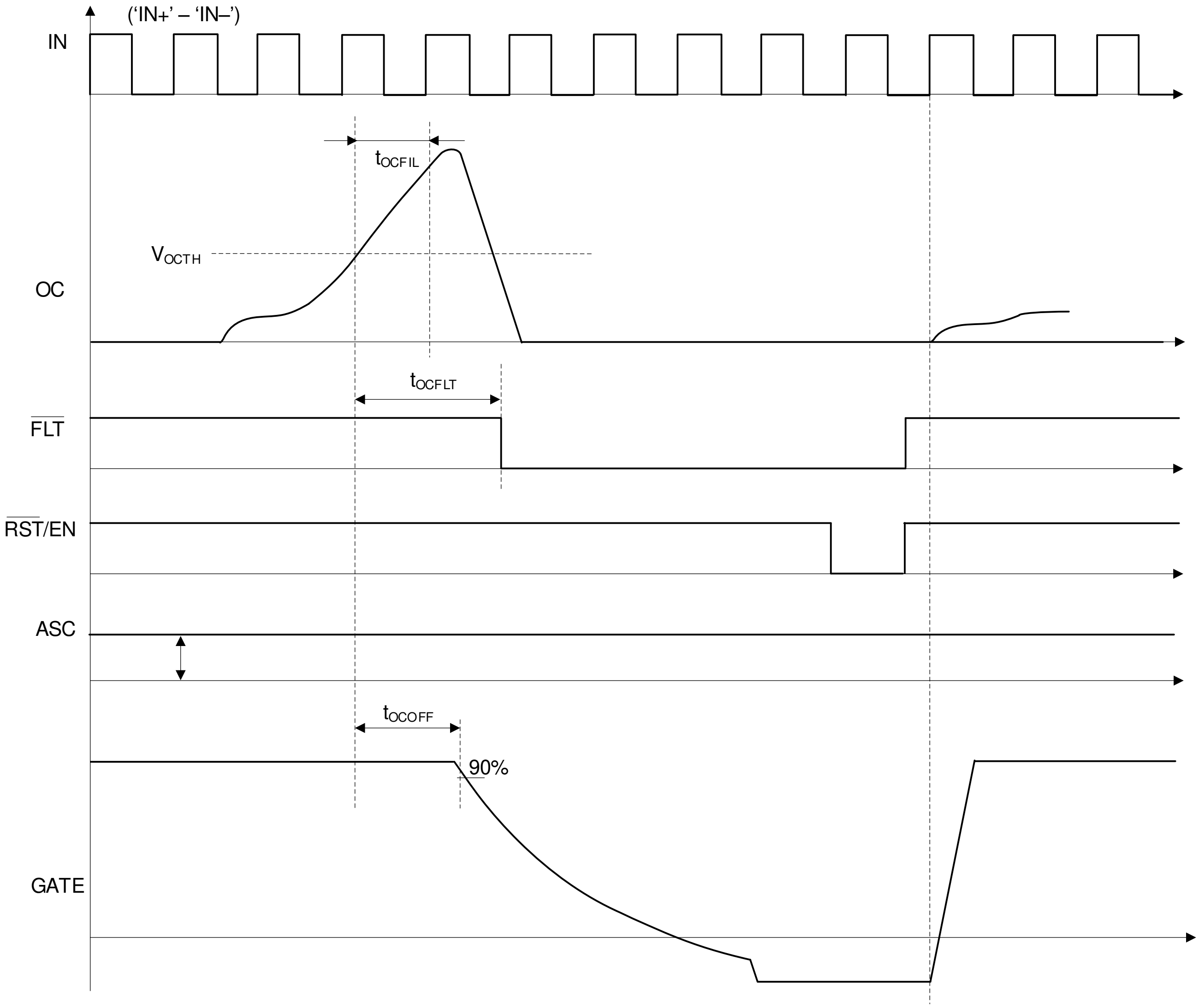

図 7-13. ASC Support with OC Fault

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8 Detailed Description

8.1 Overview

The UCC21738-Q1 device is an advanced isolated gate driver with state-of-art protection and sensing features for SiC MOSFETs and IGBTs. The device can support up to 2121-V DC operating voltage based on SiC MOSFETs and IGBTs, and can be used to above 10-kW applications such as HEV/EV traction inverter, motor drive, on-board and off-board battery charger, solar inverter, and so forth. The galvanic isolation is implemented by the capacitive isolation technology, which can realize a reliable reinforced isolation between the low voltage DSP/MCU and high voltage side.

The ±10-A peak sink and source current of the UCC21738-Q1 can drive the SiC MOSFET modules and IGBT modules directly without an extra buffer. The driver can also be used to drive higher power modules or parallel modules with external buffer stage. The input side is isolated with the output side with a reinforced isolation barrier based on capacitive isolation technology. The device can support up to 1.5-kV_{RMS} working voltage, 12.8-kV_{PK} surge immunity with longer than 40 years isolation barrier life. The strong drive strength helps to switch the device fast and reduce the switching loss, while the 150V/ns minimum CMTI ensures the reliability of the system with fast switching speed. The small propagation delay and part-to-part skew can minimize the deadtime setting, so the conduction loss can be reduced.

The device includes extensive protection and monitor features to increase the reliability and robustness of the SiC MOSFET and IGBT based systems. The 12-V output side power supply UVLO is suitable for switches with gate voltage ≥ 15 V. The active Miller clamp feature prevents the false turn on caused by Miller capacitance during fast switching. An external Miller clamp FET can be used, providing more versatility to the system design. The device has a state-of-art overcurrent and short circuit detection time, and fault reporting function to the low voltage side DSP/MCU. The soft turn off is triggered when the overcurrent or short circuit fault is detected, minimizing the short circuit energy while reducing the overshoot voltage on the switches.

The active short circuit feature can create a phase-to-phase short circuit for a three-phase inverter, which is useful for motor drive applications to protect the battery if the microcontroller loses control.

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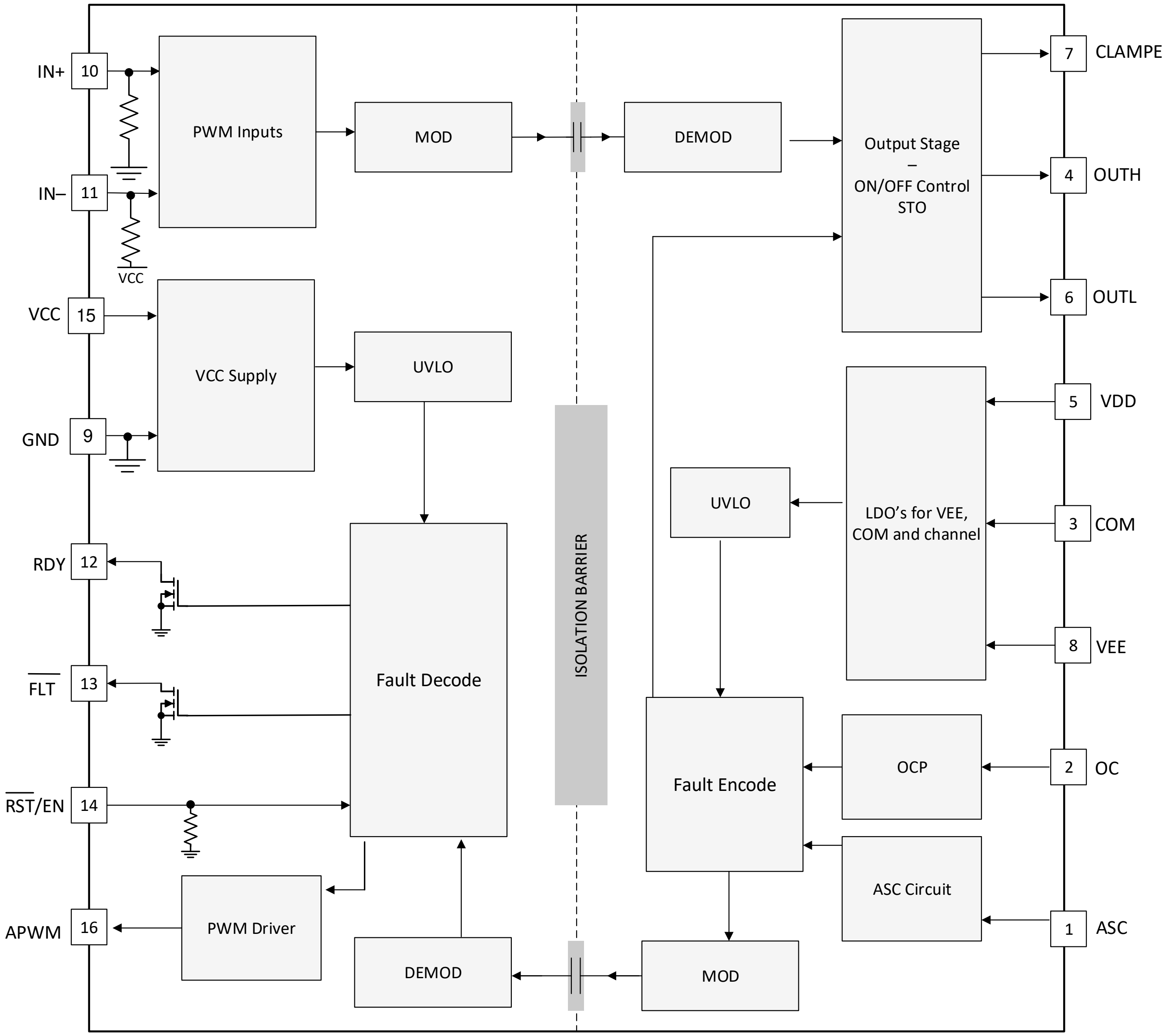
8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power Supply

The input side power supply VCC can support a wide voltage range from 3 V to 5.5 V. The device supports a bipolar power supply on the output side with a wide range from 13 V to 33 V from VDD to VEE. The negative power supply with respect to switch source or emitter is usually adopted to avoid false turn on when the other switch in the phase leg is turned on. The negative voltage is especially important for SiC MOSFET due to its fast switching speed.

8.3.2 Driver Stage

UCC21738-Q1 has ±10-A peak drive strength and is suitable for high power applications. The high drive strength can drive a SiC MOSFET module, IGBT module or paralleled discrete devices directly without an extra buffer stage. The UCC21738-Q1 can also be used to drive higher power modules or parallel modules with an extra buffer stage. Regardless of the values of VDD, the peak sink and source current can be kept at 10 A. The driver features an important safety function wherein, when the input pins are floating, the OUTH/OUTL is held low. The split output of the driver stage is depicted in 図 8-1. The driver has rail-to-rail output by implementing a hybrid pullup structure with a P-Channel MOSFET in parallel with an N-Channel MOSFET, and an N-Channel MOSFET to pulldown. The pullup NMOS is the same as the pulldown NMOS, so the on resistance R_{NMOS} is the same as R_{OL}. The hybrid pullup structure delivers the highest peak-source current when it is most needed, during the Miller plateau region of the power semiconductor turn-on transient. The R_{OH} in 図 8-1 represents the on-resistance of the pullup P-Channel MOSFET. However, the effective pullup resistance is much smaller than R_{OH}. Since the pullup N-Channel MOSFET has much smaller on-resistance than the P-Channel MOSFET, the pullup N-Channel MOSFET dominates most of the turn-on transient, until the voltage on OUTH pin is about 3V below VDD voltage. The effective resistance of the hybrid pullup structure during this period is about 2 x R_{OL} . Then the P-Channel MOSFET pulls up the OUTH voltage to VDD rail. The low pullup impedance results in strong drive strength during the turn-on transient, which shortens the charging time of the input capacitance of the power semiconductor and reduces the turn-on switching loss.

The pulldown structure of the driver stage is implemented solely by a pulldown N-Channel MOSFET. This MOSFET can ensure the OUTL voltage be pulled down to VEE rail. The low pulldown impedance not only results in high sink current to reduce the turn-off time, but also helps to increase the noise immunity considering the Miller effect.

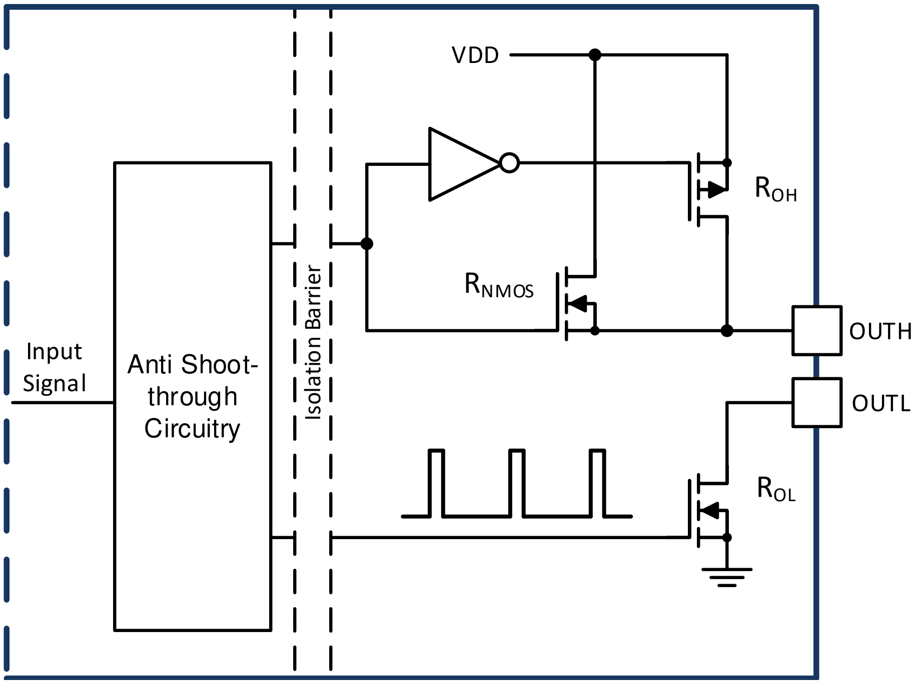


図 8-1. Gate Driver Output Stage

8.3.3 VCC and VDD Undervoltage Lockout (UVLO)

The UCC21738-Q1 implements the internal UVLO protection feature for both input and output power supplies VCC and VDD. When the supply voltage is lower than the threshold voltage, the driver output is held as LOW. The output only goes HIGH when both VCC and VDD are out of the UVLO status. The UVLO protection feature not only reduces the power consumption of the driver itself during low power supply voltage condition, but also increases the efficiency of the power stage. For SiC MOSFET and IGBT, the on-resistance reduces while the gate-source voltage or gate-emitter voltage increases. If the power semiconductor is turned on with a low VDD value, the conduction loss increases significantly and can lead to a thermal issue and efficiency reduction of the power stage. The UCC21738-Q1 implements a 12-V threshold voltage of VDD UVLO, with 800-mV hysteresis. This threshold voltage is suitable for both SiC MOSFET and IGBT.

The UVLO protection block features with hysteresis and deglitch filter, which help to improve the noise immunity of the power supply. During the turn-on and turn-off switching transient, the driver sources and sinks a peak transient current from the power supply, which can result in a sudden voltage drop of the power supply. With hysteresis and UVLO deglitch filter, the internal UVLO protection block ignores small noises during the normal switching transients.

The timing diagrams of the UVLO feature of VCC and VDD are shown in 図 7-8 and 図 7-9. The RDY pin on the input side is used to indicate the power-good condition. The RDY pin is open drain. During UVLO condition, the RDY pin is held in low status and connected to GND. Normally the pin is pulled up externally to VCC to indicate the power good.

8.3.4 Active Pulldown

The UCC21738-Q1 implements an active pulldown feature to ensure the OUTH/OUTL pin clamping to VEE when the VDD is open. The OUTH/OUTL pin is in high-impedance status when VDD is open, the active pulldown feature can prevent the output being falsely turned on before the device is back to control.

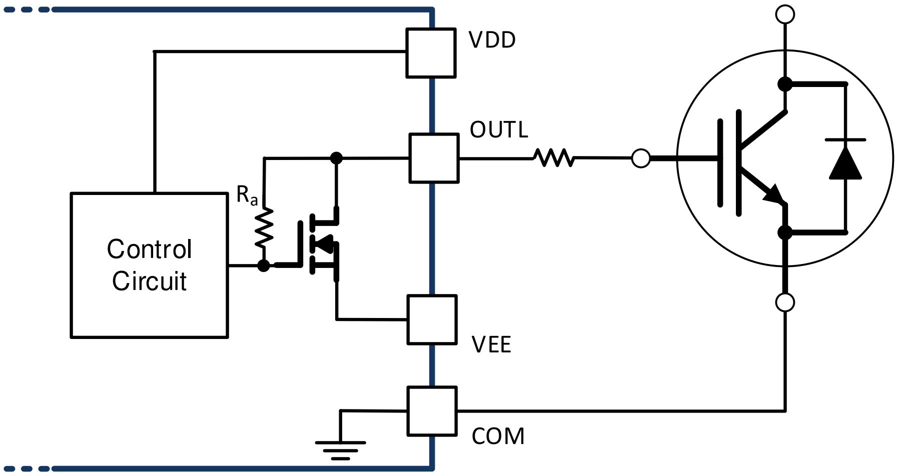


図 8-2. Active Pulldown

8.3.5 Short Circuit Clamping

During a short circuit condition, the Miller capacitance can cause a current sinking to the OUTH/OUTL pin due to the high dV/dt and boost the OUTH/OUTL voltage. The short circuit clamping feature of the UCC21738-Q1 can clamp the OUTH/OUTL pin voltage to be slightly higher than VDD, which can protect the power semiconductors from a gate-source and gate-emitter overvoltage breakdown. This feature is realized by an internal diode from the OUTH/OUTL to VDD.

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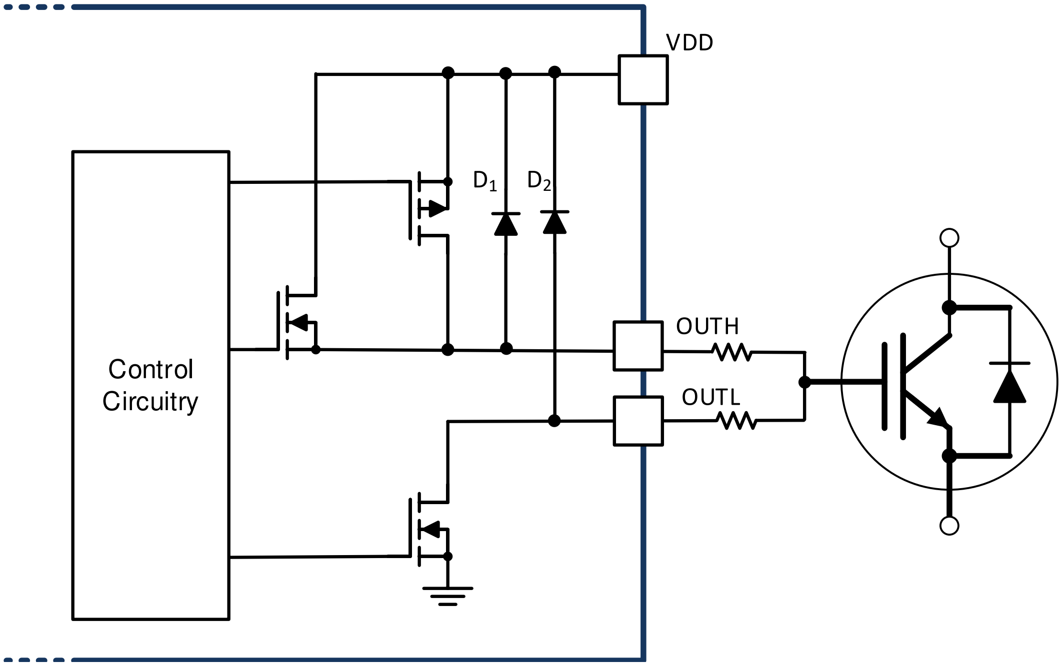

図 8-3. Short Circuit Clamping

8.3.6 External Active Miller Clamp

The active Miller clamp feature is important to prevent the false turn-on while the driver is in the OFF state. In applications in which the device can be in synchronous rectifier mode, the body diode conducts the current during the dead time while the device is in the OFF state, the drain-source or collector-emitter voltage remains the same and the dV/dt happens when the other power semiconductor of the phase leg turns on. The low internal pulldown impedance of the UCC21738-Q1 can provide a strong pull down to hold OUTL to VEE. However, external gate resistance is usually adopted to limit the dV/dt. The Miller effect during the turn-on transient of the other power semiconductor can cause a voltage drop on the external gate resistor, which boosts the gate-source or gate-emitter voltage. If the voltage on V_{GS} or V_{GE} is higher than the threshold voltage of the power semiconductor, a shoot-through can happen and cause catastrophic damage. The active Miller clamp feature of the UCC21738-Q1 drives an external MOSFET, which connects to the device gate. The external MOSFET is triggered when the gate voltage is lower than V_{CLMPTH}, which is 2 V above VEE, and creates a low impedance path to avoid the false turn-on issue.

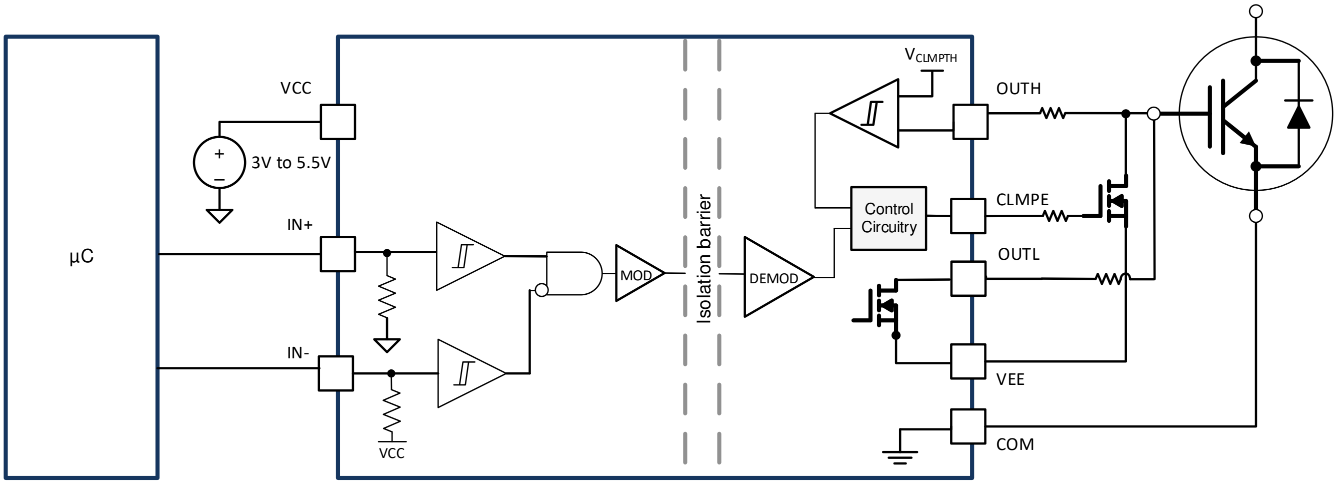

図 8-4. Active Miller Clamp

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8.3.7 Overcurrent and Short Circuit Protection

The UCC21738-Q1 implements a fast overcurrent and short circuit protection feature to protect the SiC MOSFET or IGBT from catastrophic breakdown during fault. The OC pin of the device has a typical 0.7-V threshold with respect to COM, source or emitter of the power semiconductor. When the input is in floating condition, or the output is held in low state, the OC pin is pulled down by an internal MOSFET and held in LOW state, which prevents the overcurrent and short circuit fault from false triggering. The OC pin is in high-impedance state when the output is in high state, which means the overcurrent and short circuit protection feature only works when the power semiconductor is in ON state. The internal pulldown MOSFET helps to discharge the voltage of OC pin when the power semiconductor is turned off.

The overcurrent and short circuit protection feature can be used to SiC MOSFET module or IGBT module with SenseFET, traditional desaturation circuit, and shunt resistor in series with the power loop for lower power applications. For the SiC MOSFET module or IGBT module with SenseFET, the SenseFET integrated in the module can scale down the drain current or collector current. With an external high precision sense resistor, the drain current or collector current can be accurately measured. If voltage of the sensed resistor higher than the overcurrent threshold V_{OCTH} is detected, a soft turn-off is initiated. A fault is reported to the input side $\overline{\text{FLT}}$ pin to the DSP/MCU. The output is held to LOW after the fault is detected, and can only be reset by the $\overline{\text{RST}}$/EN pin. The state-of-art overcurrent and short circuit detection time helps to ensure a short shutdown time for the SiC MOSFET and IGBT.

The overcurrent and short circuit protection feature can also be paired with desaturation circuit and shunt resistors. The DESAT threshold can be programmable in this case, which increases the versatility of the device. Detailed application diagrams of the desaturation circuit and shunt resistor are given in 図 8-5.

- High current and high dI/dt during the overcurrent and short circuit fault can cause a voltage bounce on the shunt resistor’s parasitic inductance and board layout parasitic, which results in a false trigger of the OC pin. A high precision, low ESL, and small value resistor must be used in this approach.
- A shunt resistor approach is not recommended for high power applications and short circuit protection of low power applications.

Detailed applications of the overcurrent and short circuit feature are discussed in セクション 9.

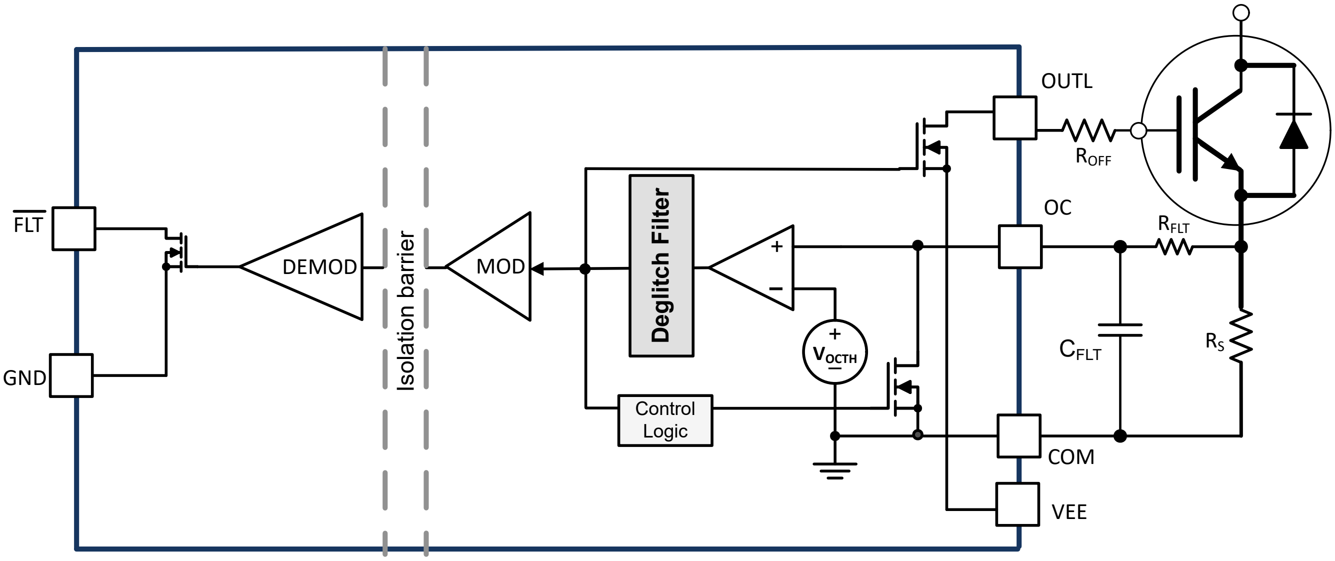

図 8-5. Overcurrent and Short Circuit Protection

8.3.8 Soft Turn-off

The UCC21738-Q1 initiates a soft turn-off when the overcurrent and short circuit protection are triggered, or when the $\overline{\text{RST}}$/EN is pulled low for longer than t_{RSTPD}. When the overcurrent and short circuit faults occur, the

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power semiconductor transitions from the linear region to the saturation region very quickly. The gate voltage controls the channel current. By pulling down the gate voltage with a soft turn-off current, the dI/dt of the channel current is controlled by the gate voltage and decreases softly; thus, overshooting the power semiconductor is limited, preventing overvoltage breakdown. 図 7-10 shows the the soft turn-off timing diagram.

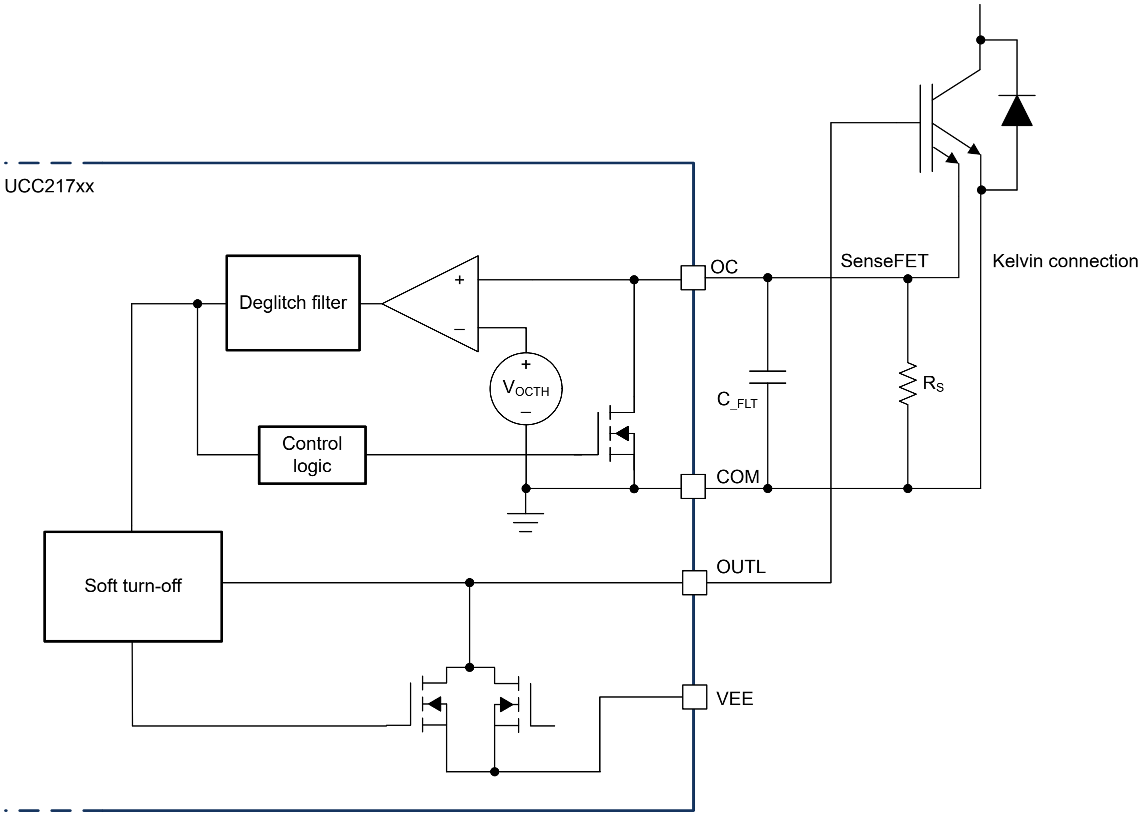

図 8-6. Soft Turn-off

8.3.9 Fault ($\overline{\text{FLT}}$), Reset, and Enable ($\overline{\text{RST}}$/EN)

The $\overline{\text{FLT}}$ pin is open drain and can report a fault signal to the DSP/MCU when overcurrent and short circuit faults are detected through the OC pin. The $\overline{\text{FLT}}$ pin is pulled down to GND, and is held in a low state unless a reset signal is received from $\overline{\text{RST}}$/EN. The device has a fault mute time, $t_{FLTMUTE}$, within which the device ignores any reset signal.

$\overline{\text{RST}}$/EN is pulled down internally. The device is disabled by default if the $\overline{\text{RST}}$/EN pin is floating. The pin has two purposes:

- Resets the overcurrent and short circuit fault signaled on the $\overline{\text{FLT}}$ pin. The $\overline{\text{RST}}$/EN pin is active low. If the pin is set and held in a low state for more than t_{RSTFIL}, the fault signal is reset and $\overline{\text{FLT}}$ is reset back to the high impedance status at the rising edge of the $\overline{\text{RST}}$/EN pin.
- Enables and shuts down the device. If the $\overline{\text{RST}}$/EN pin is pulled low, the driver is disabled and shut down by the regular turn off. The pin must be pulled up externally to enable the part; otherwise, the device is disabled by default.

8.3.10 ASC Support and APWM Monitor

When VCC loses power, or the MCU is malfunctioning, the motor can lose control and reversely charge the battery. Overvoltage of the battery can cause battery break down, or even a fire hazard. In this case, the active short circuit (ASC) function is used to protect the system by forcing the output signal high, turning on the switch,

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and creating an active short circuit loop between the phases to bypass the battery. The timing diagram of ASC support with VCC UVLO, VDD UVLO, and OC fault are shown in 図 7-11, 図 7-12, and 図 7-13.

The UCC21738-Q1 encodes the voltage signal V_{ASC} to a PWM signal, passing through the reinforced isolation barrier, and output to the APWM pin on the input side. Thus, the ASC pin status can be monitored. The PWM signal can either be transferred directly to the DSP/MCU to calculate the duty cycle, or filtered by a simple RC filter as an analog signal. The ASC input voltage varies from 0 V to 5 V, and the corresponding duty cycle of the APWM output ranges from 5% to 95% with a 400-kHz frequency.

8.4 Device Functional Modes

The table below lists the device function.

表 8-1. Function Table

INPUT						OUTPUT			
VCC	VDD	IN+	IN-	$\overline{\text{RST}}$/EN	ASC	RDY	$\overline{\text{FLT}}$	OUTH/OUTL	CLMPE
PD	PU	X	X	X	High	Low	HiZ	High	Low
PU	PU	X	X	X	High	HiZ	HiZ	High	Low
PD	PU	X	X	X	Low	Low	HiZ	Low	High
PU	PU	X	X	Low	Low	HiZ	HiZ	Low	High
PU	PD	X	X	X	X	Low	HiZ	Low	Unknown*
PU	Open	X	X	X	X	Low	HiZ	HiZ	HiZ
PU	PU	Low	X	High	Low	HiZ	HiZ	Low	High
PU	PU	X	High	High	Low	HiZ	HiZ	Low	High
PU	PU	High	Low	High	Low	HiZ	HiZ	High	Low

PU: Power Up (VCC ≥ 3 V, VDD ≥ 12.8 V); PD: Power Down (VCC ≤ 2.2 V, VDD ≤ 10.4 V); X: Irrelevant; HiZ: High Impedance

Unknown*: CLMPE state depends on the powered-down VDD voltage

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9 Applications and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The device is very versatile because of the strong drive strength, wide range of the output power supply, high isolation ratings, high CMTI, and superior protection and sensing features. The 1.5-kVRMS working voltage and 12.8-kVPK surge immunity can support both SiC MOSFET and IGBT modules with DC bus voltage up to 2121 V. The device can be used in both low power and high power applications such as traction inverter in HEV/EV, on-board charger and charging pile, motor driver, solar inverter, industrial power supplies, and so forth. The device can drive the high power SiC MOSFET module, IGBT module, or paralleled discrete device directly without external buffer drive circuit based on NPN/PNP bipolar transistor in totem-pole structure, which allows the driver to have more control to the power semiconductor and saves cost and space of the board design. The UCC21738-Q1 can also be used to drive very high power modules or paralleled modules with external buffer stage. The input side can support power supply and microcontroller signals from 3.3 V to 5 V, and the device level shifts the signal to the output side through the reinforced isolation barrier. The device has a wide output power supply range from 13 V to 33 V and supports a wide range of negative power supply. This allows the driver to be used in SiC MOSFET applications, IGBT applications, and many others. The 12-V UVLO benefits the power semiconductor with lower conduction loss and improves system efficiency. As a reinforced isolated single channel driver, the device can be used to drive either a low-side or high-side driver.

The device features extensive protection and monitoring features, which can monitor, report, and protect the system from various fault conditions.

- Fast detection and protection for an overcurrent and short circuit fault. The feature is preferable in a split source SiC MOSFET module or a split emitter IGBT module. For modules with no integrated current mirror or paralleled discrete semiconductors, the traditional desaturation circuit can be modified to implement short circuit protection. The semiconductor is shut down when a fault is detected and the $\overline{\text{FLT}}$ pin is pulled down to indicate the fault detection. The device is latched unless a reset signal is received from the $\overline{\text{RST}}$/EN pin.
- Soft turn-off feature to protect the power semiconductor from catastrophic breakdown during an overcurrent and short circuit fault. The shutdown energy can be controlled while the overshoot of the power semiconductor is limited.
- UVLO detection to protect the semiconductor from excessive conduction loss. Once the device is detected to be in UVLO mode, the output is pulled down and the RDY pin indicates the power supply is lost. The device is back to normal operation mode once the power supply is out of the UVLO status. The power-good status can be monitored from the RDY pin.
- Active short circuit feature creates phase-to-phase short circuit in the three-phase inverter to protect the battery from overvoltage breakdown.
- Active Miller clamp feature protects the power semiconductor from false turn on by driving an external MOSFET. This feature allows flexibility of board layout design and the pulldown strength of the Miller clamp FET.
- Enable and disable function through the $\overline{\text{RST}}$/EN pin.
- Short circuit clamping
- Active pulldown

9.2 Typical Application

図 9-1 shows the typical application of a half bridge using two UCC21738-Q1 isolated gate drivers. The half bridge is a basic element in various power electronics applications, such as a traction inverter in a HEV/EV to convert DC current of the electric battery of the vehicle to AC current to drive the electric motor in the propulsion

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system. The topology can also be used in motor drive applications to control the operating speed and torque of the AC motors.

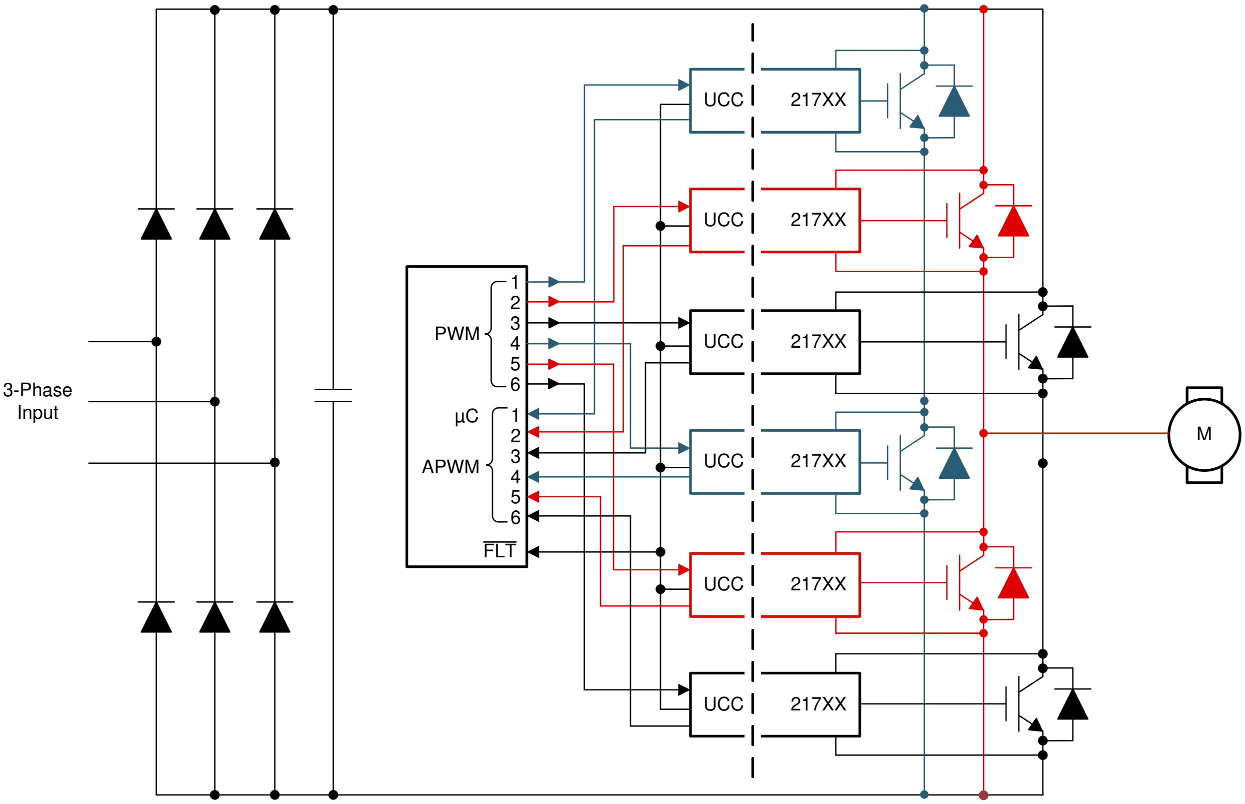

図 9-1. Typical Application Schematic

9.2.1 Design Requirements

Design of the power system for end equipment should consider some design requirements to ensure reliable operation of the UCC21738-Q1 throughout the load range. The design considerations include peak source and sink current, power dissipation, overcurrent, and short circuit protection and so forth.

A design example for a half bridge based on IGBT is given in this subsection. The design parameters are shown in 表 9-1.

表 9-1. Design Parameters

PARAMETER	VALUE
Input Supply Voltage	5 V
IN-OUT Configuration	Noninverting
Positive Output Voltage VDD	15 V
Negative Output Voltage VEE	–5 V
DC Bus Voltage	800 V
Peak Drain Current	300 A
Switching Frequency	50 kHz
Switch Type	IGBT Module

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9.2.2 Detailed Design Procedure

9.2.2.1 Input Filters for IN+, IN-, and $\overline{\text{RST}}$/EN

In the applications of a traction inverter or motor drive, the power semiconductors are in hard switching mode. With the strong device drive strength, the dV/dt can be high, especially for a SiC MOSFET. Noise cannot only be coupled to the gate voltage due to the parasitic inductance, but also to the input side as the nonideal PCB layout and coupled capacitance.

The UCC21738-Q1 features a 40-ns internal deglitch filter to the IN+, IN-, and $\overline{\text{RST}}$/EN pins. Any signal less than 40 ns can be filtered out from the input pins. For noisy systems, an external low-pass filter can be added externally to the input pins. Adding low-pass filters to the IN+, IN-, and $\overline{\text{RST}}$/EN pins can effectively increase noise immunity and increase signal integrity. When not in use, the IN+, IN-, and $\overline{\text{RST}}$/EN pins should not be floating. IN- should be tied to GND if only IN+ is used for a noninverting input to output configuration. The purpose of the low-pass filter is to filter out high frequency noise generated by the layout parasitics. While choosing the low-pass filter resistors and capacitors, both the noise immunity effect and delay time should be considered according to the system requirements.

9.2.2.2 PWM Interlock of IN+ and IN-

The UCC21738-Q1 features a PWM interlock for the IN+ and IN- pins, which can be used to prevent a phase leg shoot-through issue. As shown in 表 8-1, the output is logic low while both IN+ and IN- are logic high. When only IN+ is used, IN- can be tied to GND. To utilize the PWM interlock function, the PWM signal of the other switch in the phase leg can be sent to the IN- pin. As shown in 図 9-2, PWM_T is the PWM signal to the top-side switch, and PWM_B is the PWM signal to the bottom-side switch. For the top-side gate driver, the PWM_T signal is given to the IN+ pin, while the PWM_B signal is given to the IN- pin; for the bottom-side gate driver, the PWM_B signal is given to the IN+ pin, while PWM_T signal is given to the IN- pin. When both PWM_T and PWM_B signals are high, the outputs of both gate drivers are logic low to prevent the shoot-through condition.

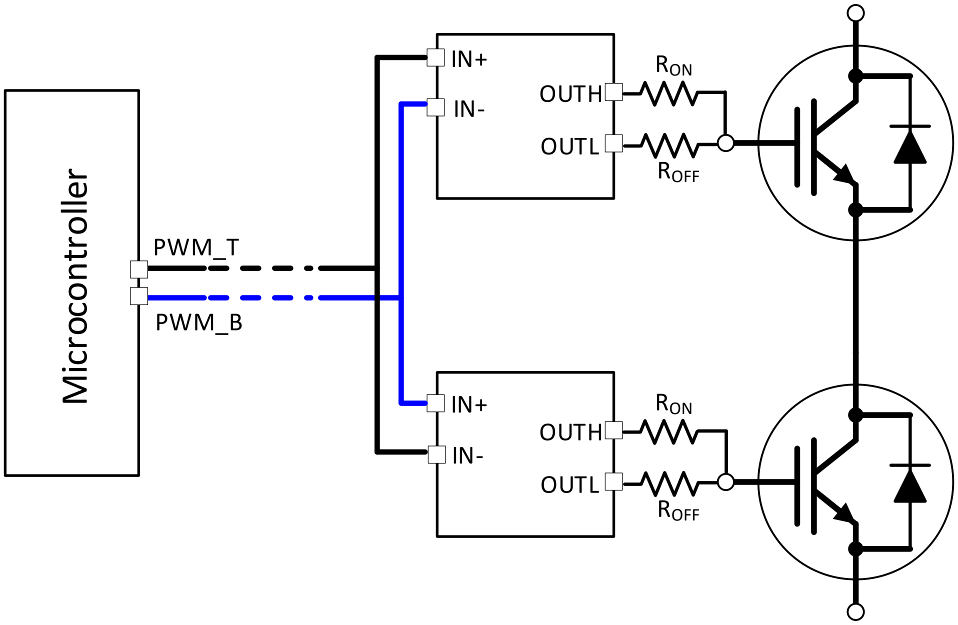

図 9-2. PWM Interlock for a Half Bridge

9.2.2.3 $\overline{\text{FLT}}$, RDY, and $\overline{\text{RST}}$/EN Pin Circuitry

The $\overline{\text{FLT}}$ and RDY pins are open-drain outputs. The $\overline{\text{RST}}$/EN pin has a 50-kΩ internal pulldown resistor, so the driver is in the OFF status if the $\overline{\text{RST}}$/EN pin is not pulled up externally. A 5-kΩ resistor can be used as pullup resistor for the $\overline{\text{FLT}}$, RDY, and $\overline{\text{RST}}$/EN pins.

To improve noise immunity due to parasitic coupling and common-mode noise, low-pass filters can be added between the $\overline{\text{FLT}}$, RDY, and $\overline{\text{RST}}$/EN pins and the microcontroller. A filter capacitor between 100 pF to 300 pF can be added.

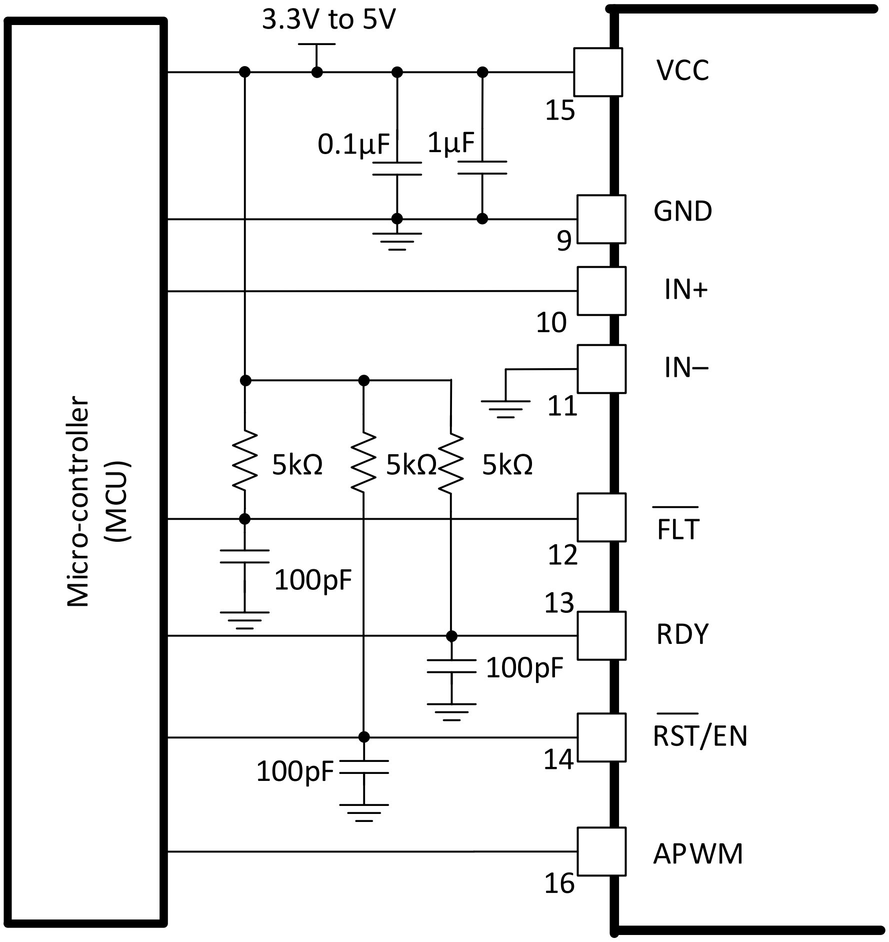

図 9-3. $\overline{\text{FLT}}$, RDY and $\overline{\text{RST}}$/EN Pins Circuitry

9.2.2.4 $\overline{\text{RST}}$/EN Pin Control

The $\overline{\text{RST}}$/EN pin has two functions. It can be used to enable and shut down the outputs of the driver and reset the fault signaled on the $\overline{\text{FLT}}$ pin. The $\overline{\text{RST}}$/EN pin needs to be pulled up to enable the device; when the pin is pulled down, the device is in disabled status. With a 50-kΩ pulldown resistor existing, the driver is disabled by default.

When the driver is latched after an overcurrent or short circuit fault is detected, the $\overline{\text{FLT}}$ pin and output are latched low and need to be reset by the $\overline{\text{RST}}$/EN pin. The $\overline{\text{RST}}$/EN pin is active low. The microcontroller needs to send a signal to the $\overline{\text{RST}}$/EN pin after the fault mute time $t_{FLTMUTE}$ to reset the driver. This pin can also be used to automatically reset the driver. The continuous input signals IN+ or IN- can be applied to the $\overline{\text{RST}}$/EN pin, so the microcontroller does not need to generate another control signal to reset the driver. If the noninverting input IN+ is used, then IN+ can be tied to the $\overline{\text{RST}}$/EN pin. If inverting input IN- is used, then a NOT logic is needed between the inverting PWM signal from the microcontroller and the $\overline{\text{RST}}$/EN pin. In this case, the driver can be reset in every switching cycle without an extra control signal from the microcontroller to the $\overline{\text{RST}}$/EN pin.

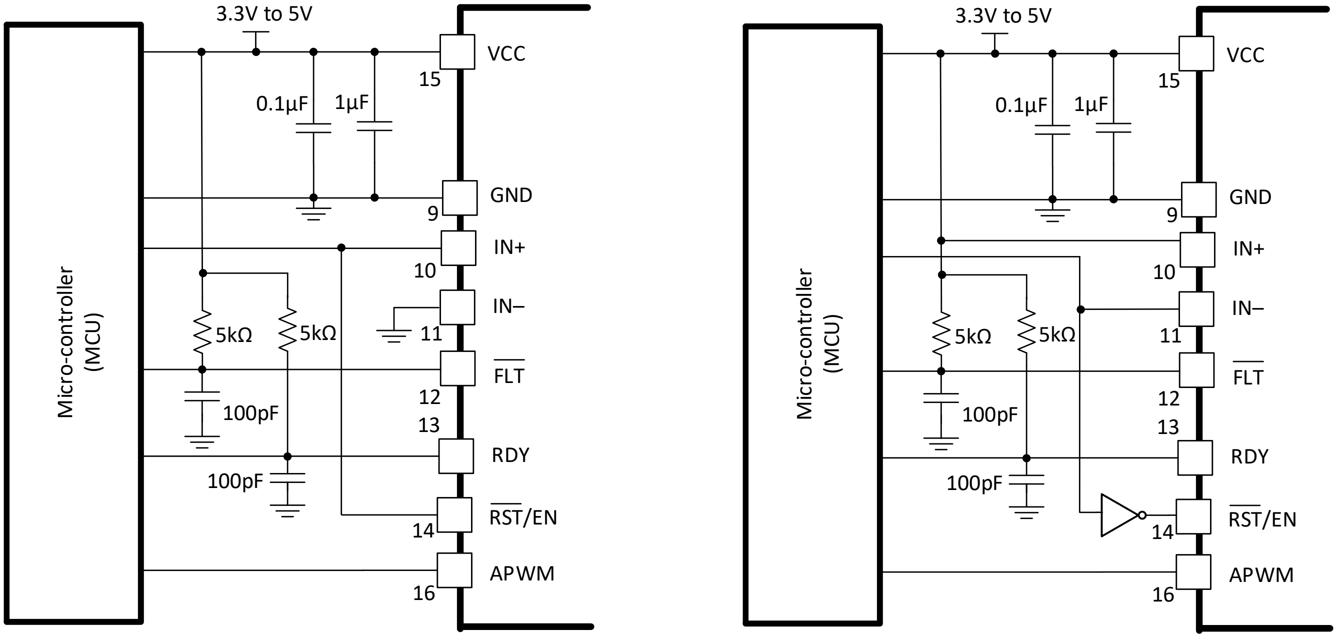

図 9-4. Automatic Reset Control

9.2.2.5 Turn-On and Turn-Off Gate Resistors

The UCC21738-Q1 features split outputs OUTH and OUTL, which enables independent control of the turn-on and turn-off switching speed. The turn-on and turn-off resistances determine the peak source and sink currents, which controls the switching speed in turn. Meanwhile, the power dissipation in the gate driver should be considered to ensure the device is in the thermal limit. Initially, the peak source and sink currents are calculated as:

$$I_{source\_pk} = \min\left(10A, \frac{VDD - VEE}{R_{OH\_EFF} + R_{ON} + R_{G\_Int}}\right)$$
$$I_{sink\_pk} = \min\left(10A, \frac{VDD - VEE}{R_{OL} + R_{OFF} + R_{G\_Int}}\right) \quad (1)$$

Where

- R_{OH_EFF} is the effective internal pullup resistance of the hybrid pullup structure, which is approximately 2 × R_{OL}, about 0.7 Ω.
- R_{OL} is the internal pulldown resistance, about 0.3 Ω.
- R_{ON} is the external turn-on gate resistance.
- R_{OFF} is the external turn-off gate resistance.
- R_{G_Int} is the internal resistance of the SiC MOSFET or IGBT module.

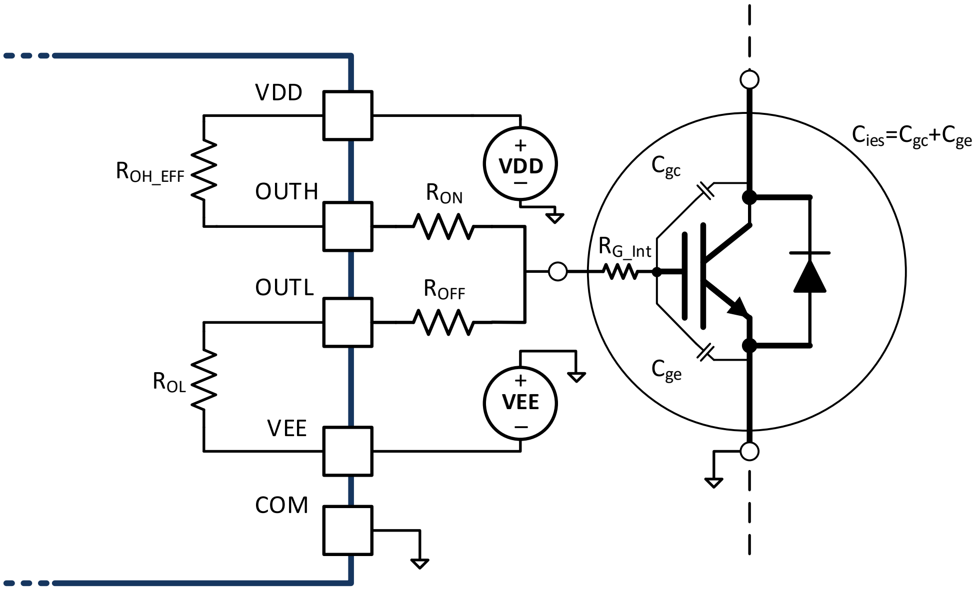

図 9-5. Output Model for Calculating Peak Gate Current

For example, for an IGBT module-based system with the following parameters:

- Q_g = 3300 nC
- R_{G_Int} = 1.7 Ω
- R_{ON} = R_{OFF}= 1 Ω

The peak source and sink currents in this case are:

$$I_{source\_pk} = \min(10A, \frac{VDD - VEE}{R_{OH\_EFF} + R_{ON} + R_{G\_Int}}) \approx 5.9A$$
$$I_{sink\_pk} = \min(10A, \frac{VDD - VEE}{R_{OL} + R_{OFF} + R_{G\_Int}}) \approx 6.7A \tag{2}$$

Thus by using 1-Ω external gate resistance, the peak source current is 5.9 A, and the peak sink current is 6.7 A. The collector-to-emitter dV/dt during the turn-on switching transient is dominated by the gate current at the Miller plateau voltage. The hybrid pullup structure ensures peak source current at the Miller plateau voltage, unless the turn-on gate resistor is too high. The faster the collector-to-emitter, V_{ce}, voltage rises to V_{DC}, the smaller the turn-on switching loss. The dV/dt can be estimated as Q_{gc}/I_{source_pk}. For the turn-off switching transient, the drain-to-source dV/dt is dominated by the load current, unless the turn-off gate resistor is too high. After V_{ce} reaches the dc bus voltage, the power semiconductor is in saturation mode and the channel current is controlled by V_{ge}. The peak sink current determines the dI/dt, which dominates the V_{ce} voltage overshoot accordingly. If using relatively large turn-off gate resistance, V_{ce} overshoot can be limited. The overshoot can be estimated by:

$$\Delta V_{ce} = L_{stray} \cdot I_{load} / ((R_{OFF} + R_{OL} + R_{G\_Int}) \cdot C_{ies} \cdot \ln(V_{plat} / V_{th})) \tag{3}$$

Where

- L_{stray} is the stray inductance in the power switching loop, as shown in 図 9-6.
- I_{load} is the load current, which is the turn-off current of the power semiconductor.
- C_{ies} is the input capacitance of the power semiconductor.
- V_{plat} is the plateau voltage of the power semiconductor.
- V_{th} is the threshold voltage of the power semiconductor.

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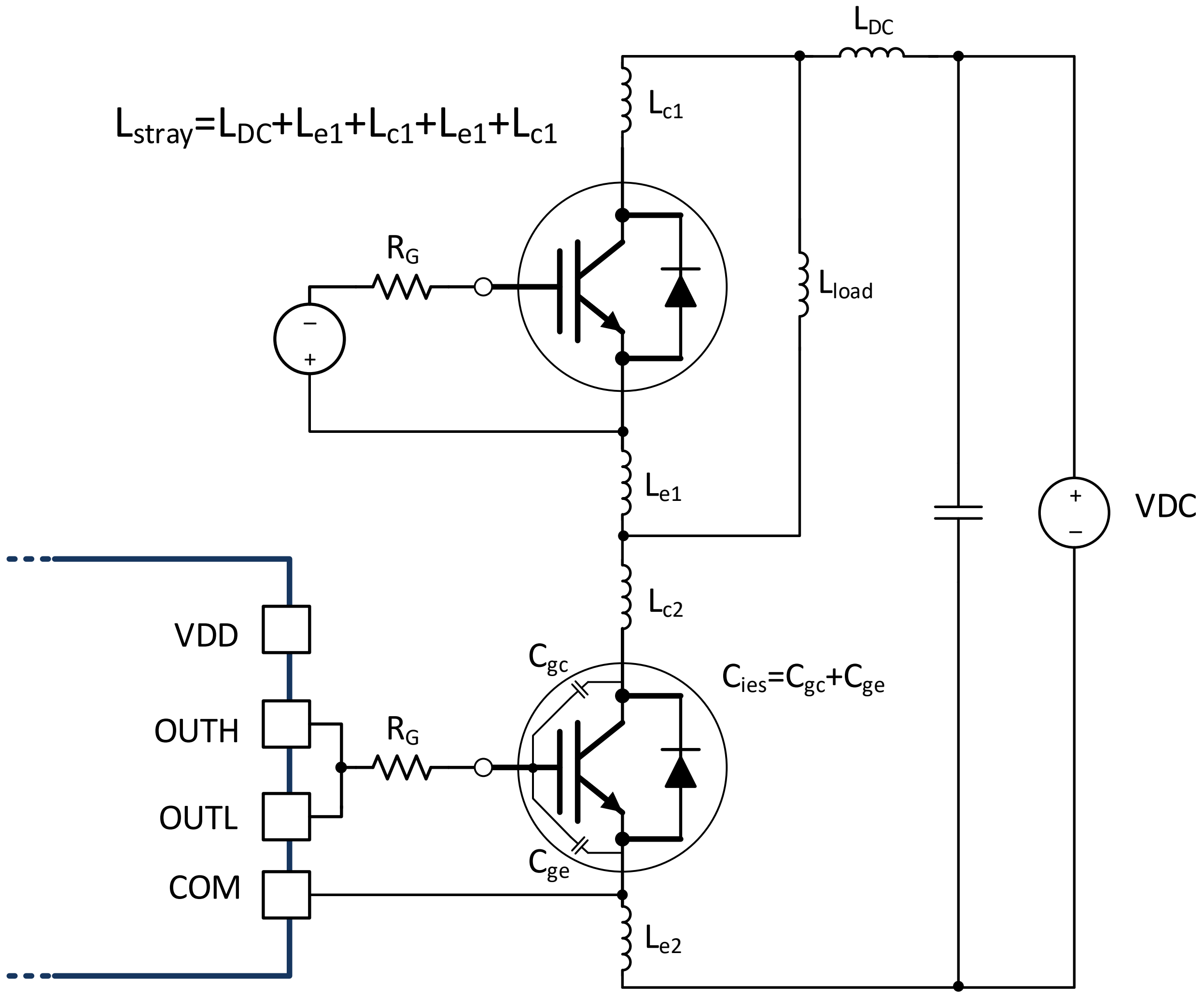

図 9-6. Stray Parasitic Inductance of IGBTs in a Half-Bridge Configuration

Power dissipation should be taken into account to maintain the gate driver within the thermal limit. The power loss of the gate driver includes the quiescent loss and the switching loss, which can be calculated as:

$$P_{DR} = P_Q + P_{SW} \tag{4}$$

P_Q is the quiescent power loss for the driver, which is I_q x (VDD-VEE) = 5 mA x 20 V = 0.100 W. The quiescent power loss is the power consumed by the internal circuits such as the input stage, reference voltage, logic circuits, protection circuits when the driver is switching when the driver is biased with VDD and VEE, and also the charging and discharging current of the internal circuit when the driver is switching. The power dissipation when the driver is switching can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left(\frac{R_{OH\_EFF}}{R_{OH\_EFF} + R_{ON} + R_{G\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G\_Int}}\right) \cdot (VDD - VEE) \cdot f_{sw} \cdot Q_g \tag{5}$$

Where

- Q_g is the gate charge required at the operation point to fully charge the gate voltage from VEE to VDD.
- f_{sw} is the switching frequency.

In this example, the P_{SW} can be calculated as:

$$P_{SW} = \frac{1}{2} \cdot \left(\frac{R_{OH\_EFF}}{R_{OH\_EFF} + R_{ON} + R_{G\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{G\_Int}}\right) \cdot (VDD - VEE) \cdot f_{sw} \cdot Q_g = 0.505W \quad (6)$$

Thus, the total power loss is:

$$P_{DR} = P_Q + P_{SW} = 0.10W + 0.505W = 0.605W \quad (7)$$

When the board temperature is 125°C, the junction temperature can be estimated as:

$$T_j = T_b + \psi_{jb} \cdot P_{DR} \approx 150°C \quad (8)$$

Therefore, for the application in this example, with 125°C board temperature, the maximum switching frequency is ~50 kHz to keep the gate driver in the thermal limit. By using a lower switching frequency, or increasing external gate resistance, the gate driver can be operated at a higher switching frequency.

9.2.2.6 External Active Miller Clamp

The external active Miller clamp feature allows the gate driver to stay at the low status when the gate voltage is detected below V_{CLMPTH}. When the other switch of the phase leg turns on, the dV/dt can cause a current through the parasitic Miller capacitance of the switch and sink in the gate driver. The sinking current causes a negative voltage drop on the turn-off gate resistance, and bumps up the gate voltage to cause a false turn on. The external active Miller clamp features allow flexibility of board layout and active Miller clamp pulldown strength. Limited by the board layout, if the driver cannot be placed close enough to the switch, an external active Miller clamp MOSFET can be placed close to the switch and the MOSFET can be chosen according to the peak current needed. Caution must be exercised when the driver is placed far from the power semiconductor. Since the device has high peak sink and source currents, the high dI/dt in the gate loop can cause a ground bounce on the board parasitics. The ground bounce can cause a positive voltage bump on the CLMPE pin during the turn-off transient, and results in the external active Miller clamp MOSFET to turn on shortly and add extra drive strength to the sink current. To reduce the ground bounce, a 2-Ω resistance is recommended to the gate of the external active clamp MOSFET.

When V_{OUTH} is detected to be lower than V_{CLMPTH} above VEE, the CLMPE pin outputs a 5-V voltage with respect to VEE, the external clamp FET is in linear region and the pulldown current is determined by the peak drain current, unless the on-resistance of the external clamp FET is large.

$$I_{CLMPE\_PK} = \min\left(I_{D\_PK}, \frac{V_{DS}}{R_{DS\_ON}}\right) \quad (9)$$

Where

- I_{D_PK} is the peak drain current of the external clamp FET
- V_{DS} is the drain-to-source voltage of the clamp FET when the CLMPE is activated
- R_{DS_ON} is the on-resistance of the external clamp FET

The total delay time of the active Miller clamp circuit from the gate voltage detection threshold V_{CLMPTH} can be calculated as t_{DCLMPE}+t_{CLMPER}. t_{CLMPER} depends on the parameter of the external active Miller clamp MOSFET. As long as the total delay time is longer than the dead time of high-side and low-side switches, the driver can effectively protect the switch from a false turn-on issue caused by the Miller effect.

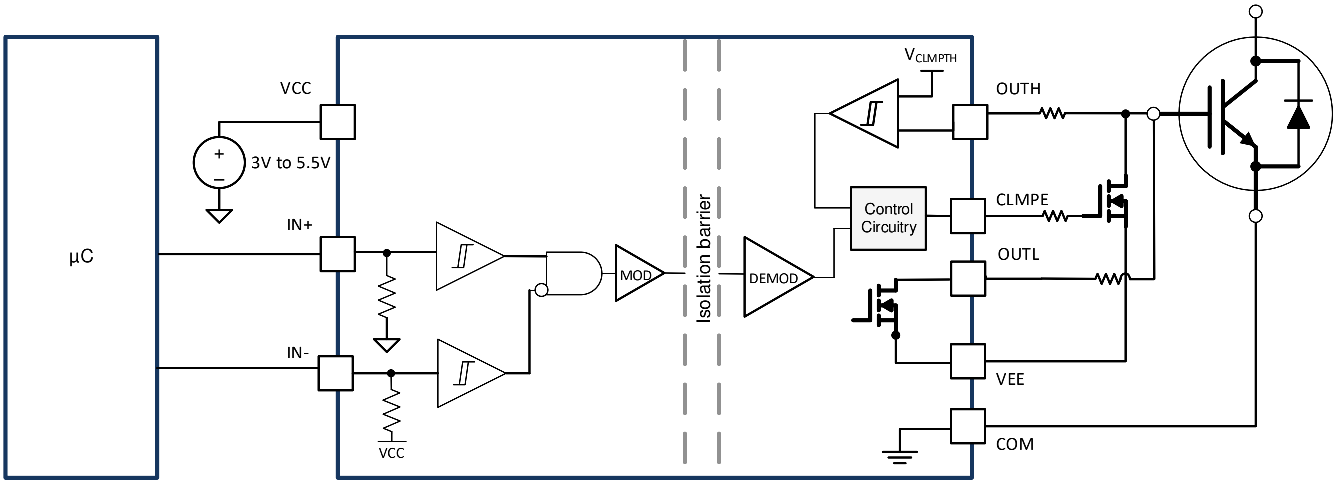

図 9-7. External Active Miller Clamp Configuration

9.2.2.7 Overcurrent and Short Circuit Protection

Fast and reliable overcurrent and short circuit protection is important to protect the catastrophic break down of the SiC MOSFET and IGBT modules, and improve the system reliability. The UCC21738-Q1 features a state-of-art overcurrent and short circuit protection, which can be applied to both SiC MOSFET and IGBT modules with various detection circuits.

9.2.2.7.1 Protection Based on Power Modules with Integrated SenseFET

The overcurrent and short circuit protection function is suitable for the SiC MOSFET and IGBT modules with integrated SenseFET. The SenseFET scales down the main power loop current and outputs the current with a dedicated pin of the power module. With the external high precision sensing resistor, the scaled down current can be measured and the main power loop current can be calculated. The value of the sensing resistor R_S sets the protection threshold of the main current. For example, with a ratio of 1:N = 1:50000 of the integrated current mirror, by using R_S as 20 Ω, the threshold protection current is:

$$I_{OC\_TH} = \frac{V_{OCTH}}{R_S} \cdot N = 1750A \tag{10}$$

The overcurrent and short circuit protection based on the integrated SenseFET has high precision, as it is sensing the current directly. The accuracy of the method is related to two factors: the scaling down ratio of the main power loop current and the SenseFET, and the precision of the sensing resistor. Since the current is sensed from the SenseFET, which is isolated from the main power loop, and the current is scaled down significantly with much less dI/dt, the sensing loop has good noise immunity. To further improve the noise immunity, a low-pass filter can be added. A 100-pF to 10-nF filter capacitor can be added. The delay time caused by the low-pass filter should also be considered for the protection circuitry design.

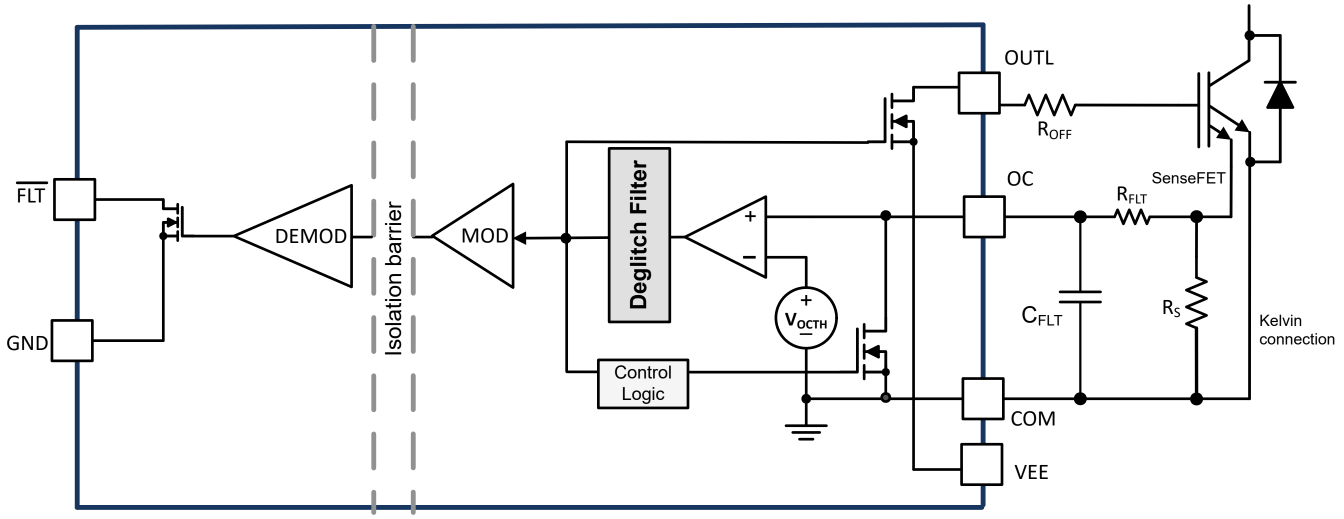

図 9-8. Overcurrent and Short Circuit Protection Based on IGBT Module with SenseFET

9.2.2.7.2 Protection Based on Desaturation Circuit

For SiC MOSFET and IGBT modules without SenseFET, the desaturation (DESAT) circuit is the most popular circuit which is adopted for overcurrent and short circuit protection. The circuit consists of a current source, a resistor, a blanking capacitor and a diode. Normally the current source is provided from the gate driver, when the device turns on, a current source charges the blanking capacitor and the diode forward biased. During normal operation, the capacitor voltage is clamped by the switch V_{CE} voltage. When a short circuit happens, the capacitor voltage is quickly charged to the threshold voltage which triggers device shutdown. For the UCC21738-Q1, the OC pin does not feature an internal current source. The current source should be generated externally from the output power supply. When UCC21738-Q1 is in the OFF state, the OC pin is pulled down by an internal MOSFET, which creates an offset voltage on the OC pin. By choosing R1 and R2 significantly higher than the pulldown resistance of the internal MOSFET, the offset can be ignored. When the UCC21738-Q1 is in the ON state, the OC pin is high impedance. The current source is generated by the output power supply VDD and the external resistor divider R1, R2, and R3. The overcurrent detection threshold voltage of the IGBT is:

$$V_{DET} = V_{OCTH} \cdot \frac{R_2 + R_3}{R_3} - V_F \tag{11}$$

The blanking time of the detection circuit is:

$$t_{BLK} = -\frac{R_1 + R_2}{R_1 + R_2 + R_3} \cdot R_3 \cdot C_{BLK} \cdot \ln(1 - \frac{R_1 + R_2 + R_3}{R_3} \cdot \frac{V_{OCTH}}{V_{DD}}) \tag{12}$$

Where:

- V_{OCTH} is the detection threshold voltage of the gate driver
- R_1, R_2, and R_3 are the resistances of the voltage divider
- C_{BLK} is the blanking capacitor
- V_F is the forward voltage of the high voltage diode D_{HV}

The modified desaturation circuit has all the benefits of the conventional desaturation circuit. The circuit has negligible power loss and is easy to implement. The detection threshold voltage of IGBT and blanking time can be programmed by external components. Different with the conventional desaturation circuit, the overcurrent detection threshold voltage of the IGBT can be modified to any voltage level, either higher or lower than the detection threshold voltage of the driver. A parallel schottky diode can be connected between the OC and COM

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pins to prevent negative voltage on the OC pin in a noisy system. Since the desaturation circuit measures the V_{CE} of the IGBT or V_{DS} of the SiC MOSFET, not directly the current, the accuracy of the protection is not as high as the SenseFET based protection method. The current threshold cannot be accurately controlled in the protection.

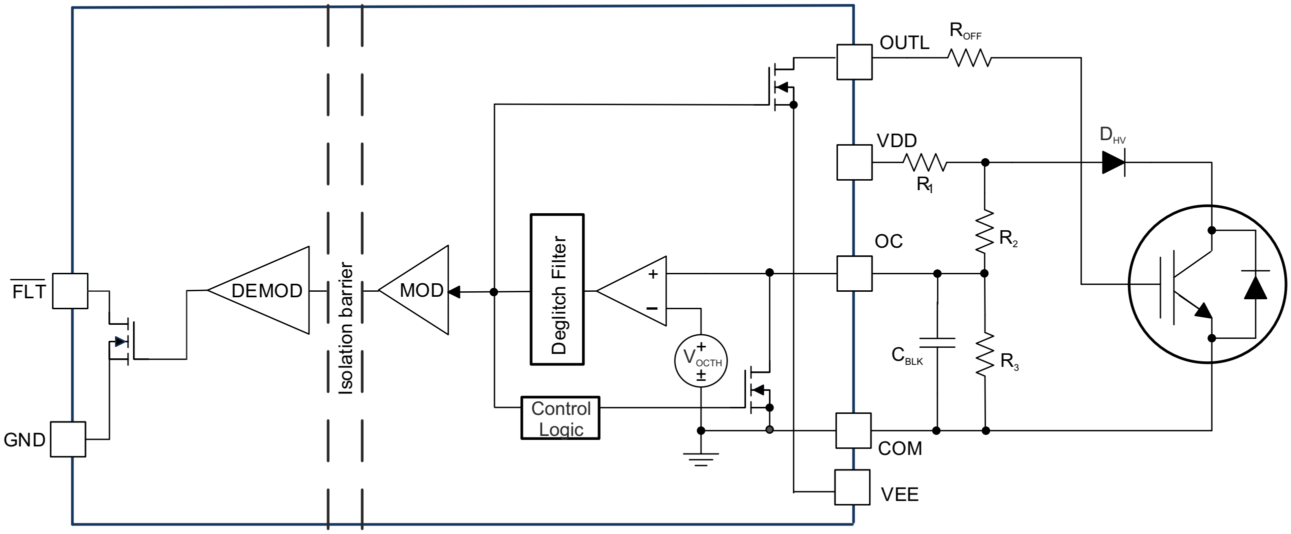

図 9-9. Overcurrent and Short Circuit Protection Based on Desaturation Circuit

9.2.2.7.3 Protection Based on Shunt Resistor in Power Loop

In lower power applications, to simplify the circuit and reduce cost, a shunt resistor can be used in series in the power loop and measure the current directly. Since the resistor is in series in the power loop, it directly measures the current and can have high accuracy by using a high precision resistor. The resistance needs to be small to reduce the power loss, and should have large enough voltage resolution for the protection. Since the sensing resistor is also in series in the gate driver loop, the voltage drop on the sensing resistor can cause the voltage drop on the gate voltage of the IGBT or SiC MOSFET modules. The parasitic inductance of the sensing resistor and the PCB trace of the sensing loop cause a noise voltage source during switching transient, which makes the gate voltage oscillate. Thus, this method is not recommended for a high power application, or when dI/dt is high. To use it in low power application, the shunt resistor loop should be designed to have the optimal voltage drop and minimum noise injection to the gate loop.

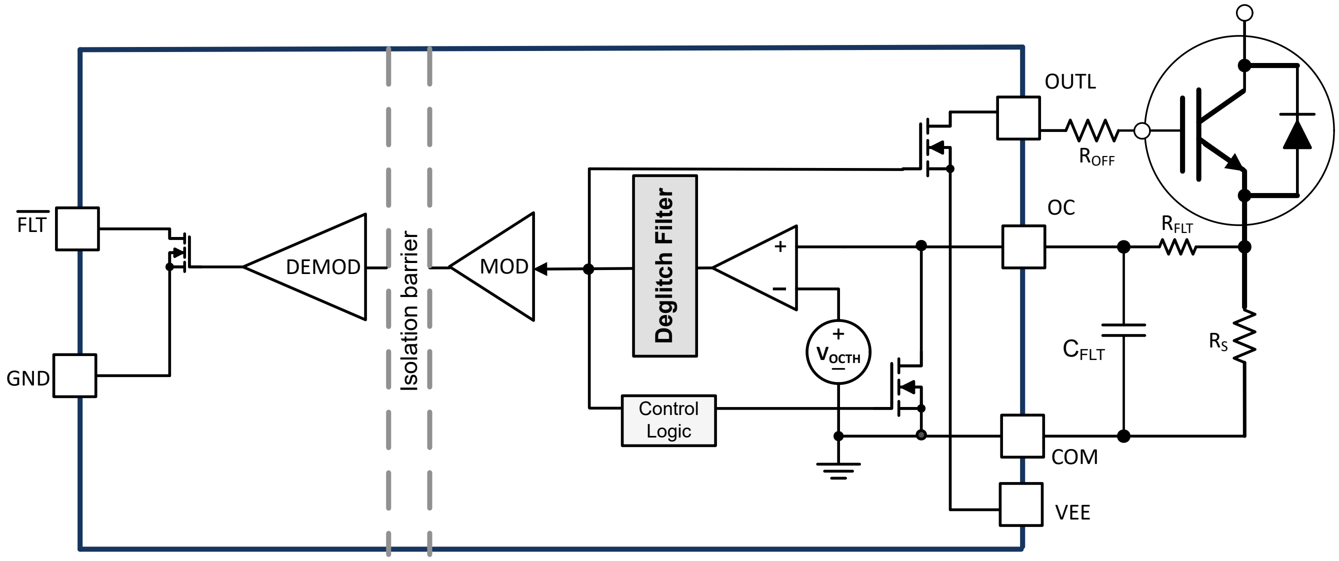

図 9-10. Overcurrent and Short Circuit Protection Based on Shunt Resistor

9.2.2.8 Higher Output Current Using an External Current Buffer

To increase the IGBT gate drive current, a noninverting current buffer (such as the NPN/PNP buffer shown in 図 9-11) can be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for peak currents up to 15 A, the D44VH10/ D45VH10 pair is for up to a 20-A peak.

In the case of an overcurrent detection, a soft turn off (STO) is activated. External components must be added to implement STO instead of normal turn-off speed when an external buffer is used. C_{STO} sets the timing for soft turn off and R_{STO} limits the inrush current to below the current rating of the internal FET (10 A). R_{STO} should be at least (VDD-VEE)/10. The soft turn-off timing is determined by the internal current source of 400 mA and the capacitor C_{STO}. C_{STO} is calculated using Equation 13.

$$C_{STO} = \frac{I_{STO} \cdot t_{STO}}{VDD - VEE} \tag{13}$$

- I_{STO} is the the internal STO current source, 400 mA
- t_{STO} is the desired STO timing

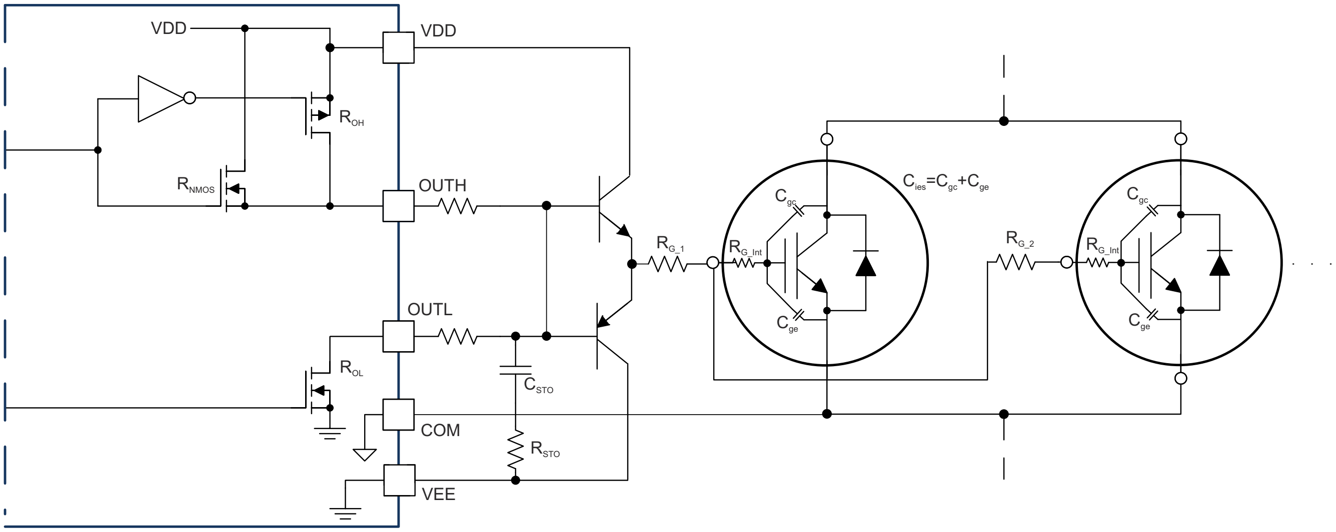

図 9-11. Current Buffer for Increased Drive Strength

9.2.3 Application Curves

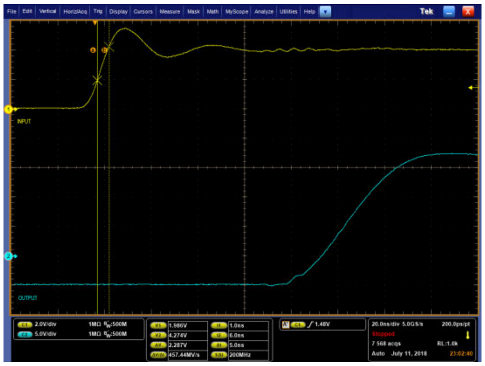

図 9-12. PWM Input (yellow) and Driver Output (blue) Rising Edge

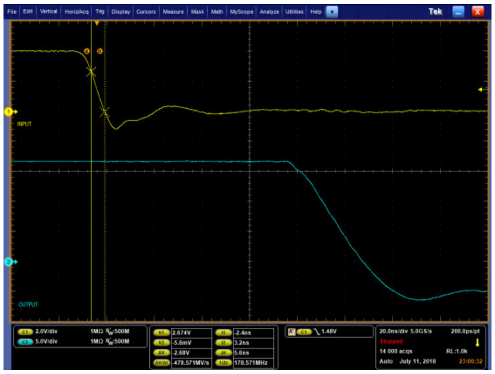

図 9-13. PWM Input (yellow) and Driver Output (blue) Falling Edge

10 Power Supply Recommendations

During the turn-on and turn-off switching transient, peak source and sink currents are provided by the VDD and VEE power supply. The large peak current is possible to drain the VDD and VEE voltage level and cause a voltage droop on the power supplies. To stabilize a power supply and ensure reliable operation, a set of decoupling capacitors are recommended at the power supplies. Considering the UCC21738-Q1 has ±10-A peak drive strength and can generate high dV/dt, a 10-μF bypass capacitor is recommended between VDD and COM, VEE and COM. A 1-μF bypass capacitor is recommended between VCC and GND due to less current comparing with output side power supplies. A 0.1-μF decoupling capacitor is also recommended for each power supply to filter out high frequency noise. The decoupling capacitors must be low ESR and ESL to avoid high frequency noise, and should be placed as close as possible to the VCC, VDD, and VEE pins to prevent noise coupling from the system parasitics of PCB layout.

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11 Layout

11.1 Layout Guidelines

Due to the strong drive strength of the UCC21738-Q1, careful considerations must be taken in PCB design. Below are some key points:

- The driver should be placed as close as possible to the power semiconductor to reduce the parasitic inductance of the gate loop on the PCB traces.
- The decoupling capacitors of the input and output power supplies should be placed as close as possible to the power supply pins. The peak current generated at each switching transient can cause high dI/dt and voltage spike on the parasitic inductance of the PCB traces.
- The driver COM pin should be connected to the Kelvin connection of the SiC MOSFET source or IGBT emitter. If the power device does not have a split Kelvin source or emitter, the COM pin should be connected as close as possible to the source or emitter terminal of the power device package to separate the gate loop from the high power switching loop.
- Use a ground plane on the input side to shield the input signals. The input signals can be distorted by the high frequency noise generated by the output side switching transients. The ground plane provides a low-inductance filter for the return current flow.
- If the gate driver is used for the low-side switch, which the COM pin is connected to the dc bus negative, use the ground plane on the output side to shield the output signals from the noise generated by the switch node; if the gate driver is used for the high-side switch, which the COM pin is connected to the switch node, use of the ground plane is not recommended.
- If the ground plane is not used on the output side, separate the return path of the OC and AIN ground loop from the gate loop ground which has large peak source and sink currents.
- No PCB trace or copper is allowed under the gate driver. A PCB cutout is recommended to avoid any noise coupling between the input and output side which can contaminate the isolation barrier.

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11.2 Layout Example

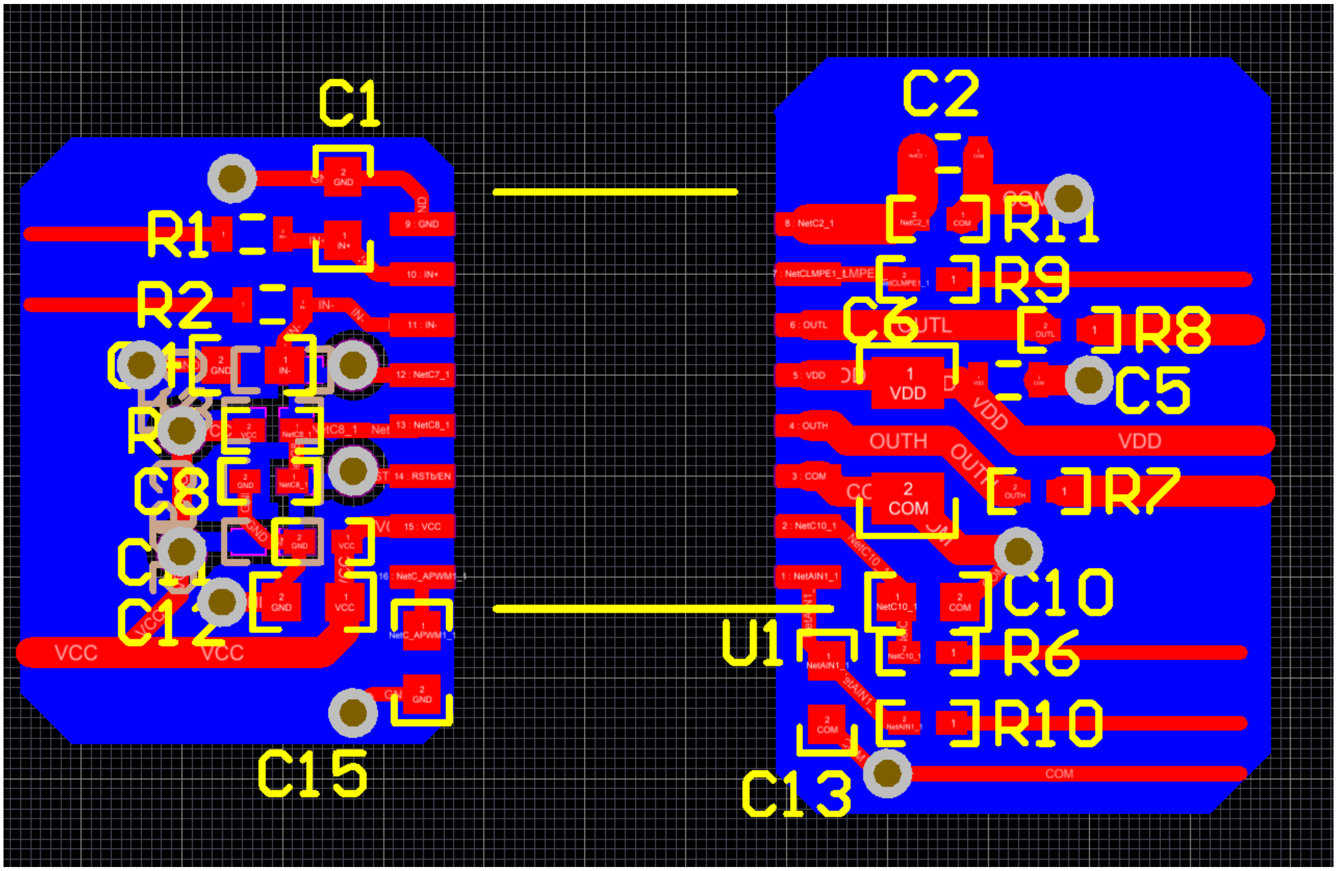

図 11-1. Layout Example

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12 Device and Documentation Support

12.1 Device Support

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *Isolation Glossary*

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12.7 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC21738QDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UCC21738Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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GENERIC PACKAGE VIEW

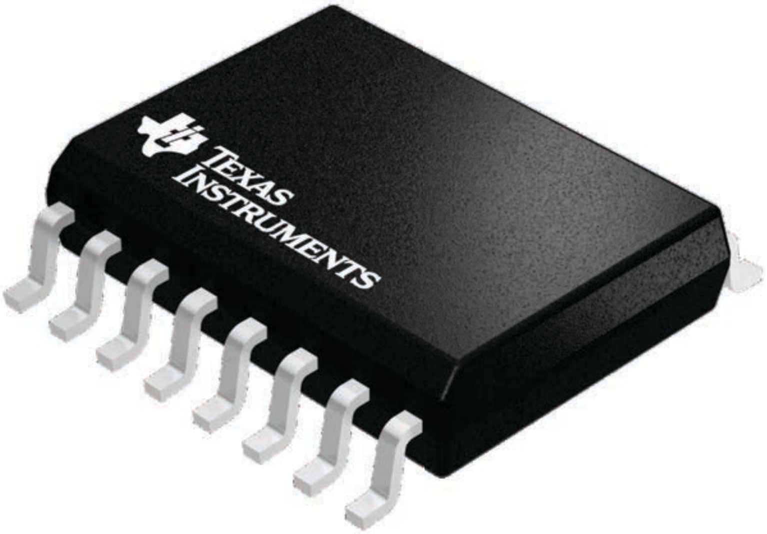
DW 16

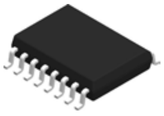
SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



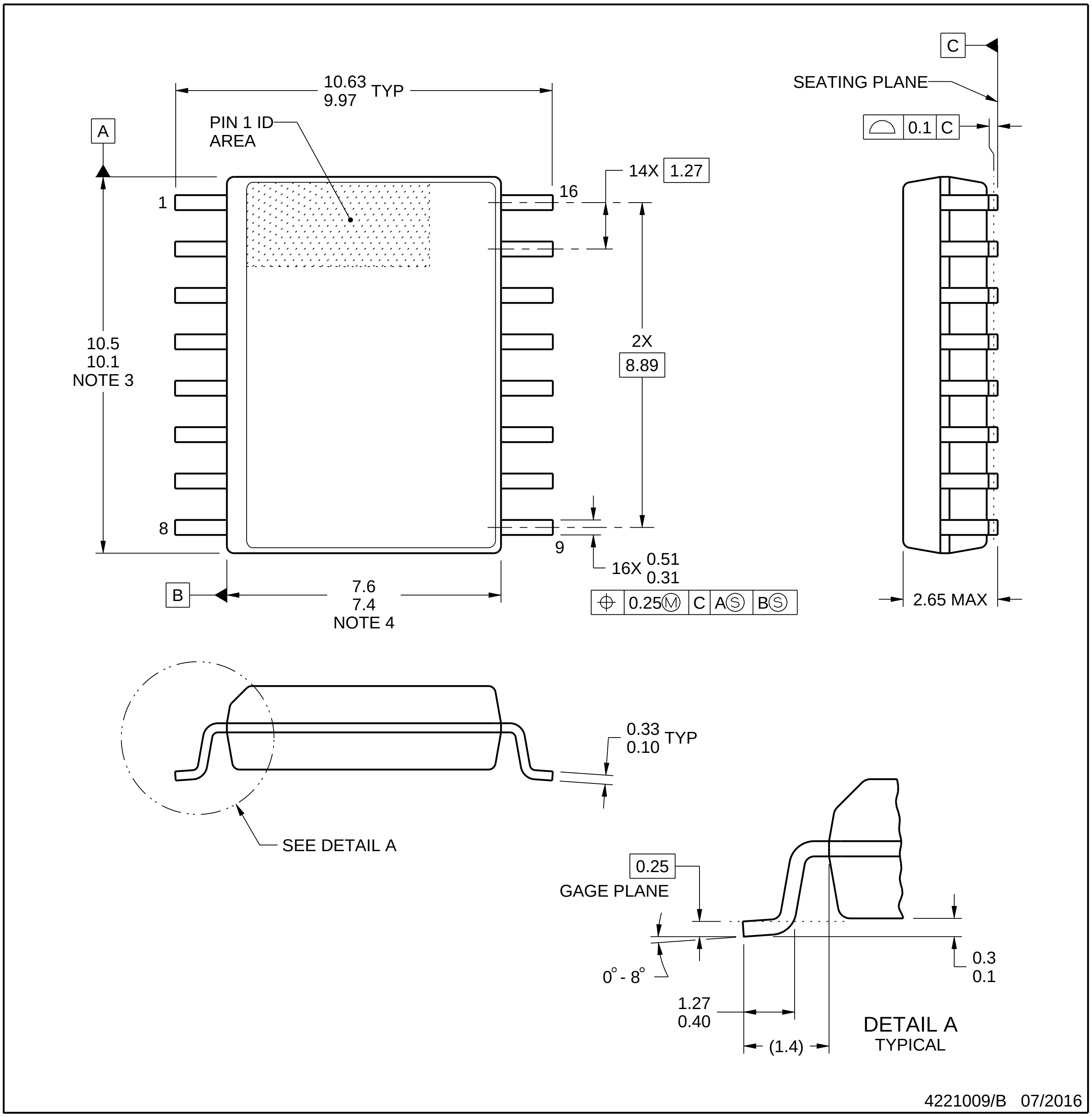


PACKAGE OUTLINE

DW0016B

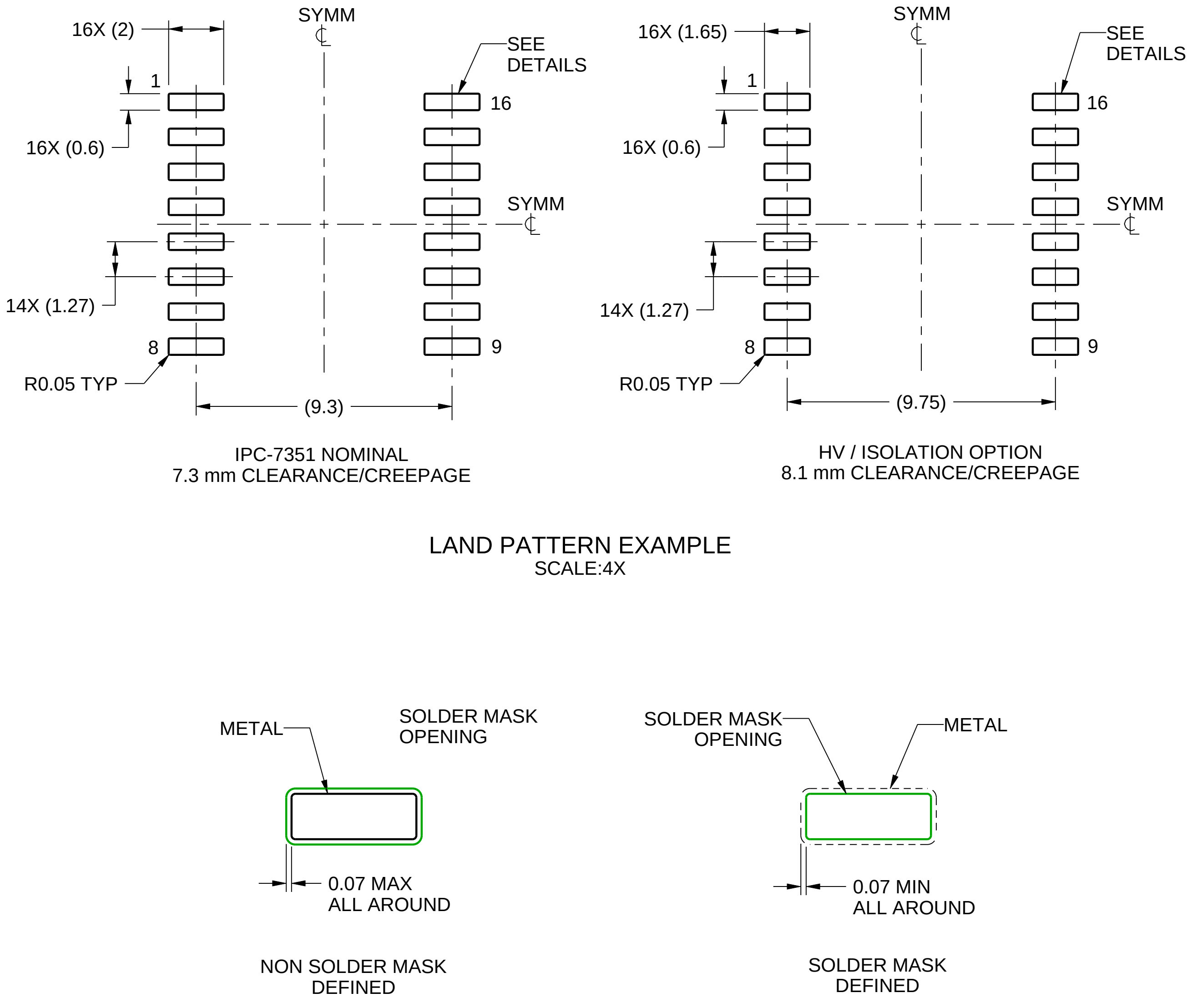
SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



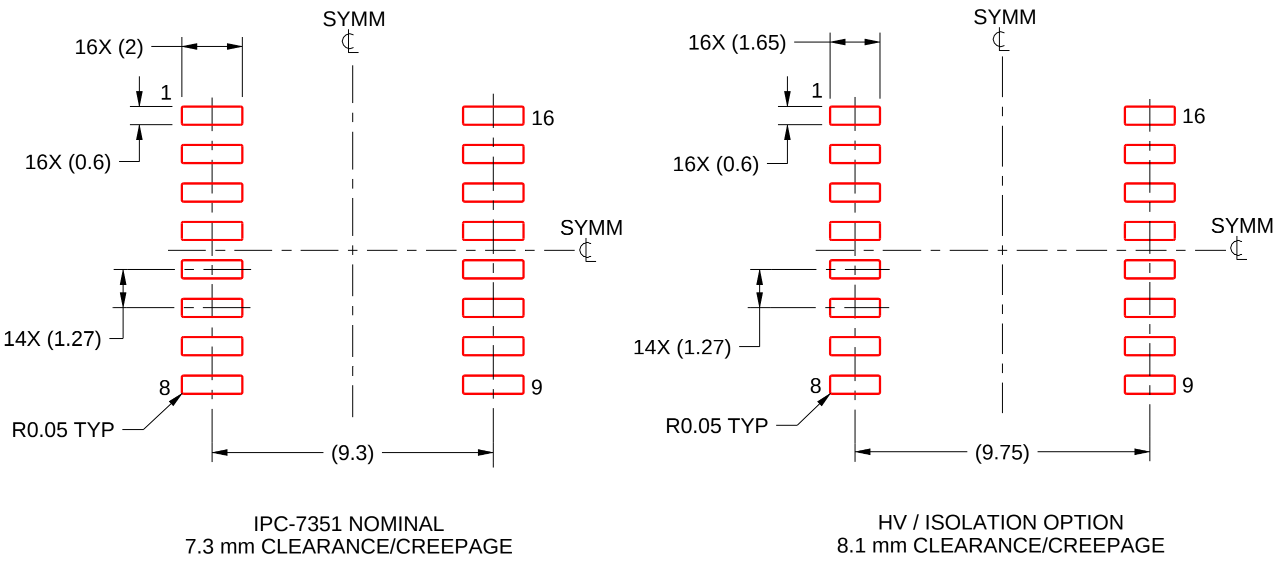
LAND PATTERN EXAMPLE
SCALE:4X

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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