

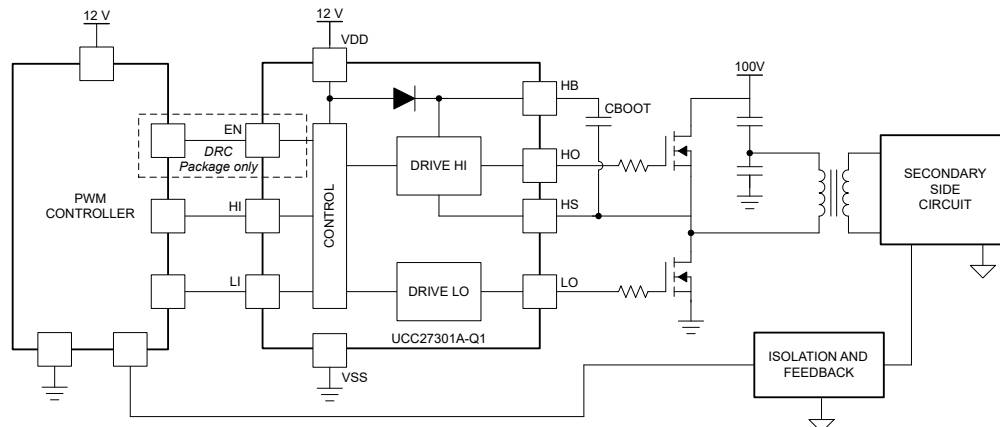
# UCC27301A-Q1 車載用、120V、3.7A/4.5A ハーフブリッジ・ドライバ、8V UVLO、クロス導通保護およびイネーブル搭載

## 1 特長

- 車載アプリケーション向けに認定済み
- 以下の結果で AEC-Q100 認定済み：
  - 温度グレード 1 ( $T_j = -40^{\circ}\text{C} \sim 150^{\circ}\text{C}$ )
  - HBM ESD 分類レベル 1B
  - CDM ESD 分類レベル C3
- 入力がインターロックされたハイサイドおよびローサイド構成によって 2 つの N チャネル MOSFET を駆動
- クロス導通保護機能は、両方の出力が同時にオンにならないようにすることで短絡を防止します
- 最大ブート電圧：DC 120V
- 3.7A シンク、4.5A ソース出力電流
- ブートストラップ・ダイオードを内蔵
- 入力ピンは電源電圧範囲に依存せず  $-10\text{V} \sim +20\text{V}$  を入力可能
- TTL 対応入力
- VDD 動作範囲：UVLO 付き 8V ~ 17V (絶対最大定格 20V)
- 立ち上がり時間 7.2ns、立ち下がり時間 5.5ns (1000pF 負荷時)
- イネーブル / デイセーブル機能、デイセーブル時の低消費電流 (7 $\mu\text{A}$ ) (DRC パッケージのみ)
- 高速伝搬遅延時間 (標準 20ns)
- 4ns の遅延マッチング
- 接合部温度定格： $-40^{\circ}\text{C} \sim +150^{\circ}\text{C}$

## 2 アプリケーション

- 車載用 DC/DC コンバータ
- 電動パワー・ステアリング (EPS)
- オンボード・チャージャ (OBC)
- 一体型ベルト・スタータ・ジェネレータ
- 車載用 HVAC (エアコン) コンプレッサ・モジュール



代表的なアプリケーションの図

## 3 概要

UCC27301A-Q1 車載用ハーフ・ブリッジ・ドライバは、115V の絶対最大スイッチ・ノード (HS) 電圧定格を持つ堅牢な N チャネル MOSFET ドライバです。ハーフ・ブリッジまたは同期整流降圧構成に基づくトポロジで 2 つの N チャネル MOSFET を制御できます。UCC27301A-Q1 はピーク・ソース電流能力が 3.7A、ピーク・シンク電流能力が 4.5A であるため、ミラー・プラトー通過時のスイッチング損失を最小限に抑えて大電力 MOSFET を駆動できます。UCC27301A-Q1 (HS ピン) の負の過渡電圧を処理できるため、寄生インダクタンスや浮遊容量によって生じる固有の負電圧からハイサイド・チャンネルを保護できます。

入力構造では DC  $-10\text{V}$  を直接処理できるため、堅牢性が増し、整流ダイオードなしでゲート駆動トランスに直接インターフェイスもできます。また、LI および HI 入力は電源電圧に依存せず、絶対最大定格は 20V です。

### 製品情報

部品番号	パッケージ (1)	イネーブル・ピン	本体サイズ (公称)
UCC27301A-Q1	DDA (PowerPAD™ SOIC, 8)	なし	4.90 × 3.90mm
UCC27301A-Q1	DRC (VSON, 10)	あり	3.00 × 3.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



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### 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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• DRC パッケージを「製品プレビュー」から「事前情報」に変更.....	1

## 5 概要 (続き)

ローサイドとハイサイドのゲート・ドライバが独立して制御され、それぞれのオン/オフ間に 4ns でマッチングが行われます。ただし、入力はインターロックされているため、HO と LO の両方の出力を同時に High にすることはできません。120V 定格のブートストラップ・ダイオードを内蔵しているため、ディスクリット・ブートストラップ・ダイオードは必要はありません。ハイサイド・ドライバとローサイド・ドライバの両方に低電圧誤動作防止機能 (UVLO) が搭載され、対称的なオン/オフ動作を実現しながら、駆動電圧が規定のスレッシュホルド未満の場合は出力が強制的に Low になります。

## 6 Pin Configuration and Functions

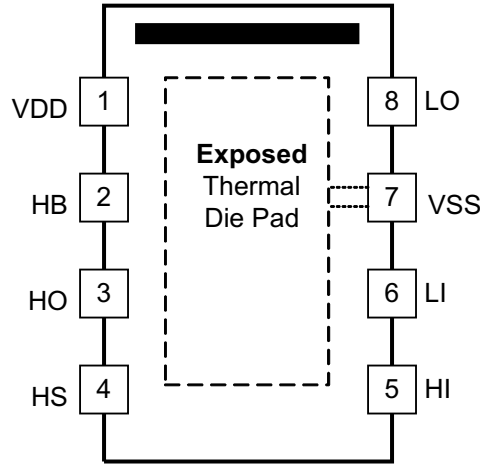


图 6-1. DDA Package 8-Pin SOIC with PowerPad™ Top View

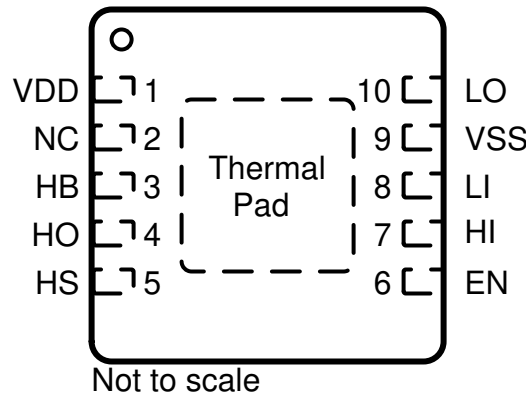


图 6-2. DRC Package 10-Pin SON Top View

表 6-1. Pin Functions

NAME	PIN		TYPE <sup>(4)</sup>	DESCRIPTION
	NO. (DDA)	NO. (DRC)		
EN	N/A	6	I	Enable input. When this pin is pulled high, it will enable the driver. If left floating or pulled low, it will disable the driver. A filter capacitor, typically 1-10nF, is recommended to be placed from EN to VSS (pin 7) to increase noise immunity in sensitive applications.
HB	2	3	P	High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 $\mu$ F to 0.1 $\mu$ F. The capacitor value is dependant on the gate charge of the high-side MOSFET and must also be selected based on speed and ripple criteria.
HI	5	7	I	High-side input. <sup>(1)</sup>
HO	3	4	O	High-side output. Connect to the gate of the high-side power MOSFET.
HS	4	5	P	High-side source connection. Connect to source of high-side power MOSFET. Connect the negative side of bootstrap capacitor to this pin.
LI	6	8	I	Low-side input. <sup>(1)</sup>
LO	8	10	O	Low-side output. Connect to the gate of the low-side power MOSFET.
VDD	1	1	P	Positive supply to the lower-gate driver. Decouple this pin to VSS (GND). Typical decoupling capacitor range is 0.22 $\mu$ F to 4.7 $\mu$ F (see <sup>(2)</sup> ).

**表 6-1. Pin Functions (continued)**

PIN			TYPE <sup>(4)</sup>	DESCRIPTION
NAME	NO. (DDA)	NO. (DRC)		
VSS	7	9	G	Negative supply terminal for the device that is generally grounded.
Thermal pad <sup>(3)</sup>			—	Electrically referenced to V <sub>SS</sub> (GND). Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.

- (1) HI, LI, and EN inputs are assumed to connect to a low impedance source signal. The source output impedance is assumed less than 100 Ω. If the source impedance is greater than 100 Ω, add a bypassing capacitor, each, between HI to VSS, LI to VSS, and EN to VSS. The added capacitor value depends on the noise levels presented on the pins, typically from 1 nF to 10 nF should be effective to eliminate the possible noise effect. When noise is present on two pins, HI or LI, the effect is to cause HO and LO malfunctions to have wrong logic outputs.
- (2) For cold temperature applications TI recommends the upper capacitance range. Follow the [Layout Guidelines](#) for PCB layout.
- (3) The thermal pad is not directly connected to any leads of the package; however, it is electrically and thermally connected to the substrate which is the ground of the device.
- (4) G = Ground, I = Input, O = Output, and P = Power.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range and all voltages are with respect to  $V_{SS}$  (unless otherwise noted).<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{DD}$	Supply voltage	-0.3	20	V
$V_{HI}, V_{LI}$	Input voltages on HI and LI	-10	20	V
$V_{EN}$	Input voltages on EN	-10	20	V
$V_{LO}$	Output voltage on LO	DC	$V_{DD} + 0.3$	V
		Repetitive pulse < 100 ns <sup>(2)</sup>	$V_{DD} + 0.3$	
$V_{HO}$	Output voltage on HO	DC	$V_{HS} - 0.3$ $V_{HB} + 0.3$	V
		Repetitive pulse < 100 ns <sup>(2)</sup>	$V_{HS} - 2$ $V_{HB} + 0.3$	
$V_{HS}$	Voltage on HS	DC	-1    115	V
		Repetitive pulse < 100 ns <sup>(2)</sup>	$-(24V - V_{DD})$ 115	
$V_{HB}$	Voltage on HB	-0.3	120	V
	Voltage on HB-HS	-0.3	20	V
$T_J$	Operating junction temperature	-40	150	°C
	Lead temperature (soldering, 10 sec.)		300	°C
$T_{stg}$	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Values are verified by characterization and are not production tested.

### 7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per AEC Q100-011	±1500

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

Over operating free-air temperature range and all voltages are with respect to  $V_{SS}$  (unless otherwise noted).

		MIN	NOM	MAX	UNIT
$V_{DD}$	Supply voltage	8	12	17	V
$V_{HS}$	Voltage on HS	-1		105	V
	Voltage on HS (repetitive pulse < 100 ns) <sup>(1)</sup>	$-(24V - V_{DD})$		110	
$V_{HB}$	Voltage on HB	$V_{HS} + 8.0, V_{DD} - 1$	$V_{HS} + 17, 115$		
$SR_{HS}$	Voltage slew rate on HS			50	V/ns
$T_J$	Operating junction temperature	-40		150	°C

- (1) Values are verified by characterization and are not production tested.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		UCC27301A-Q1	UCC27301A-Q1	UNIT
		DDA (PowerPad™ SOIC)	DRC (VSON)	
		8 Pins	10 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.1	51.9	°C/W

## 7.4 Thermal Information (continued)

THERMAL METRIC <sup>(1)</sup>		UCC27301A-Q1	UCC27301A-Q1	UNIT
		DDA (PowerPad™ SOIC)	DRC (VSON)	
		8 Pins	10 Pins	
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	60.8	58.3	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	21.3	24.6	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	6.3	1.7	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	21.3	24.6	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	6.2	9.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

## 7.5 Electrical Characteristics

V<sub>DD</sub> = V<sub>HB</sub> = 12 V, V<sub>HS</sub> = V<sub>SS</sub> = 0 V, No load on LO or HO, T<sub>A</sub> = T<sub>J</sub> = -40°C to +150°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENTS</b>						
I <sub>DD</sub>	VDD quiescent current	V <sub>LI</sub> = V <sub>HI</sub> = 0, V <sub>EN</sub> = 3V	0.05	0.085	0.17	mA
I <sub>DDO</sub>	VDD operating current	f = 500 kHz, C <sub>LOAD</sub> = 0, V <sub>EN</sub> = 3V	2.1	2.5	6.5	mA
I <sub>HB</sub>	Boot voltage quiescent current	V <sub>LI</sub> = V <sub>HI</sub> = 0 V, V <sub>EN</sub> = 3V	0.015	0.065	0.1	mA
I <sub>HBO</sub>	Boot voltage operating current	f = 500 kHz, C <sub>LOAD</sub> = 0, V <sub>EN</sub> = 3V	1.5	2.5	5.1	mA
I <sub>HBS</sub>	HB to VSS quiescent current	V <sub>HS</sub> = V <sub>HB</sub> = 105 V, V <sub>EN</sub> = 3V		0.0005	1	μA
I <sub>HBSO</sub>	HB to VSS operating current	f = 500 kHz, C <sub>LOAD</sub> = 0, V <sub>EN</sub> = 3V		0.07	1.2	mA
I <sub>DD_DIS</sub>	Driver Current when EN pin is pulled low (Disabled)	UCC27301AQDRCRQ1 only, V <sub>EN</sub> = 0		7		μA
<b>INPUT</b>						
V <sub>HIT_HI</sub>	Input voltage high threshold		1.7	2.3	2.55	V
V <sub>HIT_LI</sub>	Input voltage high threshold		1.7	2.3	2.55	V
V <sub>LIT_HI</sub>	Input voltage low threshold		1.2	1.6	1.9	V
V <sub>LIT_LI</sub>	Input voltage low threshold		1.2	1.6	1.9	V
V <sub>IHYS_HI</sub>	Input voltage Hysteresis			0.7		V
V <sub>IHYS_LI</sub>	Input voltage Hysteresis			0.7		V
R <sub>IN_HI</sub>	Input pulldown resistance	V <sub>IN</sub> = 3V		68		kΩ
R <sub>IN_LI</sub>	Input pulldown resistance	V <sub>IN</sub> = 3V		68		kΩ
<b>ENABLE</b>						
V <sub>EN</sub>	Voltage threshold on EN pin to enable the driver	UCC27301AQDRCRQ1 only	1.7	2.3	2.55	V
V <sub>DIS</sub>	Voltage threshold on EN pin to disable the driver	UCC27301AQDRCRQ1 only	1.2	1.6	1.9	V
V <sub>ENHYS</sub>	Enable pin Hysteresis	UCC27301AQDRCRQ1 only		0.7		V
R <sub>EN</sub>	EN pin internal pull-down resistance	UCC27301AQDRCRQ1 only, V <sub>EN</sub> = 3V		80		kΩ
T <sub>EN</sub>	EN pin response time	UCC27301AQDRCRQ1 only, V <sub>EN</sub> = 3V		18	70	μs
T <sub>DIS</sub>	EN pin response time	UCC27301AQDRCRQ1 only, V <sub>EN</sub> = 0V		1.5	10	μs
<b>UNDERVOLTAGE PROTECTION (UVLO)</b>						
V <sub>DDR</sub>	VDD rising threshold		6.2	7	7.8	V
V <sub>DDHYS</sub>	VDD threshold hysteresis			0.5		V
V <sub>HBR</sub>	VHB rising threshold		5.6	6.7	7.9	V
V <sub>HBHYS</sub>	VHB threshold hysteresis			1.1		V
<b>BOOTSTRAP DIODE</b>						
V <sub>F</sub>	Low-current forward voltage	I <sub>VDD-HB</sub> = 100 μA		0.65	0.85	V
V <sub>FI</sub>	High-current forward voltage	I <sub>VDD-HB</sub> = 100 mA		0.9	1.05	V

## 7.5 Electrical Characteristics (continued)

 $V_{DD} = V_{HB} = 12\text{ V}$ ,  $V_{HS} = V_{SS} = 0\text{ V}$ , No load on LO or HO,  $T_A = T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_D$	Dynamic resistance, $\Delta V/\Delta I$	$I_{VDD-HB} = 160\text{ mA}$ and $180\text{ mA}$	0.3	0.5	0.85	$\Omega$
<b>LO GATE DRIVER</b>						
$V_{LOL}$	Low level output voltage	$I_{LO} = 100\text{ mA}$		0.1	0.19	V
$V_{LOH}$	High level output voltage	$I_{LO} = -100\text{ mA}$ , $V_{LOH} = V_{DD} - V_{LO}$		0.16	0.29	V
	Peak pullup current <sup>(1)</sup>	$V_{LO} = 0\text{ V}$		3.7		A
	Peak pulldown current <sup>(1)</sup>	$V_{LO} = 12\text{ V}$		4.5		A
<b>HO GATE DRIVER</b>						
$V_{HOL}$	Low level output voltage	$I_{HO} = 100\text{ mA}$		0.1	0.19	V
$V_{HOH}$	High level output voltage	$I_{HO} = -100\text{ mA}$ , $V_{HOH} = V_{HB} - V_{HO}$		0.16	0.29	V
	Peak pullup current <sup>(1)</sup>	$V_{HO} = 0\text{ V}$		3.7		A
	Peak pulldown current <sup>(1)</sup>	$V_{HO} = 12\text{ V}$		4.5		A

(1) Parameter not tested in production.

## 7.6 Switching Characteristics

 $V_{DD} = V_{HB} = 12\text{ V}$ ,  $V_{HS} = V_{SS} = 0\text{ V}$ , No load on LO or HO,  $T_A = T_J = -40^\circ\text{C}$  to  $+150^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>PROPAGATION DELAYS</b>						
$t_{DLFF}$	VLI falling to VLO falling	$C_{LOAD} = 0\text{ pF}$ , from $V_{LIT}$ of LI to 90% of LO falling		16		ns
$t_{DHFF}$	VHI falling to VHO falling	$C_{LOAD} = 0\text{ pF}$ , from $V_{LIT}$ of HI to 90% of HO falling		16		ns
$t_{DLRR}$	VLI rising to VLO rising	$C_{LOAD} = 0\text{ pF}$ , from $V_{HIT}$ of LI to 10% of LO rising		20		ns
$t_{DHRR}$	VHI rising to VHO rising	$C_{LOAD} = 0\text{ pF}$ , $C_{LOAD} = 0\text{ pF}$ , from $V_{HIT}$ of HI to 10% of HO rising		20		ns
<b>DELAY MATCHING</b>						
$t_{MON}$	LI ON, HI OFF	$T_J = 25^\circ\text{C}$ , from 10% of LO rising to 90% of HO falling		4	9.5	ns
$t_{MON}$	LI ON, HI OFF	$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$ , from 10% of LO rising to 90% of HO falling		4	17	ns
$t_{MOFF}$	LI OFF, HI ON	$T_J = 25^\circ\text{C}$ , from 90% of LO falling to 10% of HO rising		4	9.5	ns
$t_{MOFF}$	LI OFF, HI ON	$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$ , from 90% of LO falling to 10% of HO rising		4	17	ns
<b>OUTPUT RISE AND FALL TIME</b>						
$t_{R\_LO}$	LO rise time	$C_{LOAD} = 1000\text{ pF}$ , from 10% to 90%		7.2		ns
$t_{R\_HO}$	HO rise time	$C_{LOAD} = 1000\text{ pF}$ , from 10% to 90%		7.2		ns
$t_{F\_LO}$	LO fall time	$C_{LOAD} = 1000\text{ pF}$ , from 10% to 90%		5.5		ns
$t_{F\_HO}$	HO fall time	$C_{LOAD} = 1000\text{ pF}$ , from 10% to 90%		5.5		ns
$t_{R\_LO\_p1}$	LO rise time (3 V to 9 V)	$C_{LOAD} = 0.1\text{ }\mu\text{F}$ , (3V to 9V)		0.36	0.6	$\mu\text{s}$
$t_{R\_HO\_p1}$	HO rise time (3 V to 9 V)	$C_{LOAD} = 0.1\text{ }\mu\text{F}$ , (3V to 9V)		0.36	0.6	$\mu\text{s}$
$t_{F\_LO\_p1}$	LO fall time (9 V to 3 V)	$C_{LOAD} = 0.1\text{ }\mu\text{F}$ , (9V to 3V)		0.15	0.4	$\mu\text{s}$
$t_{F\_HO\_p1}$	HO fall time (9 V to 3 V)	$C_{LOAD} = 0.1\text{ }\mu\text{F}$ , (9V to 3V)		0.15	0.4	$\mu\text{s}$
<b>MISCELLANEOUS</b>						
$t_{IN\_PW}$	Minimum input pulse width that changes the output LO				50	ns
$t_{IN\_PW}$	Minimum input pulse width that changes the output HO				50	ns
$t_{OFF\_BSD}$	Bootstrap diode turnoff time <sup>(1) (2)</sup>	$I_F = 20\text{ mA}$ , $I_{REV} = 0.5\text{ A}$ <sup>(3)</sup>		20		ns

(1) Parameter not tested in production.



- (2) Typical values for  $T_A = 25^\circ\text{C}$ .
- (3)  $I_F$ : Forward current applied to bootstrap diode,  $I_{REV}$ : Reverse current applied to bootstrap diode.

## 8 Detailed Description

### 8.1 Overview

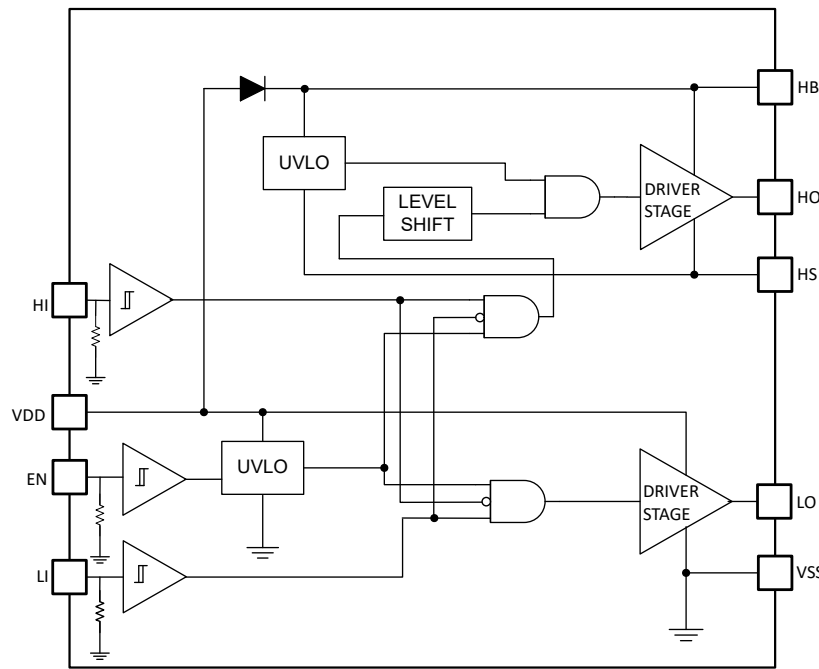
The UCC27301A-Q1 is a high-voltage gate driver designed to drive both the high-side and the low-side N-channel MOSFETs in a synchronous buck or a half-bridge configurations. The two outputs are independently controlled with two TTL-compatible input signals. The device can also work with CMOS type control signals at its inputs as long as the signals meet the turn-on and turn-off threshold specifications of the device. The floating high-side driver is capable of operating with an HB voltage up to 115 V with respect to VSS. A 120-V bootstrap diode is integrated in the UCC27301A-Q1 device to charge the high-side gate drive bootstrap capacitor. A robust level shifter operates at high speed while consuming low power and provides clean level transitions from the control logic to the high-side gate driver. Undervoltage lockout (UVLO) is provided on both the low-side and the high-side power rails. EN pin is provided (in DRC packaged parts) to enable or disable the driver. The driver also has input interlock functionality, which shuts off both the outputs when the two inputs overlap.

In the UCC27301A-Q1 automotive device, the high side and low side have separate, interlocked inputs that allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the UCC27301A-Q1. The high-side driver is referenced to the switch node (HS), which is typically the source pin of the high-side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to V<sub>SS</sub>, which is typically ground. The UCC27301A-Q1 functions are divided into the input stages, UVLO protection, level shift, boot diode, and output driver stages.

**表 8-1. UCC27301A-Q1 Highlights**

FEATURE	BENEFIT
+3.7-A/-4.5-A peak source and sink currents	High peak current ideal for driving large power MOSFETs with minimal power loss (fast-drive capability at Miller plateau)
Input pins (HI and LI) can directly handle -10 VDC up to 20 VDC	Increased robustness and ability to handle undershoot and overshoot can interface directly to gate-drive transformers without having to use rectification diodes.
120-V internal boot diode	Provides voltage margin to meet telecom 100-V surge requirements
Switch node (HS pin) able to handle -18 V maximum for 100 ns	Allows the high-side channel to have extra protection from inherent negative voltages caused by parasitic inductance and stray capacitance
Robust ESD circuitry to handle voltage spikes	Excellent immunity to large dV/dT conditions
16-ns/20-ns propagation delays with 7.2-ns rise time and 5.5-ns fall time	Best-in-class switching characteristics and extremely low-pulse transmission distortion
Cross-conduction protection	Interlocks inputs to prevent shoot-through
Enable/disable functionality	Offers additional control over the driver for different system states (such as powerup sequencing) and a low quiescent current consumption when disabled
4-ns (typical) delay matching between channels	Avoids transformer volt-second offset in bridge
Symmetrical UVLO circuit	Ensures high-side and low-side shut down at the same time
TTL optimized thresholds with increased hysteresis	Complementary to analog or digital PWM controllers; increased hysteresis offers added noise immunity

## 8.2 Functional Block Diagram



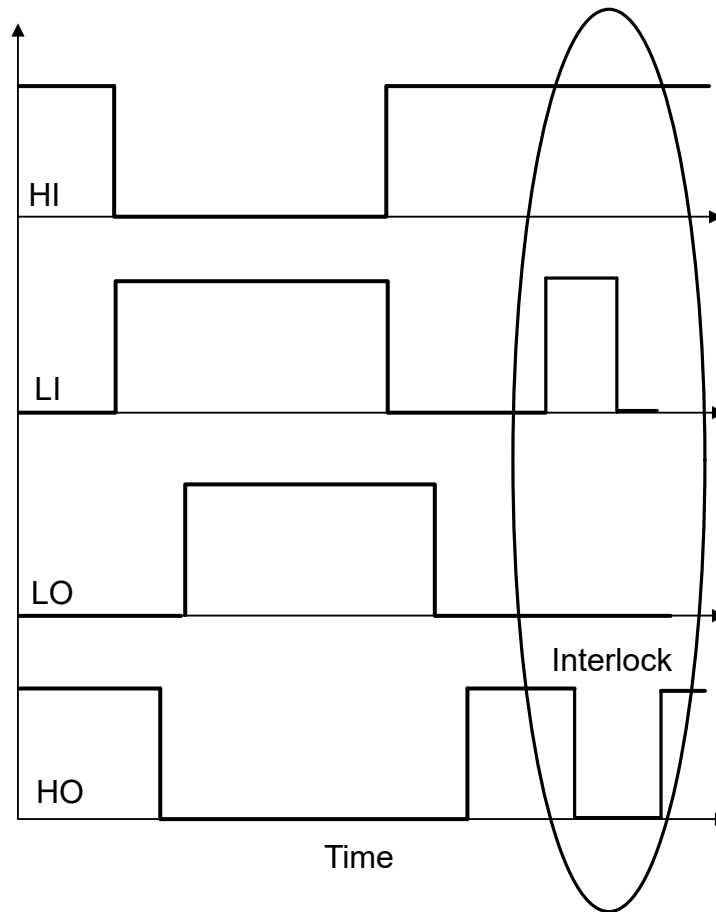
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## 8.3 Feature Description

### 8.3.1 Input Stages and Cross-Conduction Protection

The two inputs operate independently, with an exception that both outputs will be pulled low when both inputs are high or overlap. The independence allows for full control of two outputs compared to the gate drivers that have a single input. The device has input interlock or cross-conduction protection. Whenever both the inputs are high, the internal logic turns both the outputs off. Once the device is in this mode, when one of the inputs goes low, the outputs follow the input logic. There is no other fixed time de-glitch filter implemented in the device and therefore propagation delay and delay matching are not sacrificed. In other words, there is no built-in dead-time due to the interlock feature. Any noise on the input that could cause the output to shoot-through will be filtered by this feature and the system stays protected.

The inputs are TTL-logic compatible. The device can also work with CMOS type control signals at its inputs as long as the signals meet the turn-on and turn-off threshold specifications of the device. Because the inputs are independent of supply voltage, they can be connected to outputs of either digital controller or analog controller. Inputs can accept wide slew rate signals and input can withstand negative voltage to increase the robustness. Small filter at the inputs of the driver further improves system robustness in noise prone applications. The inputs have internal pull down resistors with typical value of 68 kΩ. Thus, when the inputs are floating, the outputs are held low.



⊗ 8-1. Interlock or Input Shoot-Through Protection

### 8.3.2 Enable

The device in DRC package has an enable (EN) pin. The outputs will be active only if the EN pin voltage is above the threshold voltage. Outputs will be held low if EN pin is left floating or pulled-down to ground. An internal 80-k $\Omega$  resistor pulls the EN pin to VSS. Thus, leaving the EN pin floating disables the device. Externally pulling EN pin to ground shall also disable the device. If the EN pin is not used, then it is recommended to tie it to VDD pin. If a pull-up resistor needs to be used then a strong pull-up resistor is recommended. For 12-V supply voltage, a 10-k $\Omega$  pull-up is suggested. In noise prone application, a small filter capacitor, 1 nF to 10 nF, should be connected from the EN pin to VSS pin as close to the device as possible. An analog or a digital controller output pin could be connected to EN pin to enable or disable the device. Built-in hysteresis helps prevent any nuisance tripping or chattering of the outputs.

### 8.3.3 Undervoltage Lockout (UVLO)

Both the high-side and the low-side driver stages include UVLO protection circuitry which monitors the supply voltage (VDD) and the bootstrap capacitor voltage ( $V_{HB}$  to  $V_{HS}$ ). The UVLO circuit inhibits each output until sufficient supply voltage is available to turn on the external MOSFETs. The built-in UVLO hysteresis prevents chattering during supply voltage variations. When the supply voltage is applied to the VDD pin of the device, both the outputs are held low until VDD exceeds the UVLO threshold. Any UVLO condition on the bootstrap capacitor ( $V_{HB}$ – $V_{HS}$ ) disables only the high-side output (HO).

### 8.3.4 Level Shifter

The level shift circuit is the interface from the high-side input, which is a VSS referenced signal, to the high-side driver stage which is referenced to the switch node (HS pin). The level shift allows control of the HO output which is referenced to the HS pin. The delay introduced by the level shifter is kept as low as possible and

therefore the device provides excellent propagation delay characteristic and delay matching with the low-side driver output. Low delay matching allows power stages to operate with less dead time. The reduction in dead time is very important in applications where high efficiency is required.

### 8.3.5 Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC27301A-Q1 family of drivers. The diode anode is connected to  $V_{DD}$  and cathode connected to  $V_{HB}$ . With the  $V_{HB}$  capacitor connected to HB and the HS pins, the  $V_{HB}$  capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

### 8.3.6 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from  $V_{DD}$  to  $V_{SS}$  and the high side is referenced from  $V_{HB}$  to  $V_{HS}$ . The device output stages feature a pull-up structure which delivers the highest peak source current when it is most needed, during the Miller plateau region of the power switch turn on transition. The output pull-up and pull-down structure of the device is totem pole NMOS-PMOS structure.

### 8.3.7 Negative Voltage Transients

In most applications, the body diode of the external low-side power MOSFET clamps the HS node to ground. In some situations, board capacitance and inductance can cause the HS node to transiently swing several volts below ground, before the body diode of the external low-side MOSFET clamps this swing. The HS pin in the device is allowed to swing below ground as long as specifications are not violated and conditions mentioned in this section are followed.

Ensure that the HB to HS operating voltage is within the recommended operating conditions. Hence, if the HS pin transient voltage is  $-5$  V, then VDD (and thus HB) is ideally limited to 12 V to keep the HB to HS voltage below 17 V. Generally when HS swings negative, HB follows HS instantaneously and therefore the HB to HS voltage does not significantly overshoot.

HS must always be at a lower potential than HO. Pulling HO more negative than specified conditions can activate parasitic transistors which may result in excessive current flow from the HB supply. This may result in damage to the device. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and VSS to protect the device from this type of transient. The diode must be placed as close to the device pins as possible in order to be effective.

Low ESR bypass capacitors from HB to HS and from VDD to VSS are essential for proper operation of the gate driver device. The capacitor should be located at the leads of the device to minimize series inductance. The peak currents from LO and HO can be quite large. Any series inductance with the bypass capacitor causes voltage ringing at the leads of the device which must be avoided for reliable operation.

Based on application board design and other operating parameters, along with HS pin, other pins such as HI and LI input pins might also transiently swing below ground. To accommodate such operating conditions, the input pins of the device are capable of handling absolute maximum of  $-10$  V. Based on the layout and other design constraints, sometimes the outputs, HO and LO, might also see transient voltages for short durations. Therefore, the device can also handle  $-2$ -V transients with less than 100-ns duration on the HO and LO output pins.

## 8.4 Device Functional Modes

When the device is enabled, the device operates in normal mode and UVLO mode. See [セクション 8.3.3](#) for more information on UVLO operation mode. In normal mode when the VDD and VHB–HS are above UVLO threshold, the output stage is dependent on the states of the EN, HI and LI pins. The output HO and LO will be low if input state is floating.

**表 8-2. Device Logic Table**

EN <sup>(1)</sup>	HI	LI	HO <sup>2</sup>	LO <sup>3</sup>
L	X	X	L	L

表 8-2. Device Logic Table (continued)

EN <sup>(1)</sup>	HI	LI	HO <sup>2</sup>	LO <sup>3</sup>
H	L	L	L	L
H	L	H	L	H
H	H	L	H	L
H	H	H	L	L

- (1) EN pin is available only in DRC package.  
 (2) HO is measured with respect to HS.  
 (3) LO is measured with respect to VSS.

## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

To affect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers, and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

### 9.2 Typical Application

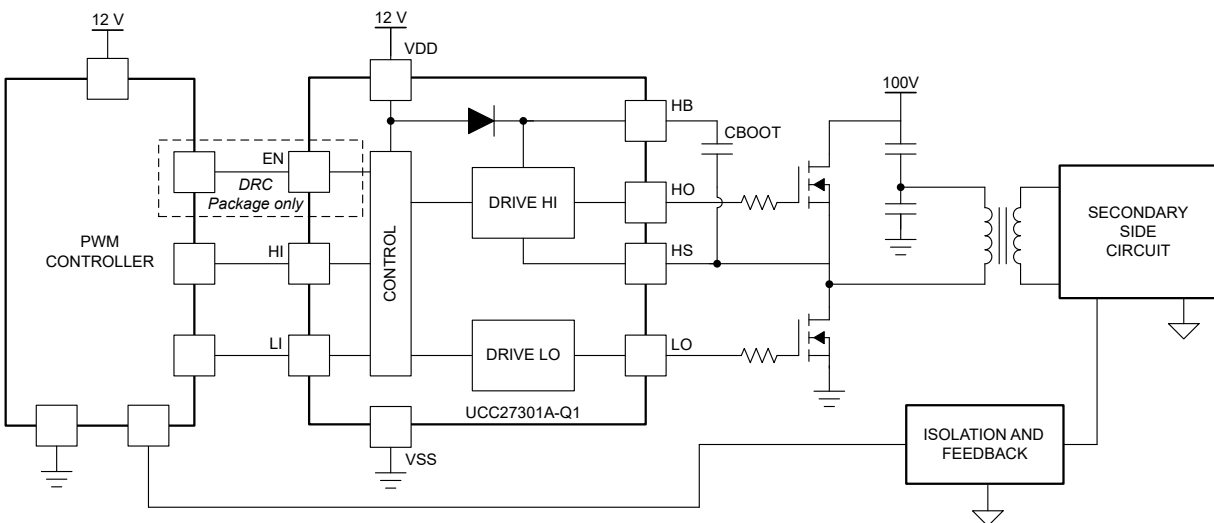


図 9-1. UCC27301A-Q1 Typical Application Diagram

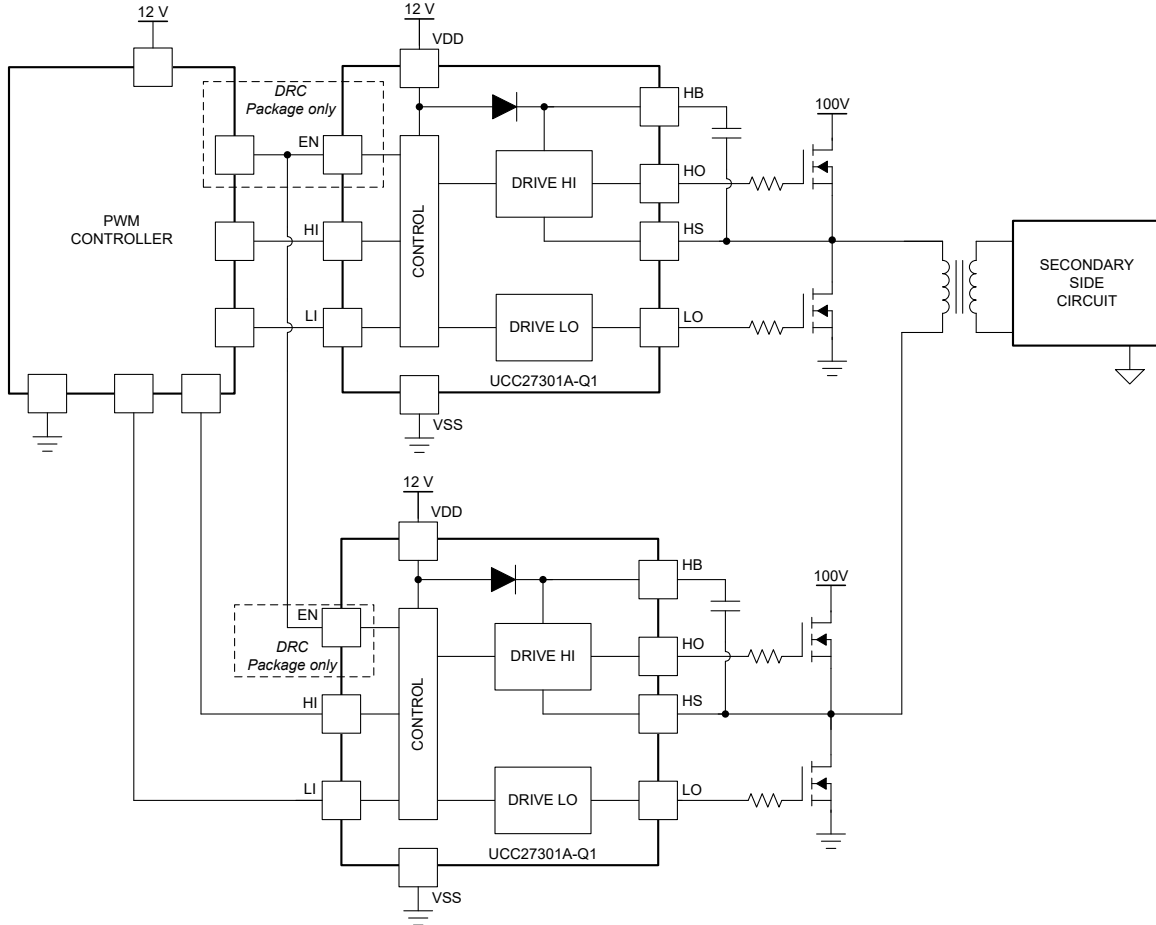


图 9-2. UCC27301A-Q1 Automotive Typical Application Diagram

### 9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Specifications

DESIGN PARAMETER	EXAMPLE VALUE
Supply voltage, VDD	12 V
Voltage on HS, VHS	0 V to 100 V
Voltage on HB, VHB	12 V to 112 V
Output current rating, IO	-4.5 A to 3.7A
Operating frequency	500 kHz



## 9.2.2 Detailed Design Procedure

### 9.2.2.1 Input Threshold Type

The UCC27301A-Q1 device has an input absolute maximum voltage range from –10 V to 20 V. This increased robustness means that both parts can be directly interfaced to gate drive transformers. The device features TTL compatible input threshold logic with wide hysteresis. The threshold voltage levels are low voltage and independent of the VDD supply voltage, which allows compatibility with both logic-level input signals from microcontrollers as well as higher-voltage input signals from analog controllers. See the Electrical Characteristics section for the actual input threshold voltage levels and hysteresis specifications of the device.

### 9.2.2.2 V<sub>DD</sub> Bias Supply Voltage

The bias supply voltage to be applied to the VDD pin of the device should never exceed the values listed in the Electrical Characteristics table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the VDD bias supply equals the voltage differential. With a wide operating range from 8 V to 17 V, the device can be used to drive a variety of power switches, such as Si MOSFETs, IGBTs, and wide-bandgap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

### 9.2.2.3 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff should be as fast as possible in order to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds with the targeted power MOSFET. The system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as  $dV_{DS}/dt$ ). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned-on with a  $dV_{DS}/dt$  of 20 V/ns or higher with a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to  $V_{DS(on)}$  in on state) must be completed in approximately 20 ns or less. When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET ( $Q_{GD}$  parameter in the SPP20N60C3 data sheet is 33 nC typical) is supplied by the peak current of gate driver. According to power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET,  $V_{GS(TH)}$ .

To achieve the targeted  $dV_{DS}/dt$ , the gate driver must be capable of providing the  $Q_{GD}$  charge in 20 ns or less. In other words a peak current of 1.65 A ( $= 33 \text{ nC} / 20 \text{ ns}$ ) or higher must be provided by the gate driver. The UCC27301A-Q1 gate driver is capable of providing 3.7-A peak sourcing current which clearly exceeds the design requirement and has the capability to meet the switching speed needed. The 2.4× overdrive capability provides an extra margin against part-to-part variations in the  $Q_{GD}$  parameter of the power MOSFET along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the  $dI/dt$  of the output current pulse of the gate driver. In order to illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle ( $\frac{1}{2} \times I_{PEAK} \times \text{time}$ ) would equal the total gate charge of the power MOSFET ( $Q_G$  parameter in SPP20N60C3 power MOSFET datasheet = 87 nC typical). If the parasitic trace inductance limits the  $dI/dt$  then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the  $Q_G$  required for the power MOSFET switching. In other words the time parameter in the equation would dominate and the  $I_{PEAK}$  value of the current pulse would be much less than the true peak current capability of the device, while the required  $Q_G$  is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

### 9.2.2.4 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used and the acceptable level of pulse distortion to the system. The UCC27301A-Q1 device features 16-ns and 20-ns (typical) propagation delays, which ensures very little pulse distortion and allows operation at very high-frequencies. See the Switching Characteristics table for the propagation and switching characteristics of the device.

### 9.2.2.5 Power Dissipation

Power dissipation of the gate driver has two portions as shown in 式 1.

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

Use 式 2 to calculate the DC portion of the power dissipation (PDC).

$$P_{DC} = I_Q \times V_{DD} \quad (2)$$

where

- $I_Q$  is the quiescent current for the driver.

The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through, and so forth). The UCC27301A-Q1 features very low quiescent currents and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the PDC on the total power dissipation within the gate driver can be safely assumed to be negligible. The power dissipated in the gate-driver package during switching (PSW) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage  $V_G$ , which is very close to input bias supply voltage  $V_{DD}$ )
- Switching frequency
- Use of external gate resistors. When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by 式 3.

$$E_G = \frac{1}{2} C_{LOAD} \times V_{DD}^2 \quad (3)$$

- where
- $C_{LOAD}$  is load capacitor
- $V_{DD}$  is bias voltage feeding the driver

There is an equal amount of energy dissipated when the capacitor is charged and when it is discharged. This leads to a total power loss given by 式 4.

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} \quad (4)$$

where

- $f_{SW}$  is the switching frequency

The switching load presented by a power MOSFET/IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge  $Q_G$ , determine the power that must be dissipated when switching a capacitor which is calculated using the equation  $Q_G = C_{LOAD} \times V_{DD}$  to provide 式 5 for power.

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} = Q_G \times V_{DD} \times f_{SW} \quad (5)$$

This power  $P_G$  is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on and off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor.

## 10 Power Supply Recommendations

The bias supply voltage range for which the device is recommended to operate is from 8 V to 17 V. The lower end of this range is governed by the internal undervoltage-lockout (UVLO) protection feature on the  $V_{DD}$  pin supply circuit blocks. Whenever the driver is in UVLO condition when the  $V_{DD}$  pin voltage is below the  $V_{(ON)}$  supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the  $V_{DD}$  pin of the device (which is a stress rating). Keeping a 3-V margin to allow for transient voltage spikes, the maximum recommended voltage for the  $V_{DD}$  pin is 17 V. The UVLO protection feature also involves a hysteresis function, which means that when the  $V_{DD}$  pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification  $V_{DD(hys)}$ . Therefore, ensuring that, while operating at or near the 8-V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the  $V_{DD}$  pin voltage has dropped below the  $V_{(OFF)}$  threshold, which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up the device does not begin operation until the  $V_{DD}$  pin voltage has exceeded the  $V_{(ON)}$  threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the  $V_{DD}$  pin. Although this fact is well known, it is important to recognize that the charge for source current pulses delivered by the HO pin is also supplied through the same  $V_{DD}$  pin. As a result, every time a current is sourced out of the HO pin, a corresponding current pulse is delivered into the device through the  $V_{DD}$  pin. Thus, ensure that a local bypass capacitor is provided between the  $V_{DD}$  and GND pins and located as close to the device as possible for the purpose of decoupling is important. A low-ESR, ceramic surface-mount capacitor is required. TI recommends using a capacitor in the range 0.22  $\mu$ F to 4.7  $\mu$ F between  $V_{DD}$  and GND. In a similar manner, the current pulses delivered by the LO pin are sourced from the HB pin. Therefore a 0.022- $\mu$ F to 0.1- $\mu$ F local decoupling capacitor is recommended between the HB and HS pins.

## 11 Layout

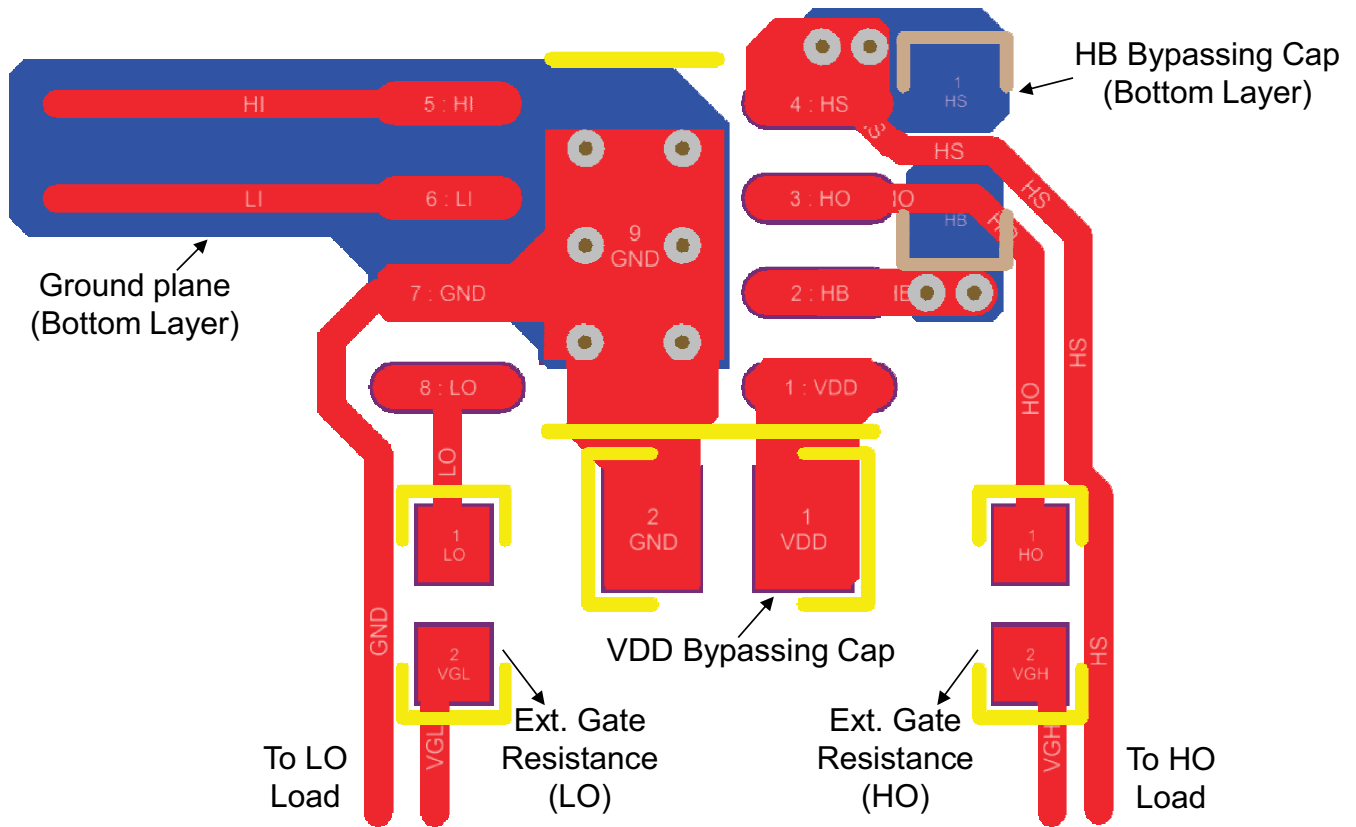
### 11.1 Layout Guidelines

To improve the switching characteristics and efficiency of a design, the following layout rules must be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the  $V_{DD} - V_{SS}$  and  $V_{HB} - V_{HS}$  (bootstrap) capacitors as close as possible to the device.
- Pay close attention to the GND trace. Use the thermal pad of the DRM package as GND by connecting it to the VSS pin (GND). The GND trace from the driver goes directly to the source of the MOSFET, but must not be in the high current path of the MOSFET drain or source current.
- Use similar rules for the HS node as for GND for the high-side driver.
- For systems using multiple UCC27301A-Q1 devices, TI recommends that dedicated decoupling capacitors be located at  $V_{DD} - V_{SS}$  for each device.
- Care must be taken to avoid placing VDD traces close to LO, HS, and HO signals.
- Use wide traces for LO and HO closely following the associated GND or HS traces. A width of 60 to 100 mils is preferable where possible.
- Use as least two or more vias if the driver outputs or SW node must be routed from one layer to another. For GND, the number of vias must be a consideration of the thermal pad requirements as well as parasitic inductance.
- Avoid LI and HI (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high impedance leads.

A poor layout can cause a significant drop in efficiency or system malfunction, and it can even lead to decreased reliability of the whole system.

## 11.2 Layout Example



11-1. UCC27301A-Q1 PCB Layout Example for SOIC package

ADVANCE INFORMATION

ADVANCE INFORMATION

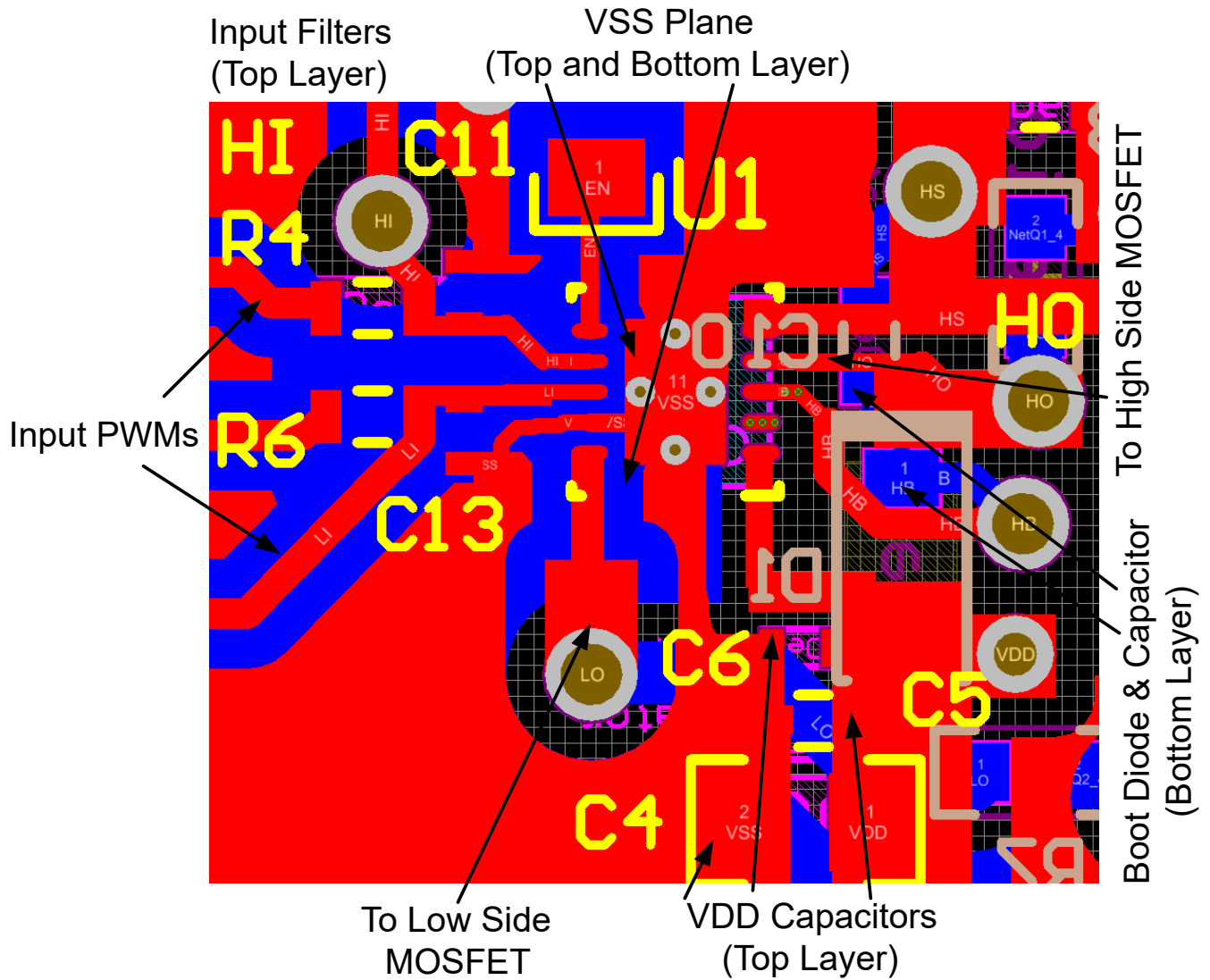


FIG 11-2. UCC27301A-Q1 PCB Layout Example for VSON package

### 11.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive-power requirements of the load and the thermal characteristics of the package. For a gate driver to be useful over a particular temperature range, the package must allow for efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package are listed in Thermal Information section. For detailed information regarding the table, refer to the Application Note from Texas Instruments entitled *Semiconductor and IC Package Thermal Metrics* (SPRA953). The UCC27301A-Q1 device is offered in a 10-pin VSON package (DRC).

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 サード・パーティ製品に関する免責事項

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### 12.2 Documentation Support

#### 12.2.1 Related Documentation

PowerPAD™ *Thermally Enhanced Package*, Application Report (SLMA002)

PowerPAD™ *Made Easy*, Application Report (SLMA004)

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 12.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 13.1 Package Option Addendum

**Packaging Information**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish <sup>(6)</sup>	MSL Peak Temp <sup>(3)</sup>	Op Temp (°C)	Device Marking <sup>(4) (5)</sup>
PUCC27301AQ DDARQ1	PREVIEW	SO	DDA	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	
PUCC27301AQ DRCRQ1	PREVIEW	VSON	DRC	10	3000	RoHS & Green	NIPDAU		-40 to 125	

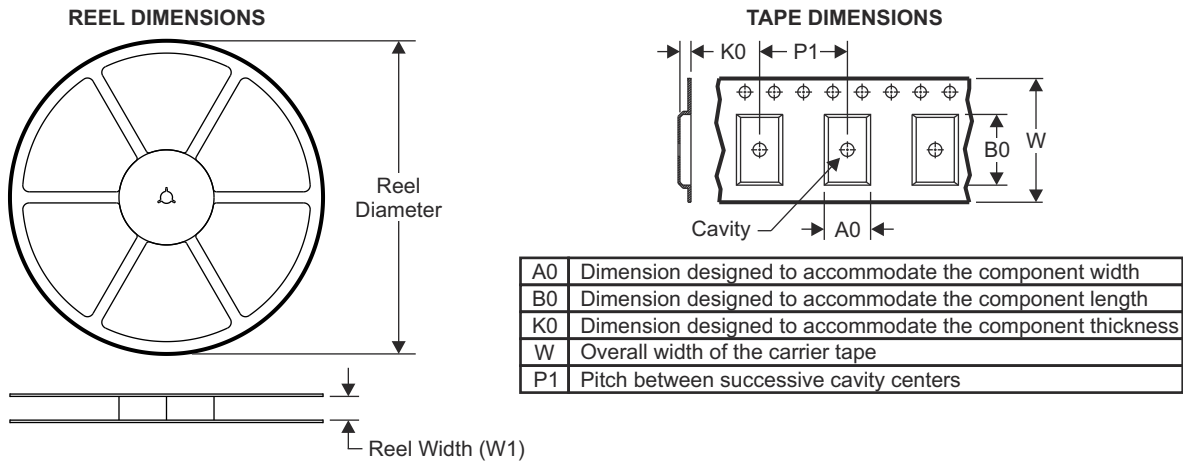
- (1) The marketing status values are defined as follows:  
**ACTIVE:** Product device recommended for new designs.  
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.  
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.  
**PRE\_PROD** Unannounced device, not in production, not available for mass market, nor on the web, samples not available.  
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.  
**OBSOLETE:** TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check [www.ti.com/productcontent](http://www.ti.com/productcontent) for the latest availability information and additional product content details.  
**TBD:** The Pb-Free/Green conversion plan has not been defined.  
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.  
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.  
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

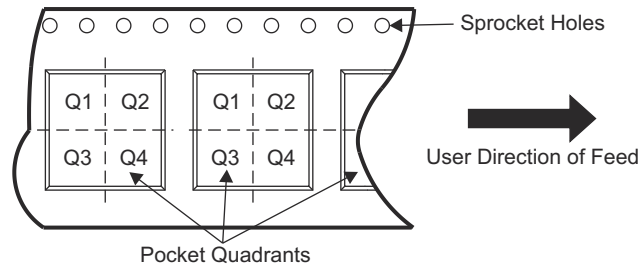
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



### 13.2 Tape and Reel Information



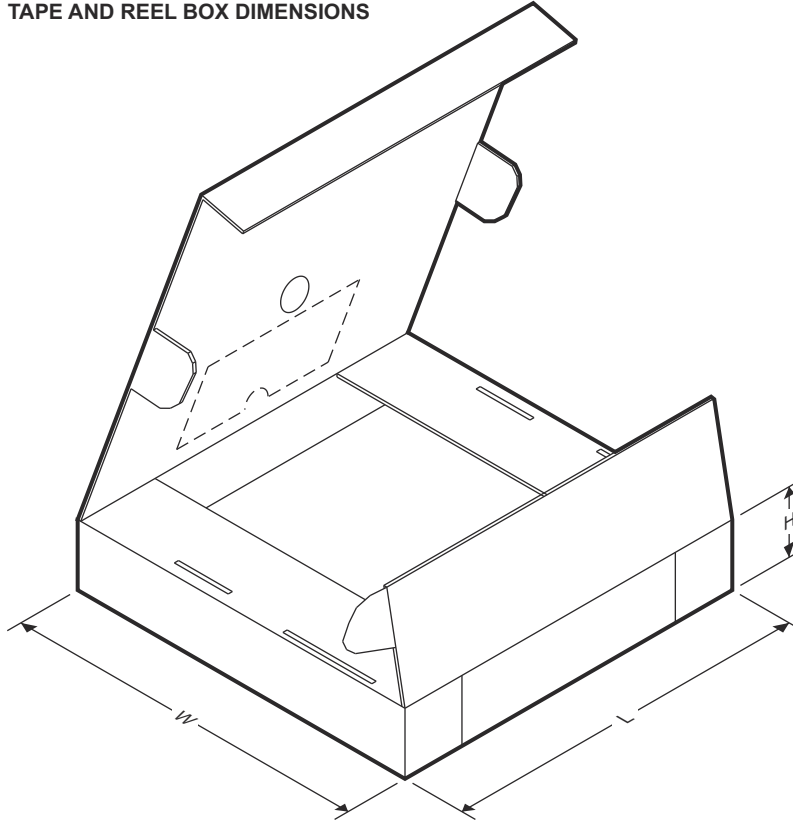
#### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PUCC27301AQDDARQ1	SO	DDA	8	3000	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
PUCC27301AQDRCRQ1	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

ADVANCE INFORMATION


**TAPE AND REEL BOX DIMENSIONS**

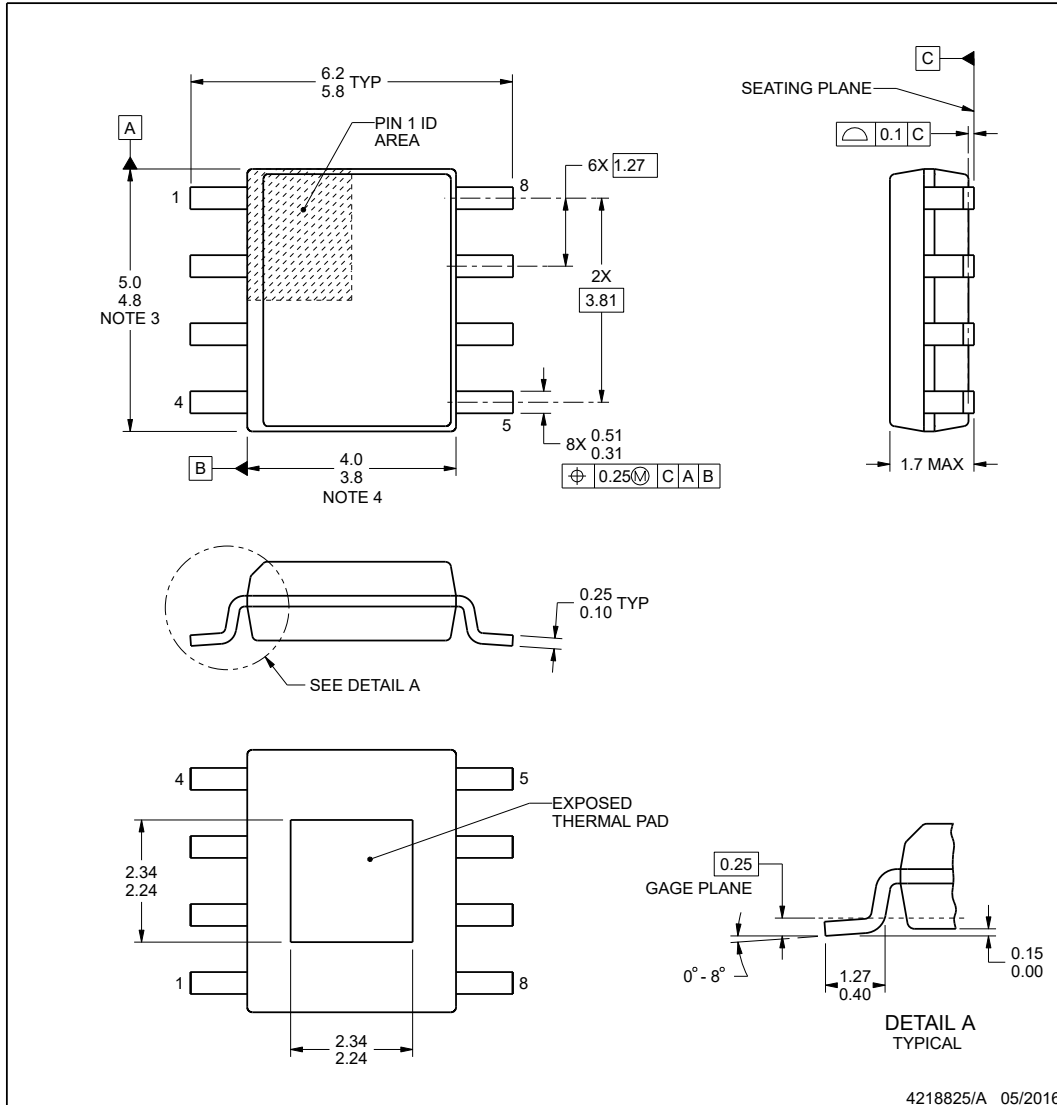


Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PUCC27301AQDDARQ1	SO	DDA	8	3000	340.5	336.1	25
PUCC27301AQDRCRQ1	VSON	DRC	10	3000	367.0	367.0	35

ADVANCE INFORMATION

### 13.3 Mechanical Data

**DDA0008A**

**PACKAGE OUTLINE**  
**PowerPAD™ SOIC - 1.7 mm max height**  
 PLASTIC SMALL OUTLINE



4218825/A 05/2016  
 PowerPAD is a trademark of Texas Instruments.

**NOTES:**

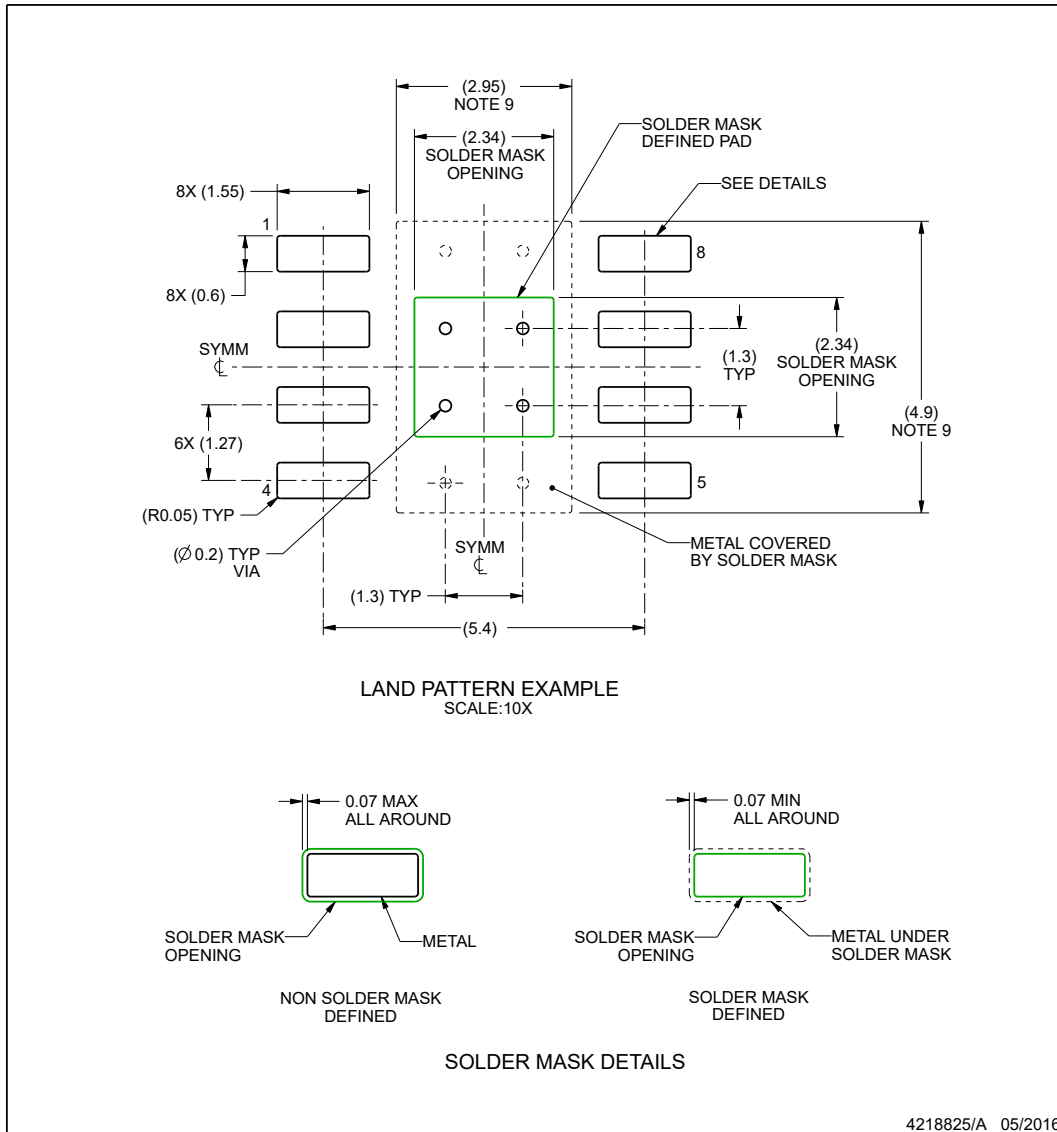
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.

**EXAMPLE BOARD LAYOUT**

**DDA0008A**

**PowerPAD™ SOIC - 1.7 mm max height**

PLASTIC SMALL OUTLINE



NOTES: (continued)

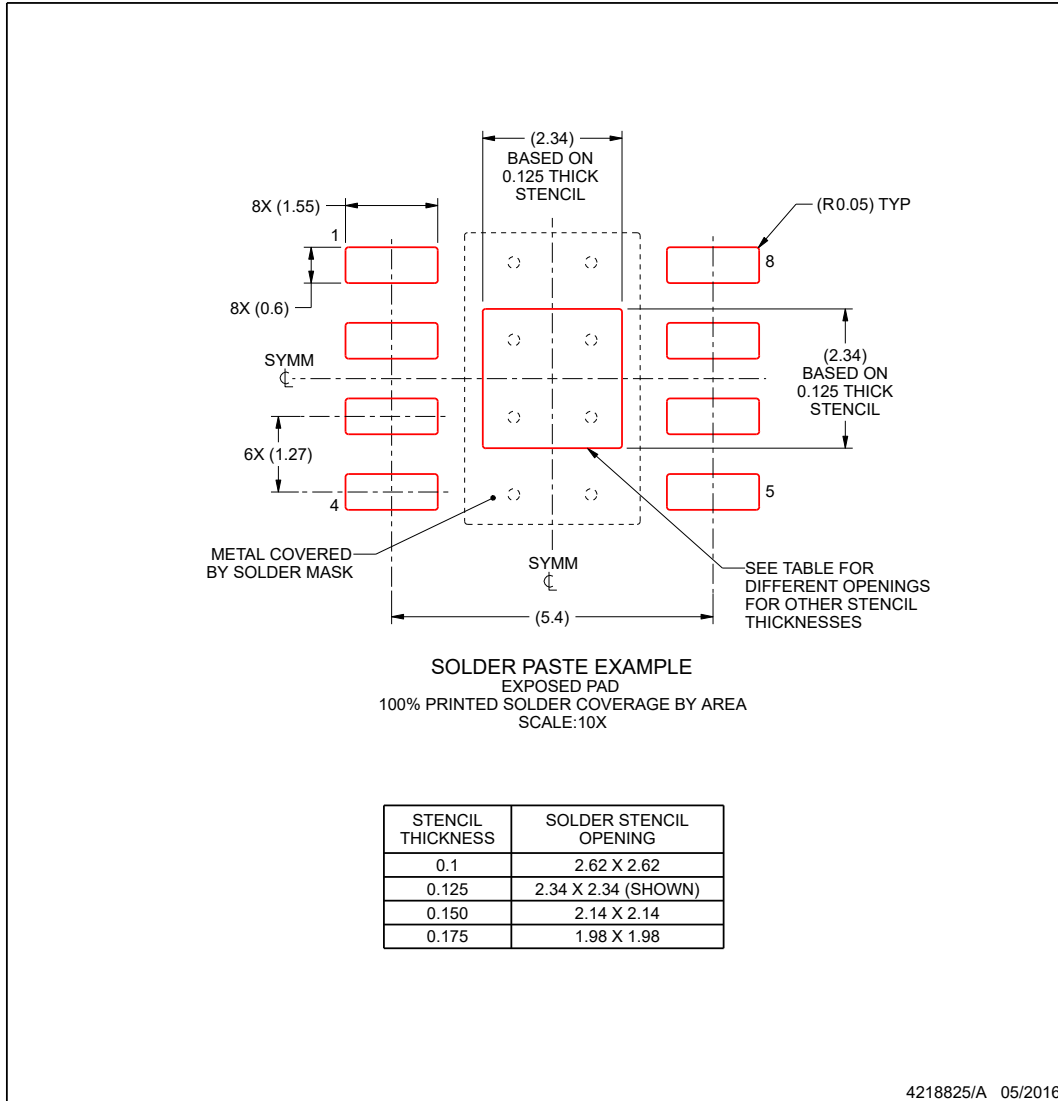
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**EXAMPLE STENCIL DESIGN**

**DDA0008A**

**PowerPAD™ SOIC - 1.7 mm max height**

PLASTIC SMALL OUTLINE



NOTES: (continued)

- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.

**ADVANCE INFORMATION**



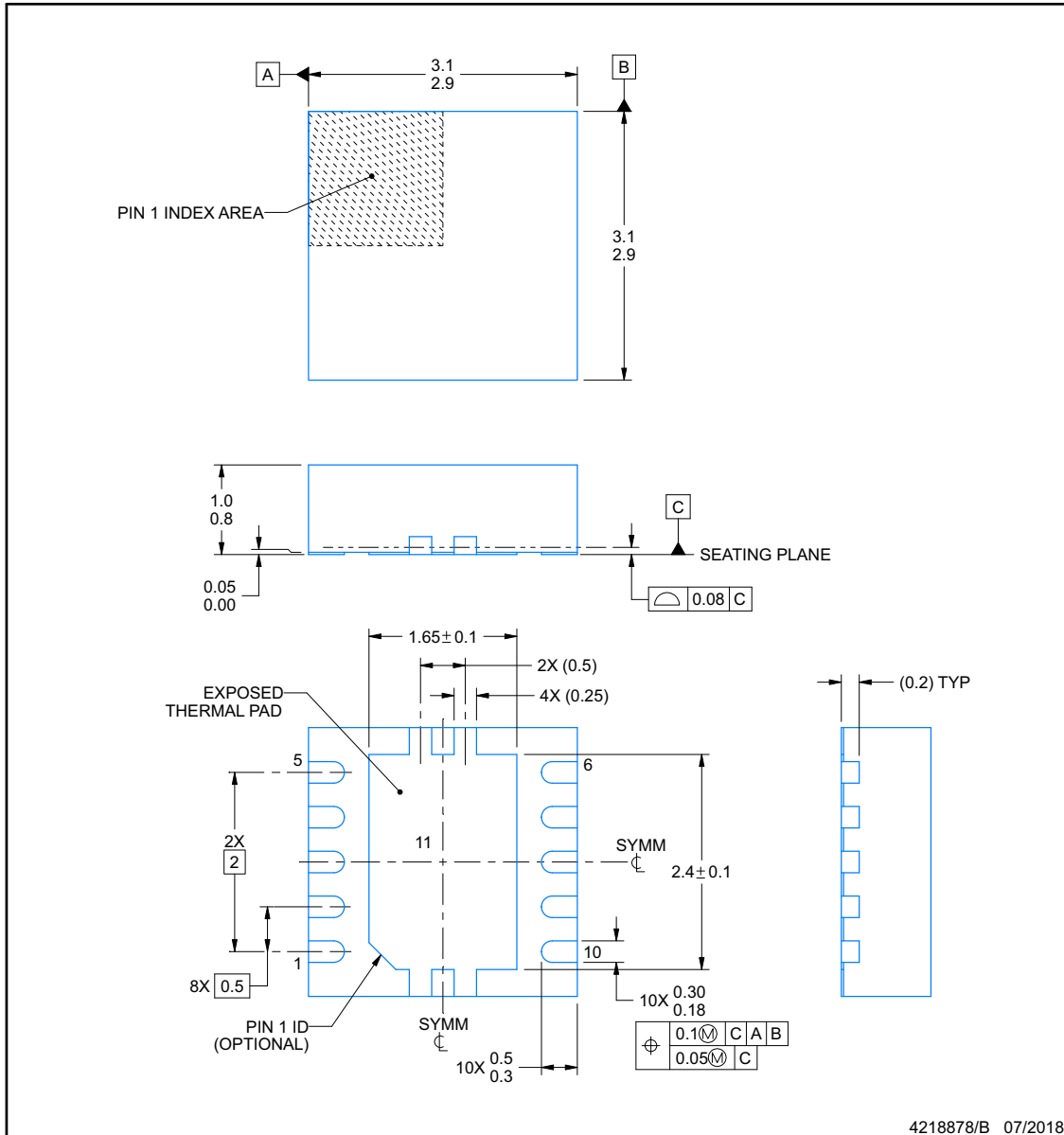
**PACKAGE OUTLINE**

**DRC0010J**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD

**ADVANCE INFORMATION**



**NOTES:**

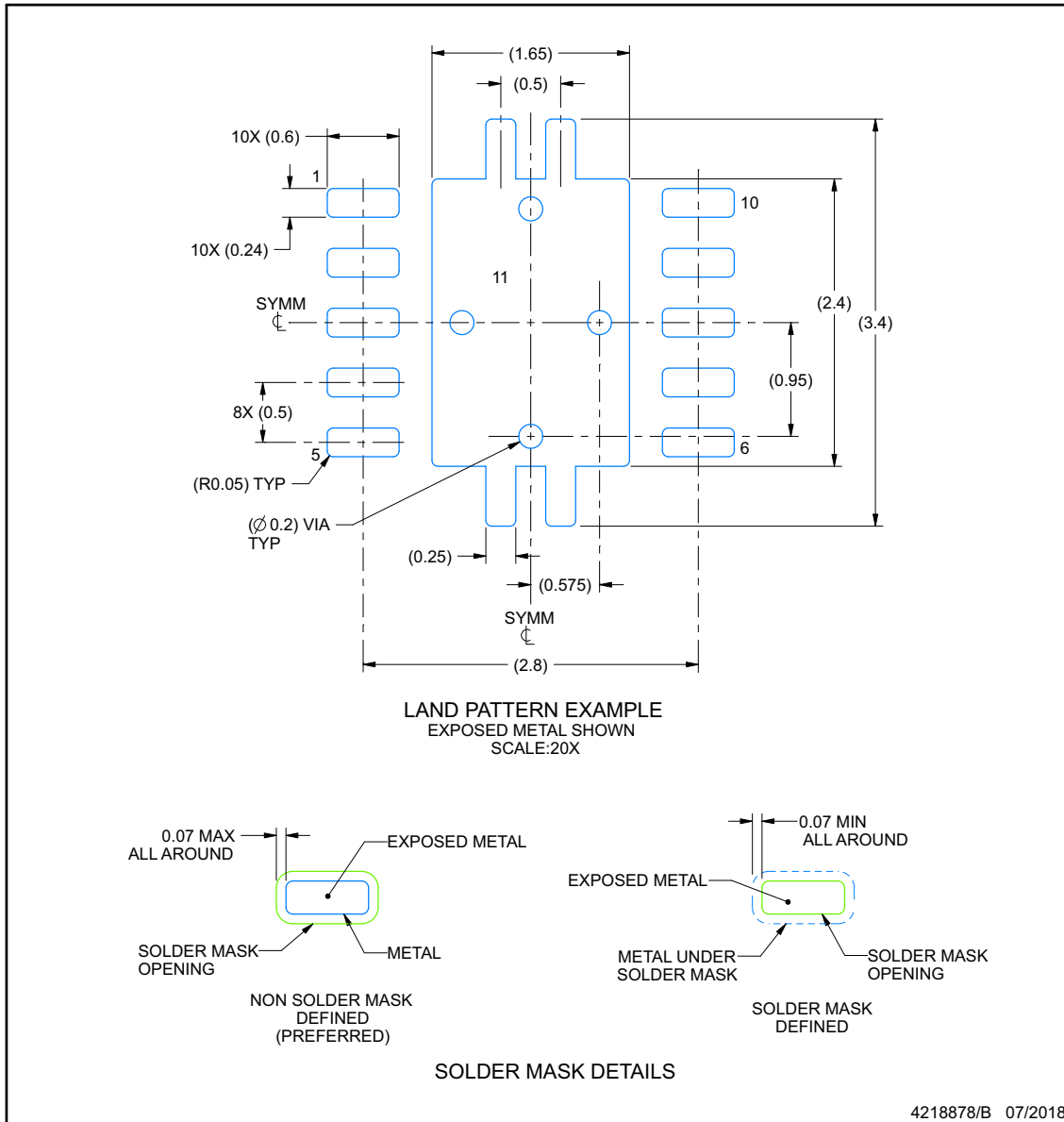
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

**DRC0010J**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

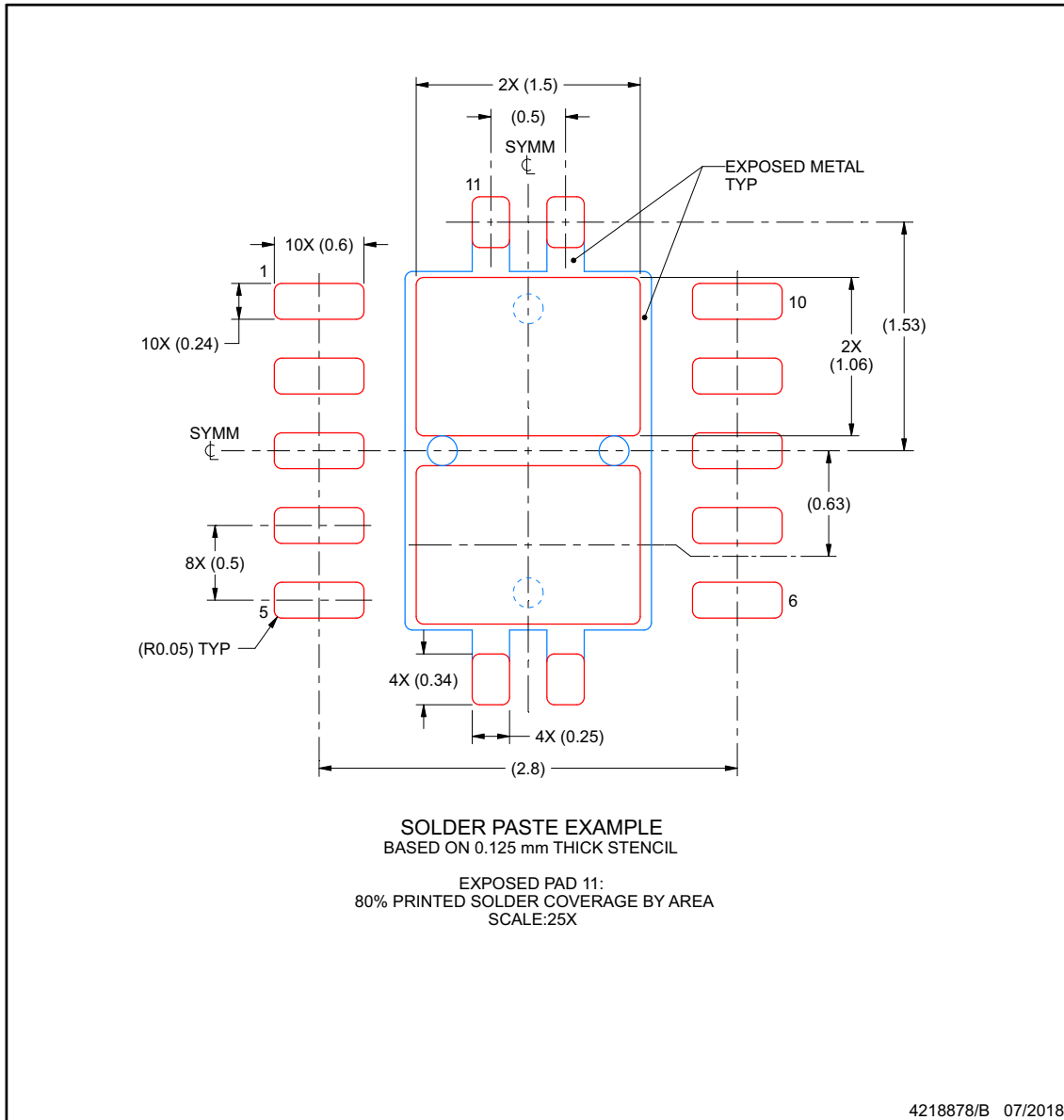
**EXAMPLE STENCIL DESIGN**

**DRC0010J**

**VSON - 1 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD

ADVANCE INFORMATION



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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