

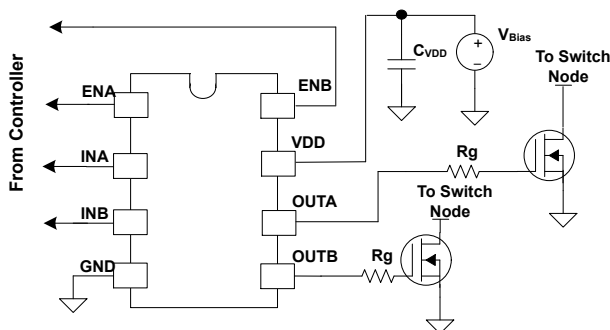
# UCC27444-Q1 20V、4A デュアルチャネル、ローサイド・ゲート・ドライバ、-5V 入力機能付き、車載用アプリケーション向け

## 1 特長

- 車載アプリケーション向けに認定済み
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1: -40°C ~ +125°C の動作時 周囲温度範囲
  - デバイス HBM ESD 分類レベル H2
  - デバイス CDM ESD 分類レベル C6
- 各チャネルの 4A (代表値) ピーク・ソースおよびシンク 駆動電流
- -5V まで扱える INA および INB 入力ピン
- 絶対最大 VDD 電圧: 20V
- 広い VDD 動作範囲: 4.5V ~ 18V
- 2 つの独立したゲート駆動チャネル
- 出力ごとに独立したイネーブル機能
- 高速伝搬遅延時間: 18ns (代表値)
- 高速立ち上がり / 立ち下がり時間: 11ns/7ns (代表値)
- 2 チャネル間遅延マッチング: 1ns (代表値)
- SOIC8 および VSSOP8 PowerPAD™ パッケージ・オプション
- 動作時の接合部温度範囲: -40°C ~ 125°C

## 2 アプリケーション

- **スイッチ・モード電源 (SMPS)**
- **力率改善 (PFC) 回路**
- **DC/DC コンバータ**
- **AC インバータと VF ドライブ**
- **マイクロ・インバータ**
- **DC 高速充電ステーション**



アプリケーション概略図

## 3 概要

UCC27444-Q1 は、MOSFET および GaN パワー・スイッチを効率的に駆動するデュアルチャネル高速ローサイド・ゲート・ドライバです。UCC27444-Q1 は 4A (代表値) のピーク駆動能力を持っています。これにより、パワー・スイッチの立ち上がり / 立ち下がり時間を短縮し、スイッチング損失を低減し、効率を向上させます。本デバイスの高速伝搬遅延 (代表値 18ns) は、システムのデッドタイム最適化、パルス幅利用率、制御ループ応答、過渡性能を改善させることで出力段の効率を向上させます。

UCC27444-Q1 は、INx 入力で -5V を扱えるため、中程度のグラウンド・バウンスが発生するシステムの堅牢性を向上させることができます。入力をほとんどのコントローラ出力に接続できるため、制御の柔軟性を最大限に高めることができます。独立したイネーブル信号を使うと、メイン制御ロジックとは無関係に電力段を制御できます。システム障害が発生した場合、イネーブル・ローにすることで、ゲート・ドライバを迅速にシャットオフできます。多くの高周波スイッチング電源では、電源デバイスのゲートにノイズを生じさせます。このノイズがゲート・ドライバの出力ピンに注入され、ドライバを誤動作させる可能性があります。本デバイスは、過渡逆電流と逆電圧への対応能力があるため、電源デバイスやパルス変圧器のゲートのノイズが許容され、ドライバの誤動作を防止できます。

UCC27444-Q1 は、低電圧動作とパワーオン・リセット (POR) 機能も搭載しており、システムの堅牢性が向上します。パワー・デバイスの動作に十分なバイアス電圧がない場合は、強力な内部プルダウン MOSFET によってゲート・ドライバの出力が LOW に保持されます。

### 製品情報

部品番号 <sup>(1)</sup>	パッケージ	本体サイズ (公称)
UCC27444-Q1	SOIC (8)	4.90mm × 3.91mm
	VSSOP (8)	3.00mm × 3.00mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



## Table of Contents

<b>1 特長</b> .....	1	7.4 Device Functional Modes.....	15
<b>2 アプリケーション</b> .....	1	<b>8 Application and Implementation</b> .....	16
<b>3 概要</b> .....	1	8.1 Application Information.....	16
<b>4 Revision History</b> .....	2	8.2 Typical Application.....	17
<b>5 Pin Configuration and Functions</b> .....	3	<b>9 Power Supply Recommendations</b> .....	21
<b>6 Specifications</b> .....	4	<b>10 Layout</b> .....	22
6.1 Absolute Maximum Ratings.....	4	10.1 Layout Guidelines.....	22
6.2 ESD Ratings.....	4	10.2 Layout Example.....	23
6.3 Recommended Operating Conditions.....	4	10.3 Thermal Considerations.....	23
6.4 Thermal Information.....	4	<b>11 Device and Documentation Support</b> .....	24
6.5 Electrical Characteristics.....	5	11.1 サード・パーティ製品に関する免責事項.....	24
6.6 Switching Characteristics.....	6	11.2 ドキュメントの更新通知を受け取る方法.....	24
6.7 Timing Diagrams.....	7	11.3 サポート・リソース.....	24
6.8 Typical Characteristics.....	8	11.4 Trademarks.....	24
<b>7 Detailed Description</b> .....	12	11.5 静電気放電に関する注意事項.....	24
7.1 Overview.....	12	11.6 用語集.....	24
7.2 Functional Block Diagram.....	13	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	24
7.3 Feature Description.....	13		

## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### Changes from Revision \* (May 2022) to Revision A (July 2023)

Page

• ステータスを「事前情報」から「量産データ」に変更.....	1
---------------------------------	---

## 5 Pin Configuration and Functions

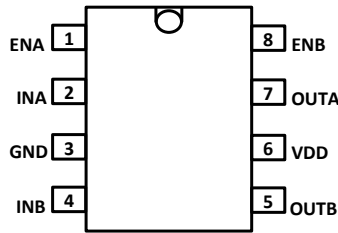


图 5-1. D Package 8-Pin SOIC Top View

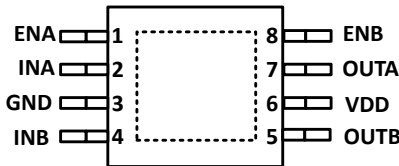


图 5-2. DGN Package 8-Pin VSSOP Top View

表 5-1. Pin Functions

NAME	PIN		TYPE <sup>(1)</sup>	DESCRIPTION
	DGN	D		
ENA	1	1	I	Enable input for Channel A. Biasing ENA, LOW will disable Channel A output regardless of the state of INA. Pulling ENA, HIGH enables the Channel A output. If ENA is left floating, Channel A is enabled by default due to an internal pullup resistor. It is recommended to connect this pin to VDD if unused.
ENB	8	8	I	Enable input for Channel B. Biasing ENB, LOW disables Channel B output regardless of the state of INB. Pulling ENB, HIGH enables the Channel B output. If ENB is left floating, Channel B is enabled by default due to an internal pullup resistor. It is recommended to connect this pin to VDD if unused.
GND	3	3	—	Ground: All signals are referenced to this pin.
INA	2	2	I	Input to Channel A. INA is the non-inverting input of the UCC27444-Q1 device. Connect this pin to GND if unused.
INB	4	4	I	Input to Channel B. INB is the non-inverting input of the UCC27444-Q1 device. Connect this pin to GND if unused.
OUTA	7	7	O	Channel A Output
OUTB	5	5	O	Channel B Output
VDD	6	6	I	Bias supply input. Bypass this pin with two ceramic capacitors, generally $\geq 1 \mu\text{F}$ and $0.1 \mu\text{F}$ , which are referenced to GND pin of this device.
	Thermal Pad	—	—	Connect to GND through large copper plane. This pad is not a low-impedance path to GND.

(1) I = Input; O = Output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2) (3)</sup>

		MIN	MAX	UNIT
Supply voltage, VDD		-0.3	20	V
Output Voltage, OUTA, OUTB	DC	-0.3	VDD +0.3	V
	100ns Pulse	-2	VDD +0.3	V
Input Voltage INA, INB,		-5	VDD+0.3	V
Input Voltage ENA, ENB		-0.3	VDD+0.3	V
Operating junction temperature, T <sub>J</sub>		-40	150	°C
Lead temperature	Soldering, 10 sec.		300	°C
	Reflow		260	
Storage temperature, T <sub>stg</sub>		-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See [セクション 6.4](#) of the datasheet for thermal limitations and considerations of packages.
- (3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD classification level H2	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD classification level C6	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range. All voltages are with reference to GND (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, VDD		4.5	12	18	V
Input voltage, INA, INB		-2		VDD	V
Output Voltage, OUTA, OUTB		0		VDD	V
Operating junction temperature, T <sub>J</sub>		-40		125	°C

### 6.4 Thermal Information

THERMAL METRIC		UCC27444-Q1		UNIT
		DGN	D	
		8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	57.3	131.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	82.0	73.4	
R <sub>θJB</sub>	Junction-to-board thermal resistance	30.5	74.6	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	5.0	25.6	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	30.4	73.8	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	13.1	n/a	

## 6.5 Electrical Characteristics

Unless otherwise noted, VDD = 4.5 V to 18 V, T<sub>A</sub> = T<sub>J</sub> = –40°C to 125°C, 1-μF capacitor from VDD to GND, no load on the output. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>BIAS CURRENTS</b>						
I <sub>VDD</sub>	VDD static supply current	V <sub>INx</sub> = 3.3 V, ENx = VDD		150	380	μA
I <sub>VDD</sub>	VDD static supply current	V <sub>INx</sub> = 0 V, ENx = VDD		107	180	μA
I <sub>VDDO</sub>	VDD operating current	C <sub>LOAD</sub> = 1.8 nF, f <sub>SW</sub> = 1000 kHz, ENx = VDD, V <sub>INx</sub> = 0 V – 3.3 V PWM		39	45	mA
I <sub>DIS</sub>	VDD disable current	V <sub>INx</sub> = 3.3 V, ENx = 0 V		450	570	μA
<b>POWER ON RESET (POR)</b>						
V <sub>VDD_ON</sub>	VDD POR rising threshold		2.1	3.0	4.0	V
V <sub>VDD_OFF</sub>	VDD POR falling threshold		1.8	2.7	3.5	V
V <sub>VDD_HYS</sub>	VDD POR hysteresis			0.3		V
<b>INPUT (INA, INB)</b>						
V <sub>INx_H</sub>	Input signal high threshold	Output High, ENx = HIGH	1.6	2.2	2.5	V
V <sub>INx_L</sub>	Input signal low threshold	Output Low, ENx = HIGH	0.8	1.2	1.5	V
V <sub>INx_HYS</sub>	Input signal hysteresis			1		V
<b>ENABLE (ENA, ENB)</b>						
V <sub>ENx_H</sub>	Enable signal high threshold	Output High, INx = HIGH	1.7	2.3	2.7	V
V <sub>ENx_L</sub>	Enable signal low threshold	Output Low, INx = HIGH	1.1	1.8	2.2	V
V <sub>ENx_HYS</sub>	Enable signal hysteresis			0.7		V
R <sub>ENx</sub>	EN pin pullup resistance	ENx = 0 V		100		kΩ
<b>OUTPUTS (OUTA, OUTB)</b>						
I <sub>SRC</sub> <sup>(1)</sup>	Peak output source current	VDD = 14 V, C <sub>VDD</sub> = 10 μF, C <sub>L</sub> = 0.1 μF, f = 1 kHz		4		A
I <sub>SNK</sub> <sup>(1)</sup>	Peak output sink current	VDD = 14 V, C <sub>VDD</sub> = 10 μF, C <sub>L</sub> = 0.1 μF, f = 1 kHz		–4		A
R <sub>OH</sub> <sup>(2)</sup>	Pullup resistance	I <sub>OUT</sub> = –10 mA See <a href="#">セクション 7.3.4</a> .		1.2	2.5	Ω
R <sub>OL</sub>	Pulldown resistance	I <sub>OUT</sub> = 10 mA		0.7	1.2	Ω

(1) Parameter not tested in production.

(2) Output pullup resistance in this table is a DC measurement that measures resistance of PMOS structure only (not N-channel structure).

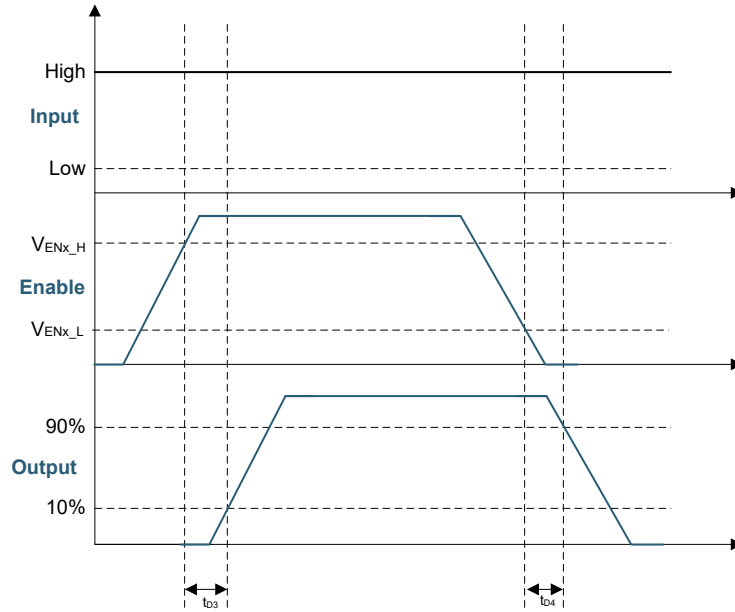
## 6.6 Switching Characteristics

Unless otherwise noted,  $V_{DD} = V_{EN} = 4.5 \text{ V to } 18 \text{ V}$ ,  $T_A = T_J = -40^\circ\text{C to } 125^\circ\text{C}$ , 1- $\mu\text{F}$  capacitor from  $V_{DD}$  to  $GND$ , no load on the output. Typical condition specifications are at  $25^\circ\text{C}$  (1).

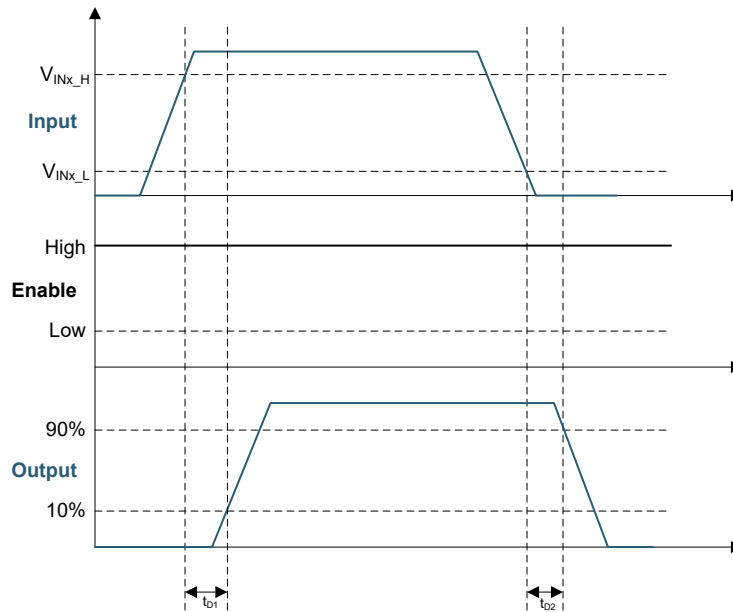
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{Rx}$	Rise time	$C_{LOAD} = 1.8 \text{ nF}$ , 10% to 90%, $V_{in} = 0 \text{ V} - 5 \text{ V}$		11	25	ns
$t_{Fx}$	Fall time	$C_{LOAD} = 1.8 \text{ nF}$ , 90% to 10%, $V_{in} = 0 \text{ V} - 5 \text{ V}$		7	23	ns
$t_{D1x}$	Turn-on propagation delay	$C_{LOAD} = 1.8 \text{ nF}$ , $V_{INx\_H}$ of the input rise to 10% of output rise, $V_{in} = 0 \text{ V} - 5 \text{ V}$ , $F_{sw} = 500 \text{ kHz}$ , 50% duty cycle		18	33	ns
$t_{D2x}$	Turn-off propagation delay	$C_{LOAD} = 1.8 \text{ nF}$ , $V_{INx\_L}$ of the input fall to 90% of output fall, $V_{in} = 0 \text{ V} - 5 \text{ V}$ , $V_{DD} = 5 \text{ V} - 18 \text{ V}$ , $F_{sw} = 500 \text{ kHz}$ , 50% duty cycle		30	50	ns
$t_{D3x}$	Enable propagation delay	$C_{LOAD} = 1.8 \text{ nF}$ , $V_{ENx\_H}$ of the enable rise to 10% of output rise, $V_{in} = 0 \text{ V} - 5 \text{ V}$ , $F_{sw} = 500 \text{ kHz}$ , 50% duty cycle		19	31	ns
$t_{D4x}$	Disable propagation delay	$C_{LOAD} = 1.8 \text{ nF}$ , $V_{ENx\_L}$ of the enable fall to 90% of output fall, $V_{in} = 0 \text{ V} - 5 \text{ V}$ , $F_{sw} = 500 \text{ kHz}$ , 50% duty cycle		24	52	ns
$t_M$	Delay matching between two channels	$C_{LOAD} = 1.8 \text{ nF}$ , $V_{in} = 0 \text{ V} - 5 \text{ V}$ , $F_{sw} = 500 \text{ kHz}$ , 50% duty cycle, $INA = INB$ , $ t_{RA} - t_{RB} $ , $ t_{FA} - t_{FB} $		1	5	ns
$t_{PWmin}$	Minimum input pulse width	$C_L = 1.8 \text{ nF}$ , $V_{in} = 0 \text{ V} - 5 \text{ V}$ , $F_{sw} = 500 \text{ kHz}$ , $V_o > 1.5 \text{ V}$		8	22	ns

(1) Switching parameters are not tested in production.

## 6.7 Timing Diagrams



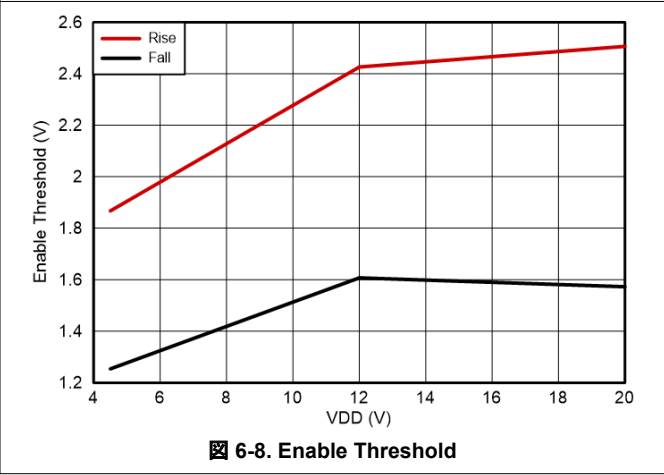
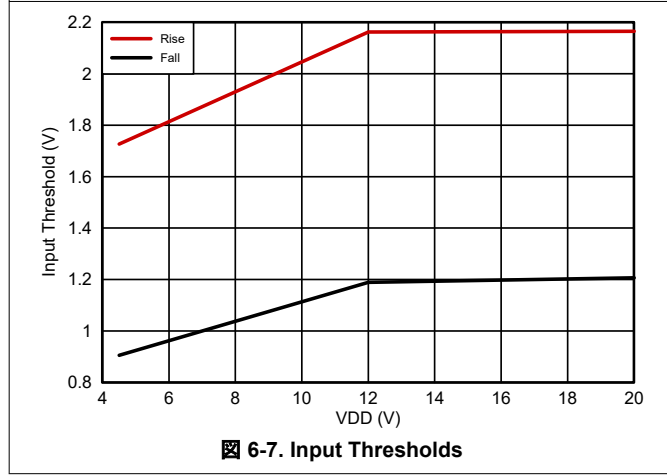
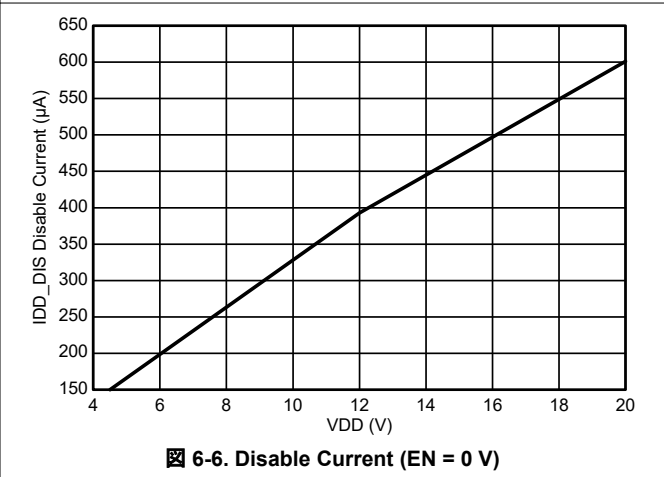
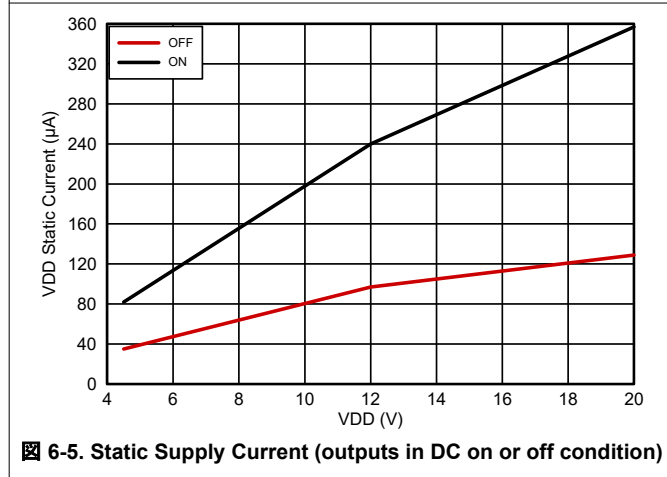
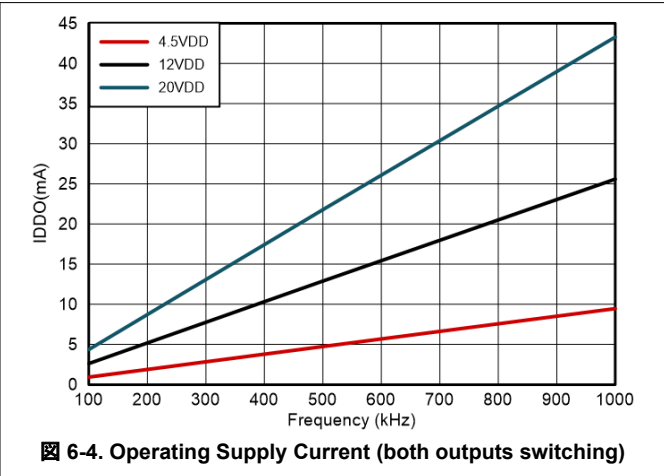
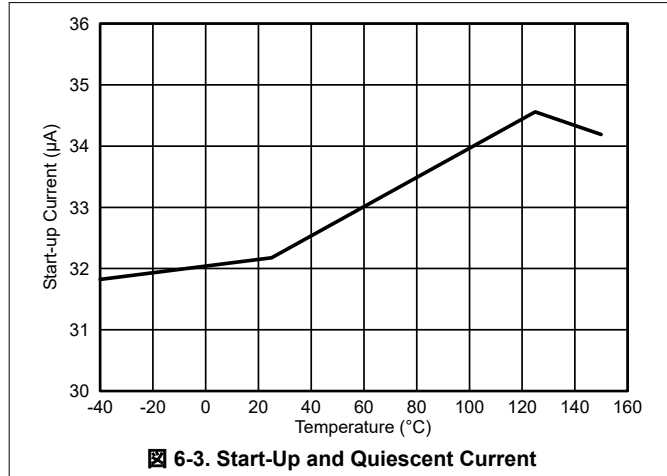
**6-1. Enable Function**



**6-2. Input-Output Operation**

## 6.8 Typical Characteristics

Unless otherwise specified, VDD = 12 V, INx = 3.3 V, ENx = 3.3 V, T<sub>J</sub> = 25°C, no load





## 6.8 Typical Characteristics (continued)

Unless otherwise specified, VDD = 12 V, INx = 3.3 V, ENx = 3.3 V, T<sub>J</sub> = 25°C, no load

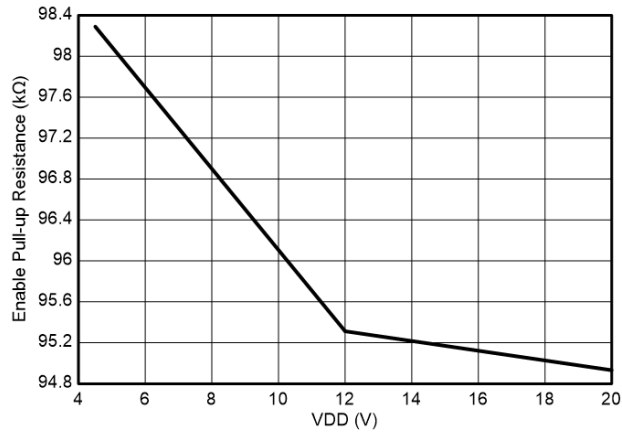


图 6-9. Enable Pullup Resistance

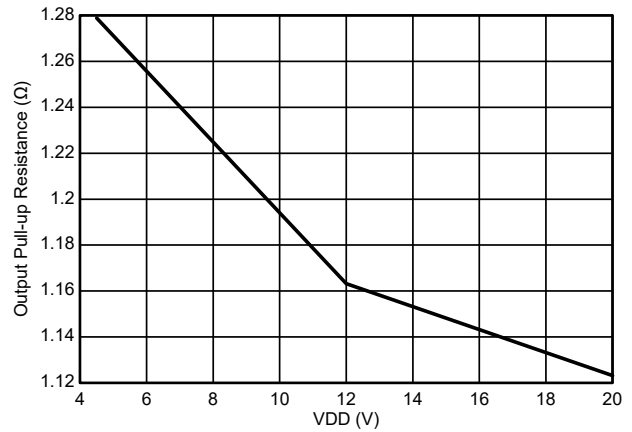


图 6-10. Output Pullup Resistance

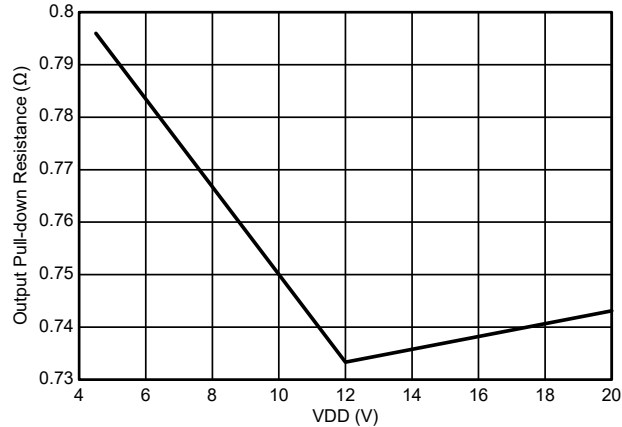


图 6-11. Output Pulldown Resistance

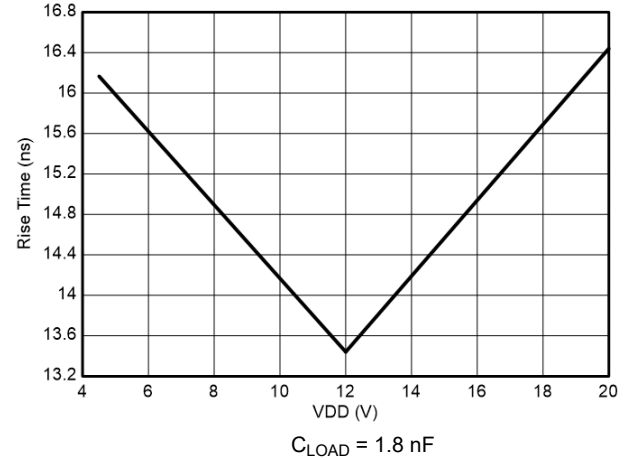


图 6-12. Output Rise Time vs VDD

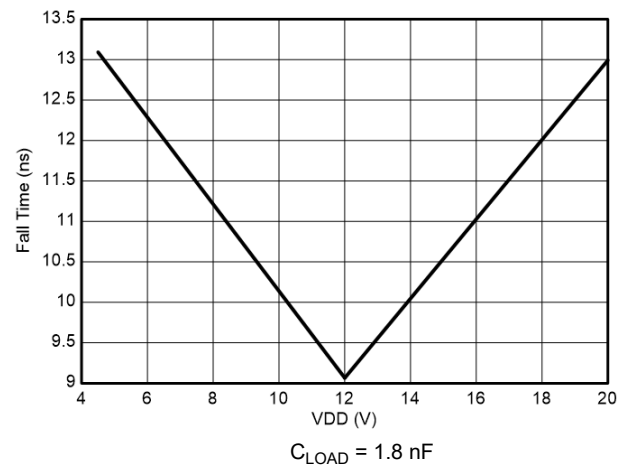


图 6-13. Output Fall Time vs VDD

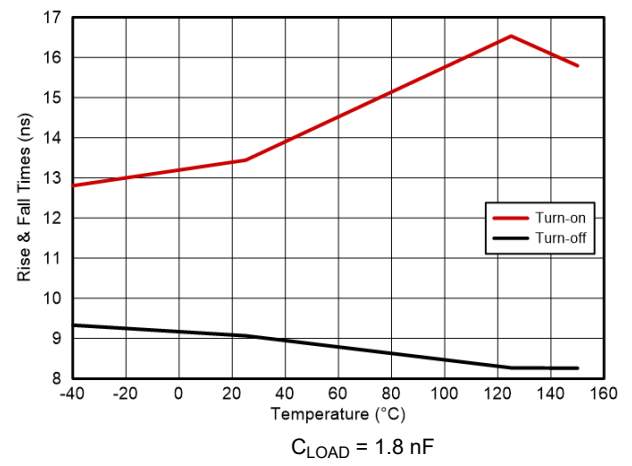


图 6-14. Output Rise and Fall Time vs Temperature

## 6.8 Typical Characteristics (continued)

Unless otherwise specified, VDD = 12 V, INx = 3.3 V, ENx = 3.3 V, T<sub>J</sub> = 25°C, no load

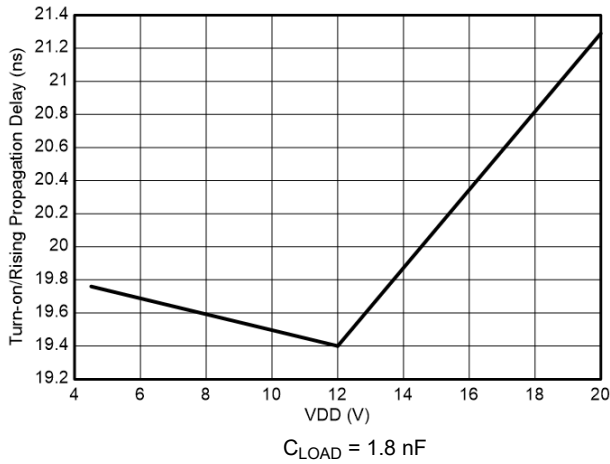


Figure 6-15. Input to Output Rising (turn-on) Propagation Delay vs VDD

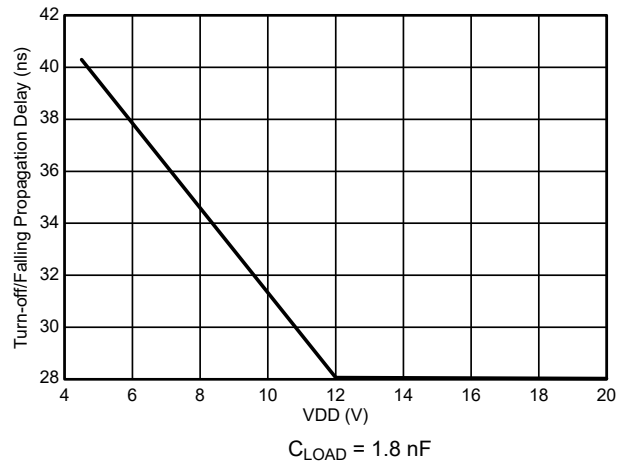


Figure 6-16. Input to Output Falling (turn-off) Propagation Delay vs VDD

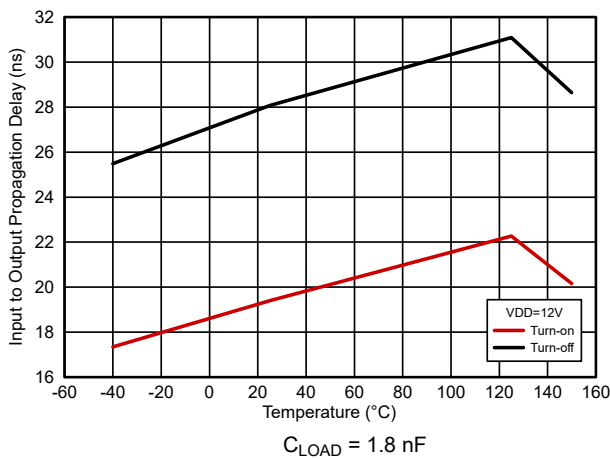


Figure 6-17. Input Propagation Delay vs Temperature

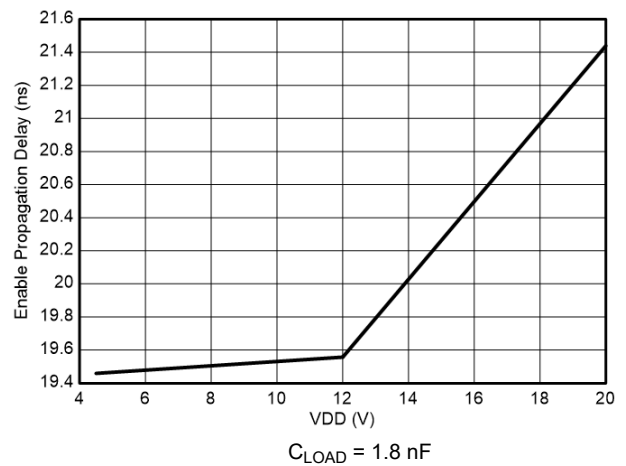


Figure 6-18. Enable to Output Rising Propagation Delay

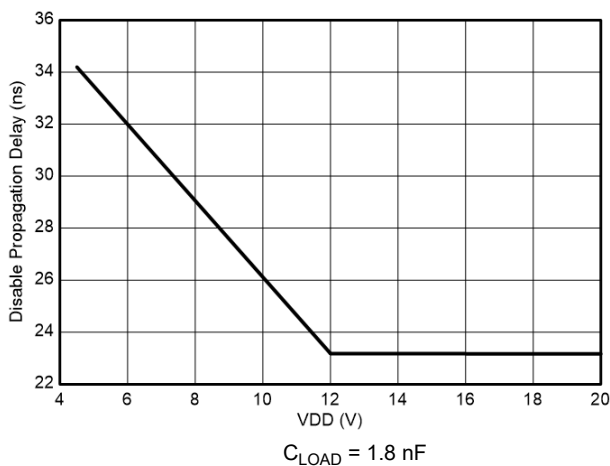


Figure 6-19. Enable to Output Falling Propagation Delay

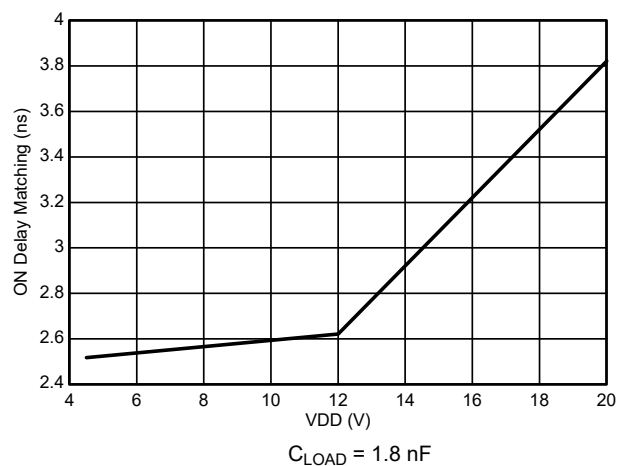


Figure 6-20. Turn-On/Rising Delay Matching

## 6.8 Typical Characteristics (continued)

Unless otherwise specified, VDD = 12 V, INx = 3.3 V, ENx = 3.3 V, T<sub>J</sub> = 25°C, no load

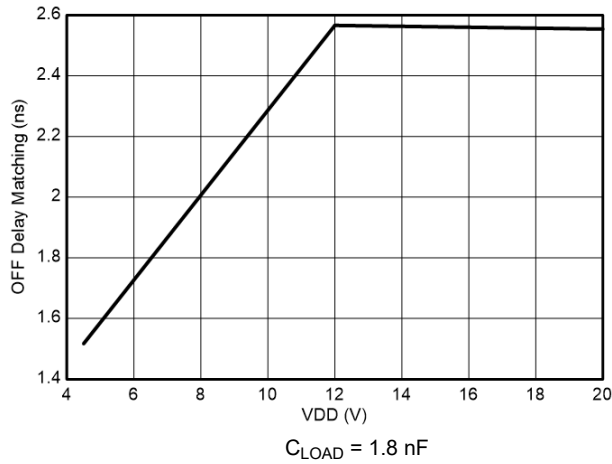


Figure 6-21. Turn-Off and Falling Delay Matching

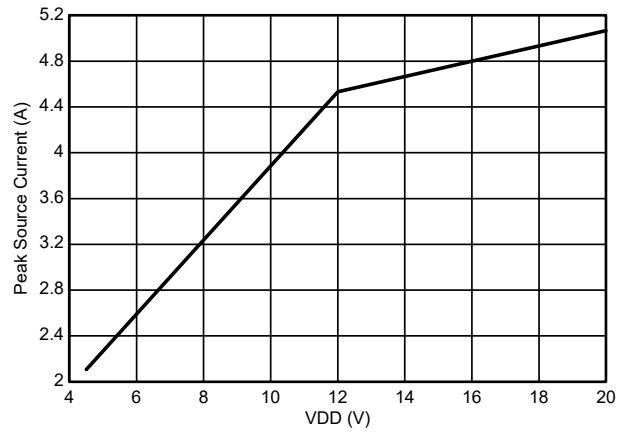


Figure 6-22. Peak Source Current vs VDD

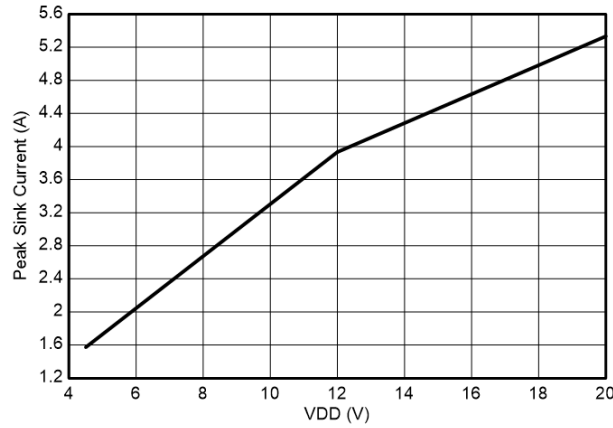


Figure 6-23. Peak Sink Current vs VDD

## 7 Detailed Description

### 7.1 Overview

The UCC27444-Q1 device is the dual-channel, low-side, high-speed, gate driver devices featuring 4-A source and sink current capability, fast switching characteristics, and a host of other features. [UCC27444-Q1 Features and Benefits](#) details the advantages of the gate driver's features, which combine to ensure efficient, robust, and reliable operation in high-frequency switching power circuits. The robust inputs of UCC27444-Q1 can handle –5 V, ensuring reliable operation in noisy environments. The driver has good transient handling capability on its output due to its reverse current handling, as well as rail-to-rail output drive, and a small propagation delay (typically 18 ns). With this built-in robustness, the UCC27444-Q1 device can also be directly connected to a gate drive transformer.

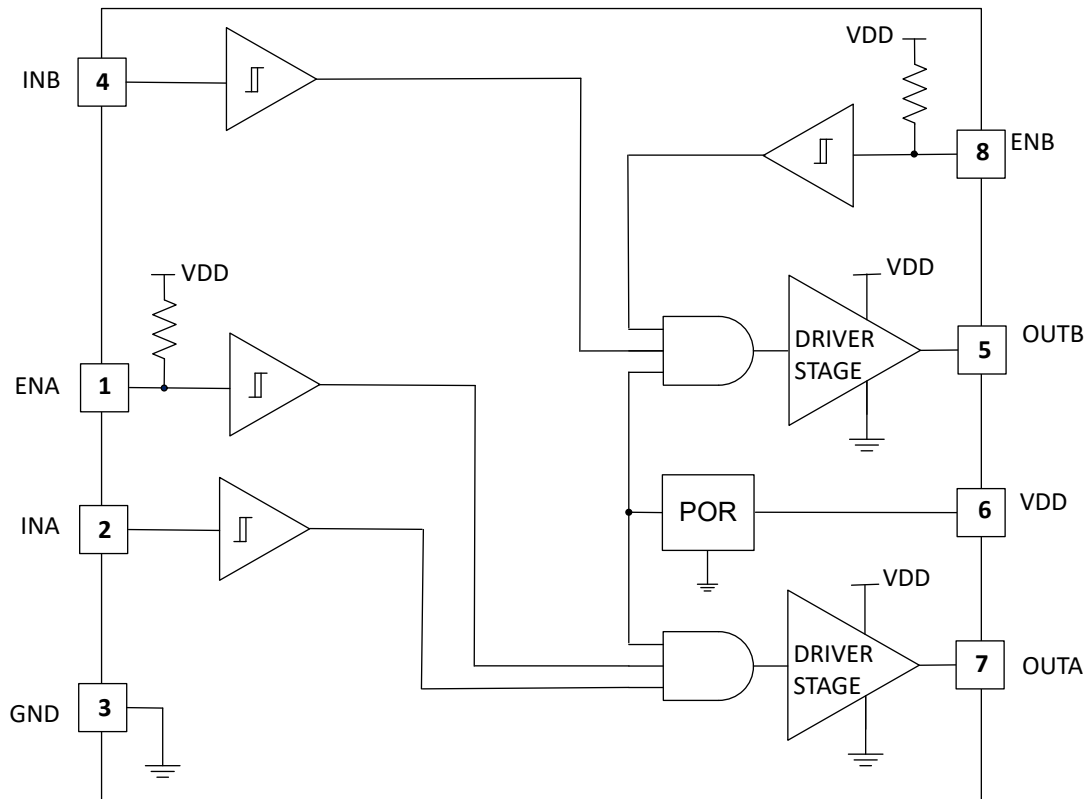
The input threshold of UCC27444-Q1 is compatible with TTL low-voltage logic, which is fixed and independent of VDD supply voltage. The driver can also work with CMOS-based controllers as long as the threshold requirement is met.

Each channel has an enable pin, ENx, with a fixed TTL compatible threshold. The ENx pins are internally pulled up. Pulling ENx low disables the corresponding channel, while leaving ENx open provides normal operation. The ENx pins can be used as an additional input with the same performance as the INx pins.

**表 7-1. UCC27444-Q1 Features and Benefits**

FEATURE	BENEFIT
–5-V IN capability	Enhanced signal reliability and device robustness in noisy environments that experience ground bounce on the gate driver
18-ns (typical) propagation delay	Extremely fast control to power device response times.
1-ns (typical) delay matching between channels	Ease of optimizing timing of power device switching such as selecting dead time.
VDD POR protection	Outputs are held low in power on reset conditions, which ensures predictable, glitch-free operation at power-up and power-down.
Outputs are enabled when enable pins (ENx) are in floating condition.	Pin-to-pin compatibility with legacy devices from Texas Instruments in designs where Pin 1 and Pin 8 are "No Connect" pins

## 7.2 Functional Block Diagram



Typical ENx pullup resistance is 100 k $\Omega$ .

## 7.3 Feature Description

### 7.3.1 Operating Supply Current

The UCC27444-Q1 device features low quiescent  $I_{DD}$  currents. The typical operating supply current in fully-on state (under static and switching conditions) are summarized in the Electrical Characteristics table. The total supply current is the sum of the quiescent  $I_{DD}$  current, the average  $I_{OUT}$  current because of switching, and any current related to pullup resistors on the enable pins. Knowing the operating switching frequency ( $f_{SW}$ ) and the MOSFET gate charge ( $Q_G$ ) at the drive voltage being used, the average  $I_{OUT}$  current can be calculated as product of  $Q_G$  and  $f_{SW}$ .

The Typical Characteristics provides a complete characterization of the  $I_{DD}$  current as a function of switching frequency at different  $V_{DD}$  bias voltages. The linear variation and close correlation with the theoretical value of the average  $I_{OUT}$  indicate a negligible shoot-through inside the gate driver device, displaying its high-speed characteristics.

### 7.3.2 Input Stage

The input pins of the UCC27444-Q1 gate driver device are based on a TTL compatible input threshold logic. With a high threshold of 2.2 V and a low threshold of 1.2 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power controller devices.

The UCC27444-Q1 device high resistance driver inputs reduces leakage currents in the input pins. The driver input signals are expected to be in a defined high or low state to control the driver outputs. If a controller is used which may have undefined or tri-state conditions on the driver control signals, it is recommended to have an external pull down resistance from the INx pins to ground.

The input pins can handle wide range of slew rate. In most power supply applications, the gate driver is either driven by the output of a digital controller or logic gates. Therefore, in most applications the input signal slew rate is fast and is no concern for the UCC27444-Q1 family of devices. If limiting the rise or fall times to the power

device is the primary goal, then an external gate resistor is highly recommended between the output of the driver and the gate of the switching power device. This external resistor has the additional benefit of reducing part of the gate-charge related power dissipation in the gate driver device package and transferring it into the external resistor itself. In short, some of the power gets dissipated in the gate resistor rather than inside of the gate driver. Additionally, the input pins of UCC27444-Q1 are capable of handling  $-5$  V. This improves the system robustness in noisy (electrical) applications. This also enables the driver to directly connect to the output of a gate drive transformer without the use of rectifying diodes, which saves board space and BOM cost.

### 7.3.3 Enable Function

The enable function is an extremely beneficial feature in gate driver devices, especially for certain applications such as synchronous rectification where the driver outputs are disabled in light-load conditions to prevent negative current circulation and to improve light-load efficiency.

The UCC27444-Q1 device is equipped with independent enable pins (ENx) for exclusive control of each driver channel operation. The enable pins are based on a non-inverting configuration (active-high operation). Thus, when ENx pins are driven high, the drivers are enabled and when ENx pins are driven low, the driver outputs are disabled. Similar to the input pins, the enable pins are also based on a TTL compatible threshold logic that is independent of the supply voltage and are effectively controlled using logic signals from 3.3-V or 5-V controllers. The ENx pins are internally pulled up to VDD using pullup resistors, as a result of which the outputs of the device are enabled in the default state. Hence even if the ENx pins are left floating the driver output is enabled. Essentially, this floating allows the UCC27444-Q1 device to be pin-to-pin compatible with TI's previous generation of drivers (UCC27324, UCC27424, UCC27524), where Pin 1 and Pin 8 are either ENx or N/C pins.

### 7.3.4 Output Stage

The UCC27444-Q1 device output stage features a P-Channel architecture on the pullup structure, which delivers the highest peak source current when it is most needed, during the Miller plateau region of the power switch turn-on transition (when the power switch drain or collector voltage experiences  $dV/dt$ ). This pull up architecture closely emulates the behavior of the popular industry driver devices UCC2732x and UCC2742x. One characteristic of this pullup driver stage architecture is relatively consistent driver output rise and fall times over a wide VDD range.

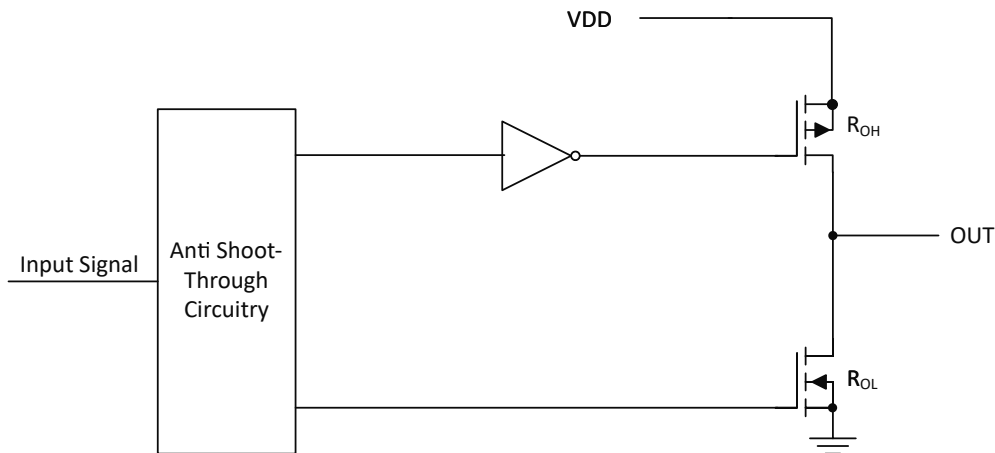


FIG 7-1. UCC27444-Q1 Gate Driver Output Structure

The  $R_{OH}$  parameter is a DC measurement and it is representative of the on-resistance of the P-Channel device on the pull-up stage of the device.

The pull-down structure in the UCC27444-Q1 device is simply comprised of a N-Channel MOSFET. The  $R_{OL}$  parameter, which is also a DC measurement, is representative of the impedance of the pulldown stage in the device.

Each output stage in the UCC27444-Q1 device is capable of supplying 4-A peak source and 4-A peak sink current pulses. The output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the

MOS-output stage which delivers very low dropout. The presence of the MOSFET-body diodes also offers low impedance to transient overshoots and undershoots. The outputs of these drivers are designed to withstand 4 A of peak reverse current transients without damage to the device.

The UCC27444-Q1 device is particularly suited for dual-polarity, symmetrical drive-gate transformer applications where the primary winding of transformer driven by OUTA and OUTB, with inputs INA and INB being driven complementary to each other. This is possible because of the extremely low dropout offered by the MOS output stage of these devices, both during high ( $V_{OH}$ ) and low ( $V_{OL}$ ) states along with the low impedance of the driver output stage. All of these allow alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure proper reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turn-on or turn-off interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

### 7.3.5 Low Propagation Delays and Tightly Matched Outputs

The UCC27444-Q1 driver device features a low, 18-ns (typical) propagation delay between input and output which offers fast response time from the control signals to the power devices. Additionally, the driver devices also feature extremely accurate, 1-ns (typical) matched internal propagation delays between the two channels, which is beneficial for applications that require dual gate drives with critical timing. For example, in a PFC application, a pair of paralleled MOSFETs can be driven independently using each output channel, with the inputs of both channels driven by a common control signal from the PFC controller. In this case, the 1-ns delay matching ensures that the paralleled MOSFETs are driven in a simultaneous fashion, minimizing turn-on and turn-off delay differences.

## 7.4 Device Functional Modes

表 7-2. Device Logic Table

ENA	ENB	INA	INB	UCC27444-Q1	
				OUTA	OUTB
H	H	L	L	L	L
			H	L	H
		H	L	H	L
			H	H	H
L	L	Any	Any	L	L
H Or Float	H Or Float	Float	Float	X	X
Float	Float	L	L	L	L
			H	L	H
		H	L	H	L
			H	H	H

## 8 Application and Implementation

---

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

---

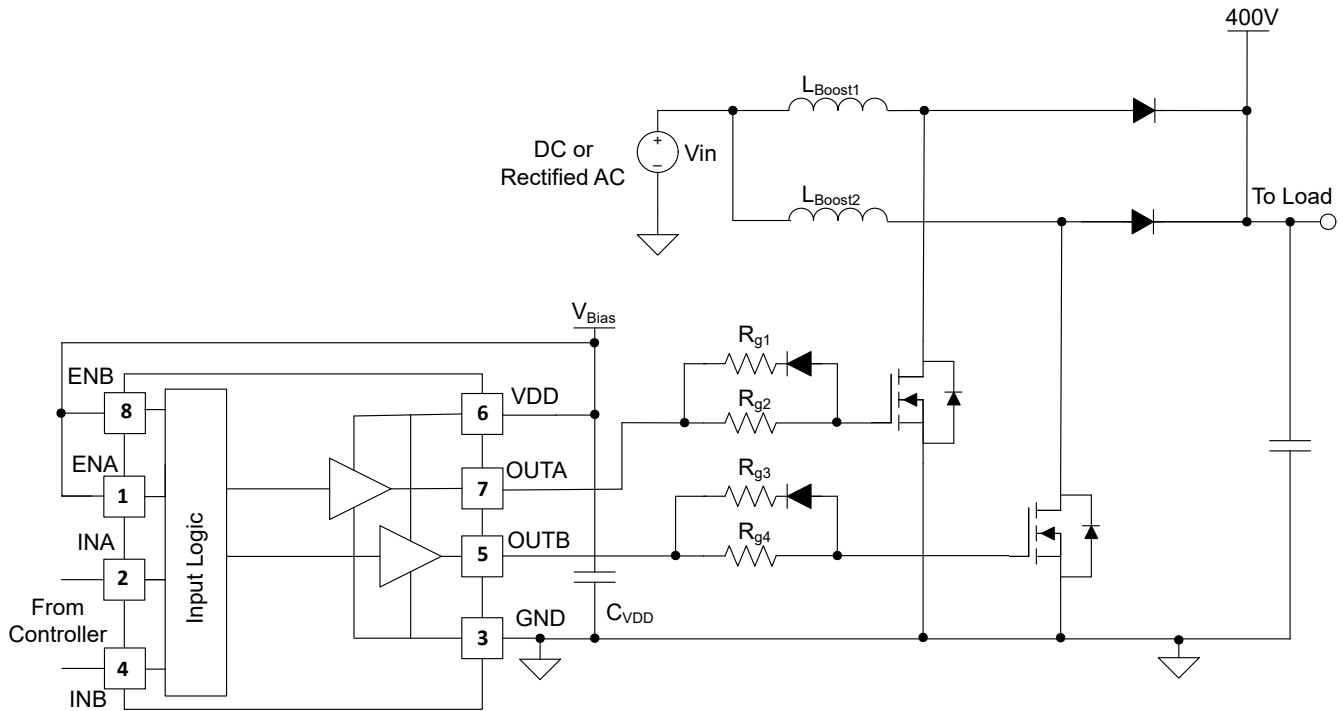
### 8.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. In order to achieve fast switching of power devices and reduce associated switching-power losses, a powerful gate driver device is employed between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate driver devices are indispensable when it is not feasible for the PWM controller device to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning ON a power switch. A level-shifting circuitry is required to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn ON the power device and minimize conduction losses. Traditional buffer-drive circuits based on NPN/PNP bipolar transistors in a totem-pole arrangement, as emitter-follower configurations, prove inadequate with digital power because the traditional buffer-drive circuits lack level-shifting capability. Gate driver devices effectively combine both the level-shifting and buffer-drive functions. Gate driver devices also find other needs, such as minimizing the effect of high frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controller devices by moving gate-charge power losses into the controller.

Finally, emerging wide band-gap power device technologies, such as GaN switches, which are capable of supporting very high switching frequency operation, are driving special requirements in terms of gate-drive capability. These requirements include a low operating voltage range (5 V to 6 V), low propagation delays, good delay matching, and availability in compact, low inductance packages with good thermal capability. In summary, gate driver devices are an extremely important component in switching power combining benefits of high performance, low cost, low component count, board space reduction, and simplified system design.



## 8.2 Typical Application



**8-1. UCC27444-Q1 Typical Application Diagram**

### 8.2.1 Design Requirements

When selecting and designing-in the gate driver device for an end application, some functional aspects must be considered and evaluated first, in order to make the most appropriate selection. Among these considerations are bias voltage, POR, drive current, and power dissipation.

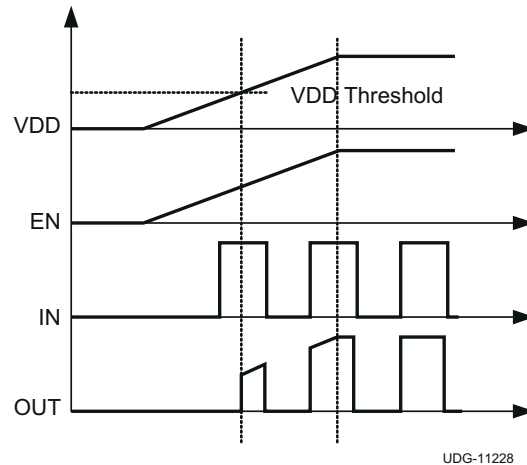
### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 VDD and Power On Reset

The UCC27444-Q1 device has an internal power on reset (POR) protection feature on the VDD pin supply circuit blocks. When VDD is rising and the level is still below POR threshold, this circuit holds the output low, regardless of the status of the inputs. The POR is typically 3 V with 300-mV typical hysteresis. This hysteresis prevents chatter when VDD supply voltages have noise, specifically at the lower end of the VDD operating range. POR hysteresis is also important to avoid any false tripping due to the bias noise generated because of fast switching transitions, where large peak currents are drawn from the bias supply bypass capacitors. The driver capability to operate at wide bias voltage range, along with good switching characteristics, is especially important in driving emerging power semiconductor devices, such as advanced low gate charge fast MOSFETs, and GaN FETs.

At power-up, the UCC27444-Q1 driver device output remains low until the VDD voltage reaches the POR rising threshold, irrespective of the state of any other input pins such as INx and ENx. After the POR rising threshold, the magnitude of the OUT signal rises with V<sub>DD</sub> until steady-state V<sub>DD</sub> is reached.

For the best high-speed circuit performance and to prevent noise problems because the device draws current from the VDD pin to bias all internal circuits, use two VDD bypass capacitors. Also, use surface mount, low ESR capacitors. A 0.1- $\mu$ F ceramic capacitor should be located less than 1 mm from the VDD to GND pins of the gate-driver device. In addition, a larger capacitor ( $\geq 1 \mu$ F) must be connected in parallel (also as close to the driver IC as possible) to help deliver the high-current peaks required by the load. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.



**8-2. Power-Up Sequence**

### 8.2.2.2 Drive Current and Power Dissipation

The UCC27444-Q1 driver is capable of delivering 4 A of peak current to a switching power device gate (MOSFET, GaN FET) for a period of several-hundred nanoseconds at  $V_{DD} = 12$  V. High peak current is required to turn ON the device quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground, which repeats at the operating switching frequency of the power device. The power dissipated in the gate driver device package depends on the following factors:

- Gate charge of the power MOSFET (usually a function of the drive voltage  $V_{GS}$ , which is very close to input bias supply voltage  $V_{DD}$  due to low  $V_{OH}$  drop-out).
- Switching frequency
- External gate resistors

Because UCC27444-Q1 features low-quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is very small compared to the losses due to switching of the power device.

When a driver device is tested with a discrete capacitive load, calculating the power that is required from the bias supply is fairly simple. The following equation provides an example of the energy that must transfer from the bias supply to charge the capacitor.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \quad (1)$$

where

- $C_{LOAD}$  is the load capacitor.
- $V_{DD}$  is the bias voltage of the driver.

There is an equal amount of energy dissipated when the capacitor is discharged. This leads to a total power loss, as shown in the following equation example.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} \quad (2)$$

where

- $f_{SW}$  is the switching frequency.

With  $V_{DD} = 12$  V,  $C_{LOAD} = 10$  nF and  $f_{SW} = 300$  kHz, the switching power loss is calculated as follows:

$$P_G = 10\text{nF} \times 12\text{V}^2 \times 300\text{kHz} = 0.432\text{W} \quad (3)$$

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge  $Q_g$ , the power that must dissipate when charging a capacitor is determined, which by using the equivalence  $Q_g = C_{\text{LOAD}}V_{\text{DD}}$  is shown in the following equation.

$$P_G = C_{\text{LOAD}}V_{\text{DD}}^2f_{\text{SW}} = Q_gV_{\text{DD}}f_{\text{SW}} \quad (4)$$

Assuming that the UCC27444-Q1 device is driving power MOSFET with 60 nC of gate charge ( $Q_g = 60\text{ nC}$  at  $V_{\text{DD}} = 12\text{ V}$ ) on each output, the gate charge related power loss is calculated using the equation below.

$$P_G = 2 \times 60\text{nC} \times 12\text{V} \times 300\text{kHz} = 0.432\text{W} \quad (5)$$

This power  $P_G$  is dissipated in the resistive elements of the circuit when the MOSFET turns on or turns off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{\text{SW}} = 0.5 \times Q_G \times V_{\text{DD}} \times f_{\text{SW}} \times \left( \frac{R_{\text{OFF}}}{R_{\text{OFF}} + R_{\text{GATE}}} + \frac{R_{\text{ON}}}{R_{\text{ON}} + R_{\text{GATE}}} \right) \quad (6)$$

where

- $R_{\text{OFF}} = R_{\text{OL}}$
- $R_{\text{ON}}$  (effective resistance of pull-up structure)

The above equation is necessary when the external gate resistor is large enough to reduce the peak current of the driver. In addition to the above gate-charge related power dissipation, dissipation in the driver is related to the power associated with the quiescent bias current consumed by the device to bias all internal circuits such as input stage (with pullup and pulldown resistors), enable, and POR sections. As shown in the electrical characteristics table, the maximum quiescent current is less than 0.6 mA. The power loss due to DC current consumption of the driver internal circuit can be calculated as below.

$$P_Q = I_{\text{DD}}V_{\text{DD}} \quad (7)$$

Assuming total internal current consumption to be 0.6 mA (maximum) at bias voltage of 12 V, the DC power loss in the driver is:

$$P_Q = 0.6\text{ mA} \times 12\text{V} = 7.2\text{mW} \quad (8)$$

This power loss is insignificant compared to gate charge related power dissipation calculated earlier.

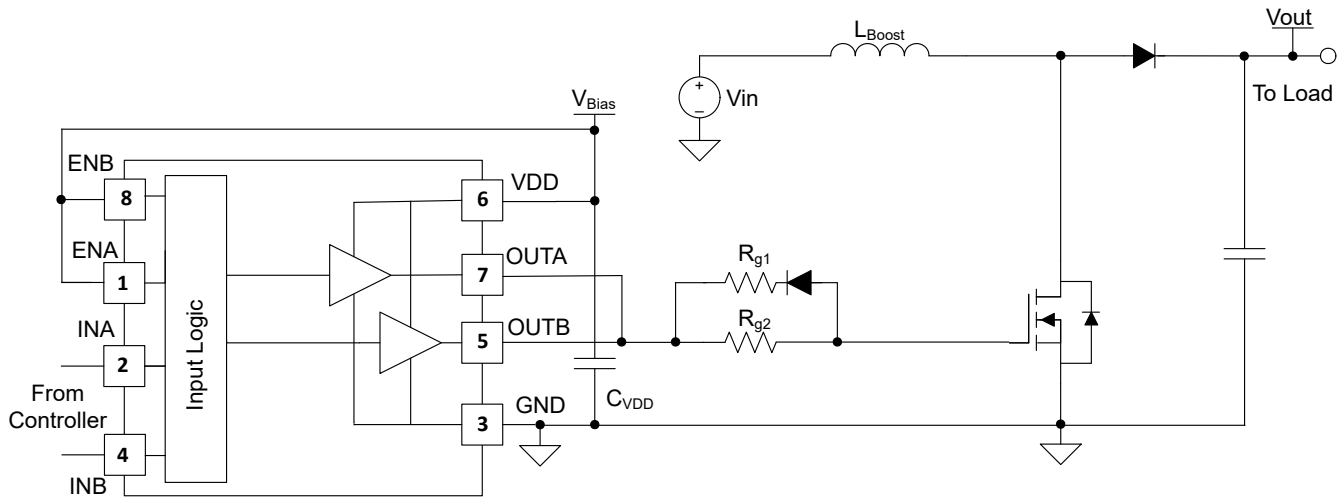
With a 12-V supply, the bias current is estimated as follows, with an additional 0.6-mA overhead for the quiescent consumption:

$$I_{DD} \sim \frac{P_G}{V_{DD}} = \frac{0.432 \text{ W}}{12 \text{ V}} = 0.036 \text{ A} \tag{9}$$

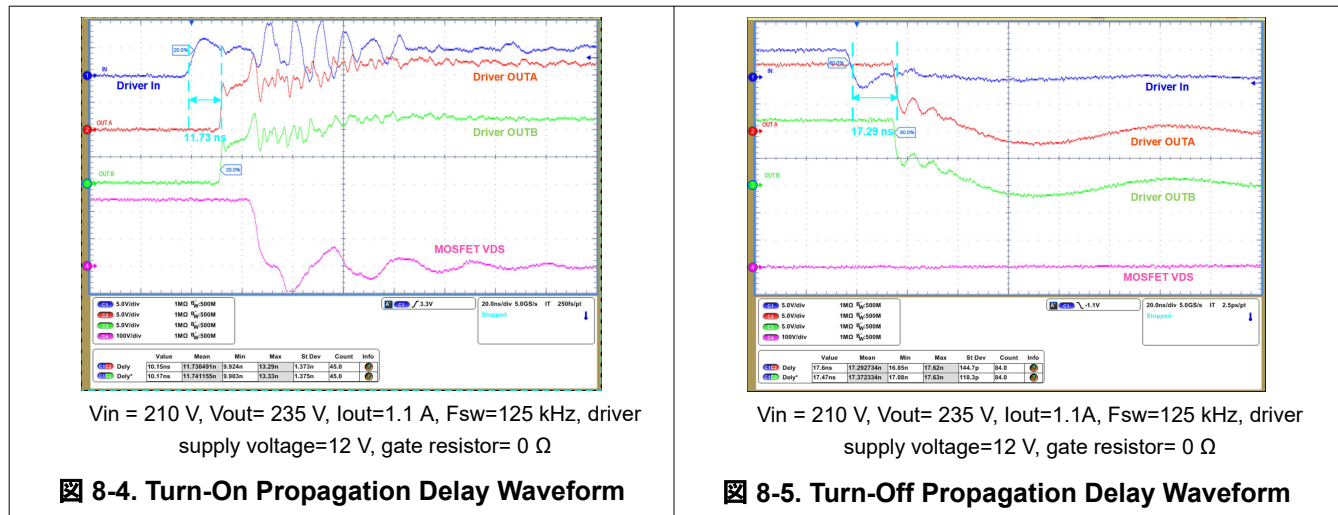
If the gate driver is used with inductive load, then special attention should be paid to the ringing on each pin of the gate driver device. The ringing should not exceed the recommended operating rating of the pin.

### 8.2.3 Application Curves

The figures below show the typical switching characteristics of the UCC27444-Q1 device used in high-voltage boost converter application. In this application, the UCC27444-Q1 is driving the IGBT switch that has a gate charge of 110nC.



**8-3. UCC27444-Q1 Used to Drive IGBT in the Boost Converter**



## 9 Power Supply Recommendations

The bias supply voltage range for the UCC27444-Q1 device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal power-on-reset (POR) protection feature on the  $V_{DD}$  pin supply circuit blocks. If the driver is in a POR condition when the  $V_{DD}$  pin voltage is below the VDD POR turn-on (rising) threshold, the POR protection feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). It is necessary to have sufficient margin from the absolute maximum rating of the device to realize full operating life of the device. Therefore, the upper limit of recommended voltage of the VDD pin is 18 V.

The POR protection feature also has a hysteresis function. This means, when the VDD pin bias voltage exceeds the rising threshold voltage, the device begins to operate normally. If the VDD bias voltage drops below the rising threshold while on, the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification of the falling threshold. Therefore, while operating at or near the 4.5-V, design engineer should ensure that the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device. Otherwise, the device output may turn-off. During system shutdown, the device operation continues until the VDD pin voltage has dropped below the VDD turn-off (falling) threshold, which must be accounted for while evaluating system shutdown timing or sequencing requirements. At system startup, the device does not begin operation until the VDD pin voltage has exceeded VDD turn-on (rising) threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, recognizing that the charge for source current pulses delivered by the OUTA/B pin is also supplied through the same VDD pin capacitor, is important. As a result, every time a current is sourced out of the output pins, a corresponding current pulse is delivered into the device through the VDD pin. Thus, ensure that the local bypass capacitors are provided between the VDD and GND pins and locate them as close to the device pins as possible for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is required. TI recommends having two capacitors: a 0.1- $\mu$ F ceramic surface-mount capacitor placed less than 1 mm from the VDD pin of the device and another larger ceramic capacitor ( $\geq 1 \mu$ F) must be connected in parallel.

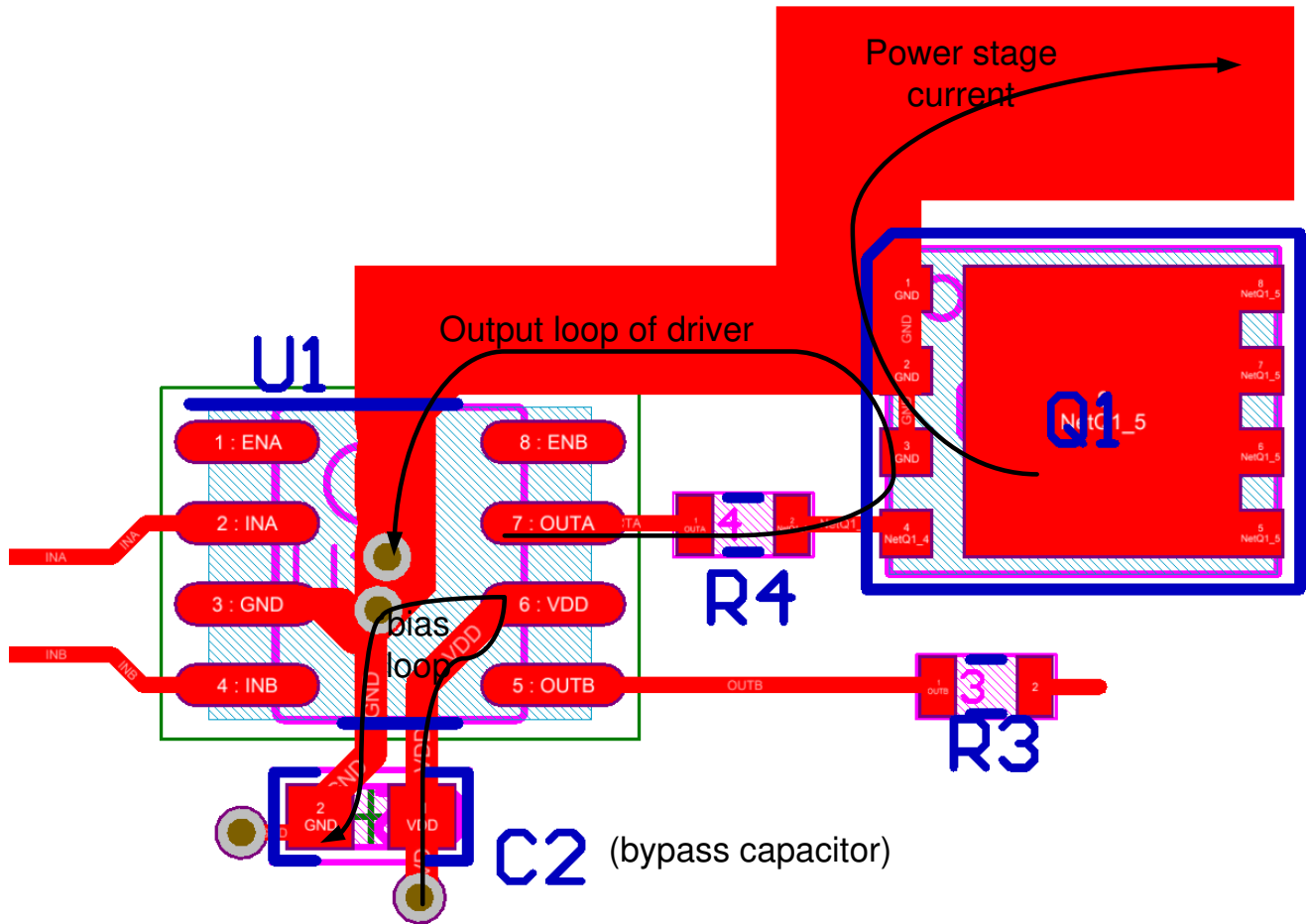
## 10 Layout

### 10.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC27444-Q1 gate driver incorporates small propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power MOSFET to facilitate very quick voltage transitions. Very high  $di/dt$  causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are recommended when designing with these high-speed drivers.

- Place the driver IC as close as possible to the power device in order to minimize the length of high-current traces between the driver IC output pins and the gate of the switching power device.
- Place the VDD bypass capacitors between VDD and GND as close as possible to the driver IC with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD pin, during turn-on of power MOSFET. The use of low inductance surface-mounted-device (SMD) components such as 50V rated X7R chip capacitors are highly recommended.
- The turn-on and turn-off current loop paths (driver device, power MOSFET and VDD bypass capacitor) must be minimized as much as possible in order to keep the stray inductance to a minimum. High  $di/dt$  is established in these loops at two instances, namely during turn-on and turn-off transients, which induces significant voltage transients on the output pin of the driver device and Gate of the power MOSFET.
- Wherever possible, parallel the source and return traces to take advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- To minimize switch node transients and ringing, adding some gate resistance and/or snubbers on the power devices may be necessary. These measures may also reduce EMI.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver is connected to the other circuit nodes such as source of power MOSFET and ground of PWM controller at one, single point. The connected paths must be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT pin of the driver IC may corrupt the input signals of the driver IC. The ground plane must not be a conduction path for any high current (power stage) loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well
- External gate resistor and parallel diode-resistor combination may come in handy when replacing any gate driver IC with UCC27444-Q1 device in existing or new designs, specifically if they do not have the same drive strength.

## 10.2 Layout Example



10-1. UCC27444-Q1 Layout Example

## 10.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a gate driver device to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced, while keeping the junction temperature within the specified limit. For detailed information regarding the thermal information table, please refer to the [Semiconductor and IC Package Thermal Metrics Application Note \(SPRA953\)](#).

Among the different package options available for the UCC27444-Q1 device, power dissipation capability of the DGN package is of particular mention. The VSSOP-8 (DGN) package offers thermal pad for removing the heat from the semiconductor junction through the bottom of the package. This pad is soldered to the copper on the printed circuit board directly underneath the device package, reducing the thermal resistance to a very low value. This allows a significant improvement in heat-sinking over the D package. The printed circuit board must be designed with thermal lands and thermal vias to complete the heat removal subsystem. Note that the exposed pads in the VSSOP-8 package are not directly connected to any leads of the package, however, PowerPAD is thermally connected to the substrate of the device. TI recommends to externally connect the exposed pads to GND pin of the driver IC in PCB layout.

## 11 Device and Documentation Support

### 11.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

### 11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 11.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の [使用条件](#) を参照してください。

### 11.4 Trademarks

PowerPAD™ is a trademark of Texas Instruments.

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 11.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 11.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27444QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	444Q	<a href="#">Samples</a>
UCC27444QDRQ1	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	27444Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## GENERIC PACKAGE VIEW

**DGN 8**

**PowerPAD VSSOP - 1.1 mm max height**

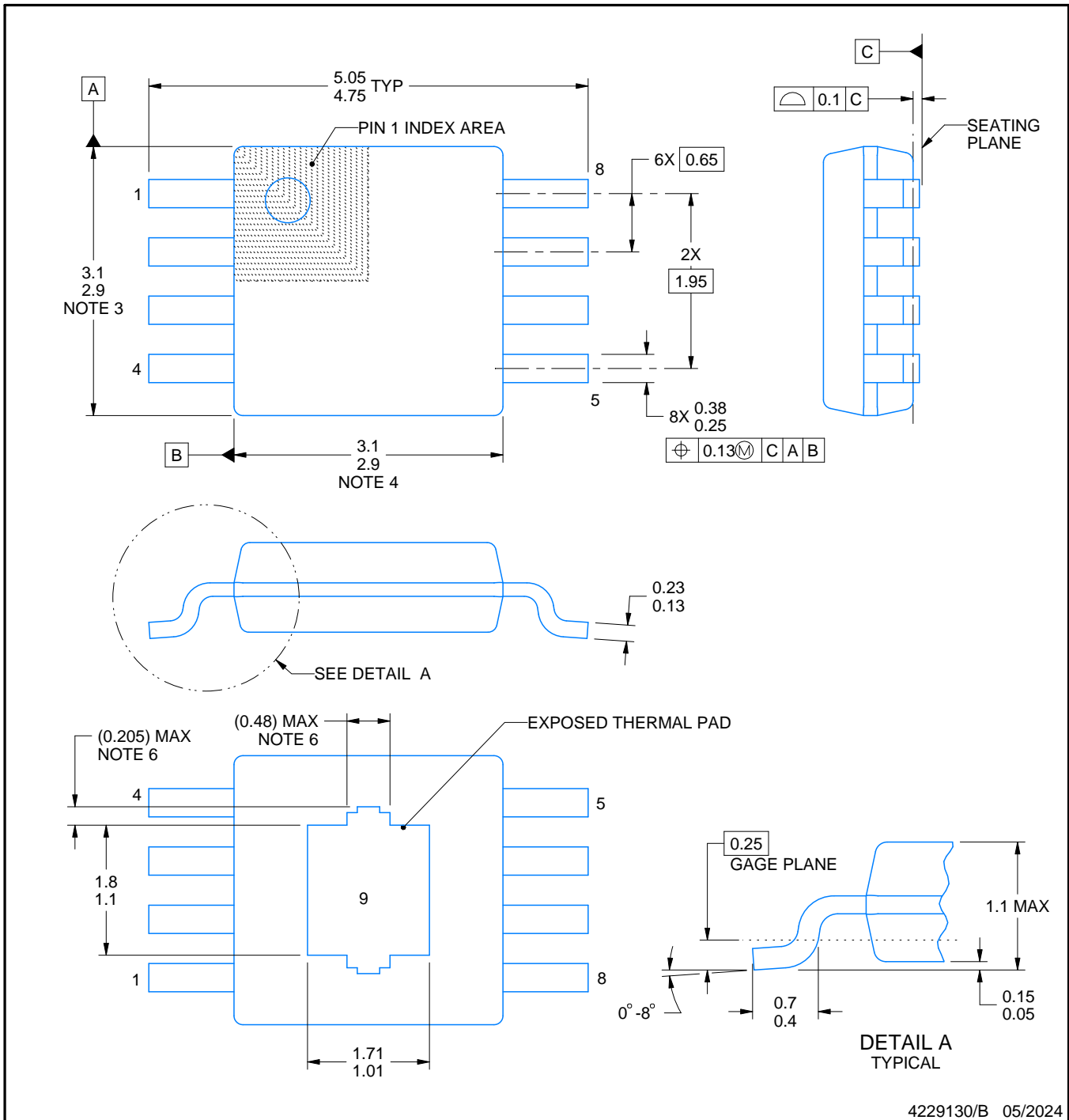
3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225482/A



4229130/B 05/2024

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.
6. Features may differ or may not be present.



# EXAMPLE STENCIL DESIGN

DGN0008H

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
EXPOSED PAD 9:  
100% PRINTED SOLDER COVERAGE BY AREA  
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.91 X 2.01
0.125	1.71 X 1.80 (SHOWN)
0.15	1.56 X 1.64
0.175	1.45 X 1.52

4229130/B 05/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

### NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated