2.5A および 5A、35V$_{MAX}$ VDD、FET および IGBT シングル ゲート ドライバ

1 特長

- 低コストのゲートドライバ (FET と IGBT の駆動に最適なソリューションを提供)
- ディスクリートトランジスタ ペアによる駆動の代替として最適 (コントローラとのインターフェイスが容易)
- CMOS 互換の入力ロジック スレッショルド (VDD が 18V を超えた場合は固定)
- 分割出力により、ターンオンとターンオフを個別に調整可能
- TTL 互換の固定スレッショルドによるイネーブル
- 高いピーク駆動電流:ソース 2.5A、シンク 5A (VDD 18V 時)
- 広い VDD 範囲:10V～35V
- グランドより低い電圧 (DC -5V) にも耐える入力ピン
- 入力がフローティング時または VDD UVLO 時は出力を Low に保持
- 高速伝搬遅延時間:17ns (標準値)
- 高速な立ち上がり / 立ち下がり時間:15ns/7ns (標準値、1800pF 負荷)
- 低電圧誤動作防止 (UVLO)
- ハイサイドまたはローサイド ドライバとして使用可能 (適切にバイアスを印加し信号を分離して設計した場合)
- 低コストで省スペースの 6 ピン DBV (SOT-23) パッケージ
- 動作温度範囲:–40℃～140℃

2 アプリケーション

- 車載用
- スイッチ モード電源
- DC/DC コンバータ
- ソーラー インバータ、モーター制御、UPS
- HEV および EV 用充電器
- 家電製品
- 再生可能エネルギーの電力変換
- SiC FET コンバータ

3 概要

UCC27532 は、最大 2.5A のソース電流と最大 5A のシンク電流 (非対称駆動) で MOSFET および IGBT パワースイッチを効率的に駆動できるシングル チャネル高速ゲート ドライバです。非対称駆動の強力なシンク能力により、寄生成分によるミラー ターンオン効果に対して耐性を高めています。また、UCC27532 デバイスは分割出力構成を実装し、ゲート駆動電流は OUTH ピンからソース、OUTL ピンからシンクされます。このピン配置により、ユーザーは OUTH および OUTL ピンに対してそれぞれ独立したオン/オフ抵抗を使用でき、スイッチングのスルー レートを簡単に制御できます。

また、レール ツー レールの駆動能力と、標準 17ns の非常に小さな伝搬遅延を特長としています。

UCC27532DBV は、18V 以下の VDD において、VDD 電圧の 55% (立ち上がり時) と VDD 電圧の 45% (立ち下がり時) に設定された CMOS 入力スレッショルドを持っています。VDD が 18V より高い場合、入力スレッショルドはその最大レベルに固定されたままになります。

このドライバには、TTL 互換の固定スレッショルドを持つ EN ピンが搭載されています。EN は内部でプルアップされているため、EN を Low にするとドライバがディスエーブルになり、オープンにすると通常動作が可能になります。EN ピンは、IN ピンと同じ性能を持つ追加の入力としても使用できます。

ドライバの入力ピンをオープンにすると、出力が Low に保持されます。ドライバのロジック動作は、アプリケーション図、タイミング図、および入出力真理値表に示されています。

VDD ピンの内部回路には、低電圧誤動作防止機能が搭載され、VDD 電源電圧が動作範囲内になるまで出力が Low に保持されます。

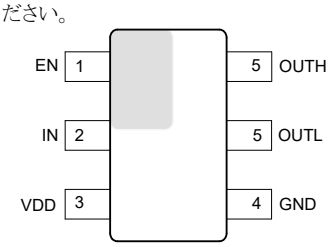
UCC27532 ドライバは、6 ピンの標準 SOT-23（DBV）パッケージで供給されます。デバイスは、-40°C～140°C の幅広い温度範囲で動作します。

パッケージ情報

部品番号	パッケージ (1) (2)	ピーク電流 (ソースおよびシンク)	入力スレッショルド ロジック	動作温度範囲 T_A
UCC27532 DBV	DBV (SOT-23、6)	2.5A、5A	CMOS (VDD バイアス電圧に依存)	-40℃～+140℃

(1) DBV パッケージは Pb フリー リード仕上げ (Pd-Ni-Au) であり、255℃～260℃のピーク リフロー温度で MSL レベル 1 に準拠し、鉛フリーはんだと Sn/Pb はんだのどちらにも対応できます。

(2) 供給されているすべてのパッケージについては、セクション 11 を参照してください。



ピン配置

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4 Pin Configuration and Functions

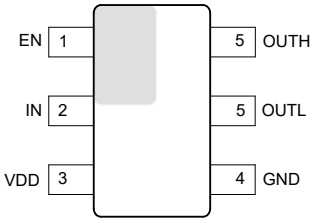


図 4-1. 6-Pin DBV SOT-23, Package (top view)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO	NAME		
1	EN	I	Enable (Pull EN to GND in order to disable output, pull it high or leave open to enable output).
2	IN	I	Driver non-inverting input (CMOS threshold for UCC27532DBV).
3	VDD	I	Bias supply input.
4	GND	-	Ground (all signals are referenced to this node).
5	OUTL	O	5-A sink current output of driver.
6	OUTH	O	2.5-A source current output of driver.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2) (3)

		MIN	MAX	UNIT
Supply voltage range,	VDD	-0.3	35	V
Continuous	OUTH, OUTL	-0.3	VDD +0.3	
Pulse	OUTH, OUTL (200 ns)	-2	VDD +0.3	
Continuous IN, EN		-5	27	V
Pulse IN, EN (1.5 µs)		-6.5	27	
Human body model, HBM (ESD)(5)			4000	
Charged device model, CDM (ESD)			1000	
Operating virtual junction temperature range, T_J		-40	150	°C
Storage temperature range, T_{stg}		-65	150	
Lead temperature	Soldering, 10 sec.		300	
	Reflow		260	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.

5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, VDD	10	18	32	V
Operating junction temperature range	-40		140	°C
Input voltage, IN	-5		25	V
Enable, EN	-5		25	

5.3 Thermal Information

THERMAL METRIC(1)		UCC27532 DBV (6 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	178.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	109.7	
θ_{JB}	Junction-to-board thermal resistance(4)	28.3	
ψ_{JT}	Junction-to-top characterization parameter(5)	14.7	
ψ_{JB}	Junction-to-board characterization parameter(6)	27.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	n/a	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

5.4 Electrical Characteristics

Unless otherwise noted, VDD = 18 V, $T_A = T_J$ = -40°C to 140°C, IN switching from 0 V to VDD, 1-µF capacitor from VDD to GND, f = 100 kHz. Currents are positive into, negative out of the specified terminal. OUTH and OUTL are tied together. Typical condition specifications are at 25°C.

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Bias Currents						
I_{DDoff}	Startup Current, VDD = 7.0	IN, EN = VDD	100	240	350	µA
		IN, EN = GND	100	250	350	
Under Voltage Lockout (UVLO)						
V_{ON}	Supply start threshold		8.0	8.9	9.8	V
V_{OFF}	Minimum operating voltage after supply start		7.3	8.2	9.1	
V_{DD_H}	Supply voltage hysteresis			0.7		
Input (IN)						
V_{IN_H}	Input signal high threshold	VDD = 16V, Output high	8.8	9.4	10	V
V_{IN_L}	Input signal low threshold	VDD = 16V, Output low	6.7	7.3	7.9	
V_{IN_HYS}	Input signal hysteresis	VDD = 16V		2.1		
Enable (EN)						
V_{EN_H}	Enable signal high threshold	VDD = 16V, Output high	1.7	1.9	2.1	V
V_{EN_L}	Enable signal low threshold	VDD = 16V, Output low	0.8	1.0	1.2	
V_{EN_HYS}	Enable signal hysteresis	VDD = 16V		0.9		
Outputs (OUTH/OUTL)						
$I_{SRC/SNK}$	Source peak current (OUTH)/ sink peak current (OUTL)(13) (1)	C_{LOAD} = 0.22 µF, f = 1 kHz		-2.5/+5		A
V_{OH}	OUTH, high voltage	I_{OUTH} = -10 mA	VDD -0.2	VDD -0.12	VDD -0.07	V
V_{OL}	OUTL, low voltage	I_{OUTL} = 100 mA		0.065	0.125	
R_{OH}	OUTH, pull-up resistance (15) (3)	T_A = 25°C, I_{OUT} = -10 mA	11	12	12.5	Ω
		T_A = -40°C to 140°C, I_{OUT} = -10 mA	7	12	20	
R_{OL}	OUTL, pull-down resistance	T_A = 25°C, I_{OUT} = 100 mA	0.45	0.65	0.85	
		T_A = -40°C to 140°C, I_{OUT} = 100 mA	0.3	0.65	1.25	
Switching Time (1) (2)						
t_R	Rise time	C_{LOAD} = 1.8 nF		15		ns
t_F	Fall time	C_{LOAD} = 1.8 nF		7		
t_{D1}	Turn-on propagation delay	C_{LOAD} = 1.8 nF, IN = 0 V to VDD		17	26	
t_{D2}	Turn-off propagation delay	C_{LOAD} = 1.8 nF, IN = VDD to 0 V		17	26	

(1) Ensured by design and tested during characterization. Not production tested.
(2) See 図 5-1.
(3) Output pull-up resistance here is a DC measurement that measures resistance of PMOS structure only, not N-channel structure. The effective dynamic pull-up resistance is 3 x R_{OL}.

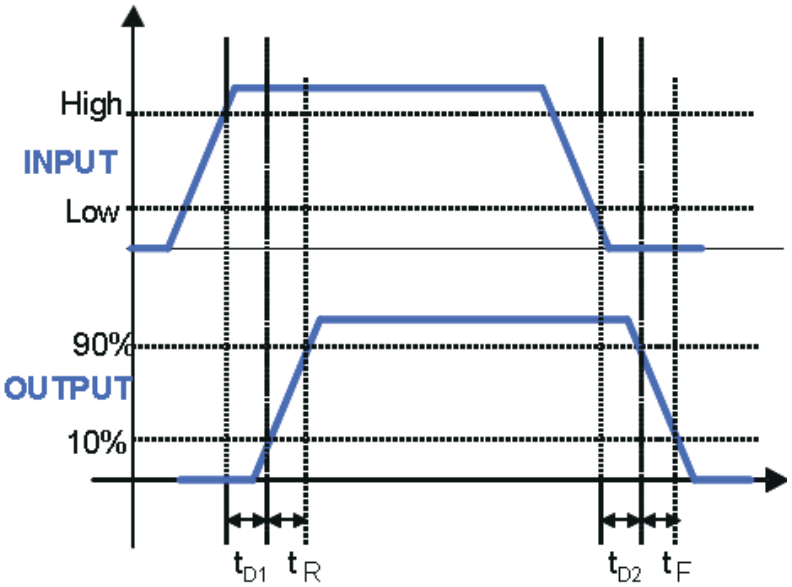


図 5-1. Timing Diagram (OUTH tied to OUTL)(Input = IN, Output = OUT (EN = VDD), or Input = EN, Output = OUT (IN = VDD)

5.5 Typical Characteristics

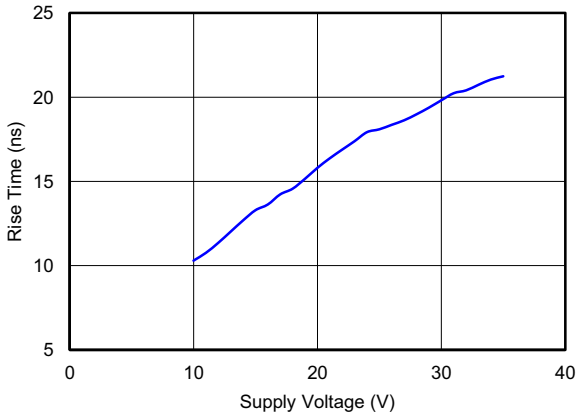


図 5-2. Rise Time vs Supply Voltage

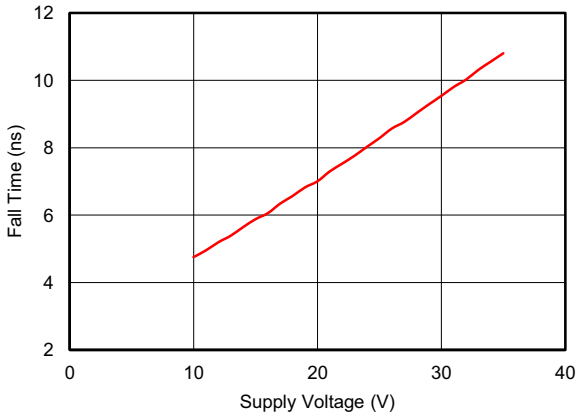


図 5-3. Fall Time vs Supply Voltage

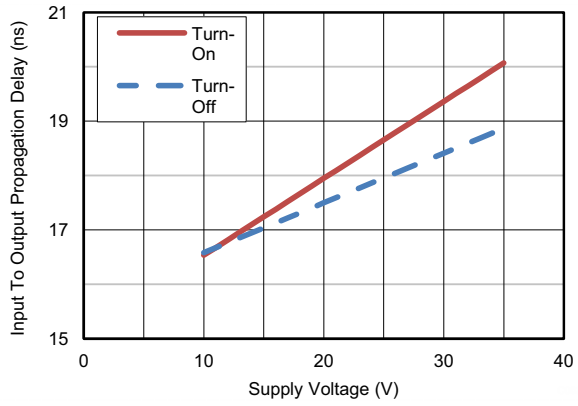


図 5-4. Propagation Delay vs Supply Voltage

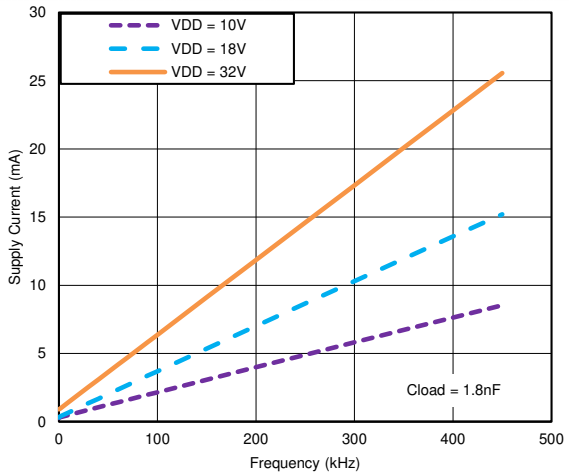


図 5-5. Operating Supply Current vs Frequency

5.5 Typical Characteristics (continued)

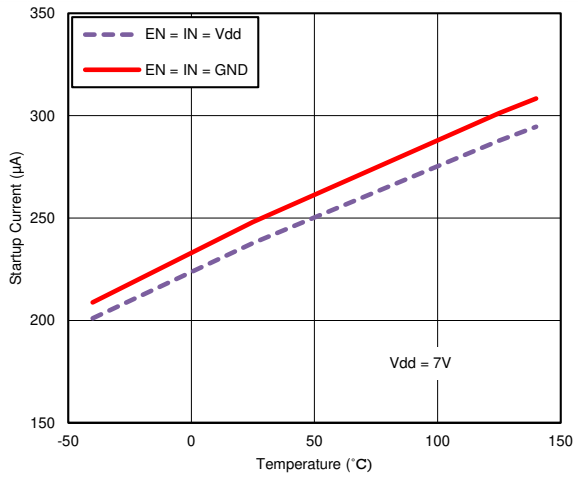


図 5-6. Start-Up Current vs Temperature

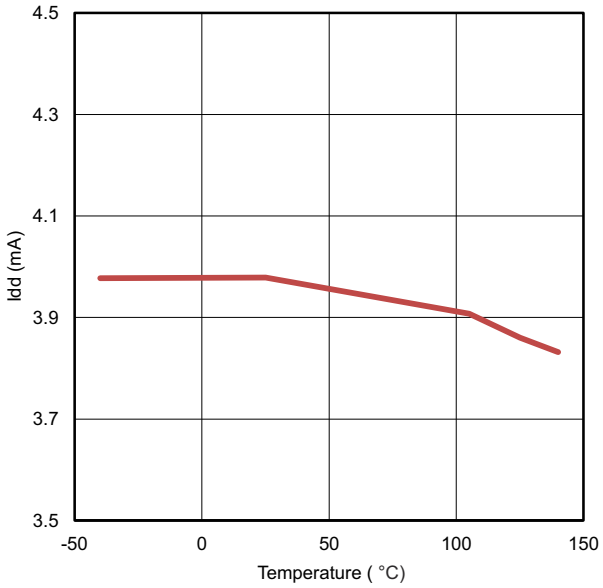


図 5-7. Operating Supply Current vs Temperature (output switching)

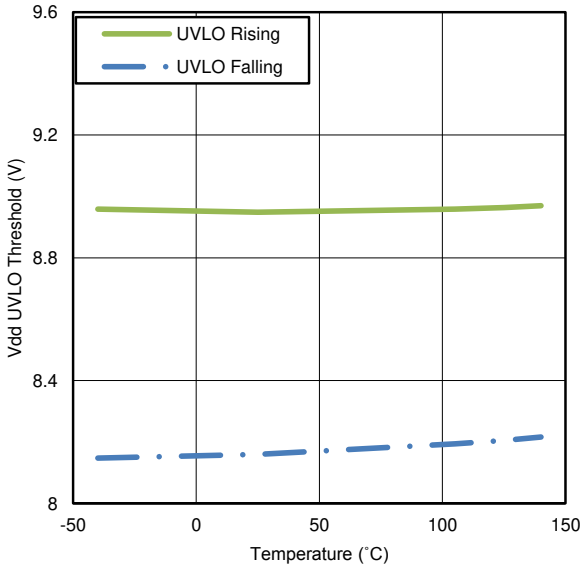


図 5-8. UVLO Threshold Voltage vs Temperature

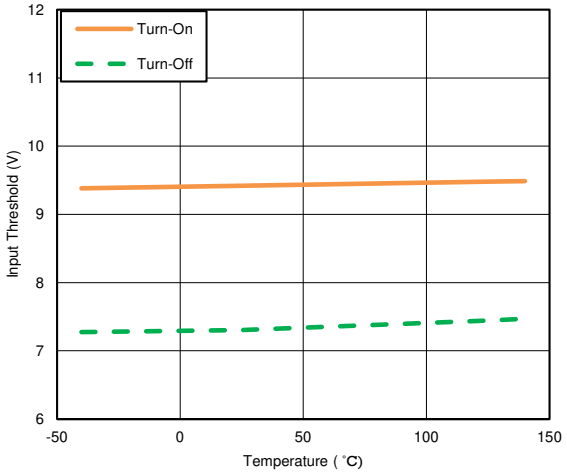


図 5-9. Input Threshold vs Temperature

5.5 Typical Characteristics (continued)

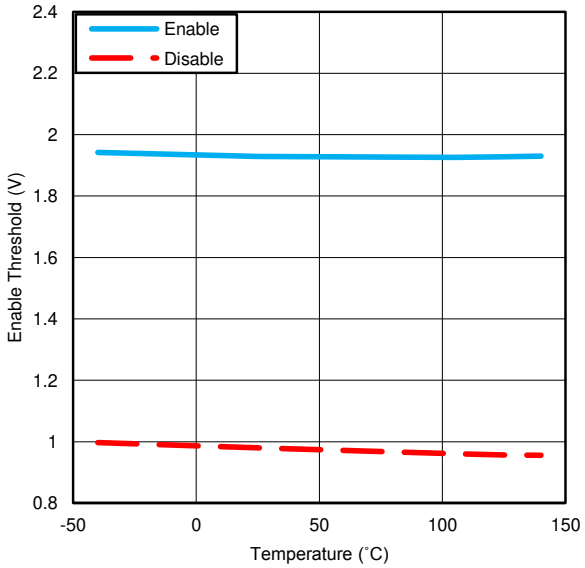


図 5-10. Enable Threshold vs Temperature

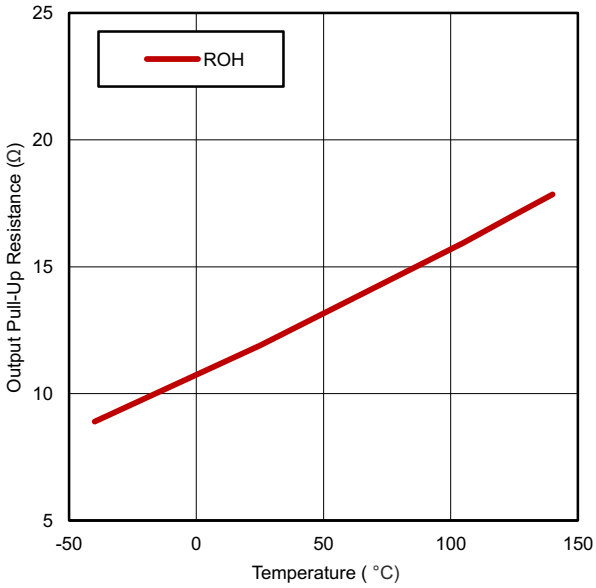


図 5-11. Output Pull-Up Resistance vs Temperature

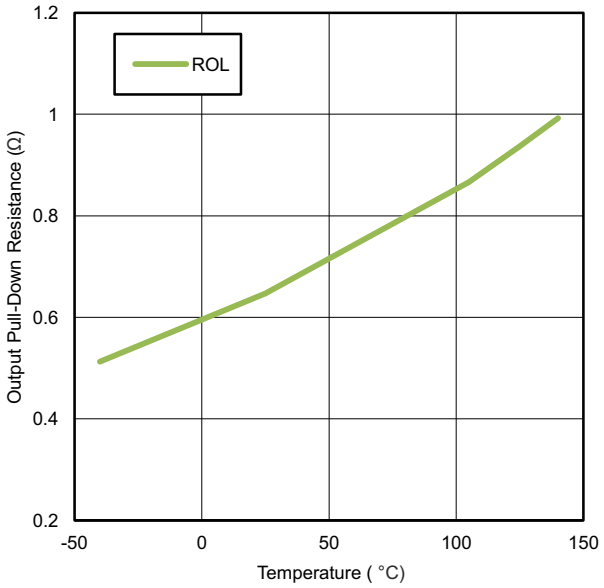


図 5-12. Output Pull-Down Resistance vs Temperature

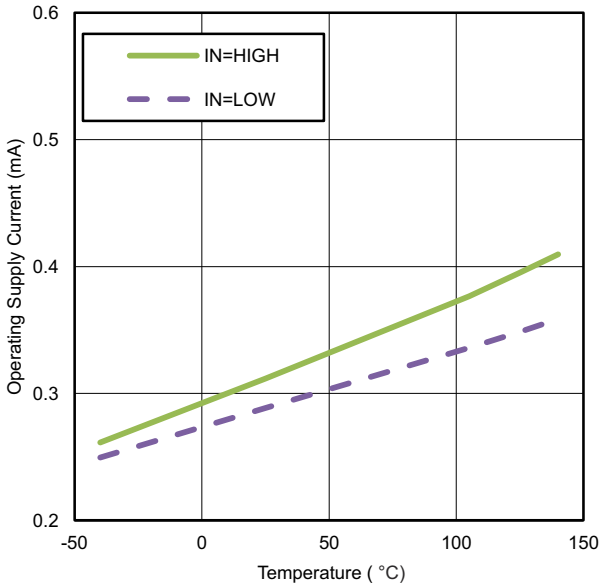


図 5-13. Operating Supply Current vs Temperature (output in DC on/off condition)

5.5 Typical Characteristics (continued)

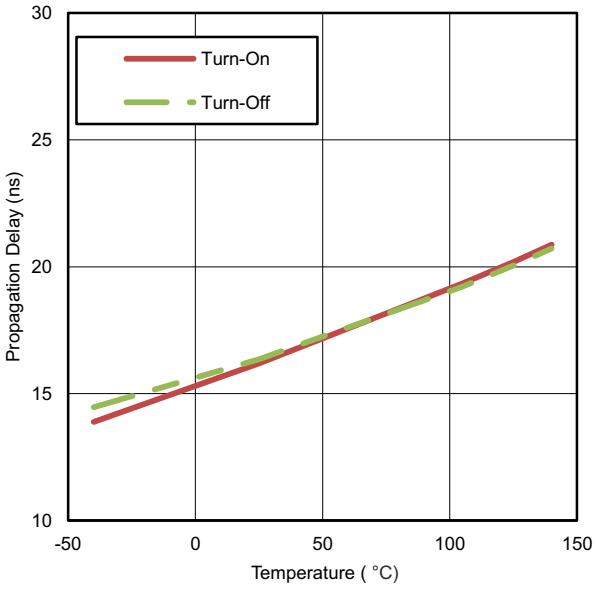


図 5-14. Input-to-Output Propagation Delay vs Temperature

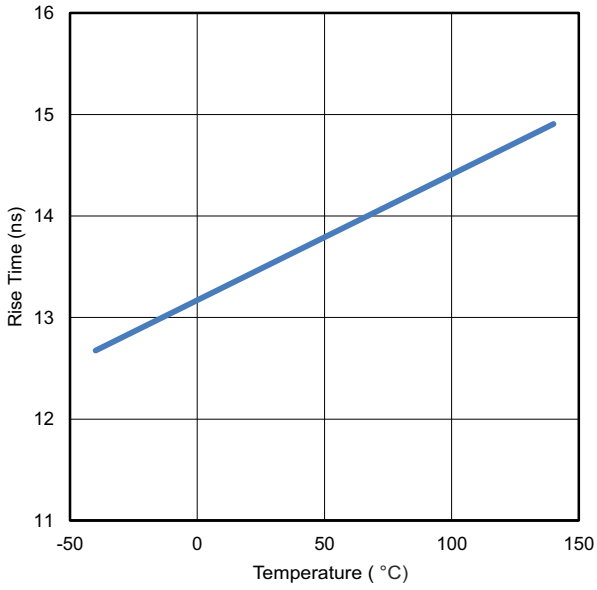


図 5-15. Rise Time vs Temperature

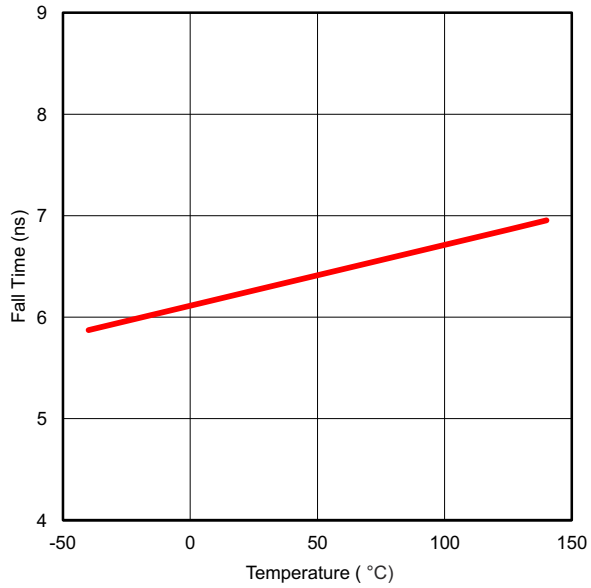


図 5-16. Fall Time vs Temperature

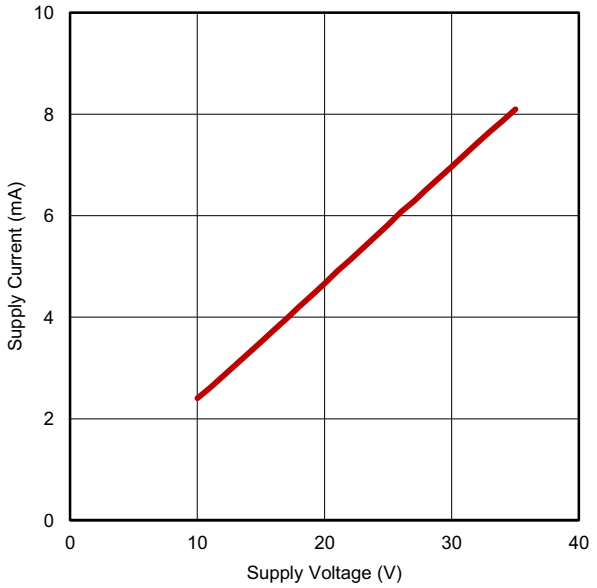


図 5-17. Operating Supply Current vs Supply Voltage (output switching)

5.5 Typical Characteristics (continued)

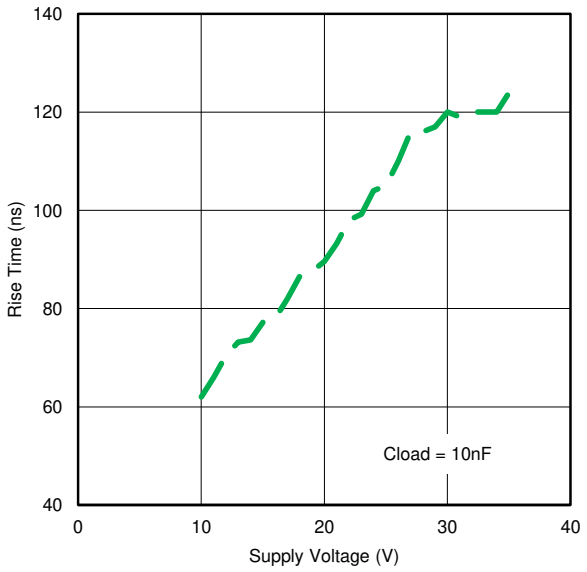


図 5-18. Rise Time vs Supply Voltage

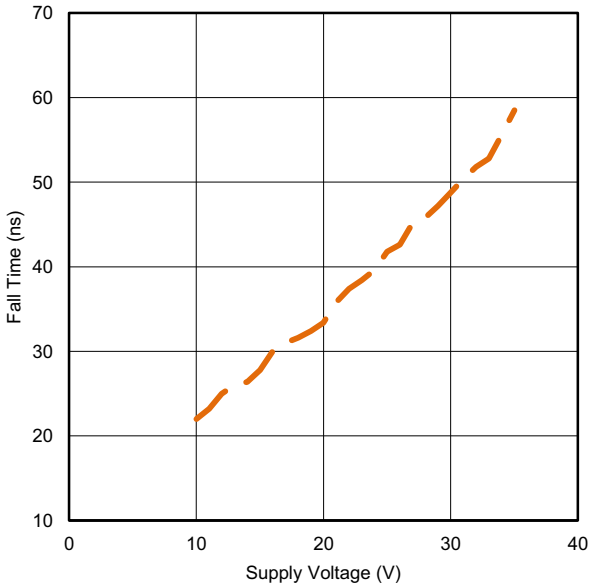
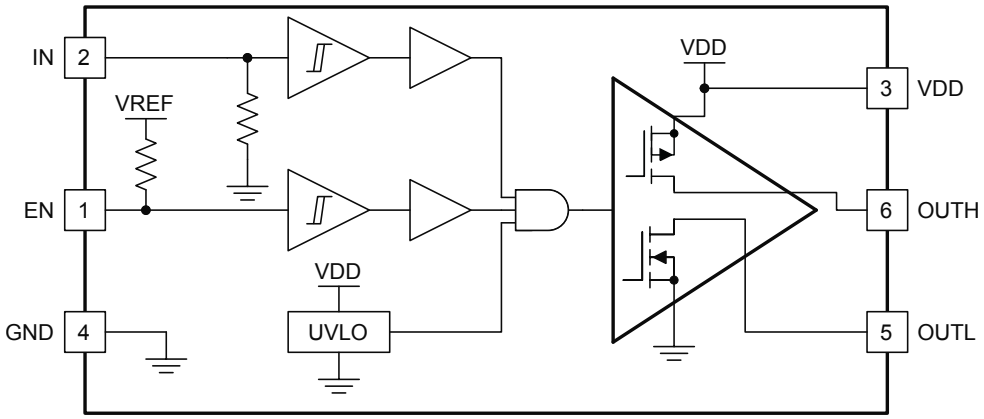


図 5-19. Fall Time vs Supply Voltage

6 Detailed Description

6.1 Functional Block Diagram

(EN Pull-Up Resistance to VREF = 500 kΩ, VREF = 5.8 V, In Pull-Down Resistance to GND = 230 kΩ)



6.2 Feature Description

6.2.1 VDD Under Voltage Lockout

The UCC27532 device has internal under voltage lockout (UVLO) protection feature on the VDD pin supply circuit blocks. To ensure acceptable power dissipation in the power switch, this UVLO prevents the operation of the gate driver at low supply voltages. Whenever the driver is in UVLO condition (when VDD voltage less than V_{ON} during power-up and when VDD voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 8.9 V with 700-mV typical hysteresis. This hysteresis helps prevent chatter when low VDD supply voltages have noise from the power supply and also when there are droops in the VDD bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at voltage levels such as 10 V to 32 V provides flexibility to drive Si MOSFETs, IGBTs, and emerging SiC FETs.

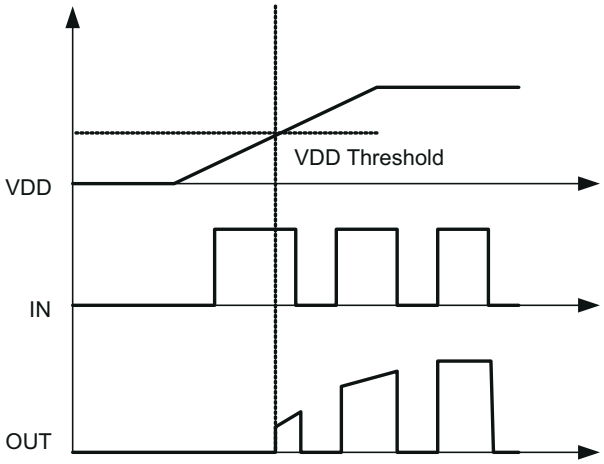


図 6-1. Power Up

6.2.2 Input Stage

The input pin of UCC27532 device is based on a standard CMOS compatible input threshold logic that is dependent on the VDD supply voltage. The input threshold is approximately 55% of VDD for rise and 45% of VDD for fall. With 18-V VDD, typical high threshold = 9.4 V and typical low threshold = 7.3 V. The 2.1-V hysteresis offers excellent noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. For proper operation using CMOS input, the input signal level should be at a voltage equal to VDD. Using an input signal slightly larger than the threshold but less than VDD for CMOS input can result in slower propagation delay from input to output for example. This device also features tight control of the input pin threshold voltage levels which eases system design considerations and guarantees stable operation across temperature. The very low input capacitance , typically 20 pF, on these pins reduces loading and increases switching speed.

The device features an important safety function wherein, whenever the input pin is in a floating condition, the output is held in the low state. This is achieved using GND pull-down resistors on the non-inverting input pin (IN pin), as shown in the device block diagram.

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly varying input signals, especially in situations where the device is located in a separate daughter board or PCB layout has long input connection traces:

- High dI/dt current from the driver output coupled with board layout parasitics can cause ground bounce. Since the device features just one GND pin which may be referenced to the power ground, this may interfere with the differential voltage between Input pins and GND and trigger an unintended change of output state. Because of fast 17 ns propagation delay, this can ultimately result in high-frequency oscillations, which increases power dissipation and poses risk of damage
- 2.1-V input threshold hysteresis boosts noise immunity compared to most other industry standard drivers.

If limiting the rise or fall times to the power device to reduce EMI is necessary, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

6.2.3 Enable Function

The Enable (EN) pin of the UCC27532 has an internal pull-up resistor to an internal reference voltage so leaving Enable floating turns on the driver and allows it to send output signals properly. If desired, the Enable can also be driven by low-voltage logic to enable and disable the driver.

6.2.4 Output Stage

The output stage of the UCC27532 device is illustrated in 図 6-2. The UCC27532 device features a unique architecture on the output stage which delivers the highest peak source current when it is most needed during the Miller plateau region of the power switch turn-on transition (when the power switch drain/collector voltage experiences dV/dt). The device output stage features a hybrid pull-up structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate driver device is able to deliver a brief boost in the peak sourcing current enabling fast turn on.

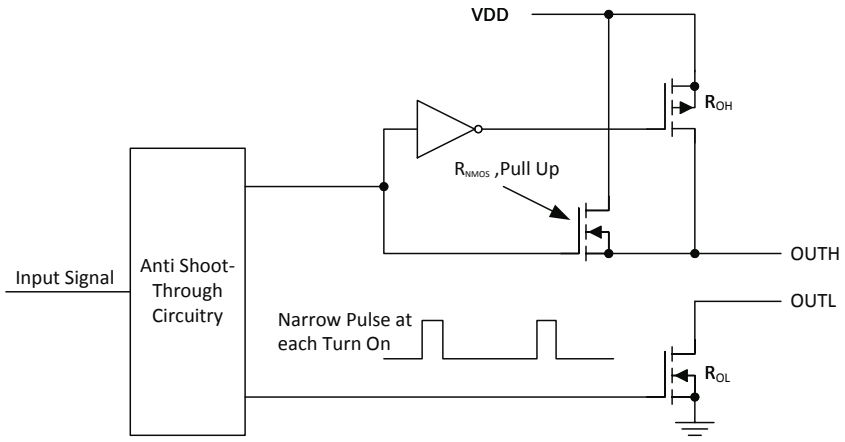


図 6-2. UCC27532 Gate Driver Output Stage

The R_{OH} parameter (see Electrical Table) is a DC measurement and it is representative of the on-resistance of the P-Channel device only, since the N-Channel device is turned-on only during output change of state from low to high. Thus the effective resistance of the hybrid pull-up stage is much lower than what is represented by ROH parameter. The pull-down structure is composed of a N-Channel MOSFET only. The ROL parameter (see セクション 5.4), which is also a DC measurement, is representative of true impedance of the pull-down stage in the device. In UCC27532, the effective resistance of the hybrid pull-up structure is approximately 3 x R_{OL}.

The UCC27532 is capable of delivering 2.5-A source, 5-A Sink (asymmetrical drive) at VDD = 18 V. Strong sink capability in asymmetrical drive results in a very low pull-down impedance in the driver output stage which boosts immunity against the parasitic Miller turn-on (high slew rate dV/dt turn on) effect that is seen in both IGBT and FET power switches .

An example of a situation where Miller turn on is a concern is synchronous rectification (SR). In SR application, the dV/dt occurs on MOSFET drain when the MOSFET is already held in Off state by the gate driver. The current charging the C_{GD} Miller capacitance during this high dV/dt is shunted by the pull-down stage of the driver. If the pull-down impedance is not low enough then a voltage spike can result in the V_{GS} of the MOSFET, which can result in spurious turn on. This phenomenon is illustrated in 図 6-3.

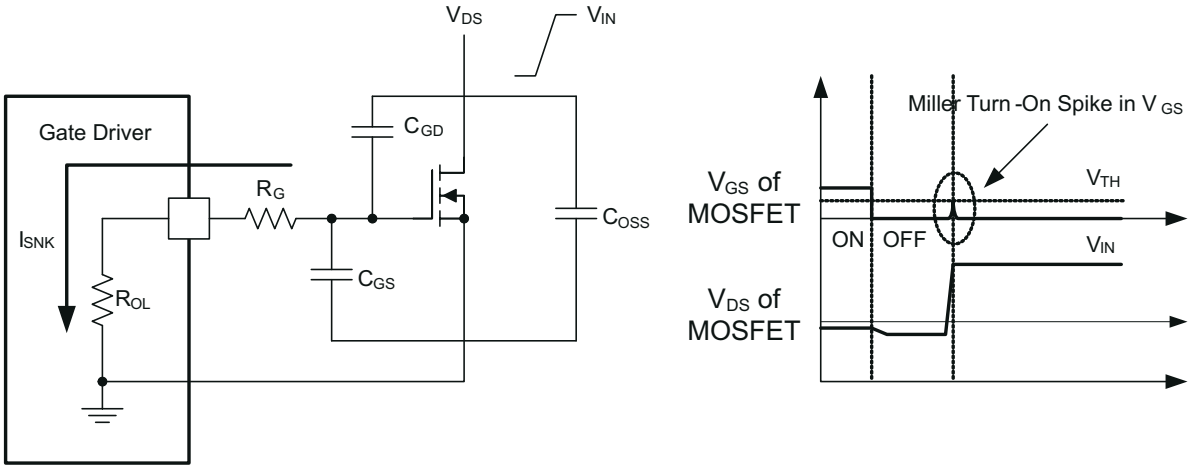


図 6-3. Low Pull-Down Impedance in UCC27532 (output stage mitigates Miller turn-on effect)

The driver output voltage swings between VDD and GND providing rail-to-rail operation, thanks to the MOS output stage which delivers very low dropout. The presence of the MOSFET body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky diode clamps may be eliminated.

6.2.5 Power Dissipation

Power dissipation of the gate driver has two portions as shown in equation below:

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

The DC portion of the power dissipation is $P_{DC} = I_Q$ x VDD where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections etc and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through). The UCC27532 features very low quiescent currents (less than 1 mA) and contains internal logic to eliminate any shoot-through in the output driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible. In practice this is the power consumed by driver when its output is disconnected from the gate of power switch.

The power dissipated in the gate driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \quad (2)$$

where

- C_{LOAD} is load capacitor and V_{DD} is bias voltage feeding the driver.

There is an equal amount of energy dissipated when the capacitor is discharged. During turn off the energy stored in capacitor is fully dissipated in drive circuit. This leads to a total power loss during switching cycle given by the following:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw} \quad (3)$$

where

- f_{SW} is the switching frequency

The switching load presented by a power FET and IGBT can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence, $Q_g = C_{LOAD} V_{DD}$, to provide the following equation for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{sw} = Q_g V_{DD} f_{sw} \quad (4)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET and IGBT is being turned on or off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turn-off. When no external gate resistor is employed between the driver and MOSFET and IGBT, this power is completely dissipated inside the driver

package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows:

$$P_{SW} = 0.5 \times Q_g \times V_{DD} \times f_{sw} \left(\frac{R_{OFF}}{(R_{OFF} + R_{GATE})} + \frac{R_{ON}}{(R_{ON} + R_{GATE})} \right) \quad (5)$$

where

- R_{OFF} = R_{OL} and R_{ON} (effective resistance of pull-up structure) = 3 x R_{OL}

6.3 Device Functional Modes

表 6-1. Input/Output Logic Truth Table

IN PIN	EN PIN	OUTH PIN	OUTL PIN	OUT (OUTH and OUTL pins tied together)
L	L	High-impedance	L	L
L	H	High-impedance	L	L
H	L	High-impedance	L	L
H	H	H	High-impedance	H

7 Application and Implementation

注

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7.1 Application Information

High-current gate driver devices are required in switching power applications for a variety of reasons. In order to enable fast switching of power devices and reduce associated switching power losses, a powerful gate driver can be employed between the PWM output of controllers or signal isolation devices and the gates of the power semiconductor devices. Further, gate drivers are indispensable when sometimes it is just not feasible to have the PWM controller directly drive the gates of the switching devices. The situation will be often encountered since the PWM signal from a digital controller or signal isolation device is often a 3.3-V or 5-V logic signal which is not capable of effectively turning on a power switch. A level shifting circuitry is needed to boost the logic-level signal to the gate-drive voltage in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar, (or p- n-channel MOSFET), transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate for this since they lack level-shifting capability and low-drive voltage protection. Gate drivers effectively combine both the level-shifting, buffer drive and UVLO functions. Gate drivers also find other needs such as minimizing the effect of switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses into itself.

The UCC27532 is very flexible in this role with a strong current drive capability and wide supply voltage range up to 35 V. This allows the driver to be used in 12-V Si MOSFET applications, 20-V and -5-V (relative to Source) SiC FET applications, 15-V and -15-V(relative to Emitter) IGBT applications and many others. As a single-channel driver, the UCC27532 can be used as a low-side or high-side driver. To use as a low-side driver, the switch ground is usually the system ground so it can be connected directly to the gate driver. To use as a high-side driver with a floating return node however, signal isolation is needed from the controller as well as an isolated bias to the UCC27532. Alternatively, in a high-side drive configuration the UCC27532 can be tied directly to the controller signal and biased with a non-isolated supply. However, in this configuration the outputs of the UCC27532 need to drive a pulse transformer which then drives the power-switch to work properly with the floating source and emitter of the power switch. Further, having the ability to control turn-on and turn-off speeds independently with both the OUTH and OUTL pins ensures optimum efficiency while maintaining system reliability. These requirements coupled with the need for low propagation delays and availability in compact, low-inductance packages with good thermal capability makes gate driver devices such as the UCC27532 extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction and simplified system design.

表 7-1. UCC27532 Features and Benefits

FEATURE	BENEFIT
High source and sink current capability, 2.5 A and 5 A (asymmetrical).	High current capability offers flexibility in employing UCC27532 device to drive a variety of power switching devices at varying speeds.
Low 17 ns (typ) propagation delay.	Extremely low pulse transmission distortion.
Wide VDD operating range of 10 V to 32 V.	Flexibility in system design.
	Can be used in split-rail systems such as driving IGBTs with both positive and negative(relative to Emitter) supplies.
	Optimal for many SiC FETs.
VDD UVLO protection.	Outputs are held Low in UVLO condition, which ensures predictable, glitch-free operation at power-up and power-down.
	High UVLO of 8.9V typical ensures that power switch is not on in high-impedance state which could result in high power dissipation or even failures.

表 7-1. UCC27532 Features and Benefits (続き)

FEATURE	BENEFIT
Outputs held low when input pin (IN) in floating condition.	Safety feature, especially useful in passing abnormal condition tests during safety certification
Split output structure (OUTH, OUTL).	Allows independent optimization of turn-on and turn-off speeds using series gate resistors.
Strong sink current (5 A) and low pull-down impedance (0.65 Ω).	High immunity to high dV/dt Miller turn-on events.
CMOS compatible input threshold logic with wide 2.1-V hysteresis.	Excellent noise immunity.
Input capable of withstanding -6.5 V.	Enhanced signal reliability in noisy environments that experience ground bounce on the gate driver.

7.2 Typical Applications

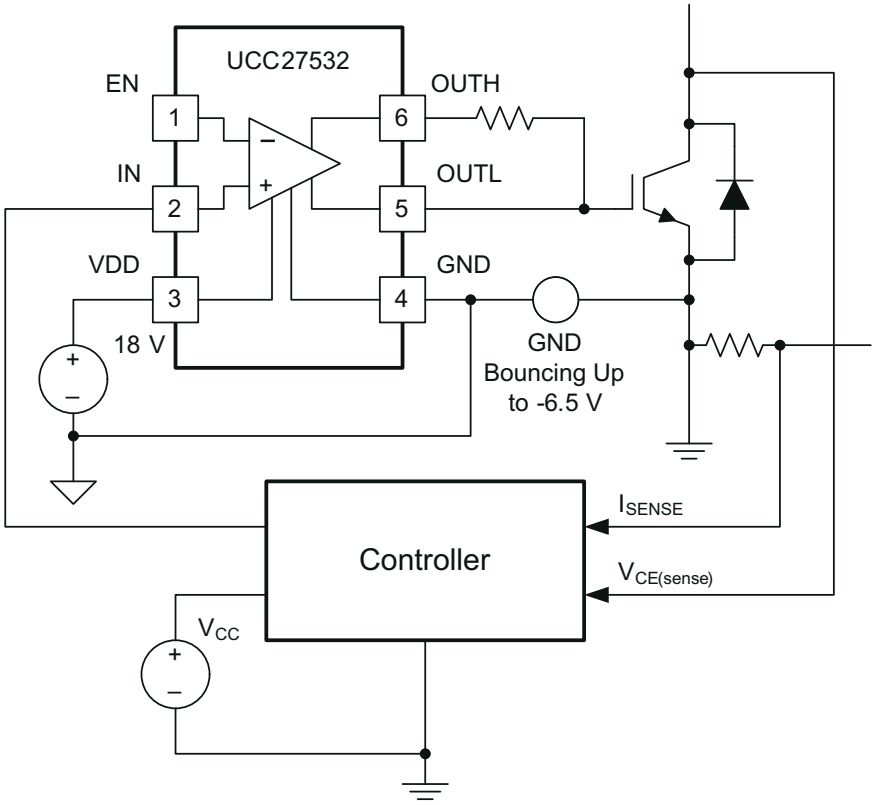

図 7-1. Driving IGBT Without Negative Bias

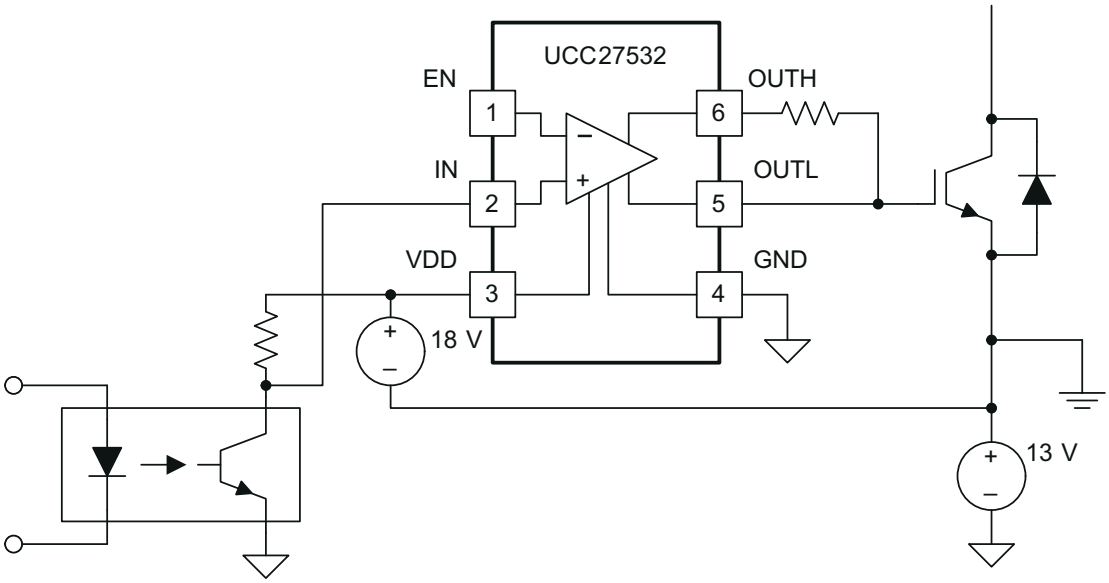

図 7-2. Driving IGBT With 13-V Negative Turn-Off Bias

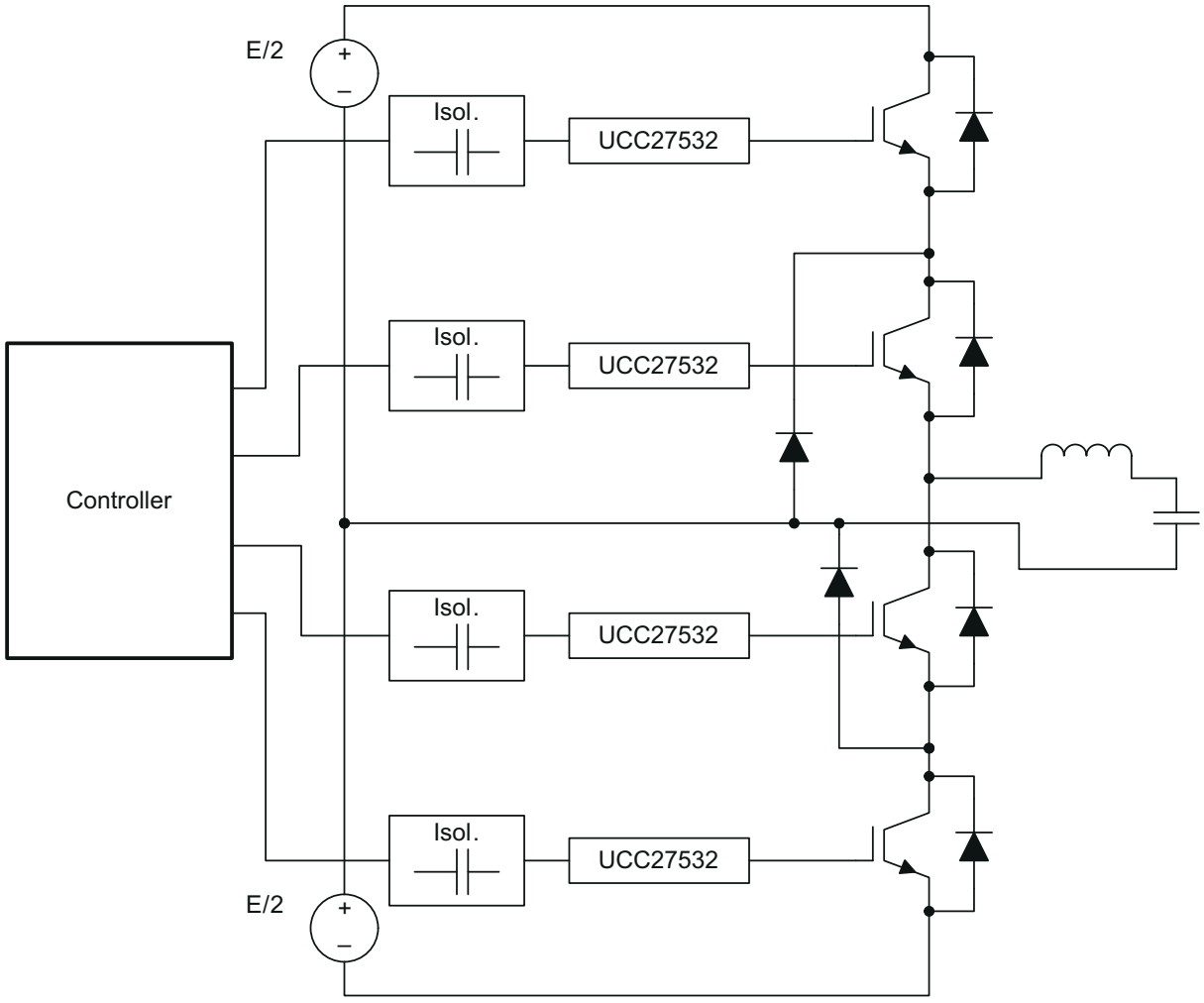

図 7-3. Using UCC27532 Drivers in an Inverter

8 Layout

8.1 Layout Guidelines

Proper PCB layout is extremely important in a high current, fast switching circuit to provide appropriate device operation and design robustness. The UCC27532 gate driver incorporates short propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak current capability is even higher (2.5-A and 5-A peak current is at VDD = 18 V). Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to power device in order to minimize the length of high-current traces between the driver Output pins and the gate of the power switch device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high peak current being drawn from VDD during turn-on of power switch. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turn-on and turn-off current loop paths (driver device, power switch and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High di/dt is established in these loops at two instances – during turn-on and turn-off transients, which induces significant voltage transients on the output pins of the driver device and gate of the power switch.
- Wherever possible, parallel the source and return traces of a current loop, taking advantage of flux cancellation
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch, ground of PWM controller etc at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

8.2 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in the ‘Thermal Information’ section of the datasheet. For detailed information regarding the thermal information table, please refer to Application Note from Texas Instruments entitled “IC Package Thermal Metrics” (SPRA953A).

9 Device and Documentation Support

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (February 2013) to Revision A (September 2024)	Page
• 「アプリケーション」のリンクを更新	1
• Added VDD = 16V to *Input (IN)* and *Enable (EN)* test conditions	5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC27532DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7532	Samples
UCC27532DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	7532	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC27532 :

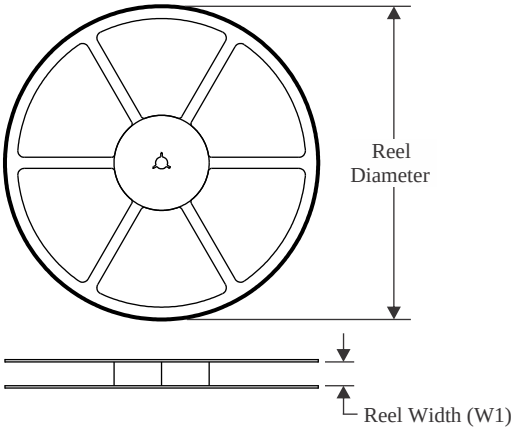
- Automotive : UCC27532-Q1

NOTE: Qualified Version Definitions:

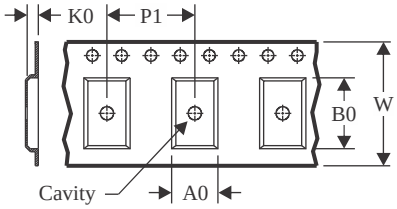
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

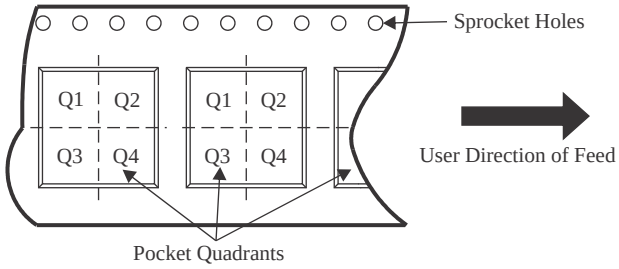


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

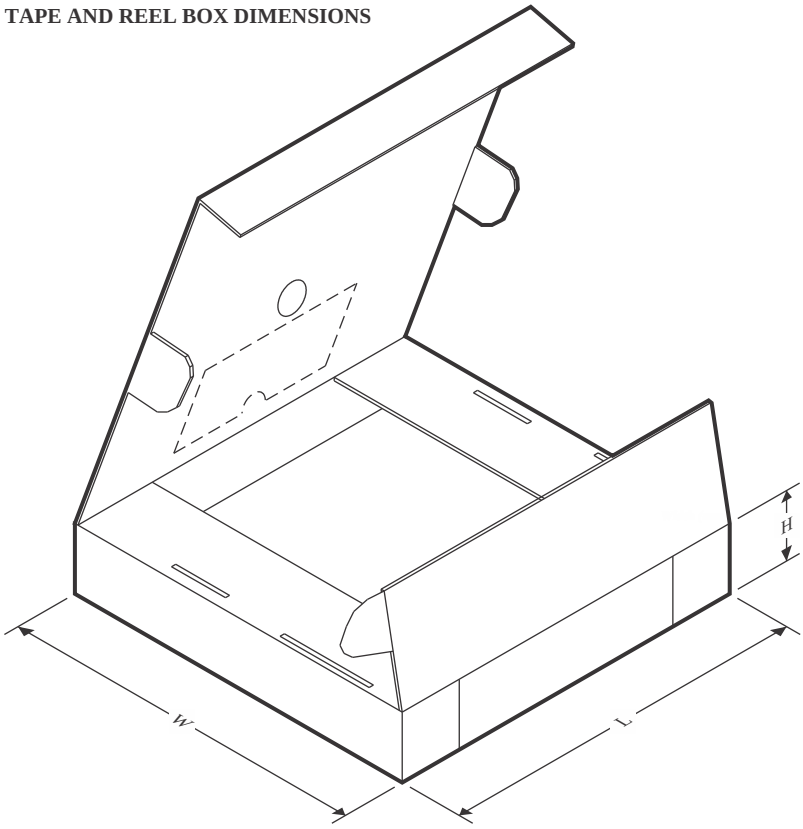
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27532DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
UCC27532DBVT	SOT-23	DBV	6	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

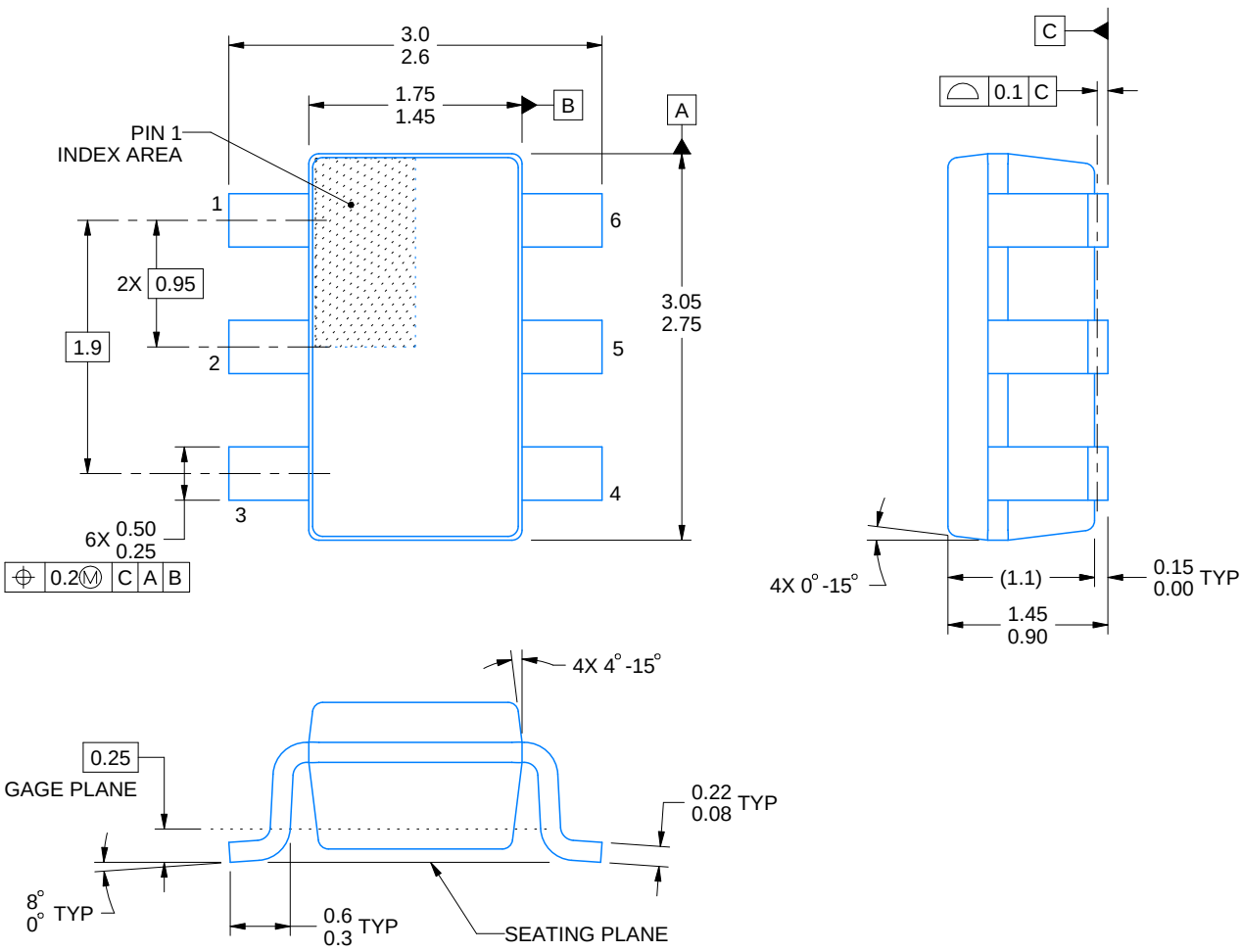
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27532DBVR	SOT-23	DBV	6	3000	200.0	183.0	25.0
UCC27532DBVT	SOT-23	DBV	6	250	200.0	183.0	25.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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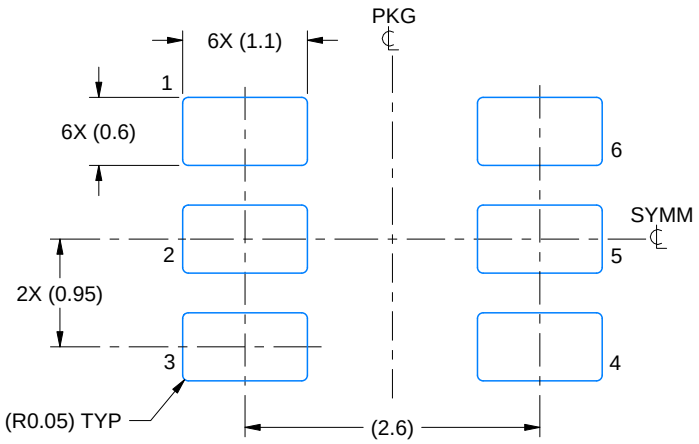
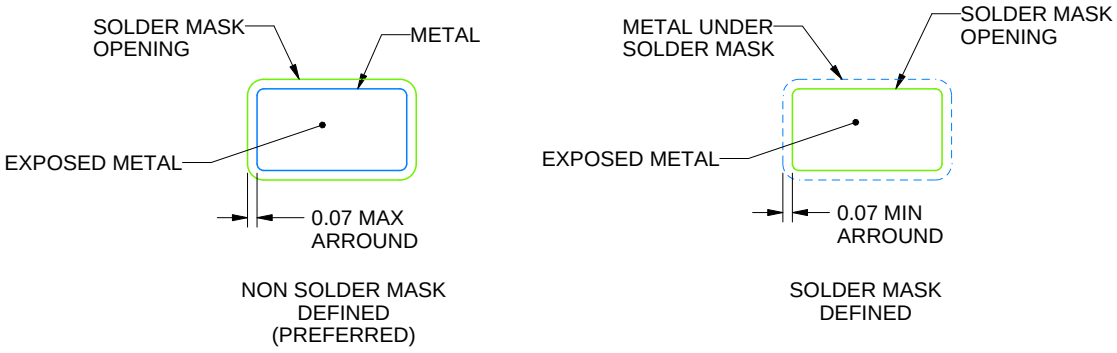
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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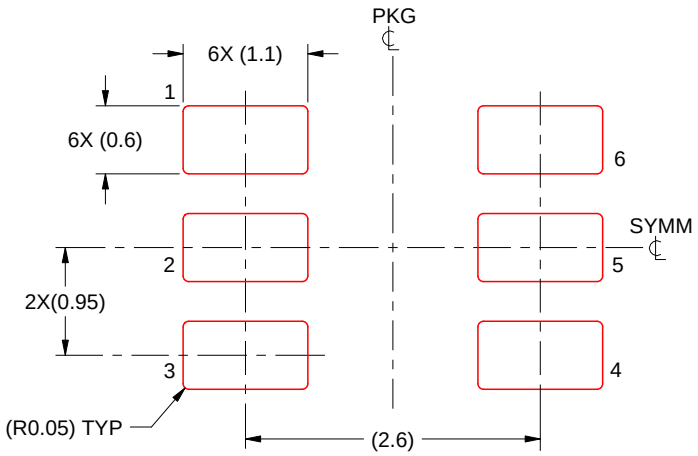
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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