TEXAS INSTRUMENTS
UCC44273
JAJSRJ4 – OCTOBER 2023

UCC44273 5V UVLO 搭載 4A/4A シングル・チャネル・ローサイド・ドライバ

1 特長

- 5 ピン DBV (SOT-23) パッケージ・オプション
- 業界標準のピン配置
- ソースおよびシンクの対称駆動ピーク電流：4A
- 負入力電圧 (-5V) に対応
- 高速伝搬遅延時間：13ns (標準値)
- 高速立ち上がり / 立ち下がり時間：9ns/7ns (標準値)
- シングル電源電圧範囲：4.5 ～ 18V
- VDD UVLO 時に出力を Low に保持 (パワーアップ / パワーダウン時のグリッチを防止)
- TTL および CMOS 互換の入力ロジック・スレッショルド (電源電圧に無関係)
- ヒステリシス付きのロジック・スレッショルドによる高いノイズ耐性
- 入力ピンのフローティング時は出力を Low に保持
- 入力ピンの絶対最大電圧レベルが VDD ピンのバイアス電源電圧に制限されない
- 動作温度範囲：-40℃～140℃

2 アプリケーション

- 力率改善 (PFC) ステージ
- 換気空調設備 (HVAC)
- スイッチモード電源
- モータ・ドライブ

3 説明

UCC44273 は、MOSFET および IGBT パワー・スイッチを効果的に駆動できるシングル・チャネル高速ローサイド・ゲート・ドライバです。本質的に貫通電流を最小限に抑える設計により、UCC44273 は、容量性負荷に対してソース/シンクともに高いピーク電流パルスを供給できます。また、レール・ツー・レールの駆動能力を持ち、伝搬遅延は標準 13ns と非常に小さくなっています。

UCC44273 デバイスは、入力ピンで -5V を処理できます。UCC44273 は、VDD = 12V でソースが 4A、シンクが 4A (対称駆動) のピーク駆動電流能力を備えています。

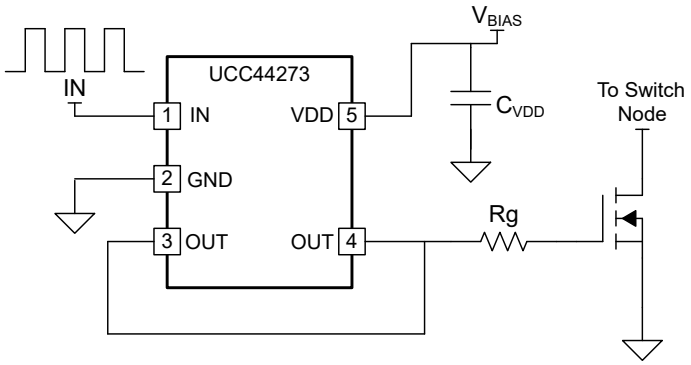
UCC44273 は、4.5 ～ 18V の広い VDD 範囲および -40°C～140°C の幅広い温度範囲で動作するよう設計されています。VDD ピンには内部に低電圧誤動作防止 (UVLO) 回路が搭載され、VDD が動作範囲外のときには出力を Low に保持します。

UCC44273 デバイスでは、入力ピンのスレッショルドが TTL および CMOS 互換の低電圧ロジックに基づき、VDD 電源電圧に依存しない固定値となっています。上限と下限のスレッショルド間に幅広いヒステリシスが設けられているため、優れたノイズ耐性が得られます。

製品情報

部品番号	パッケージ(1)	パッケージ・サイズ(2)	本体サイズ (公称)
UCC44273	DBV (SOT-23、5)	2.9mm × 2.8mm	2.90mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーションの図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
October 2023	*	Initial Release

5 Pin Configuration and Functions

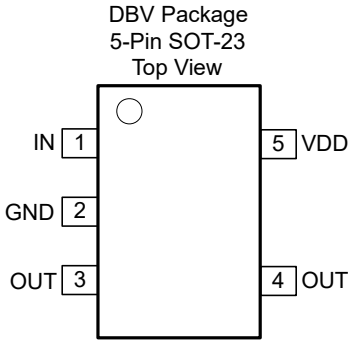


図 5-1. DBV Package 5-Pin SOT-23 Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Non-inverting PWM input.
2	GND	—	Ground. All signals reference to this pin.
3	OUT	O	Sourcing/sinking current output of driver. Pins 3 and 4 are internally connected.
4	OUT	O	Sourcing/sinking current output of driver. Pins 3 and 4 are internally connected.
5	VDD	I	Bias supply input.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	MAX	UNIT
Supply voltage	VDD	–0.3	20	V
OUT voltage	DC	–0.3	VDD + 0.3	V
	Repetitive pulse less than 200 ns(5)	–2	VDD + 0.3	
Output continuous current	I_{OUT_DC} (source/sink)		0.3	A
Output pulsed current (0.5 µs)	I_{OUT_pulsed}(source/sink)		4	
Input voltage	IN(4)	–6	20	V
Operating virtual junction temperature, T_J		–40	150	°C
Lead temperature	Soldering, 10 sec.		300	°C
	Reflow		260	
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.
(3) These devices are sensitive to electrostatic discharge; follow proper device-handling procedures.
(4) Maximum voltage on input pins is not restricted by the voltage on the VDD pin.
(5) Values are verified by characterization on bench.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage, V_{DD}	4.5	12	18	V
Operating junction temperature	–40		140	°C
Input voltage, IN	0		18	V

6.4 Thermal Information

THERMAL METRIC(1)		UCC44273 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	197.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	132.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	70.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	92.3	°C/W

6.4 Thermal Information (続き)

THERMAL METRIC[1]		UCC44273 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

VDD = 12 V, $T_A = T_J$ = –40°C to 140°C, 1-µF capacitor from VDD to GND. Currents are positive into, negative out of the specified terminal.

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
BIAS CURRENTS							
$I_{DD(off)}$	Startup current	VDD = 3.4 V	IN = VDD	40	100	160	µA
			IN = GND	20	60	115	
UNDER VOLTAGE LOCKOUT (UVLO)							
V_{ON}	Supply start threshold	T_A = 25°C		3.91	4.20	4.5	V
		T_A = -40°C to 140°C		3.70	4.20	4.65	
V_{OFF}	Minimum operating voltage after supply start			3.45	3.9	4.35	V
V_{DD_H}	Supply voltage hysteresis			0.2	0.3	0.5	V
INPUTS (IN)							
V_{IN_H}	Input signal high threshold	Output high for IN pin			2.2	2.4	V
V_{IN_L}	Input signal low threshold	Output low for IN pin		1.0	1.2		V
V_{IN_HYS}	Input signal hysteresis				1.0		V
SOURCE/SINK CURRENT							
$I_{SRC/SNK}$	Source/sink peak current	C_{LOAD} = 0.22 µF, F_{SW} = 1 kHz			±4		A
OUTPUTS (OUT)							
V_{DD}-V_{OH}	High output voltage	VDD = 12 V I_{OUT} = -10 mA			50	90	mV
		VDD = 4.5 V I_{OUT} = -10 mA			60	130	
V_{OL}	Low output voltage	VDD = 12 I_{OUT} = 10 mA			5	10	mV
		VDD = 4.5 V I_{OUT} = 10 mA			6	12	
R_{OH}	Output pullup resistance[1]	VDD = 12 V I_{OUT} = -10 mA			5.0	7.5	Ω
		VDD = 4.5 V I_{OUT} = -10 mA			5.0	11.0	
R_{OL}	Output pulldown resistance	VDD = 12 V I_{OUT} = 10 mA			0.5	1.0	Ω
		VDD = 4.5 V I_{OUT} = 10 mA			0.6	1.2	

(1) R_{OH} represents on-resistance of P-Channel MOSFET in pull-up structure of the UCC44273's output stage.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_R	Rise time(2)	VDD = 12 V C_{LOAD} = 1.8 nF		8	12	ns
		VDD = 4.5 V C_{LOAD} = 1.8 nF		16	22	
t_F	Fall time(2)	VDD = 12 V C_{LOAD} = 1.8 nF		7	11	ns
		VDD=4.5V C_{LOAD} = 1.8 nF		7	11	
t_{D1}	IN to output propagation delay(2)	VDD = 12 V 5-V input pulse C_{LOAD} = 1.8 nF	4	13	23	ns
		VDD = 4.5 V 5-V input pulse C_{LOAD} = 1.8 nF	4	13	26	

(1) Switching parameters are not tested in production.
(2) See timing diagram in 図 6-1.

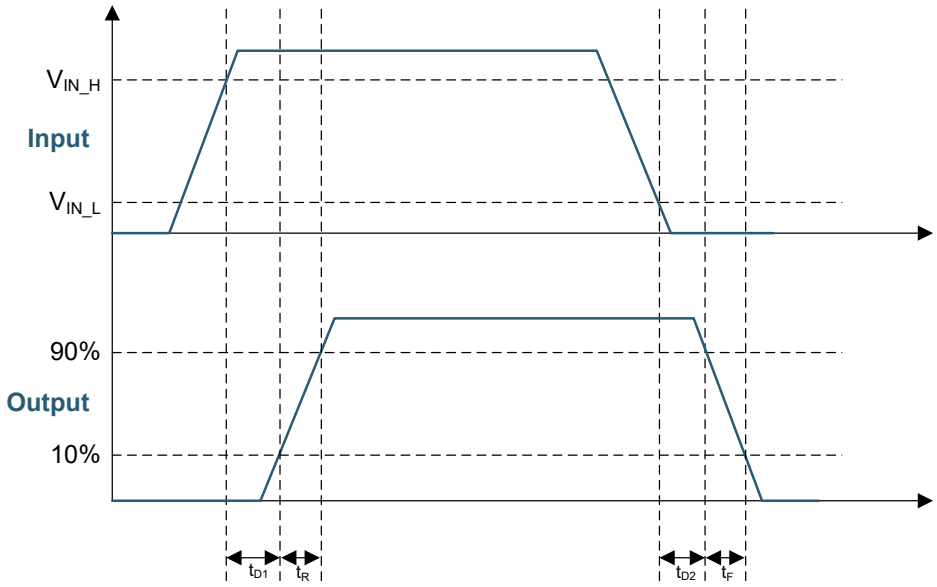


図 6-1. Non-Inverting Configuration (PWM Input to IN pin)

6.7 Typical Characteristics

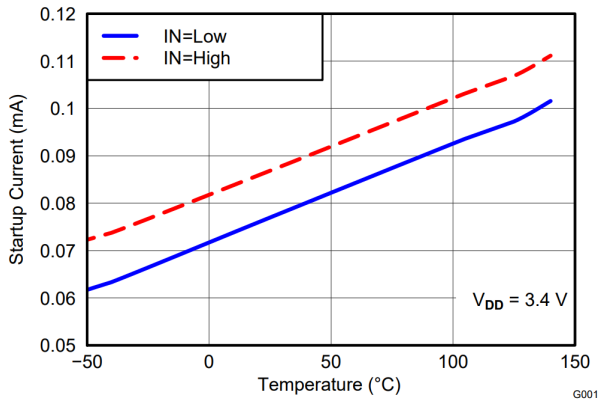


図 6-2. Start-Up Current vs Temperature

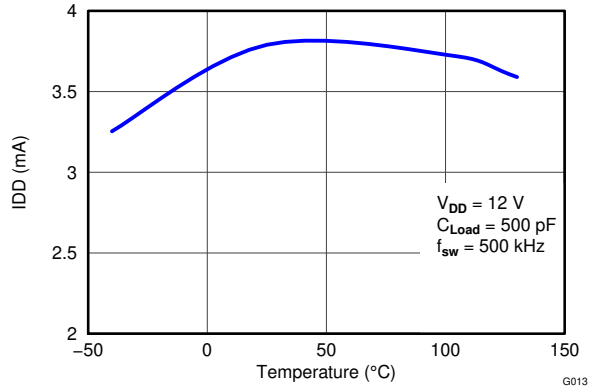


図 6-3. Operating Supply Current vs Temperature (Output Switching)

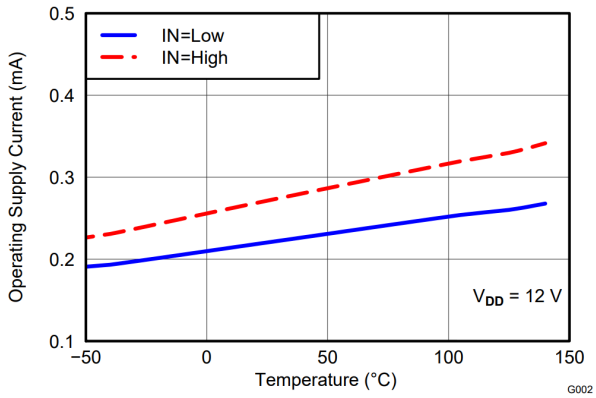


図 6-4. Supply Current vs Temperature (Output in DC ON/OFF Condition)

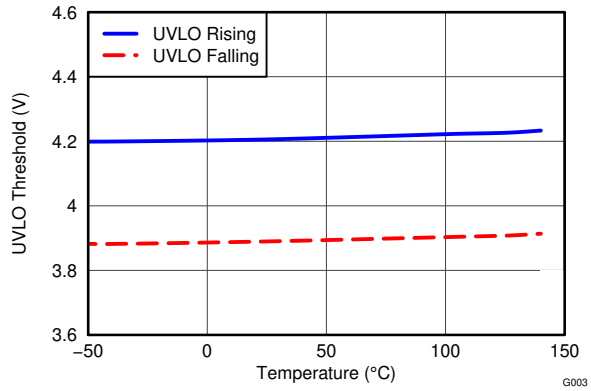


図 6-5. UVLO Threshold Voltage vs Temperature

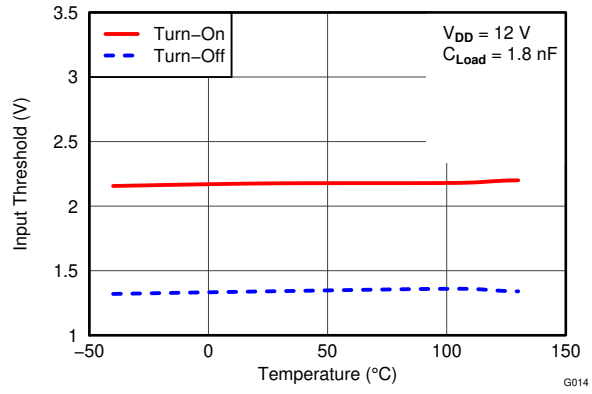


図 6-6. Input Threshold vs Temperature

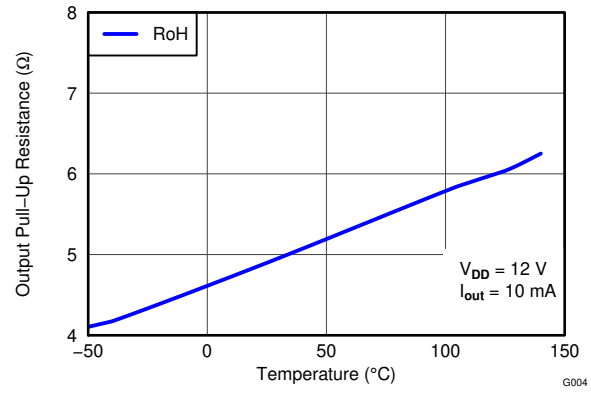


図 6-7. Output Pullup Resistance vs Temperature

6.7 Typical Characteristics (continued)

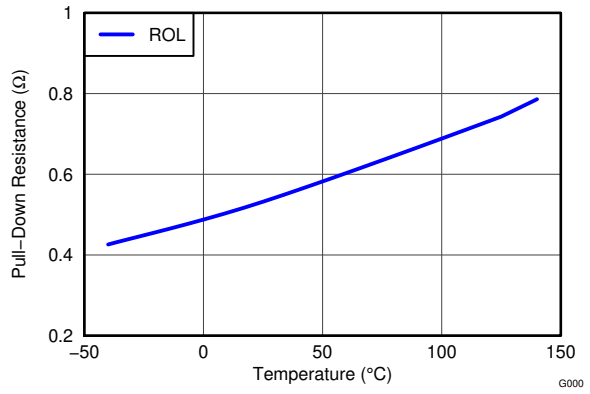


図 6-8. Output Pulldown Resistance vs Temperature

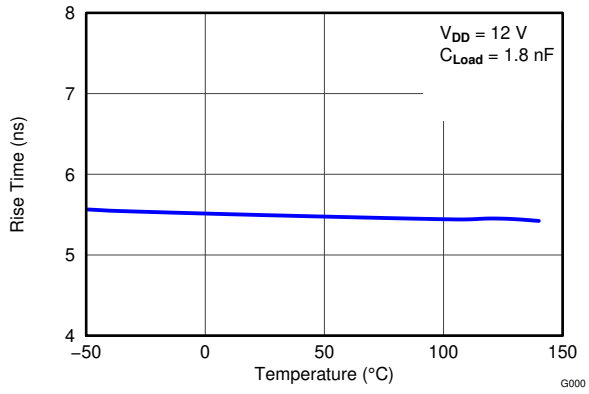


図 6-9. Rise Time vs Temperature

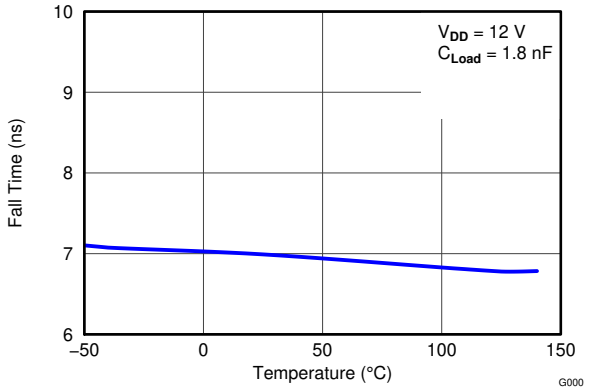


図 6-10. Fall Time vs Temperature

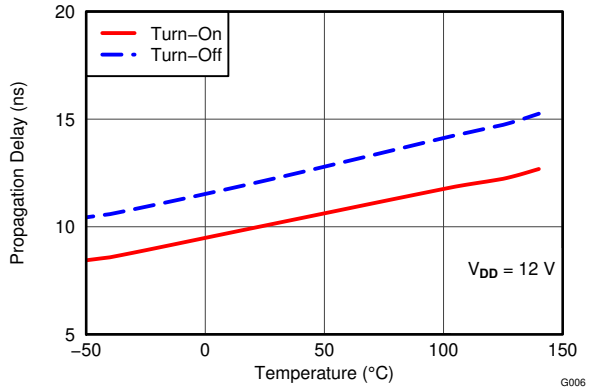


図 6-11. Input to Output Propagation Delay vs Temperature

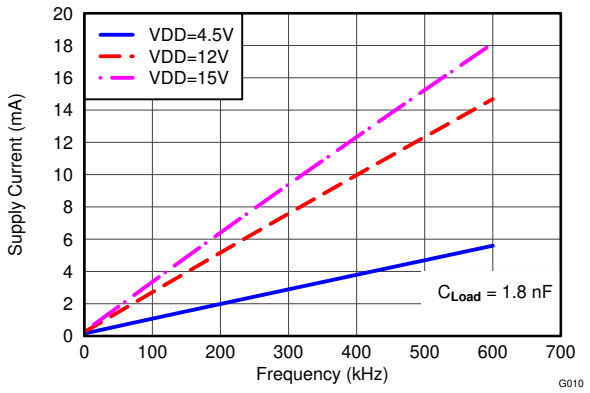


図 6-12. Operating Supply Current vs Frequency

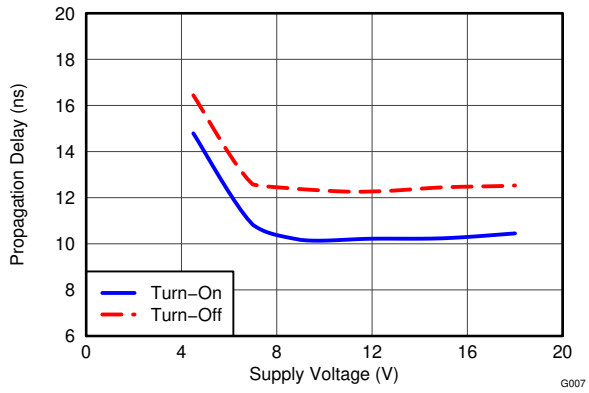


図 6-13. Propagation Delays vs Supply Voltage

6.7 Typical Characteristics (continued)

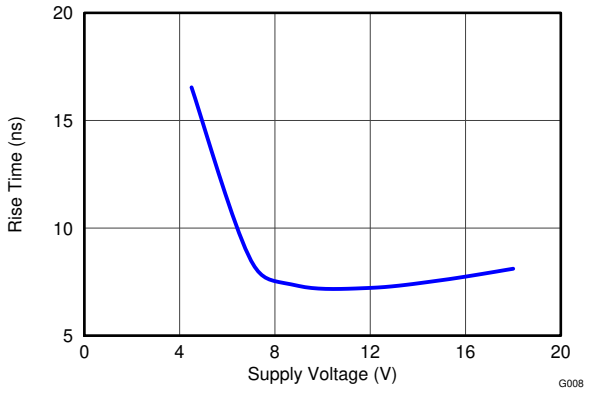


図 6-14. Rise Time vs Supply Voltage

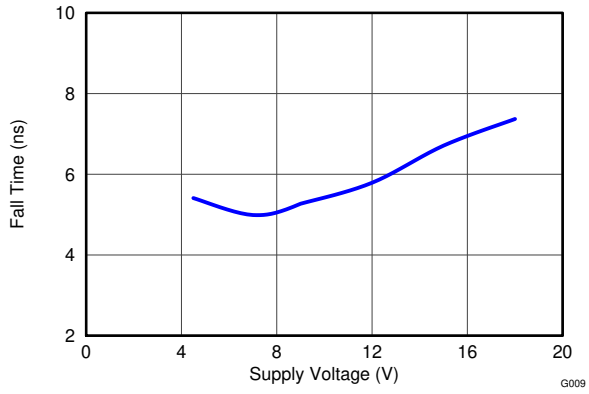


図 6-15. Fall Time vs Supply Voltage

7 Detailed Description

7.1 Overview

The UCC44273 single-channel, high-speed, low-side gate-driver device is capable of effectively driving MOSFET and IGBT power switches. Using a design that inherently minimizes shoot-through current, the UCC44273 device is capable of sourcing and sinking high peak-current pulses into capacitive loads offering rail-to-rail drive capability and extremely small propagation delay of 13 ns (typical). The UCC44273 provides 4-A source, 4-A sink (symmetrical drive) peak-drive current capability. The device is designed to operate over a wide V_{DD} range of 4.5 to 18 V, and a wide temperature range of –40°C to 140°C. Internal undervoltage lockout (UVLO) circuitry on the V_{DD} pin holds the output low outside V_{DD} operating range. The capability to operate at low voltage levels, such as below 5 V, along with best-in- class switching characteristics, is especially suited for driving emerging wide bandgap power-switching devices such as GaN power-semiconductor devices.

The input pin threshold of the UCC44273 device is based on TTL and CMOS-compatible low-voltage logic which is fixed and independent of the V_{DD} supply voltage. Wide hysteresis between the high and low thresholds offers excellent noise immunity.

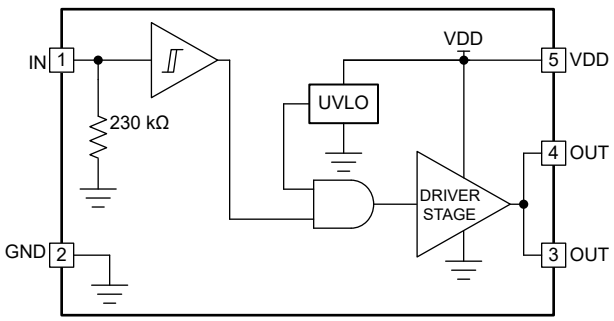
表 7-1. UCC44273 Summary

PART NUMBER	PACKAGE	PEAK CURRENT (SOURCE, SINK)	INPUT THRESHOLD LOGIC
UCC44273	SOT-23, 5 pin	4-A, 4-A (Symmetrical Drive)	CMOS and TTL-Compatible (low voltage, independent of V_{DD} bias voltage)

表 7-2. UCC44273 Features and Benefits

FEATURE	BENEFIT
High Source, Sink Current Capability 4 A, 4 A (Symmetrical)	High current capability offers flexibility in employing the UCC44273 to drive a variety of power switching devices at varying speeds
Best-in-class 13-ns (typ) Propagation delay	Extremely low-pulse transmission distortion
Expanded V_{DD} Operating range of 4.5 V to 18 V	Flexibility in system design Low V_{DD} operation ensures compatibility with emerging wide-bandgap power devices such as GaN
Expanded Operating Temperature range of –40°C to 140°C (See Recommended Operating Conditions table)	
V_{DD} UVLO Protection	Outputs are held low in UVLO condition, which ensures predictable glitch-free operation at power up and power down
Output held low when input pin (IN) in floating condition	Protection feature, especially useful in passing abnormal condition tests during protection certification
Ability of input pin to handle voltage levels not restricted by V_{DD} pin bias voltage	System simplification, especially related to auxiliary bias supply architecture
CMOS and TTL compatible input threshold logic with wide hysteresis in UCC44273	Enhanced noise immunity, while retaining compatibility with microcontroller logic-level input signals (3.3 V, 5 V) optimized for digital power
Ability to handle –5 V_{DC} at input pins	Increased robustness in noisy environments

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 V_{DD} and Undervoltage Lockout

The UCC44273 has internal Undervoltage Lockout (UVLO) protection feature on the V_{DD}-pin supply-circuit blocks. Whenever the driver is in UVLO condition (for example when V_{DD} voltage is less than V_{ON} during power up and when V_{DD} voltage is less than V_{OFF} during power down), this circuit holds all outputs LOW, regardless of the status of the inputs. The UVLO is typically 4.2 V with 300-mV typical hysteresis. This hysteresis helps prevent chatter when low V_{DD} – supply voltages have noise from the power supply and also when there are droops in the V_{DD}-bias voltage when the system commences switching and there is a sudden increase in I_{DD}. The capability to operate at low voltage levels such as below 5 V, along with best-in-class switching characteristics, is especially suited for driving emerging GaN wide-bandgap power-semiconductor devices.

For example, at power up, the UCC44273 driver output remains LOW until the V_{DD} voltage reaches the UVLO threshold. The magnitude of the OUT signal rises with V_{DD} until steady-state V_{DD} is reached. In the non-inverting operation (PWM signal applied to IN pin) shown in 図 7-1, the output remains LOW until the UVLO threshold is reached, and then the output is in-phase with the input. Note that in these devices the output turns to high-state only if IN pin is high after the UVLO threshold is reached.

Because the driver draws current from the V_{DD} pin to bias all internal circuits, for the best high-speed circuit performance, two V_{DD} bypass capacitors are recommended to prevent noise problems. The use of surface-mount components is highly recommended. A 0.1-µF ceramic capacitor should be located as close as possible to the V_{DD} to GND pins of the gate driver. In addition, a larger capacitor (such as 1 µF) with relatively low ESR should be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors should present a low impedance characteristic for the expected current levels and switching frequencies in the application.

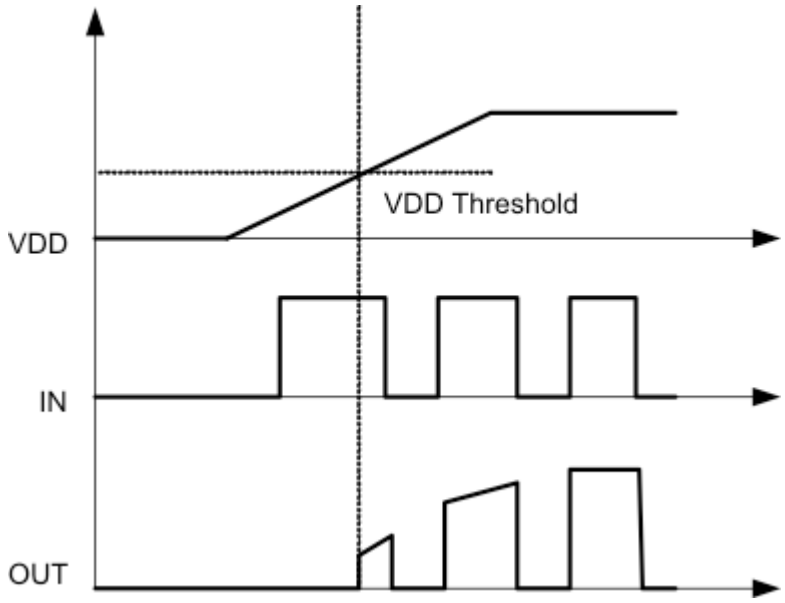


図 7-1. Power-Up (Non-Inverting Drive)

7.3.2 Operating Supply Current

The UCC44273 features very low quiescent I_{DD} currents. The typical operating-supply current in Undervoltage-Lockout (UVLO) state and fully-on state (under static and switching conditions) are summarized in 図 6-3, 図 6-3 and 図 6-4. The I_{DD} current when the device is fully on and outputs are in a static state (DC high or DC low, refer 図 6-2) represents lowest quiescent I_{DD} current when all the internal logic circuits of the device are fully operational. The total supply current is the sum of the quiescent I_{DD} current, the average I_{OUT} current due to

switching. Knowing the operating frequency (f_{SW}) and the MOSFET gate (Q_G) charge at the drive voltage being used, the average I_{OUT} current can be calculated as product of Q_G and f_{SW}.

A complete characterization of the I_{DD} current as a function of switching frequency at different V_{DD} bias voltages under 1.8-nF switching load is provided in 図 6-12. The strikingly-linear variation and close correlation with theoretical value of average I_{OUT} indicates negligible shoot-through inside the gate-driver device attesting to the high-speed characteristics of I_{OUT}.

7.3.3 Input Stage

The input pin of the UCC44273 is based on a TTL and CMOS compatible input-threshold logic that is independent of the V_{DD} supply voltage. With typical high threshold = 2.2 V and typ low threshold = 1.2 V, the logic-level thresholds can be conveniently driven with PWM-control signals derived from 3.3-V and 5-V digital-power controllers. Wider hysteresis (typically 1 V) offers enhanced noise immunity compared to traditional TTL-logic implementations, where the hysteresis is typically less than 0.5 V. These devices also feature tight control of the input-pin threshold-voltage levels which eases system-design considerations and ensures stable operation across temperature. The very low input capacitance on these pins reduces loading and increases switching speed.

The device features an important protection function wherein, whenever the input pin is in a floating condition, the output of the driver is held in the low state. This is achieved using GND-pulldown resistors on the non-inverting input pin (IN pin), (refer to セクション 7.2).

The input stage of the driver should preferably be driven by a signal with a short rise or fall time. Caution must be exercised whenever the driver is used with slowly-varying input signals, especially in situations where the device is located in a mechanical socket or PCB layout is not optimal:

- High dI/dt current from the driver output coupled with board layout parasitics causes ground bounce. Because the device features just one GND pin, which may be referenced to the power ground, the differential voltage between input pins and GND is modified and triggers an unintended change of output state. Because of fast 13-ns propagation delay, high-frequency oscillations ultimately occur, which increases power dissipation and poses risk of damage.
- 1-V input-threshold hysteresis boosts noise immunity compared to most other industry-standard drivers.
- In the worst case, when a slow input signal is used and PCB layout is not optimal, adding a small capacitor (1 nF) between input pin and ground very close to the driver device is necessary. This helps to convert the differential mode noise with respect to the input-logic circuitry into common-mode noise and avoid unintended change of output state.

If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device instead of adding delays on the input signal. This external resistor has the additional benefit of reducing part of the gate charge related power dissipation in the gate-driver device package and transferring the gate driver into the external resistor.

7.3.4 Output Stage

The UCC44273 is capable of delivering 4-A source, 4-A sink (symmetrical drive) at V_{DD} = 12 V. The output stage of the UCC44273 device is illustrated in 図 7-2. The UCC44273 features a unique architecture on the output stage which delivers the highest peak-source current when most needed during the Miller-plateau region of the power-switch turnon transition (when the power-switch drain/collector voltage experiences dV/dt). The device output stage features a hybrid pullup structure using a parallel arrangement of N-Channel and P-Channel MOSFET devices. By turning on the N-Channel MOSFET during a narrow instant when the output changes state from low to high, the gate-driver device delivers a brief boost in the peak-sourcing current enabling fast turnon.

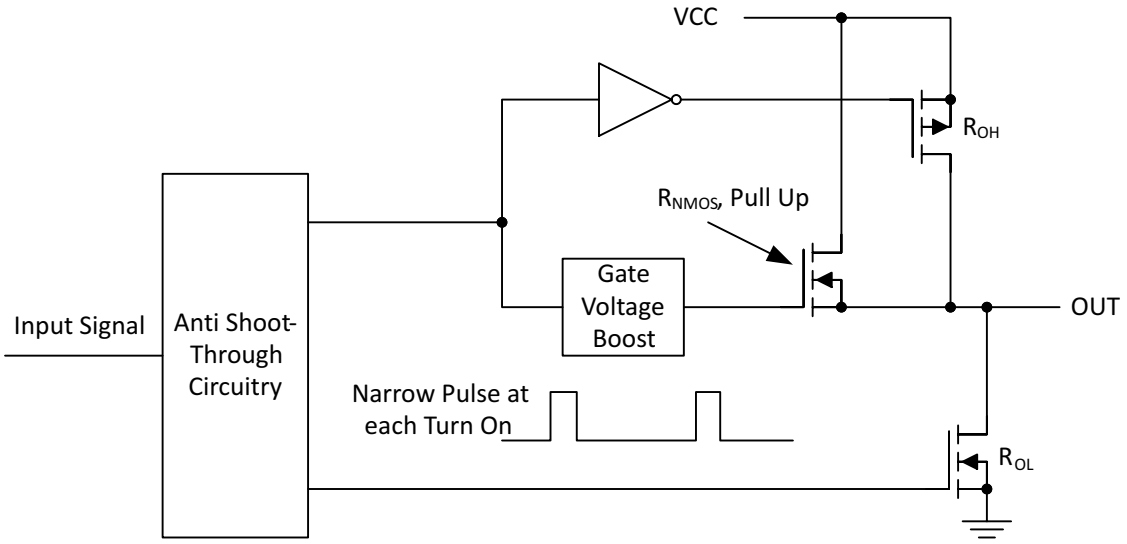


図 7-2. UCC44273 Gate Driver Output Structure

The R_{OH} parameter (see セクション 6.5) is a DC measurement and is representative of the on-resistance of the P-Channel device only, since the N-Channel device is turned on only during output change of state from low to high. Thus the effective resistance of the hybrid pullup stage is much lower than what is represented by R_{OH} parameter. The pulldown structure is composed of a N-Channel MOSFET only. The R_{OL} parameter (see セクション 6.5), which is also a DC measurement, is representative of true impedance of the pulldown stage in the device. In the UCC44273, the effective resistance of the hybrid pullup structure is approximately 1.4 × R_{OL}.

The driver-output voltage swings between V_{DD} and GND providing rail-to-rail operation because of the MOS output stage which delivers very low dropout. The presence of the MOSFET-body diodes also offers low impedance to switching overshoots and undershoots. This means that in many cases, external Schottky-diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

7.3.5 Low Propagation Delays

The UCC44273 features best-in-class input-to-output propagation delay of 13 ns (typ) at V_{DD} = 12 V. This promises the lowest level of pulse-transmission distortion available from industry-standard gate-driver devices for high-frequency switching applications. As seen in 図 6-11, there is very little variation of the propagation delay with temperature and supply voltage as well, offering typically less than 20-ns propagation delays across the entire range of application conditions.

7.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See セクション 7.3.1 for information on UVLO operation mode. In the normal mode the output state is dependent on the state of the IN pin. 表 7-3 below lists the output states for different input pin combinations.

表 7-3. Device Logic Table

IN PIN	OUT PIN
L	L
H	H
x(1)	L

(1) x = Floating Condition

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

High-current gate-driver devices are required in switching power applications for a variety of reasons. In order to effect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power-semiconductor devices. Further, gate drivers are indispensable when there are times that the PWM controller cannot directly drive the gates of the switching devices. With advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal, which is not capable of effectively turning on a power switch. A level-shifting circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Because traditional buffer-drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter-follower configurations, lack level-shifting capability, the circuits prove inadequate with digital power.

Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate-charge power losses into itself. Finally, emerging wide-bandgap power-device technologies, such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving very special requirements in terms of gate-drive capability. These requirements include operation at low V_{DD} voltages (5 V or lower), low propagation delays and availability in compact, low-inductance packages with good thermal capability. In summary gate-driver devices are extremely important components in switching power combining benefits of high-performance, low cost, component count and board space reduction with a simplified system design.

8.2 Typical Application

Typical application diagram for the UCC44273 device is shown in 図 8-1 to illustrate use in non-inverting and inverting driver configurations.

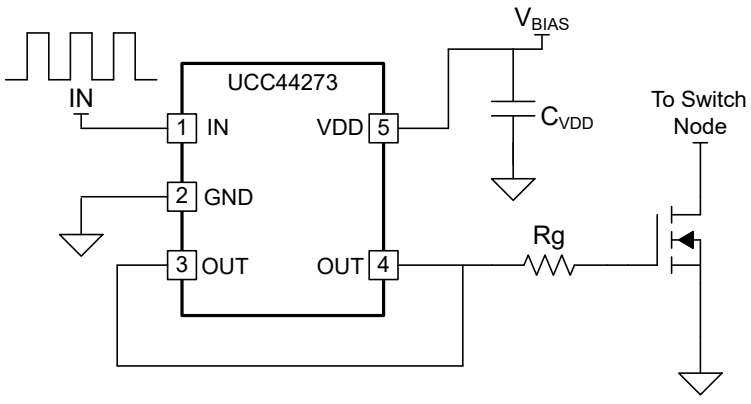


図 8-1. Typical Application

8.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some design considerations must be evaluated first to make the most appropriate selection. Among these considerations are input-to-output configuration, the input threshold type, bias supply voltage levels, peak source and sink currents, propagation delay, power dissipation, and package type.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input-to-Output Logic	Non-Inverting
Input Threshold Type	Logic Level
V_{DD} Bias Supply Voltage	10 V (minimum), 13 V (nominal), 15 V (peak)
Peak Source and Sink Currents	Minimum 3 A Source, Minimum 3 A Sink
Propagation Delay	Maximum 40 ns or Less

8.2.2 Detailed Design Procedure

8.2.2.1 Input Threshold Type

The type of input voltage threshold determines the type of controller used with the gate driver device. The UCC44273 device features a TTL and CMOS-compatible input threshold logic, with wide hysteresis. The threshold voltage levels are low voltage and independent of the V_{DD} supply voltage, which allows compatibility with both logic-level input signals from microcontrollers, as well as higher-voltage input signals from analog controllers. See セクション 6.3 for the actual input threshold voltage levels and hysteresis specifications for the UCC44273 device.

8.2.2.2 V_{DD} Bias Supply Voltage

The bias supply voltage to be applied to the V_{DD} pin of the device should never exceed the values listed in the セクション 6.3 table. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turnon and turnoff. With certain power switches, a positive gate voltage may be required for turnon and a negative gate voltage may be required for turnoff, in which case the V_{DD} bias supply equals the voltage differential. With a wide operating range from 4.5 V to 18 V, the UCC44273 device can be used to drive a variety of power switches, such as Si MOSFETs (for example, VGS = 4.5 V, 10 V, 12 V), IGBTs (VGE = 15 V, 18 V), and wide-band gap power semiconductors (such as GaN, certain types of which allow no higher than 6 V to be applied to the gate terminals).

8.2.2.3 Peak Source and Sink Currents

Generally, the switching speed of the power switch during turnon and turnoff should be as fast as possible, to minimize switching power losses. The gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power MOSFET.

Using the example of a power MOSFET, the system requirement for the switching speed is typically described in terms of the slew rate of the drain-to-source voltage of the power MOSFET (such as dV DS /dt). For example, the system requirement might state that a SPP20N60C3 power MOSFET must be turned-on with a dV DS /dt of 20V/ns or higher, under a DC bus voltage of 400 V in a continuous-conduction-mode (CCM) boost PFC-converter application. This type of application is an inductive hard-switching application and reducing switching power losses is critical. This requirement means that the entire drain-to-source voltage swing during power MOSFET turnon event (from 400 V in the OFF state to V DS(on) in on state) must be completed in approximately 20 ns or less.

When the drain-to-source voltage swing occurs, the Miller charge of the power MOSFET (QGD parameter in SPP20N60C3 power MOSFET data sheet = 33 nC typical) is supplied by the peak current of gate driver. According to the power MOSFET inductive switching mechanism, the gate-to-source voltage of the power MOSFET at this time is the Miller plateau voltage, which is typically a few volts higher than the threshold voltage of the power MOSFET, VGS(TH). To achieve the targeted dV DS /dt, the gate driver must be capable of

providing the QGD charge in 20 ns or less. In other words, a peak current of 1.65 A (= 33 nC / 20 ns) or higher must be provided by the gate driver. The UCC44273 gate driver is capable of providing 4-A peak sourcing current, which exceeds the design requirement and has the capability to meet the switching speed needed.

The 2.4x overdrive capability provides an extra margin against part-to-part variations in the QGD parameter of the power MOSFET, along with additional flexibility to insert external gate resistors and fine tune the switching speed for efficiency versus EMI optimizations. However, in practical designs the parasitic trace inductance in the gate drive circuit of the PCB will have a definitive role to play on the power MOSFET switching speed. The effect of this trace inductance is to limit the dI/dt of the output current pulse of the gate driver.

To illustrate this, consider output current pulse waveform from the gate driver to be approximated to a triangular profile, where the area under the triangle (½ × I PEAK × time) would equal the total gate charge of the power MOSFET (QG parameter in SPP20N60C3 power MOSFET datasheet = 87 nC typical).

If the parasitic trace inductance limits the dI/dt, then a situation may occur in which the full peak current capability of the gate driver is not fully achieved in the time required to deliver the QG required for the power MOSFET switching. In other words, the time parameter in the equation would dominate and the I PEAK value of the current pulse would be much less than the true peak current capability of the device, while the required QG is still delivered. Because of this, the desired switching speed may not be realized, even when theoretical calculations indicate the gate driver is capable of achieving the targeted switching speed. Thus, placing the gate driver device very close to the power MOSFET and designing a tight gate drive-loop with minimal PCB trace inductance is important to realize the full peak-current capability of the gate driver.

8.2.2.4 Propagation Delay

The acceptable propagation delay from the gate driver is dependent on the switching frequency at which it is used, and the acceptable level of pulse distortion to the system. The UCC44273 device features industry best-in-class 13-ns (typical) propagation delays, which ensure very little pulse distortion and allow operation at very high-frequencies. See セクション 6.6 for the propagation and switching characteristics of the UCC44273 device.

8.2.3 Application Curves

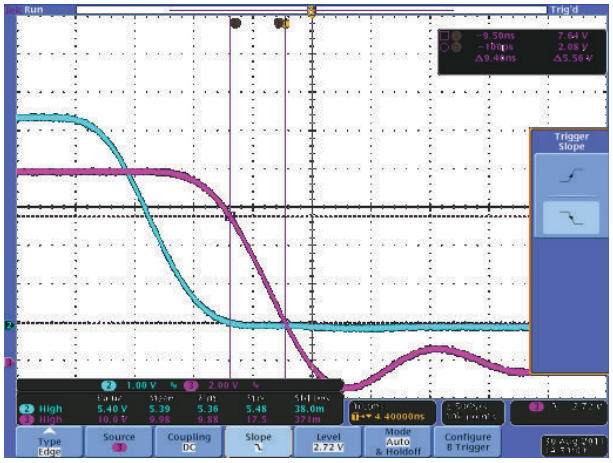


図 8-2. Typical Turnon Waveform

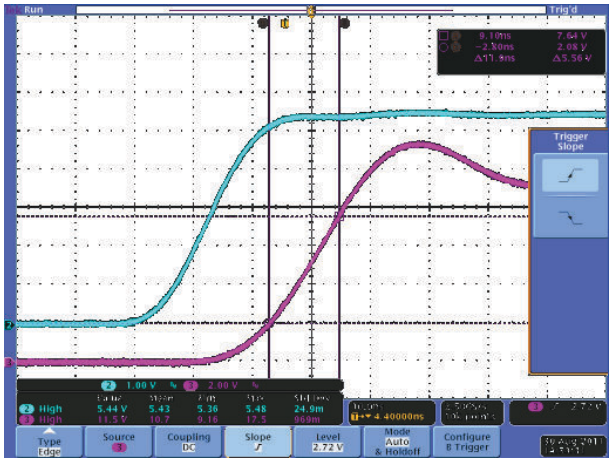


図 8-3. Typical Turnoff Waveform

8.3 Power Supply Recommendations

The bias supply voltage range for which the UCC44273 device is rated to operate is from 4.5 V to 18 V. The lower end of this range is governed by the internal UVLO protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the V_{DD} pin voltage is below the V(ON) supply start threshold, this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20-V absolute maximum voltage rating of the V_{DD} pin of the device (which is a stress rating). Keeping a 2-V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 18 V.

The UVLO protection feature also involves a hysteresis function. This means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and the device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification $V_{DD(hys)}$. While operating at or near the 4.5 V range, ensure that the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device, to avoid triggering a device shutdown.

During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below the $V_{(OFF)}$ threshold, which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system startup the device does not begin operation until the V_{DD} pin voltage has exceeded above the $V_{(ON)}$ threshold. The quiescent current consumed by the internal circuit blocks of the device is supplied through the V_{DD} pin. Keep in mind that the charge for source current pulses delivered by the OUT pin is also supplied through the same V_{DD} pin. As a result, every time a current is sourced out of the output pin (OUT), a corresponding current pulse is delivered into the device through the V_{DD} pin. Therefore, ensure that local bypass capacitors are provided between the V_{DD} and GND pins, and located as close to the device as possible for the purpose of decoupling. A low ESR, ceramic surface mount capacitor is necessary. TI recommends using 2 capacitors; a 100-nF ceramic surface-mount capacitor which can be nudged very close to the pins of the device, and another surface-mount capacitor of few microfarads added in parallel.

8.4 Layout

8.4.1 Layout Guidelines

Proper PCB layout is extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. The UCC44273 gate driver incorporates short-propagation delays and powerful output stages capable of delivering large current peaks with very fast rise and fall times at the gate of the power switch to facilitate voltage transitions very quickly. At higher VDD voltages, the peak-current capability is even higher (4-A/4-A peak current is at VDD = 12 V). Very high di/dt causes unacceptable ringing if the trace lengths and impedances are not well controlled. The following circuit layout guidelines are strongly recommended when designing with these high-speed drivers.

- Locate the driver device as close as possible to the power device in order to minimize the length of high-current traces between the output pins and the gate of the power device.
- Locate the VDD bypass capacitors between VDD and GND as close as possible to the driver with minimal trace length to improve the noise filtering. These capacitors support high-peak current being drawn from VDD during turnon of power MOSFET. The use of low inductance SMD components such as chip resistors and chip capacitors is highly recommended.
- The turnon and turnoff current-loop paths (driver device, power MOSFET and VDD bypass capacitor) should be minimized as much as possible in order to keep the stray inductance to a minimum. High dI/dt is established in these loops at two instances – during turnon and turnoff transients, which will induce significant voltage transients on the output pin of the driver device and gate of the power switch.
- Wherever possible parallel the source and return traces, taking advantage of flux cancellation.
- Separate power traces and signal traces, such as output and input signals.
- Star-point grounding is a good way to minimize noise coupling from one current loop to another. The GND of the driver should be connected to the other circuit nodes such as source of power switch or the ground of PWM controller at one, single point. The connected paths should be as short as possible to reduce inductance and be as wide as possible to reduce resistance.
- Use a ground plane to provide noise shielding. Fast rise and fall times at OUT may corrupt the input signals during transition. The ground plane must not be a conduction path for any current loop. Instead the ground plane must be connected to the star-point with one single trace to establish the ground potential. In addition to noise shielding, the ground plane can help in power dissipation as well.

8.4.2 Layout Example

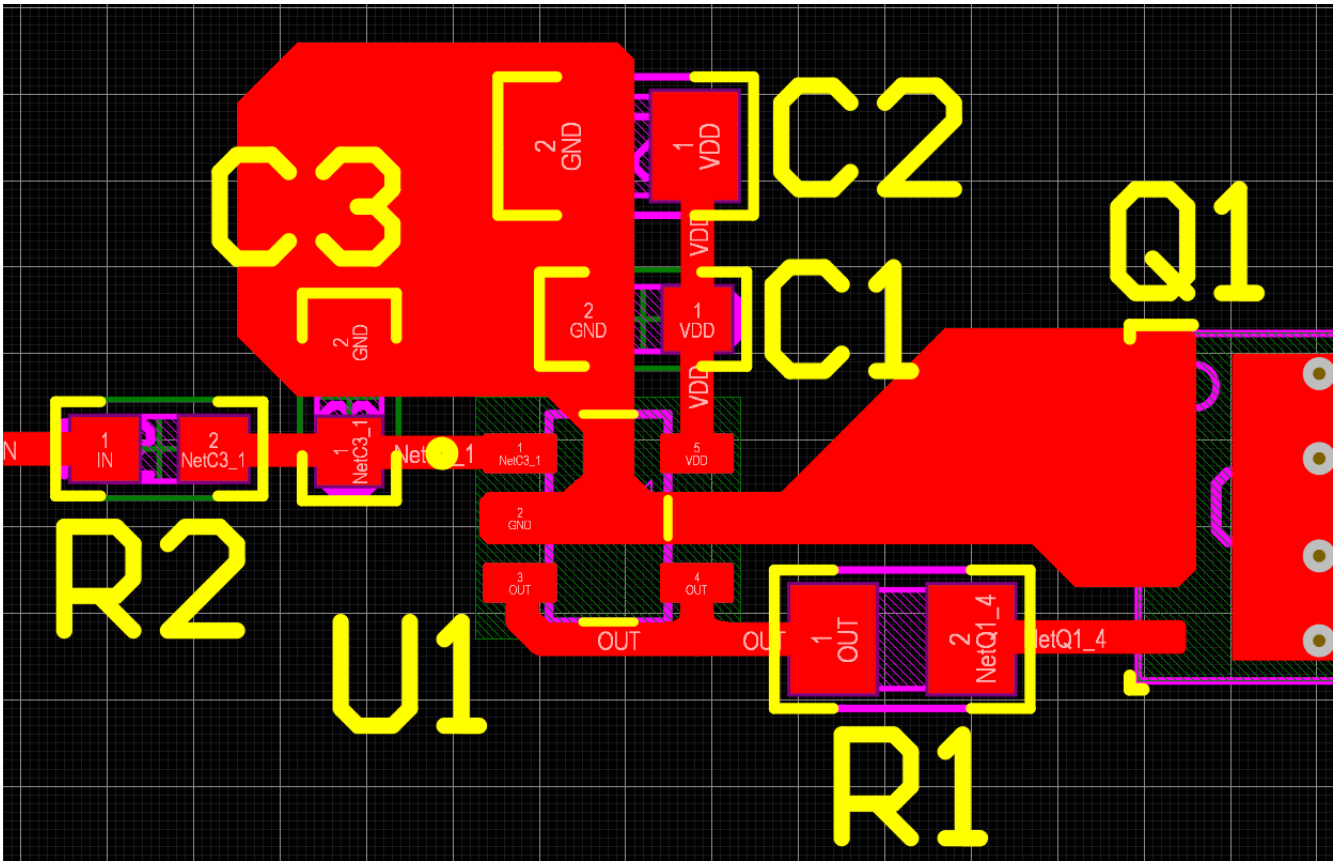


図 8-4. UCC44273 Example Layout

8.4.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive-power requirements of the load and the thermal characteristics of the package. In order for a gate driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The thermal metrics for the driver package is summarized in セクション 6.4 of the data sheet. For detailed information regarding the thermal information table, refer to the Application Note from Texas Instruments entitled *IC Package Thermal Metrics* (SPRA953).

The UCC44273 is offered in SOT-23, 5-pin package (DBV). The セクション 6.4 table summarizes the thermal performance metrics related to the package. θ_{JA} metric should be used for comparison of power dissipation between different packages. The ψ_{JT} and ψ_{JB} metrics should be used when estimating the die temperature during actual application measurements.

The DBV package heat removal occurs primarily through the leads of the device and the PCB traces connected to the leads.

8.4.4 Power Dissipation

Power dissipation of the gate driver has two portions as shown in 式 1.

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

The DC portion of the power dissipation is $P_{DC} = I_Q \times VDD$ where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage,

reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through and so on). The UCC44273 features very low quiescent currents (less than 1 mA, refer to 図 6-4) and contains internal logic to eliminate any shoot-through in the output-driver stage. Thus the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible.

The power dissipated in the gate-driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out).
- Switching frequency.
- Use of external-gate resistors.

When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly easy. The energy that must be transferred from the bias supply to charge the capacitor is given by 式 2.

$$E_G = \frac{1}{2} C_{LOAD} V_{DD}^2 \tag{2}$$

Where

- C_{LOAD} is load capacitor
- V_{DD} is bias voltage feeding the driver

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by 式 3.

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} \tag{3}$$

where

- f_{SW} is the switching frequency

The switching load presented by a power MOSFET/IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, determine the power that must be dissipated when charging a capacitor. This is done by using the equation, $Q_G = C_{LOAD} \times V_{DD}$, to provide the following equation for power:

$$P_G = C_{LOAD} V_{DD}^2 f_{SW} = Q_g V_{DD} f_{SW} \tag{4}$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on or turned off. Half of the total power is dissipated when the load capacitor is charged during turnon, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated in 式 5.

$$P_{SW} = 0.5 \times Q_G \times VDD \times f_{SW} \times \left(\frac{R_{OFF}}{R_{OFF} + R_{GATE}} + \frac{R_{ON}}{R_{ON} + R_{GATE}} \right) \tag{5}$$

where

- $R_{OFF} = R_{OL}$
- R_{ON} (effective resistance of pull-up structure) = 1.4 x R_{OL}

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC44273DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 140	4273	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

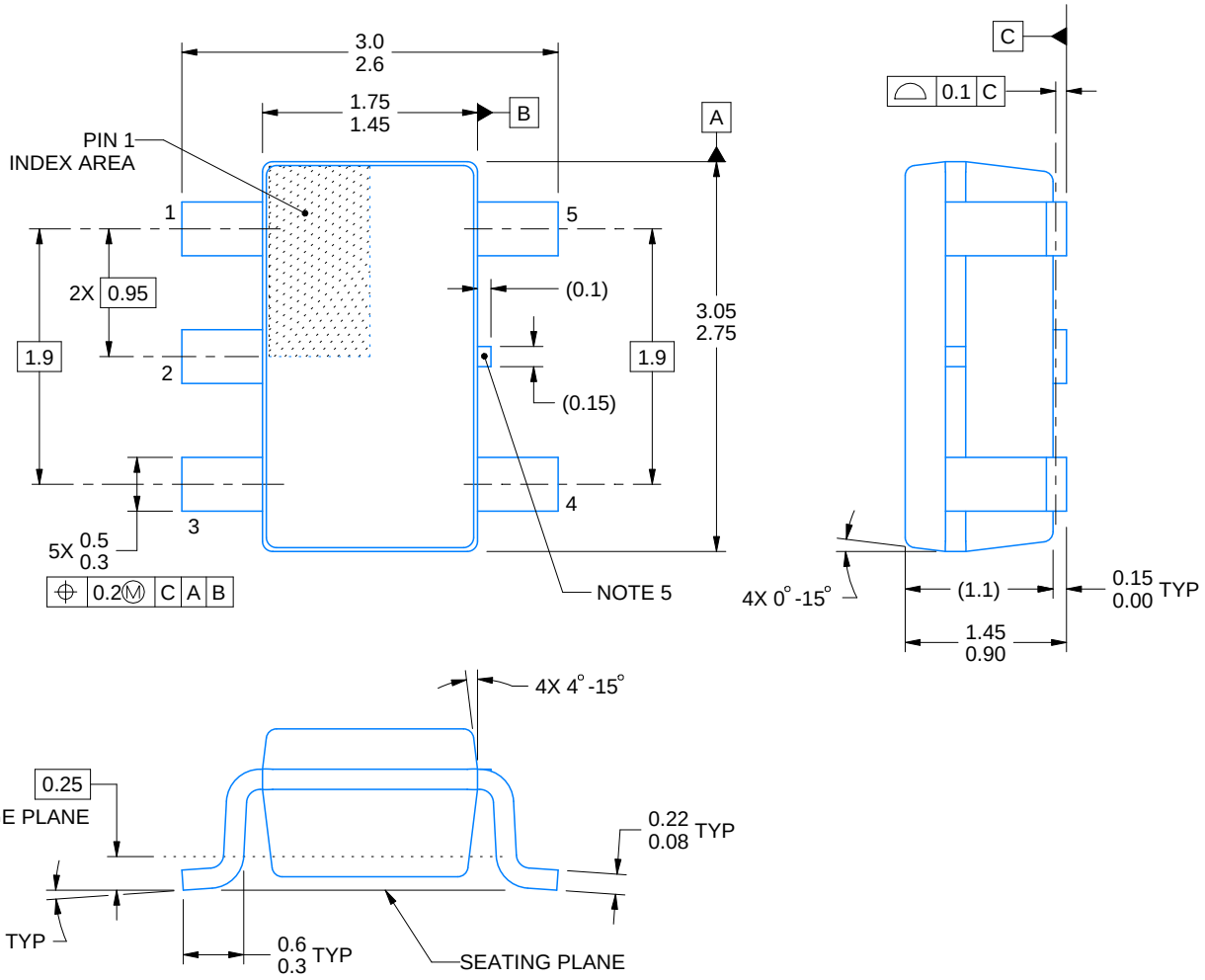
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

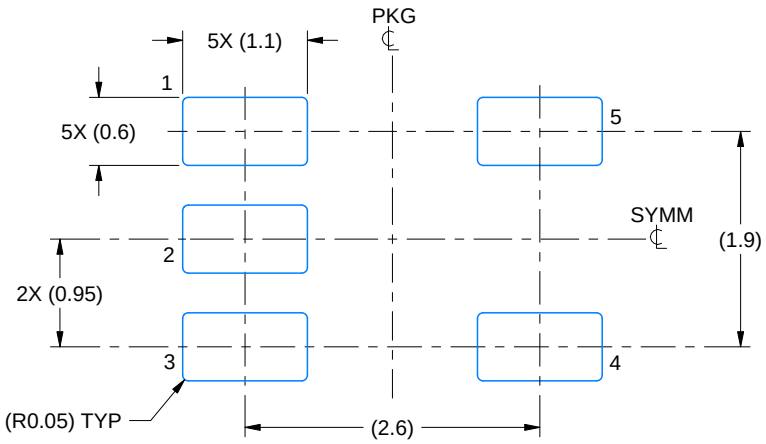
SMALL OUTLINE TRANSISTOR



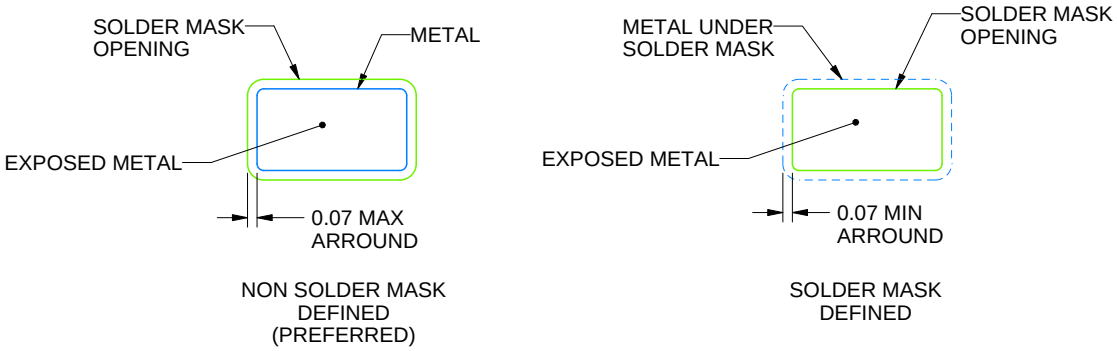
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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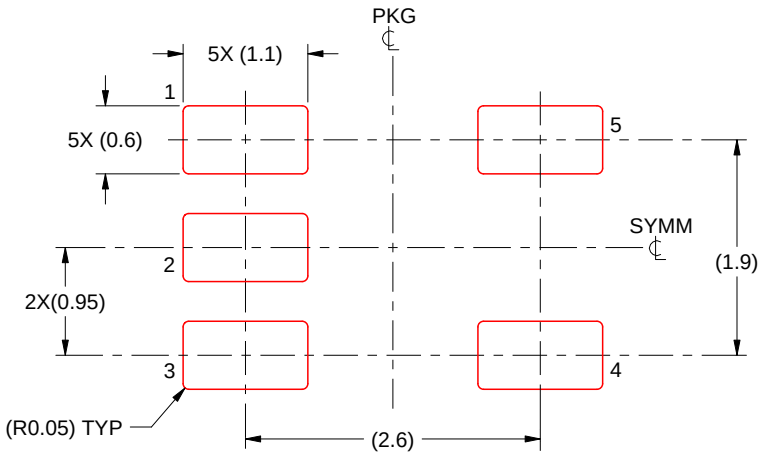
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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