参考資料

UCD7100
JAJSMV1E – MARCH 2005 – REVISED NOVEMBER 2021

UCD7100 電流センス機能搭載、デジタル制御と互換性のあるシングル・ローサイド ±4A MOSFET ドライバ

1 特長

- 可変 電流制限保護
- 3.3V、10mA の内部レギュレータ
- DSP/μC 互換入力
- シングル ±4A TrueDrive™ による高電流出力ドライバ
- 2.2nF 負荷で 10ns (標準値) の立ち上がり / 立ち下がり時間
- 25ns の入力から出力への伝搬遅延
- 25ns の電流センスと出力間の遅延
- プログラマブル電流制限スレッショルド
- デジタル出力電流制限 フラグ
- 4.5V～15V の電源電圧範囲
- 40℃～105℃で仕様を規定しています
- 鉛 (Pb) フリーのパッケージ

2 アプリケーション

- デジタル 制御 電源
- DC/DC コンバータ
- モーター・ コントローラ
- ライン・ドライバ

3 概要

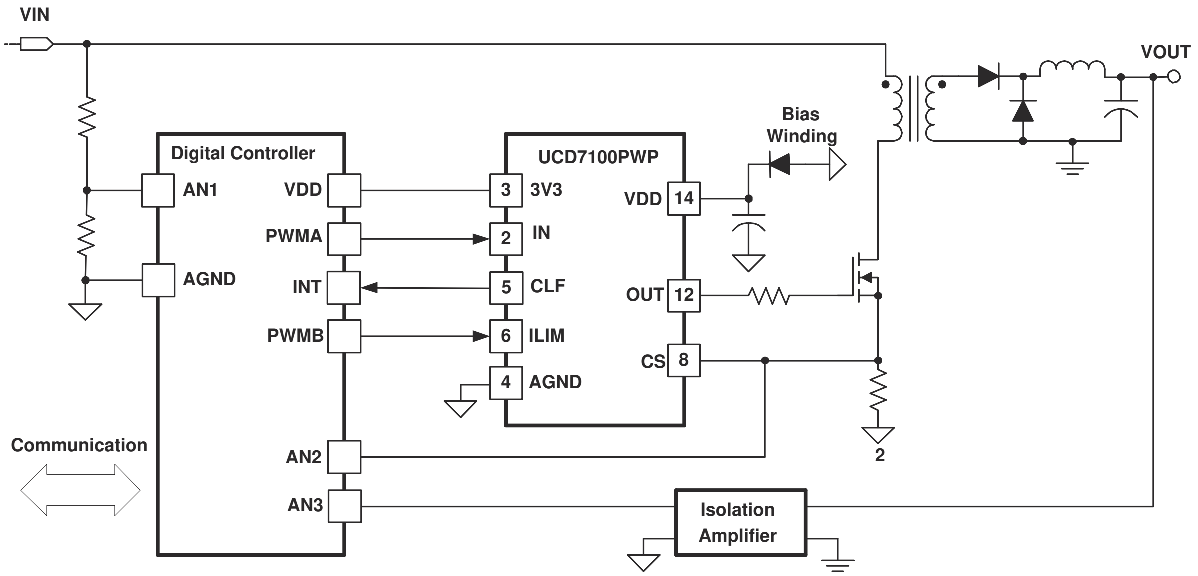
UCD7100 デバイスは、高速ローカル・ピーク電流制限保護を必要とするデジタル制御技術を使用するアプリケーション向けのデジタル制御互換ドライバ UCD7000 ファミリの製品です。

UCD7100 は、ローサイド ±4A 高電流 MOSFET ゲート・ドライバです。このドライバにより、UCD9110 や UCD9501 などのデジタル・パワー・コントローラがシングルエンド・トポロジで出力段へインターフェイスできます。プログラム可能なスレッショルドを備えたサイクル単位の電流制限機能と、ホスト・コントローラによる監視が可能なデジタル出力電流制限フラグを備えています。このドライバは、高速な 25ns のサイクル単位電流制限保護機能により、デジタル・システムが時間内に障害状態に応答できない場合には出力段をオフにできます。

製品情報[1]

部品番号	パッケージ	本体サイズ (公称)
UCD7100	HTSSOP (14)	5.00mm × 4.40mm
UCD7100A	HTSSOP (14)	5.00mm × 4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

English Data Sheet: SLUS651

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision D (October 2014) to Revision E (November 2021)	Page
• 製品情報に UCD7100A デバイスを追加	1
• Added the *Device Comparison Table*	3

5 概要 (続き)

スイッチング速度の高速化のため、UCD7100 の出力段は TrueDrive™ 出力アーキテクチャを使用しています。このアーキテクチャは、スイッチング遷移のミラー・プラトー領域において、MOSFET のゲートに ±4A の定格電流を供給します。また、デジタル・コントロールへの電力供給用に、3.3V、10mA のリニア・レギュレータも搭載しており、します。

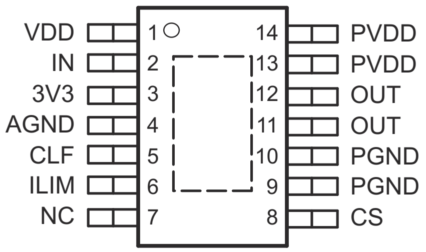
UCD7000 ドライバ・ファミリは、DSP、マイクロコントローラ、または ASIC の標準 3.3V I/O ポートと互換性があります。UCD7100 は、PowerPAD™ HTSSOP-14 で供給されます。

6 Device Comparison Table

表 6-1. UCD7100 Device Comparison

PART NUMBER	COMMENTS
UCD7100	Standard manufacturing flow
UCD7100A	Special manufacturing flow

7 Pin Configuration and Functions



NC − No internal connection

図 7-1. PWP 14 PINS Top View

表 7-1. Pin Functions

UCD7100		PIN NAME	TYPE	FUNCTION
HTSSOP-14 PIN NO.	DFN-14 PIN NO.			
1	1	VDD	I	Supply input pin to power the driver. The UCD7K devices accept an input range of 4.25 V to 15 V. Bypass the pin with at least 4.7 μF of capacitance.
2	2	IN	I	The IN pin is a high impedance digital input capable of accepting 3.3-V logic level signals up to 2 MHz. There is an internal Schmitt trigger comparator which isolates the internal circuitry from any external noise.
3	3	3V3	O	Regulated 3.3-V rail. The onboard linear voltage regulator is capable of sourcing up to 10 mA of current. Place 0.22-μF of ceramic capacitance from the pin to ground.
4	4	AGND	—	Analog ground return.
5	5	CLF	O	Current limit flag. When the CS level is greater than the ILIM voltage minus 25 mV, the output of the driver is forced low and the current limit flag (CLF) is set high. The CLF signal is latched high until the UCD7K device receives the next rising edge on the IN pin.
6	6	ILIM	I	Current limit threshold set pin. The current limit threshold can be set to any value between 0.25 V and 1.0 V.
7	7	NC	—	No Connection.
8	8	CS	I	Current sense pin. Fast current limit comparator connected to the CS pin is used to protect the power stage by implementing cycle-by-cycle current limiting.
9	9	PGND	—	Power ground return. Connect the two PGNDs together. These ground pins should be connected very closely to the source of the power MOSFET.

表 7-1. Pin Functions (continued)

UCD7100		PIN NAME	TYPE	FUNCTION
HTSSOP-14 PIN NO.	DFN-14 PIN NO.			
10	10	PGND	—	Power ground return. Connect the two PGNDs together. These ground pins should be connected very closely to the source of the power MOSFET.
11	11	OUT	O	The high-current TrueDrive™ driver output. Connect the two OUT pins together.
12	12	OUT	O	The high-current TrueDrive™ driver output. Connect the two OUT pins together.
13	13	PVDD	I	Supply pin provides power for the output drivers. It is not connected internally to the VDD supply rail. Connect the two PVDD pins together.
14	14	PVDD	I	Supply pin provides power for the output drivers. It is not connected internally to the VDD supply rail. Connect the two PVDD pins together.

8 Specifications

8.1 Absolute Maximum Ratings

			MIN	MAX[1]	UNIT[2]
V_{DD}	Supply Voltage			16	
I_{DD}	Supply Current	Quiescent		20	mA
		Switching, T_A = 25°C, T_J = 125°C, V_{DD} = 12 V		200	
V_{OUT}	Output Gate Drive Voltage	OUT	–1 V	VDD	V
$I_{OUT(sink)}$	Output Gate Drive Current	OUT		4.0	A
$I_{OUT(source)}$				–4.0	
	Analog Input	ISET, CS	–0.3	3.6	V
		ILIM	–0.3	3.6	
	Digital I/O's	IN, CLF	–0.3	3.6	
	Power Dissipation	T_A = 25°C, T_J = 125°C, (PWP-14)		2.67	W
T_J	Junction Operating Temperature		–-55	150	°C
T_{SOL}	Lead Temperature (Soldering, 10 s)			+300	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

8.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]		2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]		500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

	MIN	TYP	MAX	UNIT
Supply Voltage, VDD	4.25	12	14.5	V
Supply bypass capacitance	1			μF
Reference bypass capacitance	0.22			
Operating junction temperature	-40		105	°C

8.4 Thermal Information

THERMAL METRIC(1)		UCD7100 HTSSOP 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	29.6	
Ψ_{JT}	Junction-to-top characterization parameter	1.5	
Ψ_{JB}	Junction-to-board characterization parameter	29.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.7	

(1) For more information about traditional and new thermal metrics, see the application report, *IC Package Thermal Metrics Application Report*.

8.5 Electrical Characteristics

V_{DD} = 12 V, 4.7-μF capacitor from V_{DD} to GND, T_A = T_J = –40°C to 105°C, (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY SECTION					
Supply current, OFF	V_{DD} = 4.2 V		200	400	μA
Supply current	Outputs not switching IN = LOW		1.5	2.5	mA
LOW VOLTAGE UNDER-VOLTAGE LOCKOUT					
VDD UVLO ON		4.25	4.5	4.75	V
VDD UVLO OFF		4.05	4.25	4.45	
VDD UVLO hysteresis		150	250	350	mV
REFERENCE / EXTERNAL BIAS SUPPLY					
3V3 initial set point	T_A = 25°C	3.267	3.3	3.333	V
3V3 over temperature		3.234	3.3	3.366	
3V3 load regulation	I_{LOAD} = 1 mA to 10 mA, VDD = 5 V		1	6.6	mV
3V3 line regulation	VDD = 4.75 V to 12 V, I_{LOAD} = 10 mA		1	6.6	
Short circuit current	VDD = 4.75 to 12 V	11	20	35	mA
3V3 OK threshold, ON	3.3 V rising	2.9	3.0	3.1	V
3V3 OK threshold, OFF	3.3 V falling	2.7	2.8	2.9	
INPUT SIGNAL					
HIGH, positive-going input threshold voltage (VIT+)		1.65		2.08	V
LOW negative-going input threshold voltage (VIT-)		1.16		1.5	
Input voltage hysteresis, (VIT+ – VIT-)		0.6		0.8	
Frequency				2	MHz
CURRENT LIMIT (ILIM)					
ILIM internal current limit threshold	ILIM = OPEN	0.466	0.50	0.536	V
ILIM maximum current limit threshold	I_{LIM} = 3.3 V	0.975	1.025	1.075	V
ILIM current limit threshold	I_{LIM} = 0.75 V	0.700	0.725	0.750	
ILIM minimum current limit threshold	I_{LIM} = 0.25 V	0.21	0.23	0.25	mV
CLF output high level	CS > I_{LIM} , I_{LOAD} = -7 mA	2.64			V
CLF output low level	CS ≤ I_{LIM}, I_{LOAD} = 7 mA			0.66	
Propagation delay from IN to CLF	IN rising to CLF falling after a current limit event		10	20	ns
CURRENT SENSE COMPARATOR					

8.5 Electrical Characteristics (continued)

V_{DD} = 12 V, 4.7-μF capacitor from V_{DD} to GND, T_A = T_J = –40°C to 105°C, (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Bias voltage	Includes CS comp offset	5	25	50	mV
Input bias current			–1		uA
Propagation delay from CS to OUTx	I_{LIM} = 0.5 V, measured on OUTx, CS = threshold + 60 mV		25	40	ns
Propagation delay from CS to CLF	I_{LIM} = 0.5 V, measured on CLF, CS = threshold + 60 mV		25	50	
CURRENT SENSE DISCHARGE TRANSISTOR					
Discharge resistance	IN = low, resistance from CS to AGND	10	35	75	Ω
OUTPUT DRIVERS					
Source current(1)	V_{DD} = 12 V, IN = high, OUT = 5 V		4		A
Sink current(1)	V_{DD} = 12 V, IN = low, OUT = 5 V		4		
Source current(1)	V_{DD} = 4.75 V, IN = high, OUT = 0		2		
Sink current(1)	V_{DD} = 4.75 V, IN = low, OUT = 4.75 V		3		
Rise time, t_R (1)	C_{LOAD} = 2.2 nF, V_{DD} = 12 V		10	20	ns
Fall time, t_F (1)	C_{LOAD} = 2.2 nF, V_{DD} = 12 V		10	15	
Output with V_{DD} < UVLO	V_{DD} = 1.0 V, I_{SINK} = 10 mA		0.8	1.2	V
Propagation delay from IN to OUTx, t_{D1}	C_{LOAD} = 2.2 nF, V_{DD} = 12 V, CLK rising		20	35	ns

(1) Ensured by design. Not 100% tested in production.

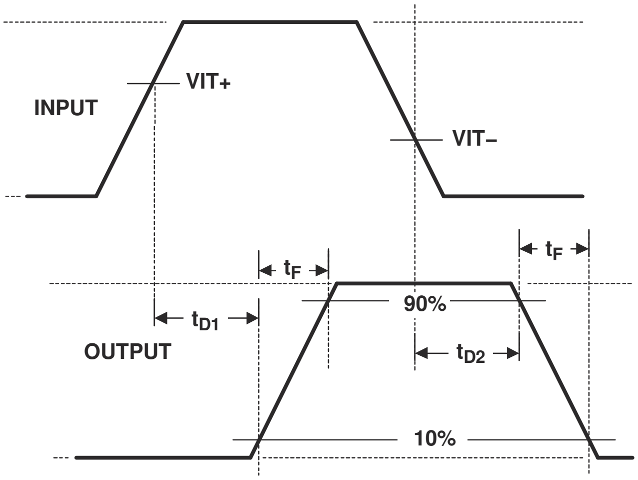


図 8-1. Timing Diagram

8.6 Typical Characteristics

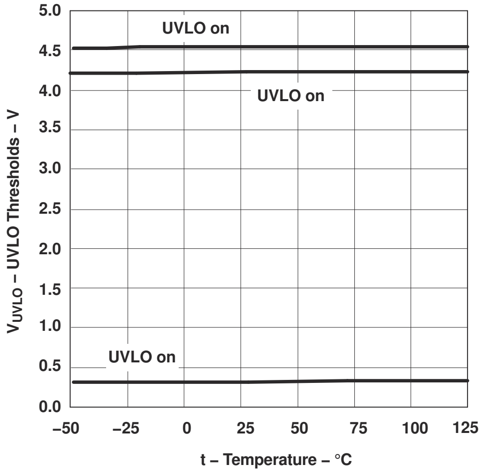


図 8-2. UVLO Thresholds vs Temperature

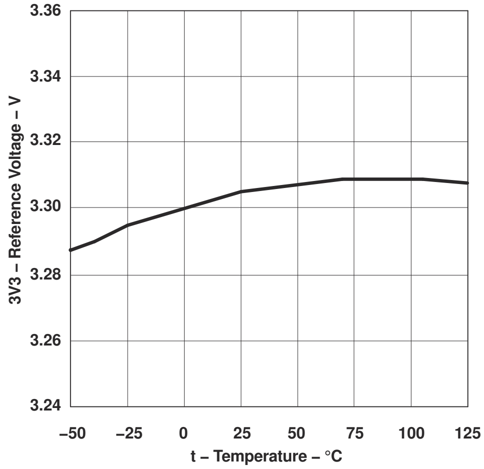


図 8-3. 3V3 Reference Voltage vs Temperature

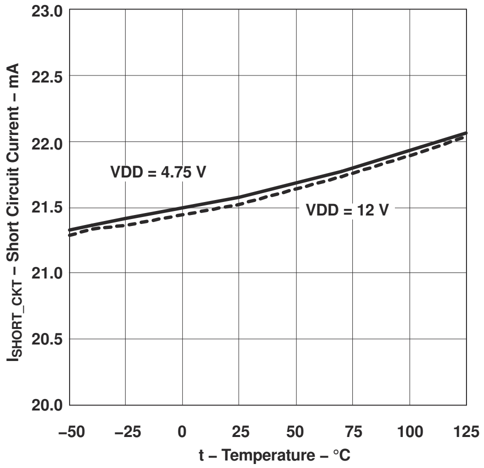


図 8-4. 3V3 Short Circuit Current vs Temperature

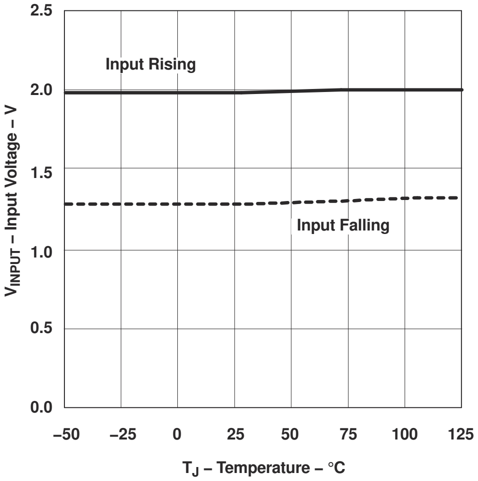


図 8-5. Input Thresholds vs Temperature

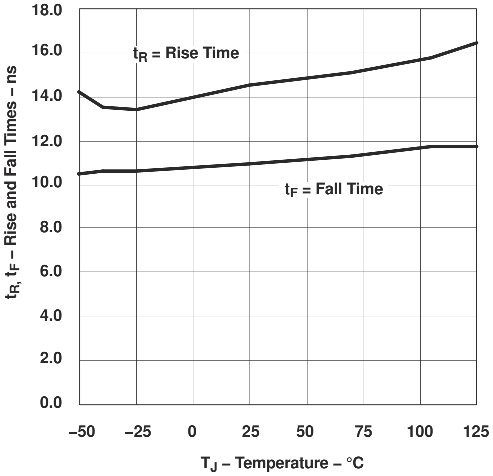


図 8-6. Output Rise Time and Fall Time vs Temperature (V_{DD} = 12 V

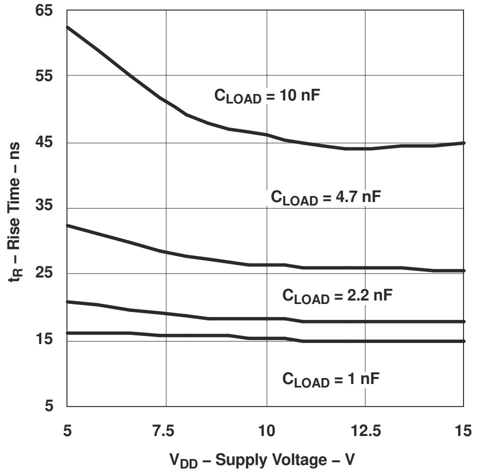


図 8-7. Rise Time vs Supply Voltage

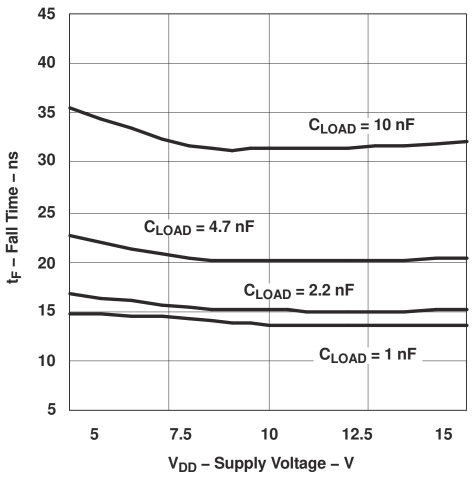


図 8-8. Fall Time vs Supply Voltage

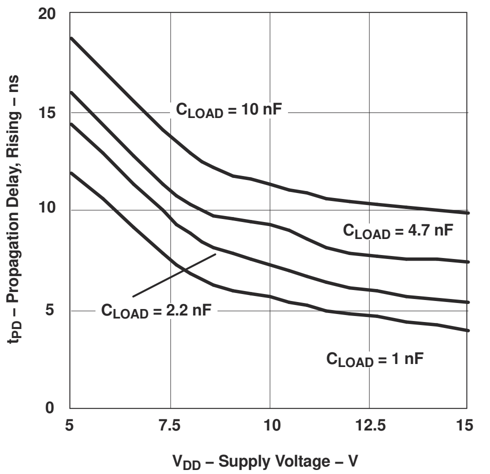


図 8-9. Propagation Delay Rising vs Supply Voltage

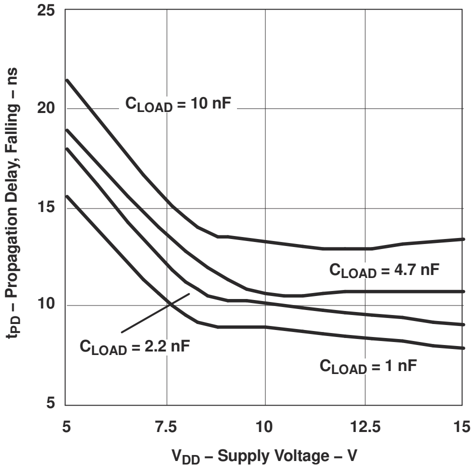


図 8-10. Propagation Delay Falling vs Supply Voltage

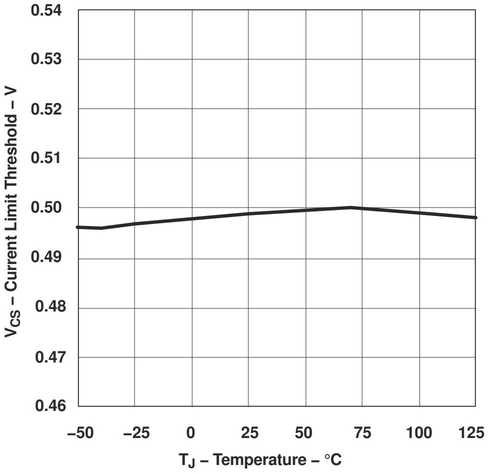


図 8-11. Default Current Limit Threshold vs Temperature

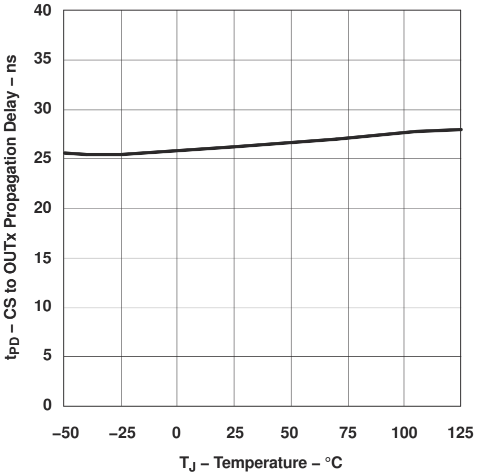


図 8-12. CS to OUTx Propagation Delay vs Temperature

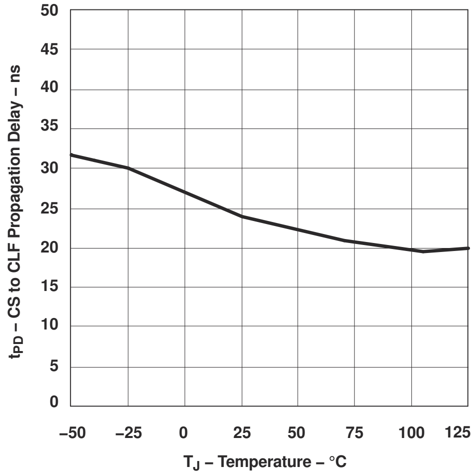


図 8-13. CS to CLF Propagation Delay vs Temperature

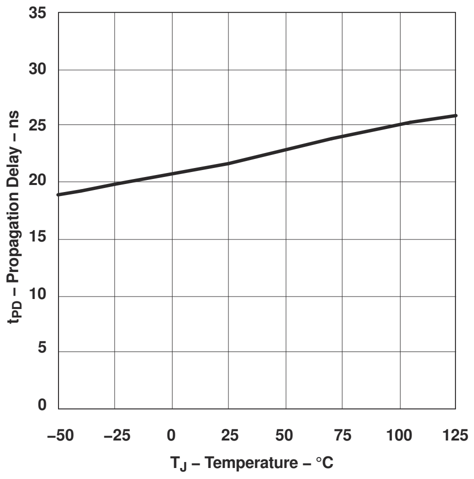


図 8-14. IN to OUT Propagation Delay vs Temperature

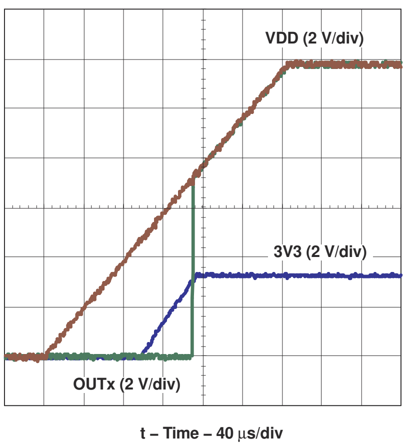


図 8-15. Start-up Behavior at V_{DD} = 12 V (Input Tied to 3V3)

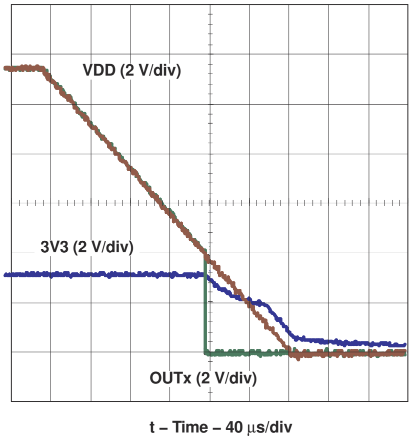


図 8-16. Shut Down Behavior at V_{DD} = 12 V (Input Tied to 3V3)

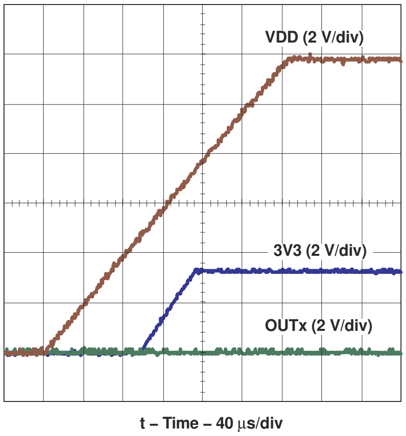


図 8-17. Start-up Behavior at V_{DD} = 12 V (Input Shortened to GND)

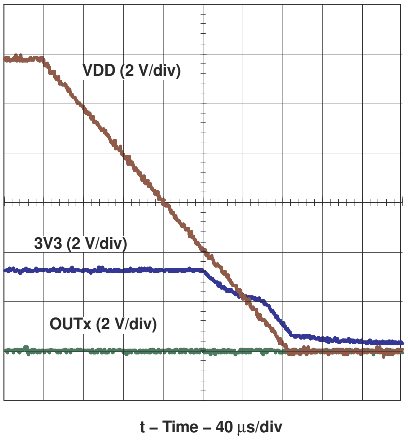


図 8-18. Shut Down Behavior at V_{DD} = 12 V (Input Shortened to GND)

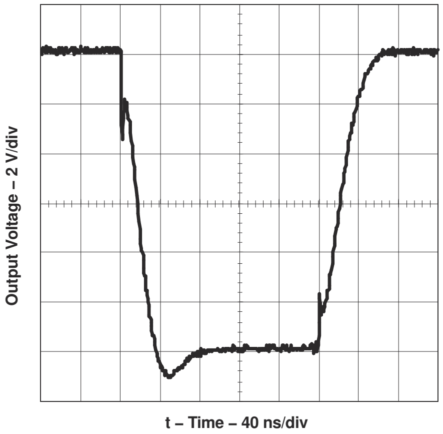


図 8-19. Output Rise and Fall Time (V_{DD} = 12 V, C_{LOAD} = 10 NF)

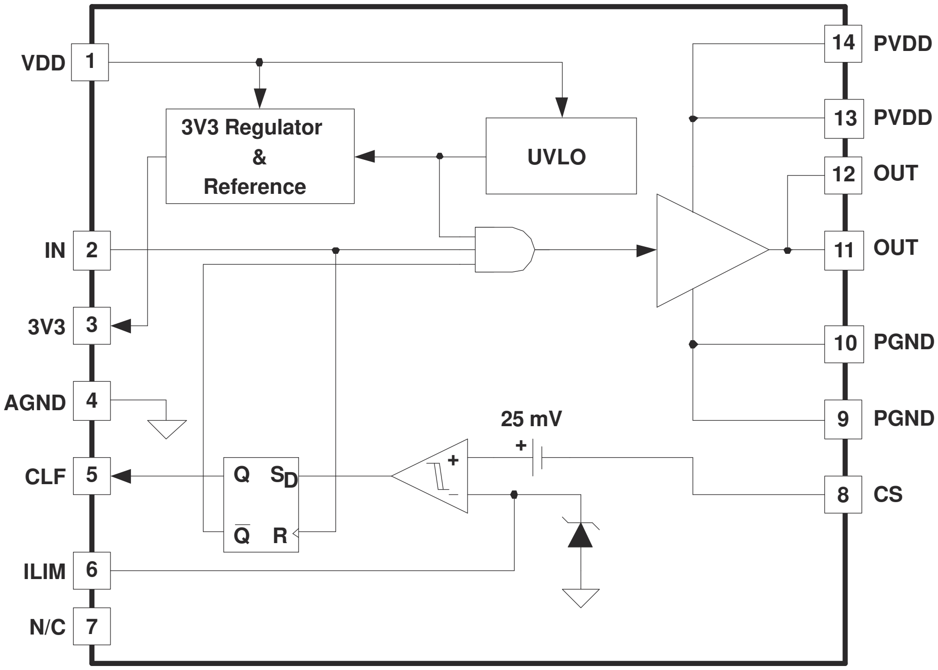
9 Detailed Description

9.1 Overview

The UCD7100 is a member of the UCD7K family of digital control compatible drivers for applications utilizing digital control techniques, or applications requiring fast local peak current limit protection.

The UCD7100 is a low-side ±4-A high-current MOSFET gate driver. The UCD7100 allows digital power controllers such as the UCD9110 or UCD9501 to interface to the power stage in single-ended topologies. It provides a cycle-by-cycle current limit function with programmable threshold and a digital output current limit flag, which can be monitored by the host controller. With a fast 25-ns cycle-by-cycle current limit protection, the driver can turn off the power stage in the unlikely event that the digital system cannot respond to a failure situation in time.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Input

The IN pin is a high impedance digital input capable of accepting 3.3-V logic level signals up to 2 MHz. There is an internal Schmitt Trigger comparator which isolates the internal circuitry from any external noise.

If limiting the rise or fall times to the power device is desired, then an external resistance can be added between the output of the driver and the load device, which is generally a power MOSFET gate. The external resistor may also help remove power dissipation from the package.

9.3.2 Current Sensing and Protection

A very fast current limit comparator connected to the CS pin is used to protect the power stage by implementing cycle-by-cycle current limiting.

The current limit threshold is equal to the lesser of the positive inputs at the current limit comparator. The current limit threshold can be set to any value between 0.25 V and 1.0 V by applying the desired threshold voltage to the current limit (ILIM) pin. When the CS level is greater than the ILIM voltage minus 25 mV, the output of the driver is forced low and the current limit flag (CLF) is set high. The CLF signal is latched high until the UCD7K device receives the next rising edge on the IN pin.

When the CS voltage is below ILIM, the driver output will follow the PWM input. The CLF digital output flag can be monitored by the host controller to determine when a current limit event occurs and to then apply the appropriate algorithm to obtain the desired current limit profile.

One of the main benefits of this local protection feature is that the UCD7K devices can protect the power stage if the software code in the digital controller becomes corrupted and hangs up. If the controller's PWM output stays high, the local current sense circuit will turn off the driver output when an over-current condition occurs. The system would likely go into a retry mode because; most DSP and microcontrollers have on-board watchdog, brown-out, and other supervisory peripherals to restart the device in the event that it is not operating properly. But these peripherals typically do not react fast enough to save the power stage. The UCD7K's local current limit comparator provides the required fast protection for the power stage.

The CS threshold is 25 mV below the ILIM voltage. This way, if the user attempts to command zero current ($I_{LIM} < 25$ mV) while the CS pin is at ground, for example at start-up, the CLF flag latches high until the IN pin receives a pulse. At start-up it is necessary to ensure that the ILIM pin always greater than the CS pin for the handshaking to work as described below. If for any reason the CS pin comes to within 25 mV of the ILIM pin during start-up, then the CLF flag is latched high and the digital controller must poll the UCD7K device, by sending it a narrow IN pulse. If the fault condition is not present the IN pulse resets the CLF signal to low indicating that the UCD7K device is ready to process power pulses.

9.3.3 Handshaking

The UCD7K family of devices have a built-in handshaking feature to facilitate efficient start-up of the digitally controlled power supply. At start-up the CLF flag is held high until all the internal and external supply voltages of the UCD7K device are within their operating range. Once the supply voltages are within acceptable limits, the CLF goes low and the device will process input drive signals. The micro-controller should monitor the CLF flag at start-up and wait for the CLF flag to go LOW before sending power pulses to the UCD7K device.

9.3.4 Driver Output

The high-current output stage of the UCD7K device family is capable of supplying ±4-A peak current pulses and swings to both VDD and GND. The driver outputs follows the state of the IN pin provided that the VDD and 3V3 voltages are above their respective under-voltage lockout threshold.

The drive output utilizes Texas Instruments' TrueDrive™ architecture, which delivers rated current into the gate of a MOSFET when it is most needed during the Miller plateau region of the switching transition providing efficiency gains.

TrueDrive™ consists of pullup/ pulldown circuits using bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. The output resistance is the $R_{DS(on)}$ of the MOSFET transistor when the voltage on the driver output is less than the saturation voltage of the bipolar transistor. This hybrid output stage also allows efficient current sourcing at low supply voltages.

Each output stage also provides a very low impedance to overshoot and undershoot due to the body diode of the external MOSFET. This means that in many cases, external-schottky-clamp diodes are not required.

9.3.5 Source/Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCD7K drivers have been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging/discharging of the drain-gate capacitance with current supplied or removed by the driver device. See Reference [1]

9.3.6 Drive Current and Power Requirements

The UCD7K family of drivers can deliver high current into a MOSFET gate for a period of several hundred nanoseconds. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground. This repeats at the operating frequency of the power device. A MOSFET is used in this discussion because it is the most common type of switching device used in high frequency power conversion equipment.

Reference [1] discusses the current required to drive a power MOSFET and other capacitive-input switching devices.

When a driver device is tested with a discrete, capacitive load it is a fairly simple matter to calculate the power that is required from the bias supply. The energy that must be transferred from the bias supply to charge the capacitor is given by:

$$E = \frac{1}{2} \times CV^2 \tag{1}$$

where C is the load capacitor and V is the bias voltage feeding the driver.

There is an equal amount of energy transferred to ground when the capacitor is discharged. This leads to a power loss given by the following:

$$P = \frac{1}{2} \times CV^2 \times f \tag{2}$$

where f is the switching frequency.

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged. An actual example using the conditions of the previous gate drive waveform should help clarify this.

With V_{DD} = 12 V, C_{LOAD} = 10 nF, and f = 300 kHz, the power loss can be calculated as:

$$P = 10\text{ nF} \times 12^2 \times 300\text{ kHz} = 0.432\text{ W} \tag{3}$$

With a 12-V supply, this would equate to a current of:

$$I = \frac{P}{V} = \frac{0.432\text{ W}}{12\text{ V}} = 0.036\text{ A} \tag{4}$$

The actual current measured from the supply was 0.037 A, and is very close to the predicted value. But, the I_{DD} current that is due to the device internal consumption should be considered. With no load the device current drawn is 0.0027 A. Under this condition the output rise and fall times are faster than with a load. This could lead to an almost insignificant, yet measurable current due to cross-conduction in the output stages of the driver. However, these small current differences are buried in the high frequency switching spikes, and are beyond the measurement capabilities of a basic lab setup. The measured current with 10-nF load is close to the value expected.

The switching load presented by a power MOSFET can be converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain of the device between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_G, one can determine the power that must be dissipated when charging a capacitor. This is done by using the equivalence $Q_G = C_{EFF} \times V$ to provide the following equation for power:

$$P = C \times V^2 \times f = Q_G \times V \times f \tag{5}$$

This equation allows a power designer to calculate the bias power required to drive a specific MOSFET gate at a specific bias voltage.

Note

The 10% and 90% thresholds depict the dynamics of the bipolar output devices that dominate the power MOSFET transition through the Miller regions of operation.

9.4 Device Functional Modes

9.4.1 Operation with V_{DD} < 4.25 V (minimum V_{DD})

The devices operate with V_{DD} voltages above 4.75 V. The maximum UVLO voltage is 4.75 V, and operates at V_{DD} voltages above 4.75 V. The typical UVLO voltage is 4.5 V. The minimum UVLO voltage is 4.25 V. At V_{DD} below the actual UVLO voltage, the devices do not operate, and OUT remains low.

9.4.2 Operation with IN Pin Open

If the IN pin is disconnected (open), a 100 kΩ internal resistor connects IN to GND to prevent unpredictable operation due to a floating IN pin, and OUT remains low.

9.4.3 Operation with ILIM Pin Open

If the ILIM pin is disconnected (open), the current limit threshold is set at 0.5 V.

9.4.4 Operation with ILIM Pin High

If the signal on ILIM pin is higher than 1 V, the current limit threshold is clamped at 1 V.

10 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

The UCD7100 is part of a family of digital compatible drivers targeting applications utilizing digital control techniques or applications that require local fast peak current limit protection.

10.2 Typical Application

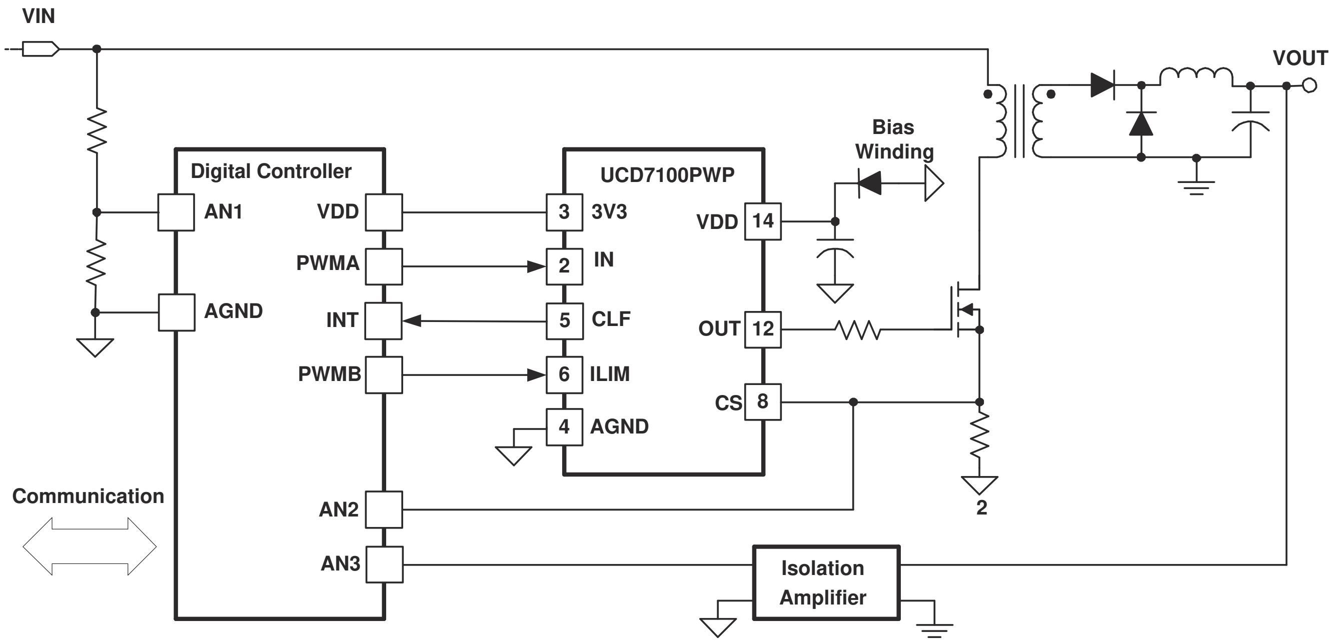


図 10-1. Typical Application

10.2.1 Design Requirements

In this design example, the UCD7100 is used to drive a forward converter which is controlled by a digital controller. The switching frequency is 100 KHz, and the input current cycle-by-cycle protection threshold is set at 5 A.

10.2.2 Detailed Design Procedure

The cycle-by-cycle current protection is implemented by connecting the current sense signal to the CS pin. When the CS level is greater than the ILIM voltage minus 25 mV, the output of the driver is forced low and the current limit flag (CLF) is set high. The CLF signal is latched high until the UCD7K device receives the next rising edge on the IN pin.

$$I_{peak} * R_{sense} = V_{ILIM} - 0.025 \tag{6}$$

$$R_{sense} = \frac{V_{ILIM} - 0.025}{I_{peak}} \tag{7}$$

The current limit threshold can be set to any value between 0.25 V and 1.0 V, so R_{sense} must be between 0.045 Ω and 0.195 Ω. For example, if R_{sense} is 0.15 Ω, then V_{ILIM} must be 0.775 V to protect input current at 5 A. If the digital controller has an internal digital-to-analog converter, then it can generate 0.775 V and connect to ILIM directly. For a digital controller without an internal digital-to-analog converter, it can generate a PWM signal, send the PWM signal through a low pass filter, then connect to the ILIM pin. Assuming the magnitude of the PWM pulse is 3.3 V, then the duty cycle is:

$$D = \frac{0.775}{3.3} \tag{8}$$

10.2.3 Application Curve

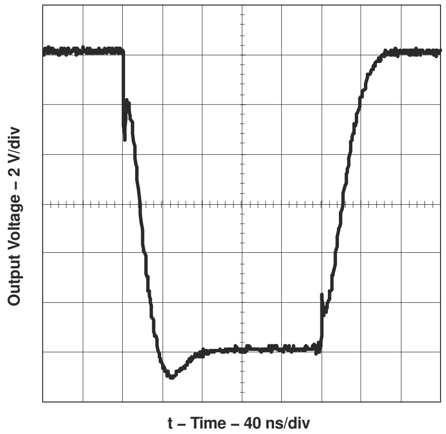


図 10-2. Output Rise and Fall Time (V_{DD} = 12 V, C_{LOAD} = 10 NF)

11 Power Supply Recommendations

11.1 Supply

The UCD7K devices accept an input range of 4.5 V to 15 V. The device has an internal precision linear regulator that produces the 3V3 output from this VDD input. A separate pin, PVDD, not connected internally to the VDD supply rail provides power for the output drivers. In all applications the same bus voltage supplies the two pins. It is recommended that a low value of resistance be placed between the two pins so that the local capacitance on each pin forms low pass filters to attenuate any switching noise that may be on the bus.

Although quiescent VDD current is low, total supply current will be higher, depending on the gate drive output current required by the switching frequency. Total V_{DD} current is the sum of quiescent V_{DD} current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Q_G), average OUT current can be calculated from:

$I_{OUT} = Q_G \times f$, where f is frequency.

For high-speed circuit performance, a V_{DD} bypass capacitor is recommended to prevent noise problems. A 4.7-μF ceramic capacitor should be located close to the V_{DD} to ground connection. A larger capacitor with relatively low ESR should be connected to the PVDD pin, to help deliver the high current peaks to the load. The capacitors should present a low impedance characteristic for the expected current levels in the driver application. The use of surface mount components for all bypass capacitors is highly recommended.

11.2 Reference and External Bias Supply

All devices in the UCD7K family are capable of supplying a regulated 3.3-V rail to power various types of external loads such as a microcontroller or an ASIC. The onboard linear voltage regulator is capable of sourcing up to 10 mA of current. For normal operation, place a minimum of 0.22 μF of ceramic capacitance from the reference pin to ground.

12 Layout

12.1 Layout Guidelines

In a power driver operating at high frequency, it is a significant challenge to get clean waveforms without much overshoot/undershoot and ringing. The low output impedance of these drivers produces waveforms with high di/dt. This tends to induce ringing in the parasitic inductances. Utmost care must be used in the circuit layout. It is advantageous to connect the driver IC as close as possible to the leads. The driver device layout has the analog ground on the opposite side of the output, so the ground should be connected to the bypass capacitors and the load with copper trace as wide as possible. These connections should also be made with a small enclosed loop area to minimize the inductance.

12.2 Layout Example

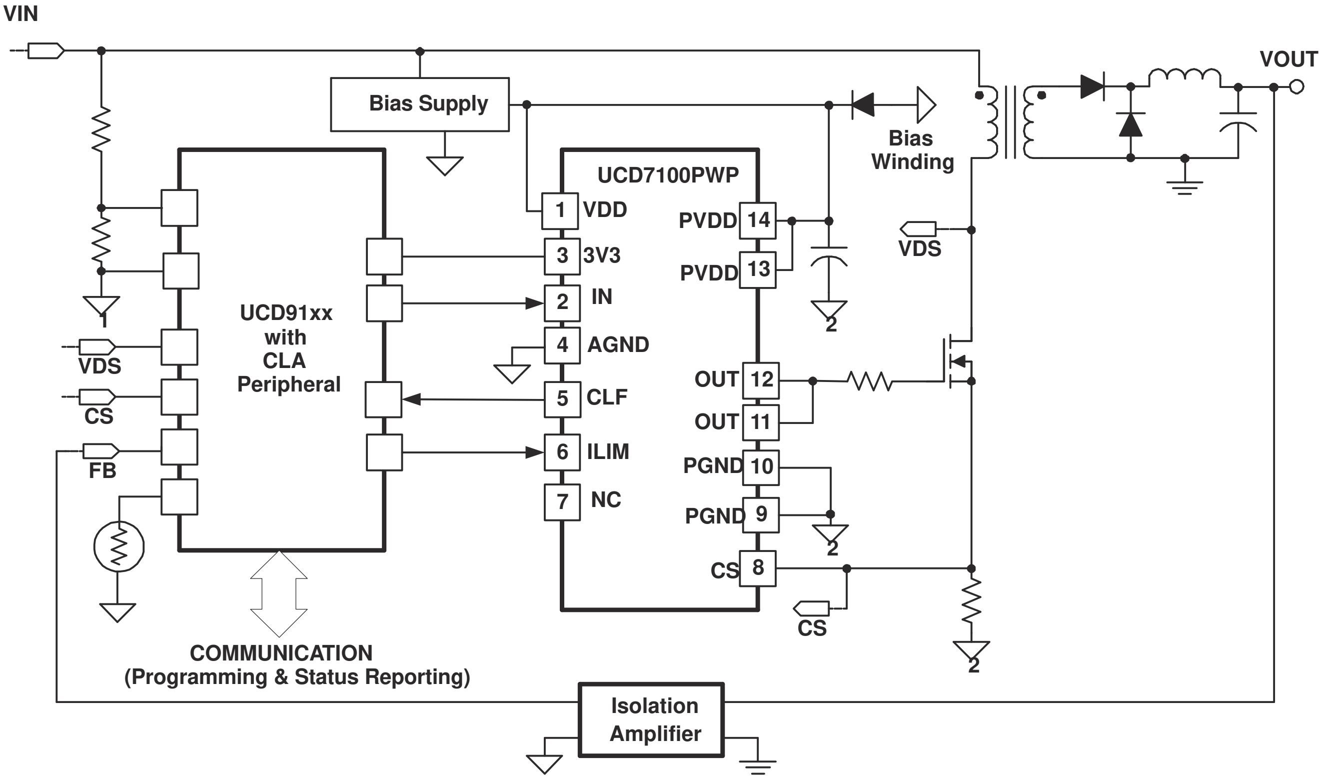


図 12-1. Isolated Forward Converter

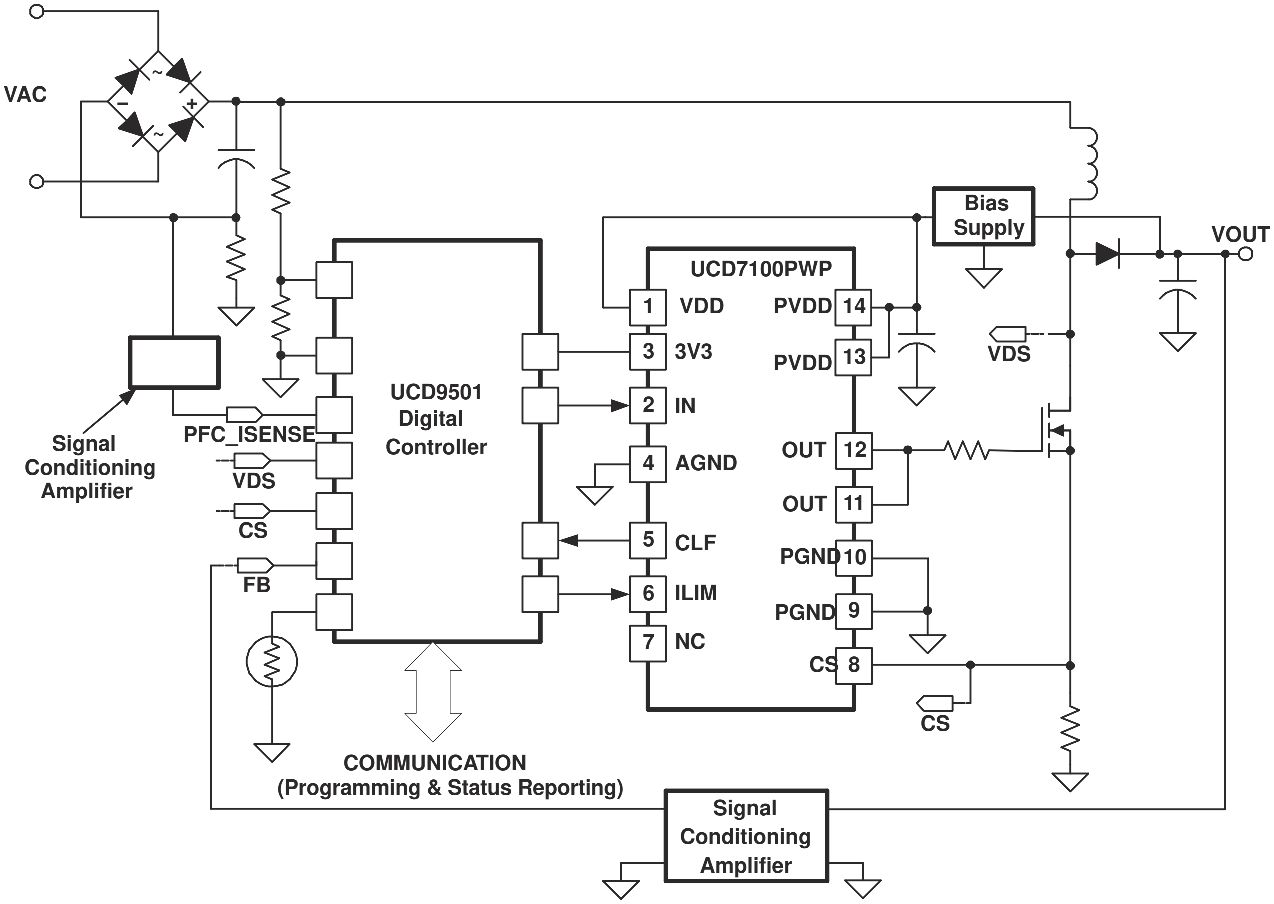


図 12-2. PFC Boost Front-End Power Supply

12.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a power driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCD7K family of drivers is available in PowerPAD™ TSSOP package to cover a range of application requirements. Both have the exposed pads to relieve thermal dissipation from the semiconductor junction.

As illustrated in Reference [2], the PowerPAD™ packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board (PCB) directly underneath the device package, reducing the Θ_{JC} down to 4.7°C/W. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as summarized in Reference [3].

Note that the PowerPAD™ is not directly connected to any leads of the package. However, it is electrically and thermally connected to the substrate which is the ground of the device.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Development Support

PRODUCT	DESCRIPTION	FEATURES
UCD7201	Dual Low Side ±4-A Drivers with Common CS	3V3, CS(1) (2)
UCD7230	±4A Synchronous Buck Driver with CS	3V3, CS(1) (2)

(1) 3V3 = 3.3V linear regulator.
(2) CS = current sense and current limit function.

13.2 Third-Party Products Disclaimer

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13.3 Documentation Support

13.3.1 Related Documentation

1. Texas Instruments, *Power Supply Seminar SEM−1400 Topic 2: Design And Application Guide For High Speed MOSFET Gate Drive Circuits, by Laszlo Balogh*
2. Texas Instruments, *Technical Brief, PowerPad Thermally Enhanced Package*
3. Texas Instruments, *Application Brief, PowerPAD Made Easy*

13.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.5 サポート・リソース

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13.6 Trademarks

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13.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13.8 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCD7100APWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCD7100	Samples
UCD7100APWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCD7100	Samples
UCD7100PWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCD7100	Samples
UCD7100PWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCD7100	Samples
UCD7100PWPRG4	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	UCD7100	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

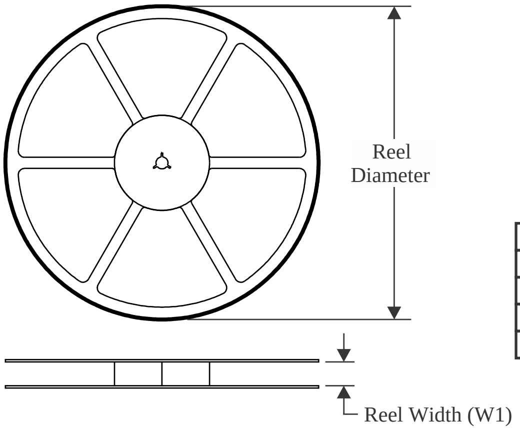
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

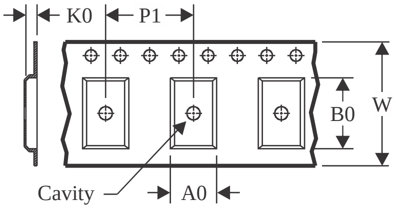
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

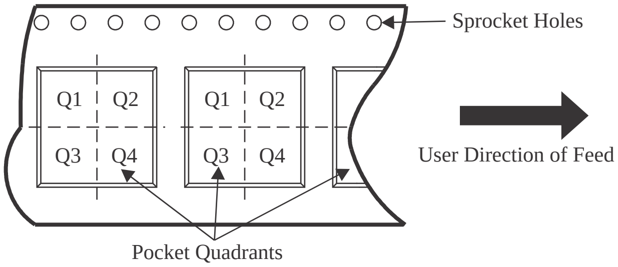


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

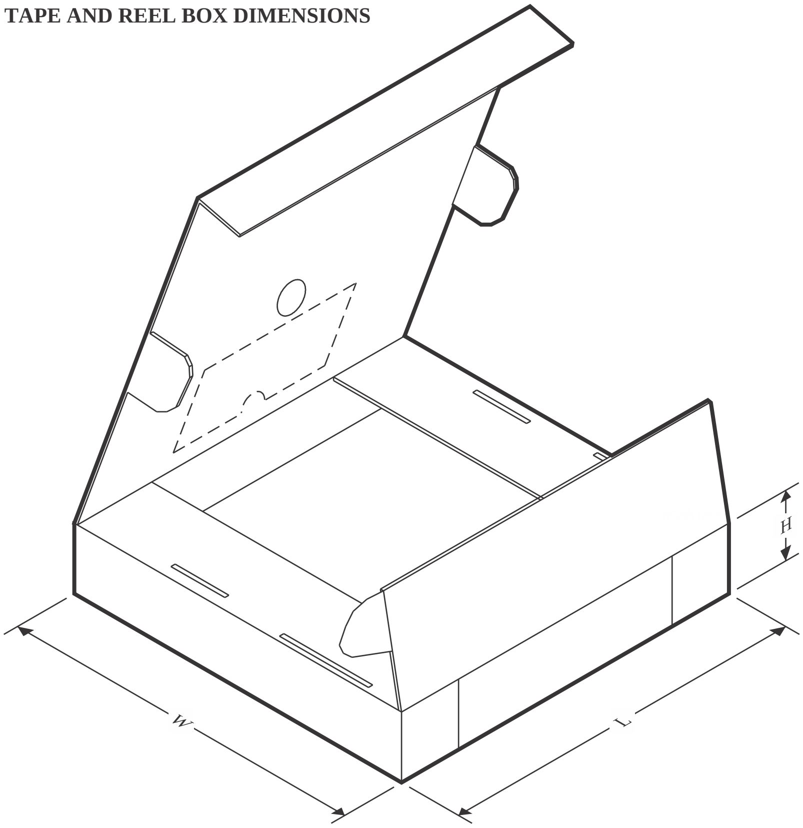
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD7100APWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
UCD7100PWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

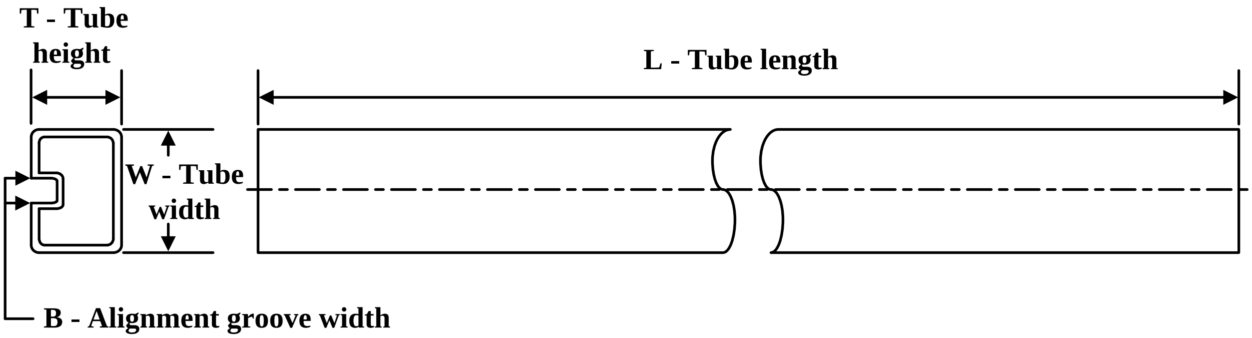
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD7100APWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
UCD7100PWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

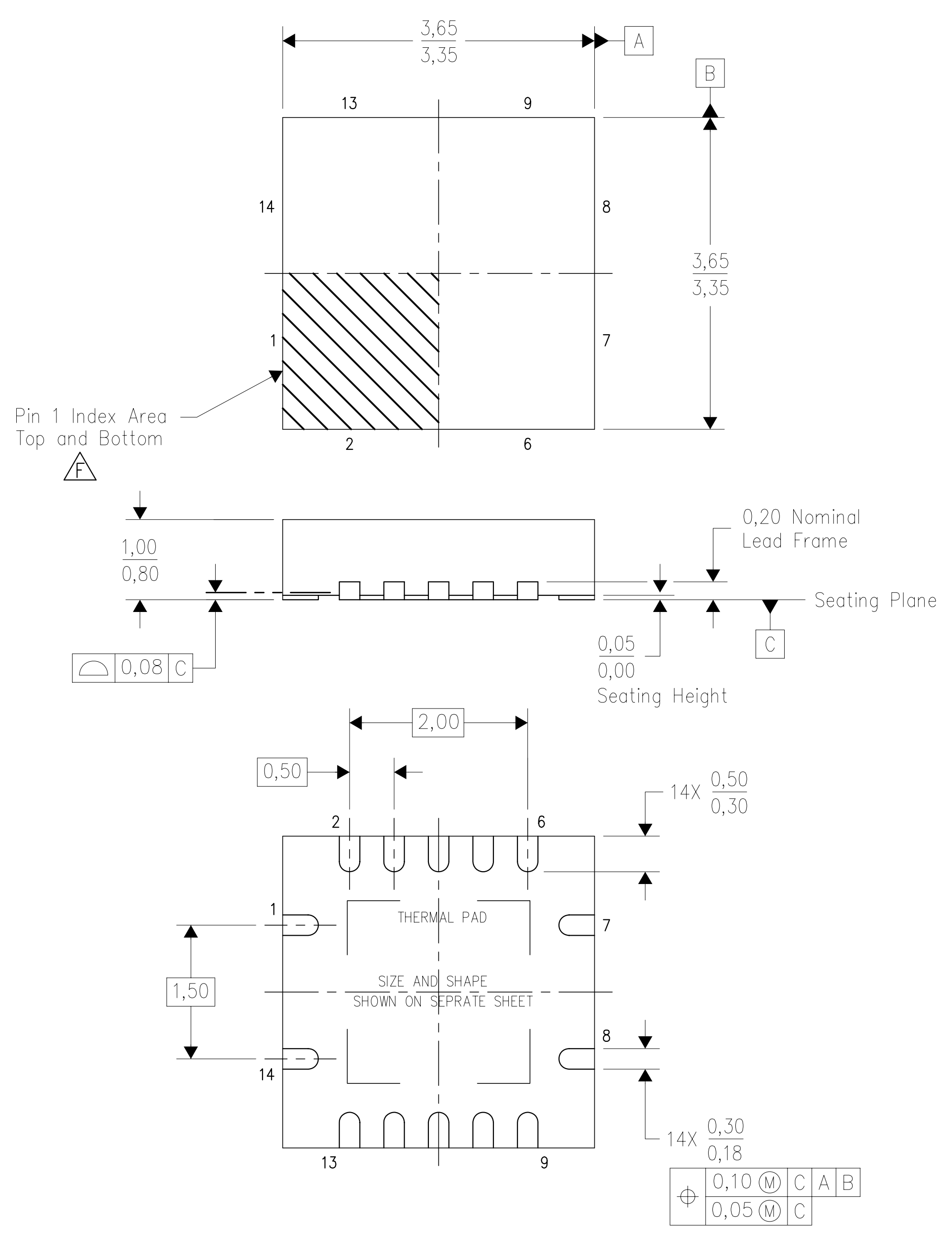
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UCD7100APWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5
UCD7100PWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5

RGY (S-PVQFN-N14) PLASTIC QUAD FLATPACK NO-LEAD



4203539-2/I 06/2011

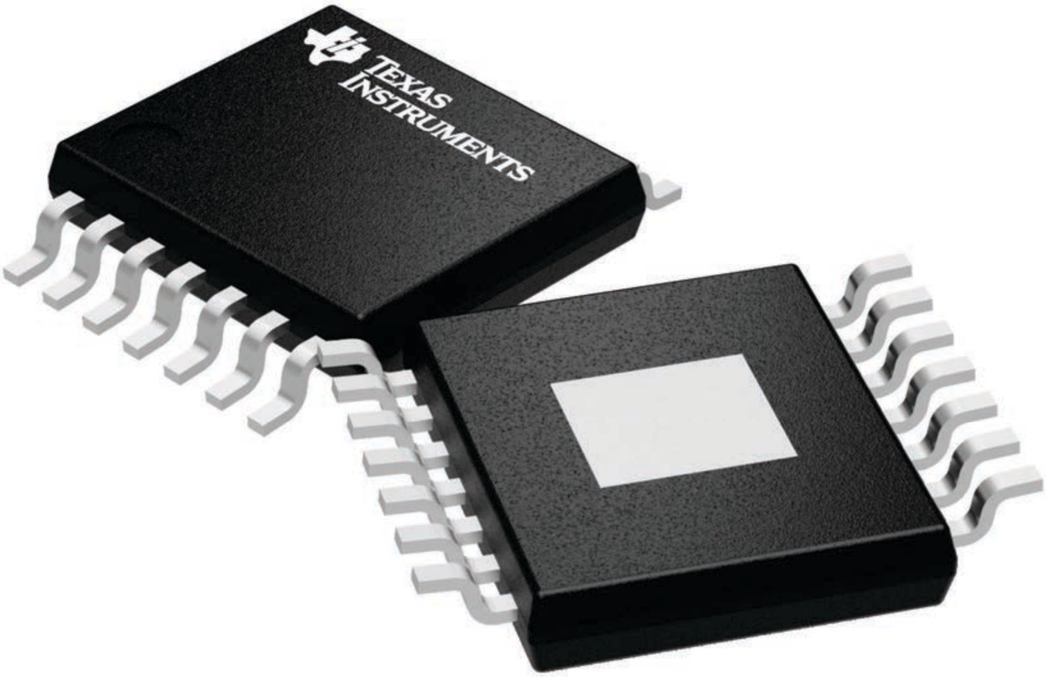
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F⚠ Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO–241 variation BA.

GENERIC PACKAGE VIEW

PWP 14 **PowerPAD TSSOP - 1.2 mm max height**

4.4 x 5.0, 0.65 mm pitch PLASTIC SMALL OUTLINE

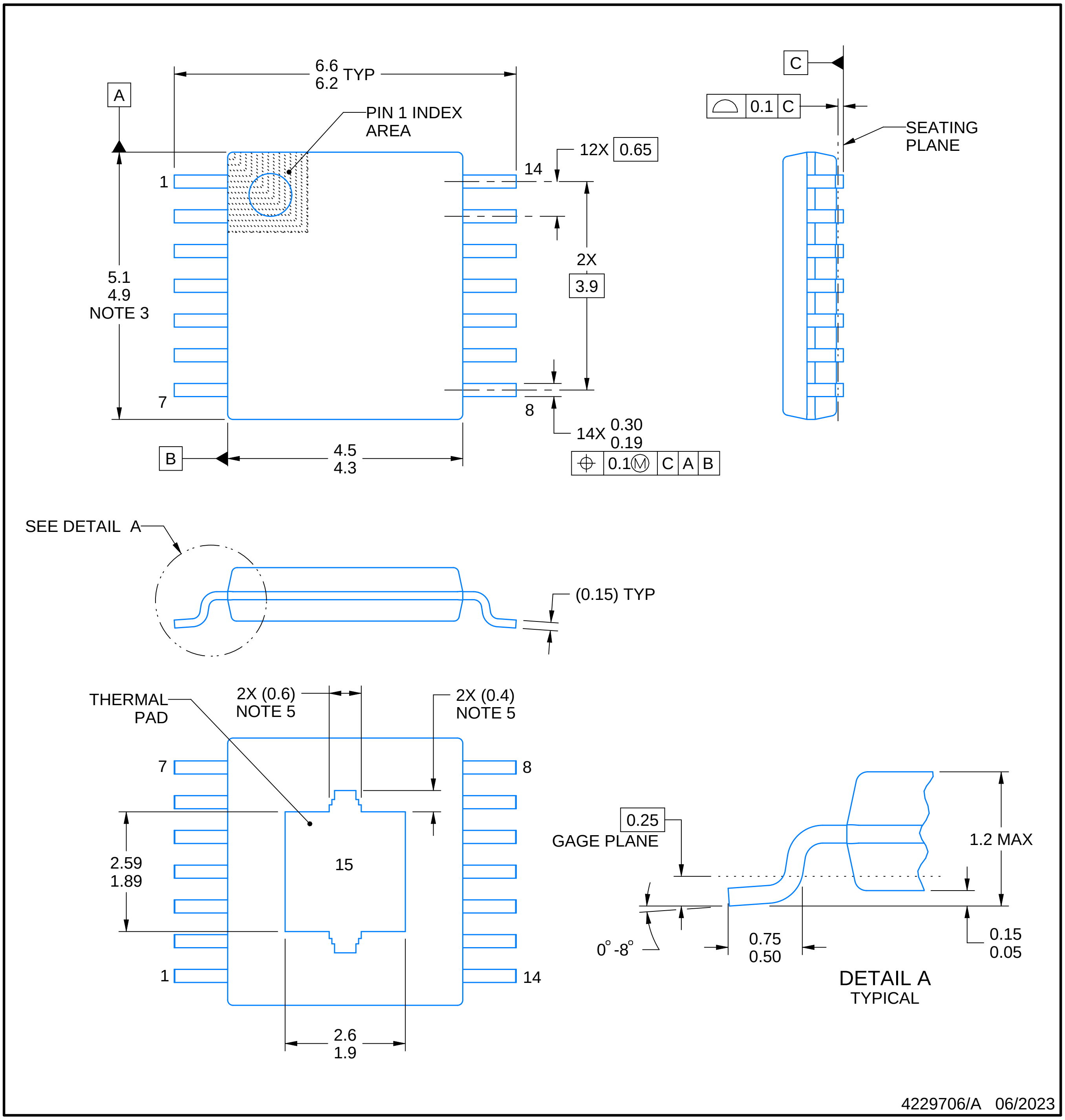
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PACKAGE OUTLINE

PowerPAD™ TSSOP - 1.2 mm max height

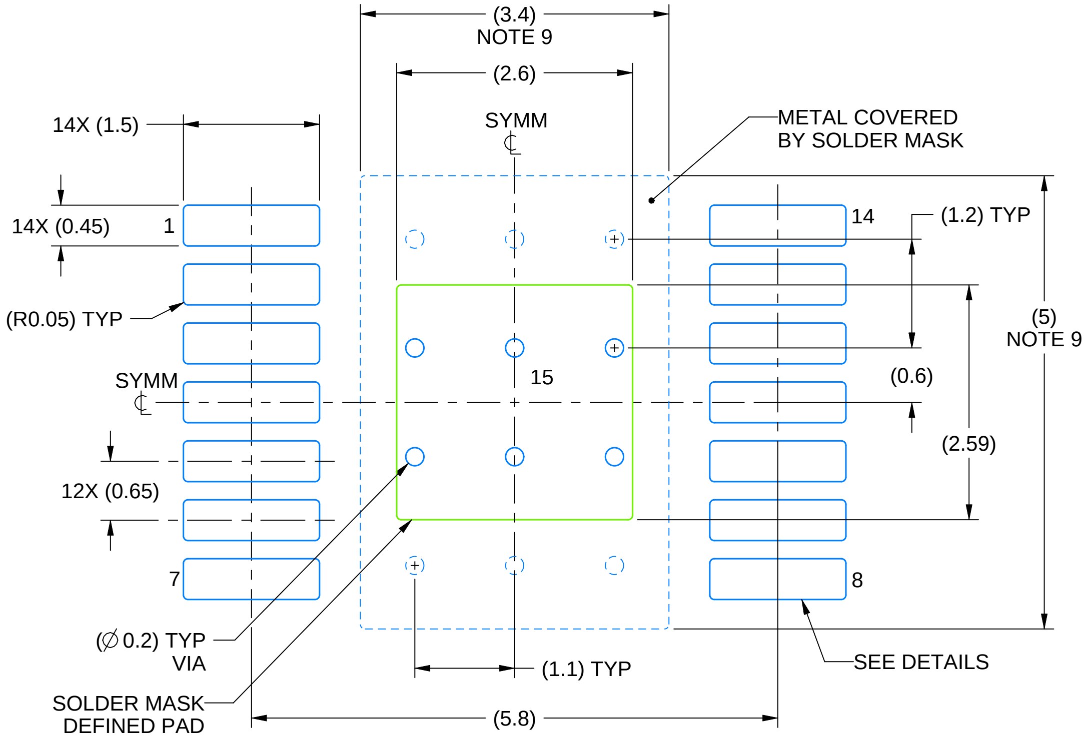
SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

NON-SOLDER MASK
DEFINED

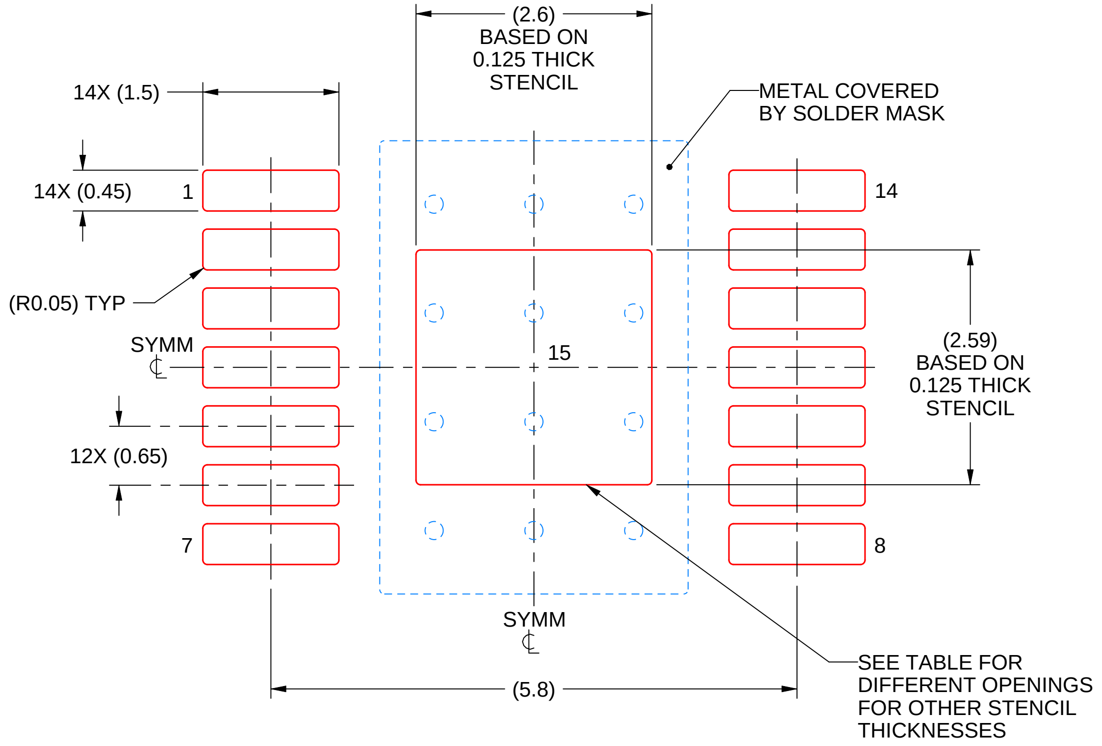
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4229706/A 06/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265