ULQ200xA-Q1 高電圧、大電流ダーリントン トランジスタ アレイ

1 特長

- 車載アプリケーション認定済み
- マシン モデルで 200V を超える ESD 保護 (C = 200pF、R = 0)
- 定格 500mA のコレクタ電流 (単一出力)
- 高電圧出力:50 V
- 出力クランプ ダイオード
- 各種のロジックと互換性のある入力
- リレー ドライバ アプリケーション

2 アプリケーション

- リレー ドライバ
- ステッパおよび DC ブラシ付きモータ ドライバ
- ランプ ドライバ
- ディスプレイ ドライバ (LED、ガス放電)
- ライン ドライバ
- ロジック バッファ

3 概要

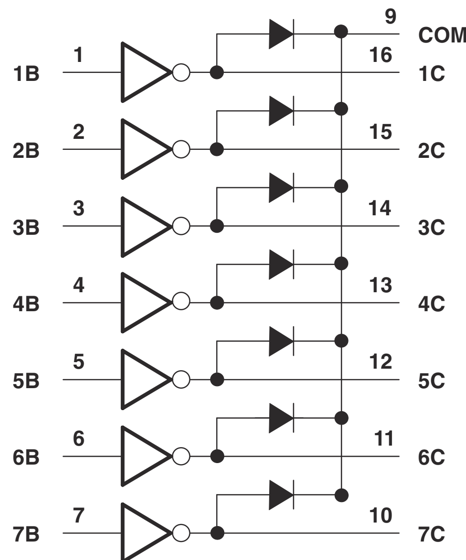
ULQ200xA-Q1 デバイスは、高電圧、大電流ダーリントン トランジスタ アレイです。各トランジスタ アレイは、誘導性負荷をスイッチングするための高電圧の出力と共通カソード クランプ ダイオードの内蔵を特長とする 7 つの NPN ダーリントン ペアで構成されています。1 つのダーリントン ペアのコレクタ電流定格は 500mA です。ダーリントン ペアを並列に接続し、大電流に対応することもできます。

ULQ2003A-Q1 は、TTL または 5V CMOS デバイスで直接駆動できるように、各ダーリントン ペアにつき 1 つの 2.7kΩ 直列ベース抵抗を内蔵しています。ULQ2004A-Q1 は、6V～15V の電源電圧を使用する CMOS デバイスで直接動作できるように、10.5kΩ の直列ベース抵抗を内蔵しています。ULQ2004A-Q1 に必要な入力電流は、ULQ2003A-Q1 に必要な入力電流よりも小さいです。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
ULQ2003A-Q1	SOIC (16)	9.90mm × 3.90mm
	TSSOP (16)	5.00mm × 4.40mm
	SOT (16)	4.20 mm × 2.00 mm
ULQ2004A-Q1	SOIC (16)	9.90mm × 3.90mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略ブロック図

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

Table of Contents

1 特長.......... 1
2 アプリケーション.......... 1
3 概要.......... 1
4 Pin Configuration and Functions.......... 2
5 Specifications.......... 4
5.1 Absolute Maximum Ratings.......... 4
5.2 ESD Ratings.......... 4
5.3 Recommended Operating Conditions.......... 4
5.4 Thermal Information.......... 4
5.5 Electrical Characteristics, ULQ2003AT and ULQ2003AQ.......... 5
5.6 Electrical Characteristics, ULQ2004AT.......... 5
5.7 Switching Characteristics, ULQ2003A and ULQ2004A.......... 6
5.8 Dissipation Ratings.......... 6
5.9 Typical Characteristics.......... 6
6 Parameter Measurement Information.......... 7
7 Detailed Description.......... 11
7.1 Overview.......... 11
7.2 Functional Block Diagram.......... 11
7.3 Feature Description.......... 12
7.4 Device Functional Modes.......... 12
8 Application and Implementation.......... 13
8.1 Application Information.......... 13
8.2 Typical Application.......... 13
8.3 System Examples.......... 16
8.4 Power Supply Recommendations.......... 16
8.5 Layout.......... 16
9 Device and Documentation Support.......... 18
9.1 Related Links.......... 18
9.2 サポート・リソース.......... 18
9.3 Trademarks.......... 18
9.4 静電気放電に関する注意事項.......... 18
9.5 用語集.......... 18
10 Revision History.......... 18
11 Mechanical, Packaging, and Orderable Information.......... 19

4 Pin Configuration and Functions

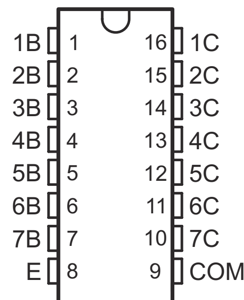


図 4-1. D or PW Package, 16-Pin SOIC or TSSOP (Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1B	I	Channel 1 through 7 Darlington base input.
2	2B		
3	3B		
4	4B		
5	5B		
6	6B		
7	7B		
8	E	—	Common emitter shared by all channels (typically tied to ground).
9	COM	—	Common cathode node for flyback diodes (required for inductive loads).

Copyright © 2024 Texas Instruments Incorporated

表 4-1. Pin Functions (続き)

PIN		I/O	DESCRIPTION
NO.	NAME		
10	7C	O	Channel 1 through 7 Darlington collector output.
11	6C		
12	5C		
13	4C		
14	3C		
15	2C		
16	1C		

5 Specifications

5.1 Absolute Maximum Ratings

at 25°C free-air temperature (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CE}	Collector-emitter voltage			50	V
	Clamp diode reverse voltage[2]			50	V
V_I	Input voltage[2]			30	V
	Peak collector current	See 図 8-2		500	mA
I_{OK}	Output clamp current			500	mA
	Total emitter-terminal current			–2.5	A
P_D	Continuous total power dissipation		See セクション 5.8		
T_A	Operating free-air temperature	ULQ200xAT	–40	105	°C
		ULQ200xAQ	–40	125	
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under セクション 5.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the emitter/substrate terminal E, unless otherwise noted.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CE}	Collector-emitter voltage	0	50	V
T_J	Junction temperature	–40	125	°C

5.4 Thermal Information

THERMAL METRIC[1]		ULQ2003A-Q1, ULQ2004A-Q1	ULQ2003A-Q1		UNIT
		D (SOIC)	PW (TSSOP)	DYY (SOT)	
		16 PINS	16 PINS	16 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	87.9	112.9	119.4	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	49.4	49.2	56.9	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	49.1	58.1	52.3	°C/W
$Ψ_{JT}$	Junction-to-top characterization parameter	11.9	9.1	2.8	°C/W
$Ψ_{JB}$	Junction-to-board characterization parameter	48.6	57.6	51.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2024 Texas Instruments Incorporated

5.5 Electrical Characteristics, ULQ2003AT and ULQ2003AQ

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$V_{I(on)}$	On-state input voltage	V_{CE} = 2 V, see 図 6-8	I_C = 200 mA				2.7	V
			I_C = 250 mA				2.9	
			I_C = 300 mA				3	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_I = 250 µA,I_C = 100 mA, see 図 6-7		ULQ2003AT		0.9	1.2	V
				ULQ2003AQ		1	1.3	
		I_I = 350 µA,I_C = 200 mA, see 図 6-7		ULQ2003AT		1	1.4	
				ULQ2003AQ		1	1.5	
		I_I = 500 µA,I_C = 350 mA, see 図 6-7		ULQ2003AT		1.2	1.7	
				ULQ2003AQ		1.2	1.8	
I_{CEX}	Collector cutoff current	V_{CE} = 50 V, I_I = 0, see 図 6-1	T_A = 25°C				100	µA
			T_A = 105°C, ULQ2003AT				165	
V_F	Clamp forward voltage	I_F = 350 mA, see 図 6-6				1.7	2.2	V
$I_{I(off)}$	Off-state input current	V_{CE} = 50 V, I_C = 500 µA, see 図 6-3			30	65		µA
I_I	Input current	V_I = 3.85 V, see 図 6-4				0.93	1.35	mA
I_R	Clamp reverse current	V_R = 50 V, T_A = 25°C, see 図 6-5					100	µA
C_i	Input capacitance	V_I = 0, f = 1 MHz				15	25	pF

5.6 Electrical Characteristics, ULQ2004AT

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{I(on)}$	On-state input voltage	V_{CE} = 2 V, see 図 6-8	I_C = 125 mA			5	V
			I_C = 200 mA			6	
			I_C = 275 mA			7	
			I_C = 350 mA			8	
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_I = 250 µA, I_C = 100 mA, see 図 6-7			0.9	1.1	V
		I_I = 350 µA, I_C = 200 mA, see 図 6-7			1	1.3	
		I_I = 500 µA, I_C = 350 mA, see 図 6-7			1.2	1.6	
I_{CEX}	Collector cutoff current	V_{CE} = 50 V, I_I = 0, see 図 6-1	T_A = 25°C			50	µA
			T_A = 105°C				
		V_{CE} = 50 V, see 図 6-2	I_I = 0			100	
			V_I = 1 V			500	
V_F	Clamp forward voltage	I_F = 350 mA, see 図 6-6			1.7	2.1	V
$I_{I(off)}$	Off-state input current	V_{CE} = 50 V, I_C = 500 µA, see 図 6-3		50	65		µA
I_I	Input current	V_I = 5 V, see 図 6-4			0.35	0.5	mA
		V_I = 12 V, , see 図 6-4			1	1.45	
I_R	Clamp reverse current	V_R = 50 V, see 図 6-5	T_A = 25°C			50	µA
			T_A = 105°C			100	
C_i	Input capacitance	V_I = 0, f = 1 MHz			15	25	pF

Copyright © 2024 Texas Instruments Incorporated

5.7 Switching Characteristics, ULQ2003A and ULQ2004A

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	See 図 6-9		1	10	µs
t_{PHL}	Propagation delay time, high- to low-level output	See 図 6-9		1	10	µs
V_{OH}	High-level output voltage after switching	V_S = 50 V, I_O = 300 mA, see 図 6-10	V_S – 500			mV

5.8 Dissipation Ratings

PACKAGE	T_A = 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING	T_A = 105°C POWER RATING	T_A = 125°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW	342 mW	190 mW

5.9 Typical Characteristics

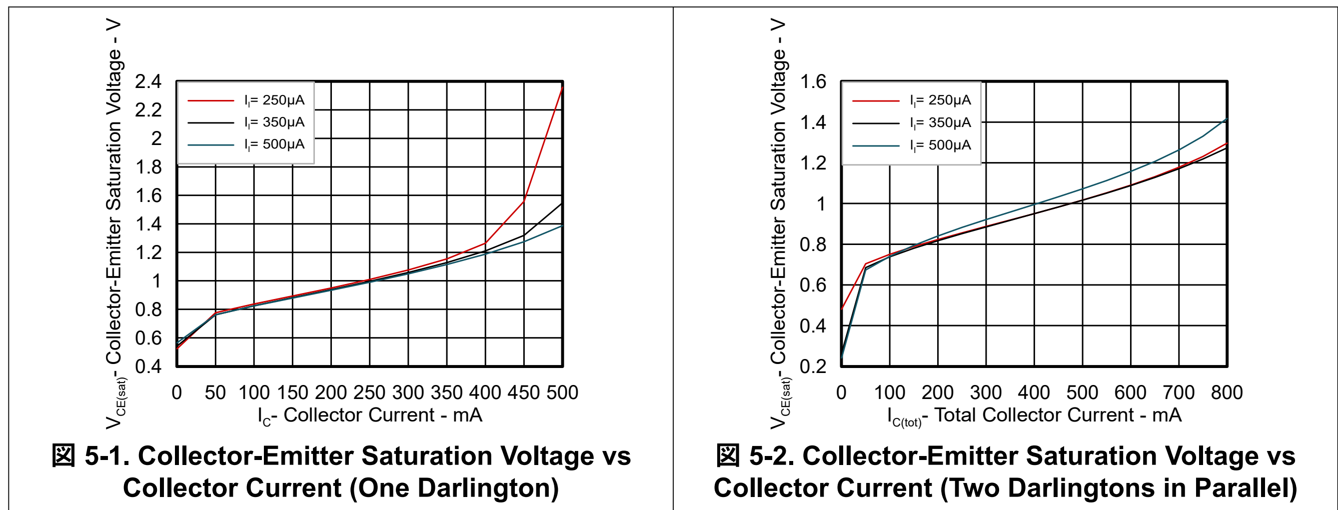


図 5-1. Collector-Emitter Saturation Voltage vs Collector Current (One Darlington)

図 5-2. Collector-Emitter Saturation Voltage vs Collector Current (Two Darlingtons in Parallel)

Copyright © 2024 Texas Instruments Incorporated

6 Parameter Measurement Information

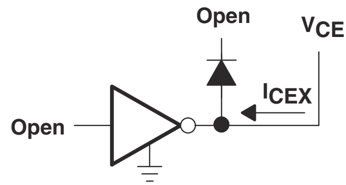


図 6-1. I_{CEX} Test Circuit

Copyright © 2024 Texas Instruments Incorporated

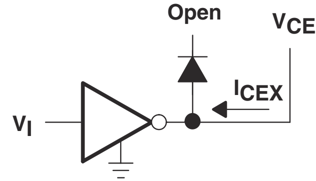


図 6-2. I_{CEX} Test Circuit

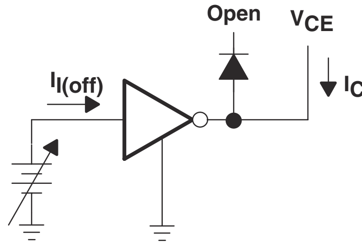


図 6-3. $I_{I(off)}$ Test Circuit

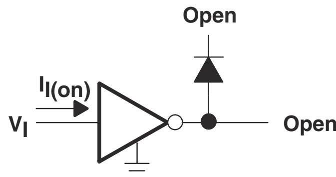


図 6-4. I_I Test Circuit

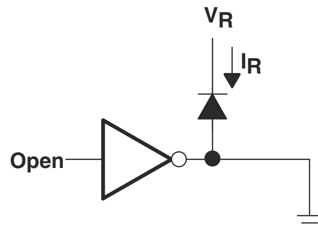


図 6-5. I_R Test Circuit

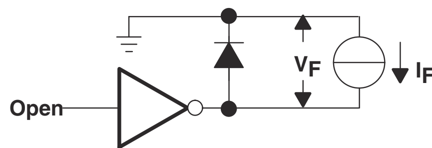
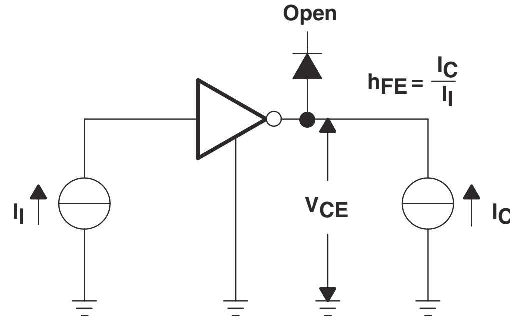


図 6-6. V_F Test Circuit

Copyright © 2024 Texas Instruments Incorporated



A. I_I is fixed for measuring $V_{CE(sat)}$, variable for measuring h_{FE}.

図 6-7. h_{FE}, $V_{CE(sat)}$ Test Circuit

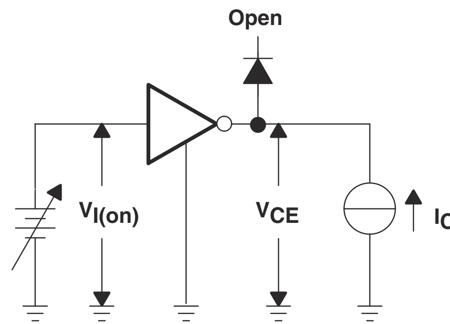


図 6-8. $V_{I(on)}$ Test Circuit

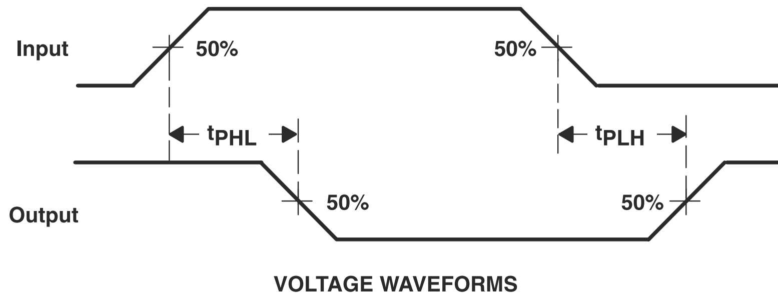
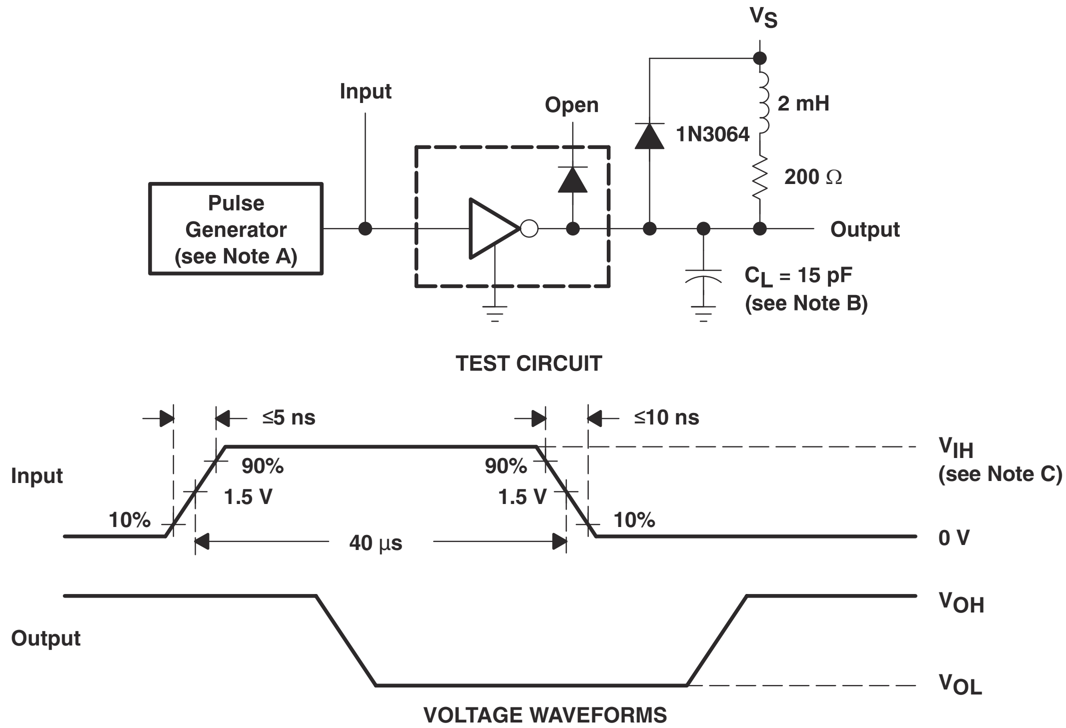


図 6-9. Propagation Delay-Time Waveforms



A. The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

C. For testing the ULQ2003A, V_{IH} = 3 V; for the ULQ2004A, V_{IH} = 8 V.

図 6-10. Latch-Up Test Circuit and Voltage Waveforms

Copyright © 2024 Texas Instruments Incorporated

7 Detailed Description

7.1 Overview

This standard device has proven ubiquity and versatility across a wide range of applications. This is due to integration of 7 Darlington transistors of the device that are capable of sinking up to 500 mA and wide GPIO range capability.

The ULQ200xA-Q1 devices comprise seven high-voltage, high-current NPN Darlington transistor pairs. All units feature a common emitter and open collector outputs. To maximize their effectiveness, these units contain suppression diodes for inductive loads. The ULNQ200xA-Q1 devices have a series base resistor to each Darlington pair, thus allowing operation directly with TTL or CMOS operating at supply voltages of 5 V or 3.3 V. The ULQ2003xA-Q1 device offers solutions to a great many interface needs, including solenoids, relays, lamps, small motors, and LEDs. Applications requiring sink currents beyond the capability of a single output may be accommodated by paralleling the outputs.

This device can operate over a wide temperature range (–40°C to 105°C for ULQ200xAT or –40°C to 125°C for ULQ2003AQ).

7.2 Functional Block Diagram

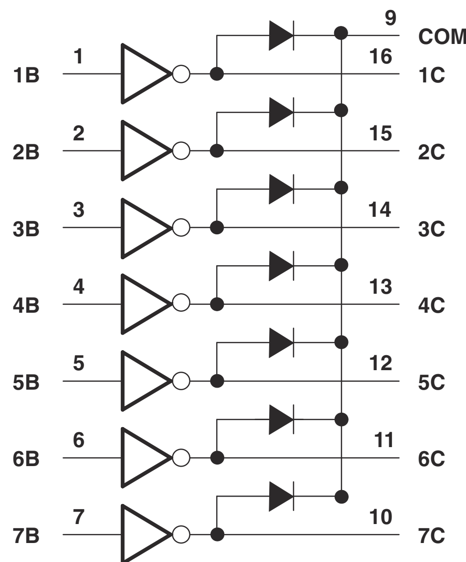
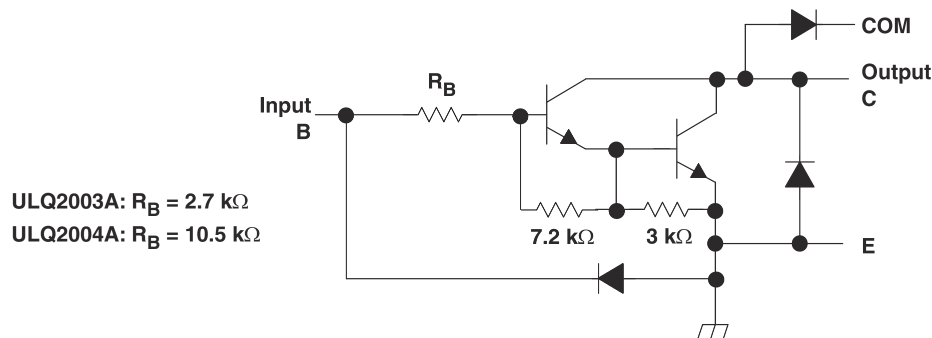


図 7-1. Logic Diagram



A. All resistor values shown are nominal.

B. The collector-emitter diode is a parasitic structure and should not be used to conduct current. If the collector(s) go below ground an external Schottky diode should be added to clamp negative undershoots.

図 7-2. Schematics (Each Darlington Pair)

Copyright © 2024 Texas Instruments Incorporated

7.3 Feature Description

Each channel of the ULQ200xA-Q1 devices consist of Darlington connected NPN transistors. This connection creates the effect of a single transistor with a very high-current gain (β2). This can be as high as 10,000 A/A at certain currents. The very high β allows for high-output current drive with a very low input current, essentially equating to operation with low GPIO voltages.

The GPIO voltage is converted to base current through the 2.7-kΩ or 10.5-kΩ resistor connected between the input and base of the predriver Darlington NPN. The 7.2-kΩ and 3-kΩ resistors connected between the base and emitter of each respective NPN act as pulldowns and suppress the amount of leakage that may occur from the input.

The diodes connected between the output and COM pin is used to suppress the kick-back voltage from an inductive load that is excited when the NPN drivers are turned off (stop sinking) and the stored energy in the coils causes a reverse current to flow into the coil supply through the kick-back diode.

In normal operation the diodes on base and collector pins to emitter will be reversed biased. If these diodes are forward biased, internal parasitic NPN transistors will draw (a nearly equal) current from other (nearby) device pins.

7.4 Device Functional Modes

7.4.1 Inductive Load Drive

When the COM pin is tied to the coil supply voltage, ULQ200xA-Q1 devices are able to drive inductive loads and suppress the kick-back voltage through the internal free-wheeling diodes.

7.4.2 Resistive Load Drive

When driving a resistive load, a pullup resistor is needed in order for the ULQ200xA-Q1 devices to sink current and for there to be a logic high level. The COM pin can be left floating for these applications.

Copyright © 2024 Texas Instruments Incorporated

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

Typically, the ULQ200xA-Q1 device drives a high-voltage or high-current (or both) peripheral from an MCU or logic device that cannot tolerate these conditions. This design is a common application of ULQ200xA-Q1 device, driving inductive loads. This includes motors, solenoids and relays. 図 8-1 shows an example of driving multiple inductive loads.

8.2 Typical Application

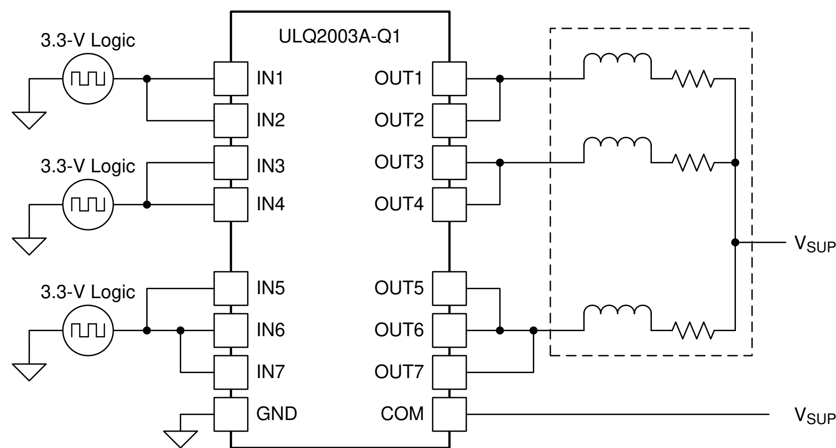


図 8-1. ULQ2003A-Q1 Device as Inductive Load Driver

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
GPIO voltage	3.3 V or 5 V
Coil supply voltage	12 V to 48 V
Number of channels	7
Output current (R_{COIL})	20 mA to 300 mA per channel
Duty cycle	100%

8.2.2 Detailed Design Procedure

When using ULQ2003A-Q1 device in a coil driving application, determine the following:

- Input voltage range
- Temperature range
- Output and drive current
- Power dissipation

8.2.2.1 Drive Current

The coil voltage (V_{SUP}), coil resistance (R_{COIL}), and low-level output voltage ($V_{CE(SAT)}$ or V_{OL}) determine the coil current.

$$I_{COIL} = (V_{SUP} - V_{CE(SAT)}) / R_{COIL} \quad (1)$$

8.2.2.2 Low-Level Output Voltage

The low-level output voltage (V_{OL}) is the same as $V_{CE(SAT)}$ and can be determined by, 図 5-1 or 図 5-2.

8.2.2.3 Power Dissipation and Temperature

The number of coils driven is dependent on the coil current and on-chip power dissipation. The number of coils driven can be determined by 図 8-2.

For a more accurate determination of number of coils possible, use 式 2 to calculate ULQ200xA-Q1 device on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li} \quad (2)$$

where

- N is the number of channels active together
- V_{OLi} is the OUT_i pin voltage for the load current I_{Li}. This is the same as $V_{CE(SAT)}$

To ensure reliability of ULQ200xA-Q1 device and the system, the on-chip power dissipation must be lower that or equal to the maximum allowable power dissipation ($PD_{(MAX)}$) dictated by 式 3.

$$PD_{(MAX)} = \frac{\left(T_{J(MAX)} - T_A\right)}{\theta_{JA}} \quad (3)$$

where

- $T_{J(max)}$ is the target maximum junction temperature
- T_A is the operating ambient temperature
- $R_{\theta JA}$ is the package junction to ambient thermal resistance

Limit the die junction temperature of the ULQ200xA-Q1 device to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation.

Copyright © 2024 Texas Instruments Incorporated

8.2.3 Application Curve

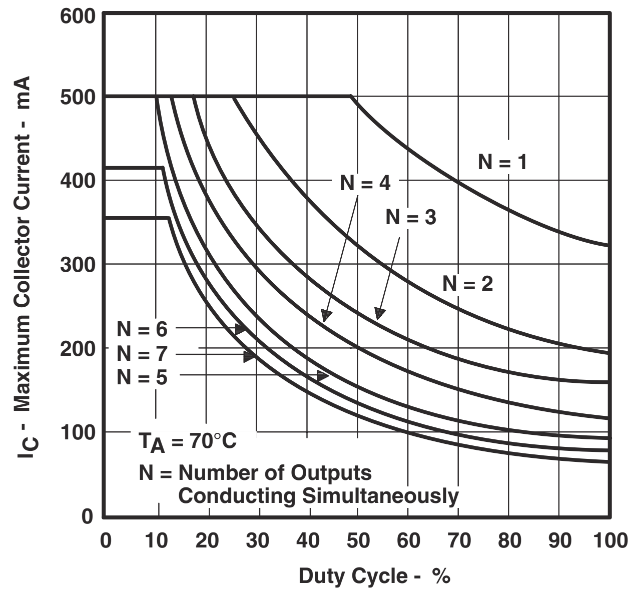


図 8-2. D Package Maximum Collector Current vs Duty Cycle

8.3 System Examples

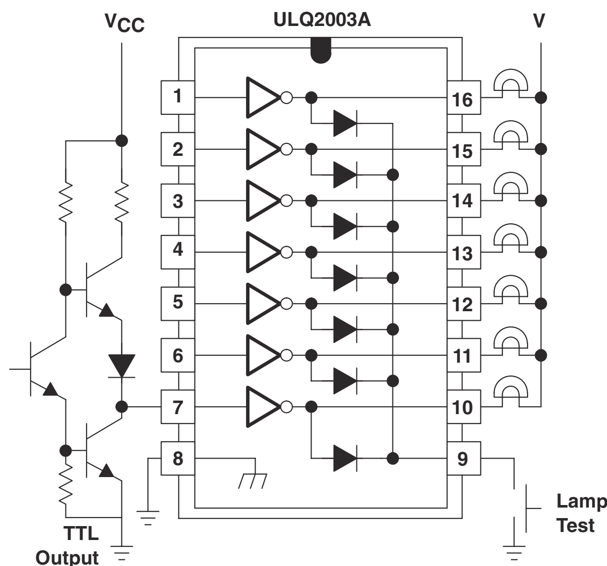


図 8-3. TTL to Load

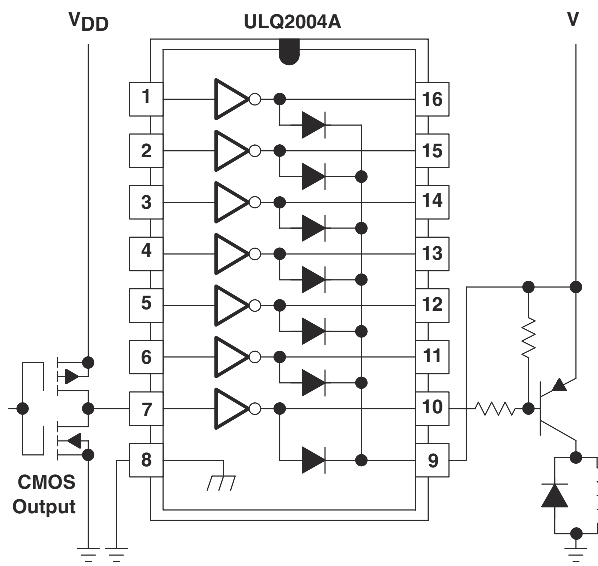


図 8-4. Buffer for Higher Current Loads

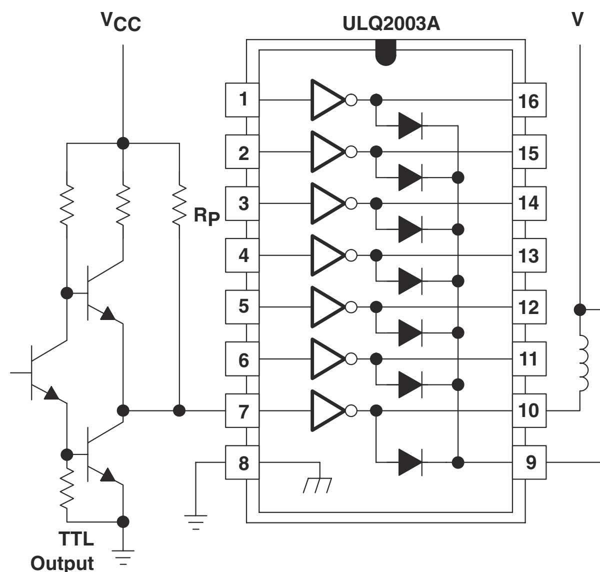


図 8-5. Use of Pullup Resistors to Increase Drive Current

8.4 Power Supply Recommendations

This device does not need a power supply. However, the COM pin is typically tied to the system power supply. When this is the case, it is very important to ensure that the output voltage does not heavily exceed the COM pin voltage. This discrepancy heavily forward biases the fly-back diodes and causes a large current to flow into COM, potentially damaging the on-chip metal or over-heating the device.

8.5 Layout

8.5.1 Layout Guidelines

Thin traces can be used on the input due to the low-current logic that is typically used to drive the ULQ200xA-Q1 devices. Take care to separate the input channels as much as possible, as to eliminate crosstalk. TI

Copyright © 2024 Texas Instruments Incorporated

recommends thick traces for the output to drive whatever high currents that may be needed. Wire thickness can be determined by the current density of the trace material and desired drive current.

Because all of the channels currents return to a common emitter, it is best to size that trace width to be very wide. Some applications require up to 2.5 A.

8.5.2 Layout Example

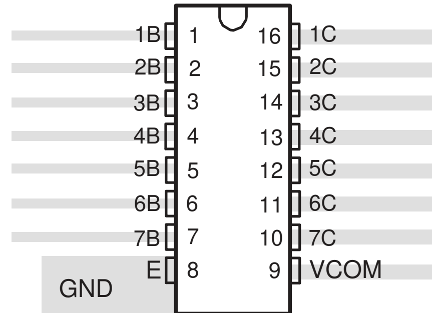


図 8-6. Package Layout

9 Device and Documentation Support

9.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ULQ2003A-Q1	Click here	Click here	Click here	Click here	Click here
ULQ2004A-Q1	Click here	Click here	Click here	Click here	Click here

9.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

9.3 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (November 2014) to Revision F (June 2024) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新........1
- データシート全体にわたって DYY パッケージを追加........1

Changes from Revision D (April 2010) to Revision E (November 2014) — **Page**

- 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加........1

Copyright © 2024 Texas Instruments Incorporated

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ULQ2003AQDRQ1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ULQ2003AQ	Samples
ULQ2003AQDYYRQ1	ACTIVE	SOT-23-THIN	DYY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	U2003AQ	Samples
ULQ2003ATDG4Q1	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 105	ULQ2003AT	
ULQ2003ATDQ1	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 105	ULQ2003AT	
ULQ2003ATDRG4Q1	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 105	ULQ2003AT	
ULQ2003ATDRQ1	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 105	ULQ2003AT	
ULQ2003ATPWRQ1	ACTIVE	TSSOP	PW	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	U2003AT	Samples
ULQ2004ATDRG4Q1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULQ2004AT	Samples
ULQ2004ATDRQ1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ULQ2004AT	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

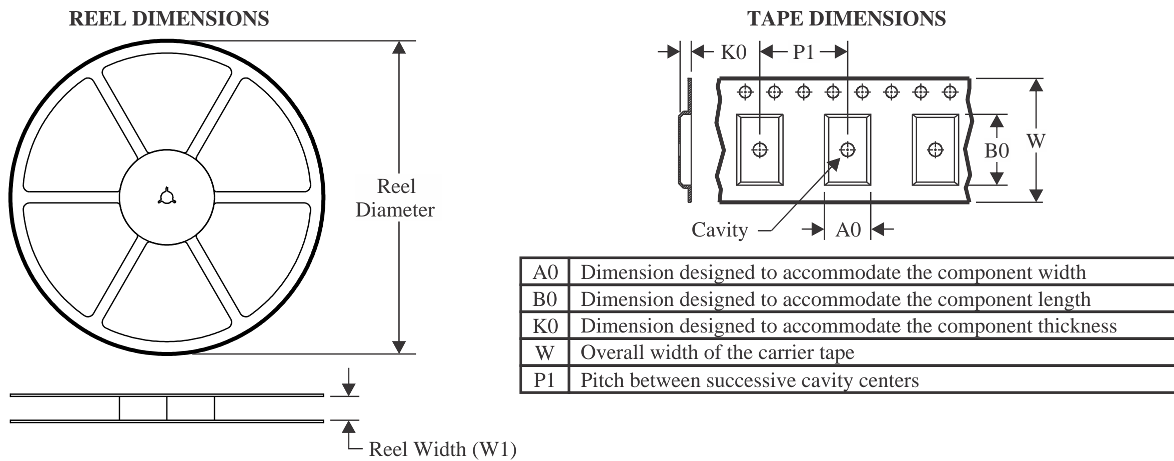
OTHER QUALIFIED VERSIONS OF ULQ2003A-Q1, ULQ2004A-Q1 :

- Catalog : ULQ2003A, ULQ2004A

NOTE: Qualified Version Definitions:

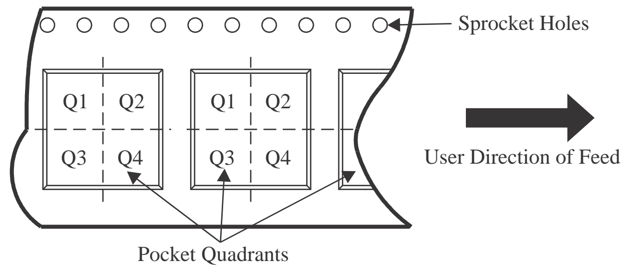
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



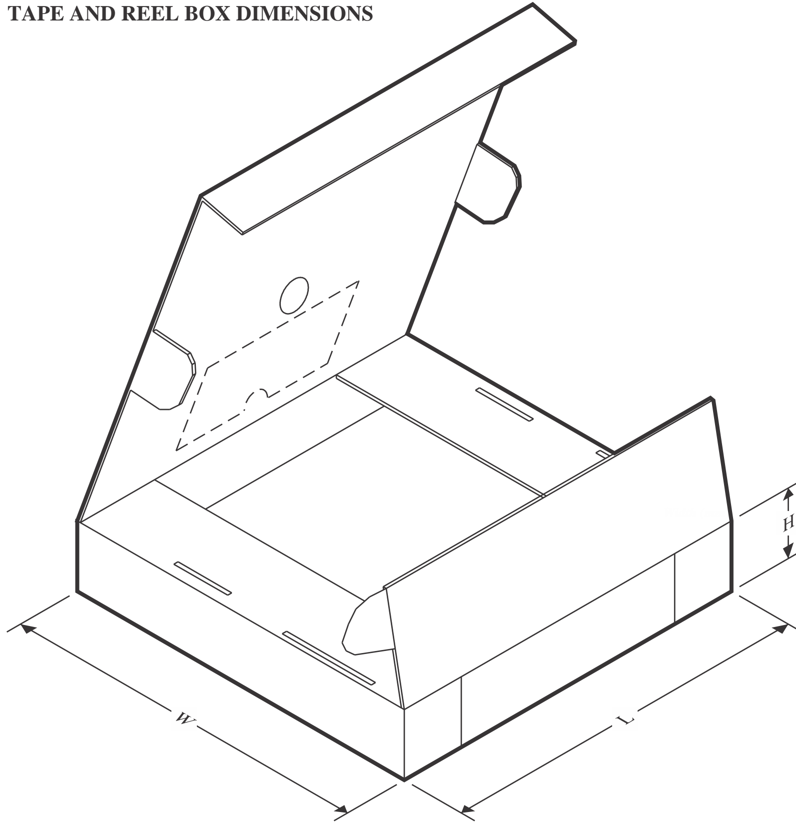
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

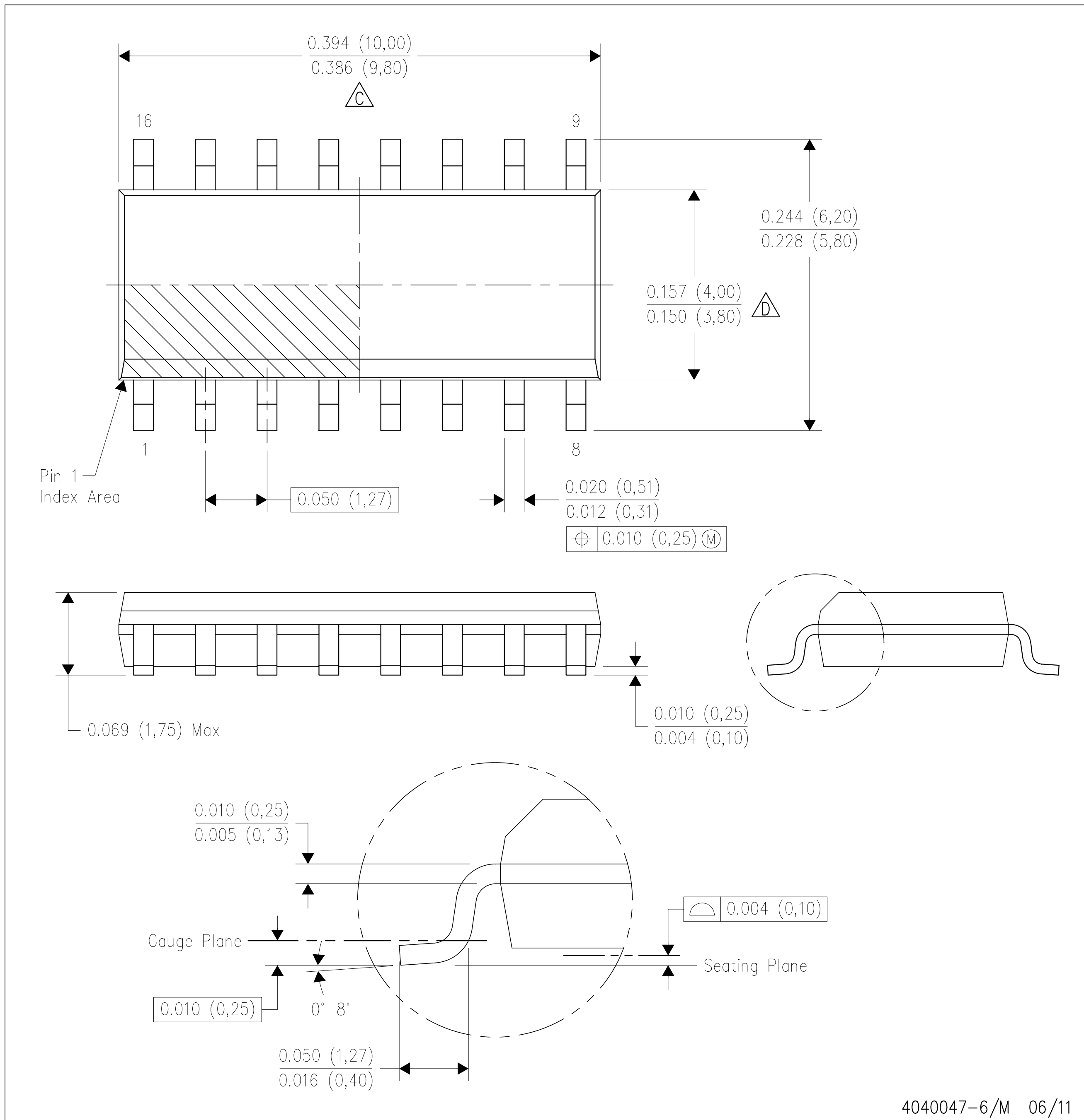
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ULQ2003AQDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULQ2003AQDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULQ2003AQDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
ULQ2003AQDYYRQ1	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
ULQ2003ATPWRQ1	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ULQ2004ATDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1



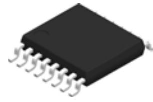
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ULQ2003AQDRQ1	SOIC	D	16	2500	353.0	353.0	32.0
ULQ2003AQDRQ1	SOIC	D	16	2500	340.5	336.1	32.0
ULQ2003AQDRQ1	SOIC	D	16	2500	356.0	356.0	35.0
ULQ2003AQDYYRQ1	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
ULQ2003ATPWRQ1	TSSOP	PW	16	2500	356.0	356.0	35.0
ULQ2004ATDRQ1	SOIC	D	16	2500	353.0	353.0	32.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

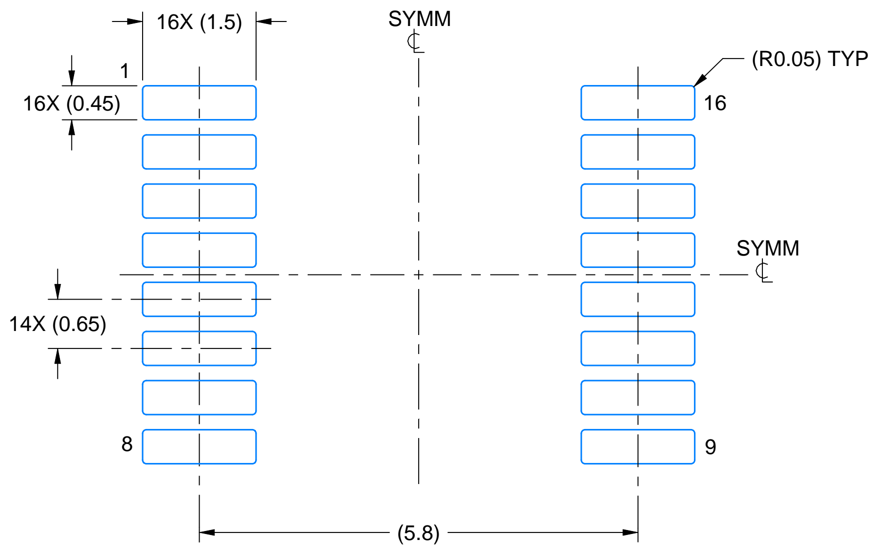
SMALL OUTLINE PACKAGE

SEATING PLANE
C
0.1 C
6.6
6.2
TYP
A
PIN 1 INDEX AREA
14X 0.65
16
1
2X
4.55
5.1
4.9
NOTE 3
8
9
16X 0.30
0.19
0.1 Ⓜ C A B
B
4.5
4.3
NOTE 4
1.2 MAX
(0.15) TYP
SEE DETAIL A
0.25
GAGE PLANE
0.15
0.05
0° -8°
0.75
0.50
DETAIL A
TYPICAL

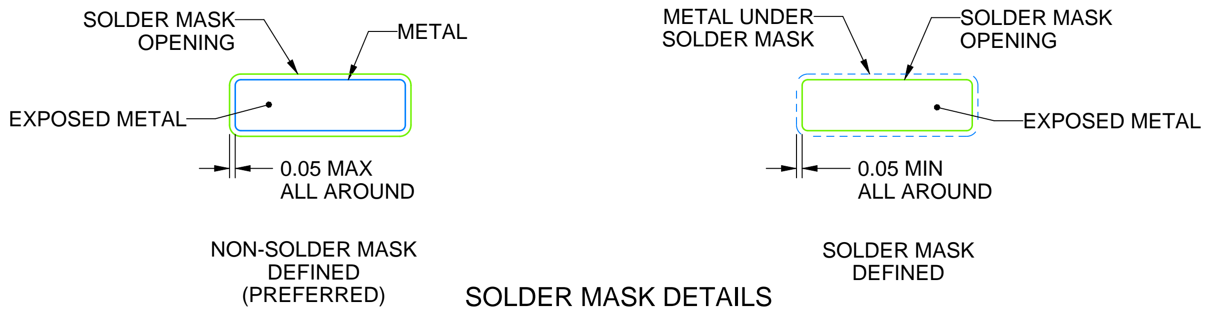
4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

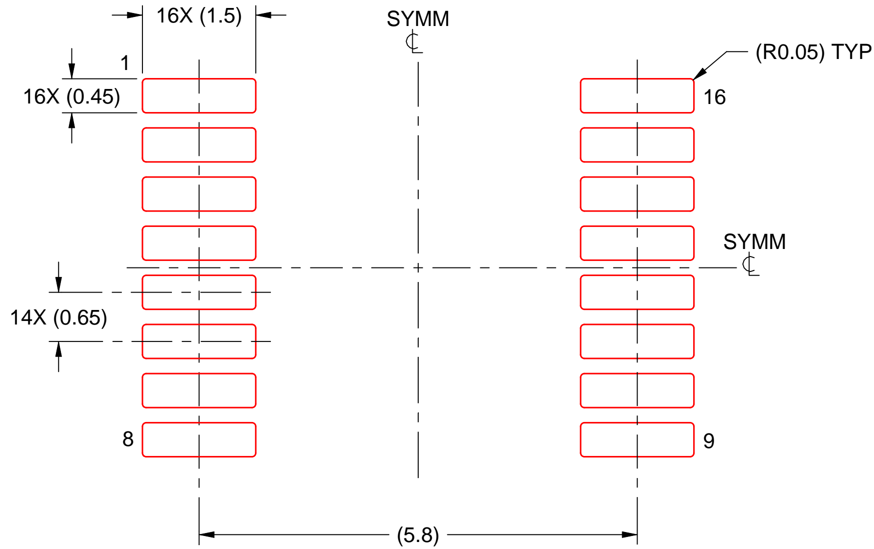


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

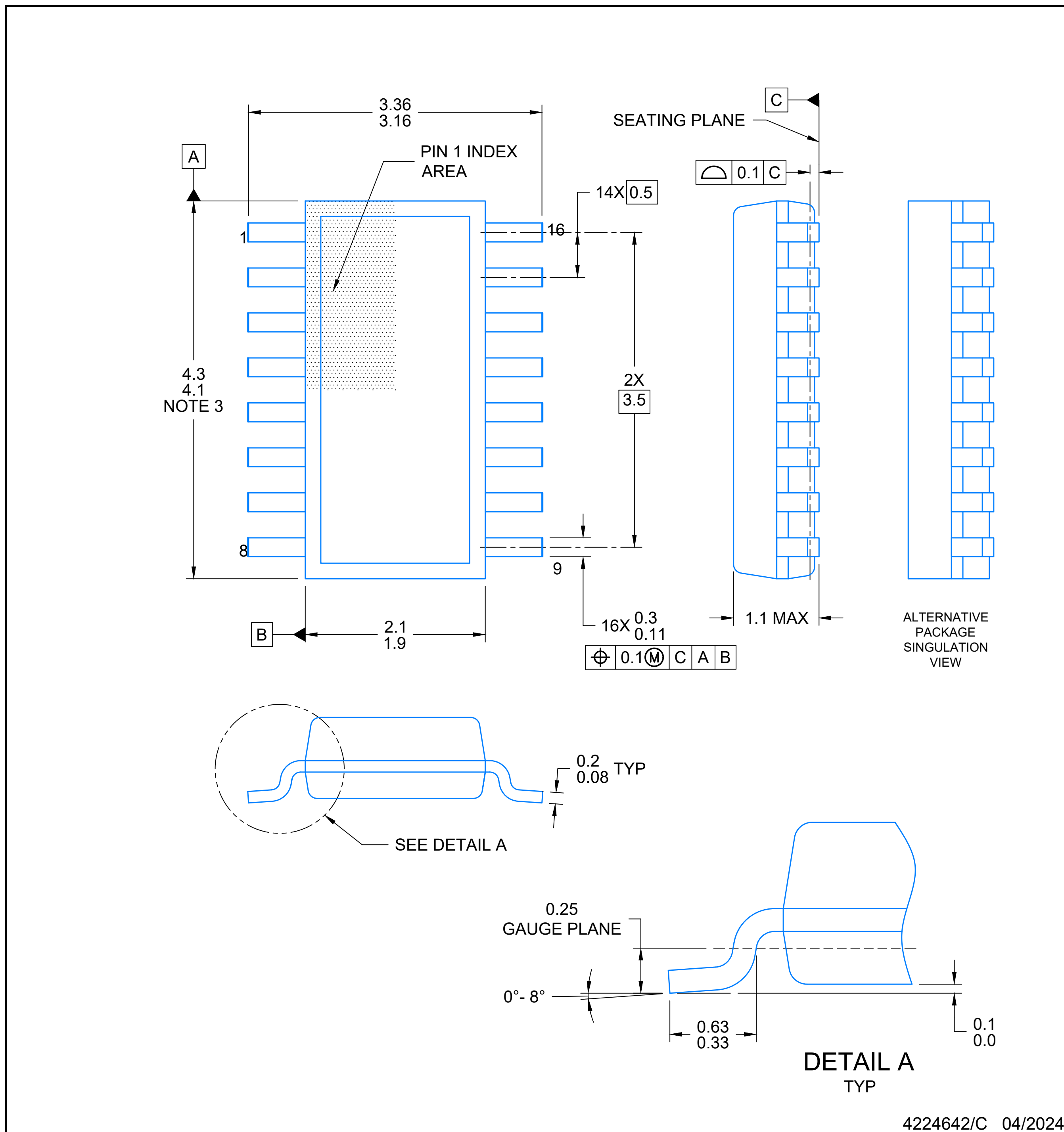


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

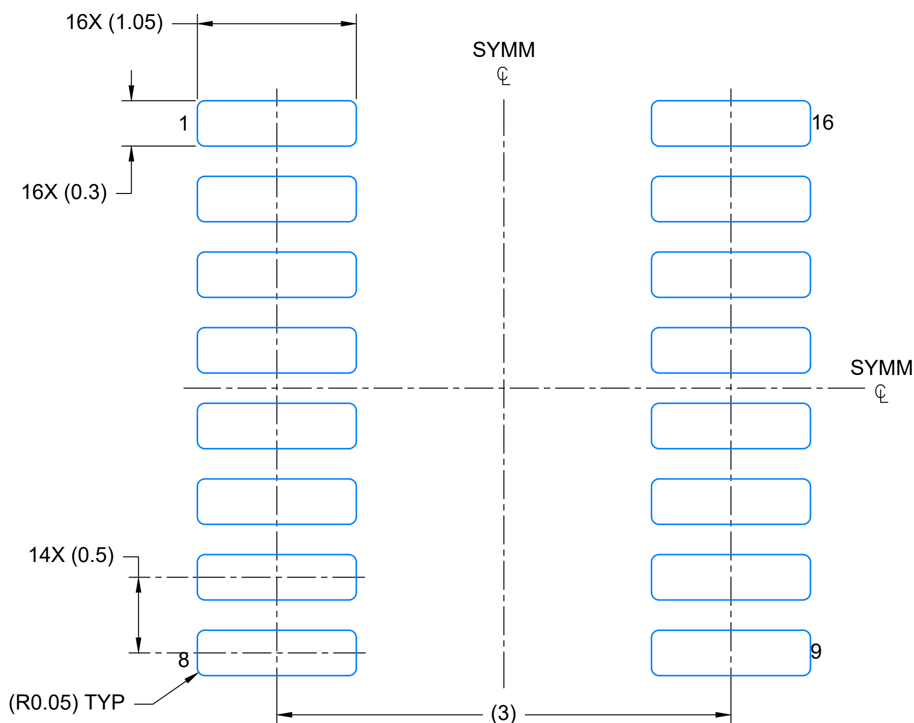
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

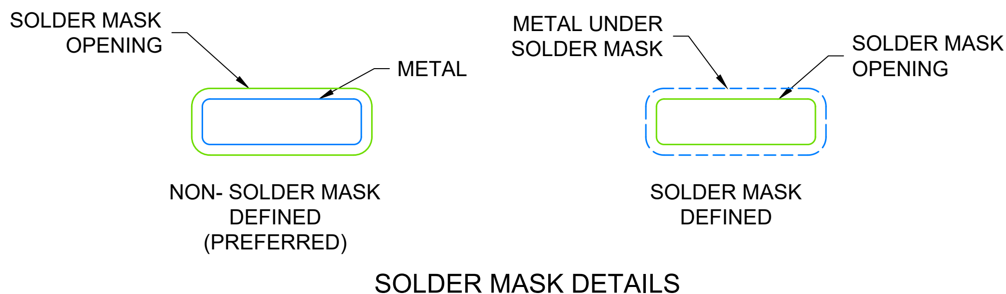


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

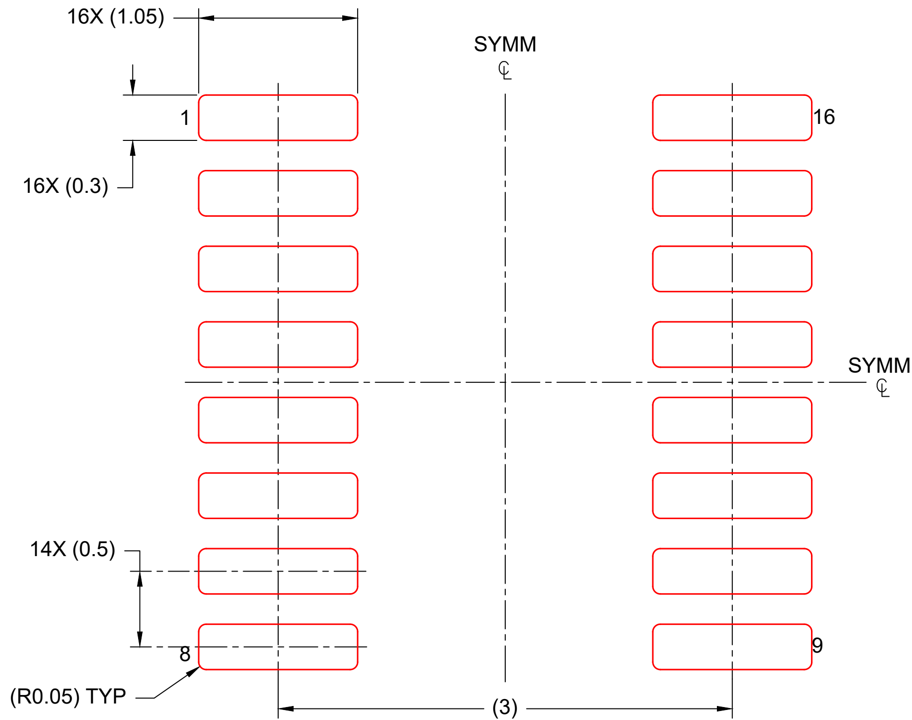


SOLDER MASK DETAILS

4224642/C 04/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/C 04/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated