参考資料

デザイン・ガイド: TIDA-00080
絶縁型デルタ・シグマ変調器を使用した AC/DC 電圧および電流測定モジュールのリファレンス・デザイン

概要

このリファレンス・デザインでは、基本または強化絶縁を備えた絶縁型デルタ・シグマ変調器を使用して、チャネル絶縁入力として構成された絶縁電流入力と、グループ絶縁入力として構成された絶縁電圧入力とを測定する多様な方法を紹介します。低ドロップアウト・レギュレータ (LDO) に接続するためのヘッドルームを織り込んで DC 出力を設定できる高効率絶縁型 DC/DC コンバータを使用すると、電源設計を簡素化し、性能と信頼性を高めることができます。性能を向上させコストを最適化するため、多様な入力電圧を選択できる各種デルタ・シグマ変調器ファミリをこのリファレンス・デザインで紹介しています。このモジュールを使用すると、大型変流器 (CT) を使用せずに高精度で電流を測定できます。

リソース

TIDA-00080	デザイン・ページ
AMC1304M25、AMC1306M25、UCC12050	プロダクト・フォルダ
SN6501DBV、TLV70450、TLV76050	プロダクト・フォルダ
AMC1311、AMC1336、OPA211ID	プロダクト・フォルダ
TPS7A3001、CDCE906、TPS55340	プロダクト・フォルダ
LP38798、TPS54232、REF3012	プロダクト・フォルダ
DAC8564、TMS320F28377D、AMC1106M05	プロダクト・フォルダ
TMDXCNCD28377D	ツール・フォルダ

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特長

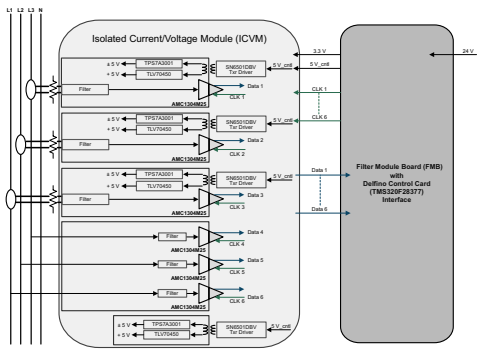
- ±250mV、±1V、0～2V の入力範囲のデルタ・シグマ変調器により、センサ・インターフェイスの電圧および電流入力測定の柔軟性を向上
- 基本または強化絶縁を利用することで、設計の柔軟性を高めコストを最適化
- 共通電源によるグループ絶縁電圧の測定 (コストを最適化) と個別電源によるチャネル絶縁電流の測定が可能
- 安定化電源の生成に使用する柔軟な出力を備えた、高効率絶縁型 DC/DC コンバータを使用した絶縁型電源
- DC および AC (50Hz) 入力で ±0.5% 未満の精度を達成
- デルタ・シグマ変調器と絶縁型 DC/DC コンバータにより 7000V_{PEAK} の強化絶縁を実現

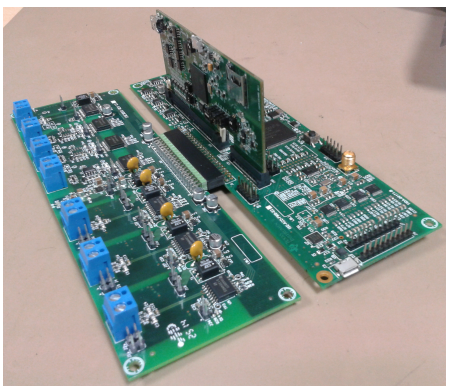
以下を備えたフィルタ・モジュール・ボード(FMB):

- F2837xD デュアルコア Delfino™マイクロコントローラ・モジュールを接続可能
- プログラマブル 3 PLL クロック・シンセサイザ / マルチプライヤ / デバイダ

アプリケーション

- 保護リレーおよびIED
- 多相エネルギー・メータ





1 System Description

Current measurement is a critical requirement in protection, substation automation, power quality, and measurement. Different current sensors are used to measure current. The most common sensor technologies today are the current transformer (CT) and the low resistance current shunt. The following sections a provide a brief explanation of the two types of sensors.

1.1 Current Transformer

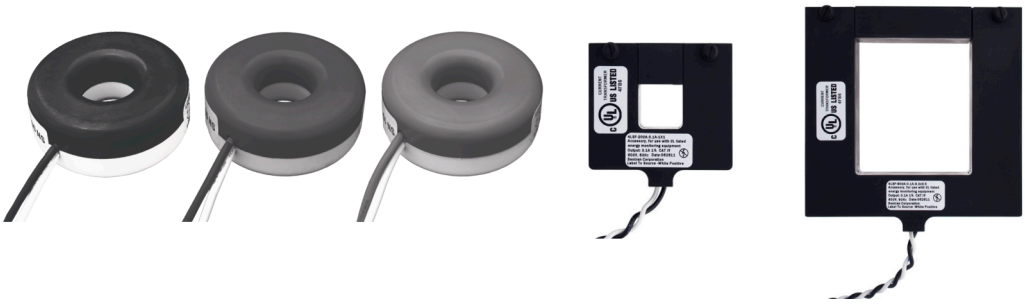


図 1. Current Transformer

A CT is a transformer that converts the primary current into a smaller secondary current. The CT is the most common sensor used for measurement and can measure up to a very high current while consuming very little power. Because of the magnetizing current, the CT typically has a small phase shift associated with it (0.1º to 0.3º). If uncalibrated, the CT will lead to a noticeable error at a low-power factor. In addition, the ferrite material used in the core can saturate at a high current.

1.2 Low Resistance Shunt

The low resistance current shunt offers good accuracy at a low cost and the current measurement is simple. When performing a high-precision current measurement, consider the parasitic inductance of the shunt. The inductance is typically in the order of only a few nH. This inductance affects the shunt's impedance magnitude at a relatively high frequency. The shunt is rather low-cost and reliable and is a popular choice for measurement applications. However, because the current shunt is fundamentally a resistive element, the heat it generates is proportional to the square of the current passing through. Manganin is a copper-manganese resistance alloy used as shunts for current sensing in various high-current applications. The alloy has a low-temperature coefficient of resistivity with peak resistance at approximately 50°C. The thermal EMF versus copper is very low. 図 2 shows low-resistance shunts.

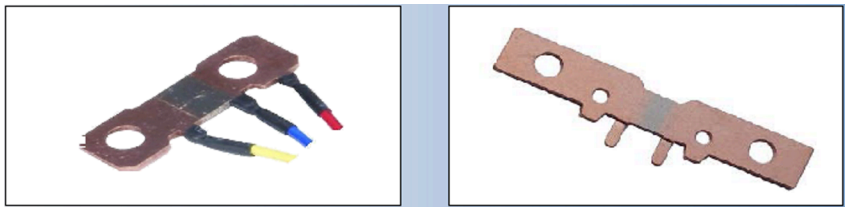


図 2. Shunt Resistors

1.3 CT and Shunt Comparison

表 1 shows the differences between the CT versus the shunt.

表 1. CT versus Shunt

CURRENT MEASUREMENT	ADVANTAGES	DISADVANTAGES
CT	Provides isolation	Measures only AC
	Lower VA loss	Size increases with current and has saturation problems
		Highly susceptible to stray AC magnetic fields
		Output is frequency dependent
Shunt	Reliable and smaller dimension	No electrical isolation
	Can measure AC and DC	Amplification required at output
	No DC offset	VA loss is shunt value dependent
	No current saturation problems	

1.4 Protection System

The main components of protection systems are:

- **External current and voltage transformer** (also called instrument transformers): Their purpose is to step down the current or voltage of a device to measurable values, within the instrumentation measurement range 5 A or 1 A in the case of a CTs, and 110 V or 230 V in the case of voltage or potential transformers (VTs or PTs). Therefore, protective equipment inputs are standardized within the ranges above.
- **Protective relays**: Intelligent electronic devices (IEDs) that receive measured signals from the secondary side of CTs and VTs and detect whether the protected unit is in a stressed condition (based on their type and configuration) or not. A trip signal is sent by protective relays to the circuit breakers to disconnect the faulty components from power system if necessary.
- **Circuit breakers**: Act upon open commands sent by protective relays when faults are detected and close commands when faults are cleared. They can also be manually opened, for example, to isolate a component for maintenance.
- **Communication channel**: Paths that deliver information and measurements from an initiating relay at one location to a receiving relay (or substation) at another location.

Protection relays play a critical role in electrical grid, substation, and distribution power systems. These relays protect the electrical power system against different electrical faults. The heart of this protection is a smart controlling unit that continuously monitors electrical parameters such as voltages, currents, and frequencies. The smart controlling unit also issues trip commands to appropriate circuit breakers during faults. There are different types of relays, depending upon the stage used, such as generator protection, distance protection, overvoltage protection, overcurrent protection, and differential protection.

1.5 AMC1304M25 ΔΣ Modulator

The AMC1304M25 module is a family of single-channel second-order ΔΣ modulators designed for medium- to high-resolution analog-to-digital conversions (ADC). The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. The isolated output of the converter (DATA) provides a stream of digital ones and zeroes. The time average of this serial output is proportional to the analog input voltage.

A differential input signal of 0 V ideally produces a stream of ones and zeroes that are high 50% of the time and low 50% of the time. The relation between ones and zeroes changes with the input signal. A positive input voltage of 250 mV (specified full-scale range) results in a bit stream with 90% ones, whereas a signal at negative full-scale (–250 mV) is only high 10% of the time. This specified FSR is also the linear range of the modulator with the performance as specified in this document.

The range between the specified FSR (±250 mV) and the absolute FSR (±312.5 mV) is the non-linear range of the modulator. The output of the modulator clips with a stream of only zeroes with an input less than or equal to the minimum value of the absolute FSR value or with a stream of only ones with an input greater than or equal to the positive value of the absolute FSR. The input voltage versus the output modulator signal is shown in 図 3.

The system clock to the AMC1304M25 is provided externally at the CLKIN pin. The data are synchronously provided at f_{CLKIN} at the DATA output pin. The data changes at the falling edge of CLKIN.

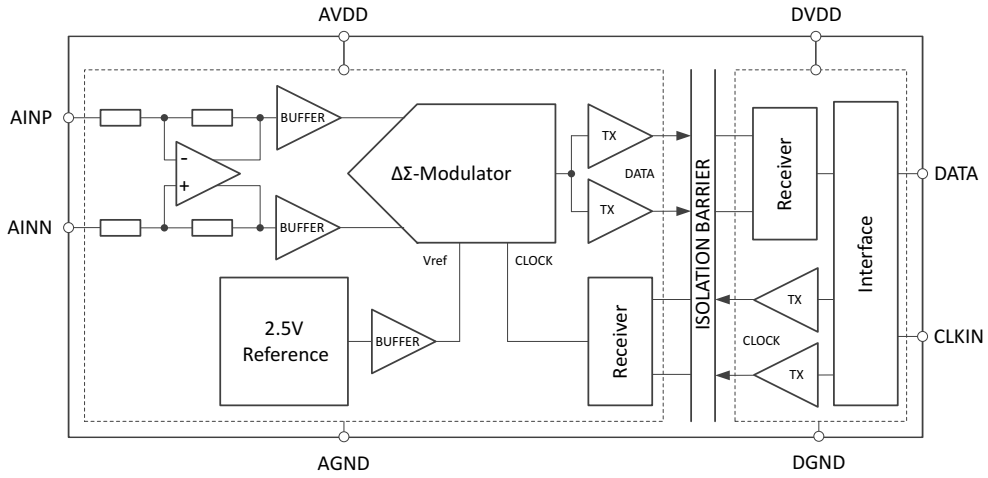


図 3. System Clock — CLKIN Pin

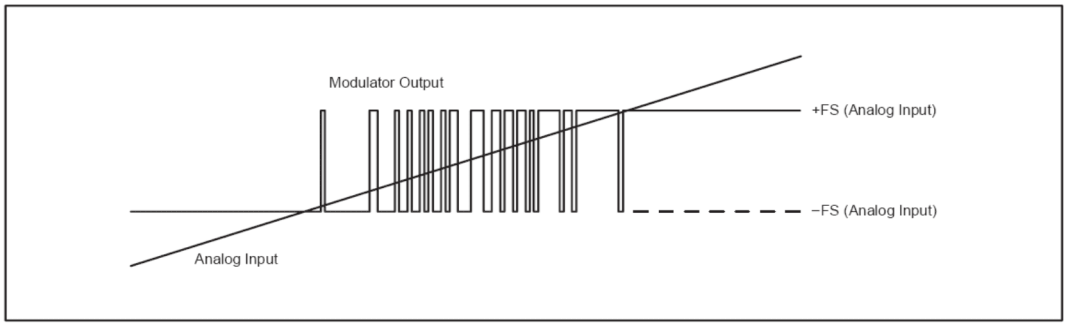


図 4. Modulator Output — Analog Input

Benefits of using AMC1304M25:

- Galvanic barrier provides EMI immunity and robust isolation barrier lifetime.
- Wide clock range gives sample rate flexibility for customer.
- Reduced input voltage range enables higher shunt currents.

1.6 Sinc (CIC) Filters

Cascaded integrator-comb (CIC) filters are multirate filters often used for implementing large sample rate changes in digital systems. CIC filters are typically employed in applications that have a large excess sample rate. The system sample rate is much larger than the bandwidth occupied by the processed signal. Implementations of CIC filters have structures that use only adders, subtracts, and delay elements. These structures make CIC filters appealing for their hardware-efficient implementations of multirate filtering.

The CIC decimator filter has two sections: an integrator section with N integrator stages that processes input data samples at sampling rate f_S, and a comb section that operates at the lower sampling rate f_S / R. This comb section consists of N comb stages with a differential delay of M samples per stage. The down sampling operation decimates the output of the integrator section by passing only every R^{th} sample to the comb section of the filter.

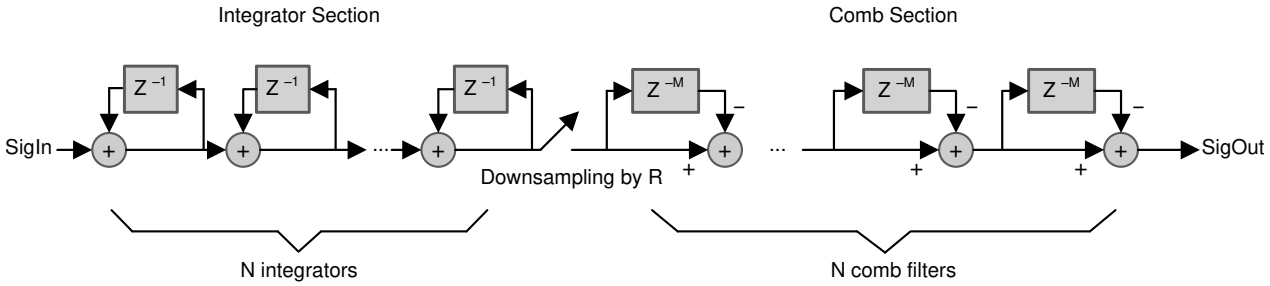


図 5. Sinc Filters

図 6 illustrates a CIC integrator stage. The difference equation that describes the integrator stage is given by

$$y(n) = x(n) + y(n-1) \tag{1}$$

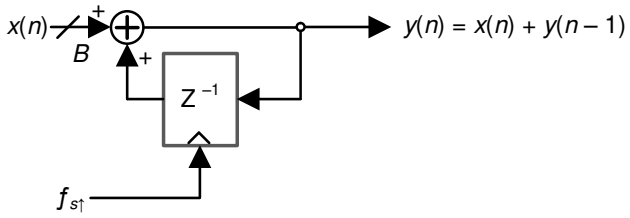


図 6. CIC Integrator Block Diagram

The corresponding z-transform and transfer function is given by

$$Y(z) = X(z) + z^{-1}Y(z)$$

$$H_I(z) = \frac{Y(z)}{X(z)}$$

$$H_I(z) = \frac{1}{1 - z^{-1}} \tag{2}$$

The N section cascade of integrators is given by

$$\left[H_I(z)\right]^N = \left[\frac{1}{1 - z^{-1}}\right]^N \tag{3}$$

1.6.1 CIC Comb Filter Stage

図 7 illustrates the general form of the comb filter architecture where the parameter M specifies the programmable comb filter differential delay. The output sequence generated by this structure is given by the difference equation

$$y(n) = x(n) - x(n - M) \tag{4}$$

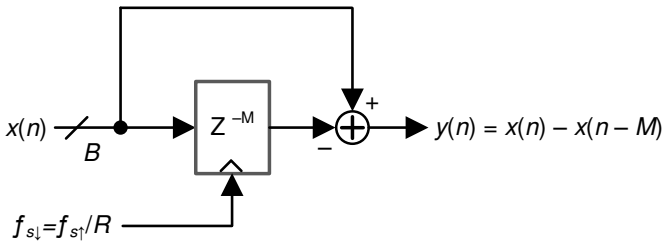


図 7. CIC Comb Filter Stage

Although M could take on many possible values, the best CIC filter performance is generally obtained by limiting M to be equal to either 1 or 2.

Taking the Z transform of both sides of the equation,

$$Y(z) = \left(1 - z^{-M}\right)X(z) \tag{5}$$

Define the function as

$$H_C(z) = \frac{Y(z)}{X(z)}$$

$$H_C(z) = \left(1 - z^{(-M)}\right) \tag{6}$$

To obtain the frequency response of a discrete-time system expressed in the Z domain, substitute $_z = re^{jw}$

Because the evaluation takes place on the unit circle, the magnitude r equals unity and therefore $_z = e^{jw}$

Making this substitution into 式 6,

$$H_C(z)|_{z=e^{j\omega}} = \left(1 - e^{-j\omega M}\right) = \left(1 - e^{-j2\pi Mf_{\downarrow}}\right) \tag{7}$$

The composite CIC filter response is composed of both the comb frequency response $H_C(z)$ and the integrator frequency response $H_I(z)$ in cascade. The composite frequency response is given by $H(z) = H_I(z)H_C(z)$ for a single stage filter. Each of these two frequency response components operate at different sample rates. However, to discuss the composite CIC filter frequency response, reference the frequency response of the comb filter sections relative to the high sample rate of the integrator. Derive this high rate reference by substituting the high rate frequency:

$$H_C(z)|_{z=e^{j\omega}} = \left(1 - e^{-j2\pi RMf_{\downarrow}}\right) \tag{8}$$

The corresponding z-transform of the comb filter referenced to the high sample rate is expressed as

$$H_C(z) = \left(1 - z^{-RM}\right) \tag{9}$$

1.6.2 CIC Filter

Because the comb sections and integrator sections are in cascade with one another, the z-transform of the composite CIC filter can then be expressed as

$$H(z) = \left[H_C(z)\right]^N \left[H_I(z)\right]^N = \left[\frac{\left(1 - z^{-RM}\right)}{\left(1 - z^{-1}\right)}\right]^N \quad (10)$$

Evaluate this equation on the unit circle in the z-plane by replacing the complex variable z with the complex exponential

$$H_C(z)|_{z=e^{j\omega}} = H\left(e^{j\omega}\right) = \left[\frac{1 - e^{-j\omega RM}}{1 - e^{-j\omega}}\right]^N \quad (11)$$

For a third-order CIC filter with differential delay of 1 (N = 3, M = 1), 式 11 can be rewritten as

$$H\left(e^{j\omega}\right) = \left[\frac{1 - e^{-j\omega R}}{1 - e^{-j\omega}}\right]^3 \quad (12)$$

In a sinc^3 filter response, the location of the first notch occurs at the frequency of output data rate f_{DATA} = f_{CLK} / R. The –3-dB point is located at f_{DATA} / 4.

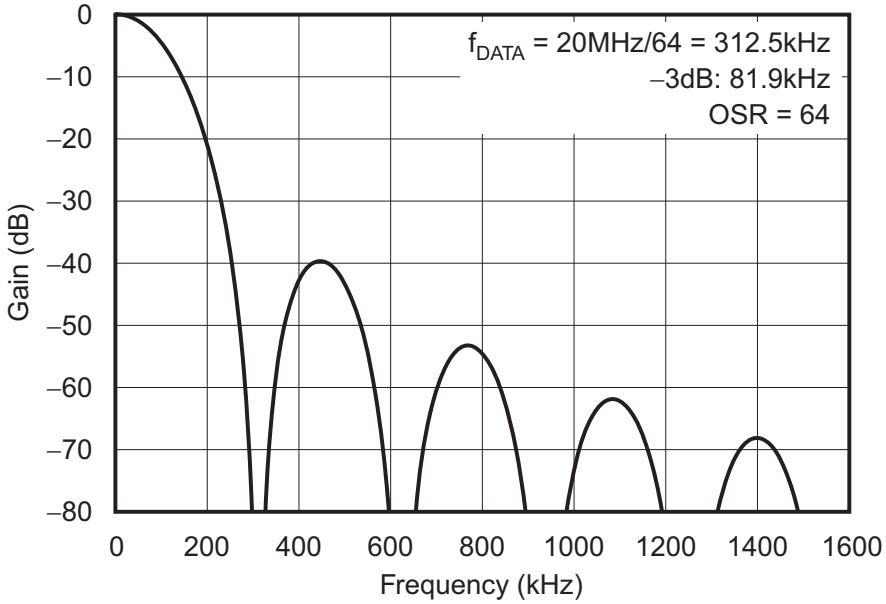


図 8. Frequency Response of the Sinc^3 Filter

図 9 shows the magnitude response of both sinc^2 and sinc^3 filter.

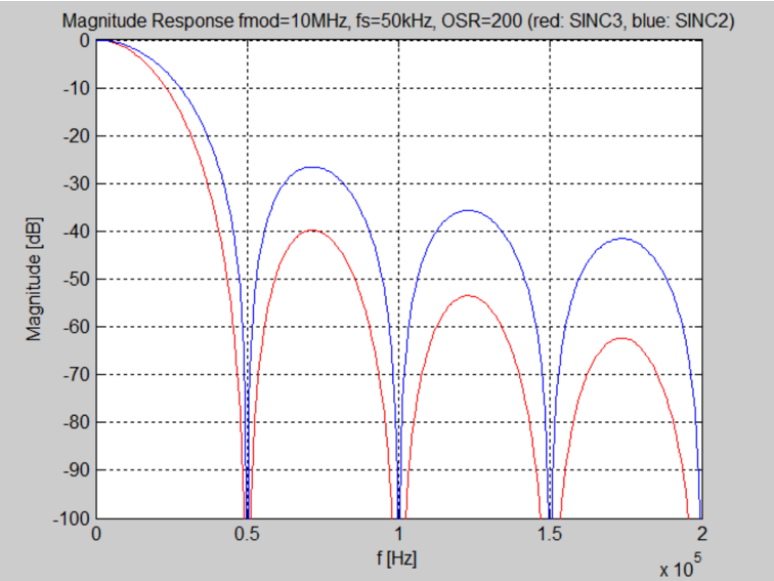


図 9. Magnitude Response of Sinc^2 and Sinc^3 Filter

1.6.3 Thumb Rules

The relationship between the modulator clock (or sampling frequency f_S), output data rate (or first notch frequency), and the decimation ratio R is given by:

- Date rate = f_S / R
- A $sinc^3$ filter –3-dB response point is 0.262 times the data rate
- For the third-order sinc filter, the step function response requires three clock periods

Using the $sinc^3$ decimation filter architecture, the output signal update rate depends on the modulator clock frequency and the decimation ratio R. Using a 20-MHz modulator in conjunction with a decimation ratio of 256 the current signal will be updated every 12.8 μs. This conversion delay is acceptable for carrier based PWM control schemes as long as this delay is significantly smaller than the PWM sub-cycle time duration TPWM / 2. For a 16-KHz PWM frequency, this configuration provides four current samples.

According to 図 10, the TI modulator AMC1304M25 provides with an oversampling rate (OSR) of 128 and a $sinc^3$ filter a result with 14-bit precision. Decreasing the OSR to 64 would reduce the precision by two bits to only 12 bits. Increasing the OSR to 256 does not significantly increase the precision but does increase the conversion settling time.

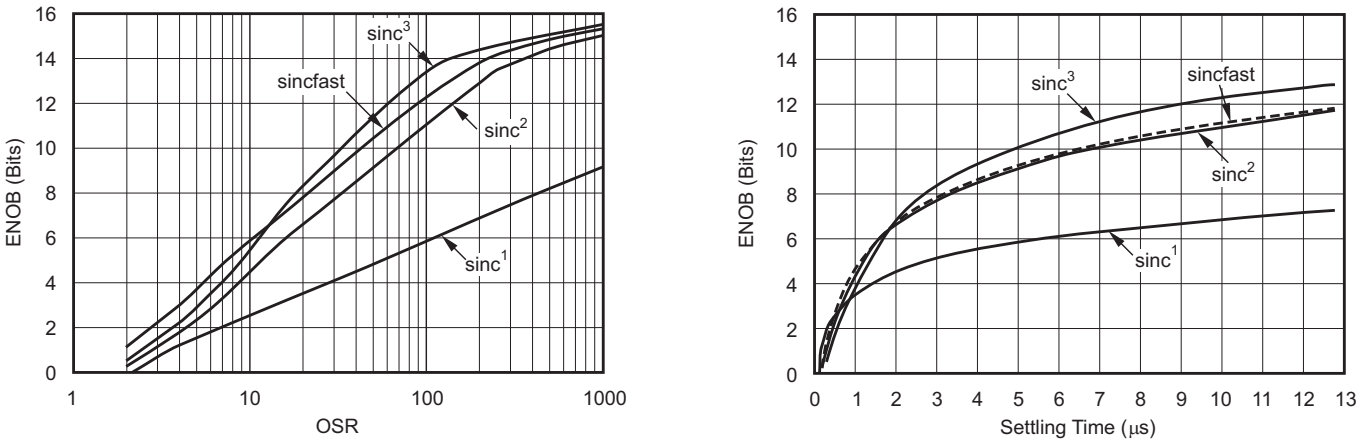


図 10. TI Modulator AMC1304M25

1.7 Isolators

A solution to use shunt and additionally achieve isolation is by using digital isolators. Isolate by:

- **Optical Coupling**: Optical coupling is the transmission of light across a transparent nonconductive barrier, such as an air gap, to achieve isolation. The main benefits of optical coupling are that light is inherently immune to external electric or magnetic fields, and optical coupling allows for transfer of steady-state information. The disadvantages of optical couplers include speed limitations, power dissipation, and the degradation of LED.
- **Inductive Coupling**: Inductive coupling uses a changing magnetic field between two coils to communicate across an isolation barrier. The most common example is the transformer where the strength of the magnetic field depends on the coil structure (number of turns per unit length) of the primary and secondary windings, the permittivity of the magnetic core, and the current magnitude.
- **Capacitive Coupling**: Capacitive coupling uses a changing electric field to transmit information across the isolation barrier. The material between the capacitor plates is a dielectric insulator and forms the isolation barrier. The plate size, which is the distance between the plates and the dielectric material, determine the electrical properties. The benefits of using a capacitive isolation barrier are efficiency, in both size and energy transfer, and immunity to magnetic fields.

1.7.1 Isolator Benefits

Industrial electronic equipment commonly uses galvanic isolators to protect systems and users from potentially hazardous voltages. Industrial equipment must operate reliably in the harshest environments where strong electromagnetic fields, surges, fast transients, and high noise floors are common. This environment presents challenges for designing reliable isolation circuits that deliver error-free operation over long equipment lifetimes. Over many decades, opto-couplers have been the default signal isolation device, but recent breakthroughs in silicon isolation technology have spawned smaller, faster, and more reliable and cost-effective solutions that have already begun supplanting opto-couplers in many end applications.

Benefits of isolators include:

- Higher integration: smaller size and lower cost-per-channel on multi-channel versions
- Higher performance: faster, tighter timing and substantially lower power
- Longer service life: no wear-out mechanisms as in opto-couplers
- Higher reliability: operating parameters remain stable over VDD, temperature, and device age
- High CMTI: fully differential isolation signal path and high receiver selectivity for CMTI greater than 15 kV/μs
- Low EMI
- High electric-field immunity: > 20 V/m, as measured by independent laboratories
- Industry-leading ESD tolerance: 3-kV HBM on all devices
- Lower external bill of materials
- Easy to use: single-chip, complete isolation solution

1.7.2 Isolation Terminologies

表 2 defines the isolation terminology.

表 2. Terminology Definitions

TERM	DEFINITION
Creepage	Distance between two points along the surface
	Measured on 1:1 artwork or on a blank board
	Locations of circuits determined by reviewing schematics
Clearance	Distance between two points through the air
	Measured on a populated sample
Functional insulation	That which is only necessary for circuit operation. Assumed to provide no safety protection
Basic insulation	Provides basic protection against electric shock with a single level; however, this category does not have a minimum thickness specification for solid insulation and is assumed to be subject to pinholes. Provides safety through a second level of protection such as supplementary insulation or protective earthing.
Supplementary insulation	Is normally used in conjunction with basic insulation to provide a second level of protection if the basic level fails. A single layer of insulating material must have a minimum thickness of 0.4 mm to be considered supplementary insulation
Double insulation	A two-level system, usually consisting of basic insulation plus supplementary insulation
Reinforced insulation	A single-insulation system equivalent to double insulation. Also requires a minimum thickness of 0.4 mm for use in a single layer
Working voltage	Voltage that may be applied continuously across the isolation barrier
	Measured as sinusoidal AC often 560 Vpk, 891 Vpk, and 1414 Vpk
	Always lower than transient voltage and surge voltage
Transient Voltage	Voltage that may occur temporarily across the barrier (failure)
	Measured as sinusoidal AC often 2.5 kV_{RMS}/4 kVpk, 6 kVpk, 5 kV_{RMS}.
	Always higher than working voltage but only occurs for a short period of time. Tested during production up to 1 min
Surge voltage	The highest instantaneous value of an isolation voltage pulse with short time duration and of specified wave shape
	Surge testing replicates lightning strikes
	The most difficult test for an isolator to withstand

This design guide focuses on a shunt-based current measurement solution, which overcomes the disadvantage of isolation and input amplification by using the AMC1304M25 Isolated ΔΣ Modulator. The AMC1304M25 is a precision ΔΣ modulator with the digital output isolated from the analog input by a capacitive isolation barrier that is highly resistant to magnetic interference. This barrier has been certified to provide reinforced isolation of up to 7000 V_{PEAK} according to UL1577 and IEC60747-5-5. Used in conjunction with isolated power supplies, this device prevents noise currents on a high common-mode voltage line from entering the local ground and interfering with or damaging sensitive circuitry.

The input of the AMC1304M25 modulator is optimized for shunt inputs or other low impedance voltage sources. The unique low-input voltage range of the device allows reduction of the power dissipation while supporting excellent AC and DC performance. When used with an appropriate digital filter, the device can be used to achieve 16-bit of resolution with a dynamic range of 76 dB at 78 kSPS.

All the relevant design files like schematics, BOM, layer plots, Altium files, Gerber, and executables for easy-to-use graphical user interfaces (GUIs) have also been provided (see 9 and 10 for more).

2 Design Specification

表 3 describes the requirements.

表 3. Design Requirements

SL NO	FEATURES	DESCRIPTION
1	Isolated ΔΣ Modulator (current inputs)	Three configured as channel isolated, with individual isolated supply
2	Isolated ΔΣ Modulator (voltage inputs)	Three configured as group isolated, sharing a common isolated supply
3	FSR (for voltages and currents)	±250 mV for current input, ±250 mV or ±1 V or 0-2 V for voltage input
4	Input frequency	50 or 60 Hz
5	OSR	256
6	Digital filter type used	$Sinc^3$
7	Current measurement accuracy	< ±0.5%, for 5 to 100% of ADC full scale
8	Voltage measurement accuracy	< ±0.5%, for 5 to 100% of ADC full scale
9	ΔΣ modulator sampling rate	32 kSPS
10	Microcontroller for signal processing	Delfino TMS320F28377D
11	Isolation level	Basic or Reinforced isolation
12	Power supply	Isolated 5 V (using isolated DC/DC converter with headroom for LDO or transformer driver) and –5 V, nonisolated 3.3 V
13	ΔΣ modulator clock frequency	8.192 MHz
	Communication interface for data transfer	USB

3 Block Diagram

Implementation of current and voltage measurement system has been implemented with three boards to have modularity.

1. The ICVM comprises of the entire signal chain for current and voltage sensing. The board has three channels for current sensing and three channels for voltage sensing. Each of the channels has provision for ESD protection diodes and a low-pass RC filter. The filtered signal is converted into a one-bit modulated stream by AMC1304M25 (±250-mV max input). This bit stream is then demodulated by a sinc filter implemented within the C2000™ processor of the Delfino control card.
2. The FMB incorporates the power supply, slot to mount the Delfino control card, digital-to-analog converter (DAC), PLL, and Sallen-Key filters.
   - A 24-V input is converted into the 5 V and 3.3 V required to operate the circuit.
   - The PLL generates the required clock for the ΔΣ modulators
   - The DAC outputs the measured current and voltage
   - A provision of Sallen-Key filters converts the one-bit data stream from ΔΣ modulators back into analog domain
3. The Delfino control card consists of a Delfino microcontroller (MCU) along with associated peripherals. The control card has USB connectivity to interface with PCs, for programming, and for debugging.

3.1 Isolated Voltage and Current Measurement Using the AMC1304M25

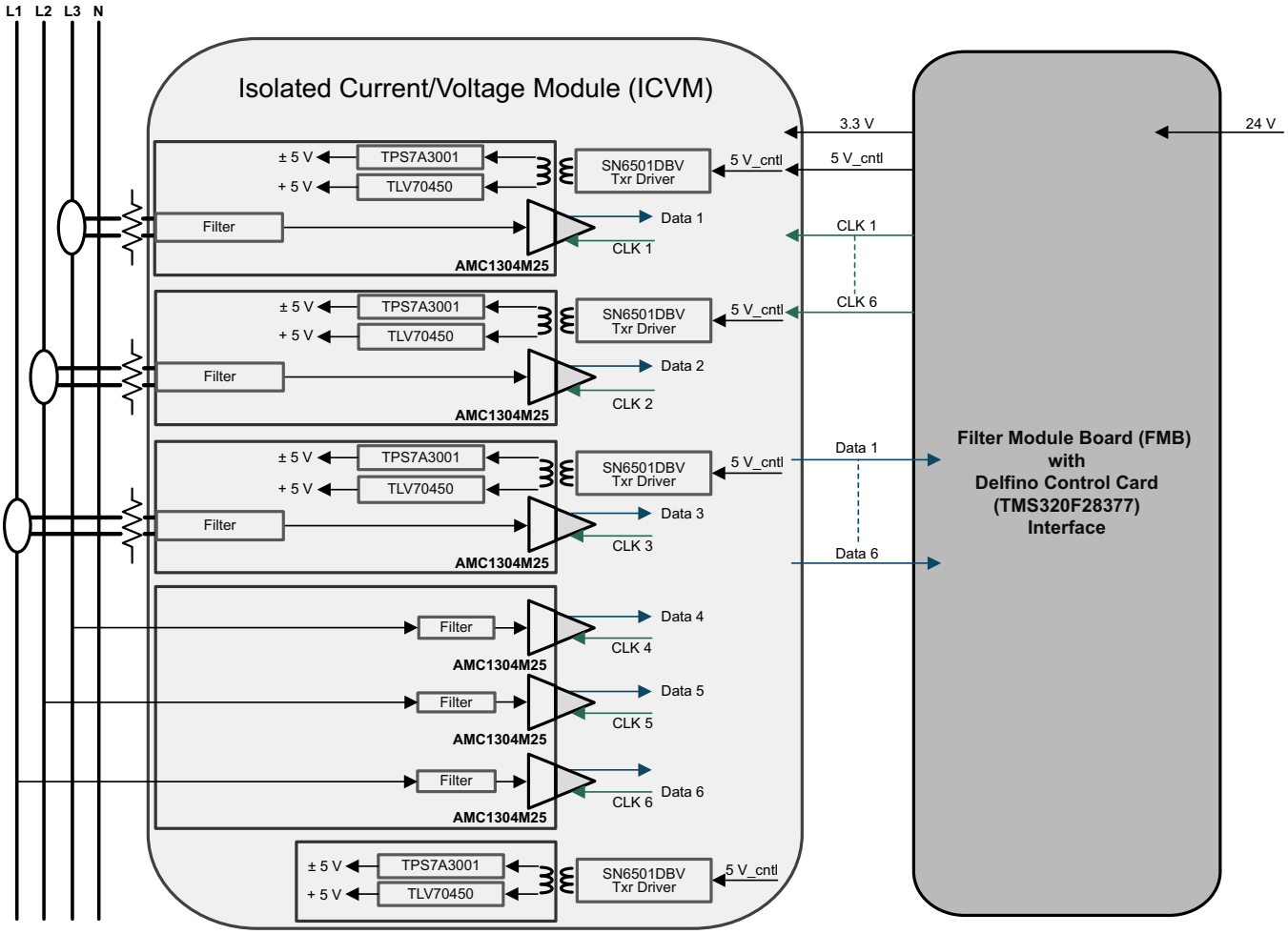


図 11. System Block Diagram

3.1.1 AMC1304M25

The AMC1304M25 converts the analog input to a digital signal and also provides isolation. The AMC1304 family is a precision ΔΣ modulator with an output separated from the input circuitry by a capacitive isolation barrier that is highly resistant to magnetic interference. The clock frequency used in the design is 8.192 MHz with a sampling rate of 32 KHz. Effectively, 16-bit data is sensed and filtered samples are transmitted to a GUI for further processing.

3.1.2 Current Inputs

Three individually isolated channels to measure currents have been provided in the design. The differential voltage across the shunt is applied to the modulator. The differential input range can be up to 175 mV_{RMS}. A two-pin screw-type terminal block has been provided to connect the analog input to the modulator.

3.1.3 Voltage Inputs

Three channels with a common isolated power supply to measure voltage inputs have been provided in the design. The output of a potential transformer (PT) or potential (resistive) divider is applied as input. The option to connect an op-amp buffer at the front of the modulator has been provided to the ΔΣ modulators. The voltage input range is 175 mV_{RMS}. A two-pin screw-type terminal block has been provided to connect the voltage inputs.

3.1.4 Cascading of AMC1304M25 for Measuring Wide Current Inputs

Currents can be measured in the following configuration:

- Three individual current inputs with individual isolated supply representing three phases with nominal current range of 10 to 200%
- Three channels cascaded (common ground) to measure wider current inputs (10 to 4000% of nominal current)

3.1.5 Power Supply and Protection

The following power supplies are generated:

- Isolated 5 V for modulator operation and overvoltage protection
- Isolated –5 V for overvoltage protection
- 3.3 V for digital operation of the modulators
- LED indication for all of the supply

3.1.6 MCU Interface Connector

A 40-pin interface connector is provided on the ICVM to interface with the FMB.

3.2 Isolated AC Voltage Measurement Using the AMC1336

This section provides details of the devices used to implement isolated AC voltage measurement.

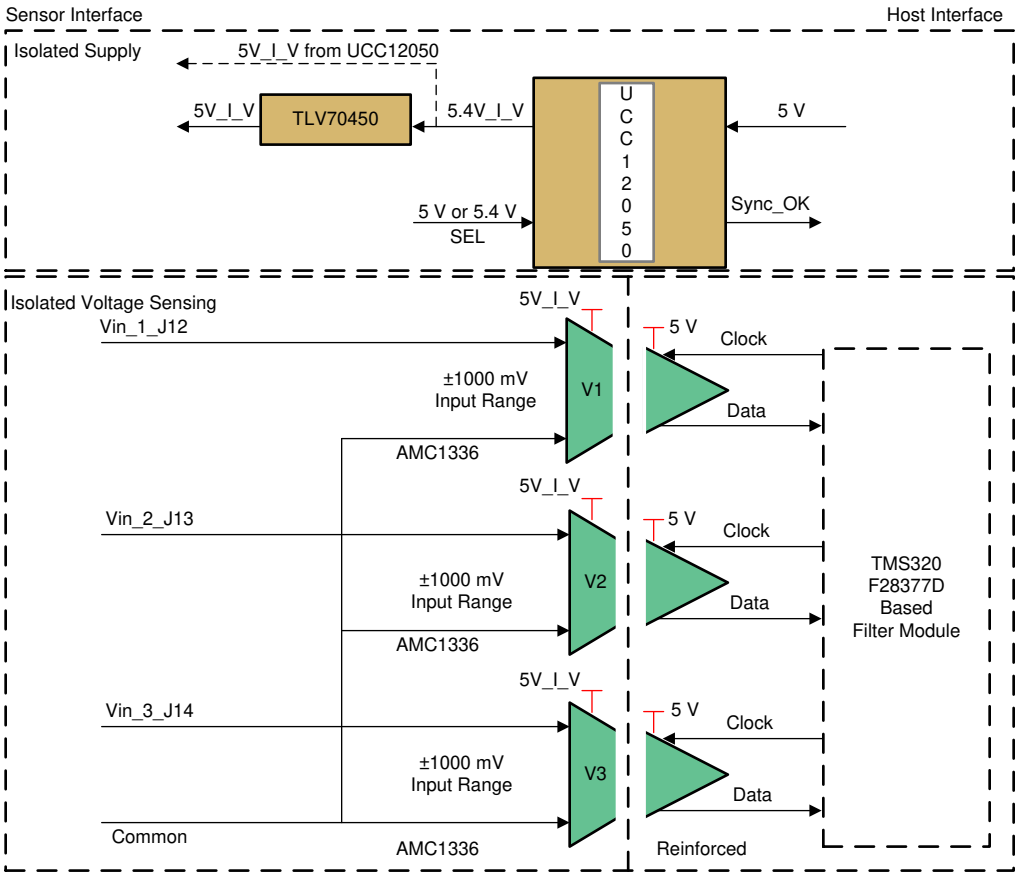


図 12. AC Voltage Measurement Subsystem

3.2.1 Delta-Sigma Modulator ACM1336

The AMC1336, a delta-sigma modulator, is used in this design to measure the input voltage. Three modulators are used for voltage measurement configured in group isolation mode. Use of an 8-pin device reduces board area and optimizes cost. The AMC1336 is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 V_{PEAK} according to the DIN V VDE V 0884-11 and UL1577 standards. Used in conjunction with isolated power supplies, this isolated modulator separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage. The unique wide, bipolar, ±1-V input voltage range of the AMC1336 and its high input resistance support direct connection of the device to resistive dividers in high-voltage applications. When used with a digital filter (for instance, as integrated in the TMS320F28004x, TMS320F2807x or TMS320F2837x microcontroller families) to decimate the output bitstream, the device can achieve 16 bits of resolution with a dynamic range of 87 dB at a data rate of 82 kSPS.

3.2.2 Isolated DC/DC Converter

The need for a common supply for multiple voltage inputs simplifies the design, and the UCC12050 has the required current rating to support multiple devices. In this design, three devices are showcased.

The required isolated power supply for voltage measurement delta-sigma modulators is generated using isolated DC/DC converter. The DC/DC converter supplies power to three modulators. The UCC12050 is a high-isolation voltage DC/DC converter designed to provide efficient isolated power to isolated circuits that require well-regulated supply voltages. The UCC12050 integrates a transformer and DC/DC controller with a proprietary architecture to achieve high efficiency with very low emissions. The UCC12050 provides 500 mW (typical) of isolated output power at high efficiency. Requiring a minimum of external components and including on-chip device protection, the UCC12050 provides extra features such as an enable pin, synchronization of switching frequency among multiple devices, and selection of isolated output voltages. The UCC12050 provides a regulated 5.0-V or 3.3-V output with selectable 400-mV headroom voltage to power an LDO. An external LDO is shown in the design to regulate the DC/DC output.

3.3 Isolated AC Current Measurement Using the AMC1306M25

This section provides details of the devices used to implement isolated AC current measurement.

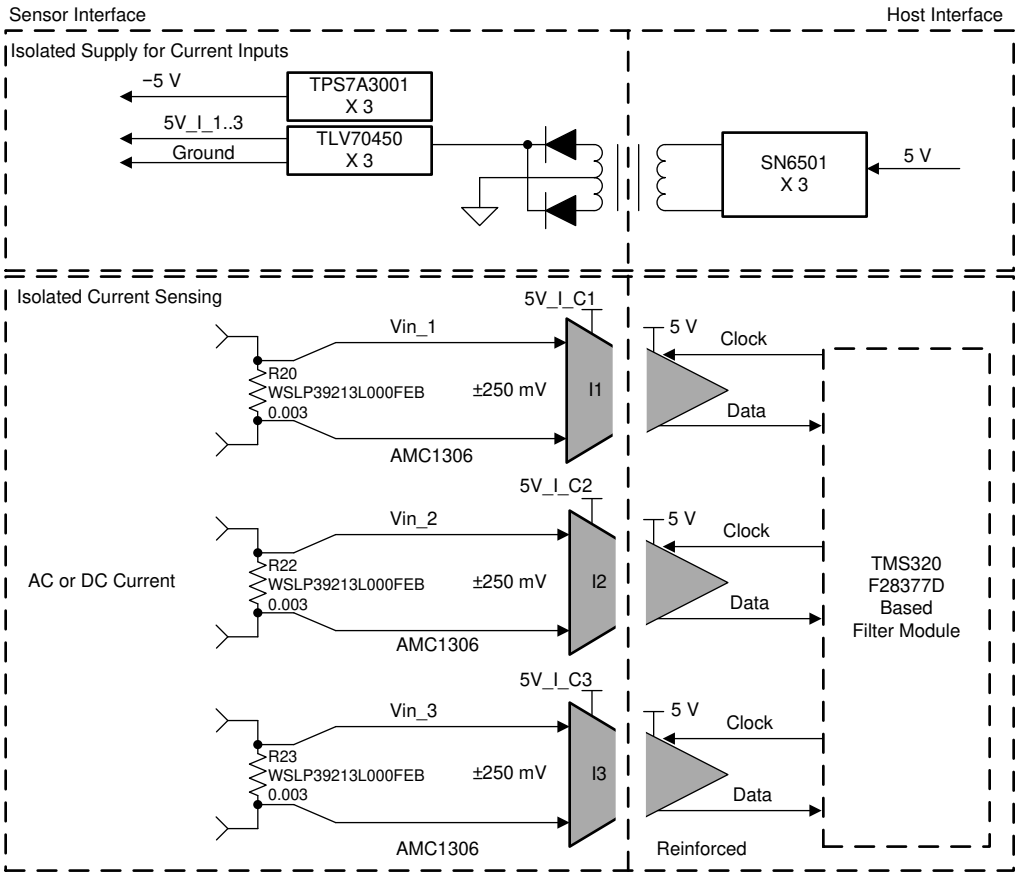


図 13. Current Measurement Subsystem

3.3.1 Delta-Sigma Modulator AMC1306M25

The AMC1306M25, a delta-sigma modulator, is used in this design to measure the input current. Three modulators are used for voltage measurement configured in group isolation mode. Use of an 8-pin device reduces board area and optimizes cost. The AMC1306 is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 V_{PEAK} according to the DIN V VDE V 0884-11 and UL1577 standards. Used in conjunction with isolated power supplies,

this isolated modulator separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage. The input of the AMC1306 is optimized for direct connection to shunt resistors or other low voltage-level signal sources. The unique low input voltage range of the ±50-mV device allows significant reduction of the power dissipation through the shunt and supports excellent AC and DC performance. The output bitstream of the AMC1306 is Manchester coded (AMC1306Ex) or uncoded (AMC1306Mx), depending on the derivate. By using an integrated digital filter (such as those in the TMS320F2807x or TMS320F2837x microcontroller families) to decimate the bitstream, the device can achieve 16 bits of resolution with a dynamic range of 85 dB at a data rate of 78 kSPS.

3.3.2 Isolated Supply

The isolated supply is similar to the AMC1304M25 based module.

3.4 Isolated DC Voltage Measurement Using the AMC1311

This section provides details of the devices used to implement isolated DC voltage measurement.

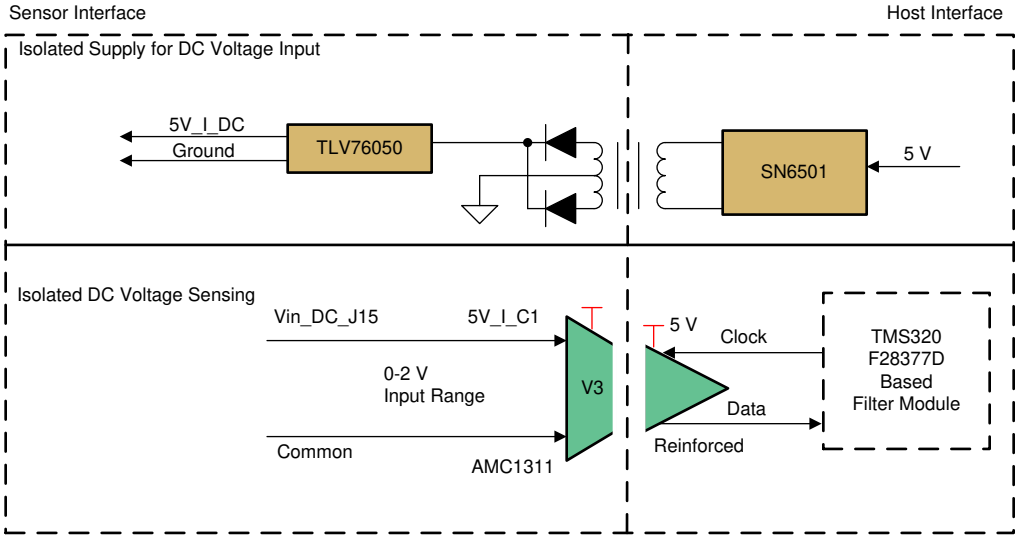


図 14. DC Voltage Measurement Subsystem

3.4.1 Delta-SIgma modulator AMC1311

The AMC1311, a delta-sigma modulator, is used in this design to measure the DC input voltage. Use of an 8-pin device reduces board area and optimizes cost. The AMC1311 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 7 kV_{PEAK} according to VDE V 0884-11 and UL1577. Used in conjunction with isolated power supplies, this isolated amplifier separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage. The high-impedance input of the AMC1311 is optimized for connection to high-voltage resistive dividers or other voltage signal sources with high output resistance. The excellent performance of the device supports accurate, low temperature drift voltage or temperature sensing and control in closed-loop systems. The integrated missing high-side supply voltage detection feature simplifies system-level design and diagnostics.

3.5 FMB

The FMB has to be connected to the ICVM for processing the modulator output and providing power, clock, and SPI signals. The FMB subsystem and the Delfino FMB are shown in 図 15.

The FMB consists of the following major blocks:

- TPS55340RTE-based flyback converter to generate 6 V from 24-V input
- LP38798SD-ADJ/NOPB to convert 6 V to 5 V
- TPS54232D to generate 3.3 V from 5 V
- SPD08-120-L-RB connector for TMS320F28377-based module
- CDCE906PW, a programmable 3-PLL clock synthesizer, multiplier, and divider to generate the clock for the ΔΣ modulator
- Interface connector to connect to the ICVM

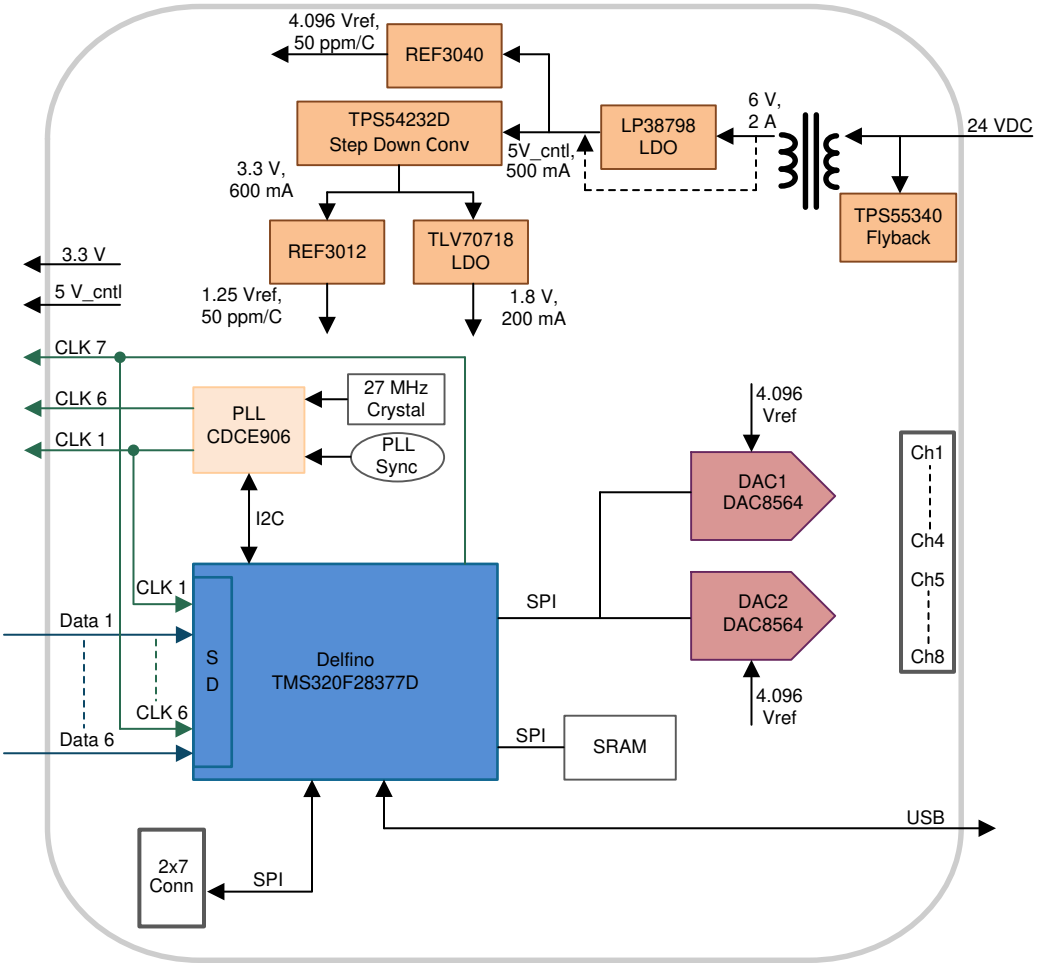


図 15. FMB Subsystem Block Diagram

This board consists of the following:

1. **Power Supply:** A 24-V DC to 6-V isolated DC-DC convertor based on flyback topology employing the TI TOS55340. The other voltage of 5 V, 3.3 V, and analog references are generated by using the TI TPS54232 (step-down convertor), TLV70718 (LDO), REF3040, REF3012, and (optional) LP38798 (LDO).
   The power consumption estimated for each of the voltage rails is:

表 4. Power Consumption Estimates

LOAD	5 V	3.3 V	1.2-V V_{REF}	4.096-V V_{REF}
AMC1304M25	100 mA	N/A	N/A	N/A
Delfino control card	200 mA	N/A	N/A	N/A
Clock CDCE906	N/A	125 mA	N/A	N/A
DACs on FMB	50 mA	N/A	N/A	25 mA (max), 75 ppm/°C
Amplifier or filters	5 mA	N/A	25 mA (max), 75 ppm/°C	N/A
Further expansion	150 mA	375 mA	N/A	N/A
Total	500 mA	600 mA	50 µA (max), 50 ppm/°C	50 µA (max), 50 ppm/°C

2. **Clocks:** The ΔΣ modulator on the ICVM board requires up to 20 MHz of clock for generating a synchronized bit stream of up to 16-bit accurate measurement. The FMB generates clock by using PLL synthesizer CDCE906. The CDCE906 can take high accuracy clock input from either a local crystal or an external clock source through the SMA connector J14. The output from CDCE906 is sourced to the Delfino controller as well as to ΔΣ modulator. Six clock outputs from the PLL are used by the six modulators meant for current and voltage measurement.
3. **DACs:** The measured input voltage and currents can be displayed simultaneously by two DAC8564s, which are 16-bit quad-channel voltage output DACs.
4. **Amplifiers and Sallen-Key Filter:** These filters are provided as an option to convert back the digital stream from modulators to analog, which can be processed by the SAR ADC for any applications.

5. **Connectors:** The FMB is provided with connector interfaces to the ICVM board, control card, clock input, JTAG, and DAC outputs. The connector's functionality is highlighted in 表 5.

表 5. Connectors on the FMB

CONNECTOR AS ON FMB	FUNCTION	CONNECTOR TYPE
J1	FMB to ICVM	2×20 pins, right angle, male, board to board
J2, J15	SPI	2×5 pins, male
J3	USB (not used currently)	USB micro type AB
J4	FMB to control card	60-pin, high-speed card edge
J5	FMB to control card	120-pin, high-speed card edge
J8, J9, J10	Controller GPIO	2×5 pins, male
J13	24-V DC input	2 pins
J14	External clock input	SMA female jack

3.6 Delfino Control Card

The Delfino F28377D control card (TMDXCNCD28377D) from TI is used for digital filtering. This 180-pin control card provides a well-filtered robust design capable of working in most industrial environments.

The F28377D control card features:

- **Delfino F28377D MCU**: High performance C2000 MCU located on the control card
- **180-pin HSEC8 Edge Card Interface**: Allows compatibility with all of C2000's 180-pin control card application kits and control card. Compatibility with 100-pin control cards can be accomplished using the TMDSADAP180TO100 adapter card (sold separately)
- **Built-In Isolated JTAG Emulation**: An XDS100v2 emulator that provides a convenient interface to Code Composer Studio™ without additional hardware. Flipping a switch allows an external JTAG emulator to be used
- **Connectivity**: Allows the user to experiment with USB, microSD card, and isolated UART/SCI with the F2837x MCU
- **Key Signal Breakout**: Most GPIO, ADC, and other key signals routed to hard gold connector fingers
- **Robust Power Supply Filtering**: Single 5-V input supply powers an on-card 3.3-V LDO. All MCU inputs are then decoupled using LC filters near the device
- **Anti-Aliasing Filters:** Noise filters (small RC filters) can be easily added on several ADC input pins

The Delfino control card is shown in 図 16.

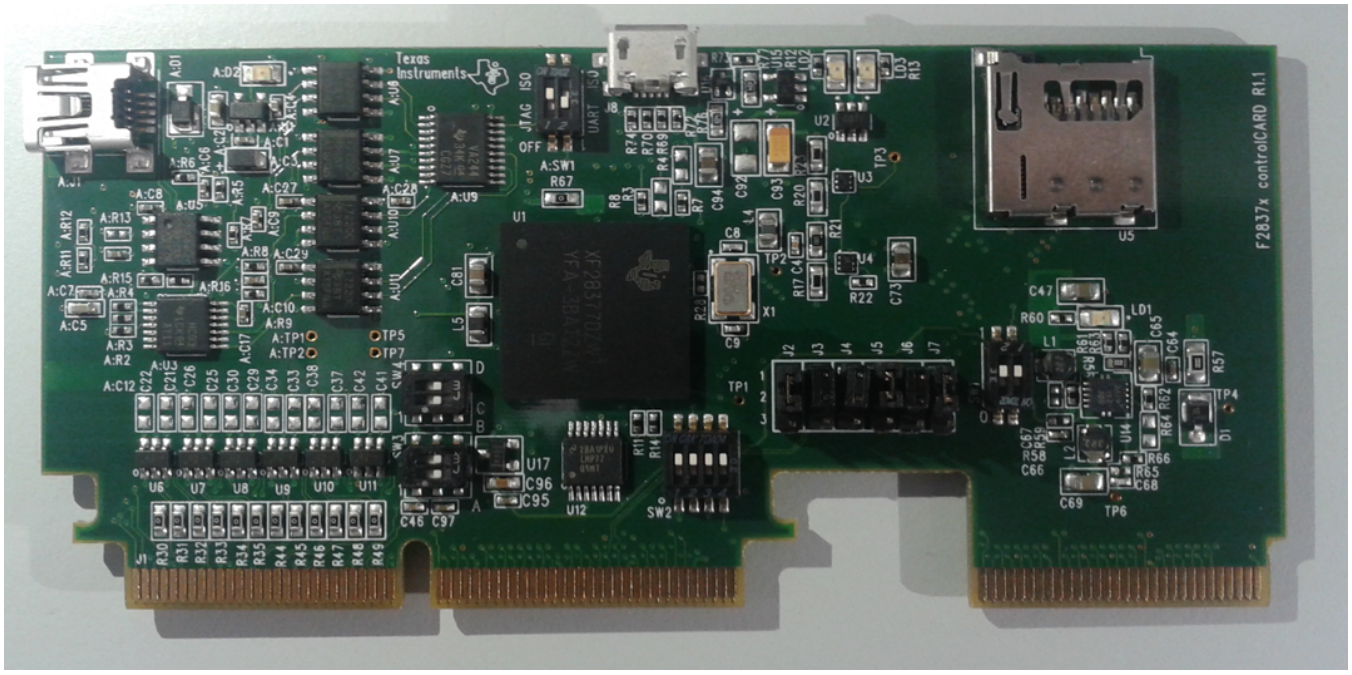


図 16. Delfino Control Card

4 Circuit Design

4.1 ICVM

4.1.1 AMC1304M25

The AMC1304M25 is a precision ΔΣ modulator with an output isolated from the input circuitry by a capacitive isolation barrier that is highly resistant to magnetic interference. This barrier has been certified to provide reinforced isolation of up to 7000 V_{PEAK} according to UL1577 and IEC60747-5-5. Used in conjunction with isolated power supplies, this device prevents noise currents on a high common-mode voltage line from entering the local ground and interfering with or damaging sensitive circuitry.

The input of the AMC1304M25 is optimized for direct connection to shunt resistors or other low voltage level signal sources. The unique low input voltage range of the device allows significant reduction of the power dissipation through the shunt while supporting excellent AC and DC performance.

A simplified schematic is shown in 図 17.

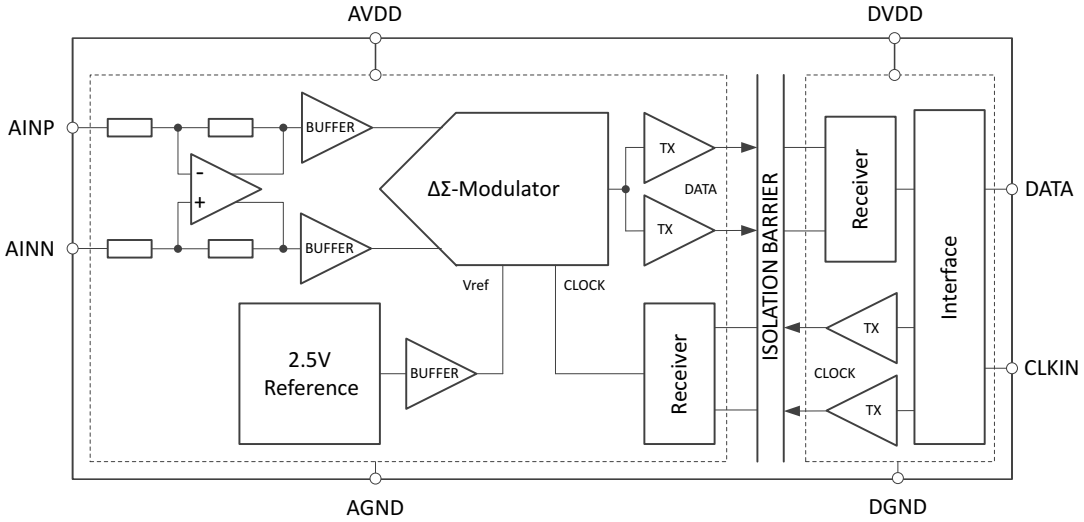


図 17. AMC1304 Pin Outs

The AMC1304M25 modulator incorporates a front-end circuitry that contains a differential amplifier and sampling stage, followed by the ΔΣ modulator.

There are two restrictions on the analog input signals VINP and VINN:

1. If the input voltage exceeds the range AGND –6 V to AVDD 0.3 V, the input current must be limited to 10 mA, because the input protection diodes on the front end of the converter begin to turn on.
2. In addition, the linearity and the noise performance of the device are ensured only when the differential analog input voltage remains within ±250 mV for AMC1304M25.

The input impedance becomes a consideration in designs with high input impedance signal source . This high impedance may degrade the gain (which trimable on the system level), linearity, and THD.

The AMC1304M25 Isolated ΔΣ Modulator is used for converting the analog current input to a digital signal and also for providing isolation.

The input of the AMC1304M25 modulator is optimized for direct connection to shunt resistors or other low voltage level signal sources. The unique low input voltage range of the device allows significant reduction of the power dissipation through the shunt while supporting excellent AC and DC performance. When used with an appropriate external digital filter, the device can be used to achieve 16-bit of resolution with a dynamic range of 76 dB (AMC1304x05) at 78 kSPS.

4.1.1.1 Features

The AMC1304M25 modulator includes the following features:

- ±250-mV input voltage range optimized for shunt resistor-based current measurement
- Excellent DC precision
- Offset error and drift: ±50 μV, 1 μV/°C
- Gain error and drift: ±1% max, 20 ppm/°C
- Certified isolation barrier: UL1577 and IEC60747-5-5 approved
- Isolation voltage: 7000 V_{PEAK}
- Working voltage: 1.5-kV DC, 1.5-$kV_{AC, RMS}$
- Surge voltage: 10 kV_{PEAK}
- Transient immunity: 15 kV/μs min
- Long isolation barrier lifetime
- High electromagnetic field immunity
- External 5- to 20-MHz clock input for synchronization
- LDO regulator with up to 18-V input voltage range
- CMOS interface
- Specified over the extended industrial temperature range

The AMC1306 is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 V_{PEAK} according to the DIN V VDE V 0884-11 and UL1577 standards. This device is in a pin-compatible family optimized for shunt-resistor-based current measurements with an input range of ±250-mV and provides uncoded bitstream output. The AMC1336 is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 V_{PEAK} according to the DIN V VDE V 0884-11 and UL1577 standards. The AMC1336 input structure is optimized for voltage measurements with an input voltage range of ±1 V.

4.1.2 Current Inputs

All the current channels are individually isolated. An AC input up to 175 mV_{RMS} can be applied. Shunt has not been provided as part of the design. To measure the input current, an external shunt has to be used. The shunt value depends on the current range expected to be measured. The voltage across the shunt (current input) must be 175 mV_{RMS}. The following connectors in 表 6 are designated as current inputs.

表 6. Current Input Connections

CURRENT INPUT	CONNECTOR
Channel 1	J11
Channel 2	J10
Channel 3	J9

注: Do not apply AC current inputs directly to the above connector inputs. This may damage the board.

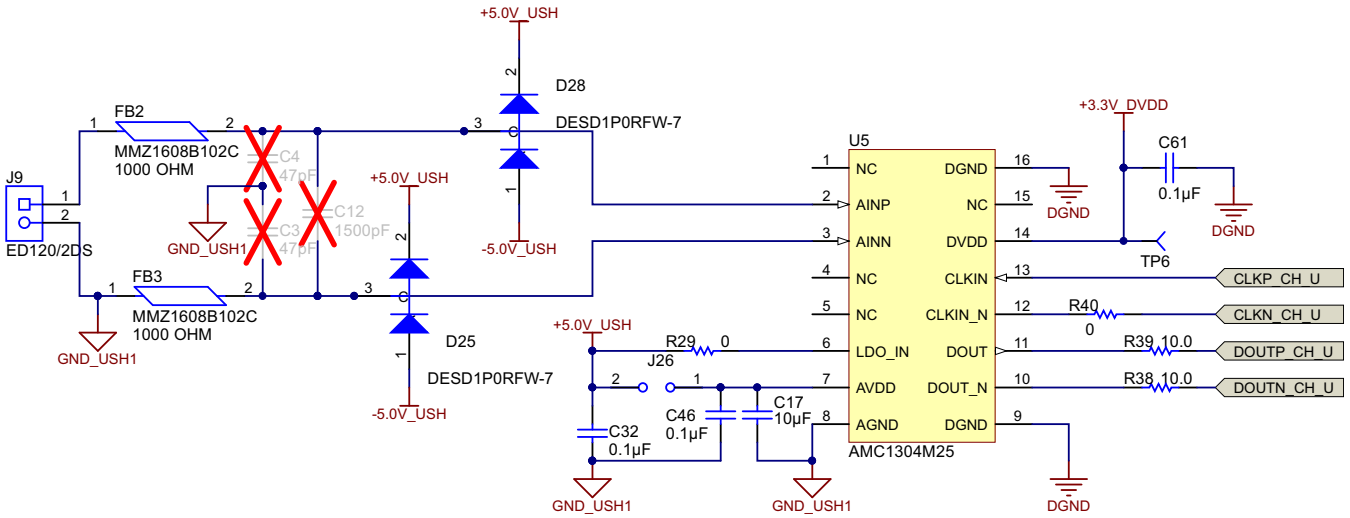


図 18. Circuit Diagram of Current Input

The RF/EMI filter is used for common mode and differential mode noise rejection for improved performance. The filtered mV signal is fed to the AMC1304M25 Isolated ΔΣ Modulator.

4.1.3 Voltage Inputs

The AC voltage input has to be attenuated outside the board, as no resistors (potential divider) has been provided on the board. The attenuated input range can be up to 175 mV_{RMS}.

The following connectors in 表 7 are designated as voltage inputs.

表 7. Voltage Input Connections

VOLTAGE INPUT	CONNECTOR
Channel 1	J14
Channel 2	J13
Channel 3	J12

注: Do not apply AC in puts directly to the above connector.

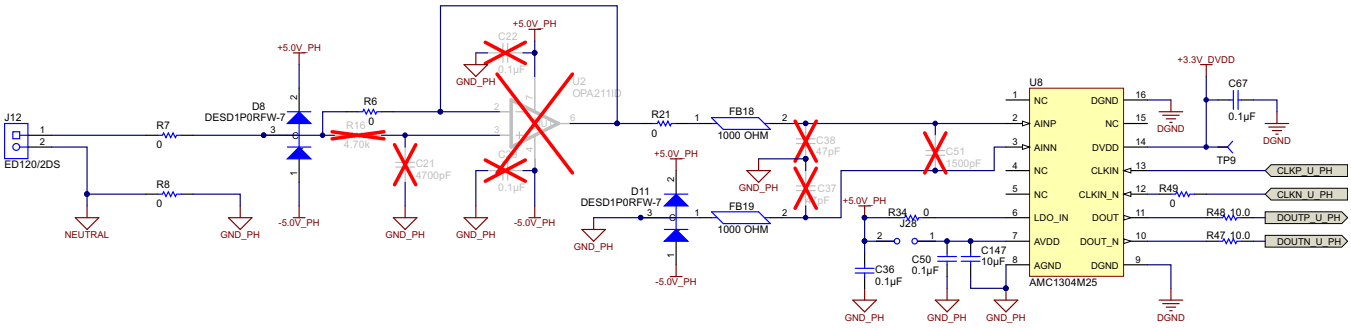


図 19. Circuit Design of Voltage Input

The RF/EMI filter is used for common-mode and differential-mode noise rejection, leading to improved performance filtering.

The AMC1304M25 input is optimized for shunt resistor-based current measurement. Op-amp based buffer circuits can be used to further improve accuracy in case errors are observed during voltage measurement. Op-amps provide low impedance input for the AMC1304M25.

4.1.4 Cascading of AMC1304M25 Current Inputs for Extending Input Current Range Measurement

4.1.4.1 Applying Three-Phase Inputs

The AMC input section is isolated from the power supply section. For current inputs to function as independent three-phase inputs, following jumpers have to be shorted with each other.

表 8. Current Ground Connections

CHANNEL	GROUND JUMPER SHORTING
Channel 1	J5 and J6
Channel 2	J3 and J4
Channel 3	J1 and J2

4.1.4.2 Applying Single Phase Input for Wide Range of Current Input

To achieve a wide range of current measurement, a provision to cascade all three current channels is given. A three-shunt cascaded connection with the board is shown in 図 20.

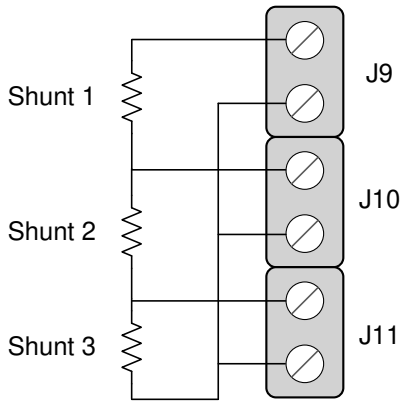


図 20. Connection Diagram for Cascaded Shunts

For extended range, grounds of three current channels must be shorted. The shunts connection will look like three shunts connected in series, and tapping from each shunt is measured by the AMC1304M25 with one common ground.

表 9. Current Cascaded Connections

CHANNEL	GROUND JUMPER SHORTING	ADDITIONAL JUMPER SHORTING
Channel 1	J5 and J6	Short J1, J3, J5
Channel 2	J3 and J4	
Channel 3	J1 and J2	

4.1.5 Isolated Power Supply

図 21 shows the design of the isolated power supply.

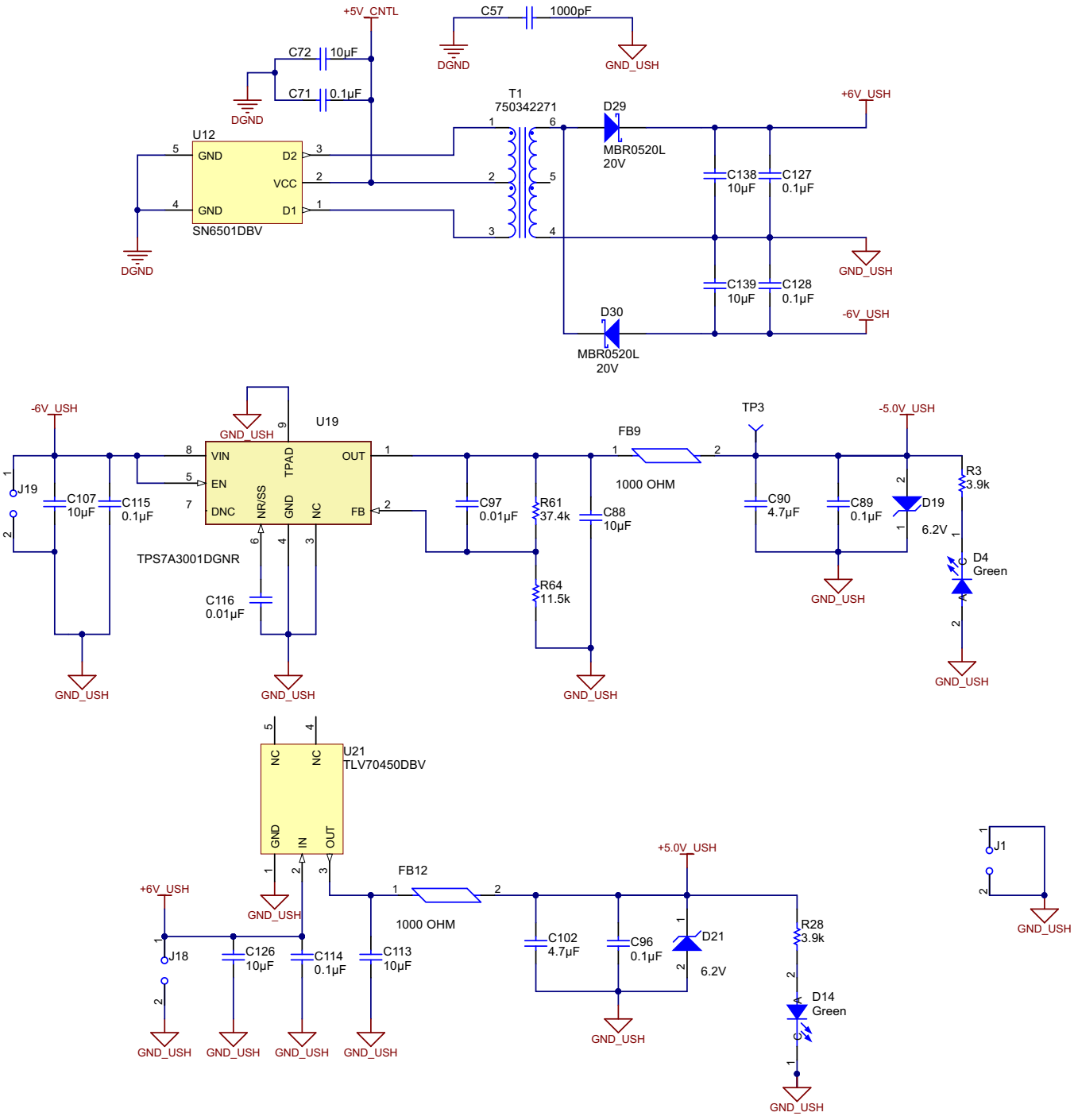


図 21. Isolated Power Supply and Protection

Some design features of the isolated power supply are:

- An SN6501, a monolithic oscillator and power-driver specifically designed for small-form factor, isolated power supplies in isolated interface applications. The SN6501 drives a low-profile, center-tapped transformer primary from a 5-V DC power supply. The design uses a transformer with a 1.64:1 turns ratio to generate ±6 V
- Isolated 5 V for modulator operation on the isolated side (TLV70450DBV, an ultra-low IQ, high Vin LDO) is used to convert the 6 V to 5 V required for the AMC1304M25 modulator operation
- Isolated –5 V for protection on the isolated side (TPS7A3001DGNR, a negative, high voltage, ultra low-noise linear regulator) is used to convert the 6 V to –5 V required for the AMC1304M25 modulator operation
- 3.3 V provided by the FMB for digital operation of the AMC1304M25 modulator

Protection is provided at each input channel with over voltage at 5-V DC and –5-V DC. The design has three current and three voltage channels. Three current channels are isolated from each other. Three voltage channels share a single isolated power supply.

注: The transformer used is custom designed. Please check with The Würth Group for samples as required.

Alternatively, the UCC12050 can be used, eliminating the need for multiple transformers based on the output requirement. The UCC12050 is a high isolation voltage DC/DC converter designed to provide efficient isolated power to isolated circuits that require well-regulated supply voltages. The UCC12050 integrates a transformer and DC/DC controller with a proprietary architecture to achieve high efficiency with very low emissions. The UCC12050 provides 500 mW (typical) of isolated output power at high efficiency. Requiring a minimum of external components and including on-chip device protection, the UCC12050 provides extra features such as an enable pin, synchronization of switching frequency among multiple devices, and selection of isolated output voltages.

4.1.6 MCU Interface Connector

The 40-pin interface connector consists of:

- A differential or single-ended clock for ΔΣ modulators
- A differential DOUT signal from ΔΣ modulators
- 3.3 V for operation of the digital side functioning of ΔΣ modulators
- 5 V to generate isolated 5 V and –5 V for Isolated ΔΣ modulator functioning and protection

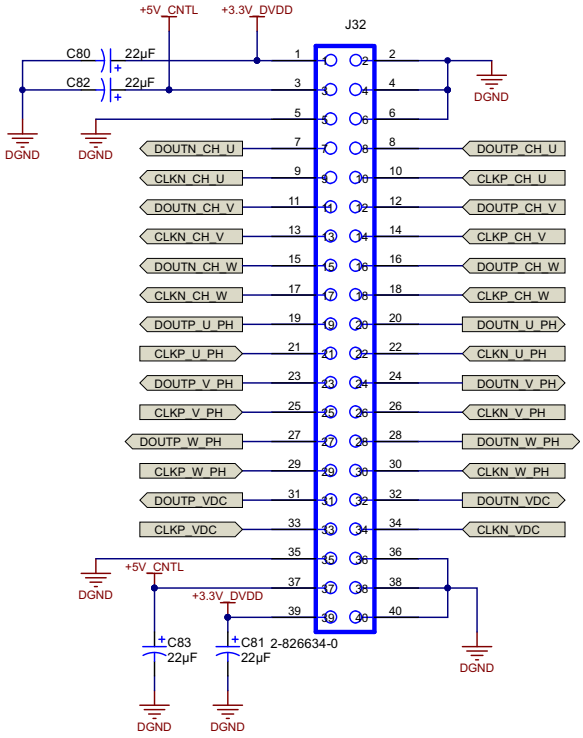


図 22. MCU Isolated Power Supply

4.2 FMB

The FMB includes the Delfino control card along with the power supply circuit.

4.2.1 DC Input: Reverse Polarity Protection

The DC input is protected against any accidental wrong wiring. The diode D23 provides this polarity protection with a peak current capability of 4 A. Due to the input capacitors of close to 125 µF, the inrush current can be high initially for milliseconds, limited only by the 24-V DC buses and source impedance.

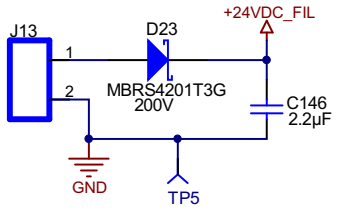


図 23. Input Polarity Protection

4.2.2 Flyback Converter 24-V to 6-V DC

The 24-V DC can vary up to ±20%. The DC-DC convertor chosen is TPS55340 with a maximum continuous input voltage of 32 V. The switching frequency is externally set at a nominal 350 kHz. The 40-V, 5-A, low-side MOSFET is incorporated inside the TPS55340 package along with the gate-drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS55340 to achieve high efficiencies. The compensation components are external to the integrated circuit.

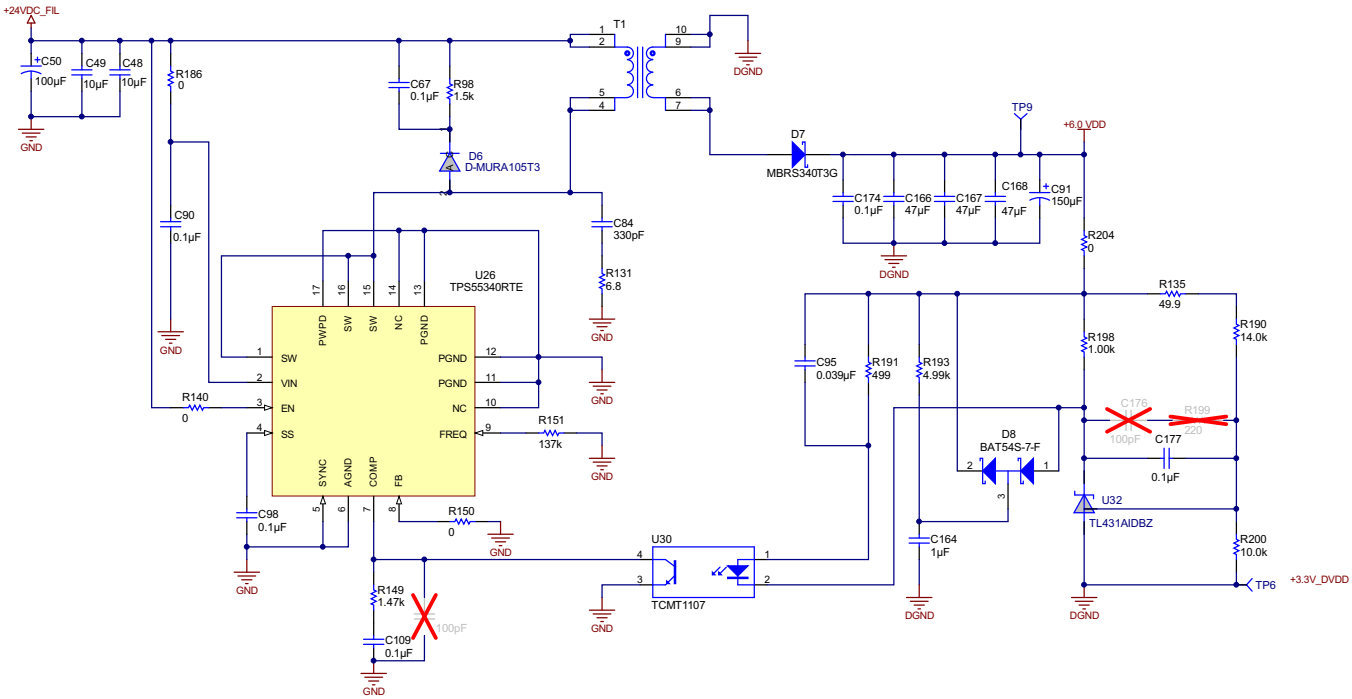


図 24. Flyback Convertor 24-V to 6-V DC

Output Voltage Selection

The output voltage required is 6 V. So, using TL431 and the V_{ref} as 2.495 V, the values of R190 and R200 are selected as 14 kΩ and 10 kΩ, respectively.

$$R190 = R200 \times \left(\frac{V_{out}}{V_{ref}} \right) - 1 \quad (13)$$

where

- V_{out} = 6 V
- V_{ref} = 2.495 V

Set the Switching Frequency

The resistance R151 has to be calculated for the desired switching frequency:

$$R_{FREQ}(k\Omega) = 57500 \times f_{sw}(kHz) - 1.03 \quad (14)$$

where

- f_{sw} = 350 KHz

So, R151 = 137 kΩ

Efficiency

The efficiency of this design peaks at a load current of about 1.5 A at 24-V input, then decreases as the load current increases toward full load. 図 25 shows the efficiency in general and 図 26 shows the light-load efficiency by using a semi-log scale.

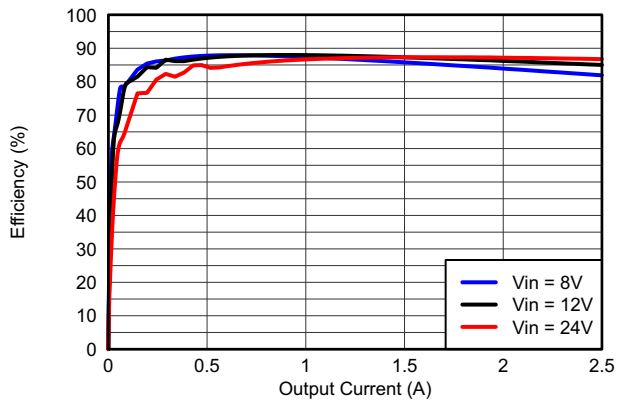


図 25. Efficiency

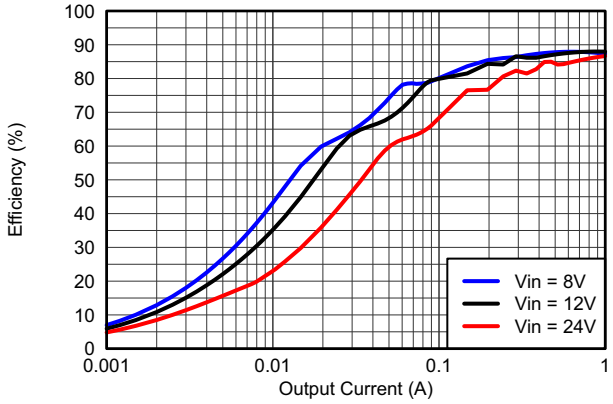


図 26. Light Load Efficiency

4.2.3 Switching Regulator 6 V to 3.3 V

The 3.3 V is generated by the step-down convertor based on TPS54232 (see 図 27). This 3.3 V is required for PLL synthesizer CDCE906.

The switching frequency is internally set at 1000 kHz. The high-side MOSFET is incorporated inside the TPS54232 package along with the gate drive circuitry. The low drain-to-source on resistance of the MOSFET allows the TPS54232 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54232 provides adjustable slow start and undervoltage lockout inputs.

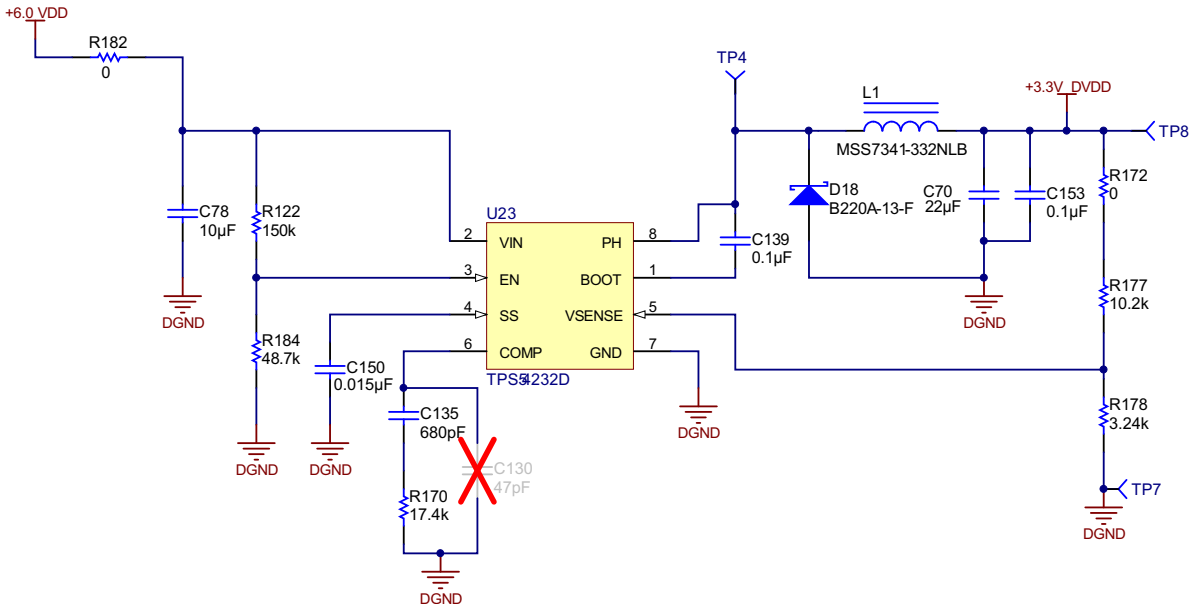


図 27. 6-V to 3.3-V Step Down Converter

4.2.4 Reference Voltages

The reference voltages are provided as a stable and noiseless voltage references for the analog circuits.

4.2.4.1 1.2-V V_{ref}

The 1.2-V V_{ref} is to provide a stable reference to the op-amp based filter circuits. The REF3012 is a precision low-power, low-voltage dropout voltage reference in a SOT23-3 package. Other key specifications include:

- High accuracy: 0.2%
- Low drift: 75 ppm/°C from –75°C to 125°C
- High output current: 25 mA

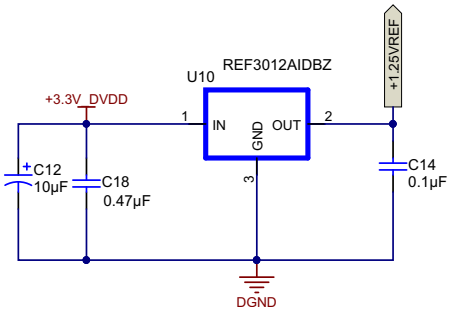


図 28. 1.2-V V_{ref}

4.2.4.2 4.096 V

The 4.096 V provides a stable external voltage reference to the DAC8564. This reference is provided as an option if the user needs a DAC output of maximum 4 V. The DAC8564 has an interval V_{ref} of 2.5 V; therefore, with an internal V_{ref} activated, the maximum DAC output shall be 2.5 V.

The REF3040 is a precision low-power, low-voltage dropout voltage reference in a SOT23-3 package.

Other key specifications include:

- High accuracy: 0.2%
- Low drift: 75 ppm/°C from –75°C to 125°C
- High output current: 25 mA

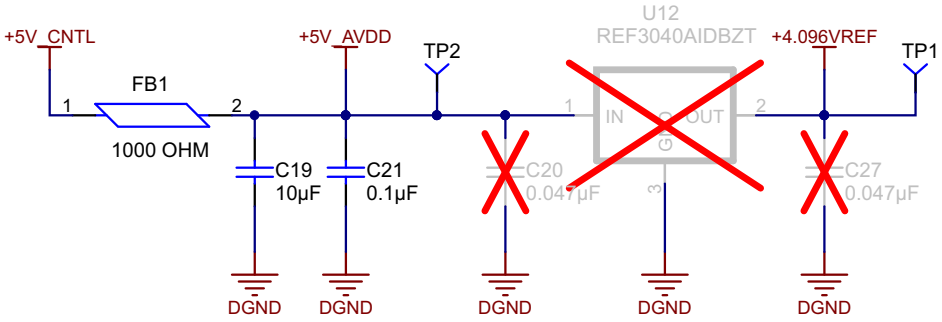


図 29. 4.096 V

4.2.5 PLL Synthesizer CDCE906-Based Programmable Clock

The CDCE906 is one of the smallest and powerful PLL synthesizer, multiplier, and divider available today. Despite its small physical outlines, the CDCE906 is the most flexible. The device has the capability to produce an almost independent output frequency from a given input frequency.

The input frequency can be derived from an LVCMOS, a differential input clock, or a single crystal. The appropriate input waveform can be selected through the SM bus data interface controller.

To achieve an independent output frequency, the reference divider M and the feedback divider N for each PLL can be set to values from 1 up to 511 for the M-Divider and from 1 up to 4095 for the N-Divider. The PLL-VCO (voltage controlled oscillator) frequency is then routed to the free programmable output switching matrix to any of the six outputs. The switching matrix includes an additional 7-bit post-divider (1 to 127) and an inverting logic for each output.

The deep M/N divider ratio allows the generation of 0 ppm clocks from, for example, a 27-MHz reference input frequency.

The CDCE906 includes three PLLs; of those, one supports spread-spectrum clocking (SSC). PLL1, PLL2, and PLL3 are designed for frequencies up to 300 MHz and optimized for zero-ppm applications with wide divider factors.

The PLL2 also supports center- and down-SSC. This PPL is a proven method to effectively reduce the energy for the selected frequency range. The electromagnetic interference (EMI) is significantly reduced, and the slew-rate controllable (SRC) output edges minimize EMI noise. Based on the PLL frequency and the divider settings, the internal loop filter components will automatically adjust to achieve a high stability and optimized jitter transfer characteristic of the PLL.

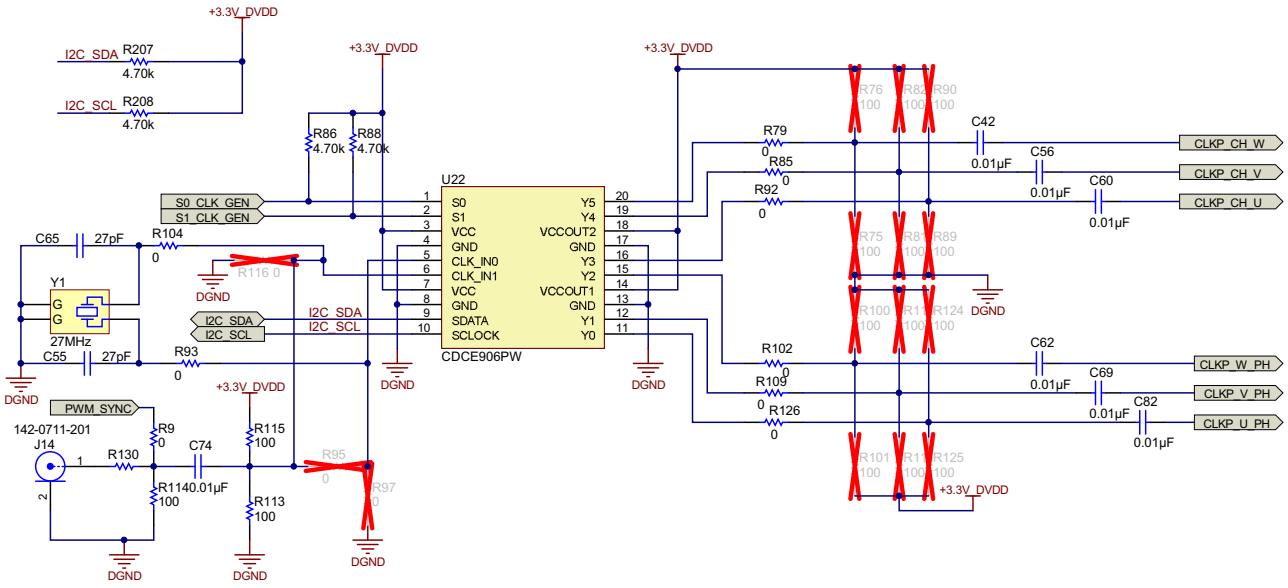


図 30. PLL Generation

In this reference design, the PLL is used to generate the reference clock for the AMC1304M25. The higher the clock rate, the higher is the OSR, the better the accuracy. The AMC can operate at a maximum of 20.1 MHz.

4.2.6 DAC8564

The two DAC8564s replicate the analog input signal for the AMC1304M25 modulator.

The DAC8564 is a 16-bit high-resolution, quad-channel, and serial input DAC with a built-in 2.5-V internal reference that is enabled by default. This DAC has a serial interface to communicate with the host microprocessor. 図 31 illustrates the 16-bit DAC output.

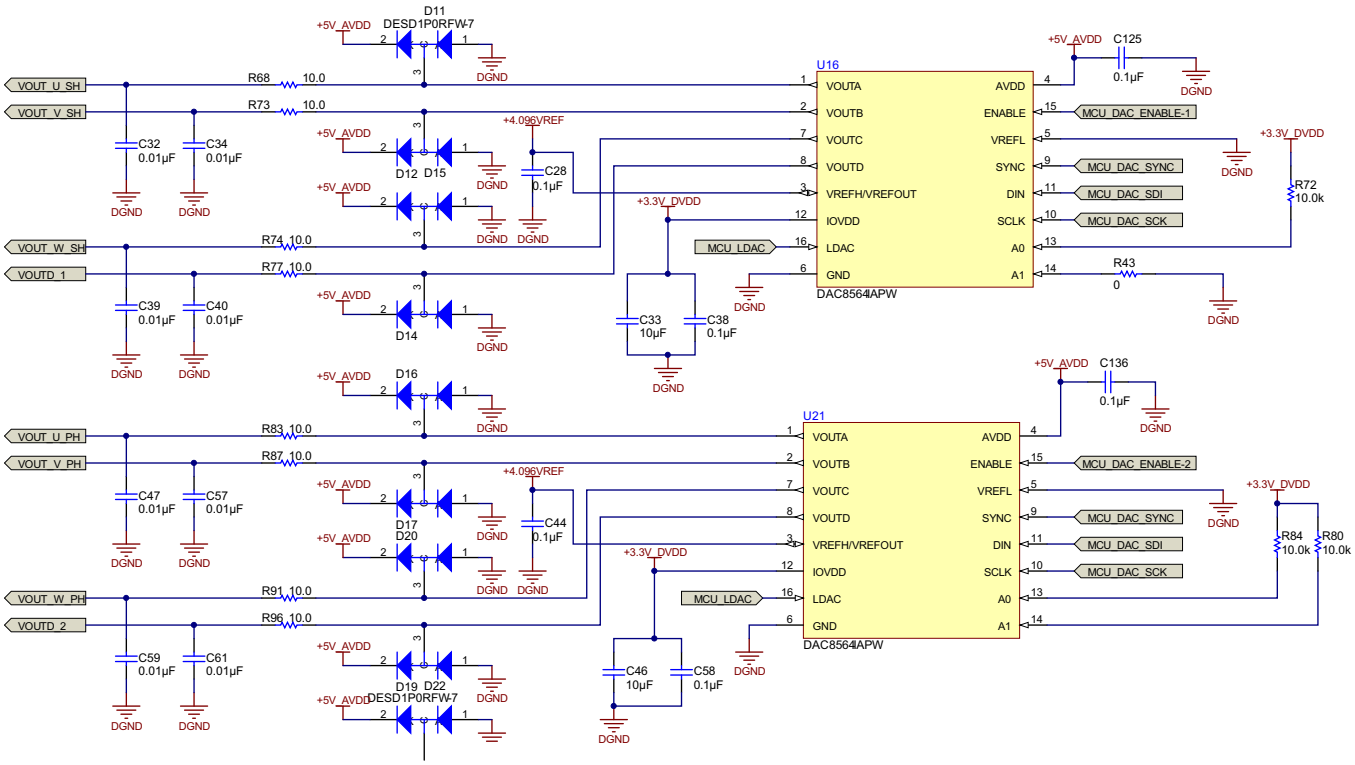


図 31. 16-Bit DAC Output

注: This DAC output is proportionate to the inputs across the modulator. This output can be used for debugging. This design has not done DAC measurement.

4.2.7 Connectors

The FMB is provided with connectors to interface the 24-V DC input, Delfino control card, and ICVM. There are more connectors to provide diagnostics functionality.

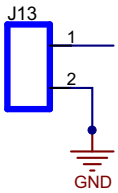


図 32. 24-V DC Input

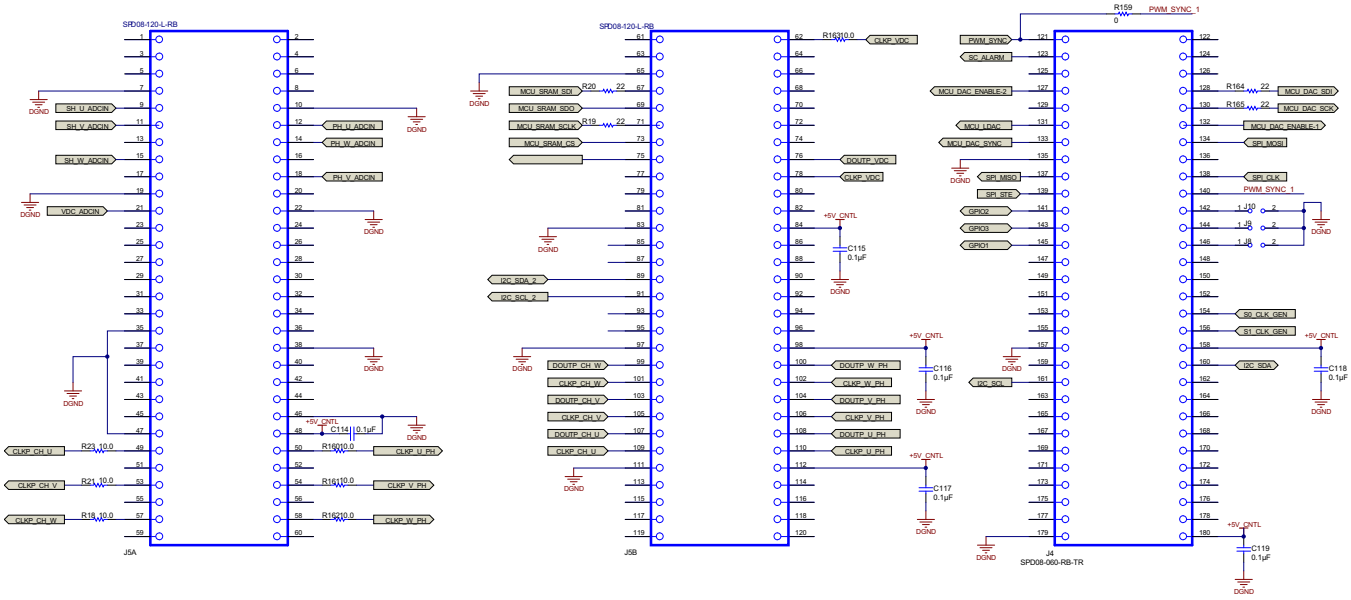


図 33. Connector to Delfino-Based Control Card

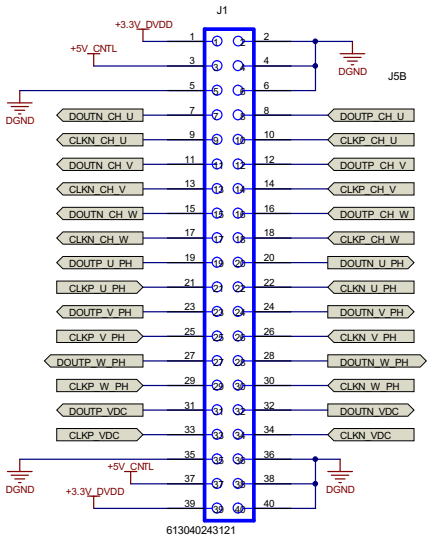


図 34. 20×20 Pin Connector to ICVM Board

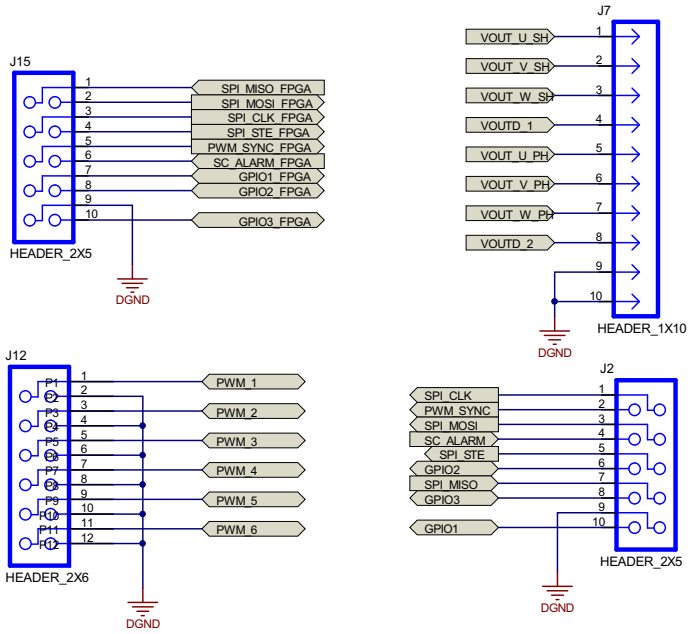


図 35. Miscellaneous Connectors: DAC, JTAG

4.3 Delfino Control Card

The MCU on the Delfino-based control card board is TMS320F28377D, a dual-core Delfino of the C2000 family of MCUs. 図 36 gives an overview of the device and integrated peripherals.

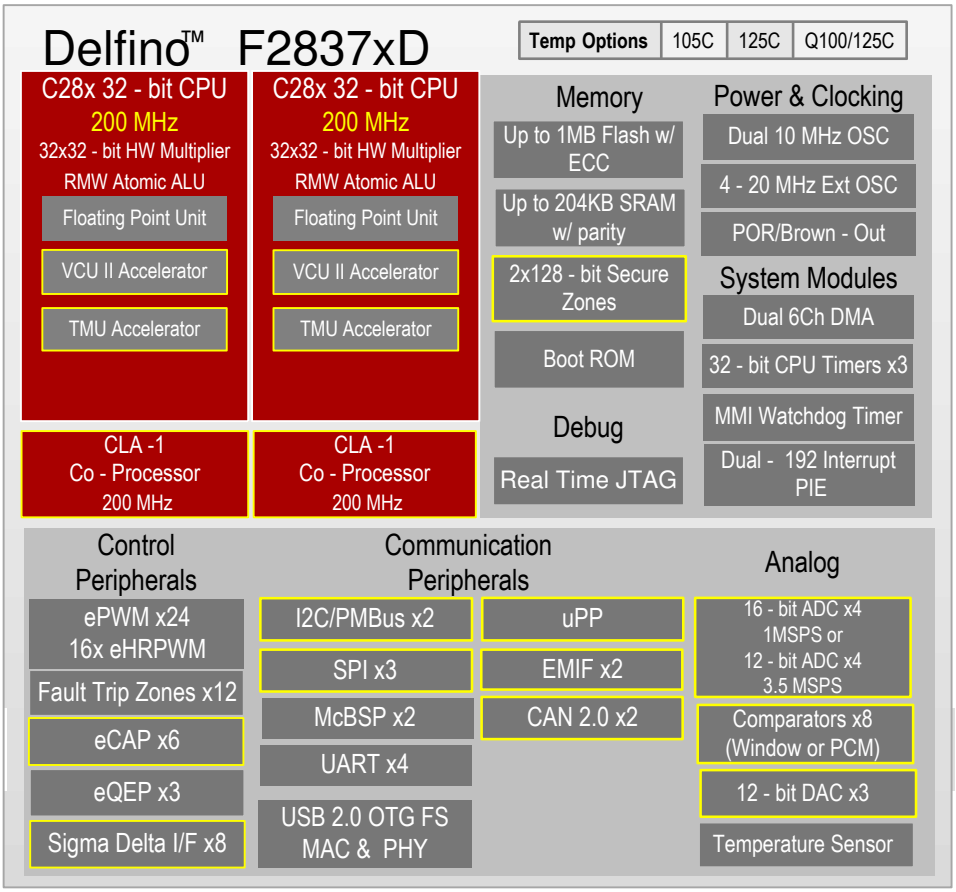


図 36. TMS320F28377D Overview

表 10 lists the peripherals used on the controller and the master allocated to the peripheral.

表 10. List of Peripherals

MCU RESOURCE	MASTER CPU	USED FOR
Sigma-delta filter modules (SDFM1 and SDFM2)	CPU1	Interface with AMC1304M25
USB	CPU1	Interface with PC GUI
ePWM8	CPU1	Generates clock for the AMC1304M25, interfaced on the third channel of the SDFM2
ePWM1, ePWM2, ePWM3, ePWM4, ePWM5, ePWM7	CPU1	Optional clock source for other AMC1304M25 interfaced on SDFM1 and ADFM2(1)
SPI-B	CPU2	Interface with DAC8564
SPI-C	CPU2	Interface to external controller
I^2C-A	CPU1	Interface with CDCE906 PLL synthesizer

(1) Indicates resource allocated on the hardware, not used for GUI firmware.

4.3.1 SDFM Peripheral

The controller has two integrated Sigma-Delta filter modules (SDFM1, SDFM2). Each SDFM supports four channels of ΔΣ demodulation. The eight channels available on the controller are used for sampling three current inputs and three voltage inputs.

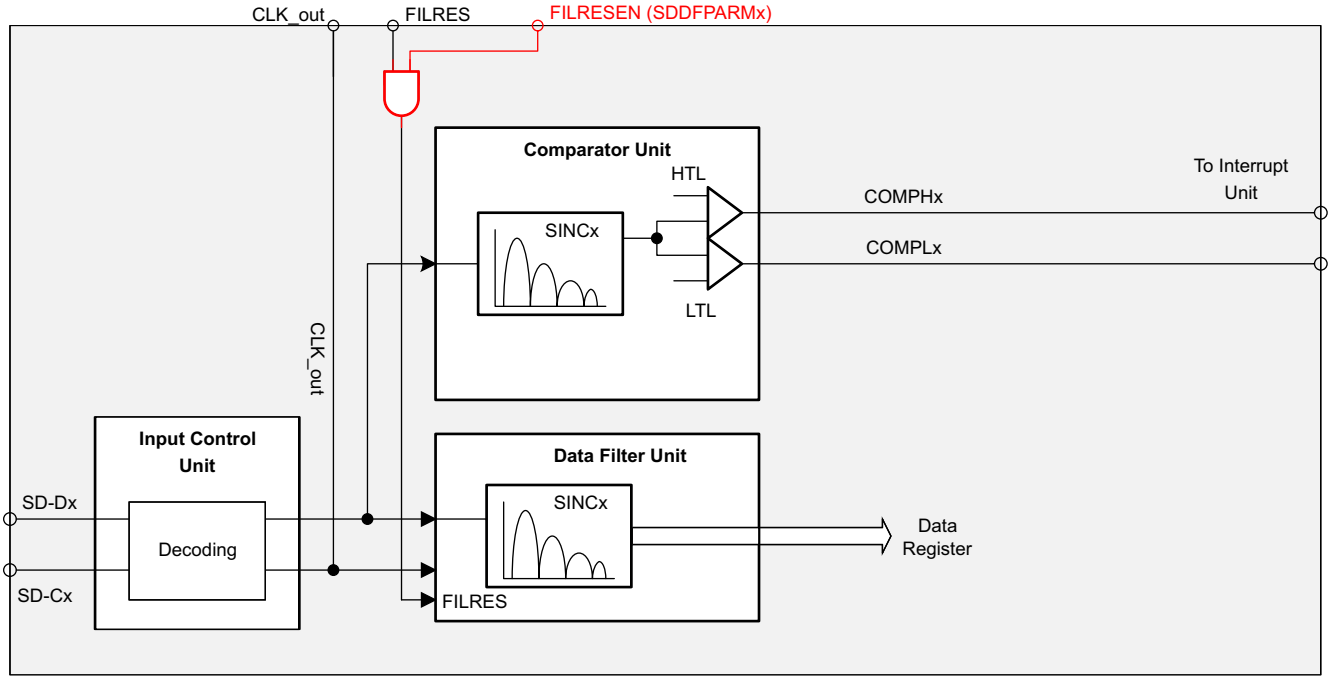


図 37. Block Diagram of Single Filter Module

図 37 shows a filter module for one channel available in the SDFM. Each SDFM peripheral has four filter modules. The main sub-modules within the SDFM are the data-filter unit, input-control unit, and the comparator unit. See the TMS320F28377D TRM to learn more about the different blocks in the peripheral device.

The input-control block supports different types of bit stream. The input-control block supports bit streams, which may operate at the same rate as the clock input, twice the clock input, half the clock input, or Manchester-encoded bit streams. AMC1304M25 gives a data rate equal to the clock input. The required configuration for input-control bocks in modulator mode is Mode 0.

The data-filter unit implements sinc filters in hardware, which converts the bit stream. The conversion result is obtained in the result registers. The data filter unit supports $sinc^1$, $sinc^2$, $sinc^3$, and sincfast filter structures with OSR of 1 to 256. GUI provides features to set modulator and sinc structures as required.

Sampling rate of the filter is given as 式 15.

$$f_{DATA}\,(\text{Sinc filter output rate}) = \frac{\text{Modular data rate}}{\text{SOSR}} \tag{15}$$

注: SOSR: Oversampling rate of the sinc filter.

The output register of the sinc filter unit is 32 bits wide, and a 16-bit mode is provided and used. In the 16-bit mode, the output, which is 32 bits, is right-shifted to a 16-bit representation in the complement of two. The shift control SH filed in SDFIPARM is used to control the right-shift operation during the conversion. The position of the MSB in 32-bit mode depends on the filter structure and the OSR. When obtaining the 16-bit data, set SH to a value to obtain the MSB of the data in the MSB of the register.

Data-bit width depends on the sinc structure and the OSR. 図 38 shows the result range. $Sinc^3$ filter types with a maximum OSR of 256 provide a resolution of 24 bits. $Sinc^3$ and 256 OSR provided the best resolution.

表 11. Peak Data Values for Different DOSR and Filter Combinations

DOSR	$SINC^1$	$SINC^2$	$SINC^3$	SINCFAST
x	x	x^2	x^3	$2x^2$
4	–4 to 4	–16 to 16	–64 to 64	–32 to 32
8	–8 to 8	–64 to 64	–512 to 512	–128 to 128
16	–16 to 16	–256 to 256	–4096 to 4096	–512 to 512
32	–32 to 32	–1024 to 1024	–32,768 to 32,768	–2048 to 2048
64	–64 to 64	–4096 to 4096	–262,144 to 262,144	–8192 to 8192
128	–128 to 128	–16,384 to 16.384	–2,097,152 to 2,097,152	–32,768 to 32,768
256	–256 to 256	–65,536 to 35,536	–16,177,216 to 16,177,216	–131,072 to 131,072

The frequency response of the filter structure is given in 図 38. Notice that $sinc^3$ provides higher attenuation and higher noise rejection. Therefore, a $sinc^3$ filter is best suited for accuracy.

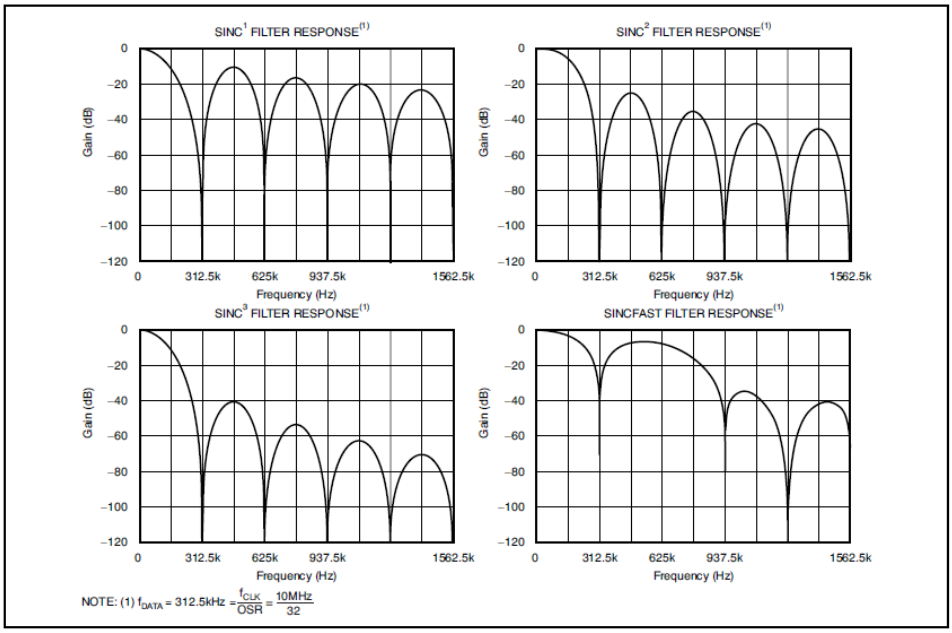


図 38. Frequency Response of Various Sinc Filters

The comparator unit implements a second sinc filter. The conversion result digitally compared to threshold values in the threshold registers (SDFCMPHx and SDFCMPLx registers). In each filter module, the comparator unit is used for overvoltage and short-circuit detection.

4.4 Scale Factor

The GUI obtains raw counts from the Delfino controller. The GUI calculates the applied voltage or current by multiplying the raw counts by a scale factor. First, calculate the intended scale factor. This calculation is called the theoretical scale factor. Once the theoretical scale factor is known, calibration should be performed. Use the following calculations to calibrate:

Scale Factor for Voltage and Current Measurement

The part used for this design is ±250 mV, and the total full-scale deflection for the part from the datasheet is 312.5 to –312.5 mV. This deflection corresponds to a range of 32767 to –32768 for a 16-bit result register. The resolution is

$$\frac{312.5\,\text{mV} - (-312.5)\,\text{mV}}{32767 - (-32768)} = 0.0095367\,\text{mV/count} \tag{16}$$

4.5 Calibration

The scale factor from 4.4 is theoretical and produces errors in performance testing from expected reading. The reasons for this are:

- The offset error of AMC1304M25
- The gain error of AMC1304M25
- The tolerance of the sense resistors

In case of 2-wire shunts, the soldering resistance adds to the shunt value and deviates the reading. For the current channel, this resistance necessitates gain compensation.

In AC voltage measuring, the error seen depends on the tolerance of the components used for voltage divider. Uncalibrated error percentage error is approximately equal to tolerance of the parts. Also, the calculation depends on the AMC1304M25 input impedance, which can vary from device to device.

4.5.1 Calibration Procedure

表 12 has steps to perform a two-point calibration. First, obtain the two readings. The readings may correspond to the maximum and minimum of the range from two readings if they are formatted in following:

表 12. Two-Point Calibration Formatting

METER READING	READING FROM PC GUI
Xa	Ya
Xb	Yb

The gain calibration can be done by modifying the scale factor calculated previously as new scale factor = (Xa – Xb) / (Ya – Yb) × Old scale factor.

For offset calibration we calculate the required offset in raw counts as = (YbXa – YaXb) / Old scale factor.

Once the new scale factor value and the offset value is found, this can be updated as explained in 6.5.

5 Software Description

5.1 Software Activities

表 13 lists and describes the software functions.

表 13. Software Specification

SI NO	FUNCTION	DESCRIPTION
1	UI installation	Install the UI in the following order: 1. LV Runtime - http://www.ni.com/download/labview-run-time-engine-2010-sp1/2292/en/ 2. VISA Runtime - http://www.ni.com/download/ni-visa-run-time-engine-5.1.2/2918/en/ 3. UI .exe file can be installed now
2	GUI interface for measurement	Interfaced to Delfino with USB2.0 interface, Bulk, RAW mode
3	Delfino initialization	Mode-0 Data rate = clock rate (Matches the AMC1304M25 ΔΣ Modulator type)
4	Sampling of analog inputs (voltage and current) and oversampling	Enable conversion on the Delfino end
		Set Delfino data register read to 16 Bit format
		Set OSR to 256, $sinc^3$
5	Filtering of the analog input	Default is $sinc^3$ filter
		($Sinc^1$ and $sinc^2$ are configurable through GUI)
		OSR is configurable in GUI
6	Scaling the sampled values (conversion of samples to mV with GUI)	$\text{Scaling Factor} = \frac{(\text{VADCmax} - \text{VADCmin})}{2^{16} \times 0.8} = \frac{[250 - (-250)]}{2^{16} \times 0.8} = 0.009536743$ (17)
		GUI multiplies samples with above scaling factor to obtain the input signal value.
7	Waveform Capture duration and parameters calculation using GUI	Waveform capture time programmable up to 120 ms
		RMS, DC, Pk-PK, Min-MAX
		Frequency computation
8	Calibration using GUI	Offset and Gain calibration
9	Capturing of instantaneous samples and storing using GUI	4096 samples per channel
		Store one channel at a time into a CSV format file
		Can capture snap shot of the screen.
10	Post processing	LPF, HPF, BPF, BSF
		Bessel, Butterworth, or Chebyshev filter
11	Display on GUI	Plot of the waveform from captured samples

5.2 Firmware Description

The required firmware for the Delfino DSP Core 1 and Core 2 must be loaded before the card can be used to test the ICVM.

The firmware was developed using the device support package for F2837xD contained in controlSUITE™. This firmware provides the device register definitions, peripheral driver libraries, and USB libraries. The libraries can be found in the installation directory of controlSUITE. The purpose of the firmware is to configure the sinc filters, set the PLL frequency, receive data from sinc filters, and interface to the PC GUI to help the user validate the AMC1304M25 performance. The firmware supports configuration changes to sinc filter parameters in the Delfino controller. The firmware is composed of:

- GUI
- DAC8564 interface
- SDFM1 and SDFM2 interfacing to AMC1304M25
- Interfacing to CDCE906 for clock generation
- ePWM to generate clock
- Fault detection

The SDFM1 and SDFM2 peripherals in the Delfino controller are interfaced with AMC1304M25. Firmware supports updating the filter type and OSR value fault detection thresholds. The SDFM1 and SDFM2 channels are renamed on the GUI to have a common naming convention.

The GUI is implemented using the internal USB in F28377D. The device is configured for device mode as a raw bulk device. The raw bulk device was chosen as it provided a convenient interface to the LabVIEW™ GUI. The raw bulk descriptor and configuration is same as the controlSUITE example by the name "usb_dev_bulk". A custom application protocol was implemented for interaction between the USB device and GUI. Implementation of this protocol can be seen in files "GUI.h" and "GUI.c" for its internal working.

For Delfino interface to the clock synthesizer CDCE906 on the I^2C bus, refer to the *Programmable 3-PLL Clock Synthesizer/Multiplier/Divider* (SCAS814) datasheet for the devices' configuration registers and definition. After power-on, the firmware sets up CDCE906 to minimum clock output of 1 MHz. The clock output can be changed from the GUI. When the user updates the switching frequency in the GUI, the GUI calculates the new clock frequency and the GUI internally calculates the required configuration values to be written into the CDCE906. Delfino receives the clock configuration from the GUI and updates the register settings in CDCE906 through the I^2C interface. The clocks required for the modulators are generated by clock synthesizer CDCE906.

The two DAC8564s are used for debugging purpose. The Delfino updates the output of the DAC to represent the conversion result by the SDFM peripheral. The user can then view the waveform on an oscilloscope. The DAC8564 is interfaced on SPI-B and the CPU2 is made master of SPI-B. Refer to the *16-Bit, Quad Channel, Ultra-Low Glitch, Voltage Output DIGITAL-TO-ANALOG CONVERTER with 2.5V, 2ppm/°C Internal Reference* (SBAS403) datasheet for the SPI frame format. To update one channel of the DAC, write a 24-bit word: the first 8 bits contain the DAC addressing, channel addressing, and the load command, and the next 16 bits are the DAC value in 16-bit straight binary. The firmware uses immediate load for all channels, and the DAC address and channel address are chosen appropriately. The LDAC feature is not used. Firmware sets up the DAC8564 to use an internal 2.5-V reference. CPU1 passes the

SDFM results to CPU2 by writing the results to a shared RAM; the address location is hard coded and maintained in both CPU1 and CPU2. The output from the SDFM is configured to 16-bit signed output; that is, range is from –32768 to 32767. This converted to 16-bit straight binary by adding 32767 to SDFM output; that is, 1.25 V from DAC represents 0, 2.5 V represents 32767, and 0 V represents –32768 from the SDFM peripheral.

図 39 shows the firmware flow graph and arrangement of tasks between CPU1 and CPU2.

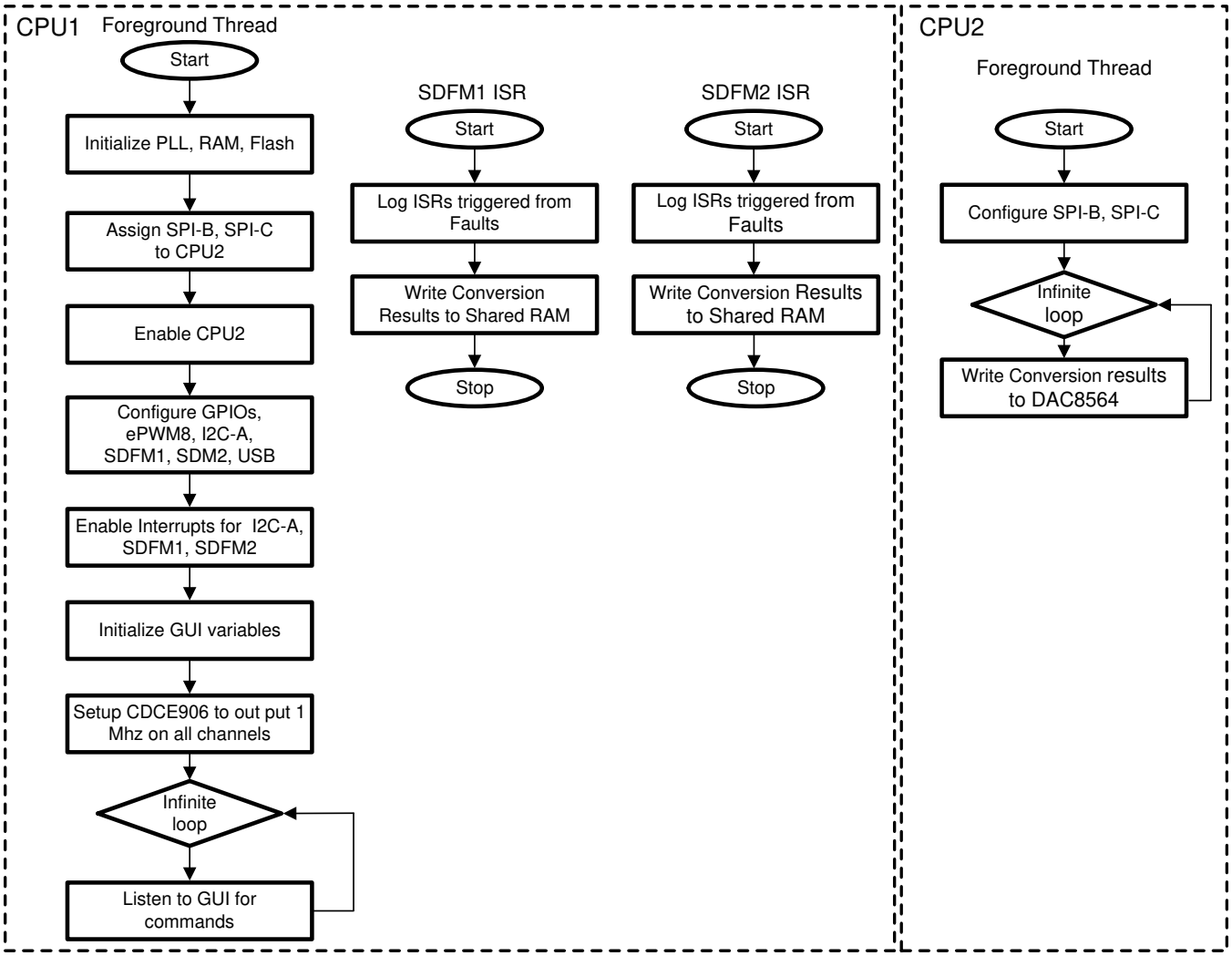


図 39. Firmware Flow Graph

The SDFM of the MCU is used for filter implementation. The SDFM features include:

- Eight external pins per SDFM module
  - ΔΣ data input pins per SDFM module (SD-Dx, where x = 1 to 4)
  - ΔΣ clock input pins per SDFM module (SD-Cx, where x = 1 to 4)
- Four different configurable modulator clock modes:
  - Modulator clock rate equals modulator data rate
  - Modulator clock rate running at half the modulator data rate
  - Modulator data is Manchester encoded. Modulator clock not required
  - Modulator clock rate is double that of modulator data rate
- Four independent configurable sinc filter units:
  - Four different filter type selections (sincfast, $sinc^1$, $sinc^2$, and $sinc^3$ options available)
  - Ability to bypass filter module
  - OSR value for filter unit programmable from 1 to 256 — 256 configured
  - Ability to enable and disable individual filter module
  - Ability to synchronize all the four independent filters of a SDFM module using the master filter enable (MFE) bit (or) using PWM signals
- Data filter output can be represented in either 16 or 32 bits
- PWMs can be used to generate a modulator clock for ΔΣ modulators

6 Test Setup

The board used for testing is shown in 図 40.

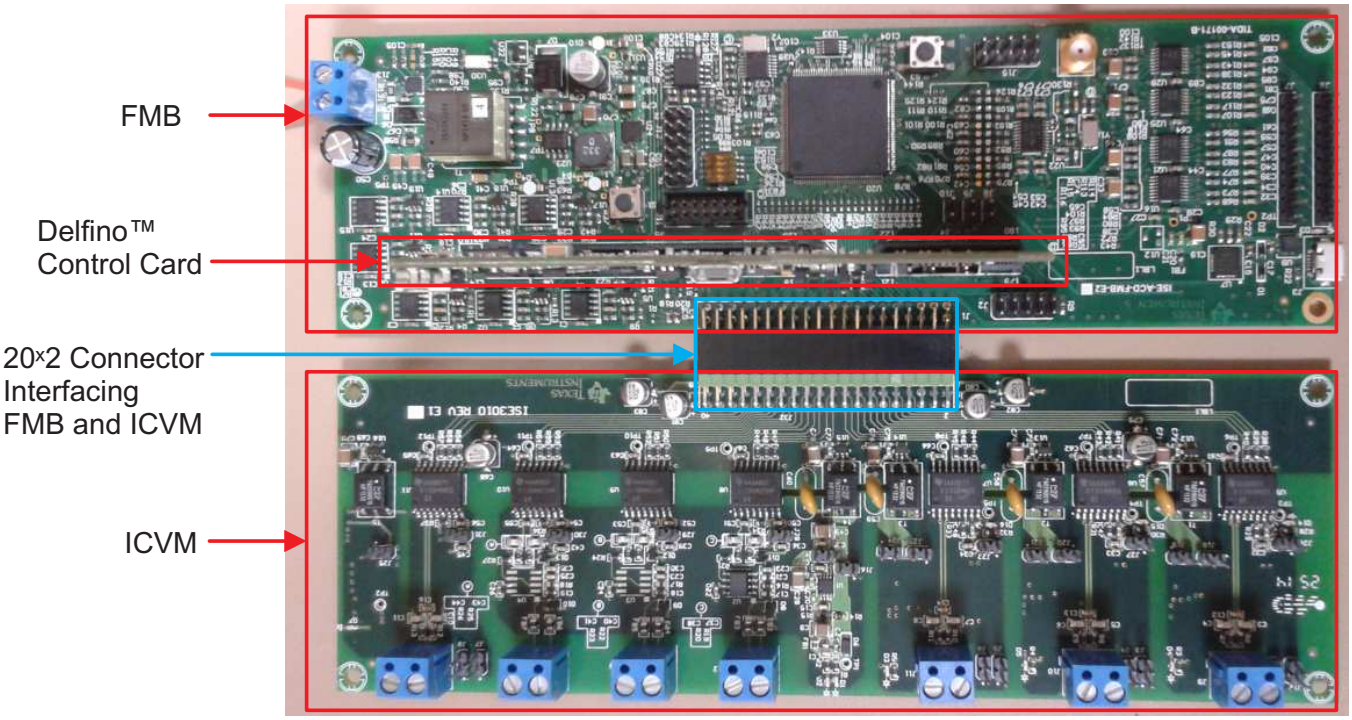


図 40. Assembled Board

The following equipment is used for testing:

- For DC input voltage: 2602 Keithley® System SourceMeter®
- For AC input voltage: Model DS360 Ultra Low Distortion Function Generator

6.1 GUI

This guide describes the functionality of the isolated current/voltage measurement test bench. The following sections explain the location and procedure for installing the software properly.

6.1.1 Installing Run-Time Engine

Download and install the LabVIEW Run-Time engine to use the IVIM Test Bench.

1. Click on the link to install the LabVIEW Run-Time Engine 2010 SP1 (32-bit Standard RTE) http://www.ni.com/download/labview-run-time-engine-2010-sp1/2292/en/
2. Run LVRTE2010_SP1f5std.exe to install the LabVIEW Run-Time Engine 2010 SP1 (32-bit Standard RTE).
3. Follow the installation wizard and complete the installation.

注: The installation files for the run-time engine are automatically extracted to a directory on disk. The installer does not remove the files after installing, if you want to remove these files from disk, be sure to note their location during the unzipping process.

6.1.2 Installing VISA

The VISA driver must be downloaded and installed to communicate with the device.

1. Click the link to install the NI-VISA 5.0.3. http://www.ni.com/download/ni-visa-5.0.3/2251/en/
2. Run visa503full_downloader.exe.
3. Follow the installation wizard and complete the installation.

6.1.3 Installing IVIM Test Bench

To install the IVIM test bench:

1. Select the Destination Directory for the IVIM Test Bench and click *Next*.

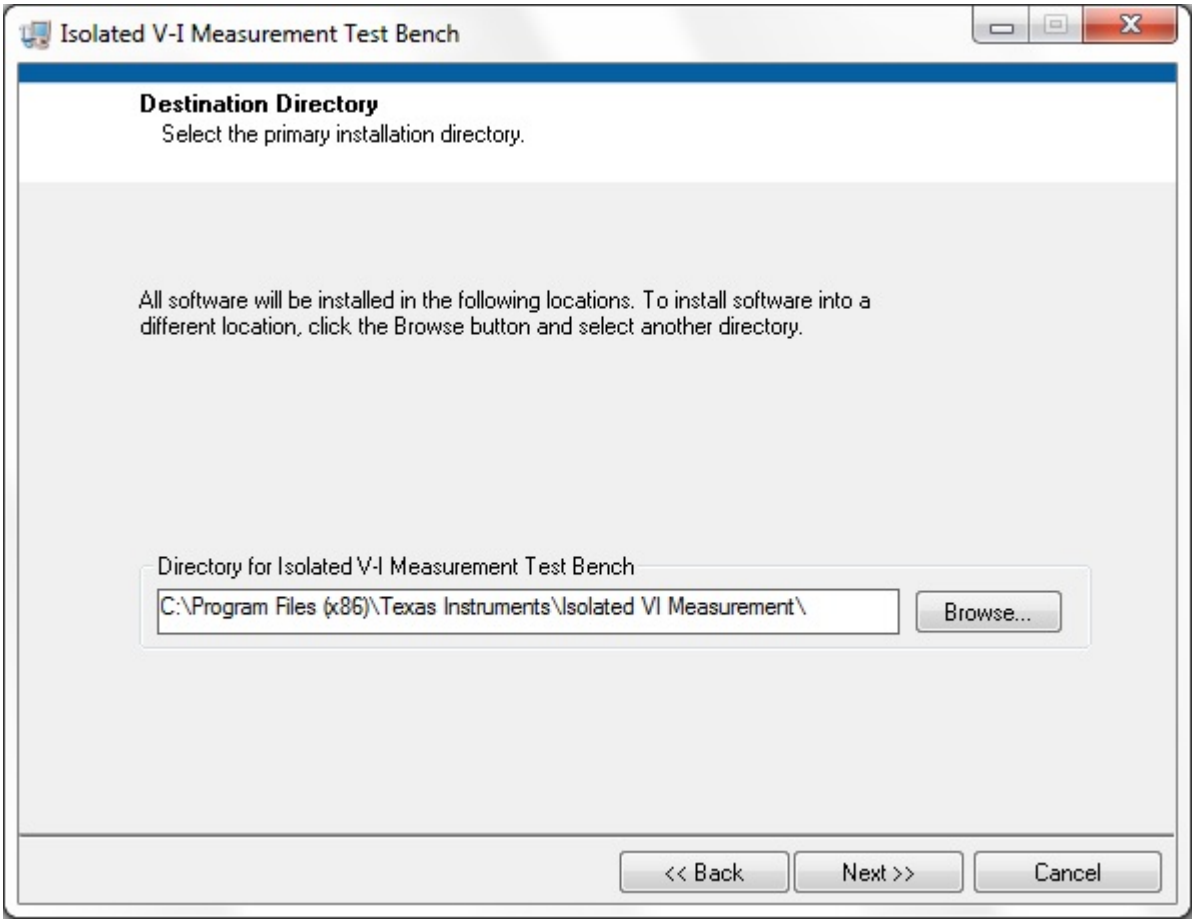


図 41. IVIM Test Bench Destination Directory

2. 図 42 shows the list of files that will be added or modified with this installation. Click *Next*.

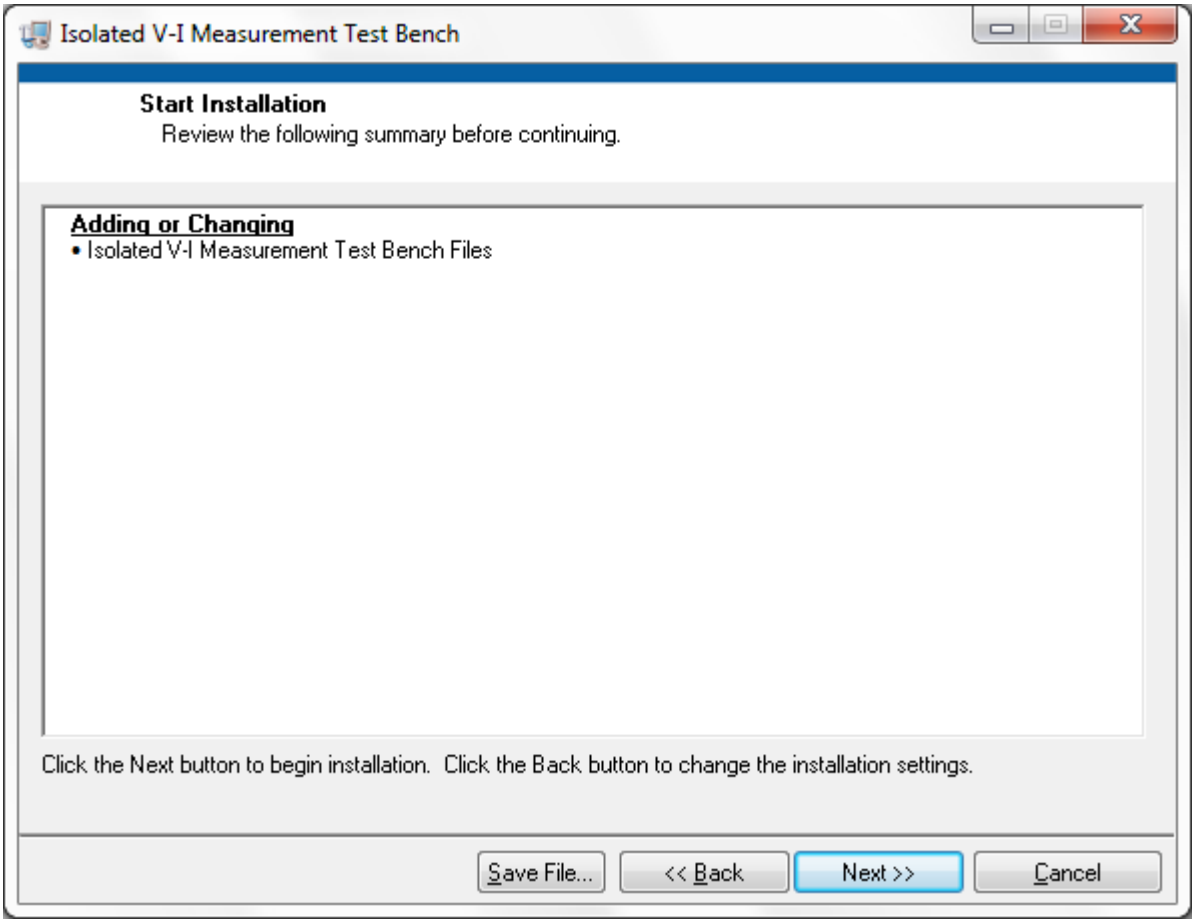


図 42. Files Added or Modified

3. The program installs and finishes as shown in 図 43. Click *Finish*.

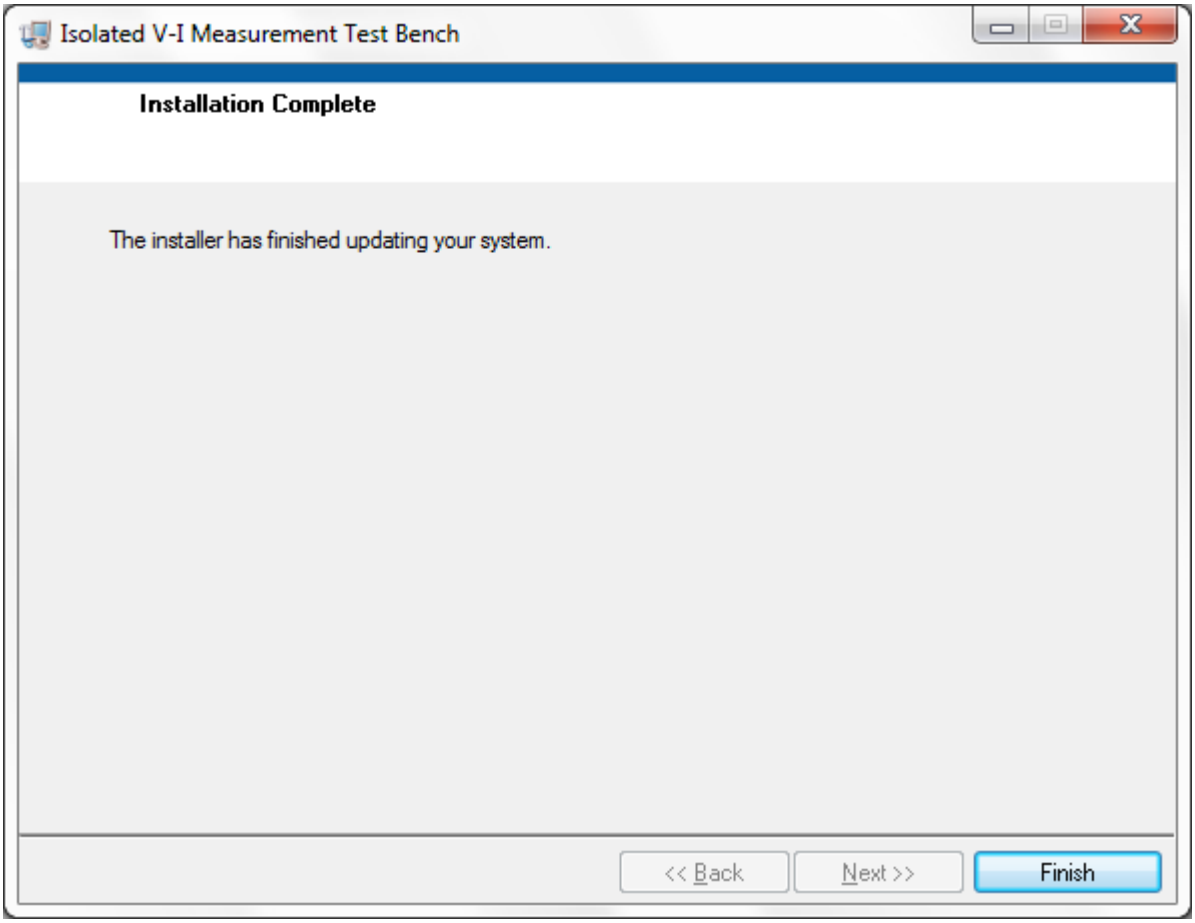


図 43. Installation Completes

6.2 Launching the IVIM Test Bench

Follow these steps to launch the IVIM Test Bench:

1. Locate the IVIM Test Bench through any of these approaches:
   - Desktop shortcut
   - Start menu shortcut
   - Installed folder location (the default location for Win 7: C:\Program Files (x86)\Texas Instruments\Isolated VI Measurement\)
2. Double-click on "Isolated V-I Measurement.exe" (highlighted in 図 44).

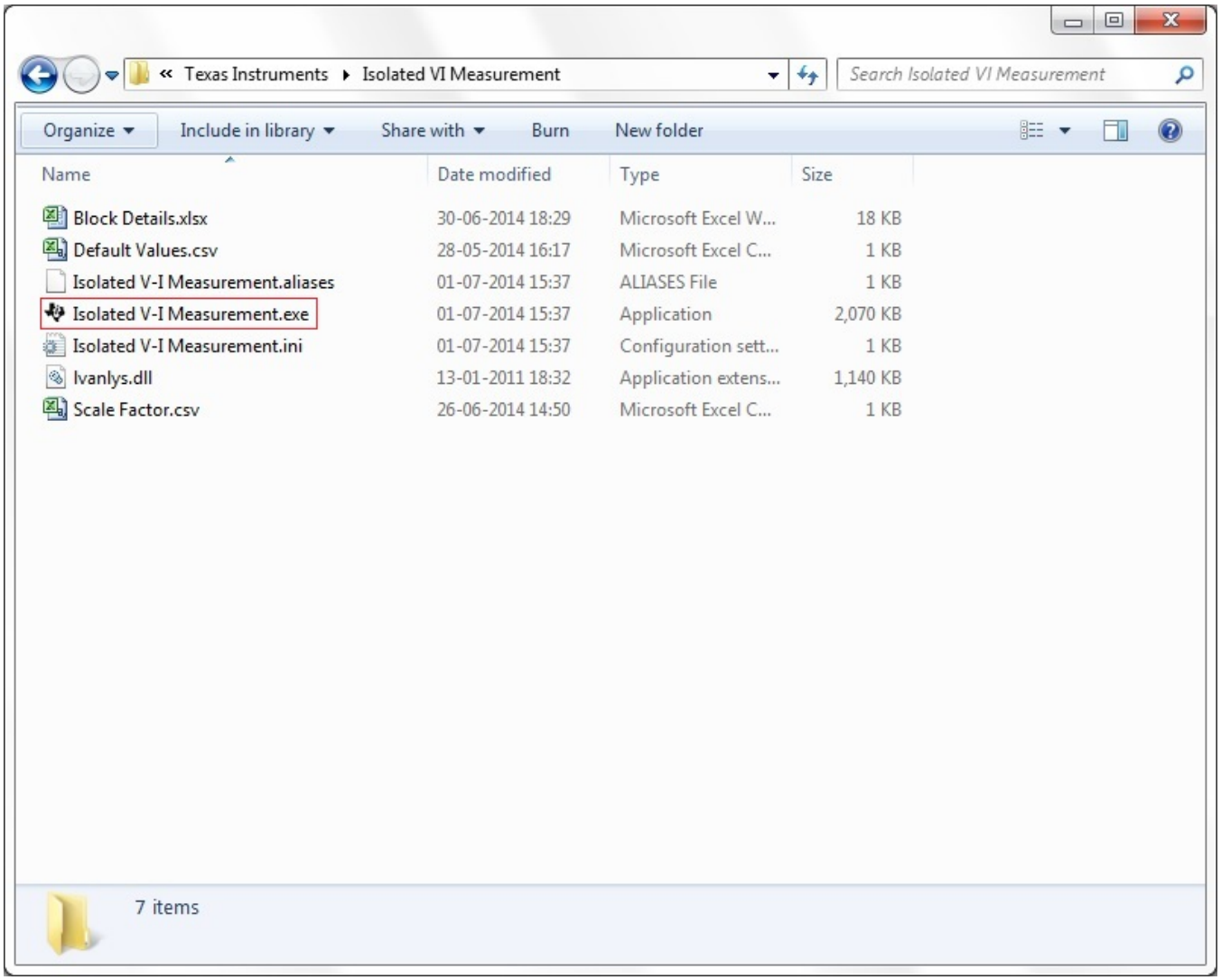


図 44. Isolated V-I Measurement Folder Structure

6.3 Mode Selection

The *Select a Mode* dialog box pops up as the application is launched. Select either MCU or FPGA, whichever is connected and the corresponding VISA resource name.

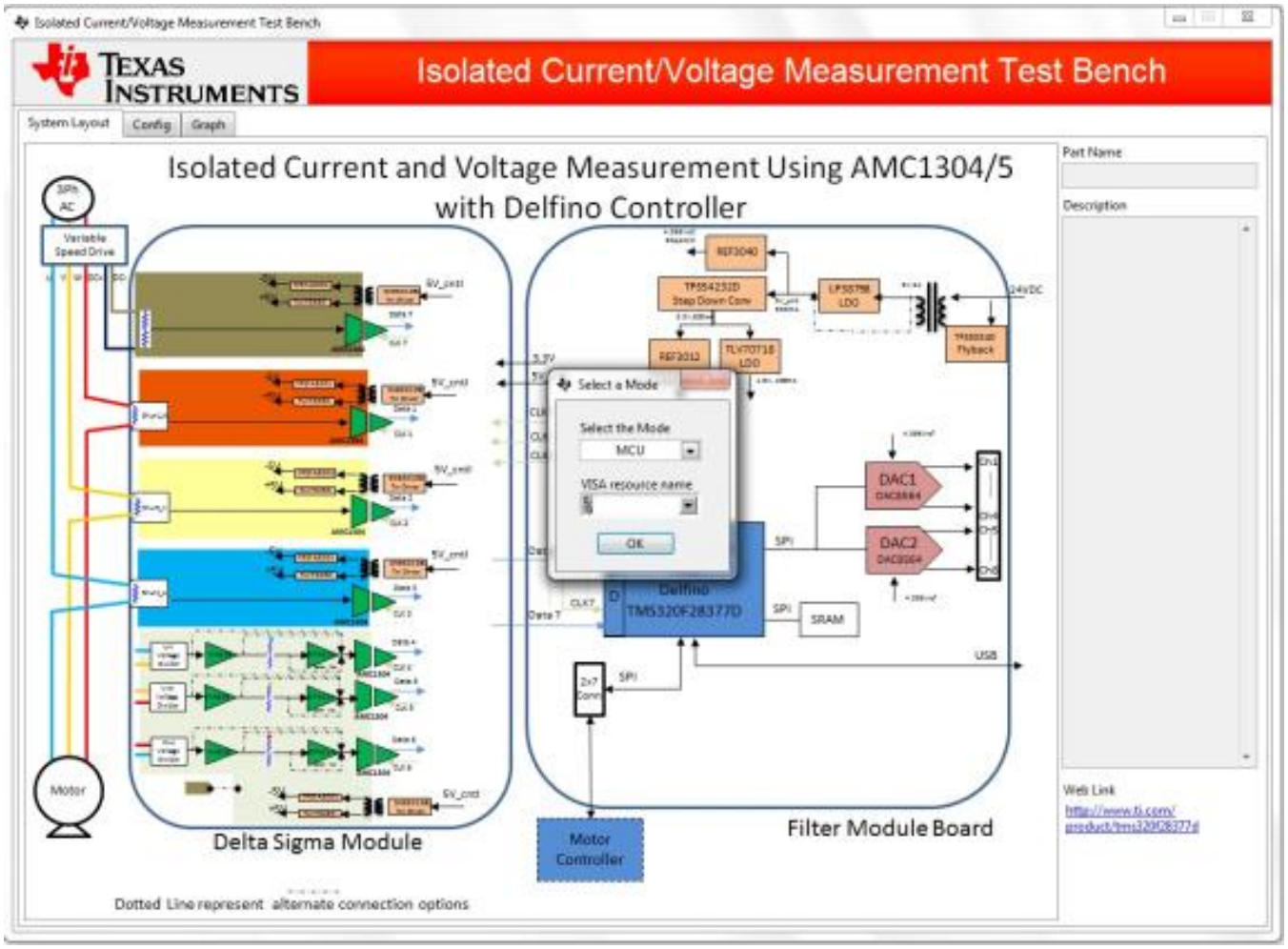


図 45. Mode Selection

As soon as the user selects the mode, the GUI starts to initialize.

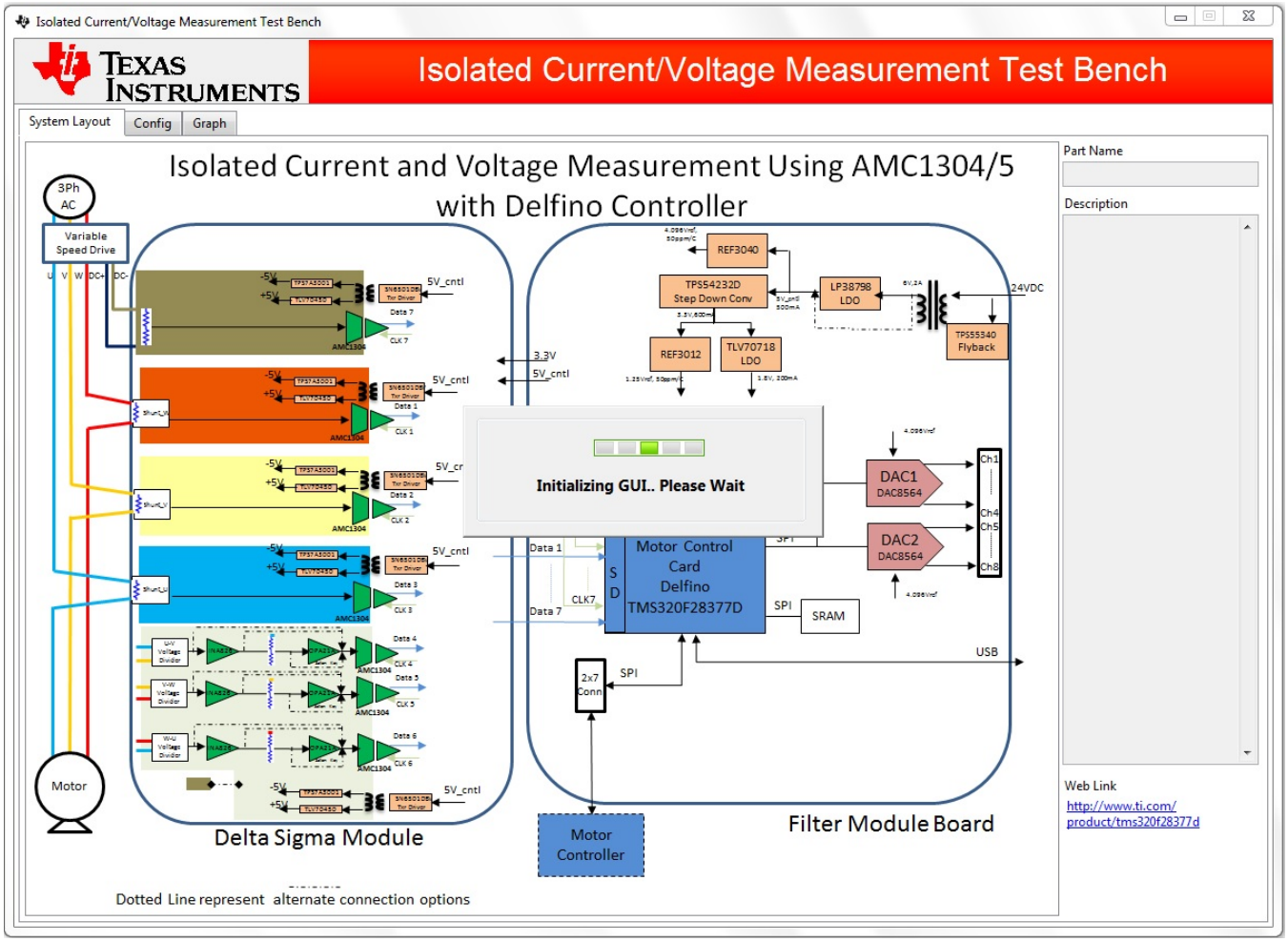


図 46. GUI Initialization

The user can proceed to use the GUI after the initialization completes.

6.4 IVIM Pages

The IVIM Test Bench has three pages:

1. System Layout
2. Config
3. Graph

6.4.1 System Layout Page

The system layout page has the block diagram with a description of the parts used in isolated current/voltage measurement. Moving the mouse pointer over any of the block shows the description of the same in right side of the page with a web link for reference.

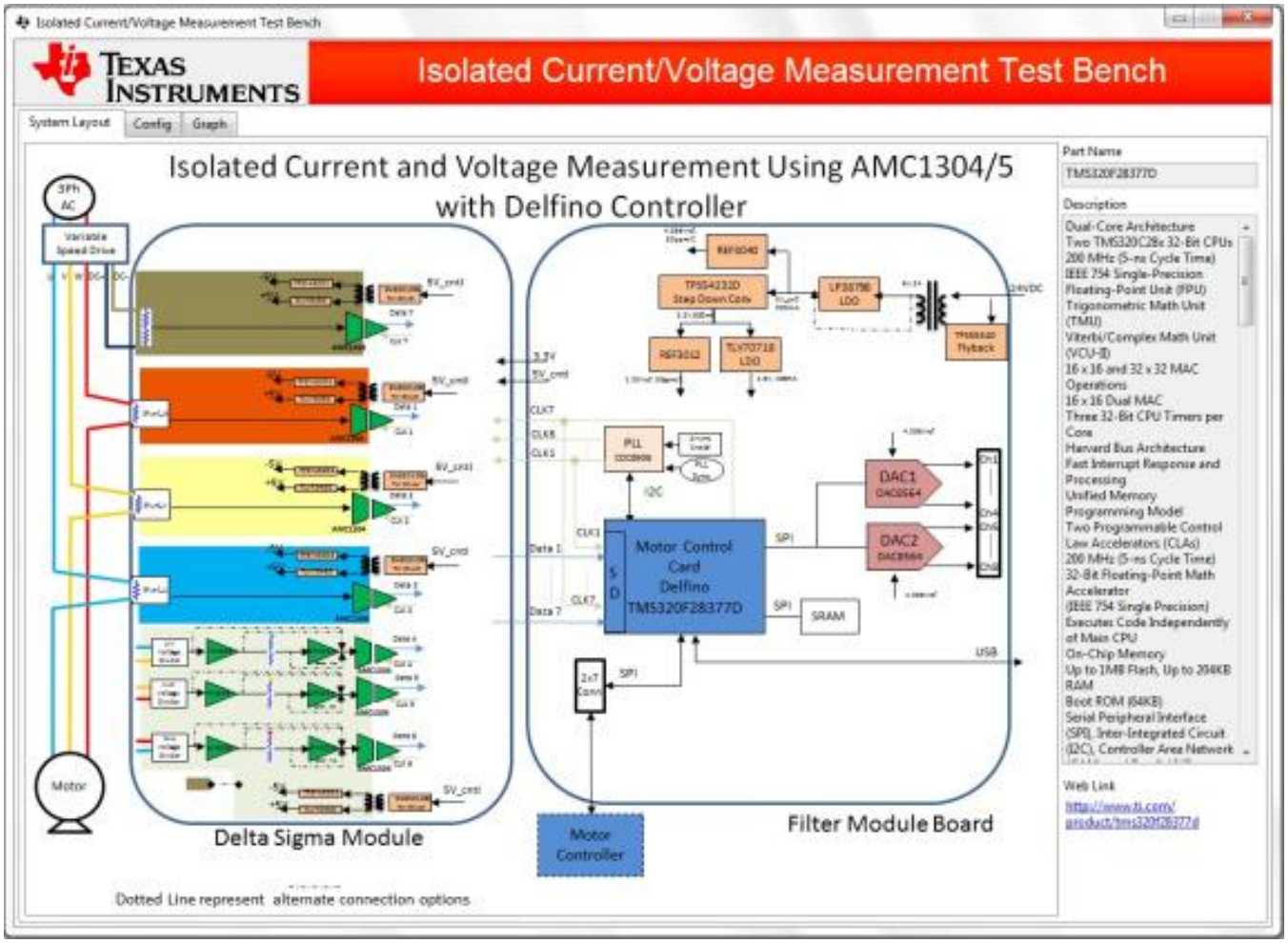


図 47. System Layout

The layout is as follows:

- **Block Diagram**: The block diagram gives the detailed description of the parts used for the ICVM.
- **Part Name**: This box displays the part name selected.
- **Description Box**: This box displays a brief description about the part in the block diagram.
- **Web Link Box**: This box displays the web reference of the part.

6.4.2 Configuration Page

This page allows the user to configure the ΔΣ filter parameters.

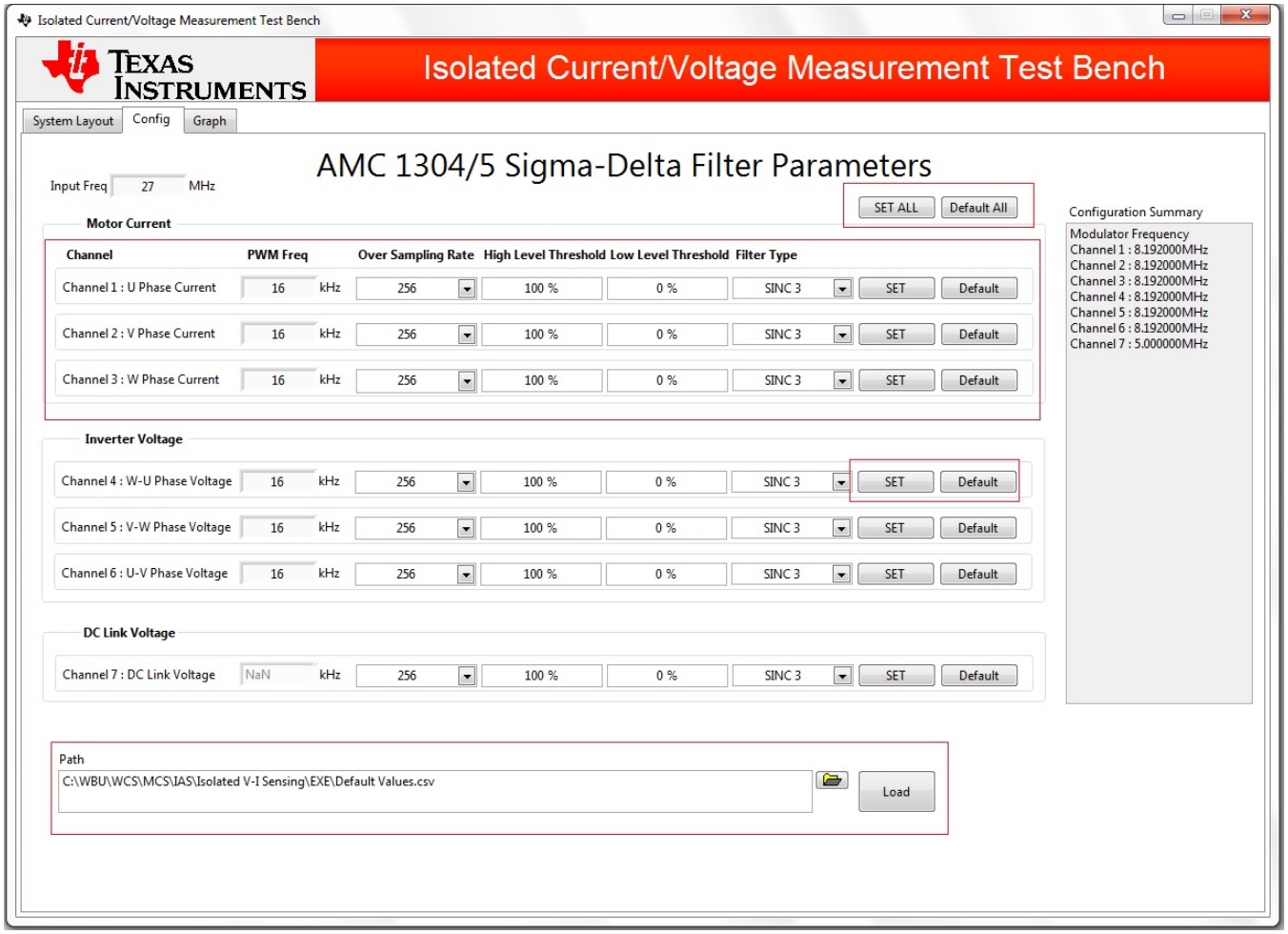


図 48. Config Page

The components of the configuration page are as follows:

- **Three Phase Currents** (designated motor current): Contains the settings for three channels which are to be configured for respective phase current
- **Three Phase Voltages** (designated inverter voltage): Contains the settings for three channels which are to be configured for respective phase voltage
- **Fourth Current-Neutral** (DC-link voltage): Contains the setting for a channel which is to be configured for measuring neutral current
- **Set Button**: Sets the configured settings for the corresponding row
- **Set All Button**: Sets the configured value for all channels
- **Default All**: Sets the default values for all channels
- **Load Button**: Loads the values for each parameter form the file specified in the in the path dialog box
- **Configuration Summary**: Displays the modulated frequency for each of the channels

6.4.2.1 Setting PWM Frequency and Oversampling Rate

The attributes of setting PWM frequency and oversampling rates:

- **PWM Frequency**: Enter the frequency value in the given text box in KHz.
- **Oversampling Rate**: Select the oversampling rate from the list.
- **Modulated Frequency**: The modulated frequency depends on the PWM frequency and oversampling rate. The modulated frequency is limited to 20 MHz.

6.4.2.2 Setting the Filter Type

The filter type for each channel can be set from the list shown in 図 49.

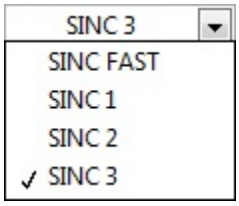


図 49. Channel Filter Type

6.4.2.3 Setting Default Value

Each channel can be configured to their default values using the *Default* button provided for each channel. The user can also use the *Default All* button to set default values to all the channels.

6.4.2.4 Configuration Summary

The configuration summary box gives the calculated modulated frequency for each channel. The modulated frequency has a limit of 5 to 20 MHz when the set values exceed the limit, the values are coerced, and the summary box indicates the error with a notification as shown in 図 50.

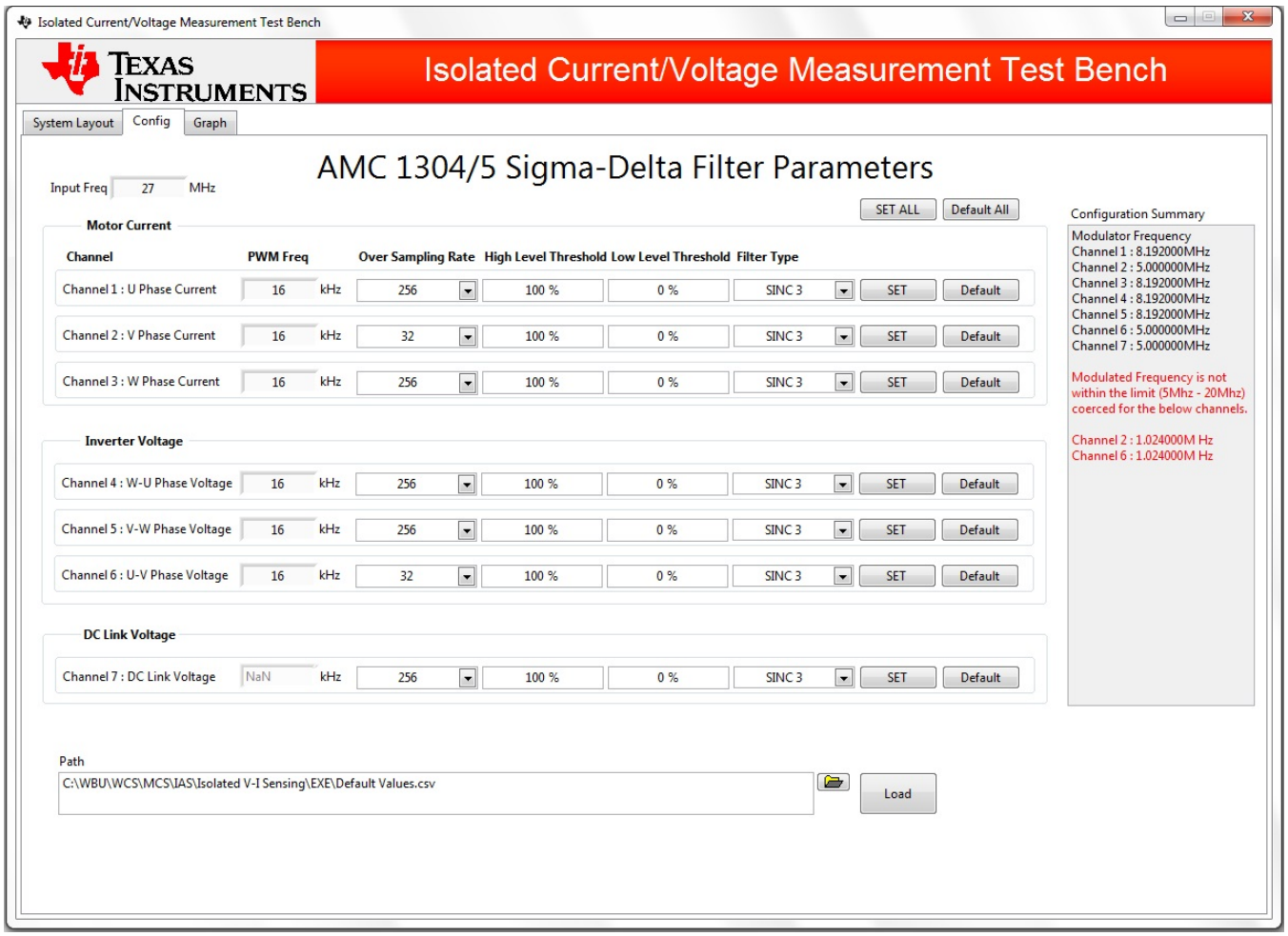


図 50. Configuration Summary

6.4.2.5 Loading the Default Value File

Select the default value file using the path control available and click on the *Load* button to load the settings to the user interface.

図 51. Load Default Values File

6.4.2.6 Setting Configuration

Set the final channel configuration using the *Set* buttons provided with each channel, or use the *Set All* button to set all channels configurations. When the *Set All* button is pressed, all the details in the config page are sent to MCU/FPGA.

6.4.3 Graph

The graph page is the result display and processing page (see 図 52). The captured values will be displayed as graphs in this page as time/frequency domain.

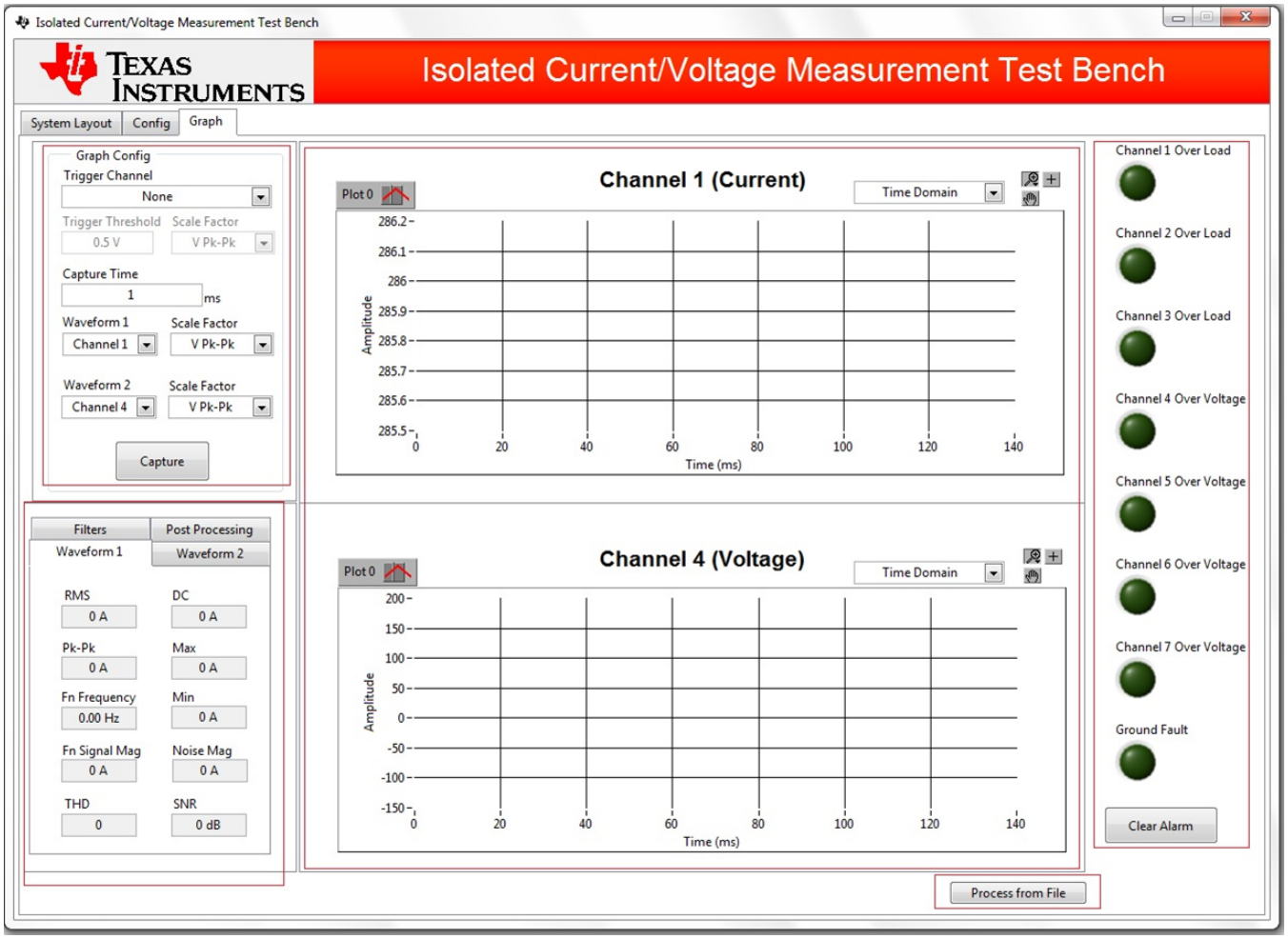


図 52. Graph Page

- **Graph Config**: Set the trigger modes and select waveforms to display.
- **Waveform Parameter Display**: The parameters of the selected waveform is displayed in this pane.
- **Graph Pane**: The captured data is plotted in the form of graph in this pane.
- **Error indicators**: Eight indicators to indicate the error. And clear alarm to clear the indication.
- **Process from File button**: The data from the file can be plotted in graph using this button.

6.4.3.1 Setting the Trigger Channel

The trigger channel can be set using the *Trigger Channel* control. The user can select any of the channels available.

- Set the trigger threshold of the selected channel in the *Trigger Threshold* control
- Select the scale factor from the *Scale Factor* control.
- Set capture time in milliseconds (ms) in the *Capture Time* control.

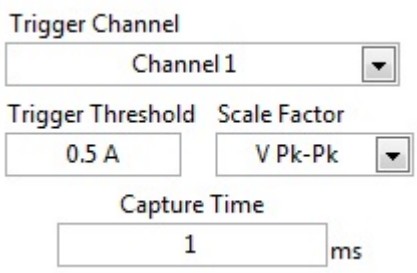


図 53. Trigger Configuration

6.4.3.2 Selecting the Waveform and Scale Factor

The waveform to be displayed and their corresponding scale factors can be selected from the *Waveform 1* and *Waveform 2* control. The scale factors are selected from their respective controls.

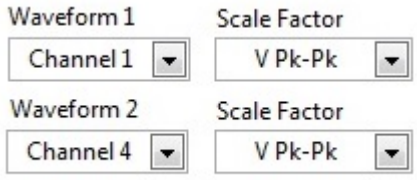


図 54. Waveform Settings

6.4.3.3 Selecting the Filter

Select the filter from the *Type* control. Set the filter characteristics by using the *Filter Type*, *High* and *Low Cutoff Freq.*, and *Order* controls.

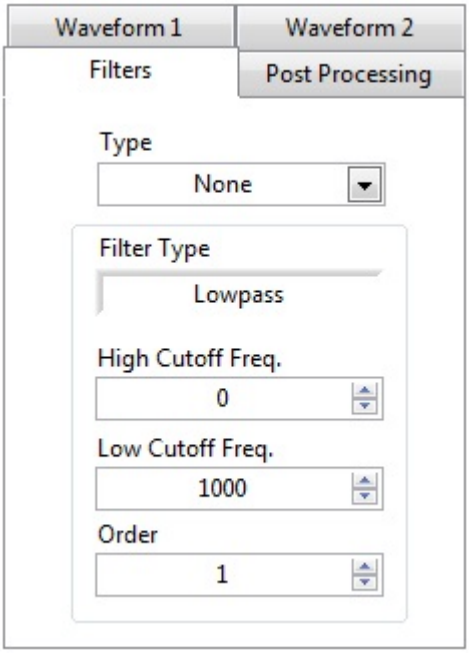


図 55. Filter Selection

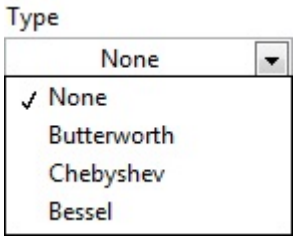


図 56. Filter Characteristics

6.4.3.4 FFT Window Selection

Set FFT windows using the *FFT-Window* control in the *Post Processing* tab.

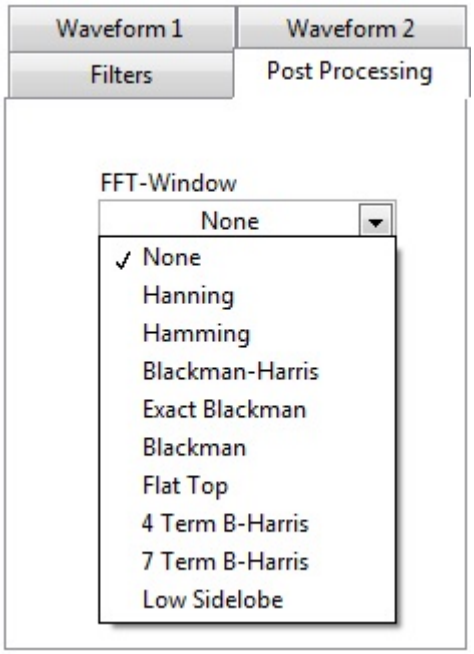


図 57. FFT Window Selection

6.4.3.5 Waveform Parameter Display

The parameters of the selected channel waveform can be seen from its waveform page as shown in 図 58.

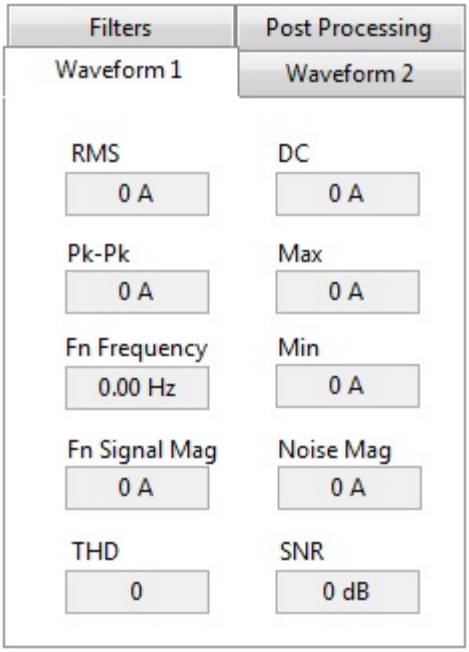


図 58. Waveform Parameter Display

6.4.3.6 Data Capture

Capture mode sends the corresponding settings to MCU/FPGA and gets the data for the time specified and displays it once in the graph.

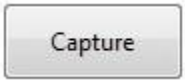


図 59. Capture Button

6.4.3.7 Selecting the Domain

Select the graph domain using the control provided for each graph. The user can select *Time Domain* or *Frequency Domain* using this control.

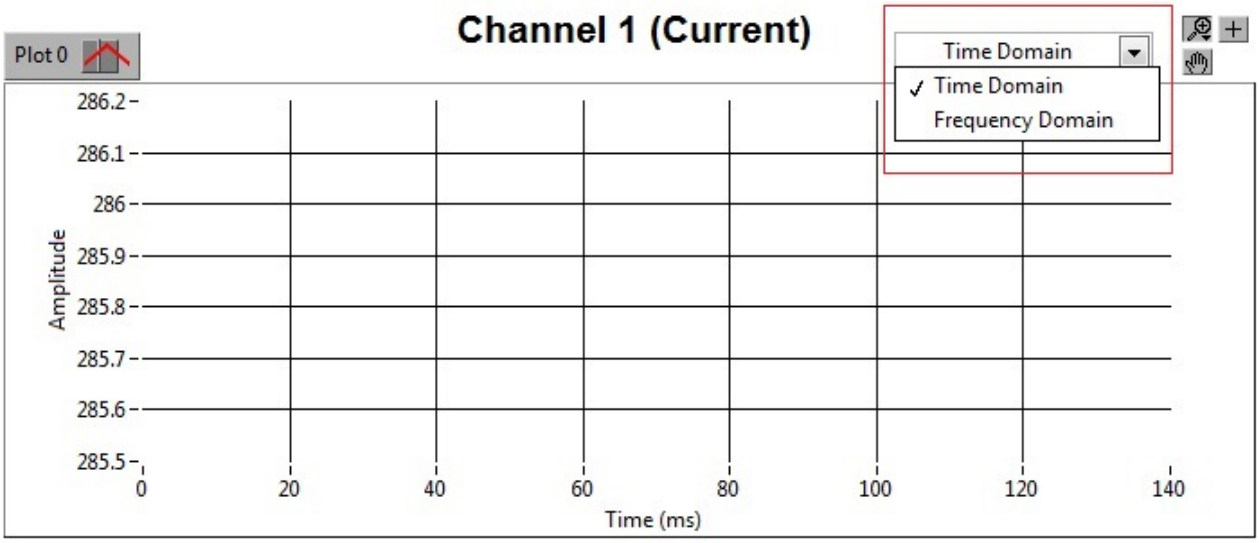


図 60. Graph Domain Selection

6.5 Editing the Scale Factor (Calibration)

The scale factor values are read from the "Scale Factor.csv" file and then loaded to the user interface. The scale factor file is placed in the same folder of the executable: Win 7: C:\Program Files (x86)\Texas Instruments\Isolated VI Measurement\

- The scale factor is the value used to convert the raw data into the equivalent voltage or current specified by the user.
- The offset is the value used to calibrate the fixed offset errors. This value will be subtracted from the raw value received from MCU/FPGA.

The structure of the scale factor file is as shown in 表 14.

表 14. Structure of Scale Factor File

SCALE LABEL	SCALE FACTOR	OFFSET
V Pk-Pk	0.023103	0
V @APC	0.00021	0
Current	3.81E-05	0
V_Inamp	0.021437137	0
Raw	1	0
CH1 CAL	3.83E-05	0
CH2 CAL	3.81E-05	0

注: Do not change the structure of the file by adding or deleting any columns. The user can only add or delete the rows.

6.6 Editing Default Values

The default value for each channel is read from the "Default Values.csv" file. The structure of this file is shown in 表 15.

表 15. Structure of Default Values

CHANNEL NAME	MODULATOR CLOCK FREQUENCY	OSR	HIGH LEVEL THRESHOLD	LOW LEVEL THRESHOLD	FILTER TYPE
1	16	256	100	0	$Sinc^3$
2	16	256	100	0	$Sinc^3$
3	16	256	100	0	$Sinc^3$
4	16	256	100	0	$Sinc^3$
5	16	256	100	0	$Sinc^3$
6	16	256	100	0	$Sinc^3$
7	16	256	100	0	$Sinc^3$

The user can edit the necessary field and save the changes.

注: Do not change the structure of the file by adding or deleting any columns or rows.

7 Test Results

7.1 Current Accuracy

The current accuracy test conditions are shown in 表 16 through 表 21, listed by channel, DC, and AC accuracy. The parameters used are:

- Individual current channels measurement (Individual channels are electrically isolated)
- Frequency for AC input is 50 Hz
- Averaging of samples done for 100 ms

表 16. DC Current Channel 1 Accuracy

INPUT AS % OF FULL SCALE (100% = 250 mV)	APPLIED DC (mV)	CHANNEL 1 DC (mV)	CHANNEL 1 ERROR (%)
5%	12.46	13.411	–0.14
10%	24.961	25.907	–0.09
15%	37.501	38.447	–0.06
20%	50.002	50.92	–0.10
25%	62.5	63.407	–0.10
30%	75.012	75.851	–0.17
35%	87.499	88.346	–0.14
40%	100.005	100.841	–0.13
45%	112.51	113.303	–0.16
50%	125.01	125.817	–0.13
55%	137.51	138.284	–0.14
60%	150.01	150.775	–0.14
65%	162.51	163.276	–0.12
70%	175.01	175.746	–0.13
75%	187.51	188.261	–0.12
80%	200.01	200.721	–0.13
85%	212.51	213.201	–0.13
90%	225.01	225.665	–0.14
95%	237.5	238.169	–0.13
100%	250.01	250.665	–0.13
Offset **0.968304**			

表 17. AC Current Channel 1 Accuracy

INPUT AS % OF FULL SCALE (100% = 175 mV)	APPLIED AC (mV)	CHANNEL 1 AC (mV)	CHANNEL 1 ERROR (%)
5%	8.751	8.462	–0.44
10%	17.503	17.218	–0.20
15%	26.257	25.977	–0.11
20%	35.005	34.735	–0.06
25%	43.759	43.492	–0.04
30%	52.502	52.249	–0.01
35%	61.255	61.008	0.01
40%	70.006	69.765	0.01
45%	78.748	78.514	0.02
50%	87.504	87.279	0.03
55%	96.246	96.042	0.05
60%	105.058	104.87	0.06
65%	113.712	113.536	0.07
70%	122.48	122.351	0.10
75%	131.2	131.134	0.14
80%	140.08	140.048	0.16
85%	148.73	148.709	0.15
90%	157.52	157.57	0.19
95%	166.21	166.262	0.18
100%	174.97	175.073	0.20
Offset **–0.25**			

表 18. DC Current Channel 2 Accuracy

INPUT AS % OF FULL SCALE (100% = 250 mV)	APPLIED DC (mV)	CHANNEL 2 DC (mV)	CHANNEL 2 ERROR (%)
5%	12.5	13.099	0.07
10%	24.99	25.572	–0.03
15%	37.52	38.084	–0.07
20%	50.02	50.565	–0.09
25%	62.52	63.051	–0.10
30%	75.02	75.537	–0.10
35%	87.51	88.025	–0.09
40%	100.02	100.513	–0.10
45%	112.52	112.995	–0.10
50%	125.02	125.482	–0.10
55%	137.51	137.975	–0.09
60%	150.01	150.462	–0.09
65%	162.51	162.958	–0.09
70%	175.01	175.449	–0.09
75%	187.51	187.94	–0.09
80%	200.01	200.433	–0.08
85%	212.51	212.924	–0.08
90%	225.01	225.41	–0.08
95%	237.51	237.906	–0.08
100%	250.08	250.467	–0.08
Offset **0.590516**			

表 19. AC Current Channel 2 Accuracy

INPUT AS % OF FULL SCALE (100% = 175 mV)		APPLIED AC (mV)	CHANNEL 2 AC (mV)	CHANNEL 2 ERROR (%)
5%		8.755	8.561	0.03
10%		17.514	17.3	–0.10
15%		26.26	26.033	–0.12
20%		35.024	34.797	–0.09
25%		43.753	43.521	–0.08
30%		52.508	52.281	–0.06
35%		61.248	61.022	–0.05
40%		70	69.771	–0.05
45%		78.75	78.522	–0.04
50%		87.505	87.278	–0.03
55%		96.249	96.019	–0.03
60%		105.054	104.832	–0.02
65%		113.771	113.599	0.02
70%		122.54	122.311	–0.03
75%		131.5	131.298	0.00
80%		140	139.904	0.07
85%		148.77	148.572	0.00
90%		157.49	157.279	–0.01
95%		166.21	166.021	0.00
100%		175.09	175.929	0.08
Offset	**–0.19649**			

表 20. DC Current Channel 3 Accuracy

INPUT AS % OF FULL SCALE (100% = 250 mV)		APPLIED DC (mV)	CHANNEL 3 DC (mV)	CHANNEL 3 ERROR (%)
5%		12.5	13.048	0.05
10%		24.99	25.514	–0.07
15%		37.52	38.026	–0.10
20%		50.02	50.499	–0.12
25%		62.52	62.98	–0.13
30%		75.02	75.458	–0.14
35%		87.51	87.944	–0.12
40%		100.02	100.426	–0.14
45%		112.52	112.902	–0.14
50%		125.02	125.383	–0.14
55%		137.51	137.873	–0.13
60%		150.01	150.354	–0.13
65%		162.51	162.845	–0.13
70%		175.01	175.33	–0.13
75%		187.51	187.818	–0.12
80%		200.01	200.302	–0.12
85%		212.51	212.788	–0.12
90%		225.01	225.268	–0.13
95%		237.51	237.759	–0.12
100%		250.08	250.312	–0.12
Offset	**0.541419**			

表 21. AC Current Channel 3 Accuracy

INPUT AS % OF FULL SCALE (100% = 175 mV)	APPLIED AC (mV)	CHANNEL 3 AC (mV)	CHANNEL 3 ERROR (%)
5%	8.755	8.549	–0.11
10%	17.514	17.29	–0.16
15%	26.26	26.022	–0.16
20%	35.024	34.782	–0.13
25%	43.753	43.504	–0.12
30%	52.508	52.262	–0.09
35%	61.248	60.999	–0.09
40%	70	69.746	–0.08
45%	78.75	78.494	–0.08
50%	87.505	87.246	–0.07
55%	96.249	95.984	–0.07
60%	105.054	104.793	–0.06
65%	113.771	113.558	–0.01
70%	122.54	122.267	–0.06
75%	131.5	131.25	–0.04
80%	140	139.754	–0.04
85%	148.77	148.519	–0.04
90%	157.49	157.222	–0.05
95%	166.21	165.96	–0.03
100%	175.09	174.866	–0.02
Offset **–0.19649**			

図 61 and 図 62 show the combined graphs for current DC and current AC accuracy.

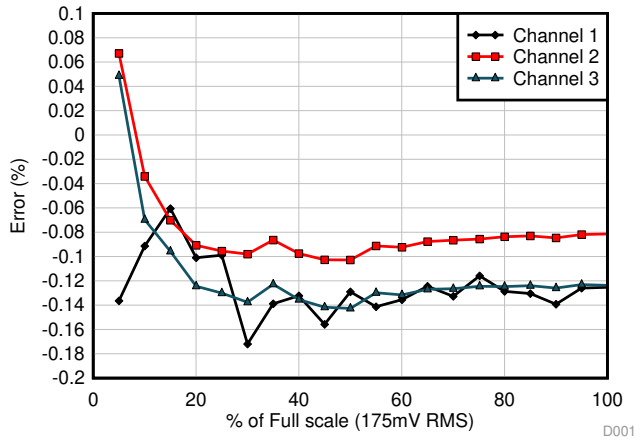


図 61. DC Current Accuracy

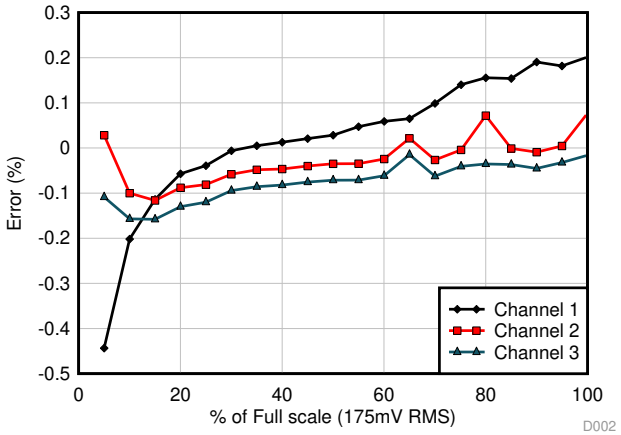


図 62. AC Current Accuracy

7.2 Multiple ΔΣ Modulators Cascaded for Wider Current Input

表 22 and 表 23 provide information for Channels 2 and 3 cascaded.

表 22. DC Current Channel 2 Accuracy

INPUT AS % OF FULL SCALE (100% = 250 mV)		APPLIED AC (mV)	CHANNEL 2 AC (mV)	CHANNEL 2 ERROR (%)
5%		12.502	12.436	–0.14%
10%		24.997	24.955	0.02%
20%		50.003	49.964	0.02%
30%		75.004	74.983	0.04%
40%		100.003	99.979	0.02%
50%		124.943	124.926	0.02%
60%		149.943	149.929	0.02%
70%		174.946	174.936	0.02%
80%		199.945	199.949	0.03%
90%		224.939	224.953	0.03%
100%		249.958	249.986	0.03%
Offset	**–0.047945**			

表 23. DC Current Channel 3 Accuracy

INPUT AS % OF FULL SCALE (100% = 250 mV)		APPLIED AC (mV)	CHANNEL 3 AC (mV)	CHANNEL 3 ERROR (%)
5%		12.502	12.38	–0.18%
10%		24.997	24.897	0.00%
20%		50.003	49.899	–0.01%
30%		75.004	74.912	0.01%
40%		100.003	99.9	0.00%
50%		124.943	124.834	–0.01%
60%		149.943	149.827	–0.01%
70%		174.946	174.824	–0.01%
80%		199.945	199.827	–0.01%
90%		224.939	224.953	0.05%
100%		249.958	249.845	–0.01%
Offset	**–0.0991915**			

The combined graph for DC accuracy is shown in 図 63.

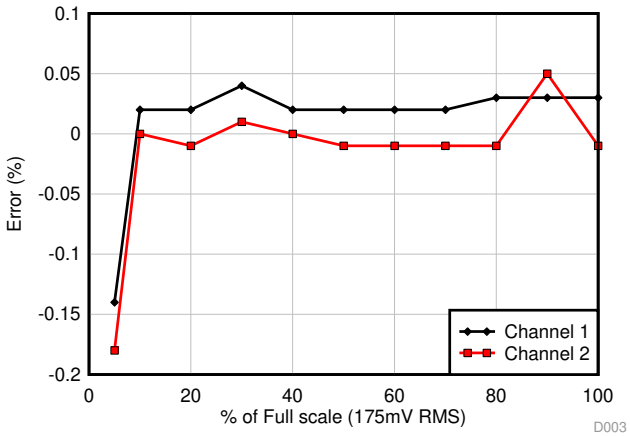


図 63. DC Current Channels Cascaded Accuracy

7.3 Voltage Accuracy

The following tables provide information to measure voltage accuracy for AC and DC Channels 1 through 3. The following parameters are used:

- All the voltage channels share the same isolated power supply
- Frequency for AC input is 50 Hz
- Averaging of samples done for 100 ms

表 24. DC Voltage Channel 1 Accuracy

INPUT AS % OF FULL SCALE (100% = 250 mV)	APPLIED DC (mV)	CHANNEL 1 DC (mV)	CHANNEL 1 ERROR (%)
5%	12.5	13.448	0.03%
10%	25.1	26.033	–0.05%
15%	37.52	38.439	–0.07%
20%	50.02	50.919	–0.09%
25%	62.51	63.412	–0.07%
30%	75.02	75.9	–0.09%
35%	87.51	88.384	–0.08%
40%	100.01	100.877	–0.08%
45%	112.52	113.367	–0.09%
50%	125.01	125.86	–0.08%
55%	137.51	138.351	–0.08%
60%	150.01	150.984	0.02%
65%	162.51	163.475	0.01%
70%	175.01	175.996	0.02%
75%	187.51	188.403	–0.03%
80%	200.01	200.89	–0.03%
85%	212.5	213.366	–0.04%
90%	225.01	225.865	–0.04%
95%	237.51	238.371	–0.04%
100%	250.01	250.891	–0.03%
Offset **0.944315**			

表 25. AC Voltage Channel 1 Accuracy

INPUT AS % OF FULL SCALE (100% = 175 mV)		APPLIED AC (mV)	CHANNEL 1 AC (mV)	CHANNEL 1 ERROR (%)
5%		8.737	8.798	–0.33%
10%		17.507	17.565	–0.19%
15%		26.253	26.328	–0.06%
20%		35.001	35.097	0.02%
25%		43.751	43.868	0.06%
30%		52.503	52.558	–0.07%
35%		61.252	61.413	0.12%
40%		70.004	70.176	0.12%
45%		78.752	78.943	0.13%
50%		87.498	87.695	0.12%
55%		96.247	96.468	0.14%
60%		105.058	105.290	0.14%
65%		113.814	114.061	0.14%
70%		122.460	122.747	0.16%
75%		131.270	131.514	0.12%
80%		140.003	140.364	0.19%
85%		148.800	149.142	0.17%
90%		157.510	157.839	0.15%
95%		166.240	166.598	0.16%
100%		175.020	175.413	0.17%
Offset	**0.09**			

表 26. DC Voltage Channel 2 Accuracy

INPUT AS % OF FULL SCALE (100% = 250 mV)		APPLIED DC (mV)	CHANNEL 2 DC (mV)	CHANNEL 2 ERROR (%)
5%		12.5	13.6	0.02%
10%		25.1	26.18	–0.07%
15%		37.52	38.583	–0.09%
20%		50.02	51.06	–0.11%
25%		62.51	63.544	–0.10%
30%		75.02	76.031	–0.11%
35%		87.51	88.511	–0.11%
40%		100.01	100.998	–0.11%
45%		112.52	113.486	–0.12%
50%		125.01	125.977	–0.10%
55%		137.51	138.459	–0.11%
60%		150.01	151.092	–0.01%
65%		162.51	163.575	–0.02%
70%		175.01	176.094	–0.01%
75%		187.51	188.497	–0.06%
80%		200.01	200.981	–0.06%
85%		212.5	213.453	–0.07%
90%		225.01	225.946	–0.07%
95%		237.51	238.446	–0.07%
100%		250.01	250.963	–0.06%
Offset	**1.09651**			

表 27. AC Voltage Channel 2 Accuracy

INPUT AS % OF FULL SCALE (100% = 175 mV)	APPLIED AC (mV)	CHANNEL 2 AC (mV)	CHANNEL 2 ERROR (%)
5%	8.737	8.799	–0.32%
10%	17.507	17.564	–0.19%
15%	26.253	26.328	–0.06%
20%	35.001	35.095	0.01%
25%	43.751	43.865	0.05%
30%	52.503	52.554	–0.07%
35%	61.252	61.408	0.11%
40%	70.004	70.176	0.12%
45%	78.752	78.937	0.12%
50%	87.498	87.695	0.12%
55%	96.247	96.468	0.14%
60%	105.058	105.281	0.13%
65%	113.814	114.049	0.13%
70%	122.46	122.736	0.15%
75%	131.27	131.502	0.11%
80%	140.003	140.364	0.19%
85%	148.8	149.127	0.16%
90%	157.51	157.839	0.15%
95%	166.24	166.598	0.16%
100%	175.02	175.395	0.16%
Offset **0.09**			

表 28. DC Voltage Channel 3 Accuracy

INPUT AS % OF FULL SCALE (100% = 250 mV)	APPLIED DC (mV)	CHANNEL 3 DC (mV)	CHANNEL 3 ERROR (%)
5%	12.46	13.444	–0.12%
10%	24.961	25.944	–0.06%
15%	37.501	38.489	–0.03%
20%	50.002	50.967	–0.07%
25%	62.5	63.459	–0.06%
30%	75.012	75.907	–0.14%
35%	87.499	88.406	–0.10%
40%	100.005	100.907	–0.10%
45%	112.51	113.377	–0.12%
50%	125.01	125.817	–0.15%
55%	137.51	138.367	–0.10%
60%	150.01	150.861	–0.10%
65%	162.51	163.367	–0.09%
70%	175.01	175.841	–0.10%
75%	187.51	188.359	–0.08%
80%	200.01	200.823	–0.09%
85%	212.51	213.201	–0.14%
90%	225.01	225.774	–0.10%
95%	237.5	238.28	–0.09%
100%	250.01	250.78	–0.09%
Offset **0.99818**			

表 29. AC Voltage Channel 3 Accuracy

INPUT AS % OF FULL SCALE (100% = 175 mV)		APPLIED AC (mV)	CHANNEL 3 AC (mV)	CHANNEL 3 ERROR (%)
5%		8.751	8.466	–0.63%
10%		17.503	17.224	–0.28%
15%		26.257	25.986	–0.16%
20%		35.005	34.747	–0.08%
25%		43.759	43.507	–0.05%
30%		52.502	52.267	–0.01%
35%		61.255	61.029	0.01%
40%		70.006	69.79	0.02%
45%		78.748	78.514	0.00%
50%		87.504	87.31	0.04%
55%		96.246	96.042	0.03%
60%		105.058	104.907	0.08%
65%		113.712	113.576	0.08%
70%		122.48	122.395	0.12%
75%		131.2	131.181	0.16%
80%		140.08	140.098	0.18%
85%		148.73	148.76	0.17%
90%		157.52	157.57	0.18%
95%		166.21	166.317	0.20%
100%		174.97	175.131	0.22%
Offset	**–0.23**			

The graphs for voltage DC and AC voltage accuracy are shown in 図 64 and 図 65.

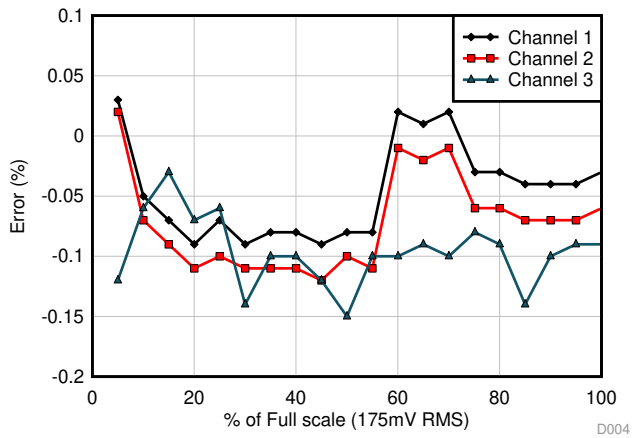


図 64. DC Voltage Accuracy

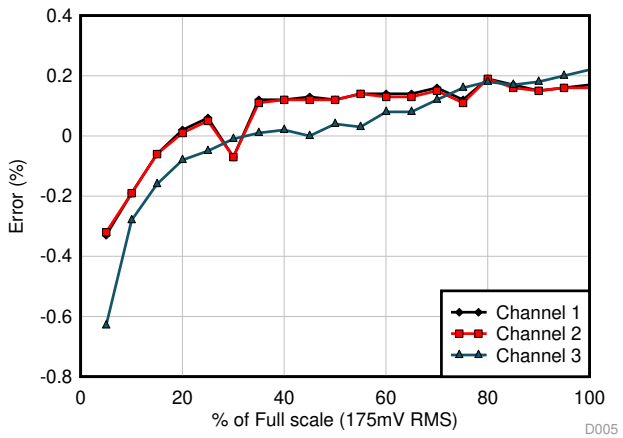


図 65. AC Voltage Accuracy

7.4 Repeatability of Measurement

表 30 through 表 31 provide information to measure repeatability accuracy for AC and DC Channels 2 through 3.

The following tables include the steps performed to check repeatability of the system (Repeat 1 and Repeat 2 data above):

- Power OFF = 30 seconds
- Power ON = 5 minutes
- Accuracy measured

表 30. Repeatability for DC Current Channel 2

INPUT AS % OF FULL SCALE (100% = 250 mV)	REFERENCE READING			READING 1			READING 2		
	APPLIED DC (mV)	Ch2 DC (mV)	Ch2 ERROR	APPLIED DC (mV)	Ch2 DC (mV)	Ch2 ERROR	APPLIED DC (mV)	Ch2 DC (mV)	Ch2 ERROR
5%	12.502	12.436	–0.14%	12.464	12.442	0.21%	12.464	12.412	–0.03%
10%	24.997	24.955	0.02%	24.966	24.942	0.09%	24.964	24.914	–0.01%
20%	50.003	49.964	0.02%	49.965	49.941	0.05%	49.966	49.931	0.03%
50%	124.943	124.926	0.02%	99.948	99.913	0.01%	124.948	124.911	0.01%
80%	199.945	199.949	0.03%	199.942	199.927	0.02%	199.942	199.925	0.02%
100%	249.958	249.986	0.03%	249.96	249.95	0.02%	249.96	249.926	0.01%
Offset	**–0.047945**								

The graph for current Channel 2 repeatability is shown in 図 66.

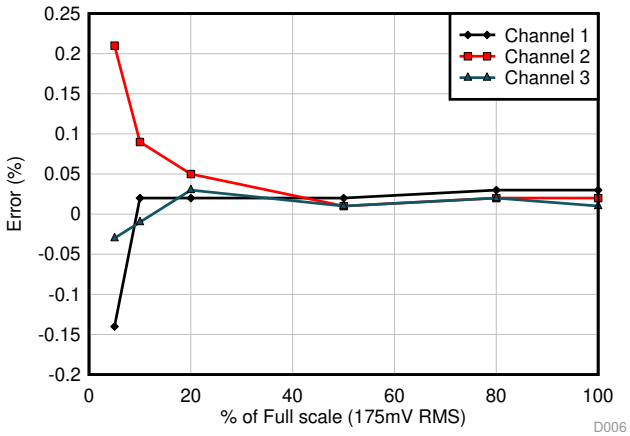


図 66. Repeatability for DC Current Channel 2

表 31. Repeatability for DC Current Channel 3

INPUT AS % OF FULL SCALE (100% = 250 mV)	REFERENCE READING			READING 1			READING 2		
	APPLIED DC (mV)	Ch3 DC (mV)	Ch3 ERROR	APPLIED DC (mV)	Ch3 DC (mV)	Ch3 ERROR	APPLIED DC (mV)	Ch3 DC (mV)	Ch3 ERROR
5%	12.502	12.38	–0.18%	12.464	12.385	0.16%	12.464	12.354	–0.09%
10%	24.997	24.897	0.00%	24.966	24.885	0.07%	24.964	24.854	–0.04%
20%	50.003	49.899	–0.01%	49.965	49.881	0.03%	49.966	49.862	–0.01%
50%	124.943	124.834	–0.01%	99.948	99.844	–0.01%	124.948	124.82	–0.02%
80%	199.945	199.827	–0.01%	199.942	199.842	0.00%	199.942	199.799	–0.02%
100%	249.958	249.845	–0.01%	249.96	249.857	0.00%	249.96	249.776	–0.03%
Offset	**–0.0991915**								

The graph for current Channel 3 repeatability is shown in 図 67.

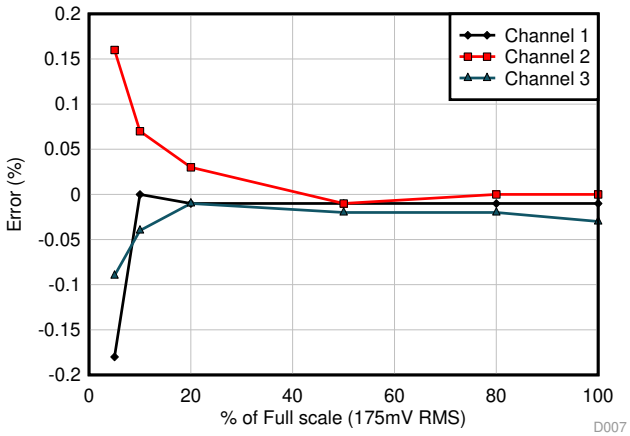


図 67. Repeatability for DC Current Channel 3

7.5 Accuracy Measurement With AC Input

表 32 through 表 34 provide accuracy measurement results for AC current inputs applied using an external current transformer to the ΔΣ modulator input. The following equipment is used:

- Variable AC current source
- High accuracy AC mV meter
- Input frequency is 50 Hz
- Averaging of samples done for 100 ms

表 32. AC Current Channel 1 Accuracy

INPUT AS % OF FULL SCALE (100% = 175 mV)		APPLIED (MEASURED AT THE ΔΣ MODULATOR INPUT) AC (mV)	MEASURED VALUES AC (mV)	ERROR (%)
10%		17.488	17.389	0.06%
23%		40.521	40.426	0.04%
34%		59.677	59.586	0.03%
43%		75.09	75.04	0.08%
58%		100.88	100.867	0.10%
80%		140.06	140.008	0.04%
100%		174.73	174.672	0.03%
120%		210.45	210.44	0.05%
140%		245.87	234.23	–4.69%
Offset	**–0.11**			

表 33. AC Current Channel 2 Accuracy

INPUT AS % OF FULL SCALE (100% = 175 mV)		APPLIED (MEASURED AT THE ΔΣ MODULATOR INPUT) AC (mV)	MEASURED VALUES AC (mV)	ERROR (%)
10%		17.509	17.472	–0.21%
23%		40.882	40.847	–0.09%
34%		60.344	60.342	0.00%
43%		74.844	74.801	–0.06%
57%		100.264	100.229	–0.06%
81%		142.03	142.087	0.04%
101%		176.13	176.194	0.04%
121%		211.08	211.028	–0.02%
141%		246.5	234.934	–4.69%
Offset	**0.0**			

表 34. AC Current Channel 3 Accuracy

INPUT AS % OF FULL SCALE (100% = 175 mV)		APPLIED (MEASURED AT THE ΔΣ MODULATOR INPUT) AC (mV)	MEASURED VALUES AC (mV)	ERROR (%)
10%		17.517	17.478	–0.22%
23%		40.791	40.755	–0.09%
35%		60.376	60.325	–0.08%
43%		74.844	74.789	–0.07%
57%		100.324	100.277	–0.07%
81%		142.49	142.431	–0.04%
101%		176.57	176.507	–0.04%
121%		211.28	211.138	–0.07%
141%		246.7	235.026	–4.73%
Offset	**0.0**			

図 68 shows the combined graph for AC current accuracy.

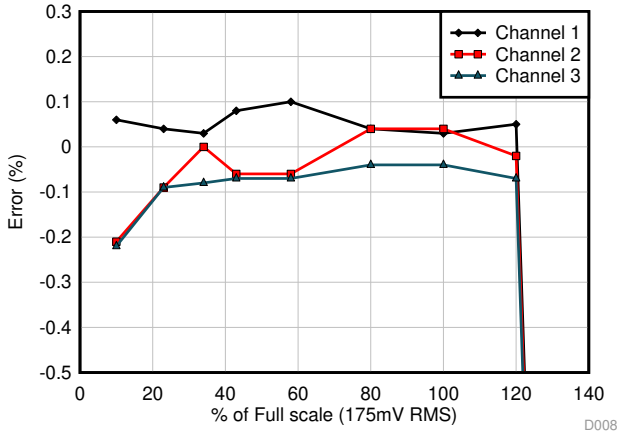


図 68. AC Current Accuracy

The recommended input is 175 mV_{RMS} for accuracy. The device is accurate up to 125% of the input with some linearity, above which the error is higher and nonlinear.

注: The range between the specified FSR (±250 mV) and the absolute FSR (±312.5 mV) is the nonlinear range of the modulator. The output of the modulator clips with a stream of only zeros with an input less than or equal to the minimum value of the absolute FSR value, or with a stream of only ones with an input greater than or equal to the positive value of the absolute FSR.

7.6 Accuracy with 50-mΩ Shunt Connected Externally

表 35 through 表 37 provide information to measure accuracy with 50-mΩ shunt.

表 35. AC Current Channel 1 Accuracy

INPUT AS % OF FULL SCALE (100% = 175 mV)		APPLIED (MEASURED ACROSS SHUNT) AC (mV)	MEASURED VALUES AC (mV)	ERROR (%)
5%		8.46	8.431	–0.05%
9%		15.552	15.54	0.08%
12%		20.902	20.89	0.06%
17%		30.146	30.131	0.03%
29%		51.354	51.334	0.01%
58%		101.170	101.139	–0.01%
87%		152.08	152.092	0.02%
102%		178.700	178.763	0.05%
114%		199.710	199.726	0.02%
Offset	**–0.025**			

表 36. AC Current Channel 2 Accuracy

INPUT AS % OF FULL SCALE (100% = 175 mV)		APPLIED (MEASURED ACROSS SHUNT) AC (mV)	MEASURED VALUES AC (mV)	ERROR (%)
5%		8.421	8.396	0.00%
9%		15.043	15.016	–0.01%
11%		19.966	19.958	0.08%
17%		30.073	30.050	0.01%
30%		52.463	52.458	0.04%
57%		99.236	99.239	0.03%
87%		151.720	151.723	0.02%
101%		176.180	176.335	0.10%
112%		196.610	196.632	0.02%
Offset	**–0.025**			

表 37. AC Current Channel 3 Accuracy

INPUT AS % OF FULL SCALE (100% = 175 mV)		APPLIED (MEASURED ACROSS SHUNT) AC (mV)	MEASURED VALUES AC (mV)	ERROR (%)
5%		9.244	9.225	0.01%
8%		14.805	14.786	0.00%
11%		19.591	19.574	0.02%
17%		29.619	29.604	0.02%
29%		50.097	50.068	–0.02%
57%		99.546	99.463	–0.06%
86%		151.230	151.147	–0.04%
104%		182.710	182.721	0.02%
112%		196.070	196.050	0.00%
Offset	**–0.02**			

図 69 shows the combined graph for AC current accuracy with a 50-mΩ shunt.

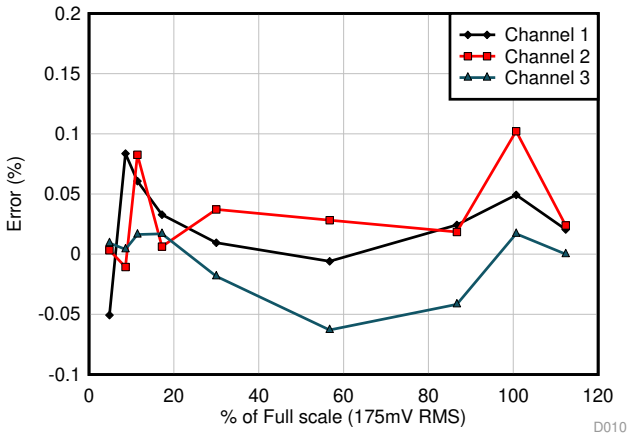


図 69. AC Current Accuracy with 50-mΩ Shunt

7.7 Accuracy with 5-mΩ Shunt Connected Externally

表 38 through 表 40 provide information to measure accuracy with a 5-mΩ shunt.

表 38. AC Current Channel 1 Accuracy

INPUT AS % OF FULL SCALE (100% = 175 mV)		APPLIED (MEASURED ACROSS SHUNT) AC (mV)	MEASURED VALUES AC (mV)	ERROR (%)
5%		8.384	8.359	0.00%
9%		15.516	15.488	–0.02%
14%		25.006	24.997	0.06%
30%		51.379	51.353	0.08%
52%		90.362	90.350	0.01%
65%		116.520	116.405	–0.08%
Offset	**–0.025**			

表 39. AC Current Channel 2 Accuracy

INPUT AS % OF FULL SCALE (100% = 175 mV)		APPLIED (MEASURED ACROSS SHUNT) AC (mV)	MEASURED VALUES AC (mV)	ERROR (%)
5%		8.190	8.156	–0.11%
9%		15.160	15.146	0.07%
14%		25.175	25.166	0.06%
30%		52.889	52.880	0.03%
52%		89.562	89.548	0.01%
65%		115.975	115.963	0.01%
Offset	**–0.025**			

表 40. AC Current Channel 3 Accuracy

INPUT AS % OF FULL SCALE (100% = 175 mV)		APPLIED (MEASURED ACROSS SHUNT) AC (mV)	MEASURED VALUES AC (mV)	ERROR (%)
5%		8.752	8.728	0.02%
9%		15.127	15.118	0.11%
14%		24.673	24.662	0.06%
30%		52.502	52.496	0.04%
52%		90.538	90.435	–0.09%
65%		113.690	113.614	–0.04%
Offset	**–0.025**			

図 70 shows the combined graph for AC current accuracy with a 5-mΩ shunt.

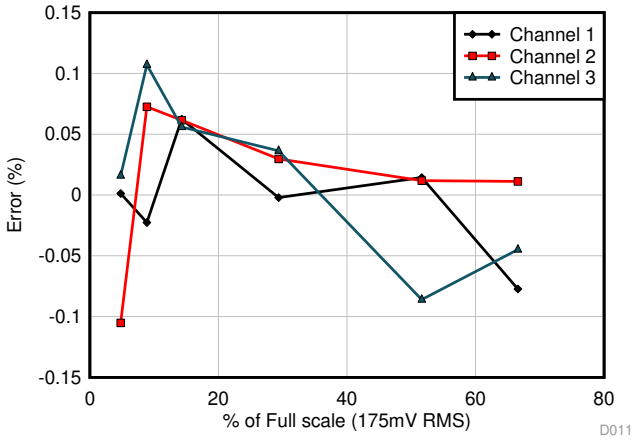


図 70. AC Current Accuracy with 5-mΩ Shunt

7.8 Isolated DC/DC Converter Testing

This section provides details of the function tests performed on the UCC12050.

表 41. Supply Output With Different SEL (VISO Selection)

EN	SEL	ISOLATED SUPPLY OUTPUT VOLTAGE (VISO) SET POINT	LOAD CURRENT	INPUT CURRENT	MEASURED VOLTAGE
HIGH	Shorted to VISO	5.0 V	100	173	4.98
HIGH	Shorted to VISO	5.0 V	150	281	3.71
HIGH	100 kΩ to VISO	5.4 V	100	206	5.37
HIGH	100 kΩ to VISO	5.4 V	10	55	5.37
HIGH	100 kΩ to VISO	5.4 V	5	49	5.37
HIGH	Shorted to GNDS	3.3 V	100	152	3.28
HIGH	100 kΩ to GNDS	3.7 V	100	149	3.67
HIGH	OPEN	UNSUPPORTED			
LOW	X	0 V		0	0

7.9 Performance testing for AMC1311, AMC1336 and AMC1306M25 based modules

The functional and performance testing for devices with lesser pin count and wider input voltage have been tested by wiring the devices externally. The performance is similar to AMC1304M25. The devices are functionally compatible to AMC1304M25 n terms of filtering and digital interface. The design files are available for customer to build and test with the above devices.

8 Power Supply Waveforms

Power supply waveforms are shown in the following illustrations.

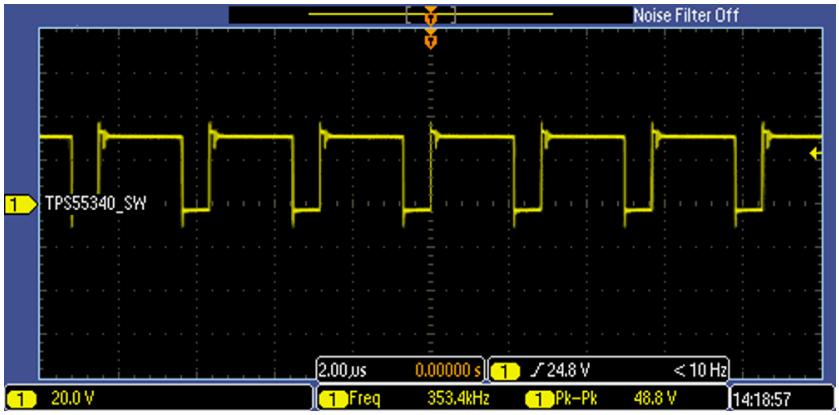


図 71. Switching Node Waveform for TPS5534 24- to 6-V DC-DC Converter on FMB

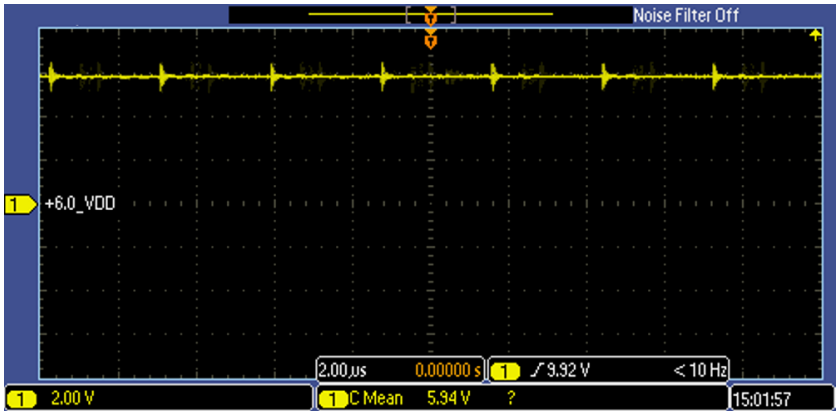


図 72. +6.0_VDD FMB

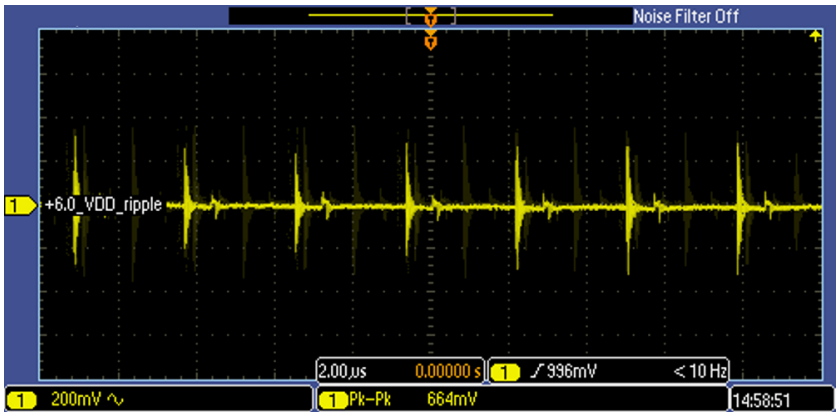


図 73. Ripple on +6.0_VDD FMB

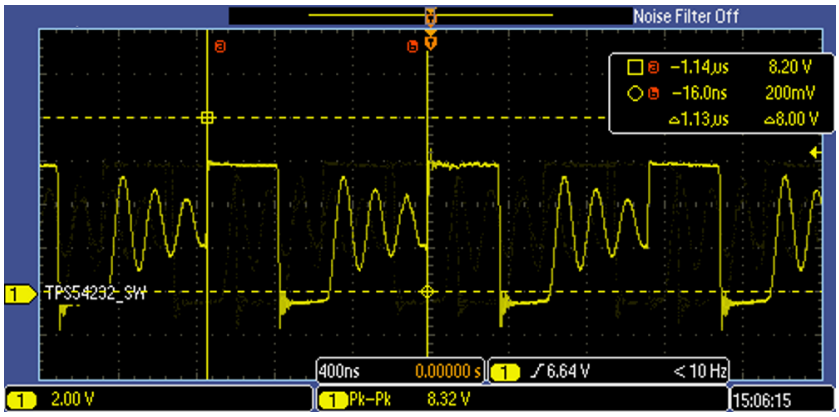


図 74. Switching Node Waveform for TPS54232, 6- to 3.3-V DC-DC Converter on FMB

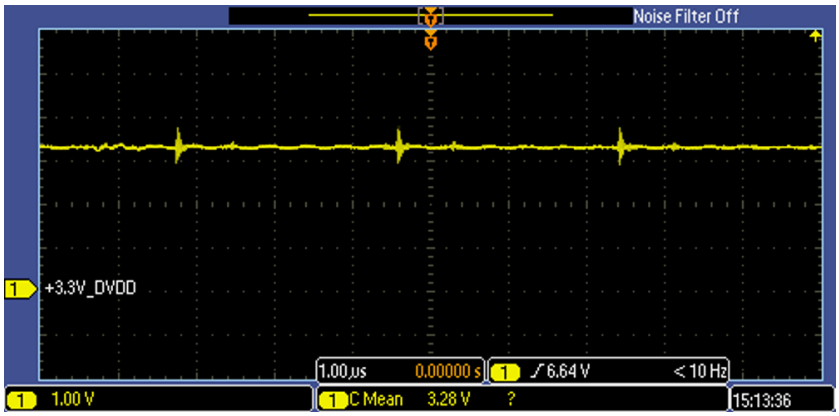


図 75. 3.3V_DVDD on FMB

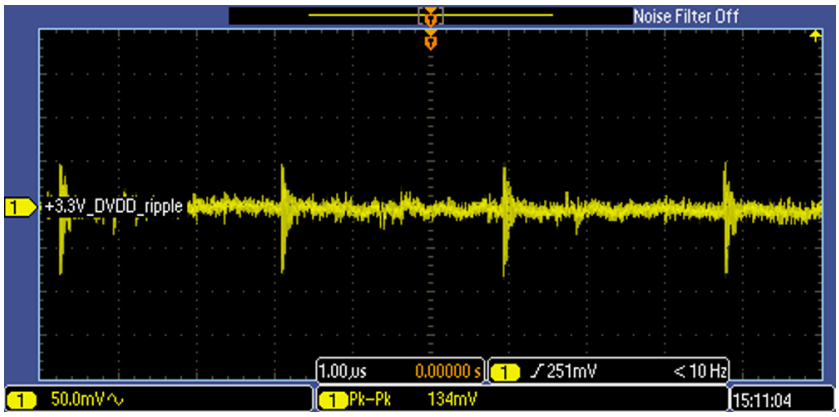


図 76. 3.3V_DVDD on FMB

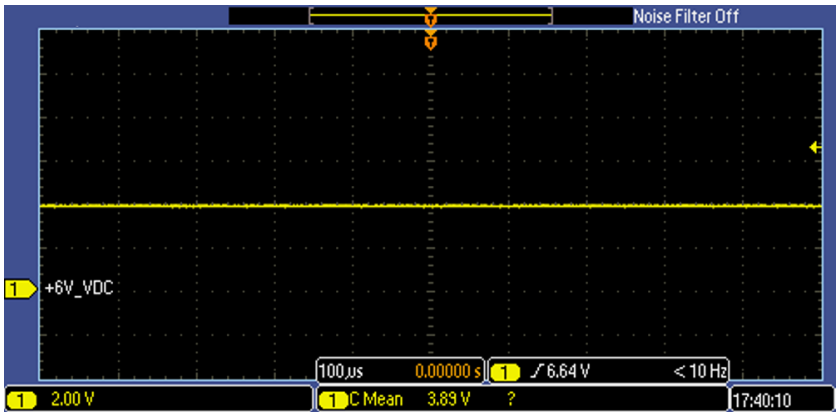


図 77. +6V_V DC on ICVM Board, Measured Across Net +6V_V DC wrt GND_V DC

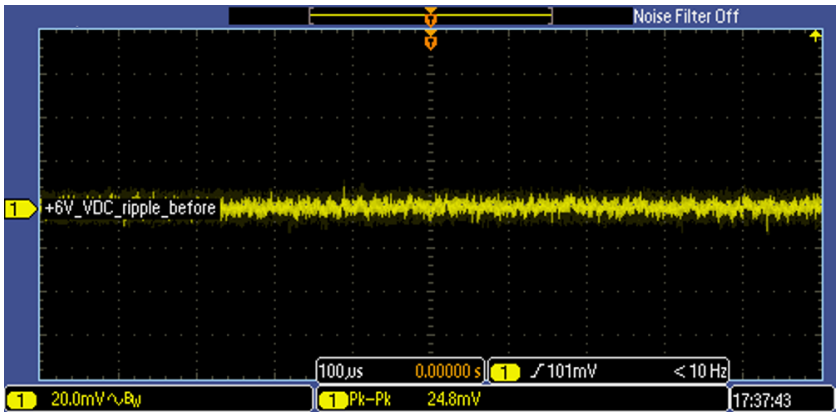


図 78. Ripple on +6V_V DC on ICVM Board, Measured Across Net +6V_V DC wrt GND_V DC, With Load Turned Off

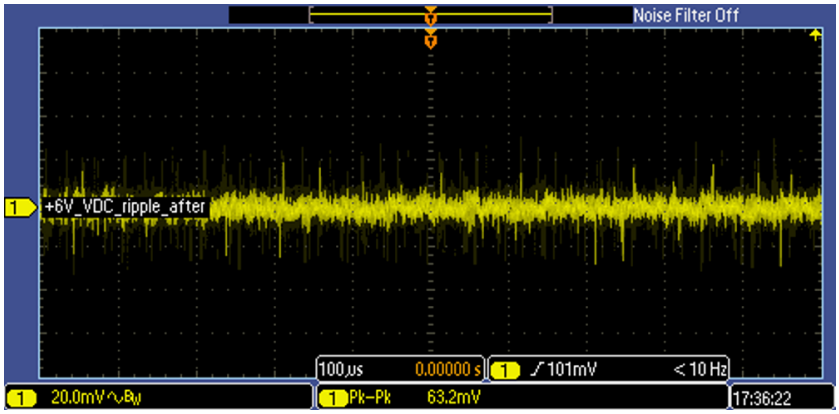


図 79. Ripple on +6V_V DC on ICVM Board, Measured Across Net +6V_V DC wrt GND_V DC, With Load Turned On

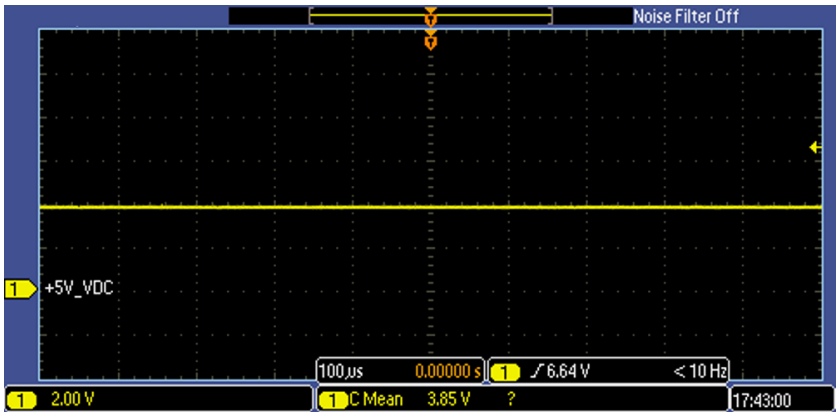


図 80. +5.0V_V DC Power Rail on ICVM Board, Measured Across Net +5.0V_V DC wrt GND_V DC

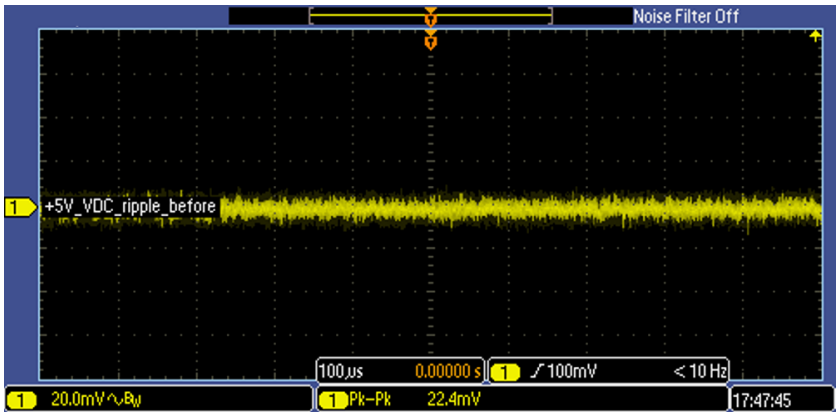


図 81. Ripple on +5.0V_V DC on ICVM Board, Measured Across Net +5.0V_V DC wrt GND_V DC, With Load Turned Off

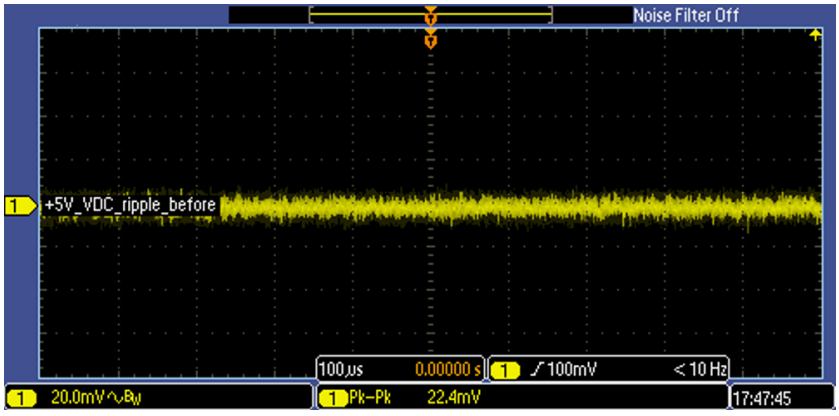


図 82. Ripple on +5.0V_V DC Power Rail on ICVM Board, Measured Across Net +5.0V_V DC wrt GND_V DC, With Load Turned On

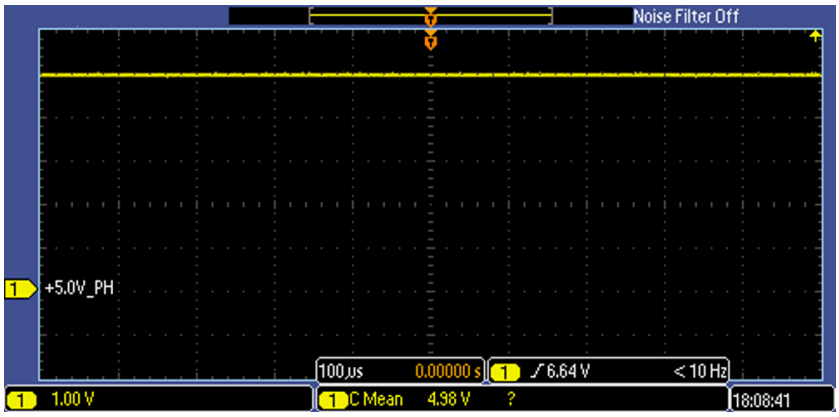


図 83. +5.0V_PH Power Rail on ICVM Board, Measured Across Net +5.0V_PH wrt GND_PH, With Load Turned On

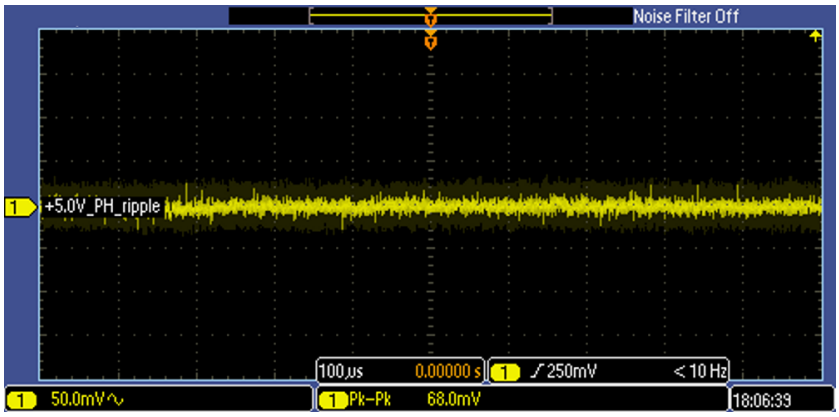


図 84. Ripple on +5.0V_PH Power Rail on ICVM Board, Measured Across Net +5.0V_PH wrt GND_PH, With Load Turned On

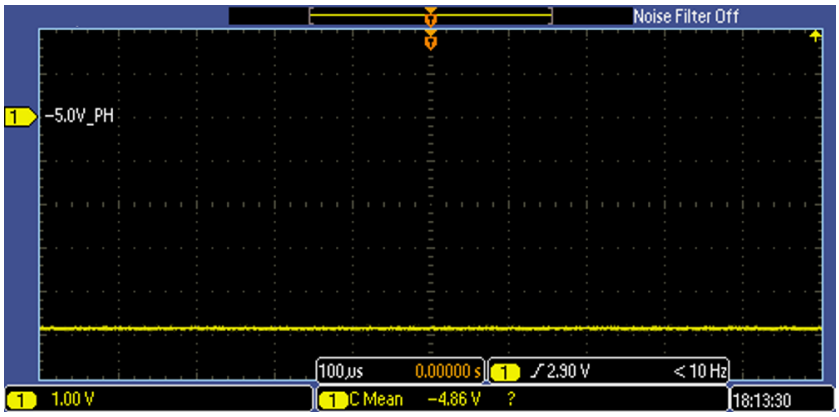


図 85. –5.0V_PH on ICVM Board, Measured Across Net –5.0V_PH wrt GND_PH, With Load Turned On

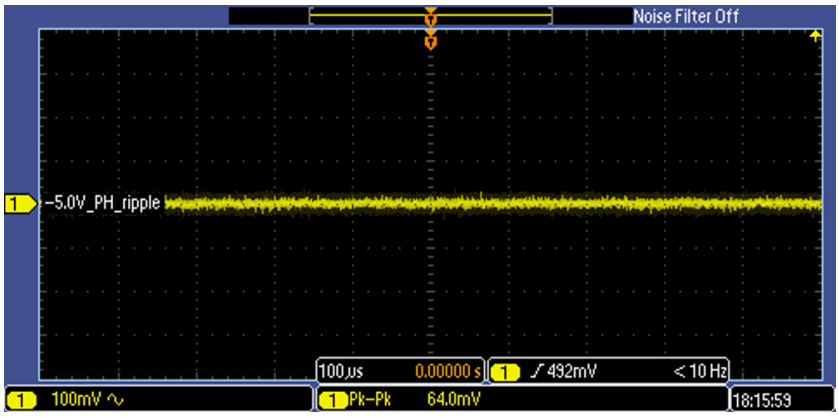


図 86. Ripple on –5.0V_PH on ICVM Board, Measured Across Net –5.0V_PH wrt GND_PH, With Load Turned On

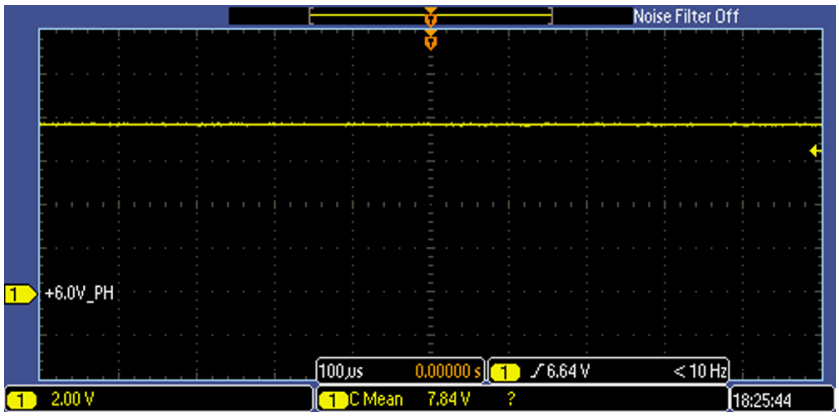


図 87. +6.0V_PH Power Rail on ICVM Board, Measured Across Net +6V_PH wrt GND_PH, With Load Turned On

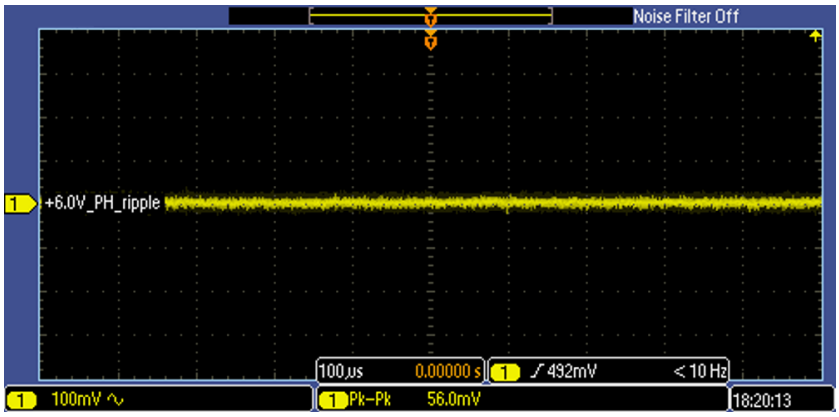


図 88. Ripple on +6.0V_PH on ICVM Board, Measured Across Net +6V_PH wrt GND_PH, With Load Turned On

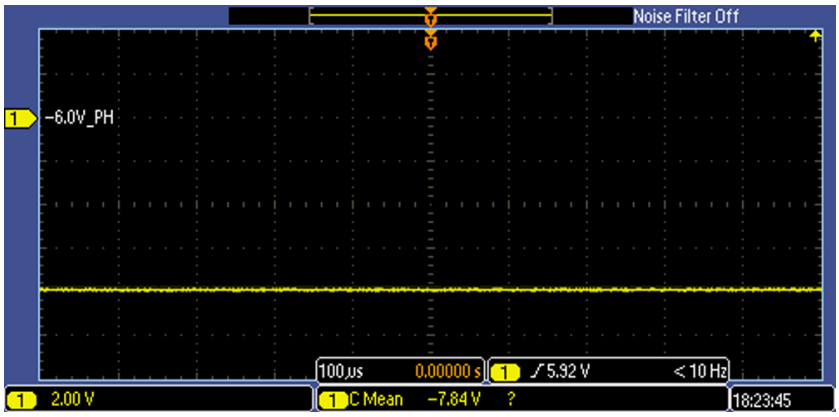


図 89. –6.0V_PH on ICVM Board, Measured Across Net –6V_PH wrt GND_PH, With Load Turned On

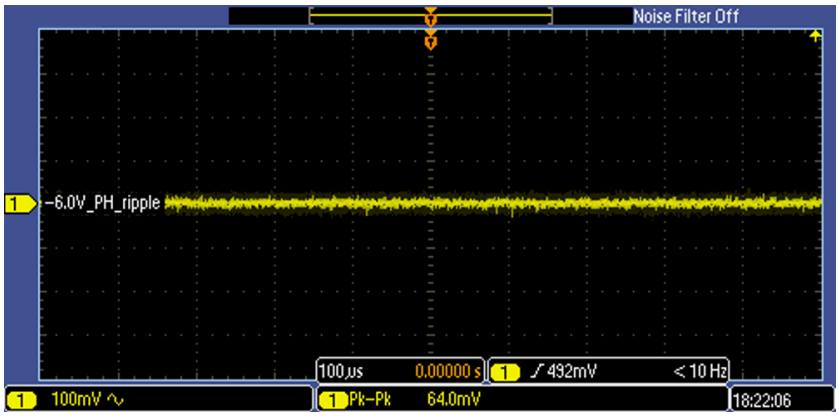


図 90. Ripple –6.0V_PH on IVCM Board, Measured Across Net –6V_PH wrt GND_PH, With Load Turned On

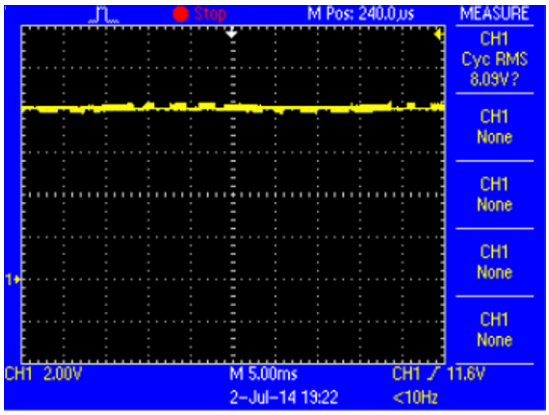


図 91. +6V_USH on ICVM Board, Measured Across Net +6V_USH wrt GND_USH, With Load Turned On

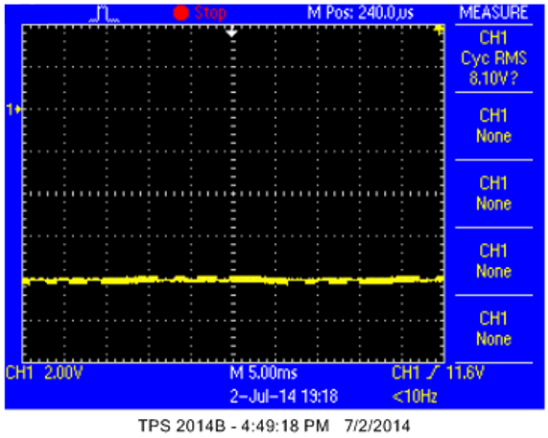


図 92. –6V_USH on ICVM Board, Measured Across –6V_USH wrt GND_USH, With Load Turned On

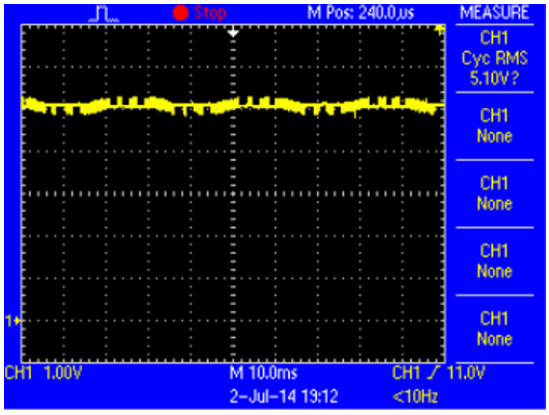


図 93. +5.0V_USH on ICVM Board, Measured Across +5V_USH wrt GND_USH, With Load Turned On

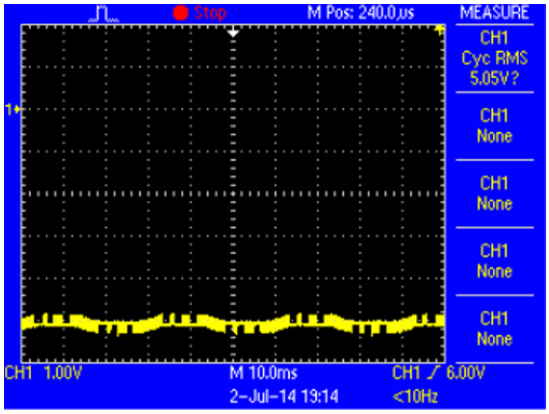


図 94. –5.0V_USH on ICVM Board, Measured Across –5V_USH wrt GND_USH, With Load Turned On

8.1 AMC1304M25 Clock and Data Graphs

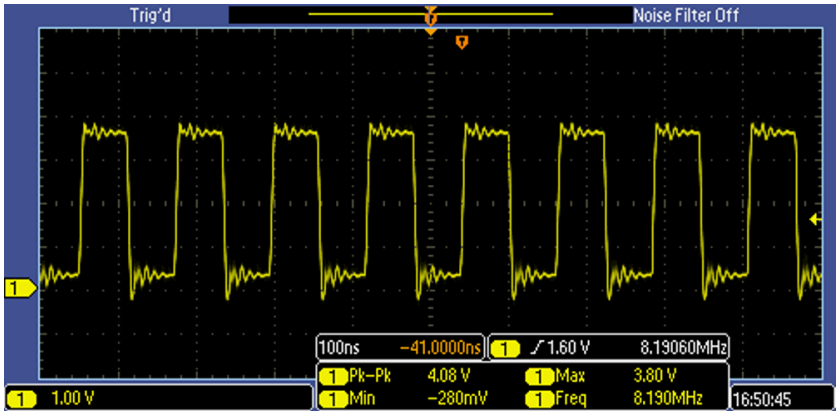


図 95. Input Clock to AMC1304M25

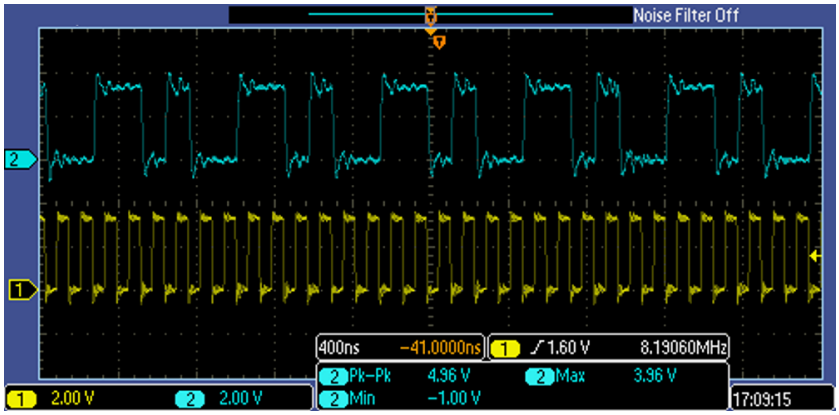


図 96. Data Out of AMC1304M25 (Blue) and Input Clock (Yellow)

9 Design Files (ICVM Board)

9.1 Schematics

To download the schematics, see the design files at TIDA-00080.

9.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00080.

9.3 Layer Plots

To download the layer plots, see the design files at TIDA-00080.

9.4 Altium Project

To download the Altium project files, see the design files at TIDA-00080.

9.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00080.

9.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00080.

10 Design Files (FMB)

10.1 Schematics

To download the schematics, see the design files at TIDA-00080.

10.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00080.

10.3 Layer Plots

To download the layer plots, see the design files at TIDA-00080.

10.4 Altium Project

To download the Altium project files, see the design files at TIDA-00080.

10.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00080.

10.6 Assembly Drawings

To download the assembly files, see the design files at TIDA-00080.

11 Software Files

To download the software files, see the design files at TIDA-00080.

12 Related Documentation

1. *UCC12050 500-mW, High-Efficiency, Low-Emissions, 5-kVRMS Isolated DC-DC Converter*, Data Sheet (SPRS880)
2. *TMS320F2837xD Dual-Core Delfino Microcontrollers*, TMS320F2837xD Data Sheet (SNVSB38A)
3. *16-Bit, Quad Channel, Ultra-Low Glitch, Voltage Output DIGITAL-TO-ANALOG CONVERTER with 2.5V, 2ppm/°C Internal Reference*, DAC8564 Data Sheet (SBAS403)
4. *Practical Applications in Digital Signal Processing* by Richard Newbold, Prentice Hall (Book)
5. *AMC1304 Family of 20-MHz, Isolated Delta-Sigma Modulators for Shunt-Based Current Measurement*, AMC1304 Data Sheet (SBAS655)
6. *AMC1305x High-Precision, Reinforced Isolated Delta-Sigma Modulators*, AMC1305 Data Sheet (SBAS654A)
7. *TMS320F2837xD Delfino Microcontrollers*, TMS320F2837xD Technical Reference Manual (SPRUHM8A)

12.1 商標

13 About the Author

PRAHLAD SUPEDA is a systems engineer at Texas Instruments India where he is responsible for developing reference design solutions for Smart Grid within industrial systems. Prahlad brings to this role his extensive experience in power electronics, EMC, analog, and mixed signal designs. Prahlad earned his bachelor of instrumentation and control engineering from Gujarat University, India. He can be reached at prahlad@ti.com.

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改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (March 2015) から **Revision B** に変更 **Page**

- ドキュメントのタイトルを 変更 1
- 「概要」を 変更 1
- デザインの「リソース」を 変更 1
- デザインの「特長」を 変更 1
- information in *Design Requirements* table 変更 13
- *Board Layout* image 削除 14
- section title from *ICVM* to *Isolated Voltage and Current Measurement Using the AMC1304M25* 変更 15
- *Isolated AC Voltage Measurement Using the AMC1336* section 追加 16
- *Isolated AC Current Measurement Using the AMC1306M25* section 追加 18
- *Isolated DC Voltage Measurement Using the AMC1311* section 追加 19
- *Delfino FMB* image 削除 20
- information regarding the AMC1306 追加 26
- information regarding the UCC12050 追加 31
- *Isolated DC/DC Converter Testing* secion 追加 83

2014年9月 発行のものから更新 **Page**

- 設計リソースCDCE906からTMS320F28377Dまで 追加 1
- ICVM設計機能の精度性能値を< 1%から 変更 1
- FMBデザインにF2837xを接続するオプションを 追加 1
- FMB設計機能からLabVIEWベースのGUIおよびCSVフォーマット保存の箇条書き項目を 削除 1
- 「シャント・ベース」 削除 1
- ブロック図とボード画像 変更 1
- Current measurement accuracy and Voltage measurement accuracy from < 1% 変更 13
- Input frequency from 45 to 65 Hz 変更 13
- board explanations after 図 11 追加 14
- 4.1: moved Sections 4.1 to 4.6 from original under the new 4.1 変更 24
- note for 図 31: 16-Bit DAC Output 追加 38
- from AMC13xx 変更 45
- the order of subsections: System Layout Page, Calibration Page, and Graph Page now fall under 6.4: IVIM Pages 変更 57
- title of 表 14 変更 67
- Design Files for the FMB 追加 94
- References 3 through 6 追加 95

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