User's Guide
SLUU260–September 2006

bq24038 (bqTINY™-III) 1.5-A Single-Chip Li-Ion and Li-Pol Charge Management IC EVM

This user's guide describes the bq24038 (bqTiny-III) Evaluation Module. The EVM provides a convenient method for evaluating the performance of a charge management and system power solution for portable applications. A completly designed and tested module is presented. The charger is designed to deliver up to 1.5 A of continuous current to the system or charger for one-cell Li-ion or Li-polymer applications using a dc power supply. The charger is programmed from the factory to deliver 1 A of charging current with a selectable 4.2- or 4.36-VDC BAT regulation output..

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1 Introduction

CAUTION

This bq24038 EVM is designed to charge a single-cell, 4.4-VDC-rated $LiMn_2O_4$ battery. A typical 4.2-VDC, single-cell LiIon battery is potentially a fire hazard if charged to the 4.4-VDC regulation (VBSEL = high) threshold. If using a 4.2-VDC-rated cell, ensure the VBSEL, JMP7 shunt is removed (VSEL = low → 4.2-V BAT regulation).

The bqTiny-III powers the system while independently charging the battery. This feature reduces the charge and discharge cycles on the battery, allows for proper charge termination, and allows the system to run with an absent or defective battery pack. This feature also allows for the system to instantaneously turn on from an external power source even when using a deeply discharged battery pack.

The bqTiny-III automatically selects the USB port or the ac adapter as the power source for the system. In the USB configuration, the host can select from the two preset input maximum rates of 100 mA and 500 mA. The bqTiny-III dynamically adjusts the USB charge rate based on the system load to stay within the 100-mA or 500-mA maximum rates. The AC pin can be programmed to perform like a USB input by pulling the PSEL pin low. An external resistor, RSET1, sets the magnitude of the charge current. If the charge current exceeds the available input current, the voltage on the OUT pin drops to the $DPPM_{OUT}$ threshold or the battery voltage, which ever is higher. The charging current is reduced to what current is available ($I_{BAT} = I_{IN} - I_{OUT}$).

The bqTiny-III charges the battery in three phases: conditioning, constant current, and constant voltage. Charge is terminated based on minimum current. A resistor-programmable charge timer provides a backup safety for charge termination. The bqTiny-III automatically re-starts the charge if the battery voltage falls below an internal threshold. The bqTiny-III automatically enters sleep mode when both supplies are removed (a drop to the battery voltage).

2 Considerations When Testing and Using bq24038 IC

Consider the following noteworthy items while testing and using the bq24038 IC.

The bq24038 has a LDO 4.4-V regulator connected to the OUT pin.

The three potential sources to power the system ($\mathbf{V}_{OUT}$) are: ac (ac-to-dc adapter), USB port, and battery. The IC is designed to power the system continuously. The battery, in most cases, is the last line of backup. If the ac or USB inputs are not available (or disabled), the battery connects to the system.

In the thermal regulation condition (T_J = 125°C—not a first-choice design mode of operation), the charge current is reduced to the battery, and the system still gets its power from the input. The battery supplement is still available in thermal regulation if the $\mathbf{V}_{OUT}$ falls to $\mathbf{V}_{BAT}$. In thermal cutoff (~155°C), the input sources are disconnected, but the internal battery FET connects the battery to $\mathbf{V}_{OUT}$.

There are two types of OUT-pin short circuit, one associated with the input IN pin (V_{OUT} < 1 V) and the other associated with the BAT pin ($V_{BAT} - V_{OUT}$ > 200 mV). For the OUT short-circuit case where the OUT pin is less than 1 V, the AC and USB input FETs are disabled. The recovery method is implemented by an internal 500-Ω pullup resistor from IN to OUT. The system load must be reduced (>200 Ω) such that the pullup can pull V_{OUT} above 1 V, and thus enable the selected input FET. For the BAT short circuit, the battery FET opens if a short on V_{OUT} pulls more than ~4 A of current (>200-mV drop across the BAT FET) from the battery. The recovery method is from a 10-mA current source between the BAT and OUT pins, so the short and any system load must be removed before the OUT pin can recover within 200 mV of V_{BAT}. Note that the current source is ~10 mA with the OUT pin near 0 V, but falls off to ~2 mA as the OUT pin goes above 1 V.

When there is no power to the system and the battery is hot-plugged, the BAT-pin voltage leads the OUT-pin voltage due to the system capacitance, and the output may go into BAT short-circuit mode. To avoid this, a feature was added to the DPPM pin. If the voltage on the DPPM pin is held below 1 V, then the short-circuit feature is disabled. Therefore, placing a small capacitor (~1 nF to 10 nF) across the DPPM resistor delays the battery short-circuit protection for several microseconds after hot-plugging a battery pack.

Another feature that protects system integrity is dynamic power path management (DPPM). The voltage on the DPPM pin ($DPPM_{IN}$) times a scaling factor of ~1.15 is the $DPPM_{OUT}$ voltage. The $DPPM_{OUT}$ voltage is the critical voltage, determined by the designer, where battery charging current is reduced to keep the system voltage ($\mathbf{V}_{OUT}$) from further decay. A special feature to keep in mind is that, when in DPPM mode, the internal oscillator timer is slowed proportionally to how much the programmed charger current is reduced. This allows the timers (safety and others) to be appropriately adjusted during operation. Therefore, when performing any test where time is measured, keep in mind this adjustment factor.

Another critical feature is power handoff. The power handoff is initiated autonomously or by request. The automatic handoff typically occurs because AC or USB is lost. If AC is selected as the primary source and the adaptor is removed, the IC automatically switches to USB power if present (USBPG = low) or to battery power if not. The transition occurs after the lost source is considered *no good*, which is when the selected input drops down to within 80 mV of the battery voltage. If the battery is fully depleted, this may cause the system to reset (Note that prior to losing power, the battery would most likely not be depleted). The reverse scenario is also true: if USB is the selected primary source and is removed, the AC would be selected if present, followed by the battery.

The input source to the system (OUT pin) can be chosen, by request, via the PSEL input pin. A high PSEL setting programs AC as the priority input, whereas a low defines the USB as the primary source. The transition occurs immediately when switched via the PSEL pin.

If the CE input pin goes low, the AC and USB inputs are disabled and the BAT pin becomes the source. There is a 5-ms delay before disabling the AC and USB inputs to allow the external process to reset and not cycle the input power.

3 Performance Specification Summary

Table 1 summarizes the performance specifications of the EVM.

Table 1. Performance Specification Summary for bq24038 EVMs

SPECIFICATION	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input dc voltage, $V_{I(AC)}$		4.8 V	5	6.5	V
Input dc USB voltage, $V_{I(USB)}$			5		V
Battery charge current, $I_{O(CHG)}$			1	2+	A
Power dissipation, bq24038 IC, 1 cell	$P_{diss} = (V_{IN} – V_{OUT})I_{OUT} + (V_{IN} – V_{BAT})I_{BAT} + (V_{IN} – V_{LDO})I_{LDO}$			See [1]	W

(1) The HPA138 (bq24038) thermal design is optimized (8^+ vias, 0.031-inch PWB, 2-oz. copper) to give $R_{\theta JA}$ ~27°C/W.

4 Test Summary

This section covers the setup and tests performed in evaluating the EVM.

4.1 Equipment

- Power supply (5.25 ± 0.25 VDC), current limit set to 2 A ± 0.2 A for ac input to the UUT
- USB high-power port (500 mA) and cable (J1 is an alternate USB connection)
- Three Fluke 75 DMMs (equivalent or better)
- Oscilloscope, Model TDS220 (equivalent or better)

4.2 Equipment Setup

- Preset the UUT power supply voltage and current prior to connection to UUT; turn off the power supply and connect the supply to J2-AC/GND (+ to AC and – to GND).
- Connect a 10-Ω load to J7-OUT/GND.
- Connect a 1k-Ω load to J5-LDO/GND.
- Connect a fully discharged (< 2.8-VDC) single-cell Li-ion or Li-polymer battery to J8-BAT+/BAT–.
- Connect the DMMs as shown in Figure 1.
- Wait to connect the USB cable until requested to do so.

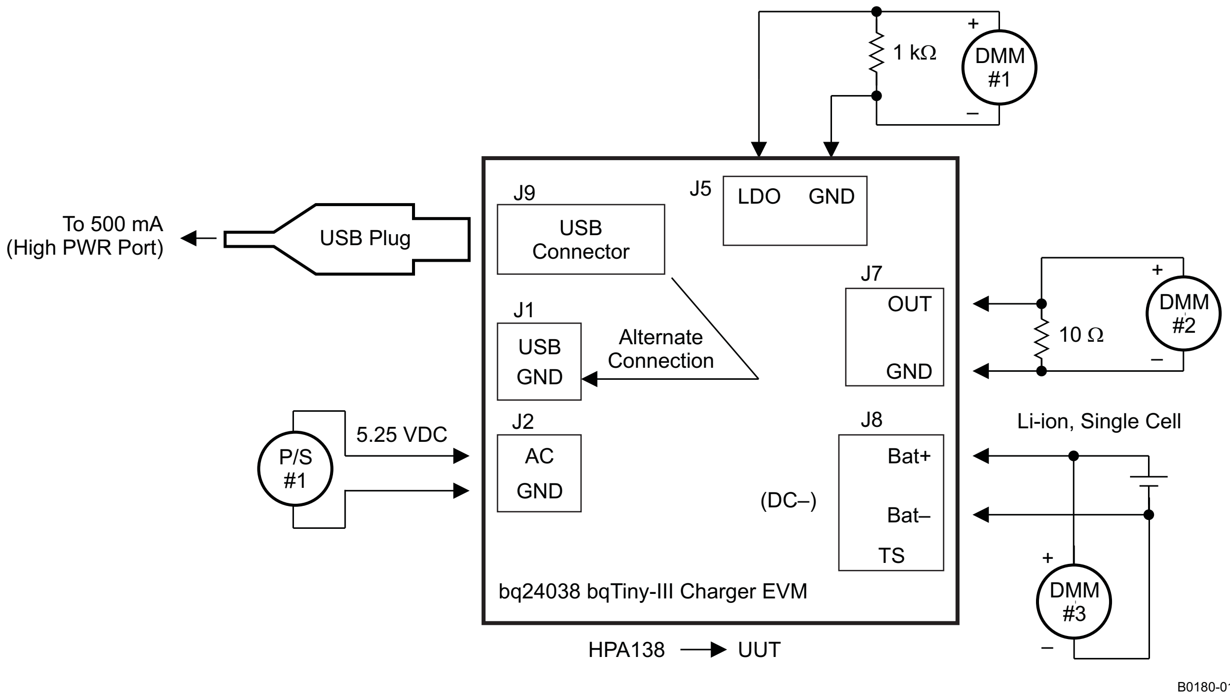

Figure 1. Test Diagram

4.3 Test Procedure

1. Verify that the equipment is set up according to *Equipment Setup,* Section 4.2.
2. Set jumpers on the UUT as follows: JMP1-0.5; JMP2-AC; JMP3-EN; set JMP4 through JMP6 to LED.
3. Remove shunt from JMP7.
4. Adjust **R_DPPM** until TP1 is **35.7 kΩ ± 0.1 k**Ω with respect to GND, and adjust **R_TMR** until TP2 is 50 kΩ with respect to GND.
5. Verify that $\mathbf{V}_{OUT}$ is approximately equal to $\mathbf{V}_{BAT}$ (if Vout < 1.1 V, the output is in short-circuit mode. To get out of this mode, momentarily disconnect the 10-Ω load, or touch a 10-Ω pullup resistor between the battery and the output).
6. Power up the **5.25-VDC supply** to the UUT.
7. Verify $\mathbf{V}_{BAT}$ is between 2.4 VDC and 3 VDC, and the charger is in pre-charge state: LEDs STAT1 (D2), STAT2 (D3), and PG (D5) are on.
   If V_{BAT} is above the low-voltage threshold ($V_{(LOWV)}$ ~3 V), then the IC is in fast-charge mode {STAT2 (D3) is off (High)}. If the IC is in fast charge, skip to Step 11.
8. Verify $\mathbf{I}_{BAT}$ is ~0.1 A ($\mathbf{I}_{BAT}$~ = I_{AC}– (V_{OUT} / R_{OUT}) –0.01 A).
9. Verify $\mathbf{V}_{OUT}$ is between 4.3 VDC and 4.5 VDC.
10. Verify $\mathbf{V}_{LDO}$ is between 3.2 VDC and 3.4 VDC.
11. Allow the battery to charge until $\mathbf{V}_{BAT}$ is between 3.2 VDC and 4 VDC. The charger should deliver the programmed constant current to the battery unless the input cannot source the required current.
12. Verify **D3** (STAT2) has turned off.

13. Verify $\mathbf{I_{BAT}}$ is ~1 A (for a 10-kΩ resistor on *ISET1*, I_{BAT}~ = I_{AC} – (V_{OUT} / R_{OUT}) – 0.01 A).
14. Verify $\mathbf{I_{AC}}$ is ~1.5 A (for 10-Ω **OUT** load and 10 kΩ on **ISET1**).
15. Apply a short between J3-4 (CE) and J3-3 (GND) on the UUT. This overrides the JMP3 100-kΩ pullup, disables the charging, puts the IC in low power mode and connects the battery to the OUT pin. Note that if CE is floated (JMP3 is removed and J3-4 connection is removed) the IC may bounce between the charging and disabled states. Verify on the scope that $\mathbf{V_{OUT}}$ does not drop out. Note that the transition between power sources is implemented by break-before-make switching and requires the capacitance on $\mathbf{V_{OUT}}$ to be able to hold up the system voltage for at least 50 µs.
16. Verify **D2** (STAT1) has turned off.
17. Verify $\mathbf{I_{AC}}$ drops below 10 mA (should be < 200 µA into the IC if PG LED (current) JMP6 is removed).
18. Verify $\mathbf{V_{OUT}}$ is within –50 mV of $\mathbf{V_{BAT}}$.
19. Remove short betwen J3-4 and J3-3 on UUT. Verify on the scope that $\mathbf{V_{OUT}}$ does not drop out. Verify **D2** (STAT1) has turned on, charging has resumed and $\mathbf{V_{OUT}}$ is powered from the input.
20. Disconnect the **5.25-VDC input supply** from the UUT ac input. Verify on the scope that $\mathbf{V_{OUT}}$ does not drop out. Verify $\mathbf{V_{OUT}}$ is within –50 mV of $\mathbf{V_{BAT}}$ and **D2** (STAT1) and **D5** (PG) LEDs turn off. This demonstrates battery power backup for loss of ac adapter.
21. Reapply the 5.25-VDC supply to the UUT ac input. Verify on the scope that $\mathbf{V_{OUT}}$ does not drop out. Verify **D2** (STAT1) and **D5** (PG) LEDs turn on.
22. Adjust R15 until the voltage on TP1 is ~3.5 VDC ($\mathbf{V_{BAT}}$ should be less than 3.9 V for this demonstration; otherwise, discharge battery).
23. Reduce the current limit on the input supply to ~1 A (going to AC pin on UUT) and verify on the scope that $\mathbf{V_{OUT}}$ has dropped to the VDPPM level of ~4 V {(3.5 V at TP1) × 1.15 = 4 V}. Note that the current into the battery is ~600 mA (1-A input minus 400 mA to the system), which has been reduced to keep the output from falling below the programmed DPPM OUTPUT threshold of 4 V. This demonstrates DPPM operation (charging current to the battery is reduced if output drops to the DPPM OUTPUT voltage threshold attempting to keep the output voltage from dropping further).
24. Further reduce the input current limit to 250 mA. Verify on the scope that $\mathbf{V_{OUT}}$ does not drop out. Verify that $\mathbf{V_{OUT}}$ drops just below $\mathbf{V_{BAT}}$ (< 50 mV). Because the available input current is less than the system **OUT** load, reducing the battery charging current to zero is still not enough reduction in load to keep the output from dropping. Once the output drops below ~60 mV, the internal battery FET turns on and allows the battery to source the OUT pin system load. This demonstrates battery supplement mode.
25. Return the current limit of the 5.25-V supply to ~2 A. Verify $\mathbf{V_{OUT}}$ returns to Vreg.
26. Set JMP2 (PSEL) to USB (PSEL = low). Verify that the input current (AC) drops to between 400 mA and 500 mA. The programmed charge current of ~1 A and the system load of 10 Ω exceeds the USB 0.5-A limit; therefore,$\mathbf{V_{OUT}}$ drops until the DPPM OUTPUT voltage threshold, or battery voltage, is reached (which ever is higher). If the DPPM OUTPUT threshold is larger, the charging current is reduced to keep the output voltage from dropping further. If the battery voltage is higher, the battery supplements the current to keep the output from dropping too much (50 mV to 200 mV) below the battery voltage. Note that setting PSEL to low (USB mode; PSEL high is ac mode) selects the USB input as the primary source. If the USB source is not present, and the ac source is present, the IC uses the ac input source as if it were a USB input. This feature is useful if only one input power connector is desired, and two sources (USB and ac adaptor) are available. A *keyed* cable or a u-controller would set the PSEL pin for the available source. Note that the system would ideally go to a lower power mode prior to selecting USB operation to avoid pulling down $\mathbf{V_{OUT}}$.
27. Plug in a USB cable from a high-power port (500 mA) into the UUT (or supply 5 VDC to J1). Verify that the USB input now supplies the input current instead of the ac (J2) input. This demonstrates that JMP2 (PSEL) defines the priority of the inputs. If PSEL = Low (USB priority), then the USB input is used first, if available, and if not it switches to ac power at USB-current levels.
28. Set JMP2 (PSEL) to AC, and verify that the ac supply is providing ~1.5 A of current (~0.44 to the load and 1 A to the battery plus miscellaneous).
29. Remove the ac-input supply and verify that the USB source is supplying between 400 mA and 500 mA of current to the input. The output should have dropped to the DPPM OUTPUT threshold or battery voltage (whichever is higher).
30. Reapply the ac-input source and verify that the ac source is now providing the ~1.5 A as before.
31. Set JMP2 (PSEL) to USB, and verify that the USB source is now providing between 400 mA and

500 mA of current.

32. Set JMP1 to 0.1 on the UUT. Verify that the input current has dropped below 100 mA and $\mathbf{V}_{OUT}$ has dropped slightly below $\mathbf{V}_{BAT}$. In this test, the system load is 10 Ω, which would result in the output dropping to 1 V at 100 mA if there were no other source to help out. As the output voltage drops to the DPPM OUTPUT threshold, the charging current is reduced to zero, but $\mathbf{V}_{OUT}$ continues to drop until it reaches the battery voltage. The internal battery FET turns on to supplement the OUTPUT. This demonstrates battery supplement mode because the system load exceeds the available input current.
33. Disconnect the USB source and verify that the ac source takes over in USB mode at the 100-mA charge level.
34. Set JMP2 to AC (PSEL = High). Verify that the (AC) input current is ~1 A. Verify that IBAT is reduced to half the programmed level, ~0.5 A. This is the ac half-charge mode and is implemented on bq24038 when ISET2 is low (0.1 A) and J2-PSEL is AC (High).
35. Set JMP1 to 0.5. Continue to let the battery charge. Note that once the battery voltage reaches regulation (~4.20 VDC) the charging current tapers off.
36. Verify that the charging terminates when the battery current tapers to C/10 or 100 mA (1 A/10, programmed charge current divided by 10). Verify D2 (STAT1) turns off (High) and D3 (STAT2) turns on (Low).
37. Skip this step if not using a 4.4-VDC-rated $LiMn_2O_4$ cell. Put shunt on JMP7. CAUTION: This programs the battery regulation voltage to 4.36 V, which can potentially cause a battery fire if a 4.2-V-rated LiIon cell is used. Use a 4.4-V-rated $LiMn_2O_4$ cell to verify regulation and termination.
38. If a load is applied across the battery such that the battery is discharged to ~4.1 V, the charger starts a new charging cycle.

This concludes the evaluation of the bq24038 EVM. Several more features implemented in the IC are not demonstrated in this user's guide. See the data sheet to learn more about thermal regulation, thermal cutoff, USB boot up, and short-circuit protection.

5 Schematic

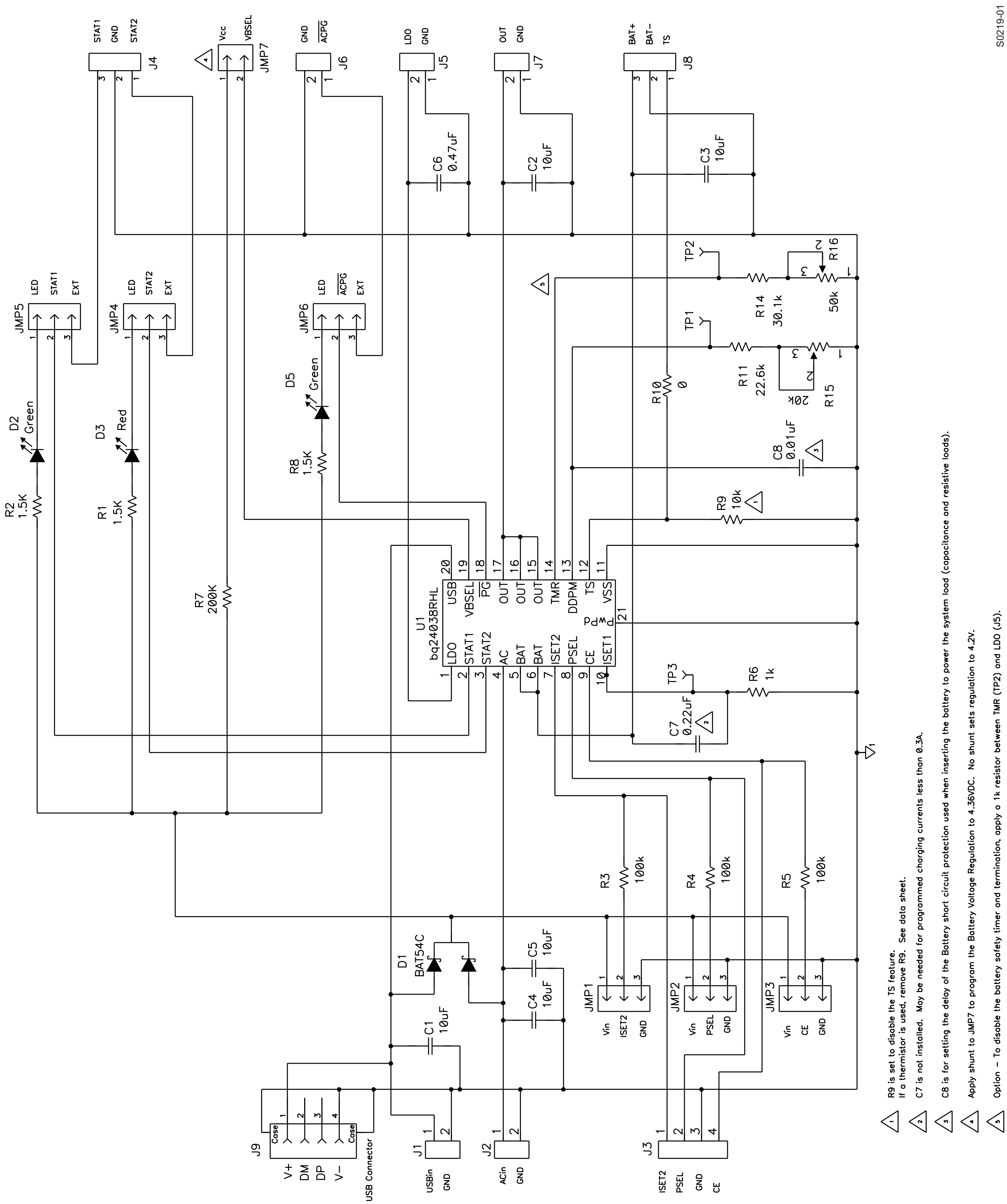

Figure 2. bq24038 EVM Schematic

6 Physical Layouts

This section contains the board layout and assembly drawings for the EVM.

6.1 Board Layout

Figure 3 shows the top assembly view of the EVM. Figure 4 shows the top etch layer of the EVM. Figure 5 shows the board second etch layer of the EVM. Figure 6 shows the board third etch layer of the EVM. Figure 7 shows the bottom etch layer of the EVM.

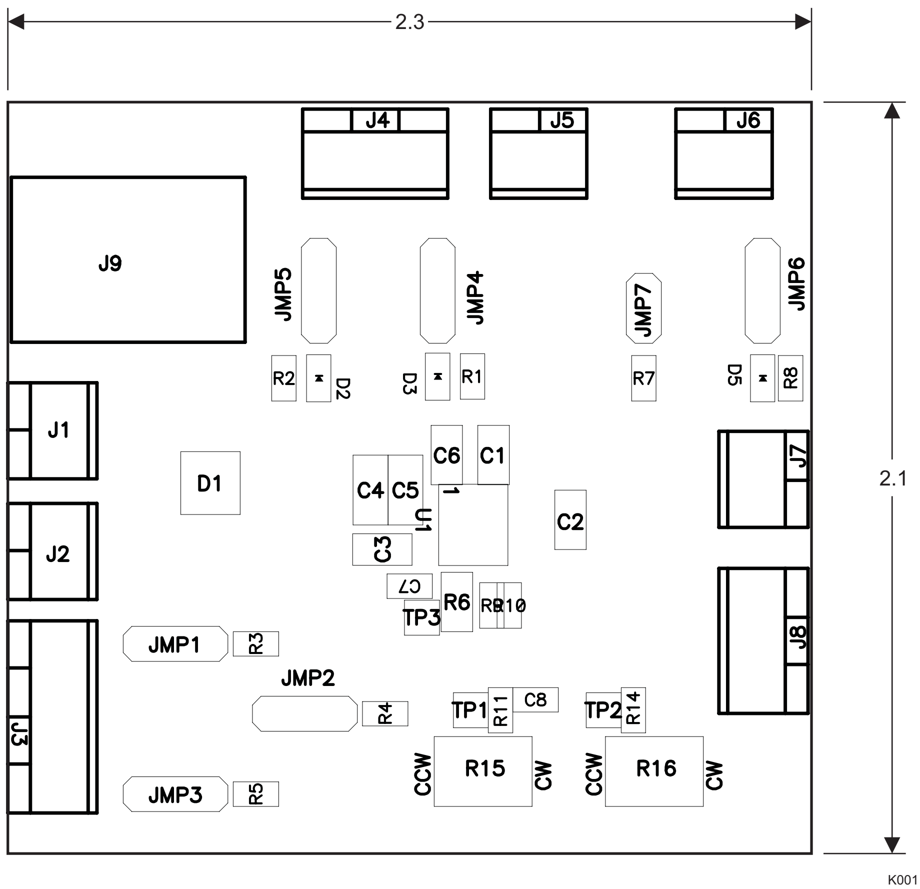

Figure 3. Top Assembly View

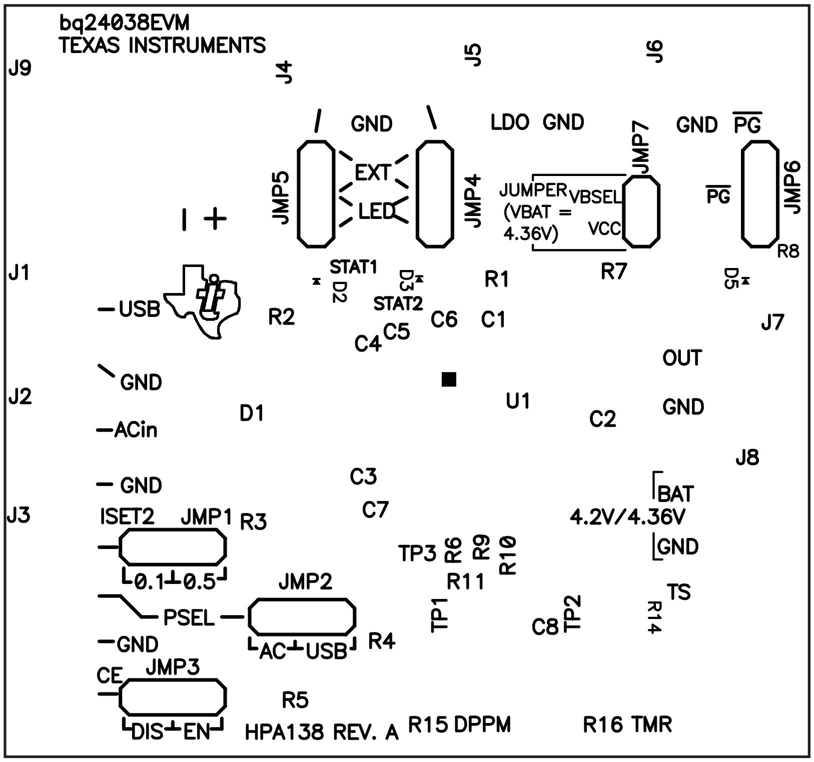

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Figure 4. Board Layout – Silkscreen

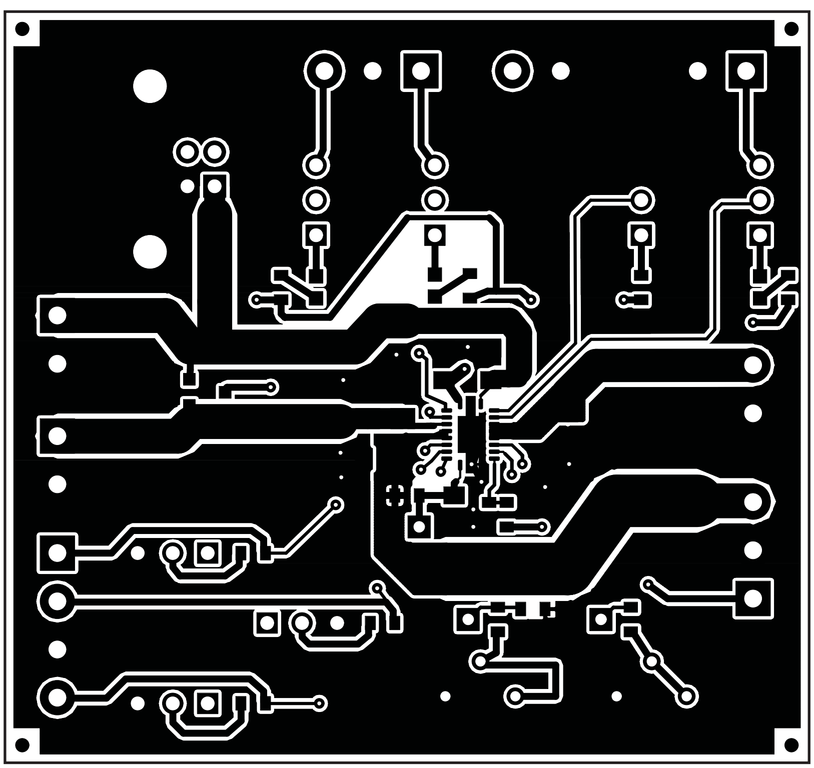

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Figure 5. Board Layout – Top Etch Layer

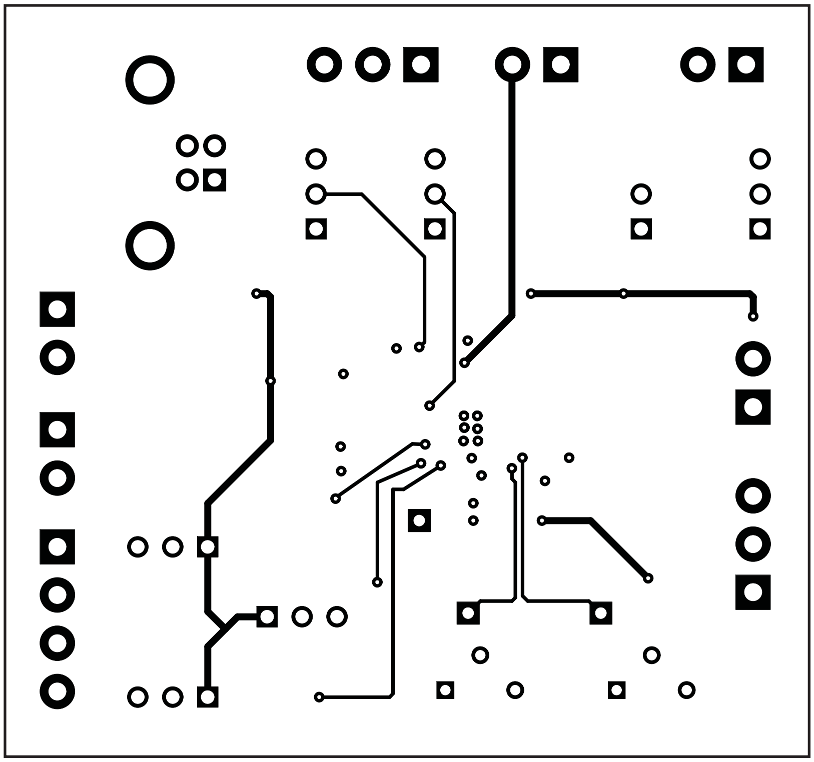

Figure 6. Board Layout – Second Etch Layer

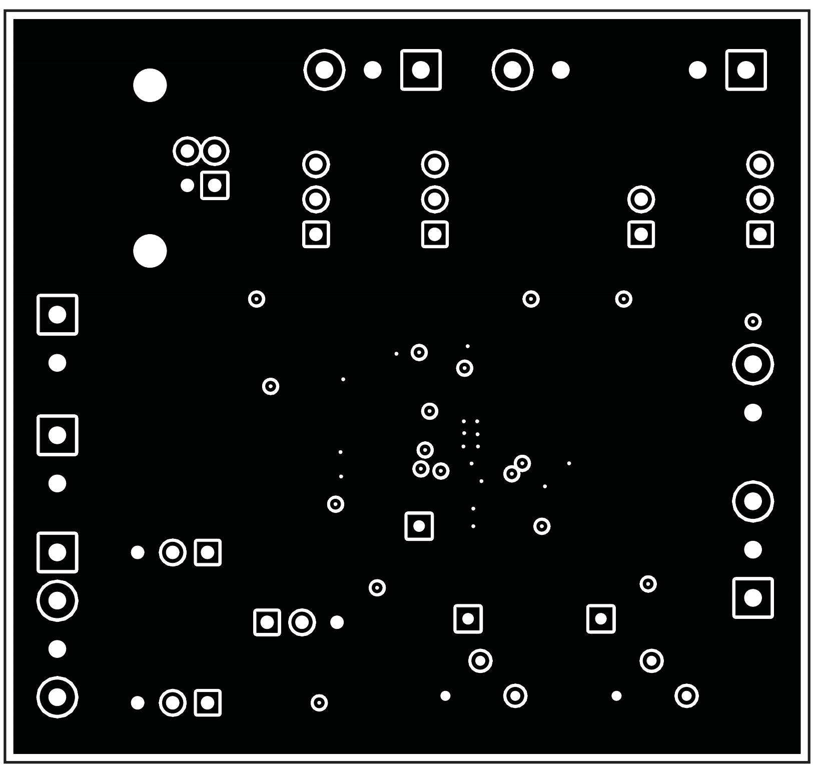

Figure 7. Board Layout – Third Etch and Bottom Layers

7 Bill of Materials

Table 2. Bill of Materials

REFDES	COUNT	DESCRIPTION	SIZE	MFR	PART NUMBER
C1, C2, C3	3	Capacitor, ceramic, 10-µF, 6.3-V, X5R, 20%	805	Panasonic	ECJ-2FB0J106M
C4, C5	2	Capacitor, ceramic, 10-µF, 25-V, X5R, 20%	1206	Panasonic	ECJ-3YB1E106M
C6	1	Capacitor, ceramic, 0.47-µF, 16-V, X7R, 10%	805	Panasonic	ECJ-2YB1C474K
C7	0	Capacitor, ceramic, 0.22-µF, 10-V, X5R, 10%	603	muRata	ECJ-1VB1A224K
C8	0	Capacitor, ceramic, 0.01-µF, 16-V, X7R, 10%	603	Std	Std
D1	1	Diode, dual Schottky, 200-mA, 30-V	SOT23	Vishay -Liteon	BAT54C
D2, D5	2	Diode, LED, green, 2.1-V, 20-mA, 6-mcd	603	Liteon	160-1183-1-ND
D3	1	Diode, LED, red, 1.8-V, 20-mA, 20-mcd	603	Liteon	160-1181-1-ND
J1, J2, J5, J6, J7	5	Terminal block, 2-pin, 6-A, 3,5-mm	0.27-inch x 0.25-inch	OST	ED1514
J3	1	Terminal block, 4-pin, 6-A, 3,5-mm	0.55-inch x 0.25-inch	OST	ED1516
J4, J8	2	Terminal block, 3-pin, 6-A, 3,5-mm	0.41-inch x 0.25-inch	OST	ED1515
J9	1	Connector, USB upstream (type B)	0.47-inch x 0.67-inch	Molex	67068-1000
JMP1, JMP2, JMP3, JMP4, JMP5, JMP6	6	Header, 3-pin, 100-mil spacing, (36-pin strip)	0.10-inch x 3-inch	Sullins	PTC36SAAN
JMP7	1	Header, 2-pin, 100-mil spacing, (36-pin strip)	0.10-inch x 2-inch	Sullins	PTC36SAAN
R1, R2, R8	3	Resistor, chip, 1.5-kΩ, 1/16-W, 1%	603	Std	Std
R3, R4, R5	3	Resistor, chip, 100-kΩ, 1/16-W, 1%	603	Std	Std
R6	1	Resistor, chip, 1-kΩ, 1/10W, 1%	805	Std	Std
R7	1	Resistor, chip, 200-kΩ, 1/16-W, 1%	603	Std	Std
R9	1	Resistor, chip, 10-kΩ, 1/16-W, 1%	603	Std	Std
R10	1	Resistor, chip, 0-Ω, 1/16-W, 1%	603	Std	Std
R11	1	Resistor, chip, 22.6-kΩ, 1/16-W, 1%	603	Std	Std
R14	1	Resistor, chip, 30.1-kΩ, 1/16-W, 1%	603	Std	Std
R15	1	Potentiometer, 20-kΩ, 1/4-inch Cermet, 12-turn, top-adjust	0.25-inch x 0.17-inch	Bourns	3266W-203
R16	1	Potentiometer, 50-kΩ, 1/4-inch Cermet, 12-turn, top-adjust	0.25-inch x 0.17-inch	Bourns	3266W-503
TP1, TP2, TP3	0	Test point, 0.032-inch hole		None	Void
U1	1	IC, single-chip charge and power path management	QFN	TI	bq24038RHL
--	1	PCB, 2.3-inch × 2.1-inch × 0.31-inch		Any	HPA138

8 References

1. *bq24030, bq24032, bq24032A, bq24035, bq24038 Single-Chip Charge and System Power-Path Management IC (bqTINY-III)* data sheet (SLUS618)

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 6.5 V and the output voltage range of 0 V to 6.5 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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