National Semiconductor
The Sight & Sound of Information

# LMH1982 SD/HD Video Clock and Timing Generator with Genlock Capability

Software Application Version 2.0

# Evaluation Software User Guide Rev. 2.1

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# 1 LMH1982 Evaluation Software User Guide

The LMH1982 software application was designed by National Semiconductor (NSC) to support the evaluation of the NSC LMH1982 Evaluation Board Platform. The application runs on a PC and uses a graphical user interface (GUI) to facilitate programming of the LMH1982.

Refer to the LMH1982 datasheet for more information about the device features and operation. For instructions on the LMH1982 evaluation board platform, see the LMH1982 Evaluation Board User Guide. Refer to the LMH1982 product page on National's website to order an evaluation board with samples and to download the software installation files.

Prior to installing the LMH1982 software application, you must install Microsoft .NET Framework version 2.0. The .NET Framework installation file, dotnetfx.exe, can be downloaded from Microsoft's Download Center website: http://www.microsoft.com/downloads/details.aspx?familyid=0856eacb-4362-4b0d-8edd-aab15c5e04f5&displaylang=en.

The LMH1982 software installation files, setup.exe and LMH1982 Setup.msi, will be provided by your NSC field office. Both files should be placed in the same source folder prior to installation.

# 2 Software Installation

1. Run dotnetfx.exe to install Microsoft .NET Framework v2.0 and follow the installation procedure. Ensure it is installed before proceeding to the next step.
2. Run setup.exe to install the LMH1982 software and follow the installation procedure.
3. When the LMH1982 software installation completes, a shortcut icon for the LMH1982 application should appear on your desktop.


# 3 Starting the Application

The evaluation setup requires the NSC LMH1982 evaluation board with the USB interface board and a PC with the software application.

The following steps should be taken before starting the application:

1. Ensure the USB board is properly mounted to the LMH1982 evaluation board.
2. Connect a USB cable between the PC and the USB board.
3. Ensure the LMH1982 evaluation board is powered prior to starting the application.
4. Run the LMH1982 application on your PC by double-clicking the icon on your desktop.
5. When the application is running, you should see "USB Connected All ACK" in the Status Bar at the bottom-left; otherwise, refer to the

Status Bar section in this user guide.

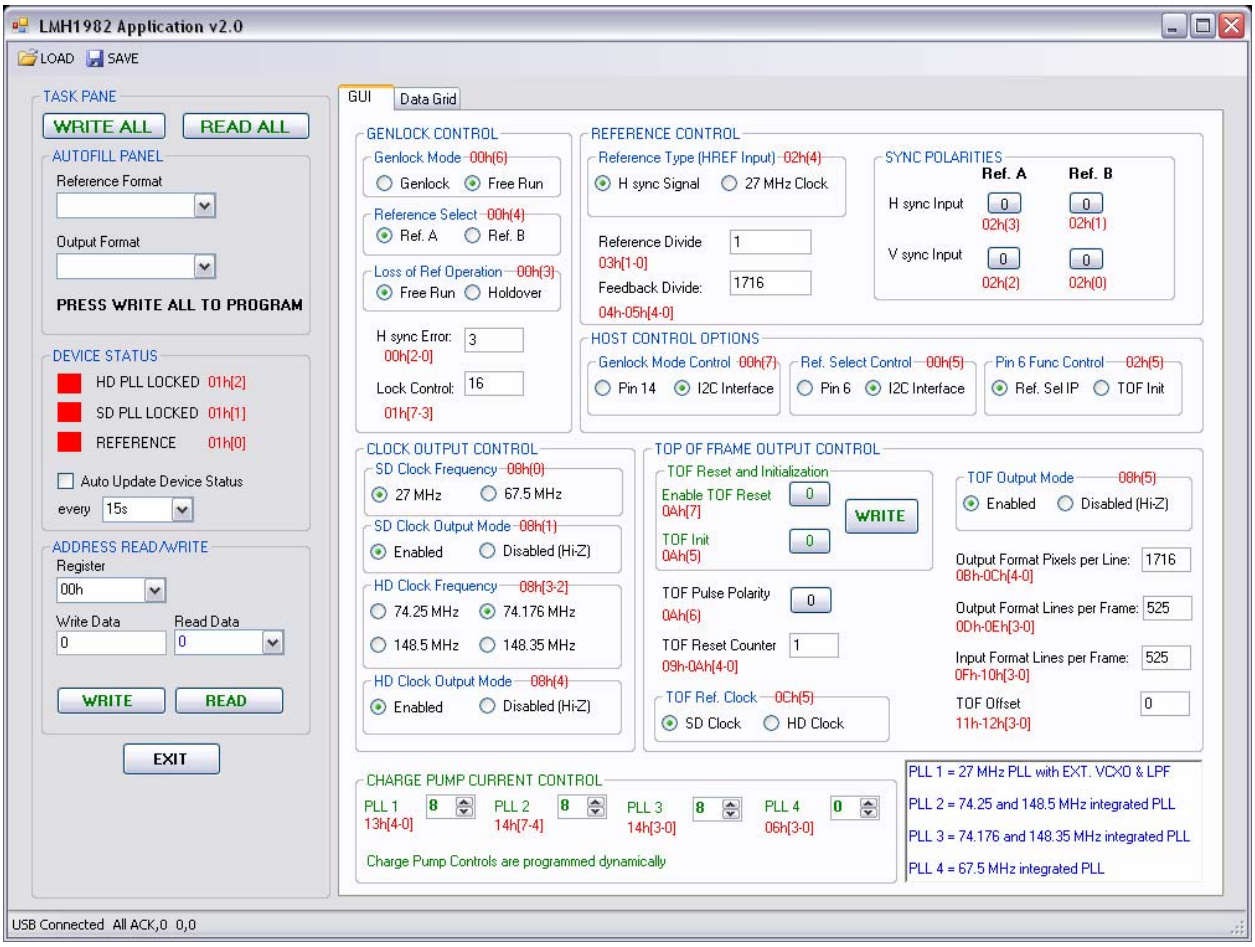
# 4 Programming Overview of the LMH1982

After powering the LMH1982, its control registers will load with default values that determine its initial condition. To operate the LMH1982 in any other condition, you must program the features of the device such as:

- Mode of operation
- Reference selection
- Host control options
- Reference timing format and input polarity
- Reference detector and lock detector control
- Output clock frequencies and output mode
- Output Top of Frame (TOF) timing characteristics and output mode
- PLL charge pump current

# 5 Using the LMH1982 Application

The LMH1982 application was designed for easy access and control of all device features. The application has four main sections: the Status Bar in the bottom-left corner, the Task Pane on the left, the GUI and Data Grid tabs on the right, and the File Menu in the upper-left corner.


LMH1982 Application v2.0
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Pin 6 Func Control 02h(5)
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TOF Init
CLOCK OUTPUT CONTROL
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67.5 MHz
SD Clock Output Mode 08h(1)
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Enabled
Disabled (Hi-Z)
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TOF Reset and Initialization
Enable TOF Reset 0
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TOF Reset Counter 1
09h-0Ah[4-0]
TOF Ref. Clock 0Ch(5)
SD Clock
HD Clock
TOF Output Mode 08h(5)
Enabled
Disabled (Hi-Z)
Output Format Pixels per Line: 1716
0Bh-0Ch[4-0]
Output Format Lines per Frame: 525
0Dh-0Eh[3-0]
Input Format Lines per Frame: 525
0Fh-10h[3-0]
TOF Offset 0
11h-12h[3-0]
CHARGE PUMP CURRENT CONTROL
PLL 1 8
13h[4-0]
PLL 2 8
14h[7-4]
PLL 3 8
14h[3-0]
PLL 4 0
06h[3-0]
Charge Pump Controls are programmed dynamically
PLL 1 = 27 MHz PLL with EXT. VCXO & LPF
PLL 2 = 74.25 and 148.5 MHz integrated PLL
PLL 3 = 74.176 and 148.35 MHz integrated PLL
PLL 4 = 67.5 MHz integrated PLL
USB Connected All ACK,0 0,0

The **Status Bar** in the bottom-left corner indicates the status of the USB interface and $I^2C$ interface.

The **Task Pane** in the left column is used to manage both the device and GUI and is accessible from both tabs. The controls in the Task Pane include:

- **WRITE ALL** button: writes data from the GUI to the control registers
- **READ ALL** button: reads all register data from the device to the GUI, Data Grid, and Device Status panel
- **Auto-Fill** panel: allows you to select the input reference format and output format for automatic population of the relevant GUI controls
- **Device Status** panel: reads the status bits and gives a visual indication of device status
- **Address Read/Write** panel: allows you to read from or write to an individual register
- **EXIT** button: exits the application

The **GUI** contains the control panels necessary to operate the main features of the device. The panels are generally organized by feature and comprised of text fields, radio, and button controls.

**NOTE**: Unless otherwise specified, the GUI controls require you to click the WRITE ALL button before the control registers are updated. Therefore, it is possible to make multiple changes to the GUI and write the data to all registers using the WRITE ALL button. WRITE ALL will sequentially write the data starting at register 00h.

*For quick reference, each control in the GUI has red text nearby to show its associated register address and bits, e.g. 00h[2-0] refers to bits 2-0 of register address 00h.*

The **File Menu** has a LOAD button and a SAVE button. SAVE allows the user to save the control register data stored in the Data Grid to a register configuration file for future reference. LOAD allows the user to open a saved configuration file and load it directly to the GUI.

The **Data Grid** contains all the register addresses and data in a memory array. The READ ALL button must be clicked to update the data grid with the current control register data. The data grid can be accessed to conveniently view all current register contents in tabular format.

## 5.1 Status Bar

The following table lists the possible Status Bar messages with associated user actions. You may disregard the numbers that follow these messages in the Status Bar.

**Table 1: Possible Status Bar Messages**

| Status Bar Message | Status / User Action |
|---|---|
| USB Connected All ACK | Normal. Proceed to use the application. |
| USB Connected I2C ACK2 missing | The $I^2C$ interface is not functioning properly. Verify the LMH1982 is powered on, $I^2C$_ENABLE# input (pin 13) is logic low, and RESET# input (pin 15) is logic high, and then click the READ ALL button. Confirm that "All ACK" appears in the Status Bar, and then proceed to use the application. |
| USB I/O Error,132 | The USB interface is not functioning properly. Verify the USB cable is connected between the PC and the USB board. If the USB board is functioning properly, the Operating System should identify it as a Human Interface Device (HID) in the Device Manager. Re-start the application and confirm a normal status bar appears before proceeding to use the application. |

## 5.2 Task Pane Controls

This section gives a detailed description of each control in the task pane.

### 5.2.1 WRITE ALL Button


Clicking the WRITE ALL button will write data to all control registers that are designated a control in the GUI.

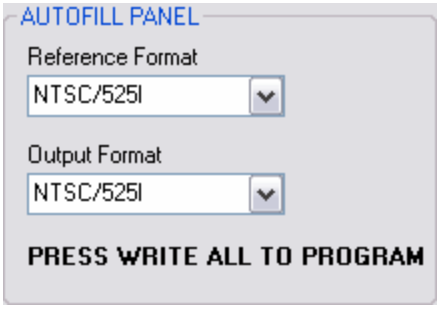
**NOTE**: Factory test registers (addresses 15h-1Fh) are not designated any controls in the GUI. It is recommended not to modify any values in these test registers via the Address Read/Write panel; otherwise, improper operation may result. If any factory test registers are programmed inadvertently, cycle the device power or toggle the RESET# input to restore the default register values.

### 5.2.2 READ ALL Button


Clicking the READ ALL button will read the data from all control registers (including the factory test registers) to populate the GUI, Data Grid, and Device Status panel.

Note: To save the current register configuration to a file, you must first click READ ALL to update the Data Grid and then use the SAVE button. See the **Error! Reference source not found.** section for more information.

### 5.2.3 Auto-Fill Panel

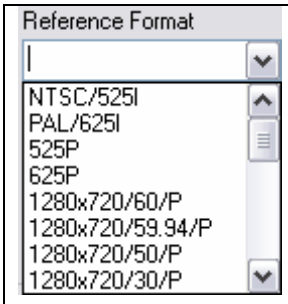
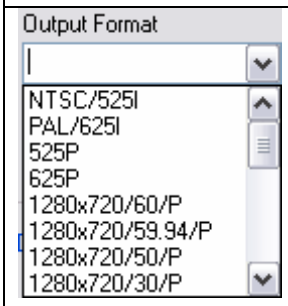



The Reference Format and Output Format drop-down lists in the Auto-Fill panel allow you to select the input reference format and/or the desired output format, respectively. When a selection is made in either list, the GUI will automatically populate specific controls with predetermined values or settings. Refer to the

Appendix section to see the controls (control registers) and corresponding values populated by the auto-fill functions. These auto-fill functions can be used as an alternative to manual manipulation of some controls in the GUI. You can always override any control populated by the auto-fill function by directly changing it in the GUI.

**IMPORTANT**: Changes to the GUI via the auto-fill functions will not be programmed to the device until WRITE ALL is clicked.

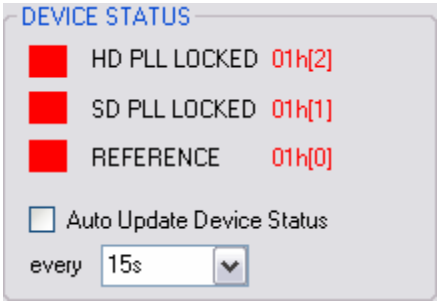
**Table 2: Auto-Fill Control Descriptions**

| | |
|---|---|
|  | The Reference Format list allows you to select the timing format of the input signals applied to the selected reference port (A or B). When a selection is made, the GUI will automatically populate with predefined values/settings for the following controls:<br>• Reference Type<br>• Reference Divide<br>• Feedback Divide<br>• Input Format Lines per Frame<br>• *TOF Reset Counter |
|  | The Output Format list allows you to select the desired output timing format. When a selection is made, the GUI will automatically populate with predefined values for the following controls:<br>• SD Clock Frequency<br>• HD Clock Frequency<br>• *TOF Reset Counter<br>• TOF Ref. Clock<br>• Output Format Pixels per Line<br>• Output Format Lines per Frame |
| *The value for the TOF Reset Counter text field is automatically updated in the GUI using a look-up table based on the selections made in the Reference and Output Format lists. | |

### 5.2.3.1 Clock Selections Available in the Reference Format List

If “27 MHz Clock” or “48 kHz Audio Clock” is selected from the Reference Format list, the Output Format will default to “PAL/625I” and the GUI will be populated with predefined values. When the device is subsequently programmed using the WRITE ALL button, this will ensure a predictable free-running output TOF pulse rate of 25 Hz (assuming there is no associated input V signal). In addition, a dialog box will prompt you to program Enable TOF Reset to 0, if you opt not to program the TOF register controls correctly. See the Top of Frame Output Control section for more information about programming the output format registers.

### 5.2.4 Device Status




The Device Status panel shows red/green indicators relating to the PLL lock status and input reference status in genlock mode. To update the device status indicators, click the READ ALL button or use the auto-update function. To auto-update the device status indicators, click the check box accordingly and select the time interval from the drop down list.

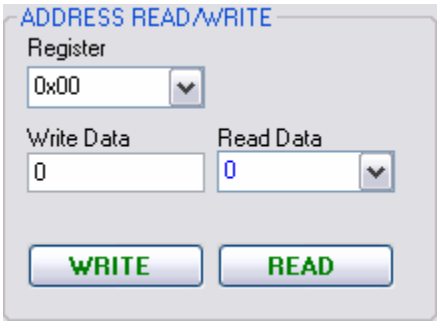
The REFERENCE status indicates when valid signal has been detected at the HREF input of the selected reference when operating in genlock mode. Green indicates a valid reference, while red indicates loss of reference. In free run mode, the REFERENCE status indicator will be red when there is no input reference.

The HD PLL LOCKED status indicates whether the HD output clock is phase-locked to the 27MHz VCXO clock. Green indicates the HD clock is locked, while red indicates it is not locked.

The SD PLL LOCKED status indicates whether the SD output clock is phase-locked to the HREF input signal. Green indicates the SD clock is locked, while red indicates it is not locked.

Refer to the LMH1982 datasheet for more information about the device status bit and status output pins.

### 5.2.5 Address Read/Write




This panel allows you to read from and write to a single register address.

To read from a register, select an address (in hex) from the Register drop down list, click READ, and the data will appear in the Read Data drop down list. The Read Data list can be selected to show the data in hex, decimal, and binary form.

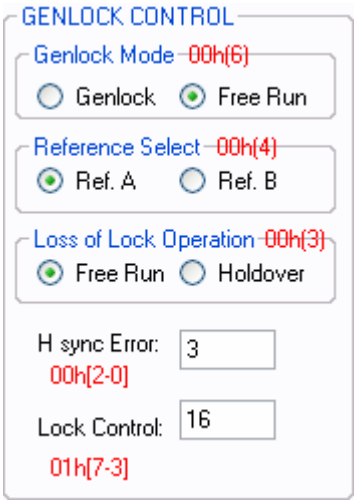
To write to a register, select a register address from the Register drop down list, type the data (in decimal), and click WRITE. The largest value that can be written to a register is 255 ($2^8 - 1$). If a value greater than 255 is entered, an error dialog box will appear, no data will be written, and a new value will need to be re-entered.

## *5.3 GUI Controls*

The GUI is divided into seven main panels for controlling the features of the LMH1982. When the application is started, it will populate the GUI with default values.

**NOTE:** Upon start-up of the evaluation software, the initial values populated in the GUI will match the default data specified in the $I^2C$ interface register map table in the LMH1982 datasheet. To update the GUI with the current register data, click READ ALL.

### 5.3.1 Genlock Control




This panel controls the mode of operation, reference selection, loss of lock operation, and the reference and lock detect threshold.

In the Genlock Mode control, you can select whether to operate the device in genlock mode or free run mode. Select Genlock to phase-lock the outputs to the selected input reference. By default, Free Run is selected. In free run mode, the outputs will be based on the external 27 MHz VCXO, which will operate independently of any input reference; therefore, the accuracy of the outputs will depend on the frequency accuracy of the VCXO. The LMH1982 voltage input, VC_FREERUN (pin 1), can be externally biased to set the VCXO input control voltage in free run mode.

In the Reference Select control, you can choose Ref A or Ref B as the input reference port for genlocking the outputs.

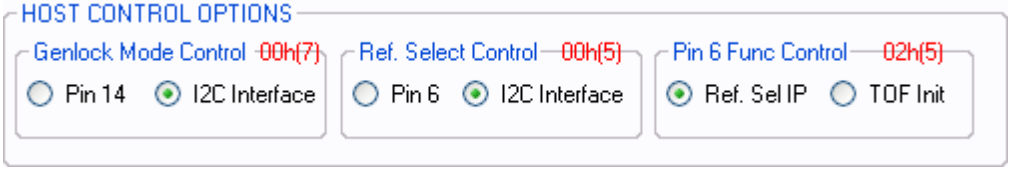
In the Loss of Ref Operation control, you can select Free Run or Holdover as the operating mode upon a loss of reference condition. If Free Run is selected, then the device will operate in free run mode until a reference is reapplied. If Holdover is selected, then the LPF output (pin 31) will

be put into high-impedance mode until a reference is reapplied. Holdover operation upon a loss of reference allows the loop filter to temporarily hold the charge stored across it (VCXO control voltage) to temporarily sustain the LMH1982 output frequency accuracy upon a loss of reference. Refer to the LMH1982 datasheet for a more complete description of the holdover feature and register programming information.

In the H sync Error text field, you can specify the maximum number of missing pulses on the selected HREF input before indicating a loss of reference (LOR). The LOR threshold will be the H sync error value multiplied by the PLL reference divider value, shown in Table 3. Refer to the datasheet for more information about the reference detector and LOR threshold programming.

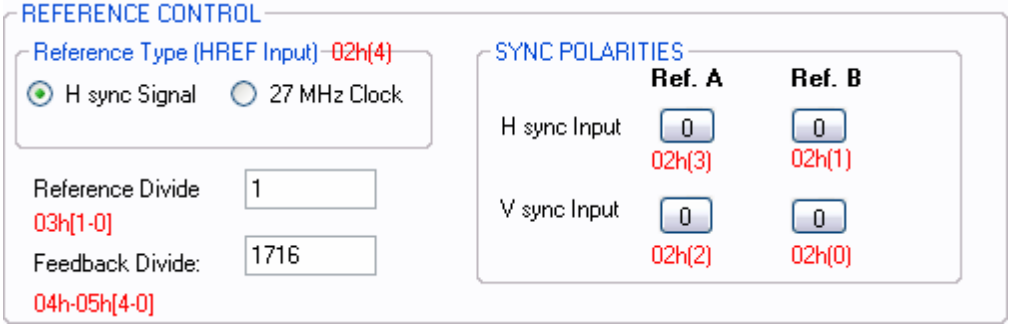
In the Lock Control text field, you can control the threshold of the lock detection circuit for PLL1 (VCXO PLL). A larger value will yield shorter lock indication time (although not actual lock time) at the expense of higher output phase error when lock is initially indicated, whereas a smaller value will yield the opposite effect. To reduce the probability of false loss of lock indication or lock status instability, LOCK_CTRL can be increased to improve the lock detector's ability to tolerate a larger amount of input phase jitter or phase error. This can help to ensure the NO_LOCK output and SD_LOCK bit are stable when the reference signal has large input jitter. Refer to the datasheet for more information about the lock detector and lock threshold programming.

### 5.3.2 Host Control Options




In this panel, the Reference Select and Genlock Mode functions can be controlled via the $I^2C$ interface (default) or via the external logic input pins. The Pin 6 Func Control allows the user to override the default reference selection capability on pin 6 and instead use pin 6 as a logic pulse input for output alignment initialization.
The $I^2C$ interface register controls for Genlock Mode and Reference Selection were described in the previous Genlock Control section. Instead of using the $I^2C$ interface, Pin 6 (REF_SEL) and Pin 14 (GENLOCK#) can be applied with logic level inputs to control the Reference Select and Genlock Mode, respectively.

### 5.3.3 Reference Control



This panel is used to specify the input timing format and input characteristics of the selected reference. The default values are set up for an NTSC reference timing format with negative polarities (active low) sync input signals. Refer to the datasheet for the table of supported input reference timing formats/standards and corresponding PLL divider register values.

If the reference signal at the HREF input is a 27 MHz clock source, select 27 MHz Clock in the Reference Type panel; otherwise, select H sync Signal.

In the text field for Reference Divide, you can specify the value of the REF_DIV register, which sets the denominator of the 27 MHz PLL divide ratio based on the look-up table below.

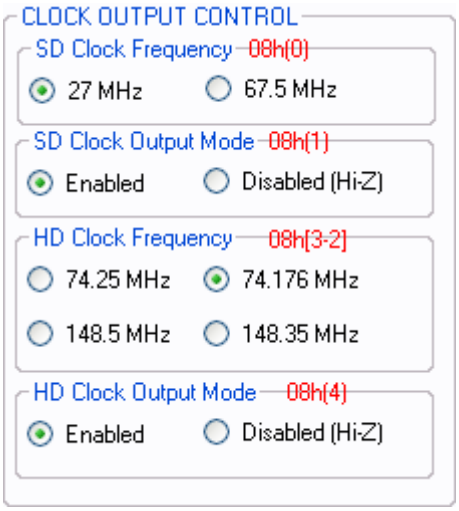
**Table 3: Reference Divider Look-Up Table**

| REF_DIV value (decimal) | REF_DIV bit 1 | REF_DIV bit 0 | Actual PLL Reference Divide value (decimal) |
|---|---|---|---|
| 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 2 |
| 2 | 1 | 0 | 5 |

In the text field for Feedback Divide, you can specify the value of the FB_DIV register, which sets the numerator of the 27 MHz PLL divide ratio.

Using the buttons in the Sync Polarities panel, you can change the button values to specify the pulse polarity for the HREF input and VREF input of both Reference A and B. A button value of 0 (default) corresponds to negative polarity (active low) and a value of 1 corresponds to positive polarity (active high).

### 5.3.4 Clock Output Control

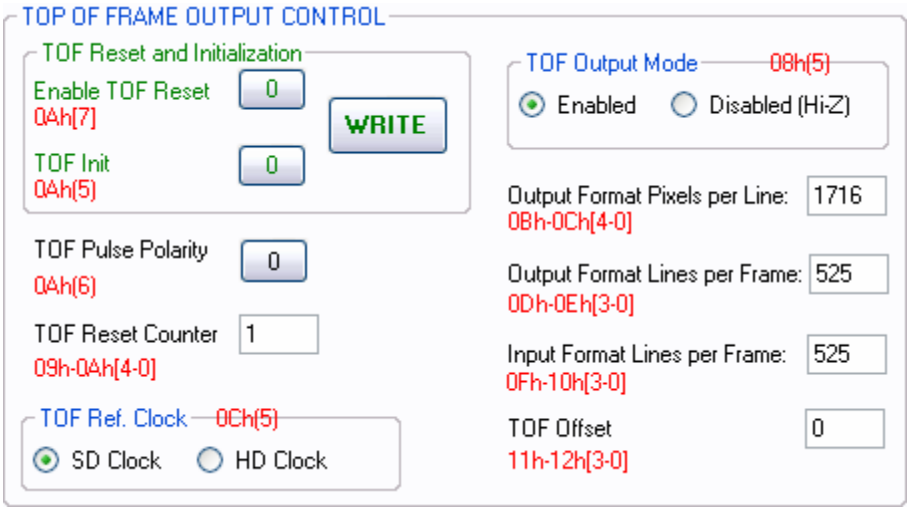



This panel allows you to select the clock frequency and output mode for the SD clock output and the HD clock output. If the clock output is not used, then you can disable the output, which sets

the LVDS output pair into high impedance (Hi-Z) mode. The default output frequencies and output modes are shown in the figure below.

**IMPORTANT:** If 148.35 MHz is selected as the HD clock, it is recommended to follow the initial programming sequence described in the LMH1982 datasheet section titled, "RECOMMENDED START-UP PROGRAMMING SEQUENCE."

### 5.3.5 Top of Frame Output Control




This panel allows you to program the output TOF timing characteristics. The default values are set up for the NTSC output timing format. Refer to the LMH1982 datasheet for detailed descriptions on programming the output format registers.

The TOF Reset and Initialization panel contains two buttons, Enable TOF Reset and TOF Init. **The dedicated WRITE button can be used instead of the WRITE ALL button to program the two buttons inside the TOF Reset and Initialization panel.** Programming a button value of 1 for Enable TOF Reset allows the TOF reset circuit to be enabled; otherwise, the reset circuit will be disabled. Programming the button value for TOF Init from 0 to 1 produces a rising edge for resetting the TOF Reset Counter. This bit should be pulsed during the output frame immediately prior to the frame the reset it to occur.

**NOTE:** For applications where the TOF output is not used and only the output clocks are required, Enable TOF Reset should be set to 0 to disconnect the internal TOF reset circuit from the internal PLL; otherwise, the internal TOF reset circuit can periodically reset the PLLs and consequently disturb output clocks. It is also recommended to set Enable TOF Reset to 0 when a reference is applied without an associated V signal, such as a 27 MHz or 48 kHz clock. Furthermore, when the TOF output is not used, the TOF output mode should be set to disabled, which will put the TOF output pin into high impedance (Hi-Z) mode.

The polarity of the output TOF pulse can be selected by changing the value of TOF Pulse Polarity button. A button value of 0 (default) corresponds to negative polarity and a value of 1 corresponds to positive polarity.

When the output is genlocked to the reference, the input reference is used to reset the internal circuit controlling the TOF output. In the text field for TOF Reset Counter, you can specify the counter reset value, or TOF_RST. Therefore, the output TOF pulse will occur every N input frames, where N = TOF_RST. Refer to the datasheet to determine the correct value for TOF_RST.

In the TOF Ref. Clock control, select the SD Clock or HD Clock as the reference clock for the output TOF pulse timing.

In the text field for Output Format Pixels per Line, specify the total number of pixels/samples per line for the desired output format.

In the text field for Output Format Lines per Frame, specify the total number of lines per frame for the desired output format.

In the text field for Input Format Lines per Frame, specify the total number of lines per frame for the input reference format.

In the text field for TOF Offset, specify the number of lines to delay the TOF output pulse. The line delay will be with respect to the input format. The TOF output pulse can be advanced by programming a value equal to the maximum number of lines per frame of the input format minus the desired advance. TOF_OFFSET must be greater than zero but less than or equal to the total lines per reference frame. If no line offset is required, then set TOF_OFFSET equal to REF_LPFM instead of zero (invalid). Refer to the datasheet for programming TOF Offset to properly align the TOF pulse with the true top of frame location for the input reference.

### 5.3.6 PLL Information Box


For your reference, this information box provides short descriptions for PLLs 1 – 4. PLL 1 uses an external loop filter and external 27 MHz VCXO, while PLLs 2 – 4 have integrated loop filters and VCOs.

### 5.3.7 Charge Pump Current Control

The Charge Pump Current for PLL 1, 2, 3, and 4 can be controlled using the up/down control to adjust the value inside each text field. With each click on the up/down control, the application dynamically writes the new value to the device. Alternatively, when a new value is typed and the ENTER key is pressed, the application will dynamically write the value to the device. A smaller value corresponds to less charge pump current. Refer to the datasheet for guidelines to program the charge pump current controls for PLLs 1-4.

**NOTE:** Data bit 4 of register 06h is inverted internally, so it must be accounted for when programming the charge pump current control text field for PLL 4 in the GUI. For example, the text field for PLL 4 should be programmed with 0d (0000b) to program an effectively value of 8d (1000b).

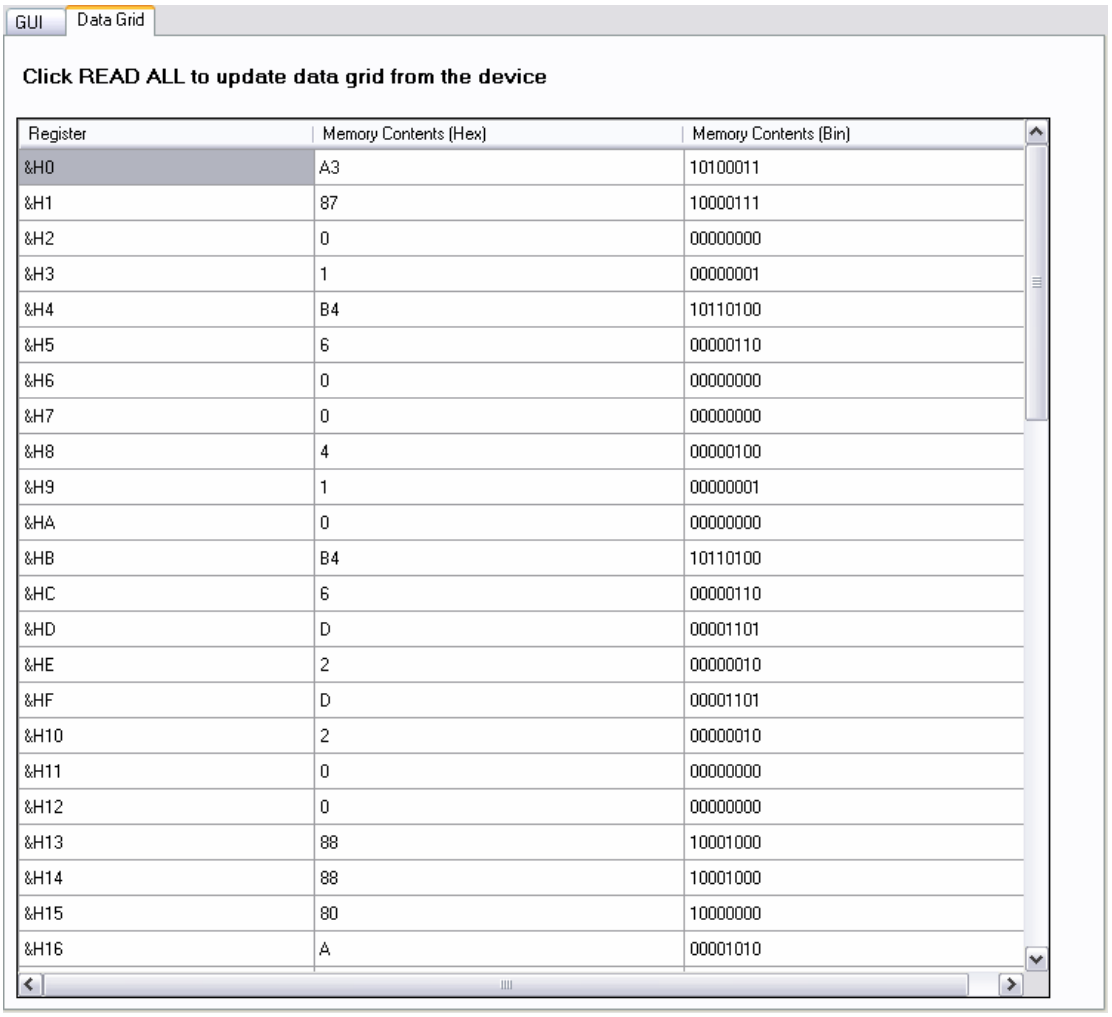
## 5.4 File Menu


The SAVE button allows you to save the register data stored in the Data Grid to a register configuration file for future reference. Before proceeding to save the file, press the READ ALL button to update the Data Grid with the latest register data. When SAVE is clicked, the application will prompt you to select a folder and file name to save the file. The saved file is essentially a text file (.txt) in comma separated values format.

The LOAD button allows you to open a saved register configuration file and load it directly to the GUI. When LOAD is click, the application will prompt you to select the file to open.

## 5.5 Data Grid

When the application is started, all control registers are read and stored to the Data Grid. The READ ALL button should be clicked to update the data grid with the current register data. The data grid may be used to view the current register data in tabular form. The data grid also enables the control register data to be saved to a file using the SAVE button in the File Menu, described in the next section.


GUI
Data Grid
Click READ ALL to update data grid from the device
Register
Memory Contents (Hex)
Memory Contents (Bin)
&H0 A3 10100011
&H1 87 10000111
&H2 0 00000000
&H3 1 00000001
&H4 B4 10110100
&H5 6 00000110
&H6 0 00000000
&H7 0 00000000
&H8 4 00000100
&H9 1 00000001
&HA 0 00000000
&HB B4 10110100
&HC 6 00000110
&HD D 00001101
&HE 2 00000010
&HF D 00001101
&H10 2 00000010
&H11 0 00000000
&H12 0 00000000
&H13 88 10001000
&H14 88 10001000
&H15 80 10000000
&H16 A 00001010

# 6 Appendix

## *Auto-Fill Control Registers with Values*

The following tables show the control registers with corresponding values populated by the Reference Format and Output Format Auto-Fill functions.

**Table 4: Reference Format Auto-Fill – Register Controls and Values**

| Video Format | Reference Type 0x02[4] | Ref_Div 0x03[2-0] | FB_Div 0x04-0x05 | Input Lines per Frame 0x0F-0x10 |
|---|---|---|---|---|
| **NTSC/525I** | 0 | 1 | 1716 | 525 |
| **PAL/625I** | 0 | 1 | 1728 | 625 |
| **525P** | 0 | 1 | 858 | 525 |
| **625P** | 0 | 1 | 864 | 625 |
| **1280x720/60/P** | 0 | 1 | 600 | 750 |
| **1280x720/59.94/P** | 0 | 2 | 3003 | 750 |
| **1280x720/50/P** | 0 | 1 | 720 | 750 |
| **1280x720/30/P** | 0 | 1 | 1200 | 750 |
| **1280x720/29.97/P** | 0 | 2 | 6006 | 750 |
| **1280x720/25/P** | 0 | 1 | 1440 | 750 |
| **1280x720/24/P** | 0 | 1 | 1500 | 750 |
| **1280x720/23.98/P** | 0 | 0 | 3003 | 750 |
| **1920x1080/60/I** | 0 | 1 | 800 | 1125 |
| **1920x1080/59.94/I** | 0 | 2 | 4004 | 1125 |
| **1920x1080/50/I** | 0 | 1 | 960 | 1125 |
| **1920x1080/60/P** | 0 | 1 | 400 | 1125 |
| **1920x1080/59.94/P** | 0 | 2 | 2002 | 1125 |
| **1920x1080/50/P** | 0 | 1 | 480 | 1125 |
| **1920x1080/30/P** | 0 | 1 | 800 | 1125 |
| **1920x1080/29.97/P** | 0 | 2 | 4004 | 1125 |
| **1920x1080/25/P** | 0 | 1 | 960 | 1125 |
| **1920x1080/24/P** | 0 | 1 | 1000 | 1125 |
| **1920x1080/23.98/P** | 0 | 1 | 1001 | 1125 |
| **27MHz clock** | 1 | 1 | 1 | 4000 |
| **48kHz audio clock** | 0 | 0 | 1125 | 1920 |

**Table 5: Output Format Auto-Fill – Register Controls and Values**

| Video Format | HD Clock Frequency 0x08[3-2] | SD Clock Frequency 0x08[0] | TOF Reset Counter 0x09-0x0A | TOF Ref. Clock 0x0C[13] | Output Pixels per Total Line 0x0B-0x0C | Output Lines per Frame 0x0D-0x0E |
|---|---|---|---|---|---|---|
| **NTSC/525I** | 1 | 0 | Determined by selection of Reference Format and Output Format. See NOTE below. | 0 | 1716 | 525 |
| **PAL/625I** | 0 | 0 | | 0 | 1728 | 625 |
| **525P** | 1 | 0 | | 0 | 858 | 525 |
| **625P** | 0 | 0 | | 0 | 864 | 625 |
| **1280x720/60/P** | 0 | 0 | | 1 | 1650 | 750 |
| **1280x720/59.94/P** | 1 | 0 | | 1 | 1650 | 750 |
| **1280x720/50/P** | 0 | 0 | | 1 | 1980 | 750 |
| **1280x720/30/P** | 0 | 0 | | 1 | 3300 | 750 |
| **1280x720/29.97/P** | 1 | 0 | | 1 | 3300 | 750 |
| **1280x720/25/P** | 0 | 0 | | 1 | 3960 | 750 |
| **1280x720/24/P** | 0 | 0 | | 1 | 4125 | 750 |
| **1280x720/23.98/P** | 1 | 0 | | 1 | 4125 | 750 |
| **1920x1080/60/I** | 0 | 0 | | 1 | 2200 | 1125 |
| **1920x1080/59.94/I** | 1 | 0 | | 1 | 2200 | 1125 |
| **1920x1080/50/I** | 0 | 0 | | 1 | 2640 | 1125 |
| **1920x1080/60/P** | 2 | 0 | | 1 | 2200 | 1125 |
| **1920x1080/59.94/P** | 3 | 0 | | 1 | 2200 | 1125 |
| **1920x1080/50/P** | 2 | 0 | | 1 | 2640 | 1125 |
| **1920x1080/30/P** | 0 | 0 | | 1 | 2200 | 1125 |
| **1920x1080/29.97/P** | 1 | 0 | | 1 | 2200 | 1125 |
| **1920x1080/25/P** | 0 | 0 | | 1 | 2640 | 1125 |
| **1920x1080/24/P** | 0 | 0 | | 1 | 2750 | 1125 |
| **1920x1080/23.98/P** | 1 | 0 | | 1 | 2750 | 1125 |

**NOTE**: TOF Reset Counter (TOF_RST register) should be programmed with the numerator value from the ratio of (Input Frame Rate / TOF Frame Rate) after the ratio is reduced to its lowest integer terms.

To ensure the output format configuration registers are correctly programmed to give a proper TOF output, the following two equations should be true:

TOF Rate = Reference Clock Frequency / (Output Pixels per Line * Output Lines per Frame)

and

TOF Reset = Numerator of ratio (REF Frame Rate / TOF Rate) after reduced to lowest integer terms.

# 7 Revision History

| Revision | Date | Comments |
|---|---|---|
| 1.0 | November 2007 | New document created. |
| 2.0 | February 2008 | Revised for LMH1982 Application v2.0. |
| 2.1 | May 2008 | Minor edits. |

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