

DS90C031,DS90C032

LVDS?????



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An Overview of LVDS Technology

National Semiconductor
Application Note 971
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INTRODUCTION

Recent growth in high-end processors, multi-media, virtual reality and networking has demanded more bandwidth than ever before. But the point-to-point physical layer interfaces have not been able to deal with moving information at the data rates required. Some of today's biggest challenges that remain to be solved include: the ability to transfer data fast, lower power systems than currently available, and economical solutions to overcome the physical layer bottleneck. Data Transmission standards like RS-422, RS-485, SCSI and others all have their own limitations most notably in transferring raw data across a media. Not anymore. Low Voltage Differential Signaling (LVDS) is a high speed (>155.5 Mbps), low power general purpose interface standard that solves the bottleneck problems while servicing a wide range of application areas.

This application note explains the key advantages and benefits of LVDS technology. Throughout this application note the DS90C031 (LVDS 5V Quad CMOS Differential Line Driver) and the DS90C032 (LVDS 5V Quad CMOS Differential Line Receiver) will be used to illustrate the key points. Over 50 LVDS devices are offered currently (1998) from National, please refer to the LVDS device datasheets for complete specifications.

STANDARDS OVERVIEW

There are two industry standards that define LVDS. The more common of the two is the generic electrical layer standard defined by the TIA. This standard is known as ANSI/TIA/EIA-644. The other application specific standard is an IEEE (Institute for Electrical and Electronics Engineering) standard titled Scalable Coherent Interface (SCI).

ANSI/TIA/EIA-644

This standard was developed under the Data Transmission Interface committee TR30.2. This standard defines driver output and receiver input characteristics. Functional specifications and/or Protocols are not within the scope of the TIA standard. It notes a recommended maximum data rate of 655 Mbps and a theoretical maximum of 1.923 Gbps based on a loss-less media; however, maximum data rate is application (desired signal quality), and device specific (transition time). It is feasible that LVDS based interface will operate in the 500 Mbps to 1.5Gbps range in the near future. Minimum media specifications are also defined within the standard. It also discusses failsafe operation of the receiver under fault conditions and other configurations issues such as multi-receiver operation. National Semiconductor held the editor position for this standard.

IEEE 1596.3 SCI-LVDS

SCI originally referenced a differential ECL interface within the SCI (Scalable Coherent Interface) 1596-1992 IEEE standard. But, this only addressed the high data rates required and did not address the low power concerns. Thus, SCI-LVDS was defined as a subset of SCI, and is specified in IEEE 1596.3 standard. SCI-LVDS specifies signaling lev-

els (electrical specifications) for the high speed/low power physical layer interface. It also defines the encoding for packet switching used in SCI data transfers. Packets are constructed from 2-byte (doublet) symbols. This is the fundamental 16-bit symbol size. No media is specified and the data rate can be in the order of 500 MT/s based on serial or parallel transmission of 1, 4, 8, 16, 32, 64,..... bits.

SCI-LVDS also supports RamLink for super low power data transmission in a restricted environment. The IEEE 1596.3 standard was approved in March 1994. National Semiconductor held the Chairperson position for this standard.

SCI-LVDS is similar to the TIA version but differs in some electrical requirements and load conditions. Both standards feature similar driver output levels, receiver thresholds and data rates. The TIA version is the more generic of the two standards and is intended for multiple applications.

LOW VOLTAGE DIFFERENTIAL SIGNALING

LVDS technology uses differential data transmission. The differential scheme has a tremendous advantage over single-ended schemes as it is less susceptible to common mode noise. Noise coupled onto the interconnect is seen as common mode modulations by the receivers and is rejected. The receivers respond only to differential voltages.

LVDS technology is not dependent on a specific power supply, such as +5V. This means there is an easy migration path to lower supply voltages such as +3.3V, +2.5V or even lower while still maintaining the same signaling levels and performance. Technologies like ECL or PECL are more dependent on the supply voltage. This feature is highly desirable in any application that foresees moving to lower supply voltages without substantial redesign or worrying about mixed voltage operation (+5V/+3.3V) on system boards.

To achieve high data rate, low power and to reduce EMI effects, signaling levels have to be reduced. The DS90C031/DS90C032 chipset's limitation on data rate is mainly dependent on the technology driving the LVDS drivers. The aggregate bandwidth that LVDS technology can drive is in the Gbps range with a loss-less media. Data rates in the 500-1,000 Mbps are possible and this limitation is primarily dependent on the media being driven.

SIGNALING LEVELS

As the name implies, LVDS features a **low voltage** swing compared to other industry data transmission standards. The signaling levels are illustrated in *Figure 1*, and a comparison to PECL levels is also shown as reference. Because of the low swing advantage, LVDS achieves a high aggregate bandwidth in point-to-point applications. National has recently introduced a new family of parts called Bus LVDS. This family extends LVDS from point-to-point applications to multi-point applications is fully discussed in other National application notes. Bus LVDS features similar voltage swings, but provides increased drive current to handle double terminations required in multi-point applications.

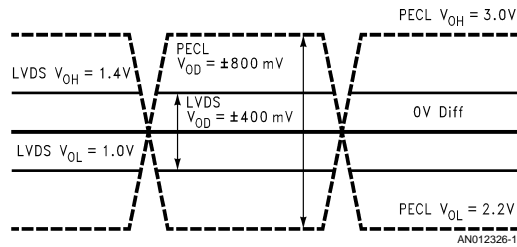


FIGURE 1. PECL vs LVDS Signal Swing

It is impossible to achieve high data rates and provide low power without utilizing low voltage swings. LVDS signaling levels are smaller (50%) than PECL levels as shown in *Figure 1*. EMI effects are also reduced as the signaling swings are much smaller than traditional CMOS, TTL or even PECL. This is due to the current mode drivers, the soft transitions, the low switching currents and the use of true differential data transmission.

LVDS TERMINATION

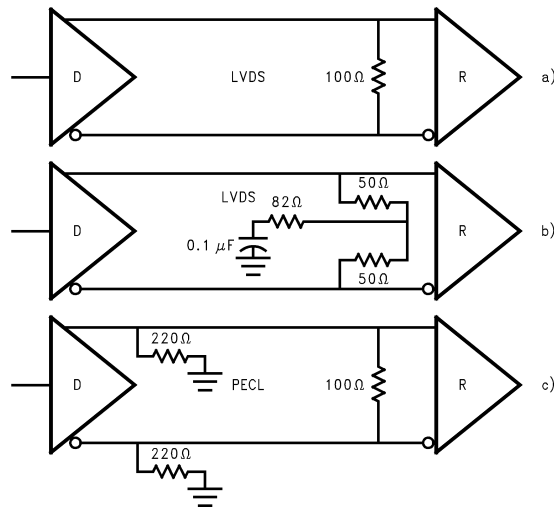
LVDS uses a constant current mode driver to obtain its many features. The value of the current source for the DS90C031 is a maximum of 4.5 mA. The transmission media must be terminated to its characteristic impedance to prevent reflections. Typically this is between 100Ω–120Ω and is matched to the actual cable. *A termination resistor is required* to generate the Differential Output Voltage (V_{OD}) across the resistive termination load at the receiver input (see *Figure 2 A*). Data transmission from the driver to receiver without the termination is not recommended. The simplicity of the LVDS termination scheme makes it easy to implement in most applications. It is recommended to have a single 100Ω termination between the driver outputs, and the use of surface mount components is also recommended to reduce the effects of parasitics. The single resistor approach is the most common LVDS termination method because of its simplicity. Proper termination not only avoids reflection problems, but also reduces unwanted electromagnetic emissions.

The user may also use a cable damping resistor with a capacitor to ground as shown in *Figure 2B*. This method provides additional common mode termination. Due to the additional complexity, this approach is not too common.

ECL and PECL require more complex terminations than the “one” resistor solution for LVDS. PECL drivers typically require 220Ω pull down resistors from each driver output to ground along with the 100Ω across the driver outputs as shown in *Figure 2C*. This termination system requires additional PCB space and increases system cost compared to the single resistor LVDS termination.

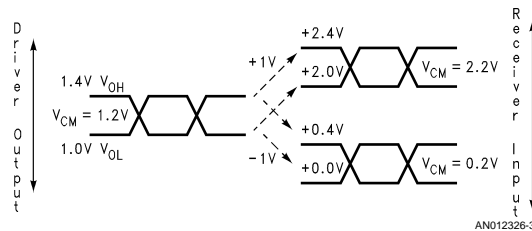
COMMON MODE RANGE

An LVDS receiver can tolerate a minimum of ±1V ground shift between the driver’s ground and the receiver’s ground. Note that LVDS has a typical driver offset voltage of +1.2V, and the summation of ground shifting, driver offset voltage and any longitudinally coupled noise is the common mode voltage seen on the receiver input pins with respect to the receiver ground. The common mode range of the receiver is +0.2V to +2.2V, and the recommended receiver input voltage range is from ground to +2.4V. For example, if a driver has a V_{OH} of 1.4V and a V_{OL} of 1.0V (with respect to the driver ground), and a +1V ground shift is present (driver ground +1V higher than receiver ground), this will become +2.4V (1.4+1.0) as V_{IH} and +2.0V (1.0+1.0) as V_{IL} on the receiver inputs referenced to the receiver ground (+2.2V V_{CM}). Similarly, with a –1V ground shift and the same driver levels results as 0.4V (1.4–1.0) V_{IH} and 0.0V (1.0–1.0) V_{IL} on the receiver inputs (+0.2V V_{CM}). This is shown graphically in *Figure 3*.



AN012326-2

FIGURE 2. a, b, c. Termination Schemes



AN012326-3

FIGURE 3. Common Mode Voltage Range

FAILSAFE FEATURE

Failsafe is a receiver feature that guarantees the output to be in a known logic state (HIGH) under certain fault conditions. This occurs when the inputs of the receiver are either open, shorted or terminated.

In some applications, not all receivers of the Quad DS90C032 may be used. In this case, the unused receiver inputs should be left *open*. If the receiver does not support failsafe and the inputs are left *open* (See Figure 4), any external noise above the receiver threshold can trigger the output and cause an error on the communication line. Since the DS90C032 supports open input failsafe, the receiver output will provide an output High for this case.

Another fault condition can occur if the inputs get accidentally *shorted* (See Figure 4). Under the above condition, the receiver output will also be at logic High and not in an unknown state.

Another case could occur if the driver is either powered off, in TRI-STATE[®] or even removed from the line while the receiver stays powered on with inputs *terminated* by the 100Ω termination resistor.

The receiver output will provide a logic high under all the above mentioned conditions. Failsafe support is receiver device dependent, please refer to the specific LVDS receiver datasheets to determine which level of failsafe support is provided. Remember that the receiver function is to amplify very small (mV), short duration (ps-ns) pulses to rail-to-rail

CMOS levels. System design should ensure that noise picked up on the interconnect is seen as common and not differential. This can be accomplished by using balanced cables, shielding from noise sources and closely-coupled differential traces on PCBs.

POWER ON/OFF REQUIREMENTS and HIGH IMPEDANCE BUS PINS

Depending upon the application high impedance bus pin may or may not be required. This refers to the loading effect of driver outputs and receiver inputs when power is off to the device. First generation LVDS parts were intended for use in point-to-point applications. In this configuration, when the driver is OFF, disabled, or unplugged, the link is down and no communication occurs. The bus loading effects of the device is of minor concern. The DS90C031/DS90C032 family of devices have direct ESD protection pins on the bus pins. Even if a driver is active and a receiver is powered off, the output current is tightly limited and will not cause a latch-up condition to occur on the receiver input.

Second generation devices offered by National (DS90LV031A/DS90LV032A) are intended for a wider range of applications where high impedance bus pins may be required. For this family of devices, the ESD protection circuitry will not load the line when the device is powered off.

To determine if a device supports high impedance bus pins, refer to the features list in the device datasheet and also the

receiver input current parameters and the driver output leakage parameters. National's family of Bus LVDS parts also feature high impedance bus pins as they are intended for multi-drop and multi-point applications.

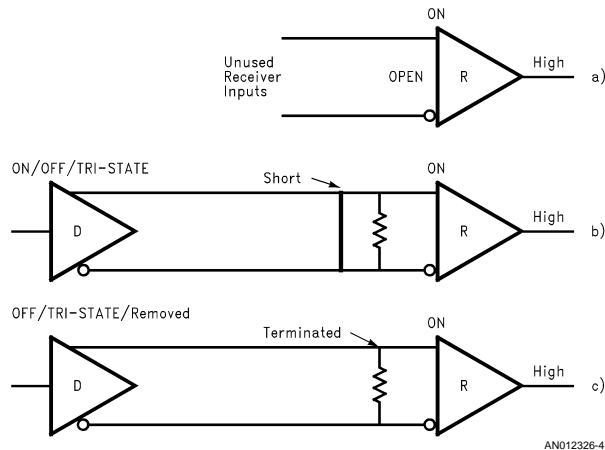


FIGURE 4. a, b, c. Failsafe Operation

POINT-TO-POINT CONFIGURATIONS

For interfaces where the transition time of the driver is substantially shorter than the time delay of the media, the interconnection must be considered a distributed load, not a lumped load. The distributed elements of a transmission line (media) can greatly affect signal quality.

More explicitly, transmission line theory dictates that if the transition (rise or fall) time of the driver is less than four times the line delay, the media must be treated as a distributed load, not a lumped load, and careful attention must be paid to any impedance discontinuities and stubs. For a given driver, if $t_r < 4 t_d$ (where t_r = driver rise time, t_d = delay of the line) then the line should be considered as a lossy line. This is usually true if the t_r of drivers are in the sub nanosecond range. A quick calculation will clarify this rule of thumb. For example, the DS90C031 driver has a typical t_r of 350 ps, and a microstrip built with FR-4 material has a t_d of 147 ps for one inch of PC trace. This calculates that, an inch of FR-4 microstrip will act as a transmission line ($350 < 4 * 147$) when driven by the DS90C031 driver. Figure 5 includes a stub between the termination resistor and the receiver input. This length must not be longer than one inch in length and should be kept as short as possible. Stub lengths of 1 inch or greater will cause the propagating signal to bounce off the high impedance end of the stubs and degrade the signal. Multiple reflections can travel up and down the line causing ringing, overshoot and undershoot which reduces the noise margin too.

The fast t_r of the DS90C031 allows the driver to achieve a higher bandwidth, but transmission line characteristics can easily crop up on a system board if not handled properly at these edge rates. To make the device work to its fullest capability, the LVDS DS90C031 and the DS90C032 should be op-

erated in a point-to-point configuration with minimum discontinuities on the transmission line. This ensures no stub problems on the line. The media **must** be terminated by a 100Ω line-to-line termination at the far end. A 100Ω termination resistor terminates the two differential line in its characteristic impedance and also provides the differential voltage (V_{OD}) for the current mode driver. Under the above conditions, the driver can drive a twp (twisted pair) wire over 10m at speeds in excess of 155.5 Mbps (77.7 MHz). Note that other LVDS devices offered by National support higher data rate operation. The FAST LVDS family of parts support 400 Mbps operation, and the Channel Link family of LVDS parts operate even faster on the LVDS lines.

BI-DIRECTIONAL APPLICATION ON ONE TWP

In a bi-directional application data can flow in only one direction at a time (see Figure 6) over the single twisted pair, however the bus needs to be terminated at both ends. This requires two 100Ω terminating resistors, assuming the cable impedance is 100Ω (one direction at a time). In Figure 6, Rt1 terminates the signal when D1 is driving, and Rt2 terminates the signal when D2 is driving. But, since the drivers are current mode (~4 mA) devices, the two resistors in parallel will load down the driver ($100\Omega \parallel 100\Omega = 50\Omega$) which cuts the signal in half. This reduces system noise margin to only 25 mV, as the minimum driver V_{OD} is now 125 mV, and the receiver threshold is 100 mV.

Since the driver output swing is severely attenuated due to dual parallel termination load, the bi-directional approach over one twp is not recommended with standard LVDS devices. Bus LVDS devices are recommended for use in applications that employ two terminations (see AN-1115).

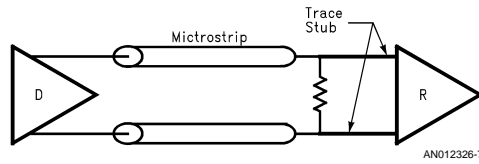


FIGURE 5. A Point-to-Point Configuration Using LVDS

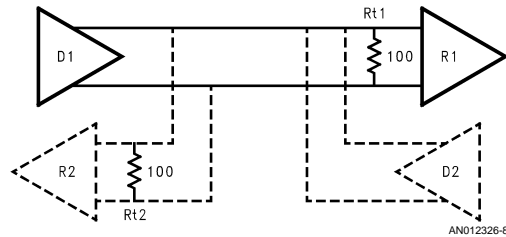


FIGURE 6. Bi-Directional Application over One Pair of Tw

MULTI-DROP CONFIGURATION

In a multi-drop configuration (see *Figure 7*), 10 receivers or more can be tied to the bus. Select an LVDS receiver that supports high impedance bus pins, if the devices use separate power supplies and some receivers may be powered off while communication is flowing from the driver to other powered up receivers. Also, the stubs between the line and each receiver have the potential to create reflections if they are too long, or cause an impedance discontinuity. Remember that only one termination resistor should be used and it must be located at the far end of the cable.

SIGNAL QUALITY ACROSS CABLE

There are numerous ways of determining signal quality on the transmission media. Bit Error Rate (BER), jitter, eye pattern, ratio of rise time and unit interval are some of the different ways designers use to determine signal quality. In this article, eye patterns will be used to demonstrate signal quality for LVDS driver and receiver.

In order to create an eye pattern, a PRBS (Pseudo Random Bit Sequence) of 511 ($2^9 - 1$) bits NRZ data was used to drive the LVDS driver inputs. The LVDS driver was con-

nected to a LVDS receiver with a 10m, 25 pair, 28AWG, twp cable (SCSI grade cable). The eye was plotted on the differential driver output at 155.5 Mbps and also at the receiver input at the end of the cable (see *Figure 8* and *Figure 9*).

A random data pattern is more prone to Inter Symbol Interference (ISI). There is a greater chance of errors occurring from inter symbol interference as the duration of pulses get shorter and shorter. A bit arriving at the receiver input might not have enough time to cross the threshold before the arrival of the next bit, resulting in lost data.

A PRBS with a pattern depth of 511 bits or 2047 ($2^{11} - 1$) or 32767 ($2^{15} - 1$) was used to generate the eye pattern. The eye pattern is then used to characterize inter symbol interference issues. The opening of the eye determines the signal quality, and jitter can be measured at the crossing point. Other industry standards, SONET/SDH for example, specifies eye patterns for signal quality analysis. LVDS technology demonstrates a wide eye opening at 155.5 Mbps over the 10m twp cable. Also refer to application note AN-808 "Long Transmission Line and Data Signal Quality" for more discussions on signal quality.

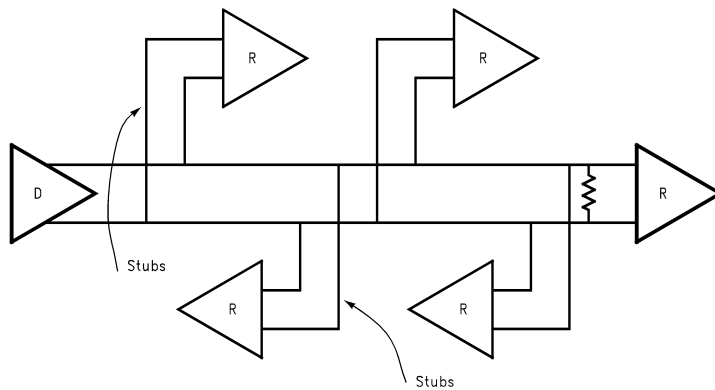


FIGURE 7. Multi-Drop Configuration for LVDS

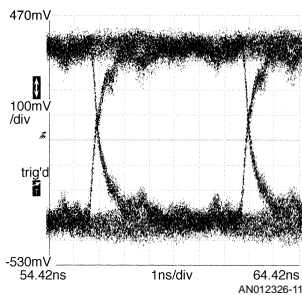


FIGURE 8. Eye Pattern at Driver Output

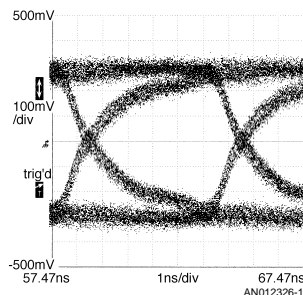


FIGURE 9. Eye Pattern at Receiver Inputs with 10m Cable

CONCLUSION

LVDS technology solves the ever increasing data rate problem while decreasing power dissipation and can be widely used in Telecom, Routers, Intelligent Hubs, LCD displays, Copiers and numerous other exciting applications. LVDS technology provides the best solution for power budget requirements in today's designs. This high speed interface allows designers to implement a simple point-to-point link without complex termination issues. Low power dissipation and the use of a core process allows for the integration of PLLs and digital blocks to provide optimized interface single chip solutions. LVDS technology provides solutions when Megabits at milliwatts are required.

REFERENCES

For TIA standards contact:
 Global Engineering Documents
<http://global.ihs.com/>

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弊社半導体製品の取り扱い・保管について

半導体製品は、取り扱い、保管・輸送環境、基板実装条件によっては、お客様での実装前後に破壊/劣化、または故障を起こすことがあります。

弊社半導体製品のお取り扱い、ご使用にあたっては下記の点を遵守して下さい。

1. 静電気

- 素手で半導体製品単体を触らないこと。どうしても触る必要がある場合は、リストストラップ等で人体からアースをとり、導電性手袋等をして取り扱うこと。
- 弊社出荷梱包単位（外装から取り出された内装及び個装）又は製品単品で取り扱いを行う場合は、接地された導電性のテーブル上で（導電性マットにアースをとったもの等）、アースをした作業者が行うこと。また、コンテナ等も、導電性のものを使うこと。
- マウンタやはんだ付け設備等、半導体の実装に関わる全ての装置類は、静電気の帯電を防止する措置を施すこと。
- 前記のリストストラップ・導電性手袋・テーブル表面及び実装装置類の接地等の静電気帯電防止措置は、常に管理されその機能が確認されていること。

2. 温・湿度環境

- 温度：0～40℃、相対湿度：40～85%で保管・輸送及び取り扱いを行うこと。（但し、結露しないこと。）

- 直射日光が当たる状態で保管・輸送しないこと。
3. 防湿梱包
 - 防湿梱包品は、開封後は個別推奨保管環境及び期間に従い基板実装すること。
 4. 機械的衝撃
 - 梱包品（外装、内装、個装）及び製品単品を落下させたり、衝撃を与えないこと。
 5. 熱衝撃
 - はんだ付け時は、最低限260℃以上の高温状態に、10秒以上さらさないこと。（個別推奨条件がある時はそれに従うこと。）
 6. 汚染
 - はんだ付け性を損なう、又はアルミ配線腐食の原因となるような汚染物質（硫黄、塩素等ハロゲン）のある環境で保管・輸送しないこと。
 - はんだ付け後は十分にフラックスの洗浄を行うこと。（不純物含有率が一定以下に保証された無洗浄タイプのフラックスは除く。）

以上