TPS256x デュアルチャネル、高精度、可変電流制限パワー・スイッチ

1 特長

- 2 つの独立した電流制限チャネル
- USB の電流制限要件に適合
- 調整可能な電流制限:250mA～2.8A (標準値)
- 2.8A において ±7.5% の電流制限精度
- 高速過電流応答:3.5µs (標準値)
- ハイサイド MOSFET:44mΩ × 2
- 動作範囲:2.5V～6.5V
- スタンバイ時電源電流:最大 2µA
- ソフトスタート機能内蔵
- システム・レベルの 15kV および 8kV ESD 耐性
- UL 認定済み:ファイル No. E169910
- CB および Nemko 認証

2 アプリケーション

- USB ポート / ハブ
- デジタル・テレビ
- セットトップ・ボックス
- VoIP 電話

3 概要

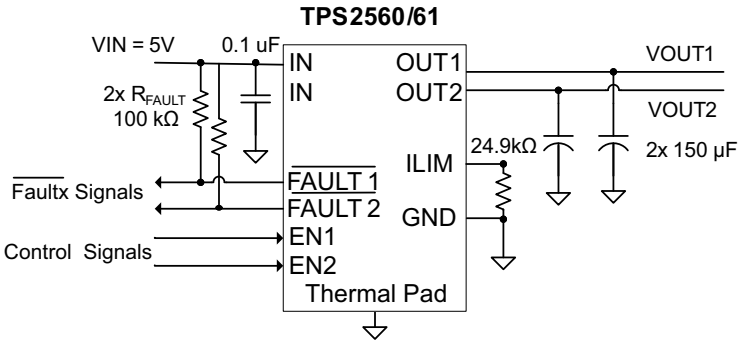
TPS2560 および TPS2561 (TPS256x) は、高精度な電流制限が必要なアプリケーション、大きな容量性負荷や短絡が発生する可能性のあるアプリケーション向けに設計された、デュアル・チャネルのパワー・ディストリビューション・スイッチです。電流制限スレッショルドは、外付け抵抗によりチャネル毎に 250mA～2.8A (標準値) の範囲でプログラミングできます。電源スイッチの立ち上がりおよび立ち下がり時間は、オン / オフ時の電流サージを最小限に抑えるように制御されます。

TPS256x の各チャネルでは、出力負荷が電流制限スレッショルドを超えた場合に、定電流モードに切り替えることで、出力電流を安全なレベルに制限します。過電流状態中および過熱状態中は、各チャネルの $\overline{\text{FAULTx}}$ 論理出力が独立して LOW にアサートされます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPS2560、TPS2561	VSON (10)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーションの図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

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- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- Added OUTx parameter to *Absolute Maximum Ratings* table ... 4

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- 「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1

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- Changed V_{ENx} to $V_{\overline{ENx}}$ in Recommended Operating Conditions ... 4
- Changed $V_{\overline{ENx}}$ to V_{ENx} in Recommended Operating Conditions ... 4

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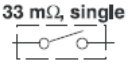
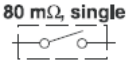
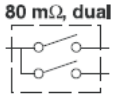
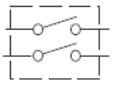
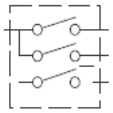
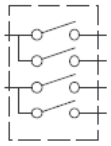
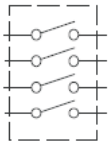
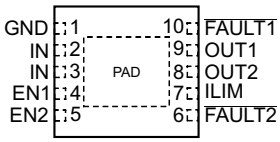
5 Device Comparison Table

GENERAL SWITCH CATALOG

33 mΩ, single	80 mΩ, single	80 mΩ, dual	80 mΩ, dual	80 mΩ, triple	80 mΩ, quad	80 mΩ, quad
						
TPS201xA 0.2 A - 2 A TPS202x 0.2 A - 2 A TPS203x 0.2 A - 2 A	TPS2014 600 mA TPS2015 1 A TPS2041B 500 mA TPS2051B 500 mA TPS2045A 250 mA TPS2049 100 mA TPS2055A 250 mA TPS2061 1 A TPS2065 1 A TPS2068 1.5 A TPS2069 1.5 A	TPS2042B 500 mA TPS2052B 500 mA TPS2046B 250 mA TPS2056 250 mA TPS2062 1 A TPS2066 1 A TPS2060 1.5 A TPS2064 1.5 A	TPS2080 500 mA TPS2081 500 mA TPS2082 500 mA TPS2090 250 mA TPS2091 250 mA TPS2092 250 mA	TPS2043B 500 mA TPS2053B 500 mA TPS2047B 250 mA TPS2057A 250 mA TPS2063 1 A TPS2067 1 A	TPS2044B 500 mA TPS2054B 500 mA TPS2048A 250 mA TPS2058 250 mA	TPS2085 500 mA TPS2086 500 mA TPS2087 500 mA TPS2095 250 mA TPS2096 250 mA TPS2097 250 mA

6 Pin Configuration and Functions



DRC Package, 10-Pin VSON, Top View

表 6-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	TPS2560	TPS2561		
$\overline{EN1}$	4	—	I	Enable input, logic low turns on channel one power switch.
EN1	—	4	I	Enable input, logic high turns on channel one power switch.
$\overline{EN2}$	5	—	I	Enable input, logic low turns on channel two power switch.
EN2	—	5	I	Enable input, logic high turns on channel two power switch.
GND	1	1	—	Ground connection; connect externally to the thermal pad.
IN	2, 3	2, 3	I	Input voltage; connect a 0.1 µF or greater ceramic capacitor from IN to GND as close to the IC as possible.
$\overline{FAULT1}$	10	10	O	Active-low open-drain output, asserted during overcurrent or overtemperature condition on channel one.
$\overline{FAULT2}$	6	6	O	Active-low open-drain output, asserted during overcurrent or overtemperature condition on channel two.
OUT1	9	9	O	Power-switch output for channel one.
OUT2	8	8	O	Power-switch output for channel two.
ILIM	7	7	O	External resistor used to set current-limit threshold; recommended 20 kΩ ≤ R_{ILIM} ≤ 187 kΩ.
Thermal pad	PAD	PAD	—	Internally connected to GND; used to heat-sink the part to the circuit board traces. Connect the thermal pad to GND pin externally.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
	Voltage on IN, ENx or $\overline{\text{ENx}}$, ILIM, $\overline{\text{FAULTx}}$	–0.3	7	V
	OUTx	–0.8	7	V
	Voltage from IN to OUTx	–7	7	V
	Continuous output current	Internally limited		–
	Continuous total power dissipation	See *Dissipation Ratings*		–
	Continuous $\overline{\text{FAULTx}}$ sink current		25	mA
	ILIM source current	Internally limited		–
T_J	Maximum junction temperature	–40	OTSD2(3)	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under the *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are referenced to GND unless otherwise noted.
(3) Ambient over temperature shutdown threshold.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings: Surge

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge(1)	±8000	V
		IEC 61000-4-2 air-gap discharge(1)	±15000	

(1) Surges per EN61000-4-2. 1999 applied to output terminals of EVM. These are passing test levels, not failure threshold.

7.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		6.5	V
$V_{\overline{ENx}}$	TPS2560 enable voltage	0		6.5	V
V_{ENx}	TPS2561 enable voltage	0		6.5	V
V_{IH}	High-level input voltage on ENx or $\overline{\text{ENx}}$	1.1			V
V_{IL}	Low-level input voltage on ENx or $\overline{\text{ENx}}$			0.66	V
I_{OUTx}	Continuous output current per channel	0		2.5	A
	Continuous $\overline{\text{FAULTx}}$ sink current	0		10	mA
R_{ILIM}	Recommended resistor limit	20		187	kΩ
T_J	Operating junction temperature	–40		125	°C

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7.5 Thermal Information

THERMAL METRIC[1]		TPS256x DRC (VSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Electrical Characteristics

over recommended operating conditions, $V_{/ENx}$ = 0 V, or V_{ENx} = V_{IN} (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	Static drain-source on-state resistance per channel, IN to OUTx	T_J = 25 °C			44	50	mΩ
		–40 °C ≤ T_J ≤ 125 °C				70	
t_r	Rise time, output	C_{Lx} = 1 µF, R_{Lx} = 100 Ω (see 図 8-1)	V_{IN} = 6.5 V	2	3	4	ms
			V_{IN} = 2.5 V	1	2	3	
t_f	Fall time, output	C_{Lx} = 1 µF, R_{Lx} = 100 Ω (see 図 8-1)	V_{IN} = 6.5 V	0.6	0.8	1.0	ms
			V_{IN} = 2.5 V	0.4	0.6	0.8	
ENABLE INPUT, EN OR $\overline{EN}$							
	Enable pin turn on/off threshold			0.66		1.1	V
	Hysteresis				55[2]		mV
I_{EN}	Input current	V_{ENx} = 0 V or 6.5 V, $V_{/ENx}$ = 0 V or 6.5 V		–0.5		0.5	µA
t_{on}	Turnon time	C_{Lx} = 1 µF, R_{Lx} = 100 Ω, (see 図 8-1)				9	ms
t_{off}	Turnoff time					6	ms
CURRENT LIMIT							
I_{OS}	Current-limit threshold per channel (Maximum DC output current I_{OUTx} delivered to load) and Short-circuit current, OUTx connected to GND	R_{ILIM} = 20 kΩ		2590	2800	3005	mA
		R_{ILIM} = 61.9 kΩ		800	900	1005	
		R_{ILIM} = 100 kΩ		470	560	645	
t_{IOS}	Response time to short circuit	V_{IN} = 5.0 V, (see 図 8-2)			3.5[2]		µs

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7.6 Electrical Characteristics (continued)

over recommended operating conditions, $V_{/ENx}$ = 0 V, or V_{ENx} = V_{IN} (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{IN_off}	Supply current, low-level output	V_{IN} = 6.5 V, no load on OUTx, $V_{\overline{ENx}}$ = 6.5 V or V_{ENx} = 0 V			0.1	2.0	µA
I_{IN_on}	Supply current, high-level output	V_{IN} = 6.5 V, no load on OUT	R_{ILIM} = 20 kΩ		100	125	µA
			R_{ILIM} = 100 kΩ		85	110	µA
I_{REV}	Reverse leakage current	V_{OUTx} = 6.5 V, V_{IN} = 0 V	T_J = 25°C		0.01	1.0	µA
UNDERVOLTAGE LOCKOUT							
UVLO	Low-level input voltage, IN	V_{IN} rising			2.35	2.45	V
	Hysteresis, IN	T_J = 25°C			35		mV
$\overline{FAULTx}$ FLAG							
V_{OL}	Output low voltage, $\overline{FAULTx}$	$I_{\overline{FAULTx}}$ = 1 mA				180	mV
	Off-state leakage	$V_{\overline{FAULTx}}$ = 6.5 V				1	µA
	$\overline{FAULTx}$ deglitch	$\overline{FAULTx}$ assertion or de-assertion due to overcurrent condition		6	9	13	ms
THERMAL SHUTDOWN							
OTSD2	Thermal shutdown threshold			155			°C
OTSD	Thermal shutdown threshold in current-limit			135			°C
	Hysteresis				20[2]		°C

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.
(2) These parameters are provided for reference only, and do not constitute part of TI's published specifications for purposes of TI's product warranty.

7.7 Dissipation Ratings

BOARD	PACKAGE	THERMAL RESISTANCE[2] $R_{\theta JA}$	THERMAL RESISTANCE $R_{\theta JC}$	$T_A \le 25°C$ POWER RATING
High-K[1]	DRC	41.6 °C/W	10.7 °C/W	2403 mW

(1) The JEDEC high-K (2s2p) board used to derive this data was a 3-in × 3-in, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.
(2) Mounting per the *PowerPAD™ Thermally Enhanced Package* application report.

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7.8 Typical Characteristics

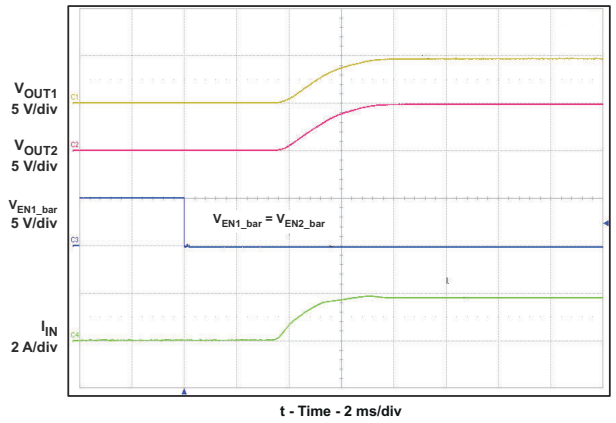

図 7-1. Turn-On Delay and Rise Time

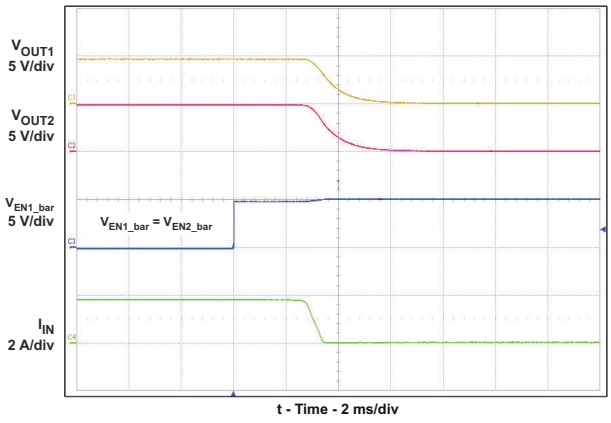

図 7-2. Turn-Off Delay and Fall Time

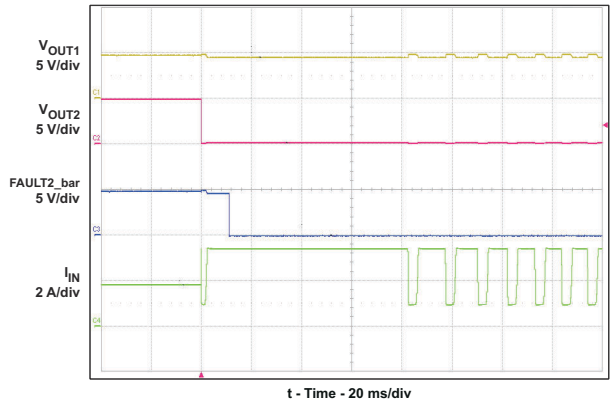

図 7-3. Full-Load to Short-Circuit Transient Response

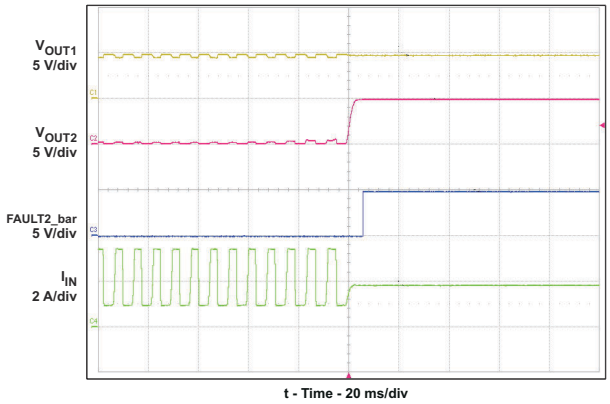

図 7-4. Short-Circuit to Full-Load Recovery Response

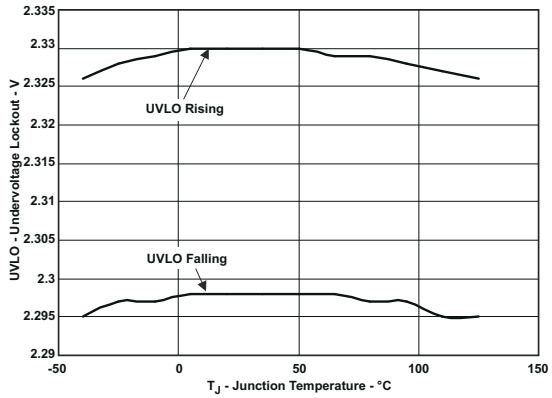

図 7-5. UVLO – Undervoltage Lockout – V

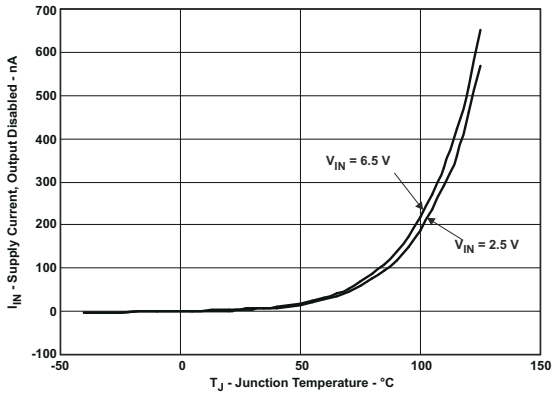

図 7-6. I_{IN} – Supply Current, Output Disabled – nA

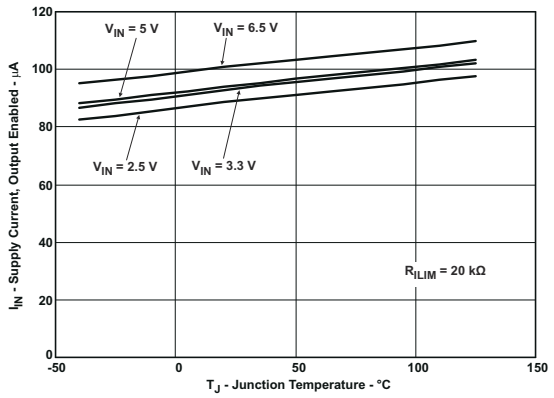

図 7-7. I_{IN} – Supply Current, Output Enabled – µA

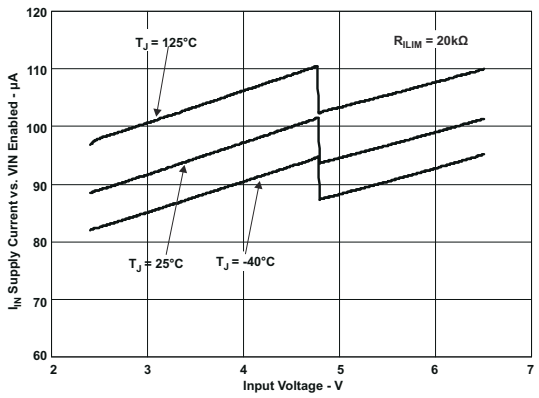

図 7-8. I_{IN} – Supply Current, Output Enabled – µA

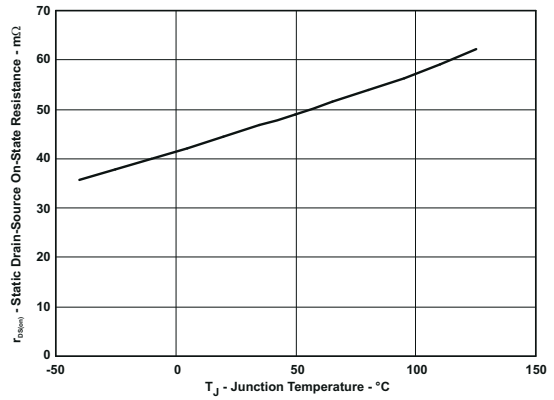

図 7-9. MOSFET $r_{DS(on)}$ vs Junction Temperature

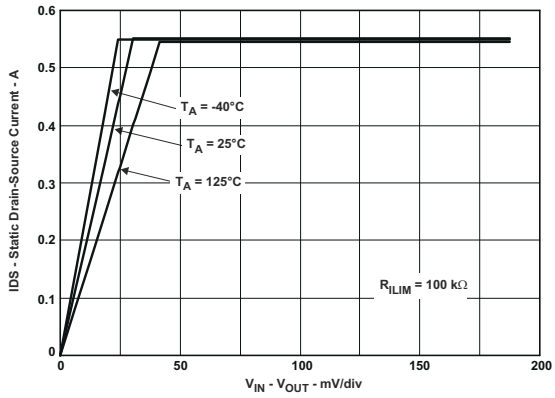

図 7-10. Switch Current vs Drain-Source Voltage Across Switch

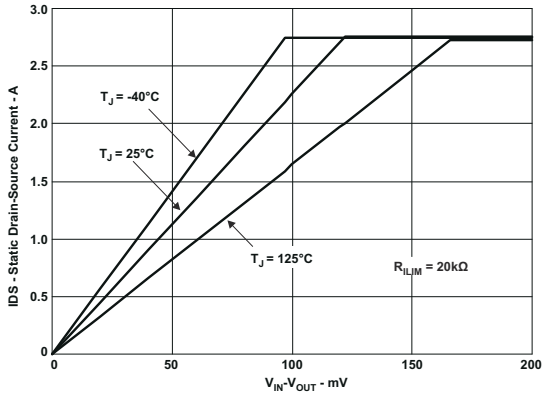

図 7-11. Switch Current vs Drain-Source Voltage Across Switch

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8 Parameter Measurement Information

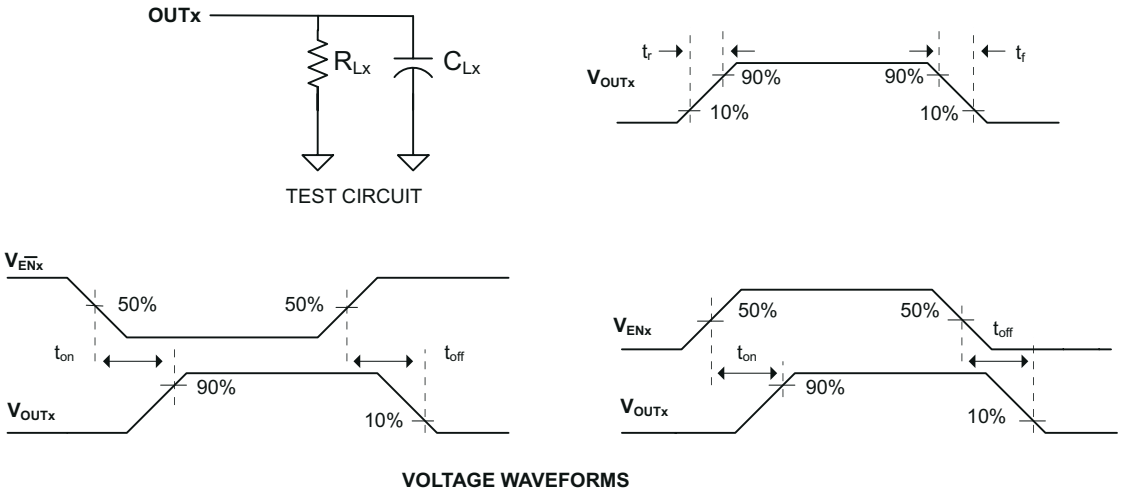


図 8-1. Test Circuit and Voltage Waveforms

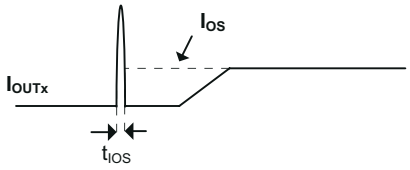


図 8-2. Response Time to Short Circuit Waveform

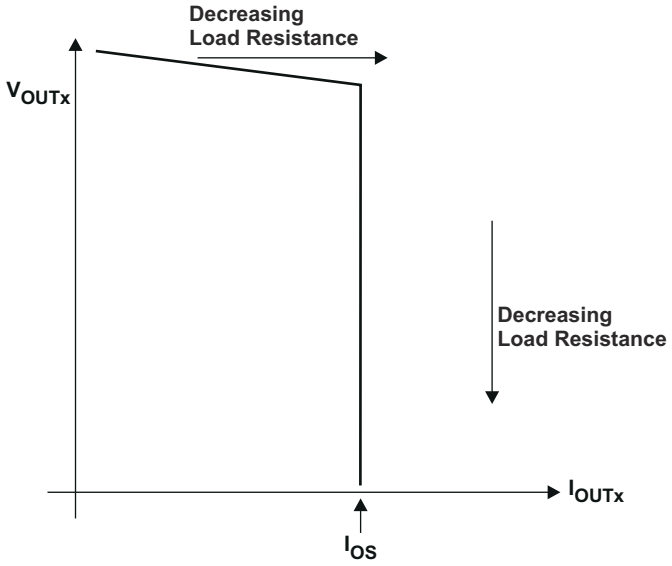


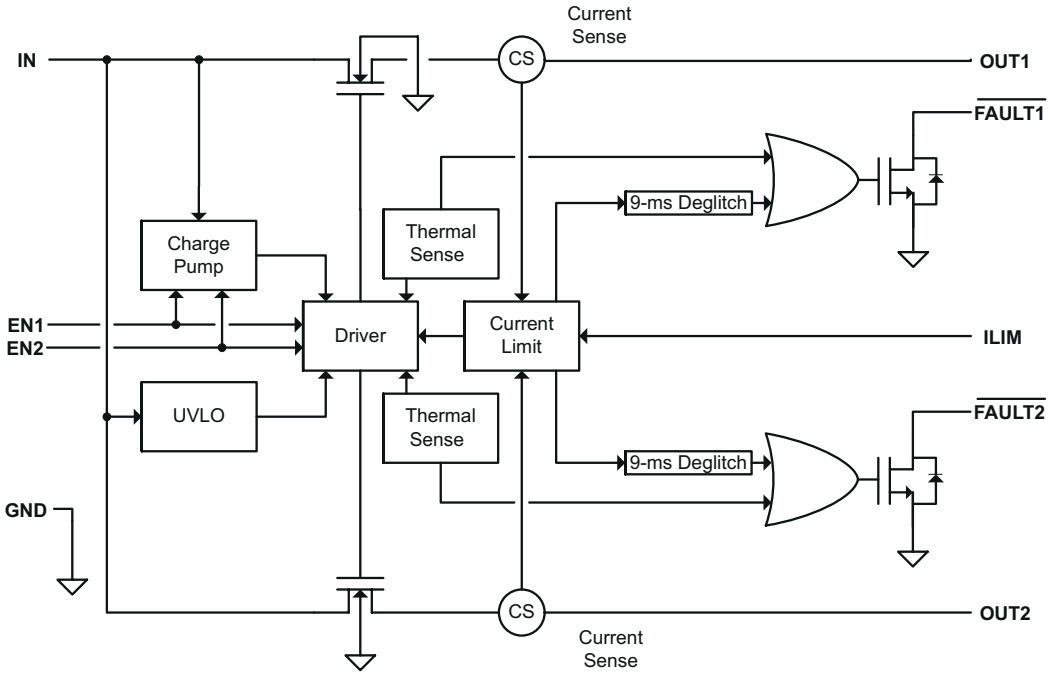
図 8-3. Output Voltage vs Current-Limit Threshold

9 Detailed Description

9.1 Overview

The TPS256x is a dual-channel, current-limited power-distribution switch using N-channel MOSFETs for applications where short circuits or heavy capacitive loads will be encountered. This device allows the user to program the current-limit threshold between 250 mA and 2.8 A (typ) per channel via an external resistor. This device incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFETs. The charge pump supplies power to the driver circuit for each channel and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.5 V and requires little supply current. The driver controls the gate voltage of the power switch. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges and provides built-in soft-start functionality. Each channel of the TPS256x limits the output current to the programmed current-limit threshold I_{OS} during an overcurrent or short-circuit event by reducing the charge pump voltage driving the N-channel MOSFET and operating it in the linear range of operation. The result of limiting the output current to I_{OS} reduces the output voltage at OUTx because the N-channel MOSFET is no longer fully enhanced.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Overcurrent Conditions

The TPS256x responds to overcurrent conditions by limiting the output current per channel to I_{OS}. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Two possible overload conditions can occur.

The first condition is when a short circuit or partial short circuit is present when the device is powered-up or enabled. The output voltage is held near zero potential with respect to ground and the TPS256x ramps the output current to I_{OS}. The TPS256x devices will limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The second condition is when a short circuit, partial short circuit, or transient overload occurs while the device is enabled and powered on. The device responds to the overcurrent condition within time t_{IOS} (see 図 8-2). The current-sense amplifier is overdriven during this time and momentarily disables the internal current-limit MOSFET. The current-sense amplifier recovers and ramps the output current to I_{OS}. Similar to the previous

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case, the TPS256x will limit the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

The TPS256x thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the above cases. The device turns off when the junction temperature exceeds 135°C (min) while in current limit. The device remains off until the junction temperature cools 20°C (typ) and then restarts. The TPS256x cycles on/off until the overload is removed (see 図 7-4).

9.3.2 $\overline{\text{FAULTx}}$ Response

The $\overline{\text{FAULTx}}$ open-drain outputs are asserted (active low) on an individual channel during an overcurrent or overtemperature condition. The TPS256x asserts the $\overline{\text{FAULTx}}$ signal until the fault condition is removed and the device resumes normal operation on that channel. The TPS256x is designed to eliminate false $\overline{\text{FAULTx}}$ reporting by using an internal delay "deglitch" circuit (9-ms typ) for overcurrent conditions without the need for external circuitry. This ensures that $\overline{\text{FAULTx}}$ is not accidentally asserted due to normal operation such as starting into a heavy capacitive load. The deglitch circuitry delays entering and leaving current-limited induced fault conditions. The $\overline{\text{FAULTx}}$ signal is not deglitched when the MOSFET is disabled due to an overtemperature condition but is deglitched after the device has cooled and begins to turn on. This unidirectional deglitch prevents $\overline{\text{FAULTx}}$ oscillation during an overtemperature event.

9.3.3 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables the power switch until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted on/off cycling due to input voltage droop during turn on.

9.3.4 Enable ($\overline{\text{ENx}}$ or ENx)

The logic enables control the power switches and device supply current. The supply current is reduced to less than 2-µA when a logic high is present on $\overline{\text{ENx}}$ or when a logic low is present on ENx. A logic low input on $\overline{\text{ENx}}$ or a logic high input on ENx enables the driver, control circuits, and power switches. The enable inputs are compatible with both TTL and CMOS logic levels.

9.3.5 Thermal Sense

The TPS256x self protects by using two independent thermal sensing circuits that monitor the operating temperature of the power switch and disable operation if the temperature exceeds recommended operating conditions. Each channel of the TPS256x operates in constant-current mode during an overcurrent conditions, which increases the voltage drop across the power switch. The power dissipation in the package is proportional to the voltage drop across the power switch, which increases the junction temperature during an overcurrent condition. The first thermal sensor (OTSD) turns off the individual power switch channel when the die temperature exceeds 135°C (min) and the channel is in current limit. Hysteresis is built into the thermal sensor, and the switch turns on after the device has cooled approximately 20°C.

The TPS256x also has a second ambient thermal sensor (OTSD2). The ambient thermal sensor turns off both power switch channels when the die temperature exceeds 155°C (min) regardless of whether the power switch channels are in current limit and will turn on the power switches after the device has cooled approximately 20°C. The TPS256x continues to cycle off and on until the fault is removed.

9.4 Device Functional Modes

There are no other functional modes.

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Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Auto-Retry Functionality

Some applications require that an overcurrent condition disables the part momentarily during a fault condition and re-enables after a pre-set time. This auto-retry functionality can be implemented with an external resistor and capacitor. During a fault condition, $\overline{\text{FAULTx}}$ pulls ENx low disabling the part. The part is disabled when ENx is pulled below the turn-off threshold, and $\overline{\text{FAULTx}}$ goes high impedance allowing C_{RETRY} to begin charging. The part re-enables when the voltage on ENx reaches the turn-on threshold, and the auto-retry time is determined by the resistor/capacitor time constant. The part will continue to cycle in this manner until the fault condition is removed.

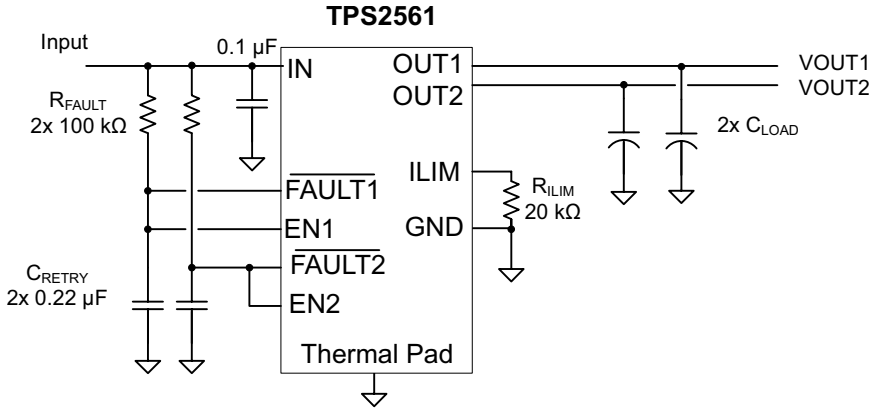

図 10-1. Auto-Retry Functionality

Some applications require auto-retry functionality and the ability to enable/disable with an external logic signal. The figure below shows how an external logic signal can drive EN through R_{FAULT} and maintain auto-retry functionality. The resistor/capacitor time constant determines the auto-retry time-out period.

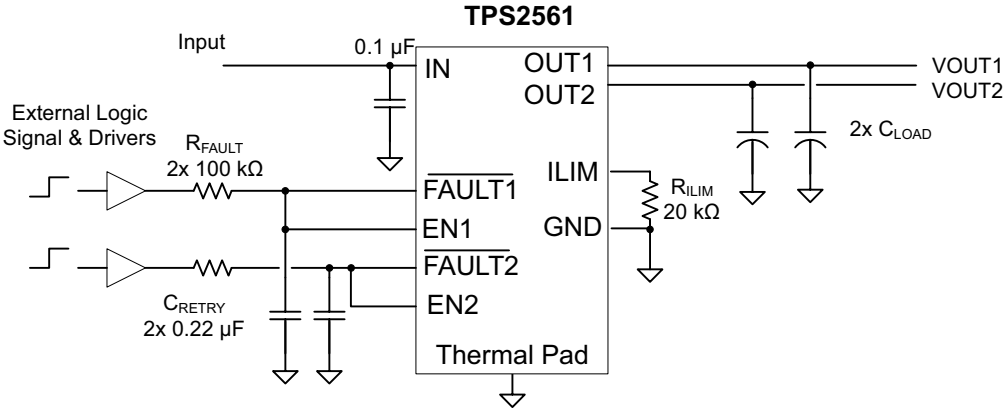

図 10-2. Auto-Retry Functionality With External EN Signal

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10.1.2 Two-Level Current-Limit Circuit

Some applications require different current-limit thresholds depending on external system conditions. 図 10-3 shows an implementation for an externally controlled, two-level current-limit circuit. The current-limit threshold is set by the total resistance from ILIM to GND (see previously discussed *Programming the Current-Limit Threshold* section). A logic-level input enables/disables MOSFET Q1 and changes the current-limit threshold by modifying the total resistance from ILIM to GND. Additional MOSFET/resistor combinations can be used in parallel to Q1/R2 to increase the number of additional current-limit levels.

Note

ILIM should never be driven directly with an external signal.

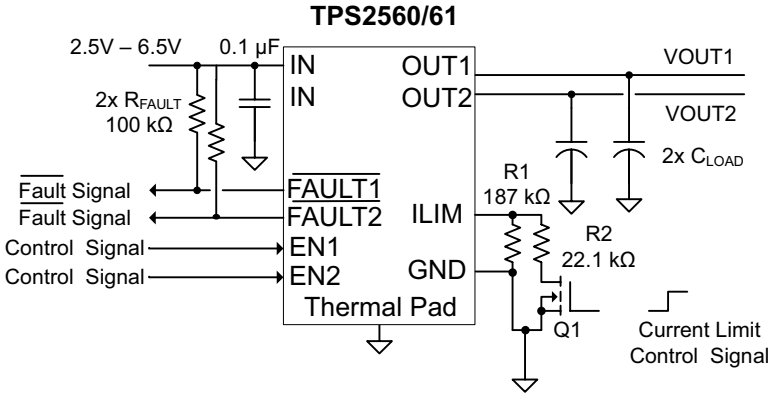

図 10-3. Two-Level Current-Limit Circuit

10.2 Typical Application

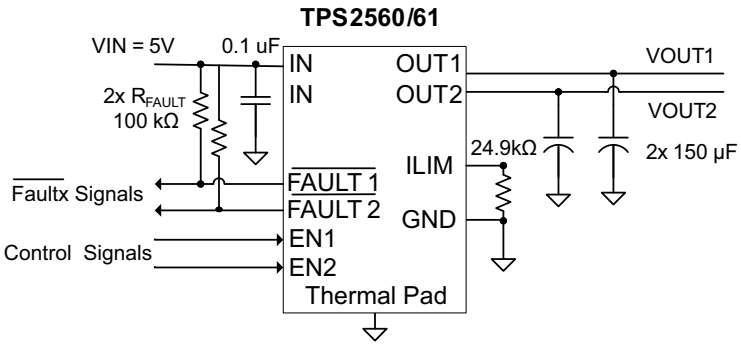

図 10-4. Typical Application Circuit

10.2.1 Design Requirements

See the design parameters in 表 10-1.

表 10-1. Design Parameters

PARAMETER	VALUE
Input voltage	5 V
Output voltage	5 V
Above a minimum current limit	2000 mA
Below a minimum current limit	1000 mA

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10.2.2 Detailed Design Procedure

10.2.2.1 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance should be optimized for the particular application. For all applications, a 0.1µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling. This precaution reduces ringing on the input due to power-supply transients. Additional input capacitance may be needed on the input to reduce voltage overshoot from exceeding the absolute maximum voltage of the device during heavy transient conditions. This is especially important during bench testing when long, inductive cables are used to connect the evaluation board to the bench power supply.

Output capacitance is not required, but placing a high-value electrolytic capacitor on the output pin is recommended when large transient currents are expected on the output.

10.2.2.2 Programming the Current-Limit Threshold

The overcurrent threshold is user programmable via an external resistor, R_{ILIM}. R_{ILIM} sets the current-limit threshold for both channels. The TPS256x use an internal regulation loop to provide a regulated voltage on the ILIM pin. The current-limit threshold is proportional to the current sourced out of ILIM. The recommended 1% resistor range for R_{ILIM} is 20 kΩ ≤ R_{ILIM} ≤ 187 kΩ to ensure stability of the internal regulation loop. Many applications require that the minimum current limit is above a certain current level or that the maximum current limit is below a certain current level, so it is important to consider the tolerance of the overcurrent threshold when selecting a value for R_{ILIM}. The following equations calculates the resulting overcurrent threshold for a given external resistor value (R_{ILIM}). The traces routing the R_{ILIM} resistor to the TPS256x should be as short as possible to reduce parasitic effects on the current-limit accuracy.

$$I_{OSmax}(mA) = \frac{52850V}{R_{ILIM}^{0.957}k\Omega}$$
$$I_{OSnom}(mA) = \frac{56000V}{R_{ILIM}k\Omega}$$
$$I_{OSmin}(mA) = \frac{61200V}{R_{ILIM}^{1.056}k\Omega} \quad (1)$$

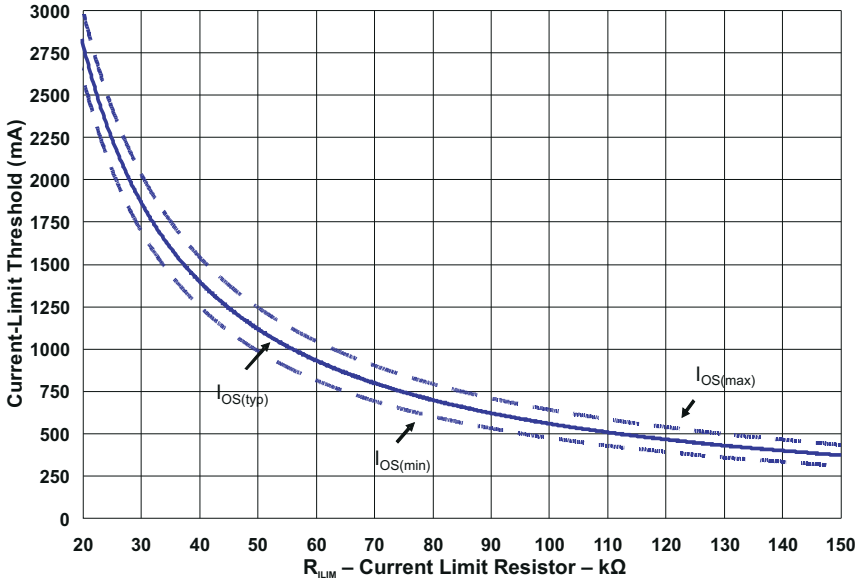

図 10-5. Current-Limit Threshold vs R_{ILIM}

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10.2.2.3 Application 1: Designing Above a Minimum Current Limit

Some applications require that current limiting cannot occur below a certain threshold. For this example, assume that 2 A must be delivered to the load so that the minimum desired current-limit threshold is 2000 mA. Use the I_{OS} equations and 図 10-5 to select R_{ILIM}.

$$I_{OSmin}(mA) = 2000mA$$
$$I_{OSmin}(mA) = \frac{61200V}{R_{ILIM}{}^{1.056}k\Omega}$$
$$R_{ILIM}(k\Omega) = \left(\frac{61200V}{I_{OSmin}mA}\right)^{\frac{1}{1.056}}$$
$$R_{ILIM}(k\Omega) = 25.52k\Omega \quad (2)$$

Select the closest 1% resistor less than the calculated value: R_{ILIM} = 25.5 kΩ. This sets the minimum current-limit threshold at 2 A . Use the I_{OS} equations, 図 10-5, and the previously calculated value for R_{ILIM} to calculate the maximum resulting current-limit threshold.

$$R_{ILIM}(k\Omega) = 25.5k\Omega$$
$$I_{OSmax}(mA) = \frac{52850V}{R_{ILIM}{}^{0.957}k\Omega}$$
$$I_{OSmax}(mA) = \frac{52850V}{25.5^{0.957}k\Omega}$$
$$I_{OSmax}(mA) = 2382mA \quad (3)$$

The resulting maximum current-limit threshold is 2382 mA with a 25.5-kΩ resistor.

10.2.2.4 Application 2: Designing Below a Maximum Current Limit

Some applications require that current limiting must occur below a certain threshold. For this example, assume that the desired upper current-limit threshold must be below 1000 mA to protect an up-stream power supply. Use the I_{OS} equations and 図 10-5 to select R_{ILIM}.

$$I_{OSmax}(mA) = 1000mA$$
$$I_{OSmax}(mA) = \frac{52850V}{R_{ILIM}{}^{0.957}k\Omega}$$
$$R_{ILIM}(k\Omega) = \left(\frac{52850V}{I_{OSmax}mA}\right)^{\frac{1}{0.957}}$$
$$R_{ILIM}(k\Omega) = 63.16k\Omega \quad (4)$$

Select the closest 1% resistor greater than the calculated value: R_{ILIM} = 63.4 kΩ. This sets the maximum current-limit threshold at 1000 mA . Use the I_{OS} equations, 図 10-5, and the previously calculated value for R_{ILIM} to calculate the minimum resulting current-limit threshold.

$$R_{ILIM}(k\Omega) = 63.4k\Omega$$
$$I_{OSmin}(mA) = \frac{61200V}{R_{ILIM}{}^{1.056}k\Omega}$$
$$I_{OSmin}(mA) = \frac{61200V}{63.4^{1.056}k\Omega}$$
$$I_{OSmin}(mA) = 765mA \quad (5)$$

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The resulting minimum current-limit threshold is 765 mA with a 63.4 kΩ resistor.

10.2.2.5 Accounting for Resistor Tolerance

The previous sections described the selection of R_{ILIM} given certain application requirements and the importance of understanding the current-limit threshold tolerance. The analysis focused only on the TPS256x performance and assumed an exact resistor value. However, resistors sold in quantity are not exact and are bounded by an upper and lower tolerance centered around a nominal resistance. The additional R_{ILIM} resistance tolerance directly affects the current-limit threshold accuracy at a system level. The following table shows a process that accounts for worst-case resistor tolerance assuming 1% resistor values. Step one follows the selection process outlined in the application examples above. Step two determines the upper and lower resistance bounds of the selected resistor. Step three uses the upper and lower resistor bounds in the I_{OS} equations to calculate the threshold limits. It is important to use tighter tolerance resistors, e.g. 0.5% or 0.1%, when precision current limiting is desired.

表 10-2. Common R_{ILIM} Resistor Selections

DESIRED NOMINAL CURRENT LIMIT	IDEAL RESISTOR	CLOSEST 1% RESISTOR	1% LOW RESISTOR TOLERANCE	1% HIGH RESISTOR TOLERANCE	IOS ACTUAL LIMITS			
					MIN	NOM	MAX	UNIT
300 mA	186.7 kΩ	187 kΩ	185.1 kΩ	188.9 kΩ	241.6	299.5	357.3	mA
400 mA	140.0 kΩ	140 kΩ	138.6 kΩ	141.4 kΩ	328.0	400.0	471.4	mA
600 mA	93.3 kΩ	93.1 kΩ	92.2 kΩ	94.0 kΩ	504.6	601.5	696.5	mA
800 mA	70.0 kΩ	69.8 kΩ	69.1 kΩ	70.5 kΩ	684.0	802.3	917.6	mA
1000 mA	56.0 kΩ	56.2 kΩ	55.6 kΩ	56.8 kΩ	859.9	996.4	1129.1	mA
1200 mA	46.7 kΩ	46.4 kΩ	45.9 kΩ	46.9 kΩ	1052.8	1206.9	1356.3	mA
1400 mA	40.0 kΩ	40.2 kΩ	39.8 kΩ	40.6 kΩ	1225.0	1393.0	1555.9	mA
1600 mA	35.0 kΩ	34.8 kΩ	34.5 kΩ	35.1 kΩ	1426.5	1609.2	1786.2	mA
1800 mA	31.1 kΩ	30.9 kΩ	30.6 kΩ	31.2 kΩ	1617.3	1812.3	2001.4	mA
2000 mA	28.0 kΩ	28 kΩ	27.7 kΩ	28.3 kΩ	1794.7	2000.0	2199.3	mA
2200 mA	25.5 kΩ	25.5 kΩ	25.2 kΩ	25.8 kΩ	1981.0	2196.1	2405.3	mA
2400 mA	23.3 kΩ	23.2 kΩ	23.0 kΩ	23.4 kΩ	2188.9	2413.8	2633.0	mA
2600 mA	21.5 kΩ	21.5 kΩ	21.3 kΩ	21.7 kΩ	2372.1	2604.7	2831.9	mA
2800 mA	20.0 kΩ	20 kΩ	19.8 kΩ	20.2 kΩ	2560.4	2800.0	3034.8	mA

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10.2.3 Application Curves

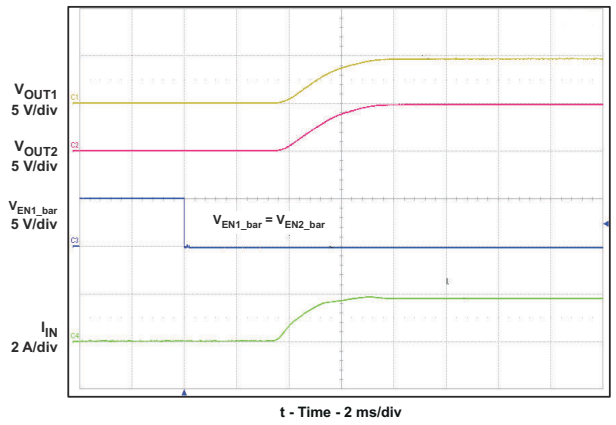

図 10-6. Turn-On Delay and Rise Time

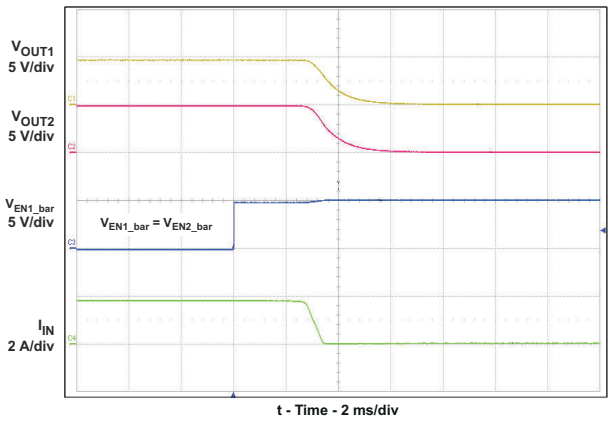

図 10-7. Turn-Off Delay and Fall Time

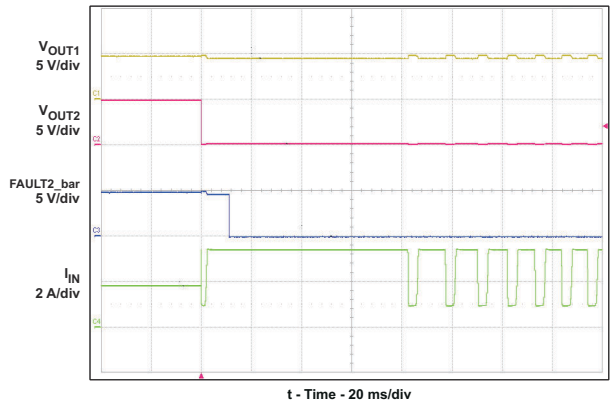

図 10-8. Full-Load to Short-Circuit Transient Response

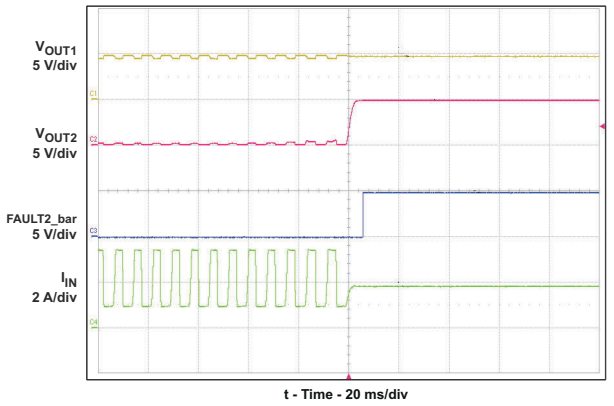

図 10-9. Short-Circuit to Full-Load Recovery Response

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10 Power Supply Recommendations

10.1 Self-Powered and Bus-Powered Hubs

A SPH has a local power supply that powers embedded functions and downstream ports. This power supply must provide between 4.75 V to 5.25 V to downstream facing devices under full-load and no-load conditions. SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs. A BPH obtains all power from an upstream port and often contains an embedded function. It must power up with less than 100 mA. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This is accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than 100 mA. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

10.2 Low-Power Bus-Powered and High-Power Bus-Powered Functions

Both low-power and high-power bus-powered functions obtain all power from upstream ports. Low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting.

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11 Layout

11.1 Layout Guidelines

- Place the 100-nF bypass capacitor near the IN and GND pins, and make the connections using a low-inductance trace
- Place a high-value electrolytic capacitor and a 100-nF bypass capacitor on the output pin is recommended when large transient currents are expected on the output
- The traces routing the RILIM resistor to the device should be as short as possible to reduce parasitic effects on the current limit accuracy
- The thermal pad should be directly connected to PCB ground plane using wide and short copper trace

11.1.1 Power Dissipation

The low on-resistance of the N-channel MOSFET allows small surface-mount packages to pass large currents. It is good design practice to estimate power dissipation and junction temperature. The below analysis gives an approximation for calculating junction temperature based on the power dissipation in the package. However, it is important to note that thermal analysis is strongly dependent on additional system level factors. Such factors include air flow, board layout, copper thickness and surface area, and proximity to other devices dissipating power. Good thermal design practice must include all system level factors in addition to individual component analysis.

Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from the typical characteristics graph. Using this value, the power dissipation can be calculated with 式 6. This step calculates the total power dissipation of the N-channel MOSFET.

$$P_D = (R_{DS(on)} \times I_{OUT1}{}^2) + (R_{DS(on)} \times I_{OUT2}{}^2) \quad (6)$$

where

- P_D = Total power dissipation (W)
- $r_{DS(on)}$ = Power switch on-resistance of one channel (Ω)
- I_{OUTx} = Maximum current-limit threshold set by R_{ILIM}(A)

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Finally, calculate the junction temperature with 式 7.

$$T_J = P_D \times R_{\theta JA} + T_A \quad (7)$$

where

- T_A = Ambient temperature (°C)
- $R_{\theta JA}$ = Thermal resistance (°C/W)
- P_D = Total power dissipation (W)

Compare the calculated junction temperature with the initial estimate. If they are not within a few degrees, repeat the calculation using the "refined" $r_{DS(on)}$ from the previous calculation as the new estimate. Two or three iterations are generally sufficient to achieve the desired result. The final junction temperature is highly dependent on thermal resistance $R_{\theta JA}$, and thermal resistance is highly dependent on the individual package and board layout. The *Dissipation Ratings* table provides example thermal resistances for specific packages and board layouts.

11.2 Layout Example

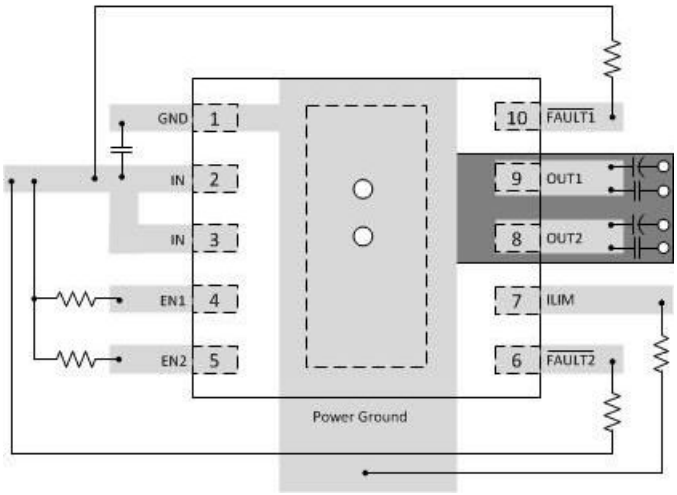

図 11-1. Layout Recommendation

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12 Device and Documentation Support

12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

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12.5 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2560DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2560	Samples
TPS2560DRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2560	Samples
TPS2561DRCR	ACTIVE	VSON	DRC	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2561	Samples
TPS2561DRCT	ACTIVE	VSON	DRC	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2561	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS2561 :

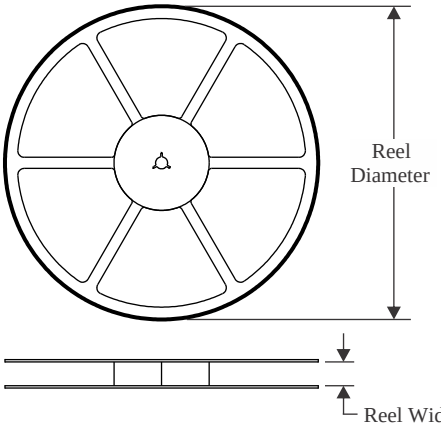
- Automotive : TPS2561-Q1

NOTE: Qualified Version Definitions:

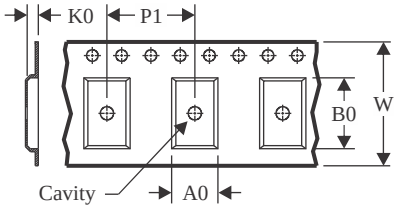
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

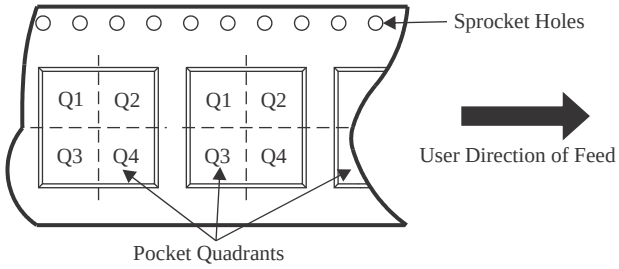


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

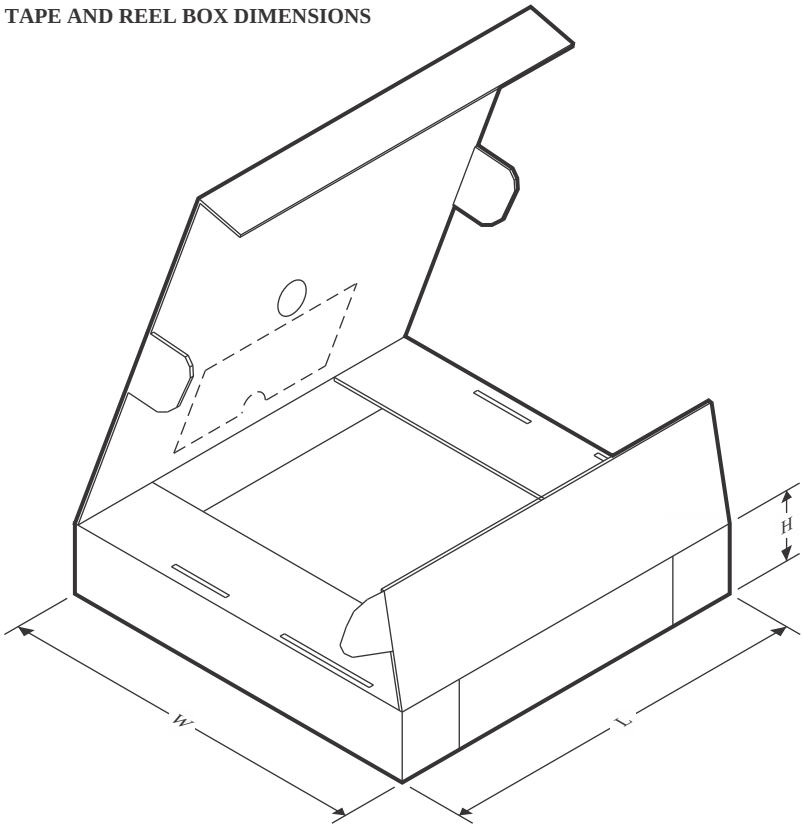
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2560DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2560DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2561DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS2561DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2560DRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS2560DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS2561DRCR	VSON	DRC	10	3000	346.0	346.0	33.0
TPS2561DRCT	VSON	DRC	10	250	182.0	182.0	20.0

GENERIC PACKAGE VIEW

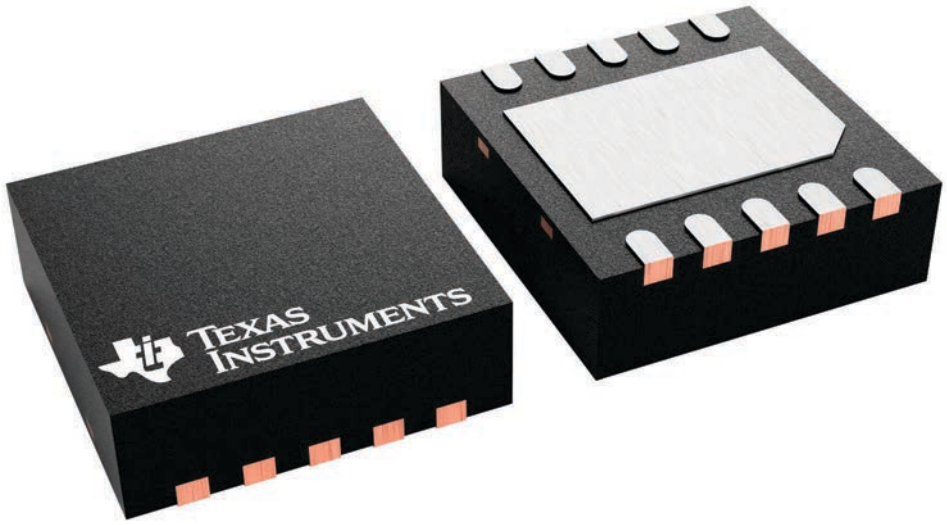
DRC 10

VSON - 1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



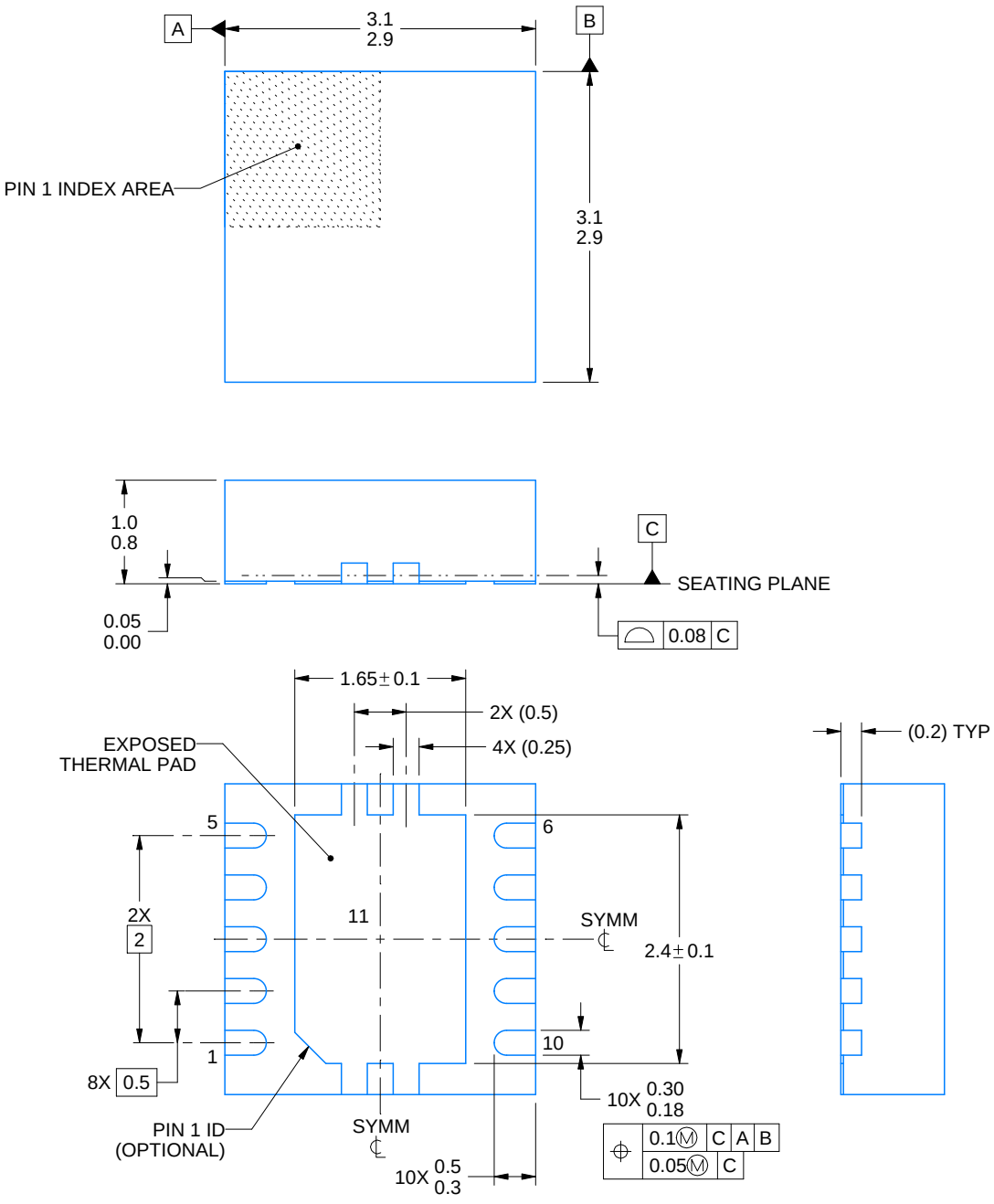
4226193/A

DRC0010J

PACKAGE OUTLINE

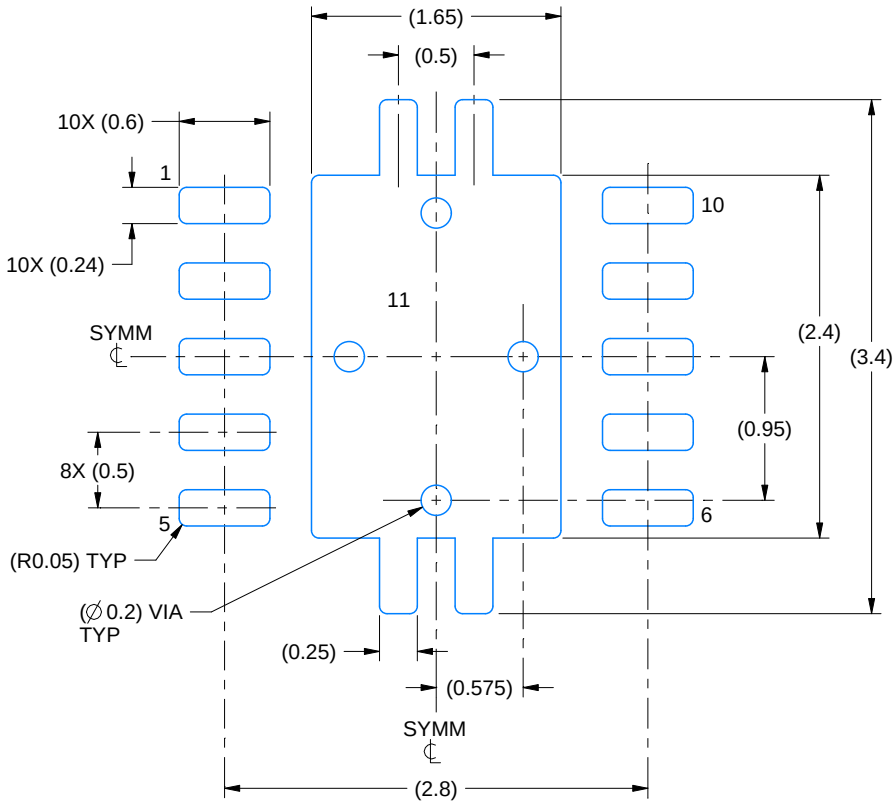
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

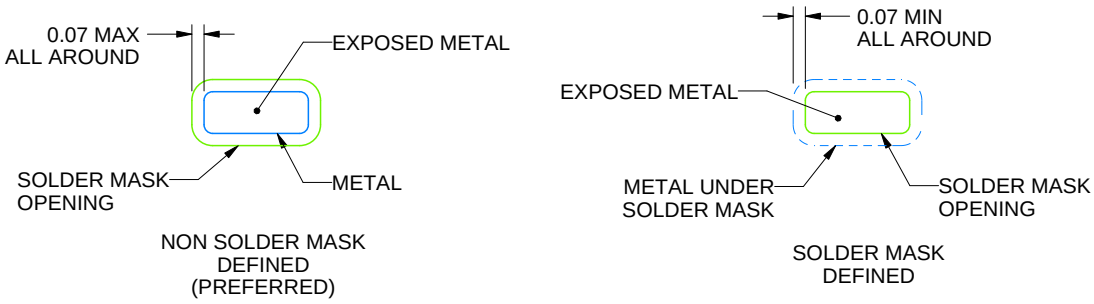


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

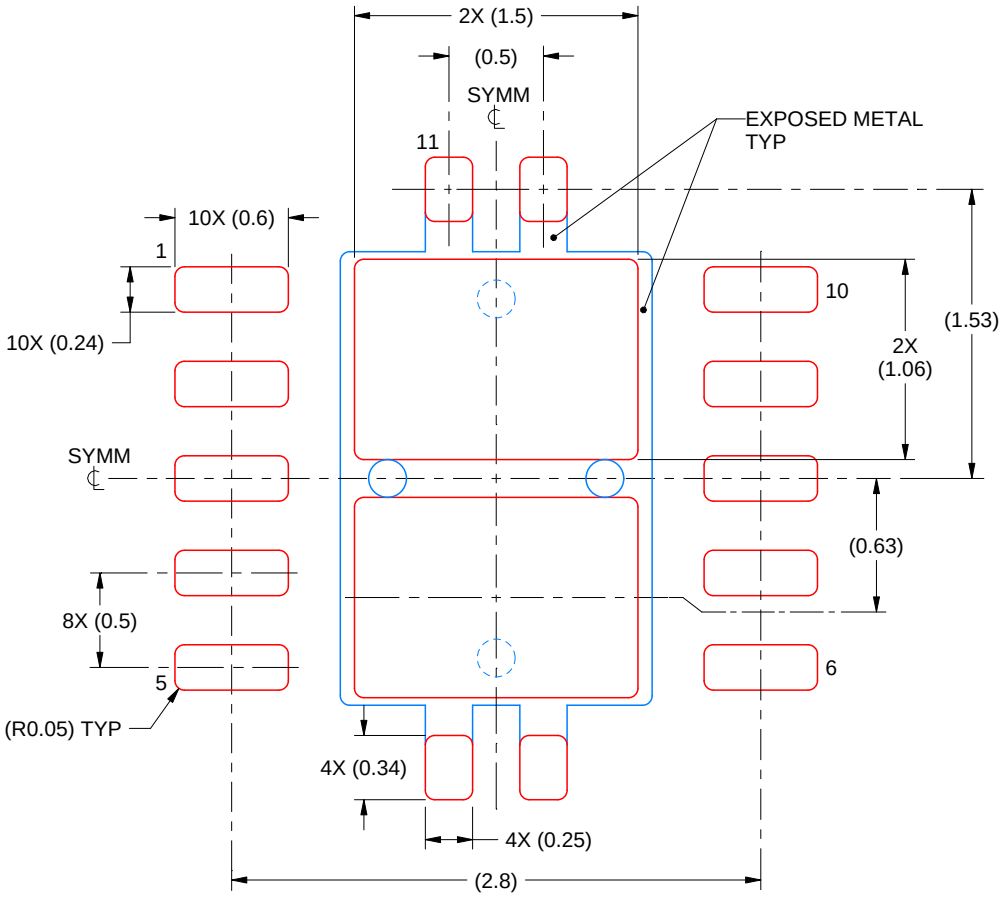
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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