

# TPS7B67xx-Q1 450mA、高電圧、超低 $I_Q$ 、低ドロップアウト・レギュレータ

## 1 特長

- 車載アプリケーション用に認定済み
- 下記内容でAEC-Q100認定済み
  - デバイス温度グレード1: 動作時周囲温度範囲  $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
  - デバイスHBM ESD分類レベルH2
  - デバイスCDM ESD分類レベルC3B
- 4V~40Vの広い $V_{IN}$ 入力電圧範囲、最大45Vの過渡電圧に対応
- 最大出力電流: 450mA
- 低消費電流( $I_Q$ )
  - EN = LOW (シャットダウン・モード)のとき4 $\mu\text{A}$ 未満
  - 軽負荷時15 $\mu\text{A}$ (typ.)
- 低ESR (0.001~20 $\Omega$ )のセラミック出力安定コンデンサ( $V_O \geq 2.5\text{V}$ のとき10 $\mu\text{F} \sim 500\mu\text{F}$ 、 $V_O = 1.5\text{V} \sim 2.5\text{V}$ のとき22 $\mu\text{F} \sim 500\mu\text{F}$ )
- 400mAでの最大ドロップアウト電圧450mV
- 1.5V~18Vの可変出力電圧
- 低電圧入力保護機能(UVLO)
- パワーオン・リセット機能を搭載
  - プログラム可能なりセット・パルス遅延
  - オープン・ドレイン・リセット出力
- フォルト保護機能を内蔵
  - 過熱保護機能
  - 短絡保護機能

- 20ピンHTSSOPパッケージ

## 2 アプリケーション

- 車載
- インフォテインメント・チューナ電源
- 車体制御モジュール
- 常時オンのバッテリー・アプリケーション
  - ゲートウェイ・アプリケーション
  - リモート・キーレス・エントリ・システム
  - イモビライザー

## 3 概要

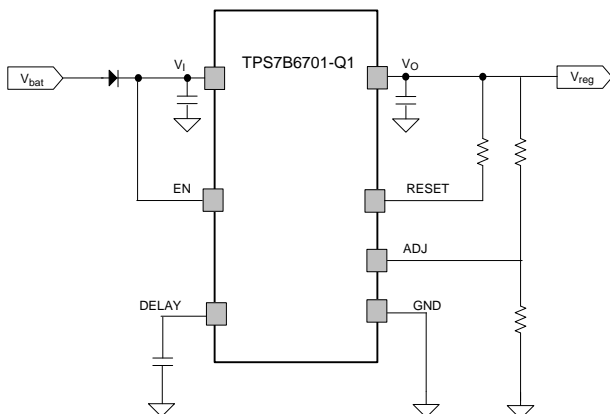
TPS7B6701-Q1、TPS7B6733-Q1、およびTPS7B6750-Q1デバイス(TPS7B67xx-Q1)は、最大40Vの $V_{IN}$ で動作するよう設計された、低ドロップアウトのリニア・レギュレータです。軽負荷時には静止電流がわずかに15 $\mu\text{A}$ であるため、車載バッテリーの持続時間を大幅に延長可能で、最大450mAの負荷を駆動できます。

### 製品情報<sup>(1)</sup>

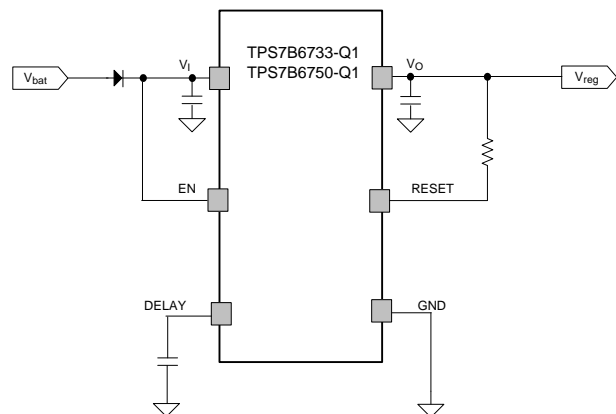
型番	パッケージ	本体サイズ(typ)
TPS7B6701-Q1	HTSSOP (20)	6.50mmx4.40mm
TPS7B6733-Q1		
TPS7B6750-Q1		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### 可変出力オプション



### 固定出力オプション



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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision C (December 2014) から Revision D に変更	Page
• Added <i>Dropout Recovery</i> section explaining LDO behavior when exiting dropout	18

Revision B (March 2014) から Revision C に変更	Page
• TPS7B6750A-Q1およびTPS7B6750B-Q1デバイスとDDPAKパッケージをデータシートから 削除	1
• Changed the word <i>terminal</i> to <i>pin</i> throughout the data sheet	5
• Changed the <i>Handling Ratings</i> table to <i>ESD Ratings</i> and moved the storage temperature into the <i>Absolute Maximum Ratings</i> table. Added corner pin values for CDM ratings.	6

Revision A (November 2013) から Revision B に変更	Page
• 表紙を更新し、以下の記述を追加: 「製品情報」表、デバイスのファミリ名をドキュメントのタイトルに追加、ナビゲーション・ボタンを追加	1
• 「特長」リストで、EN = LOWのときの $I_Q$ の値を2未満から4未満へ 変更	1
• 「改訂履歴」を2ページへ移動、「目次」を追加	4
• Replaced the <i>ORDERING INFORMATION</i> table with the <i>Device Comparison</i> Table and deleted the Device and Package columns	5
• Added Moved all electrical specifications tables and the <i>Typical Characteristics</i> section into the <i>Specifications</i> section	6
• Changed the max value for DELAY from $V_I$ to 45 V in the <i>Absolute Maximum Ratings</i> table. Also added new table note for DELAY	6
• Changed the max value for ADJ, RESET from $V_O$ to 22 V in the <i>Absolute Maximum Ratings</i> table	6
• Changed the value of $I_O$ from 1 mA to 450 mA for the Input voltage test conditions in the <i>Electrical Characteristics</i> table	7
• Added the value for $V_I$ in the test conditions of the Regulated output and the Line regulator parameters in the <i>Electrical Characteristics</i> table	7
• Moved the timing parameters (TIMING FOR RESET) out of the <i>Electrical Characteristics</i> table and into the new <i>Timing Requirements</i> table	8

• Added the <i>Overview</i> section title to the first paragraph of the <i>Detailed Description</i> section .....	12
• Updated the <i>Power-On_Reset (RESET)</i> section by making the following changes: changed the percentage that $V_O$ exceeds for the reset output to change from 90% to 91.6% (also changed this value in the <i>Reset Delay Timer (DELAY)</i> section), removed <i>The on-chip oscillator presets the delay</i> , and changed the percentage level to assert the output from 90% to 89.6%.....	13
• Changed the junction temperature value that disables thermal protection from 170°C to 175°C in the <i>Thermal Protection</i> section .....	15
• Added the <i>Device Functional Modes</i> section .....	15
• Added the <i>Typical Application</i> section in the new <i>Applications and Implementation</i> section .....	16
• Added the <i>Power Supply Recommendations</i> section .....	18
• Changed the <i>LAYOUT INFORMATION</i> section to the <i>Layout</i> section and added the <i>Layout Example</i> section.....	20
• 追加「メカニカル、パッケージ、および注文情報」セクション。また、「デバイスおよびドキュメントのサポート」セクションを追加し、商標情報と「静電放電に関する注意事項」を記載。このセクションには、新たにTI用語集への参照も記載.....	23

**2013年10月発行のものから更新**
**Page**

• 「 <i>特長</i> 」リストで最大ドロップアウト電圧を500mVから450mVへ 変更 .....	1
• 「 <i>アプリケーション</i> 」リストに車体制御モジュールを 追加 .....	1
• 可変出力と固定出力のオプションの相違を示すため、代表的なアプリケーションの回路図を 変更 .....	1
• 「 <i>概要</i> 」セクションで低電圧トラッキング機能のテキストをイネーブル機能のテキストに 変更.....	4
• ドキュメントのステータスを製品プレビューから量産データへ 変更 .....	4
• Changed the MIN value for RESET and ADJ in the <i>RECOMMENDED OPERATING CONDITIONS</i> table from 0 to 1.5 and removed low voltage parameter for those pins .....	6
• Added Added board dimensions to the high K profile <i>THERMAL INFORMATION</i> table note.....	6
• Changed test condition for the input voltage to fixed 3.3-V output and added 5-V and two adjustable output conditions ....	7
• Changed max value for the line regulation parameter from 2 to 10 .....	7
• Changed TYP value for dropout voltage where $I_O = 400$ mA from 240 to 260 .....	7
• Changed TYP value for dropout voltage where $I_O = 200$ mA from 160 to 150 .....	7
• Changed Output current-limit typ value to max value for $V_{OUT}$ short to ground .....	7
• Deleted $V_{IN}$ condition from test condition for PSRR .....	7
• Added <i>TYPICAL CHARACTERISTICS</i> section.....	9
• Added the <i>DETAILED DESCRIPTION</i> section.....	12
• Added block diagram fro the TPS7B6733-Q1 and TPS7B6750-Q1.....	12
• Added the <i>APPLICATION INFORMATION</i> section.....	16
• Added the <i>LAYOUT INFORMATION</i> section .....	20

## 5 概要 (続き)

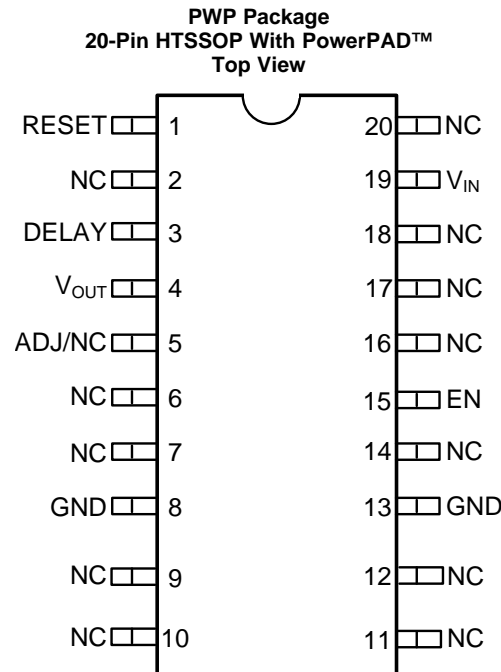
TPS7B67xx-Q1ファミリのデバイスは、短絡保護および過電流保護を内蔵しています。パワーアップ時にはリセット遅延とパワー・グッド信号が使用され、出力電圧が安定していてレギュレーション範囲内であることを示します。遅延時間は外付けコンデンサでプログラミングできます。イネーブル機能により、MCUからI/Oポート経由でデバイスのイネーブル/ディセーブルを制御できます。

このデバイス・ファミリは、-40°C～125°Cの温度範囲で動作します。

## 6 Device Comparison

ORDERABLE PART NUMBER	VOLTAGE OPTION (V <sub>OUT</sub> )
TPS7B6701QPWPRQ1	Adjustable 1.5 V to 18 V
TPS7B6733QPWPRQ1	Fixed 3.3 V
TPS7B6750QPWPRQ1	Fixed 5 V

## 7 Pin Configuration and Functions



### Pin Functions

PIN		TYPE	DESCRIPTION
NAME	PWP		
ADJ	5	I	Feedback pin. This pin is used with an external resistor divider or the NC pin when in a fixed version.
DELAY	3	O	Reset pulse delay adjustment. Connect this pin through a capacitor to GND.
EN	15	I	Enable pin. When the EN pin becomes lower than threshold, the device enters the stand-by state.
GND	8, 13	G	Ground reference
NC	2, 6, 7, 9, 10, 11, 12, 14, 16, 17, 18, 20	—	Not connected
RESET	1	O	Output ready. This open-drain pin must be connected to V <sub>OUT</sub> through an external resistor. RESET is pulled down when the output voltage goes below threshold.
V <sub>IN</sub>	19	P	Input power-supply voltage
V <sub>OUT</sub>	4	P	Output voltage
PowerPAD™		—	Thermal pad

## 8 Specifications

### 8.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Unregulated input range <sup>(2)(3)(4)</sup>	V <sub>IN</sub> , EN	-0.3	45	V
Output range	V <sub>OUT</sub>	-0.3	22	V
	DELAY <sup>(2)(3)(5)</sup>		45	
	ADJ, RESET		22	
Operating junction temperature (T <sub>J</sub> )		-40	150	°C
Storage temperature (T <sub>stg</sub> )		-65	150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Absolute negative voltage on these pins does not go below -0.3 V.
- (4) Absolute maximum voltage.
- (5) The voltage at the DELAY pin must be lower than the V<sub>IN</sub> voltage.

### 8.2 ESD Ratings

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)(2)</sup>	±2000	V	
		Charged-device model (CDM), per AEC Q100-011	All pins		±500
			Corner pins (1, 10, 11, and 20)		±750

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
- (2) The human body model is a 107-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

### 8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Unregulated input range	V <sub>IN</sub>	4	40	V
Output range	EN, DELAY	0	40	V
	V <sub>OUT</sub> , RESET, ADJ	1.5	18	
T <sub>J</sub>	Operating junction temperature range	-40	150	°C

### 8.4 Thermal Information

THERMAL METRIC <sup>(1)(2)</sup>		TPS7B67xx-Q1	UNIT
		PWP (HTSSOP)	
		20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	44.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	27.4	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	23.6	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.1	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	23.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	3.1	°C/W

- (1) The thermal data is based on JEDEC standard high K profile — JESD 51-7. Two signal, two plane, four-layer board with 2-oz copper. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.
- (2) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 8.5 Electrical Characteristics

 $V_I = 14\text{ V}$ ,  $1\text{ m}\Omega < \text{ESR} < 20\ \Omega$ ,  $T_J = -40^\circ\text{C}$  to  $150^\circ\text{C}$  unless otherwise stated

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT			
<b>SUPPLY VOLTAGE AND CURRENT (<math>V_{IN}</math>)</b>								
$V_I$	Input voltage	Fixed 3.3-V output, $I_O = 0\text{ mA}$ to $450\text{ mA}$		4	40	V		
		Fixed 5-V output, $I_O = 0\text{ mA}$ to $450\text{ mA}$		5.5	40			
		Adjustable output, $V_O \leq 3.5\text{ V}$ , $I_O = 0\text{ mA}$ to $450\text{ mA}$		4	40			
		Adjustable output, $V_O \geq 3.5\text{ V}$ , $I_O = 0\text{ mA}$ to $450\text{ mA}$		$V_O + 0.5$	40			
$I_Q$	Quiescent current	$V_I = 5.5\text{ V}$ to $40\text{ V}$ (fixed $5\text{ V}$ ), $4\text{ V}$ to $40\text{ V}$ (fixed $3.3\text{ V}$ ), $\text{EN} = \text{ON}$ , $I_O = 0.2\text{ mA}$		15	25	$\mu\text{A}$		
		$V_I = 4\text{ V}$ to $40\text{ V}$ (adjustable version, $V_O = 1.5\text{ V}$ ), $\text{EN} = \text{ON}$ , $I_O = 0.2\text{ mA}$		15	25			
		$V_I = 18.5\text{ V}$ to $40\text{ V}$ (adjustable version, $V_O = 18\text{ V}$ ), $\text{EN} = \text{ON}$ , $I_O = 0.2\text{ mA}$		25	35			
$I_{\text{Sleep}}$	Input sleep current	NO load current and $\text{EN} = \text{OFF}$			4	$\mu\text{A}$		
$I_{\text{EN}}$	EN pin current	$\text{EN} = 40\text{ V}$			1	$\mu\text{A}$		
$V_{\text{bg}}$	Band gap	Reference voltage for ADJ			-2%	1.233	2%	V
$V_{\text{INUVLO}}$	Undervoltage detection	Ramp $V_I$ down until output is turned OFF					2.6	V
$\text{UVLO}_{\text{Hys}}$	Undervoltage detection hysteresis					1		V
<b>ENABLE INPUT (EN)</b>								
$V_{\text{IL}}$	Logic input low level				0		0.4	V
$V_{\text{IH}}$	Logic input high level				1.7			V
<b>REGULATED OUTPUT (<math>V_{\text{OUT}}</math>)</b>								
$V_O$	Regulated output <sup>(1)</sup>	$V_I = V_O + 0.5\text{ V}$ to $40\text{ V}$ and $V_I \geq 4\text{ V}$ , $I_O = 0\text{ mA}$ to $450\text{ mA}$			-2%		2%	
$\Delta V_{\text{O}(\Delta\text{VI})}$	Line regulation	$V_I = V_O + 1\text{ V}$ to $40\text{ V}$ and $V_I \geq 4\text{ V}$ , $I_O = 100\text{ mA}$ , $\Delta V_O$					10	mV
$\Delta V_{\text{O}(\Delta\text{IL})}$	Load regulation	$I_O = 1\text{ mA}$ to $450\text{ mA}$ , $\Delta V_O$					10	mV
$V_{\text{dropout}}$	Dropout voltage	$V_I - V_O$ , $I_O = 400\text{ mA}$				240	450	mV
		$V_I - V_O$ , $I_O = 200\text{ mA}$				160	300	
$I_O$	Output current	$V_O$ in regulation			0		450	mA
$I_{\text{reg-CL}}$	Output current-limit	$V_O$ short to ground			140		360	mA
		$V_O = V_O$ typical $\times 0.9$			470		850	
PSRR	Power-supply ripple rejection <sup>(2)</sup>	$I_L = 100\text{ mA}$ , $C_O = 22\ \mu\text{F}$	Freq = 100 Hz		60		dB	
			Freq = 100 kHz		40			
<b>RESET</b>								
$V_{\text{OL}}$	Reset pulled low	$I_{\text{OL}} = 0.5\text{ mA}$					0.4	V
$I_{\text{OH}}$	Reset pulled $V_{\text{OUT}}$ through $10\text{-k}\Omega$ resistor	Leakage current					1	$\mu\text{A}$
$V_{\text{TH(POR)}}$	Power-on-reset threshold	$V_O$ power-up set tolerance			89.6	91.6	93.6	% of $V_{\text{OUT}}$
$V_{\text{hys}}$	Hysteresis	$V_O$ power-down set tolerance				2		% of $V_{\text{OUT}}$
<b>RESET DELAY</b>								
$I_{\text{Chg}}$	Delay capacitor charging current	$R_{\text{delay}} = 0\text{ V}$			6	9.5	14	$\mu\text{A}$
$V_{\text{th}}$	Threshold to release RESET high					1		V
<b>OPERATING TEMPERATURE RANGE</b>								
$T_J$	Junction temperature				-40		150	$^\circ\text{C}$
$T_{\text{sd}}$	Junction shutdown temperature					175		$^\circ\text{C}$
$T_{\text{hys}}$	Hysteresis of thermal shutdown					24		$^\circ\text{C}$

(1) External resistor divider variation is not considered.

(2) Design information — not tested, ensured by characterization.

## 8.6 Timing Requirements

			MIN	TYP	MAX	UNIT
<b>TIMING FOR RESET</b>						
t <sub>POR</sub>	Power-on reset delay	Where C = delay-capacitor value capacitance, C = 100 nF <sup>(1)</sup>		10.5		ms
t <sub>POR-fixed</sub>	Power-on reset delay	No capacitor on pin	100	325	550	μs
t <sub>Deglitch</sub>	Reset deglitch time		55	180	420	μs

(1) This information only will NOT be tested in production. The equation is based on:  
 $(C \times 1) / (9.5 \times 10^{-6}) = t_{\text{Delay}}$  (delay time)

Where

- C = delay capacitor value capacitance
- C range = 100 pf to 500 nF



### 8.7 Typical Characteristics

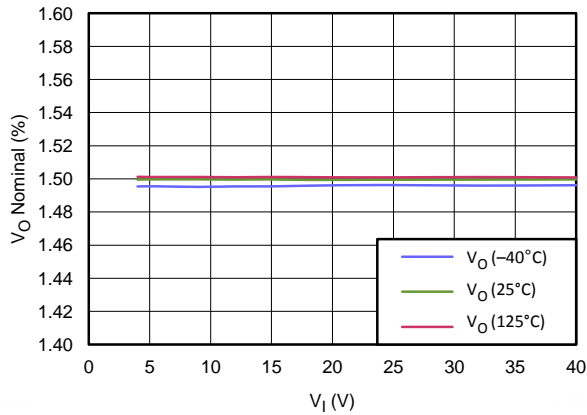


Figure 1. Line Regulation  
(V<sub>O</sub> = 1.5 V, I<sub>L</sub> = 100 mA)

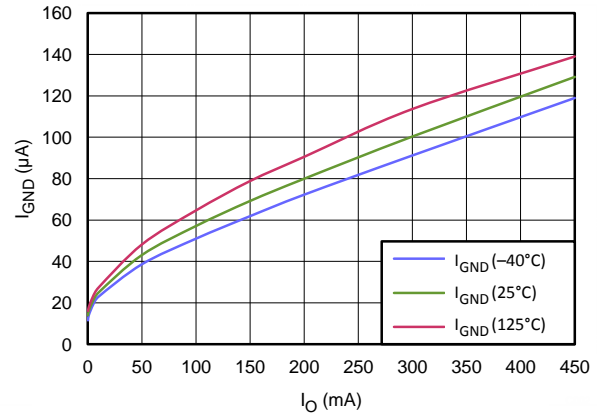


Figure 2. Ground Current vs Output Current  
(V<sub>I</sub> = 14 V, V<sub>O</sub> = 1.5 V)

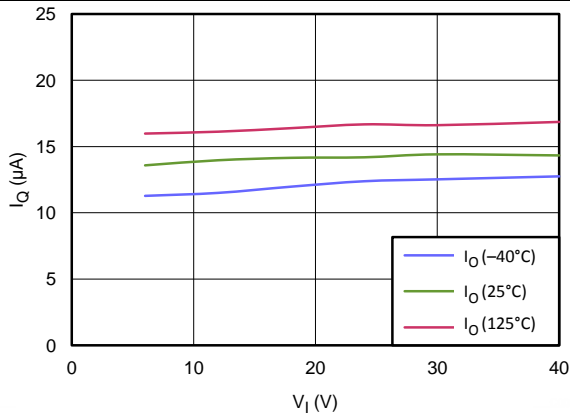


Figure 3. Quiescent Current vs Input Voltage  
(V<sub>O</sub> = 1.5 V)

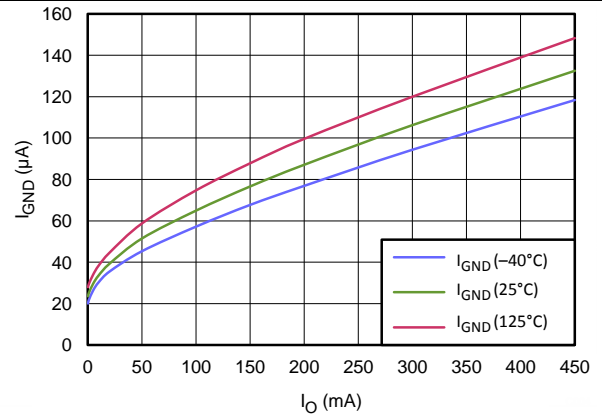


Figure 4. Ground Current vs Output Current  
(V<sub>I</sub> = 24 V, V<sub>O</sub> = 18 V)

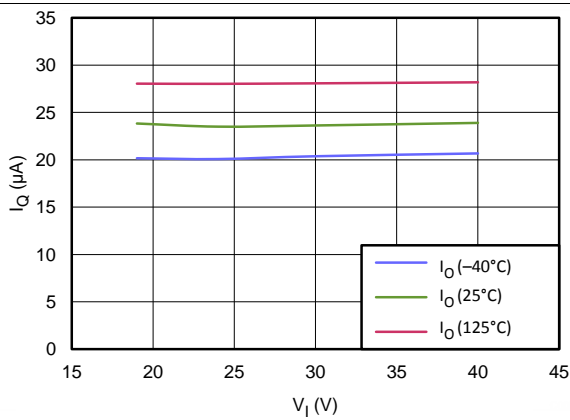


Figure 5. Quiescent Current vs Input Voltage  
(V<sub>O</sub> = 18 V)

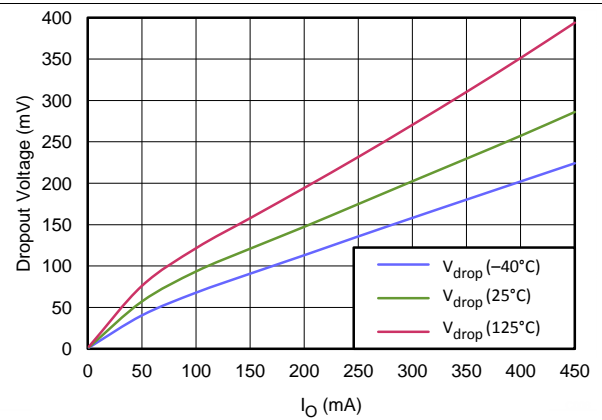


Figure 6. Dropout Voltage vs Output Current

Typical Characteristics (continued)

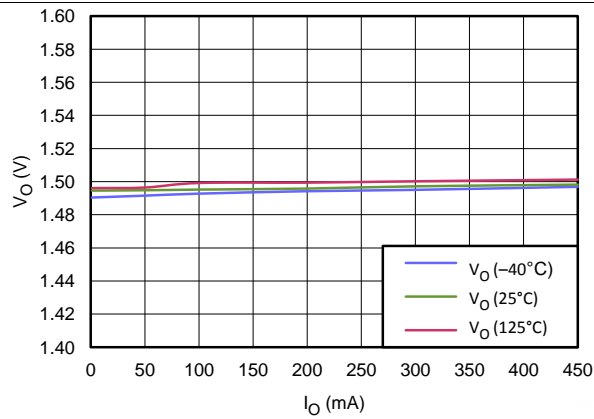


Figure 7. Load Regulation  
 ( $V_I = 14\text{ V}$ ,  $V_O = 1.5\text{ V}$ )

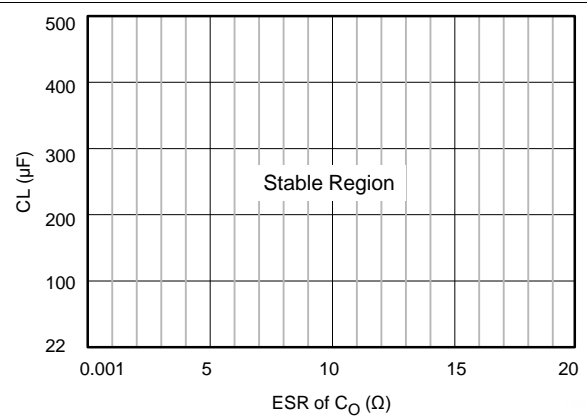


Figure 8. ESR Stability vs Load Capacitance  
 ( $V_O \leq 2.5\text{ V}$ )

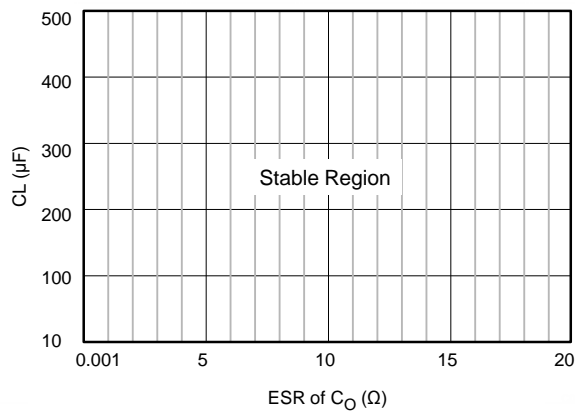


Figure 9. ESR Stability vs Load Capacitance  
 ( $V_O \geq 2.5\text{ V}$ )

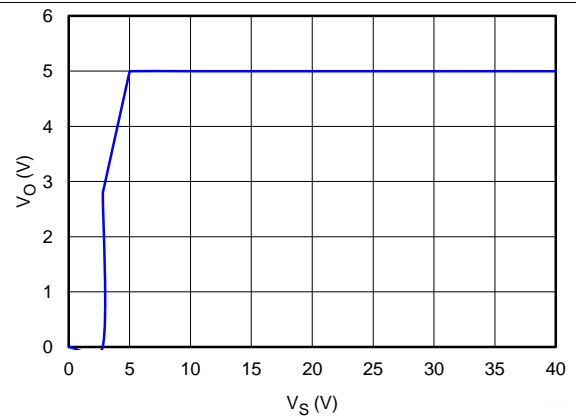


Figure 10. Output Voltage vs Supply Voltage  
 (Fixed 5-V Version,  $I_L = 0$ )

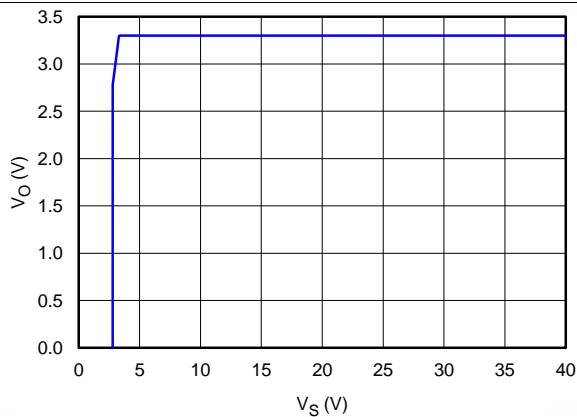


Figure 11. Output Voltage vs Supply Voltage  
 (Fixed 3.3-V Version,  $I_L = 0$ )

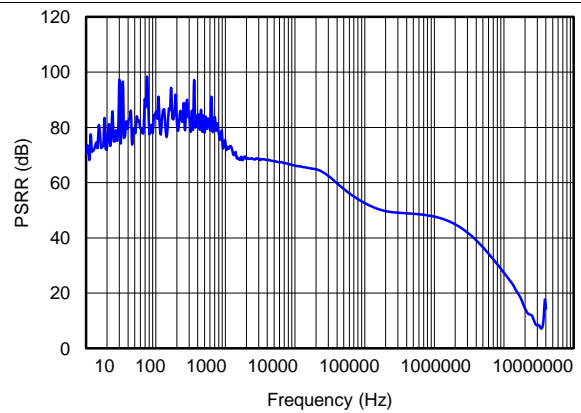


Figure 12. Power-Supply Rejection Ratio vs Frequency  
 ( $V_I = 14\text{ V}$ ,  $C_O = 47\ \mu\text{F}$ ,  $I_L = 25\text{ mA}$ )

Typical Characteristics (continued)

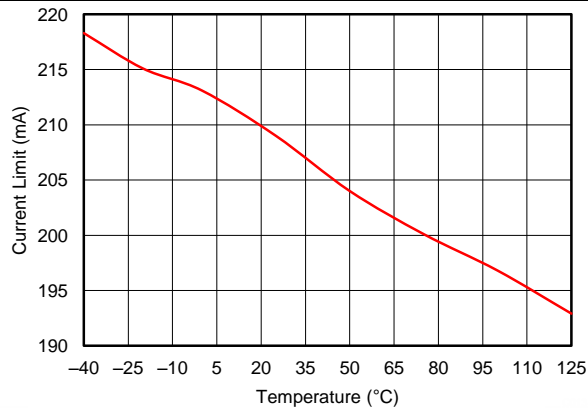


Figure 13. Short to GND Current-Limit vs Temperature

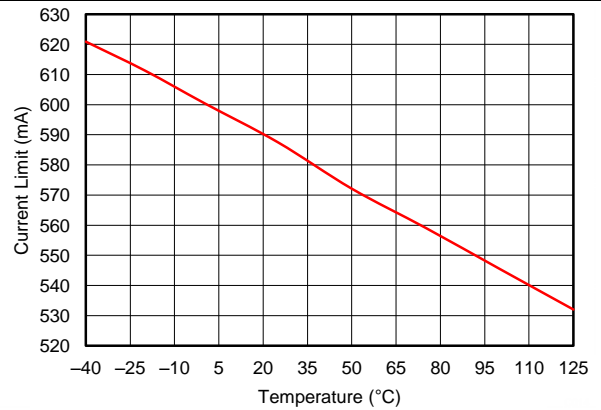


Figure 14. Current-Limit vs Temperature

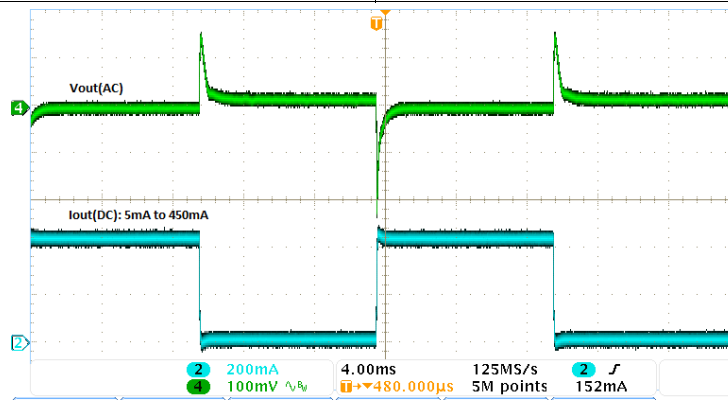


Figure 15. Load Transient  
10- $\mu$ F Ceramic Output Capacitor

## 9 Detailed Description

### 9.1 Overview

The TPS7B67xx-Q1 family of devices is an low-dropout linear regulator combined with an enable and reset function. The power-on-reset initializes when the output voltage,  $V_O$ , exceeds 91.6% of the target value. The power-on reset delay is a function of the value set by an external capacitor on the DELAY pin before releasing the RST pin high.

### 9.2 Functional Block Diagrams

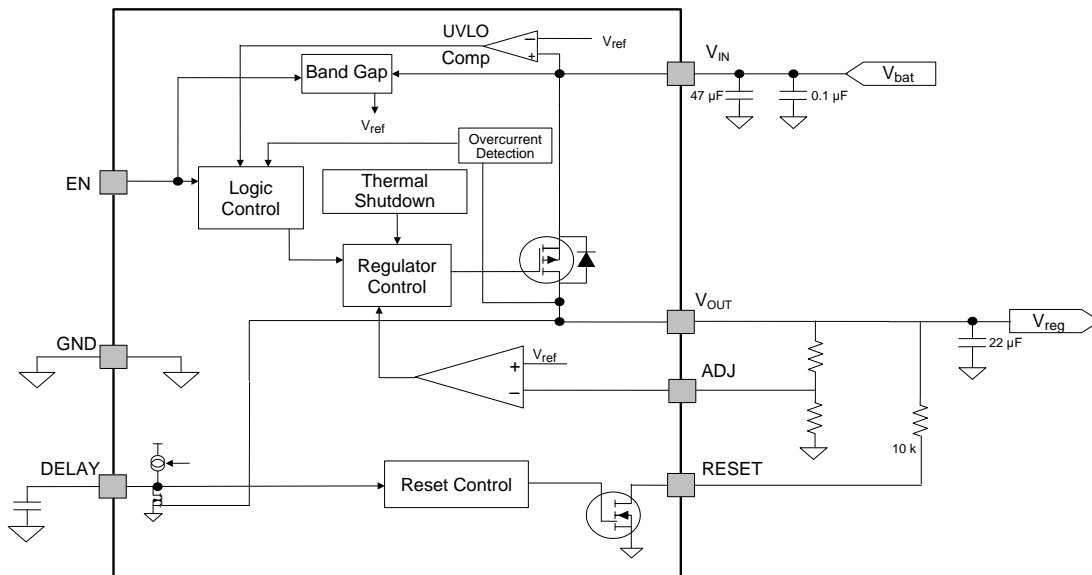


Figure 16. TPS7B6701-Q1 Functional Block Diagram

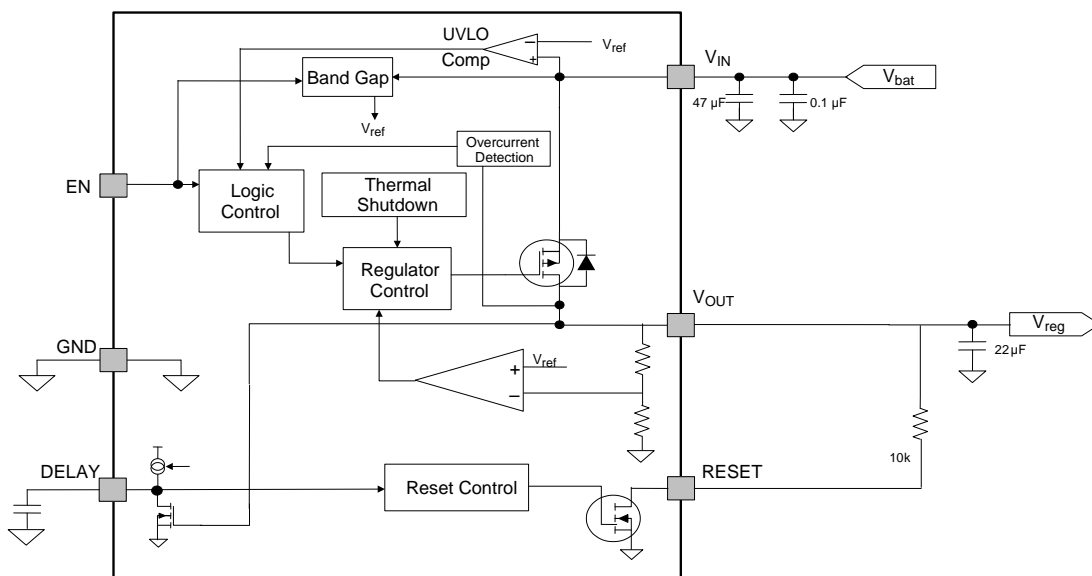


Figure 17. TPS7B6733-Q1 and TPS7B6750-Q1 Functional Block Diagram

### 9.3 Feature Description

#### 9.3.1 Enable (EN)

The enable pin is a high-voltage-tolerant pin. A high input on EN activates the device and turns on the regulator. For self-bias applications, connect this input to the  $V_{IN}$  pin.

#### 9.3.2 Regulated Output ( $V_{OUT}$ )

The  $V_{OUT}$  pin is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft start incorporated to control the initial current through the pass element.

In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

#### 9.3.3 Power-On-Reset (RESET)

The power-on-reset is an output with an external pullup resistor to the regulated supply. The reset output remains low until the regulated  $V_O$  exceeds approximately 91.6% of the set value and the power-on-reset delay has expired. The regulated output falling below the 89.6% level asserts this output low after a short de-glitch time of approximately 180  $\mu$ s (typical).

#### 9.3.4 Reset Delay Timer (DELAY)

An external capacitor on this pin sets the timer delay before the reset pin is asserted high. The constant output current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator. If this pin is open, the default delay time is 325  $\mu$ s (typical).

The reset pulse delay time  $t_d$ , is defined with the charge time of an external capacitor DELAY (see Equation 1).

$$t_d = \frac{C_{DELAY} \times 1 V}{9.5 \mu A} \quad (1)$$

The power-on-reset initializes when  $V_O$  exceeds 91.6% of the programmed value. The power-on-reset delay is a function of the value set by an external capacitor on the DELAY pin before the RESET pin is released high.

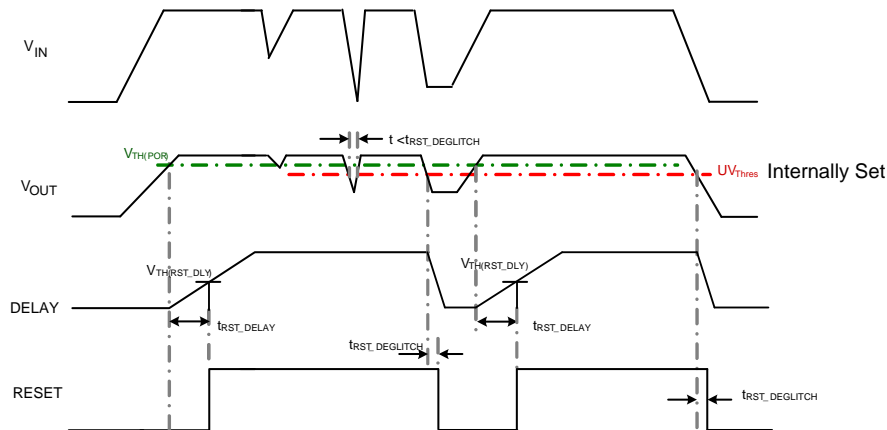


Figure 18. Conditions to Activate RESET

## Feature Description (continued)

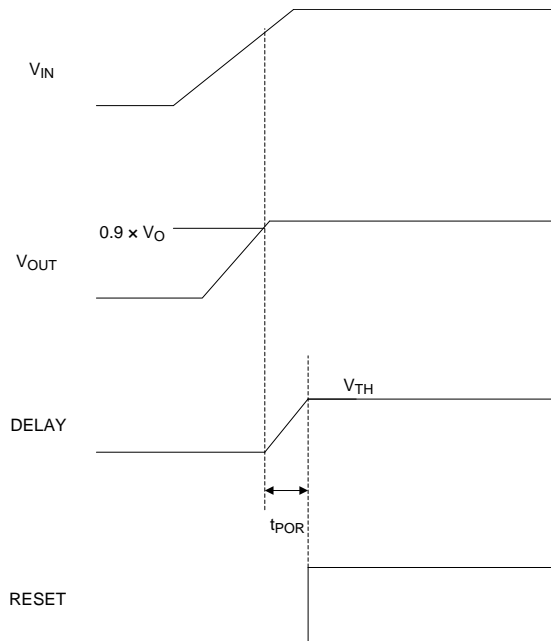


Figure 19. External Programmable-Reset Delay

### 9.3.5 Adjustable Output Voltage (ADJ for TPS7B6701)

An output voltage between 1.5 V and 18 V can be selected by using the external resistor dividers. Use Equation 2 to calculate the output voltage, where  $V_{ADJ} = 1.233$  V. In order to avoid a large leakage current and to prevent a divider error, the value of  $(R1 + R2)$  must be between 10 k and 100 k $\Omega$ .

$$V_O = V_{ADJ} \times \left(1 + \frac{R2}{R1}\right) \quad (2)$$

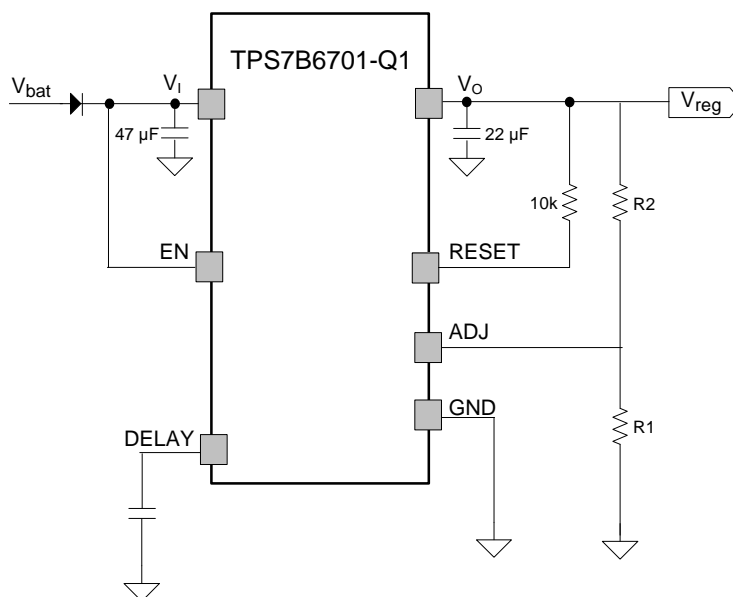


Figure 20. External Feedback Resistor Divider

## Feature Description (continued)

### 9.3.6 Undervoltage Shutdown

The TPS7B67xx-Q1 family of devices has an internally-fixed undervoltage shutdown threshold. Undervoltage shutdown activates when the input voltage on  $V_{IN}$  drops below  $V_{INUVLO}$ . This activation ensures the regulator is not latched into an unknown state during low-input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up similar to a typical power-up sequence when the input voltage is above the required levels.

### 9.3.7 Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous standard operation, the junction temperature must not exceed the TSD trip-point. If the junction temperature exceeds the TSD trip-point, the output turns off. When the junction temperature falls below the TSD trip-point minus TSD hysteresis, the output turns on again.

### 9.3.8 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 175°C which allows the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator and protects it from damage as a result of overheating.

The internal protection circuitry of the TPS7B67xx-Q1 device has been designed to protect against overload conditions. The circuitry was not intended to replace proper heat-sinking. Continuously running the TPS7B67xx-Q1 device into thermal shutdown degrades device reliability.

## 9.4 Device Functional Modes

### 9.4.1 Operation With $V_{IN} < 4\text{ V}$

The devices operate with input voltages above 4 V. The maximum UVLO voltage is 2.6 V and operates at input voltage above 4 V. The devices can also operate at lower input voltages; no minimum UVLO voltage is specified. At input voltages below the actual UVLO voltage, the devices do not operate.

### 9.4.2 Operation With EN Control

The enable rising edge threshold voltage is 1.7 V (maximum), with the EN pin is held above that voltage and the input voltage is above the 4 V, the device becomes active. The enable falling edge is 0.4 V (minimum), with the EN pin is held below that voltage the device is disabled, the IC quiescent current is reduced in this state.

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

Figure 21 and Figure 22 show typical application circuits for the TPS7B6701-Q1 device and the TPS7B6733-Q1 and TPS7B6750-Q1 device respectively. Based on the end-application, different values of external components can be used. An application can require a larger output capacitor during fast load steps in order to prevent a reset from occurring. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

### 10.2 Typical Application

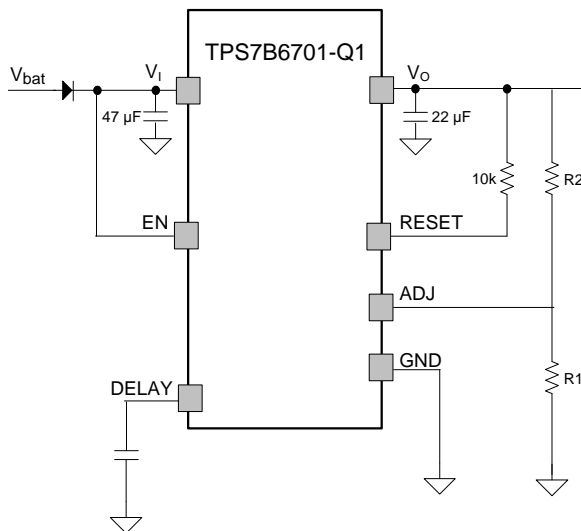


Figure 21. Typical Application Schematic for TPS7B6701-Q1

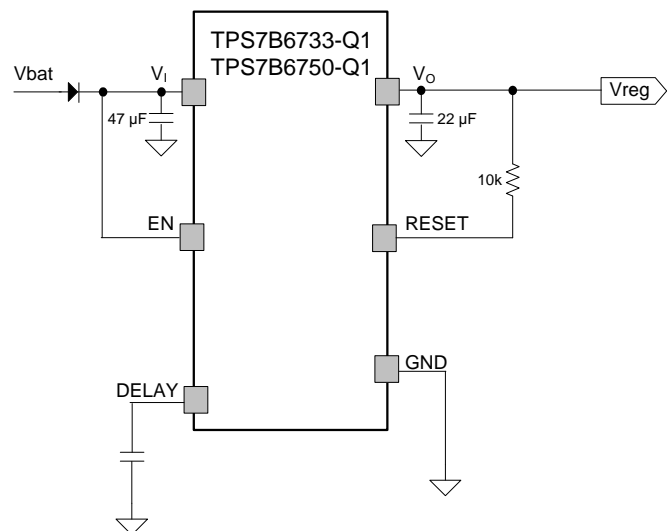


Figure 22. Typical Application Schematic for TPS7B6733-Q1 and TPS7B6750-Q1

#### 10.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4 V to 40 V
Output voltage	1.5 V to 18 V
Output current rating	450 mA
Output capacitor range	10 µF to 500 µF
Output capacitor ESR range	1 mΩ to 20 Ω
DELAY capacitor range	100 pF to 500 nF



## 10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Output capacitor
- Power-up reset delay time

### 10.2.2.1 Power Dissipation and Thermal Considerations

Device power dissipation is calculated with Equation 3.

$$P_D = I_O \times (V_I - V_O) + I_Q \times V_I$$

where

- $P_D$  = continuous power dissipation
- $I_O$  = output current
- $V_I$  = input voltage
- $V_O$  = output voltage

(3)

As  $I_Q \ll I_O$ , the term  $I_Q \times V_I$  in Equation 3 can be ignored.

For a device under operation at a given ambient air temperature ( $T_A$ ), calculate the junction temperature ( $T_J$ ) with Equation 4.

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where

- $R_{\theta JA}$  = junction-to-ambient air thermal impedance

(4)

A rise in junction temperature because of power dissipation can be calculated with Equation 5.

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D)$$

(5)

For a given maximum junction temperature ( $T_{JM}$ ), the maximum ambient air temperature ( $T_{AM}$ ) at which the device can operate is calculated with Equation 6.

$$T_{AM} = T_{JM} - (R_{\theta JA} \times P_D)$$

(6)

## 10.2.3 Application Curves



Figure 23. TPS7B6750-Q1 Power-Up Waveform



Figure 24. TPS7B6750-Q1 Power-Down Waveform

## 11 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B67xx-Q1 device, an electrolytic capacitor with a value of 47  $\mu$ F and a ceramic bypass capacitor are recommended to add at the input.

### 11.1 Dropout Recovery

All LDOs have some overshoot when recovering from dropout, how much is primarily dependent on the transient response (bandwidth) of the error amplifier. Because of design and system level tradeoffs made when creating the TPS7B67xx-Q1, the error amplifier has a slower transient response than many other LDOs, which is evident in the load transient plot in [Figure 15](#). This slower transient response can cause the output to overshoot significantly when the device is recovering from a dropout condition. A well-regulated power supply eliminates this behavior by keeping the TPS7B67xx-Q1 out of dropout. If the device is placed into dropout and the rising  $V_{IN}$  ramp rate is less than 200 mV/ms, the overshoot is limited to 0.5 V; however, faster ramp rates result in more overshoot and may require a zener diode on the output to limit the  $V_{OUT}$  overshoot.

#### 11.1.1 LDO Dropout Recovery Explained

When an LDO is in dropout the output voltage is below the accuracy specification. This condition causes the error amplifier to force the gate of the pass transistor such that the pass transistor is fully on and provides the least resistance possible, meaning  $V_{OUT}$  tracks  $V_{IN}$  as closely as possible. When the input voltage recovers, the error amplifier must force the gate of the pass device to the opposite rail making the pass transistor more resistive. The change in gate voltage takes a finite amount of time, as dictated by the bandwidth of the error amplifier. If  $V_{IN}$  rises quickly during that time then  $V_{OUT}$  tracks  $V_{IN}$  and overshoots above the nominal output voltage. [Figure 25](#) depicts a graphical representation of an LDO recovering from dropout.

The amplitude of the overshoot is determined by both the speed of the  $V_{IN}$  ramp and the transient response of the LDO, which determines how long is required for the error amplifier to respond to changes on  $V_{OUT}$ . The amount of time required for the overshoot to be discharged is determined by the load current that must drain the excess charge that has accumulated on  $C_{OUT}$ .

## Dropout Recovery (continued)

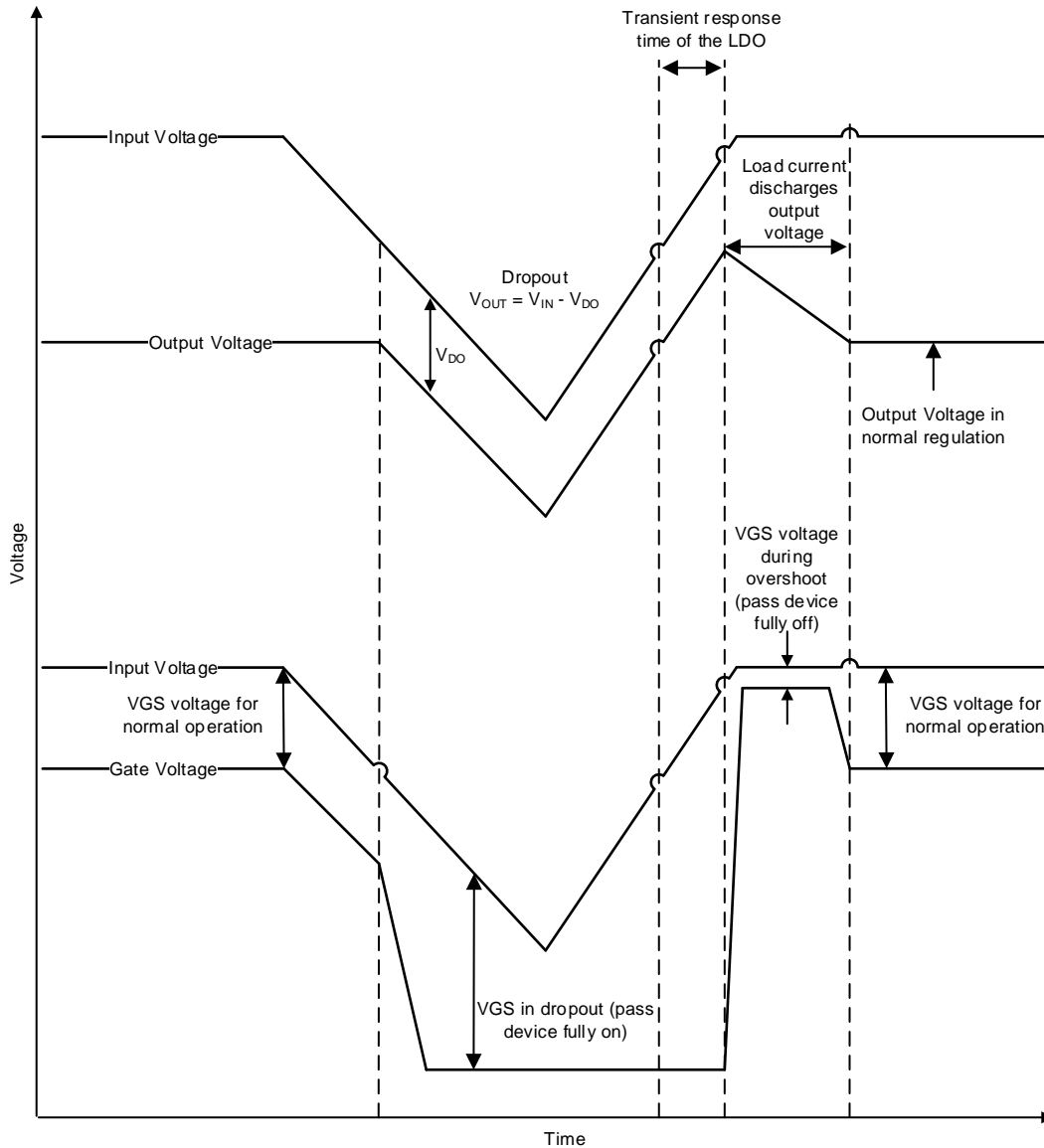


Figure 25. LDO Response Entering and Exiting Dropout

### 11.1.2 TPS7B67xx-Q1 Dropout During Startup

The TPS7B67xx-Q1 does not overshoot significantly if the LDO is enabled after the input voltage is already above  $V_{OUT(NOM)}$  plus  $V_{DO}$ . Furthermore, startup performance is not affected as long as the input voltage transitions from  $V_{UVLO+(IN)}$  to  $V_{OUT(NOM)}$  plus  $V_{DO}$  in less than 1 millisecond. Approximately 1 millisecond is required for the TPS7B67xx-Q1 reference voltage to reach its steady state value, so input voltage startup transitions that are less than 1 millisecond do not force the device into dropout. One example that does not overshoot is a 5-V output voltage with full load (full load has the highest dropout), where the input voltage ramps steadily from 0 V to 5.45 V in less than 3 milliseconds. Overshoot does not occur in this case because the input reaches  $V_{OUT}$  plus  $V_{DO}$  before the reference has come up all the way to its final value, keeping the LDO out of dropout. Figure 26 depicts an example of a startup ramp rate that is just fast enough to keep a device with a 5-V output voltage from going into dropout.

## Dropout Recovery (continued)

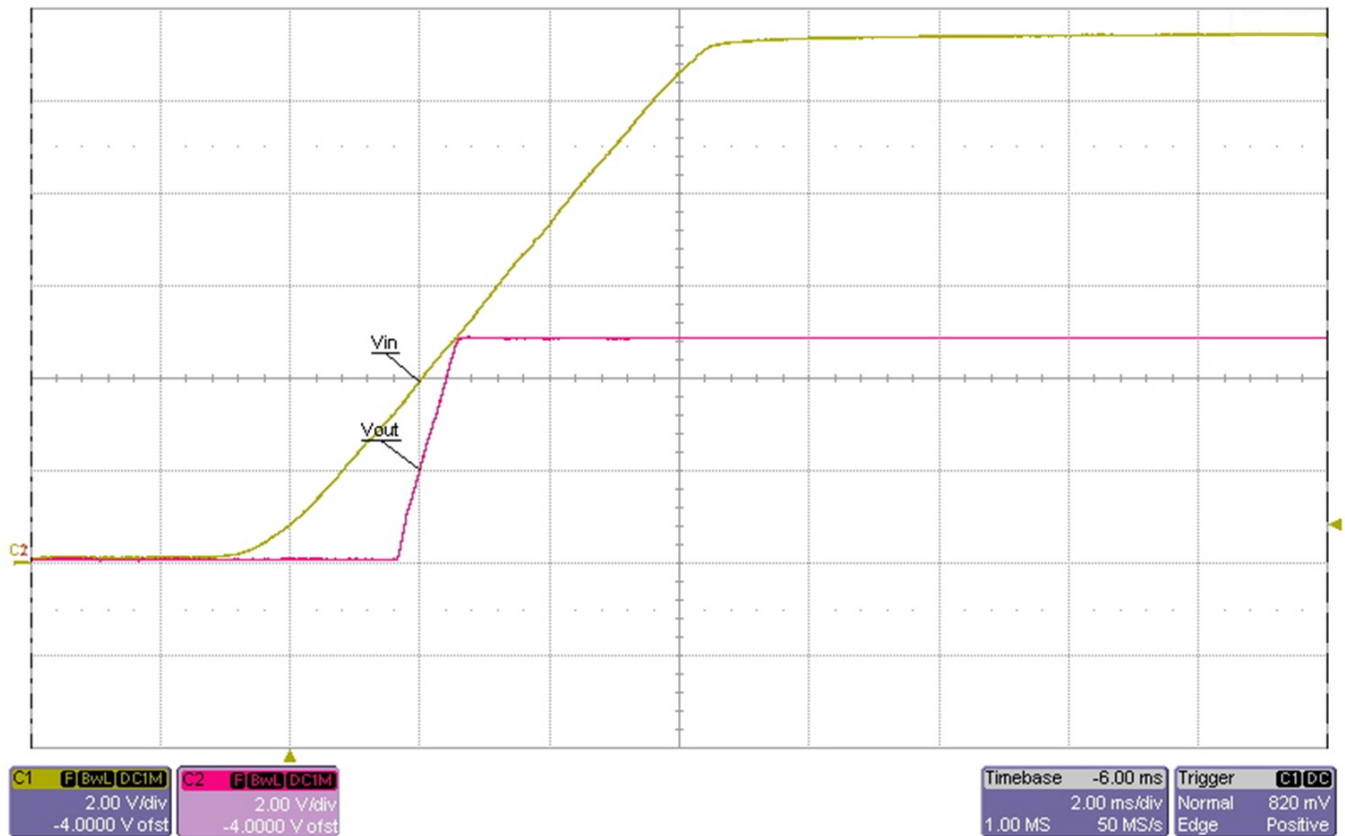


Figure 26. Startup Ramp Speed to Avoid Dropout

## 12 Layout

### 12.1 Layout Guidelines

#### 12.1.1 Enhanced Thermal Pad

For the PWP package, TI recommends to layout an enhanced thermal pad on the board in order to realize better thermal impedance; see [Figure 27](#). No extra board size is required and the standard operation is not influenced by this layout.

## Layout Guidelines (continued)

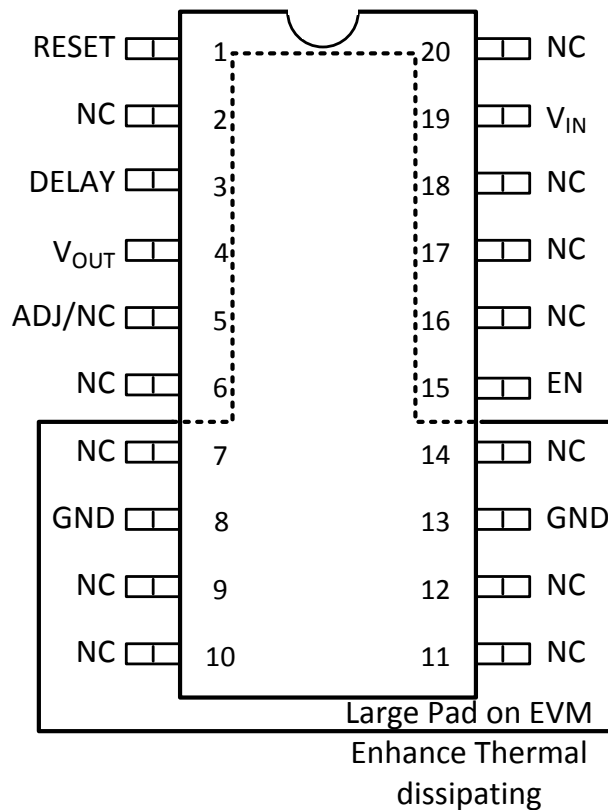


Figure 27. Thermally Enhanced Layout for the PWP Package (TPS7B6701-Q1)

### 12.1.2 Package Mounting

Solder-pad footprint recommendations for the TPS7B67xx-Q1 devices are available at the end of this data sheet and at [www.ti.com](http://www.ti.com).

### 12.1.3 Board Layout Recommendations to Improve PSRR and Noise Performance

- To improve AC performance such as PSRR, output noise, and transient response, TI recommends to design the board with separate ground planes for V<sub>IN</sub> and V<sub>OUT</sub>, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must connect directly to the GND pin of the device.
- Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close to the device as possible and on the same side of the PCB as the regulator.
- Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces can also cause instability.
- If possible, and to ensure the maximum performance listed in this data sheet, use the same layout pattern used for TPS7B67xx-Q1 evaluation board, available at [www.ti.com](http://www.ti.com).

## Layout Guidelines (continued)

### 12.1.4 Additional Layout Considerations

Because of the high impedance of the ADJ pin, the regulator is sensitive to parasitic capacitances that can couple undesirable signals from nearby components (especially from logic and digital ICs, such as microcontrollers and microprocessors). These capacitive-coupled signals can produce undesirable output-voltage transients. If undesirable output-voltage transients occur, TI recommends to use a fixed-voltage version of the TPS7B67xx-Q1 devices, or to isolate the ADJ node by flooding the local PCB area with ground-to-plane copper in order to minimize any undesirable signal coupling.

### 12.2 Layout Example

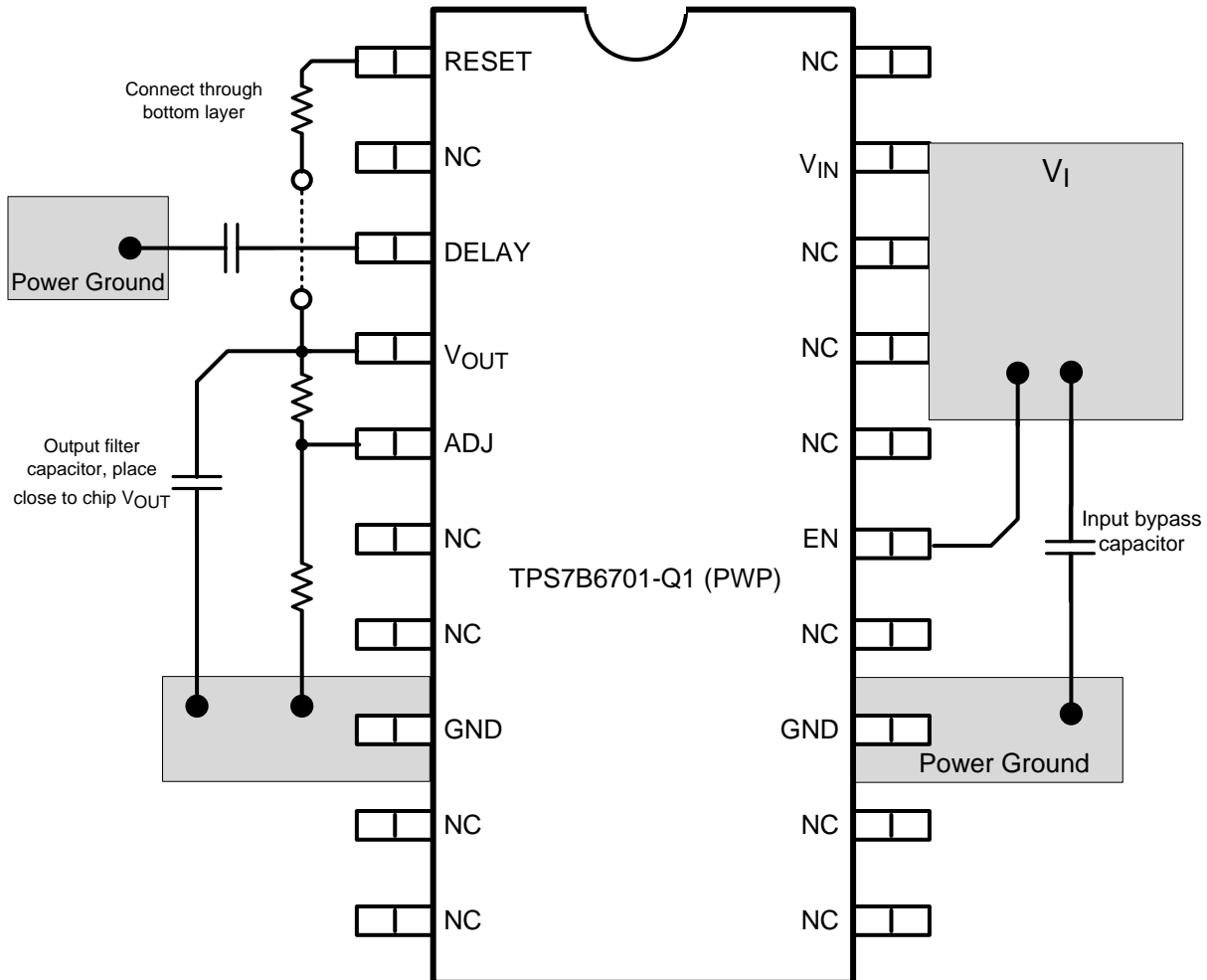


Figure 28. TPS7B6701-Q1 Layout Example

## 13 デバイスおよびドキュメントのサポート

### 13.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS7B6701-Q1	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>
TPS7B6733-Q1	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>
TPS7B6750-Q1	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>	<a href="#">ここをクリック</a>

### 13.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 13.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™オンライン・コミュニティ** *TIのE2E (Engineer-to-Engineer) コミュニティ*。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

**設計サポート** *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

### 13.4 商標

PowerPAD, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

### 13.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B6701QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B6701	<a href="#">Samples</a>
TPS7B6733QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B6733	<a href="#">Samples</a>
TPS7B6750QPWPRQ1	ACTIVE	HTSSOP	PWP	20	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B6750	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B6701QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS7B6733QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS7B6750QPWPRQ1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B6701QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS7B6733QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS7B6750QPWPRQ1	HTSSOP	PWP	20	2000	350.0	350.0	43.0

## GENERIC PACKAGE VIEW

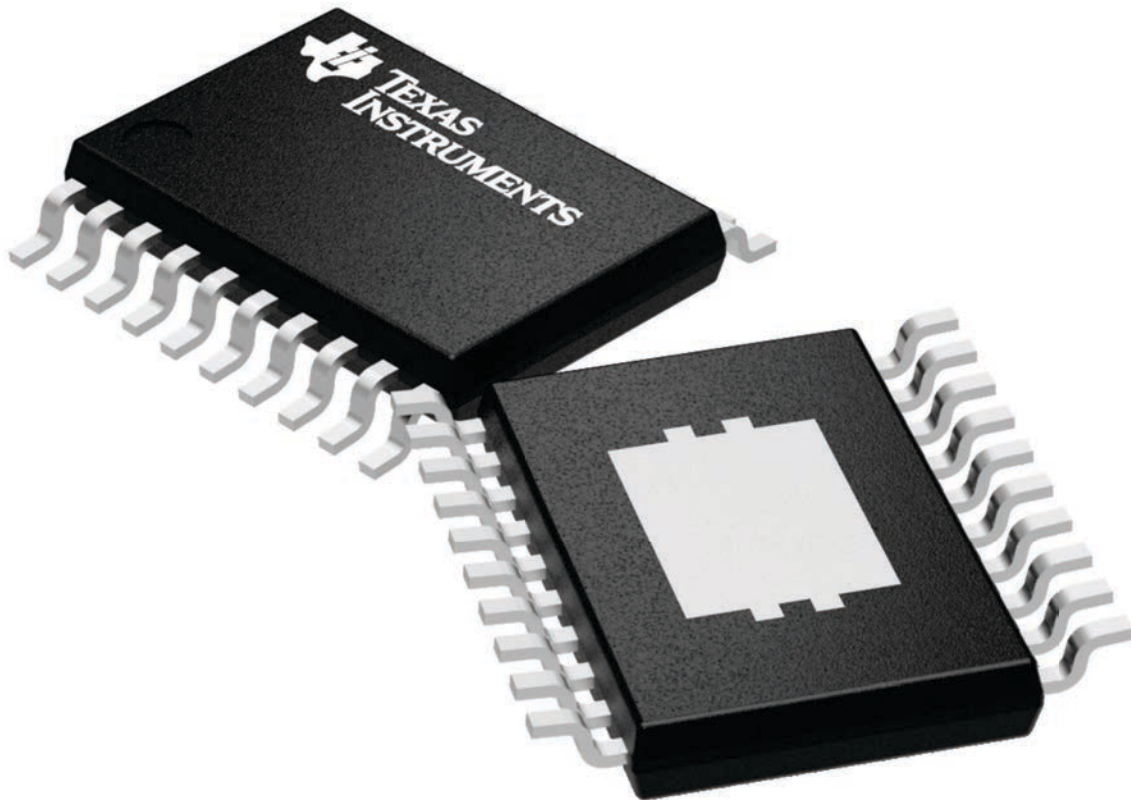
**PWP 20**

**HTSSOP - 1.2 mm max height**

6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

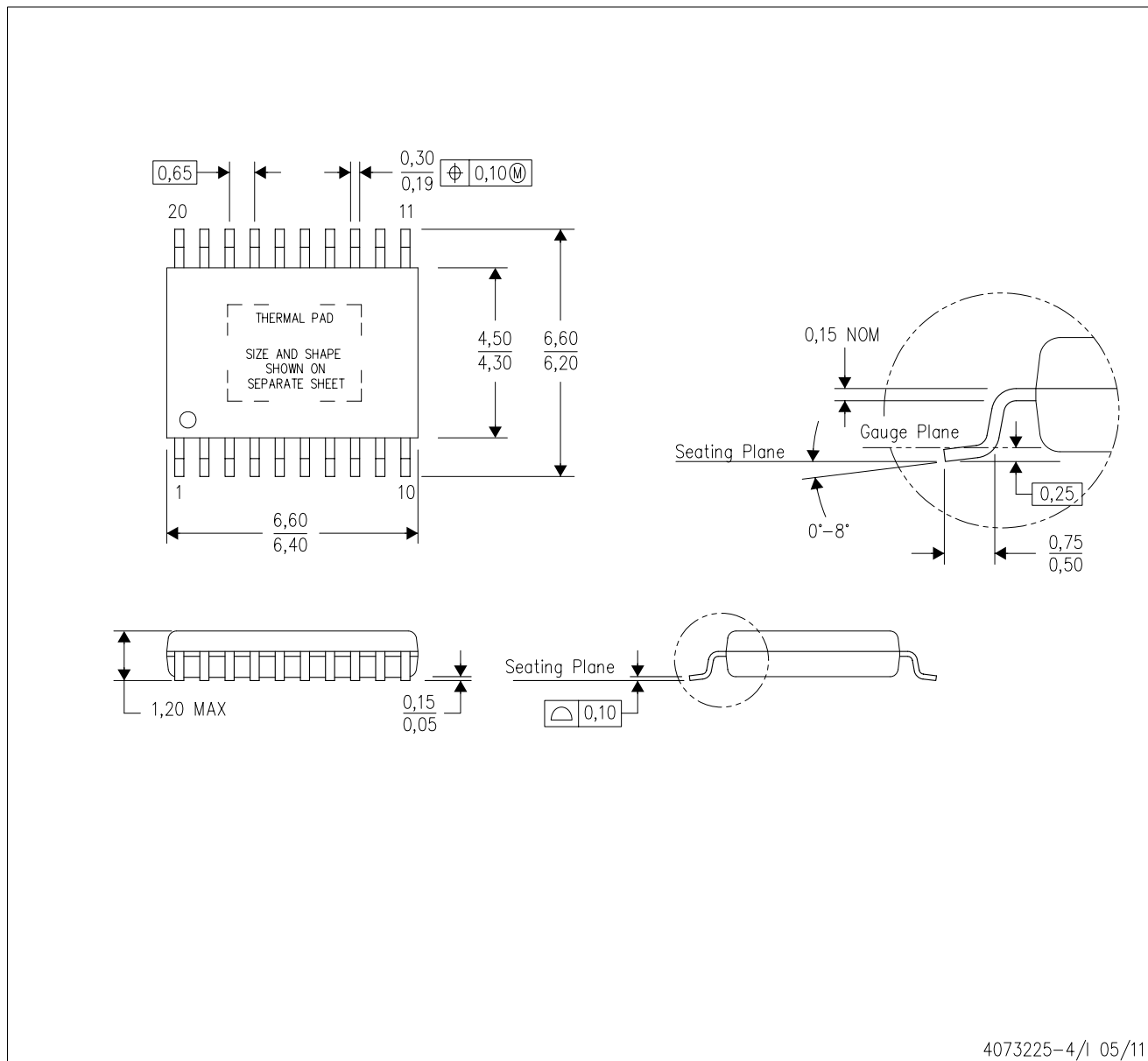


4224669/A

# MECHANICAL DATA

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-4/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

# THERMAL PAD MECHANICAL DATA

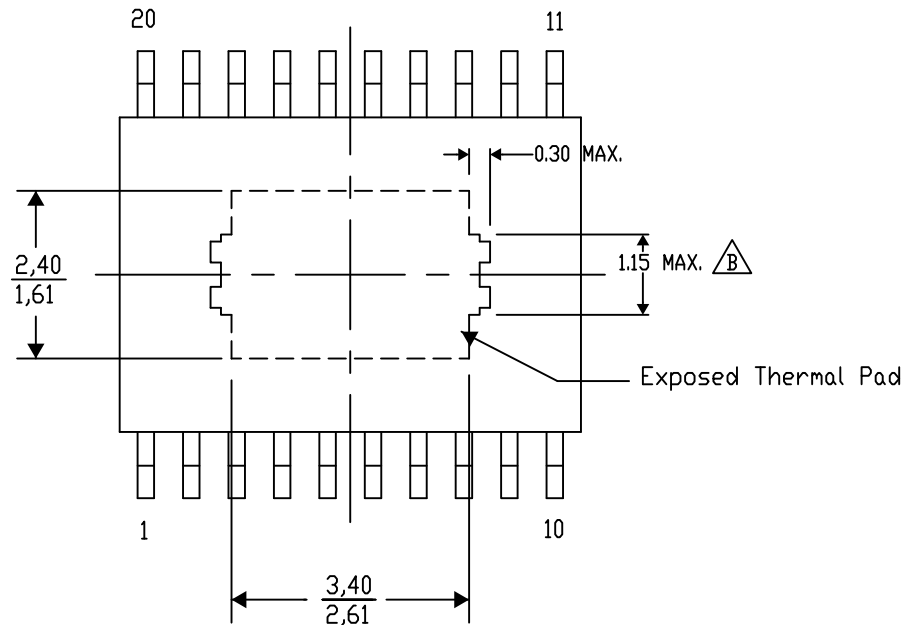
## PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-15/AO 01/16

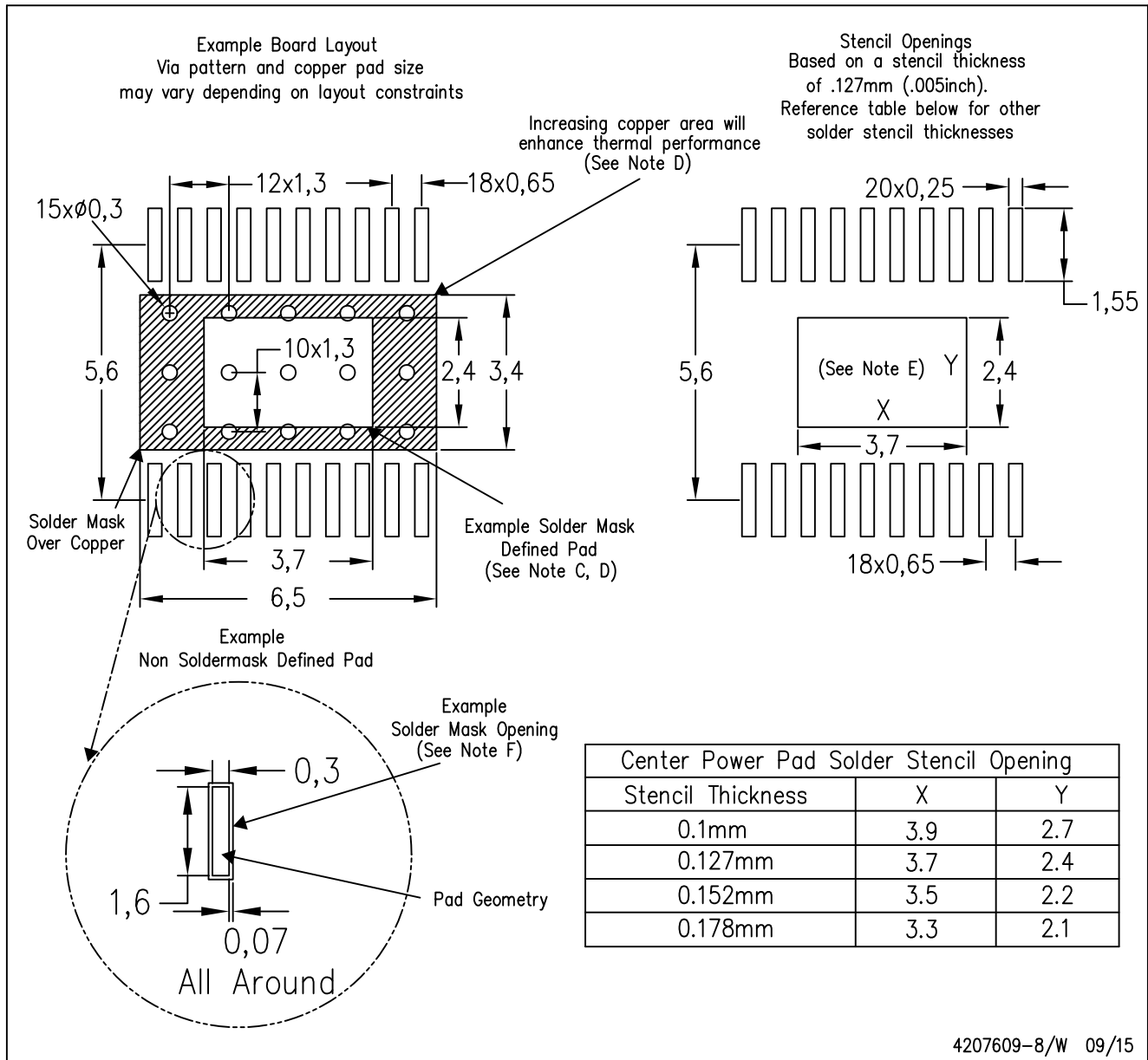
NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
  - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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