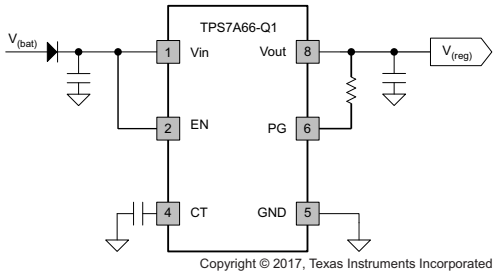
TPS7A6x-Q1 高電圧、超低 $I_{(q)}$、低ドロップアウト・レギュレータ

1 特長

- 車載アプリケーションに対応
- 以下のAEC-Q100試験ガイダンス
  - デバイス温度グレード 1
  - デバイス温度グレード 0 (TPS7A6650EDGNRQ1 のみ)
  - デバイスHBM ESD分類レベルH2
  - デバイスCDM ESD分類レベルC4
- デバイス接合部温度範囲：
  –40°C～+150°C
- 4V～40V の広い Vin 入力電圧範囲、最大 45V の過渡電圧に対応
- 出力電流：150mA
- 低い静止電流 ($I_{(q)}$)
  - EN = Low のとき (シャットダウン・モード) 2µA
  - 軽負荷時の標準値12µA
- 低ESRのセラミック出力コンデンサで安定 (2.2µF～100µF)
- 150mAにおいてドロップアウト電圧300mV (標準値、$V_{(Vin)}$ = 4V)
- 固定出力電圧 (3.3V および 5V) と可変出力電圧 (1.5V～5V)
  (可変出力電圧は TPS7A66-Q1 のみ)
- 低入力電圧トラッキング
- パワーオン・リセット機能を搭載
  - リセット・パルス遅延をプログラム可能
  - オープン・ドレイン・リセット出力
- 保護機能を搭載
  - サーマル・シャットダウン
  - 短絡保護
- 入力電圧センス・コンパレータ
  (TPS7A69-Q1 のみ)
- パッケージ
  - 8 ピン SOIC-D (TPS7A69-Q1)
  - 8 ピン HVSSOP-DGN (TPS7A6601-Q1)

ハードウェア・イネーブル・オプション



2 アプリケーション

- スリープ・モード搭載のインフォテインメント・システム
- 車体制御モジュール
- 常時オンのバッテリ・アプリケーション:
  - ゲートウェイ・アプリケーション
  - リモート・キーレス・エントリ・システム
  - イモビライザー

3 概要

TPS7A66-Q1 および TPS7A69-Q1 は、最大 40V の Vin で動作するように設計された低ドロップアウト・リニア・レギュレータです。無負荷時の静止電流がわずか 12µA であるため、特に車載用途におけるスタンバイ・マイクロプロセッサ制御ユニット・システムに最適です。

デバイスには、短絡および過電流保護機能が内蔵されています。電源投入時に出力電圧が安定し、レギュレートされていることを示すために、デバイスにはリセット遅延が実装されています。この遅延時間は、外付けコンデンサによりプログラム可能です。低電圧トラッキング機能により、小型の入力コンデンサを使用でき、コールド・クランク状況では多くの場合に昇圧コンバータが不要になります。

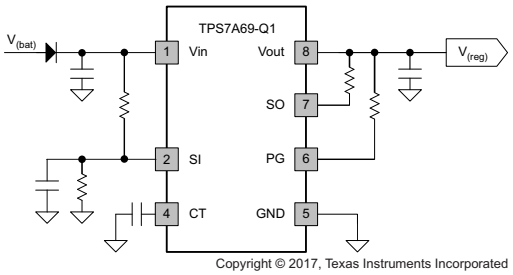
デバイスは、-40℃～125℃の温度範囲で動作します。TPS7A6650EDGNRQ1デバイスはAEC-Q100グレード0に認定済みで、-40℃～150℃の温度範囲で動作します。これらの機能のため、このデバイスは各種の車載用アプリケーションの電源に最適です。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS7A66-Q1	HVSSOP (8)	3.00mm×3.00mm
TPS7A69-Q1	SOIC (8)	4.90mm×3.91mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

入力電圧センス・オプション



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (November 2014) から Revision F に変更 **Page**

- 最初の 2 つの AEC-Q100 小項目の温度範囲を削除し、「特長」の*AEC-Q100 試験ガイダンス*項目を 変更 ... 1
- ドキュメント全体で $V_{(Vin)}$ を V_{IN} に、Vin を VIN に、$V_{(Vout)}$ を V_{OUT} に、Vout を VOUT に、$V_{(CT)}$ を V_{CT} に 変更 ... 1
- 「特長」の*デバイス接合部温度範囲*項目 追加 ... 1
- ドキュメント全体で関連デバイスを TPS7A66-Q1 および TPS7A69-Q1 に 変更 ... 1
- ドキュメント全体で MSOP を HVSSOP に 変更 ... 1
- Changed CT, EN, FB/DNC, PG, SO, and VOUT descriptions in *Pin Functions* table ... 4
- Changed pin names FB/NU to FB/DNC, Vin to VIN, and Vout to VOUT in *Pin Configuration and Functions* section ... 4
- Changed SI parameter name description and added maximum specification to SI and FB, SO, PG rows in *Absolute Maximum Ratings* table ... 4
- Added parameter names to CT and FB, SO, PG rows in *Absolute Maximum Ratings* table ... 4
- Added *lockout* to *Undervoltage lockout detection* parameter name ... 6
- Added *up to* to I_{lkg} test conditions ... 6
- Added V_{OUT} to unit of $V_{(TH-POR)}$ and $V_{(Thres)}$ ... 6
- Added CT to $V_{(th)}$ parameter name ... 6
- Added header for first section of *Switching Characteristics* table ... 7
- Added *UVLO Thresholds vs Temperature* and *Enable Thresholds vs Temperature* figures ... 8
- Added *CT Charging Current (V_{CT} = 0)* and *CT Charging Threshold* figures ... 9
- Changed *Device Functional Modes* section ... 17

Revision D (October 2014) から Revision E に変更 **Page**

- Corrected voltage unit in Handling Ratings table from V to kV ... 5

Revision C (December 2013) から Revision D に変更 **Page**

- CDM ESC分類レベルを変更 ... 1
- Changed FB/NC pin to FB/NU in Pin Functions table Added NC and NU notes to pinout drawings ... 4
- Removed ESD and T_{stg} specifications from the *Absolute Maximum Ratings* table ... 4
- Added *ESD Ratings* table ... 5
- Numerous changes throughout the *Electrical Characteristics* table ... 6
- Added *Switching Characteristics* table ... 7
- Moved an oscilloscope trace to the Applications Information section ... 10
- Changed de-glitch time in *Power-On Reset (PG) section* ... 13
- Changed reset delay timer default delay to 290 µs from 150 µs ... 13
- Changed voltage at which Power-on reset initializes to 91.6% of $V_{(Vout)}$ ... 13
- Changed selectable output voltage range and calculation for FB resistor divideer ... 15

Revision B (August 2013) から Revision C に変更 **Page**

- 「概要」セクションの型番に -Q1 を追加して訂正 ... 1
- Changed Operating ambient temperature to Operating junction temperature ... 4
- Added PSRR graph to Typical Characteristics ... 10
- Deleted a paragraph from the Thermal Protection section ... 16

Revision A (March 2013) から Revision B に変更 **Page**

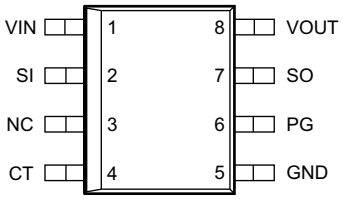
- Added two conditions to $V_{dropout}$ in the Electrical Characteristics table ... 6

2012年12月発行のものから更新 **Page**

- Deleted the ORDERING INFORMATION table ... 4
- Changed From: T_A Operating ambient temperature range –40 to 125°C To: T_J Operating ambient temperature range –40 to 150°C ... 4

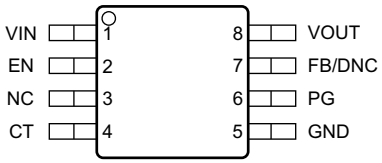
5 Pin Configuration and Functions

D Package (TPS7A69-Q1)
8-Pin SOIC
Top View



NC - No internal connection

DGN Package (TPS7A66-Q1)
8-Pin HVSSOP
Top View



NC - No internal connection
NU - Make no external connection

Pin Functions

PIN NAME	PIN NO.		TYPE	DESCRIPTION
	SOIC-D	HVSSOP-DGN		
CT	4	4	O	Reset-pulse delay adjustment. Connecting a capacitor from this pin to GND changes the PG reset delay; see the *Reset Delay Timer (CT)* section for more details.
EN	—	2	I	Enable pin. The device enters the standby state when the enable pin becomes lower than the enable threshold.
FB/DNC	—	7	I	Feedback pin when using external resistor divider or DNC pin when using the device with a fixed output voltage.
GND	5	5	G	Ground reference
NC	3	3	—	Not-connected pin
PG	6	6	O	Power good. This open-drain pin must connect to VOUT via an external resistor. V_{PG} is logic level high when V_{OUT} is above the power-on-reset threshold.
SI	2		I	Sense input pin to supervise input voltage. Connect via an external voltage divider to VIN and GND.
SO	7		O	Sense output. This open-drain pin must connect to VOUT via an external resistor. V_{SO} is logic level low when V_{SI} falls below the sense-low threshold.
VIN	1	1	P	Input power-supply voltage
VOUT	8	8	O	Regulated output voltage
Thermal pad	Pad	—	—	Thermal pad for HVSSOP-DGN package

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
VIN, EN	Unregulated input (2) (3)	–0.3	45	V
VOUT	Regulated output	–0.3	7	V
SI	Sense input (2)	–0.3	V_{IN}	V
CT	Reset delay input	–0.3	25	V
FB, SO, PG	Feedback, sense output, power good	–0.3	V_{OUT}	V
T_J	Operating junction temperature range	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND
(3) Absolute maximum voltage, withstand 45 V for 200 ms

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1]	0	4	kV
		Charged device model (CDM), per AEC Q100-011 — Corner pins (1, 4, 5, and 8)	0	1	
		Charged device model (CDM), per AEC Q100-011 — Other pins	0	1	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Unregulated input	4		40	V
V_{EN}, V_{SI}	High voltage (I/O)	0		40	V
V_{CT}	CT pin voltage	0		20	V
V_{OUT}	Regulated output	1.5		5.5	V
V_{PG}, V_{SO}, V_{FB}	Low voltage (I/O)	0		5.5	V
C_{IN}	Input capacitor[1]		10		µF
C_{OUT}	Output capacitor[1]	2.2		100	µF
T_J	Operating junction temperature	–40		150	°C

(1) Values on this row refer to the nominal value of the capacitor.

6.4 Thermal Information

THERMAL METRIC[1]		TPS7A66-Q1 HVSSOP (8 PINS)	TPS7A69-Q1 SOIC (8 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.4	113.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.0	59.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	59.57	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.7	12.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.1	52.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.5	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

V_{IN} = 14 V, 1 mΩ < ESR < 2 Ω, T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (VIN)						
V_{IN}	Input voltage	Fixed 5-V output, I_O = 1 mA	5.5		40	V
		Fixed 3.3-V output, I_O = 1 mA	4		40	
$I_{(q)}$	Quiescent current	V_{IN} = 5.5 V to 40 V, EN = ON, I_O = 0.2 mA		12	20	µA
$I_{(Sleep)}$	Input sleep current	No load current and EN = OFF			4	µA
$I_{(EN)}$	EN pin current	$V_{(EN)}$ = 40 V			1	µA
$V_{(bg)}$	Band gap	Reference voltage for FB	1.199	1.223	1.247	V
$V_{(VinUVLO)}$	Undervoltage lockout detection	Ramp V_{IN} down until output turns OFF			2.6	V
$V_{(UVLOhys)}$	Undervoltage hysteresis			1		V
ENABLE INPUT (EN)						
V_{IL}	Logic input low level		0		0.4	V
V_{IH}	Logic input high level		1.7			V
REGULATED OUTPUT (VOUT)						
V_{OUT}	Regulated output	I_O = 1 mA, T_J = 25°C	–1%		1%	
		V_{IN} = 6 V to 40 V, I_O = 1 mA to 150 mA, fixed 5-V version	–2%		2%	
		V_{IN} = 4 V to 40 V, I_O = 1 mA to 150 mA, fixed 3.3-V version	–2%		2%	
		V_{IN} = V_{OUT} + 0.45 V and Vin ≥ 4 V, I_O = 1 mA to 150 mA, adjustable version(1)	–2%		2%	
$V_{(line-reg)}$	Line regulation	V_{IN} = 5.5 V to 40 V, I_O = 50 mA			5	mV
$V_{(load-reg)}$	Load regulation	I_O = 1 mA to 150 mA			20	mV
$V_{(dropout)}$	Dropout voltage	$V_{(dropout)}$ = V_{IN} – V_{OUT}, I_{OUT} = 80 mA		180	240	mV
		V_{IN} – V_{OUT}, I_{OUT} = 150 mA		300	450	
		V_{IN} = 3 V, $V_{(dropout)}$ = V_{IN} – V_{OUT}, I_O = 5 mA	12	27.5	58	
		V_{IN} = 3 V, $V_{(dropout)}$ =V_{IN} –V_{OUT}, I_O = 30 mA	44	80	145	
I_O	Output current	V_{OUT} in regulation	0		150	mA
$I_{(lreg-CL)}$	Output current limit	V_{OUT} short to ground		500	800	mA
PSRR	Power supply ripple rejection(2)	V_{IN} = 12 V, I_L = 10 mA, output capacitance = 2.2 µF				dB
		Frequency = 100 Hz		60		
		Frequency = 100 kHz		40		
VOLTAGE SENSING PRE-WARNING						
$V_{I(S-th)}$	Sense low threshold	$V_{(SI)}$ decreasing	1.089	1.123	1.157	V
$V_{I(S-th,hys)}$	Sense threshold hysteresis		50	100	150	mV
$V_{OL(S)}$	Sense output low voltage	($V_{(SI)}$ ≤ 1.06 V, V_{IN} ≥ 4 V, $R_{(SO)}$ = 10 kΩ to V_{OUT}			0.4	V
$I_{OH(S)}$	Sense output leakage	($V_{(SO)}$ = 5 V, $V_{(SI)}$ ≥ 1.5 V)			1	µA
$I_{I(S)}$	Sense input current		–1	0.1	1	µA
RESET (PG)						
V_{OL}	Reset output, low voltage	I_{OL} = 0.5 mA			0.4	V
I_{lkg}	Leakage current	Reset pulled up to VOUT through a 10-kΩ resistor			1	µA
$V_{(TH-POR)}$	Power-on-reset threshold	V_{OUT} increasing	89.6	91.6	93.6	% of V_{OUT}
$V_{(Thres)}$	Hysteresis			2		% of V_{OUT}
RESET DELAY (CT)						
$I_{(Chg)}$	Delay-capacitor charging current	V_{CT} = 0 V		1.4		µA
$V_{(th)}$	CT threshold to release PG high			1		V
OPERATING TEMPERATURE RANGE						
T_J	Junction temperature		–40		150	°C
$T_{(shutdown)}$	Junction shutdown temperature			175		°C
$T_{(hyst)}$	Hysteresis of thermal shutdown			20		°C

(1) Adjustable version with precision external feedback resistor with tolerance of less than ±1%.
(2) Design information – not tested.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIMING FOR SENSE INPUT AND OUTPUT (SI, SO)						
$t_{(SDeglitch,rise)}$	SI or SO rising deglitch time		50		260	µs
$t_{(SDeglitch,drop)}$	SI or SO falling deglitch time		30		240	µs
TIMING FOR RESET (PG)						
$t_{(POR)}$	Power-on-reset delay	Where C = delay capacitor value; capacitance C = 100 nF(1)	50	100	180	ms
$t_{(POR-fixed)}$		No capacitor on pin	100	290	650	µs
$t_{(Deglitch)}$	Reset deglitch time		20	250		µs

(1) This information only is not tested in production and equation basis is (C × 1) / 1 × 10^{-6} = t_d (delay time).
Where C = Delay capacitor value. Capacitance C range = 100 pF to 100 nF.

6.7 Typical Characteristics

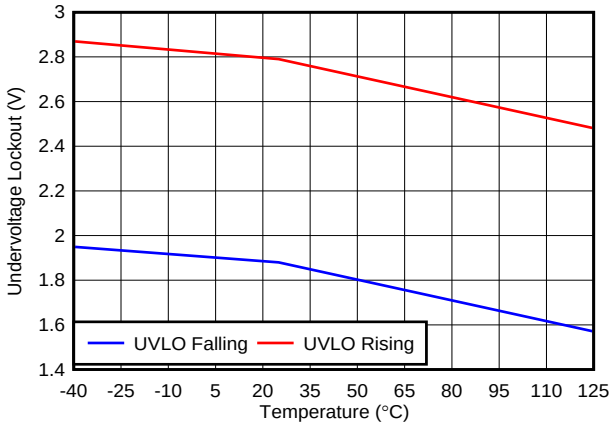


Figure 1. UVLO Thresholds vs Temperature

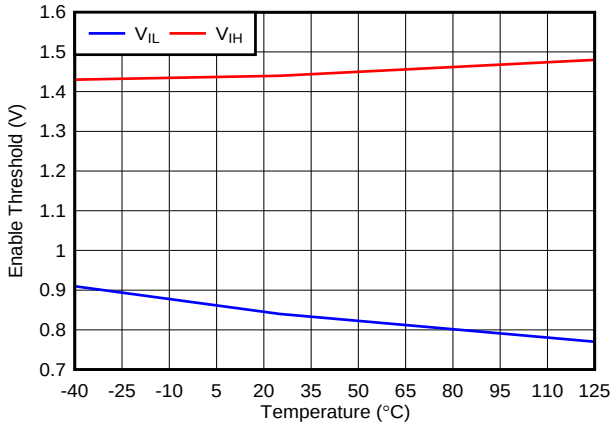


Figure 2. Enable Thresholds vs Temperature

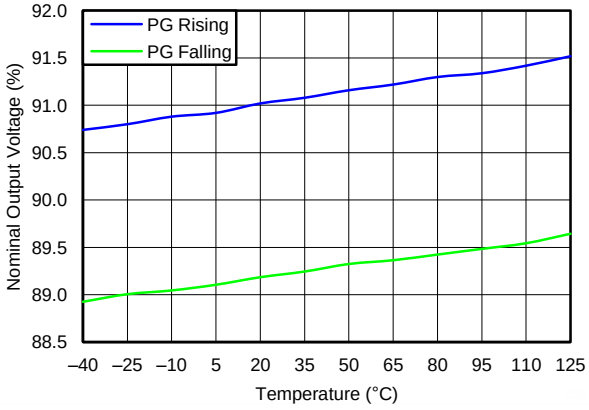


Figure 3. Power-Good Threshold Voltage vs Temperature (V_{IN} = 14 V, No Load)

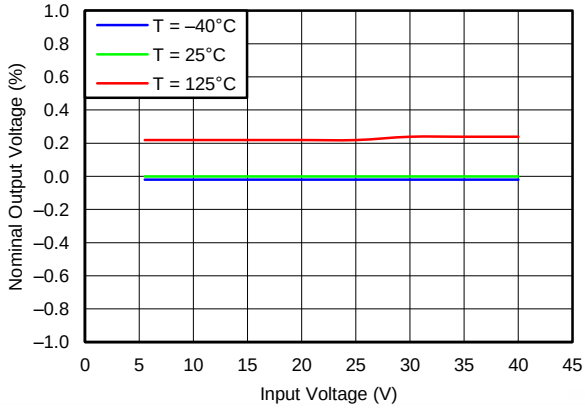


Figure 4. Line Regulation (V_{IN} = 14 V, I_L = 1 mA)

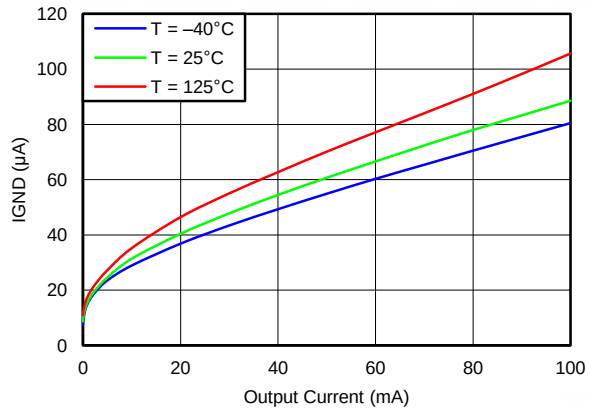


Figure 5. Ground Current vs Output Current (V_{IN} = 14 V)

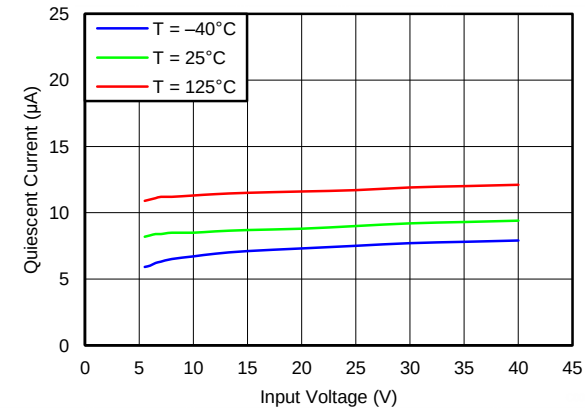


Figure 6. Quiescent Current vs Input Voltage (I_L = 0)

Typical Characteristics (continued)

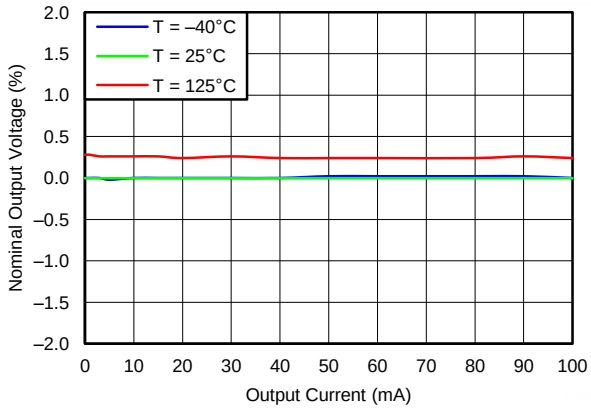


Figure 7. Load Regulation (V_{IN} = 14 V)

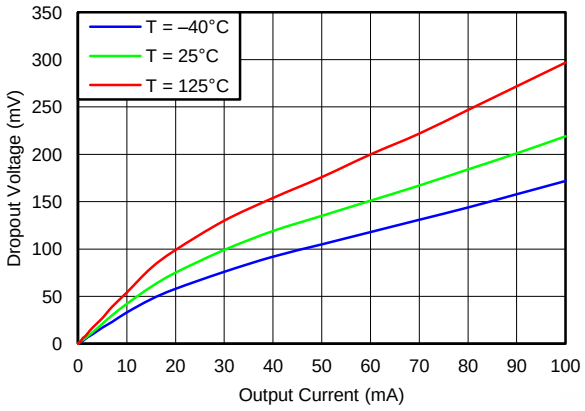


Figure 8. Dropout Voltage vs Output Current (V_{IN} = 4 V)

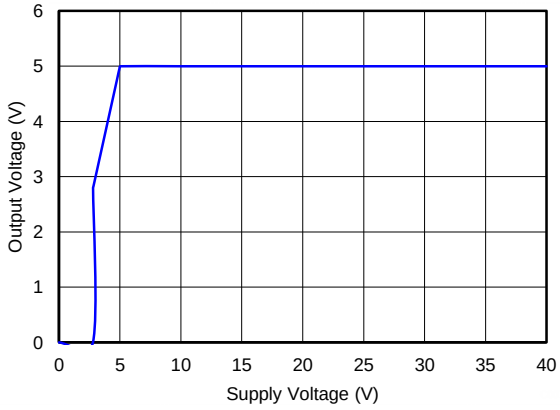


Figure 9. Output Voltage vs Supply Voltage (Fixed 5-V Version, I_L = 0)

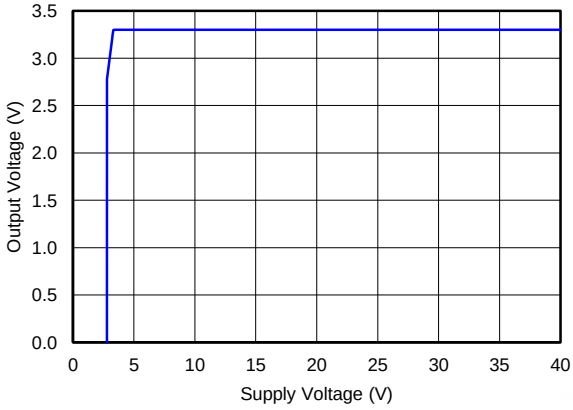


Figure 10. Output Voltage vs Supply Voltage (Fixed 3.3-V Version, I_L = 0)

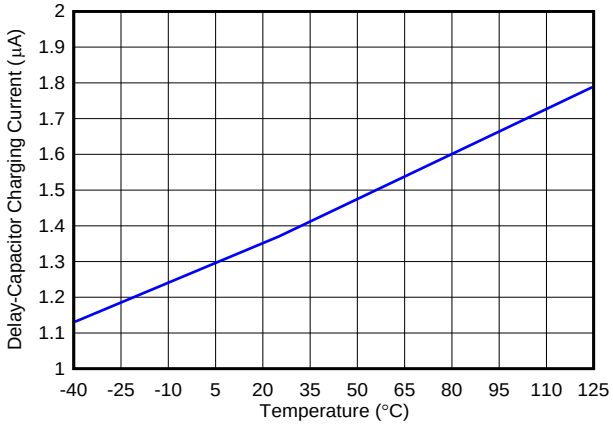


Figure 11. CT Charging Current (V_{CT} = 0)

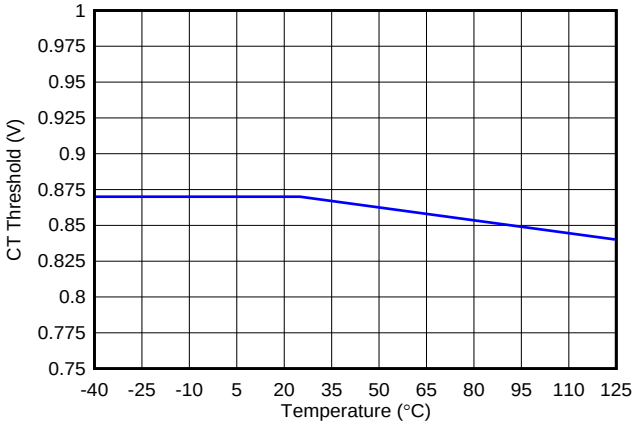


Figure 12. CT Charging Threshold

Typical Characteristics (continued)

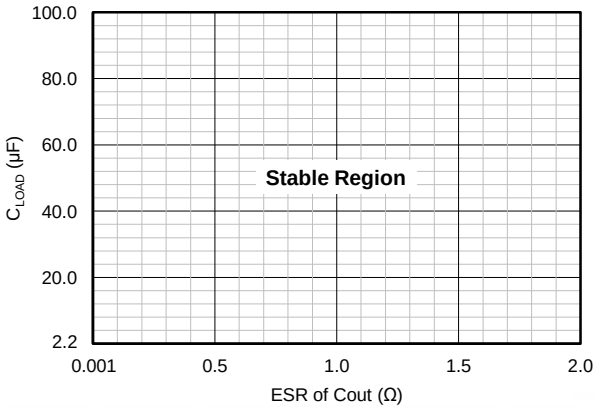


Figure 13. Load Capacitance vs ESR Stability

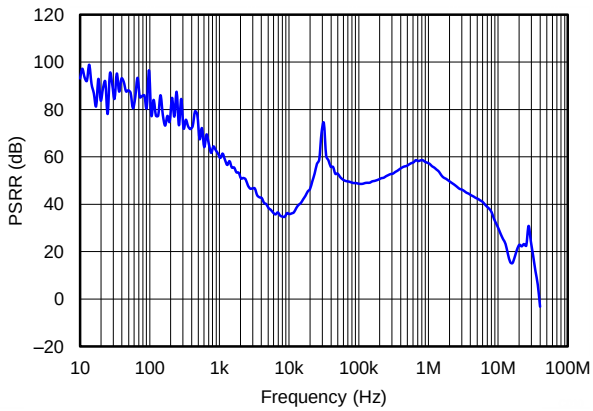
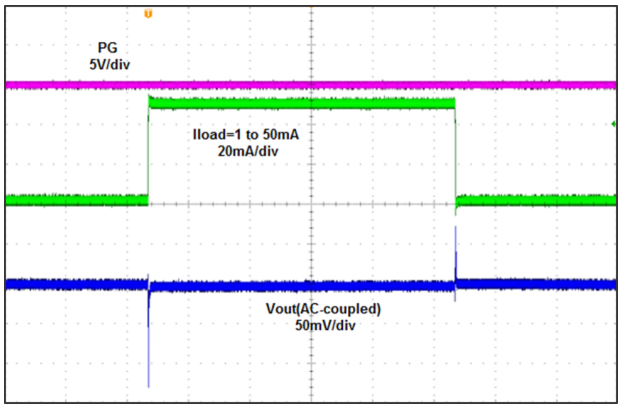
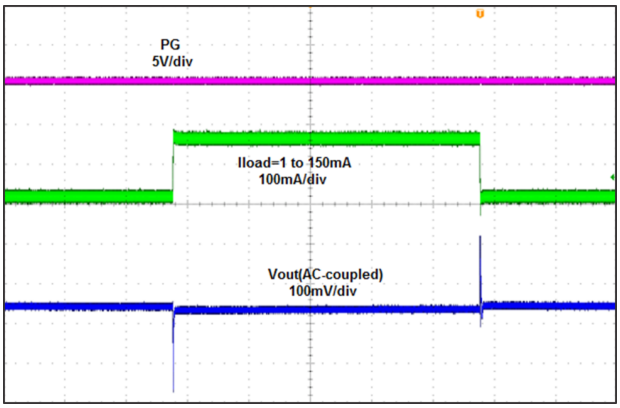


Figure 14. Power-Supply Rejection Ratio vs Frequency



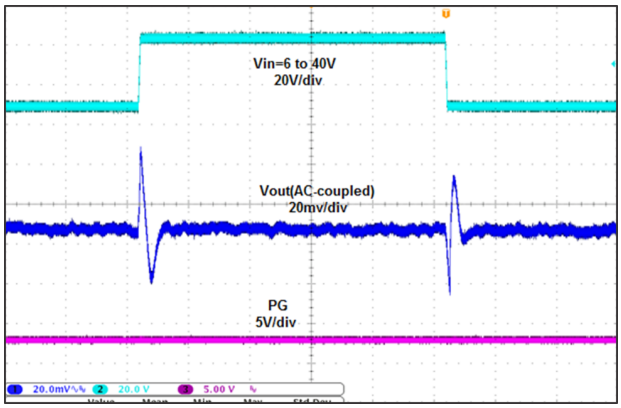
All oscilloscope waveforms were taken at room temperature.

Figure 15. Load Transient Response, 10 ms/div



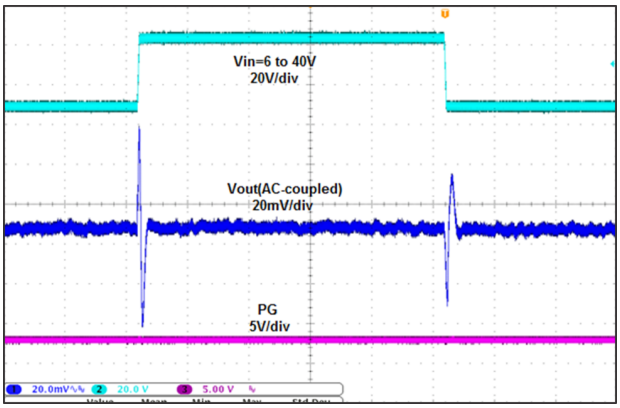
All oscilloscope waveforms were taken at room temperature.

Figure 16. Load Transient Response, 10 ms/div



All oscilloscope waveforms were taken at room temperature.

Figure 17. Line Transient Response, I_L = 1 mA, 1 V/µs



All oscilloscope waveforms were taken at room temperature.

Figure 18. Line Transient Response, I_L = 10 mA, 1 V/µs

7 Detailed Description

7.1 Overview

This device is a combination of a low-dropout linear regulator with reset function. The power-on reset initializes once the V_{OUT} output exceeds 91.6% of the target value. The power-on-reset delay is a function of the value set by an external capacitor on the CT pin before releasing the PG pin high.

7.2 Functional Block Diagrams

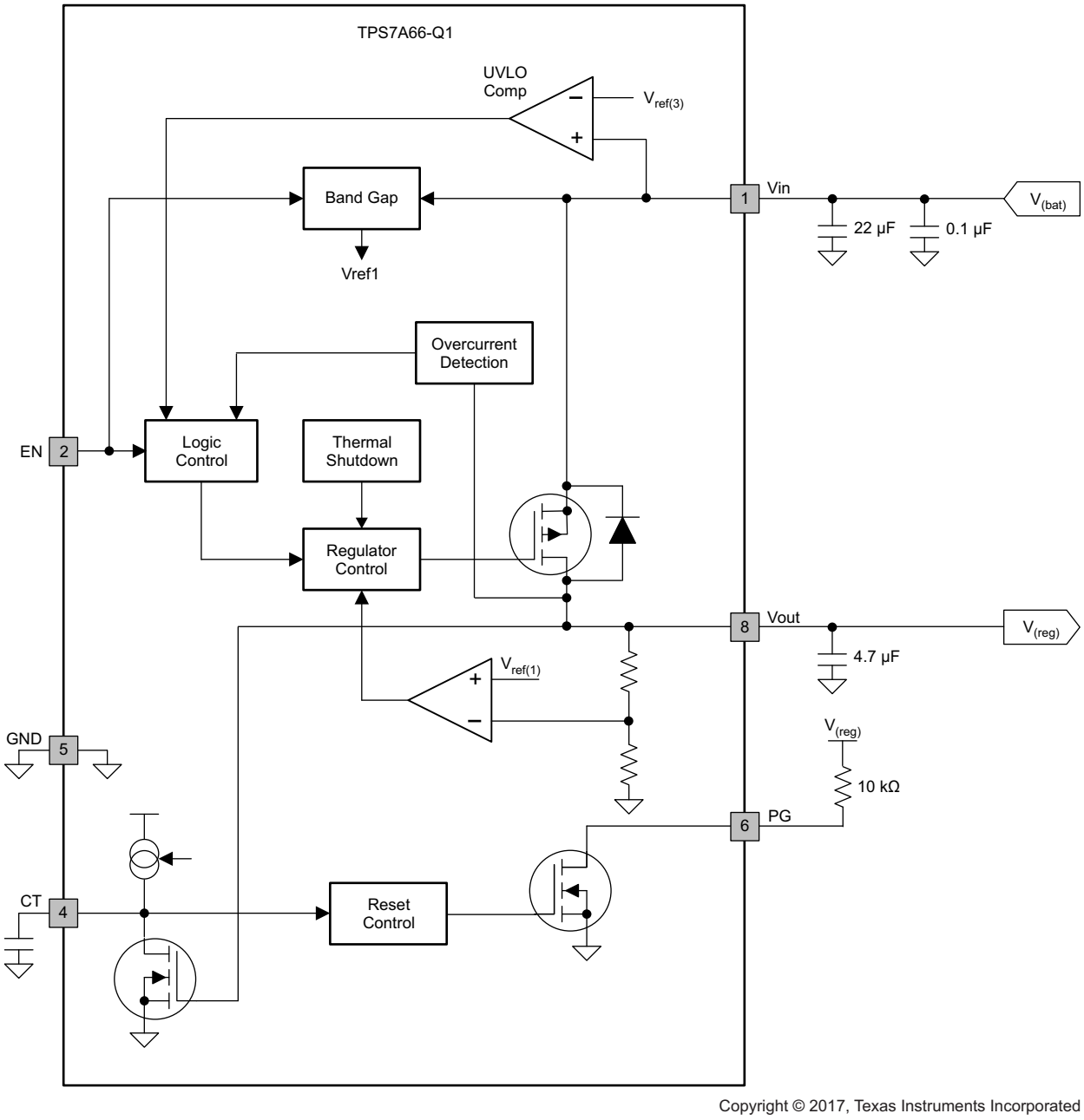


Figure 19. TPS7A66-Q1 Functional Block Diagram

Functional Block Diagrams (continued)

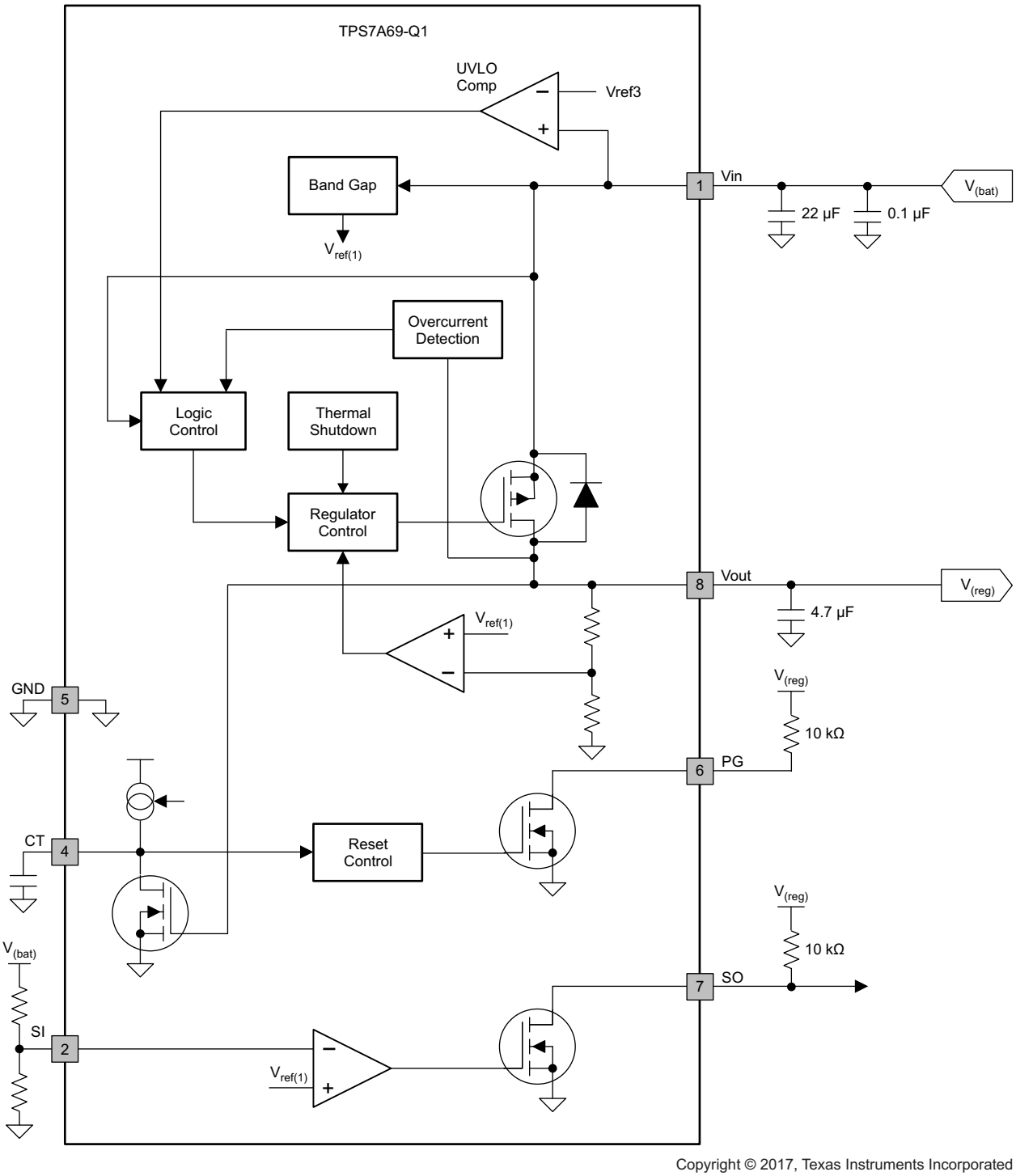


Figure 20. TPS7A69-Q1 Functional Block Diagram

7.3 Feature Description

7.3.1 Enable (EN)

This is a high-voltage-tolerant pin; high input activates the device and turns the regulator ON. One can connect this input to the VIN pin for self-bias applications.

7.3.2 Regulated Output (V_{OUT})

This is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft start incorporated to control initial current through the pass element and the output capacitor.

In the event the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

7.3.3 Power-On Reset (PG)

This is an output with an external pullup resistor to the regulated supply. The output remains low until the regulated V_{OUT} has exceeded approximately 90% of the set value and the power-on-reset delay has expired. The on-chip oscillator presets the delay. The regulated output falling below the 90% level asserts this output low after a short de-glitch time of approximately 250 µs (typical).

7.3.4 Reset Delay Timer (CT)

An external capacitor on this pin sets the timer delay before the reset pin is asserted high. The constant output current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator. If this pin is open, the default delay time is 290 µs (typ). After releasing the PG pin high, the capacitor on this pin discharges, thus allowing the capacitor to charge from approximately 0.2 V for the next power-on-reset delay-timer function.

An external capacitor, CT, defines the reset-pulse delay time, $t_{(POR)}$, with the charge time of:

$$t_{(POR)} = \frac{C_{(CT)} \times 1\,V}{1\,\mu A} \quad (1)$$

The power-on reset initializes once the output V_{OUT} exceeds 91.6% of the programmed value. The power-on-reset delay is a function of the value set by an external capacitor on the CT pin before the releasing of the PG pin high.

Feature Description (continued)

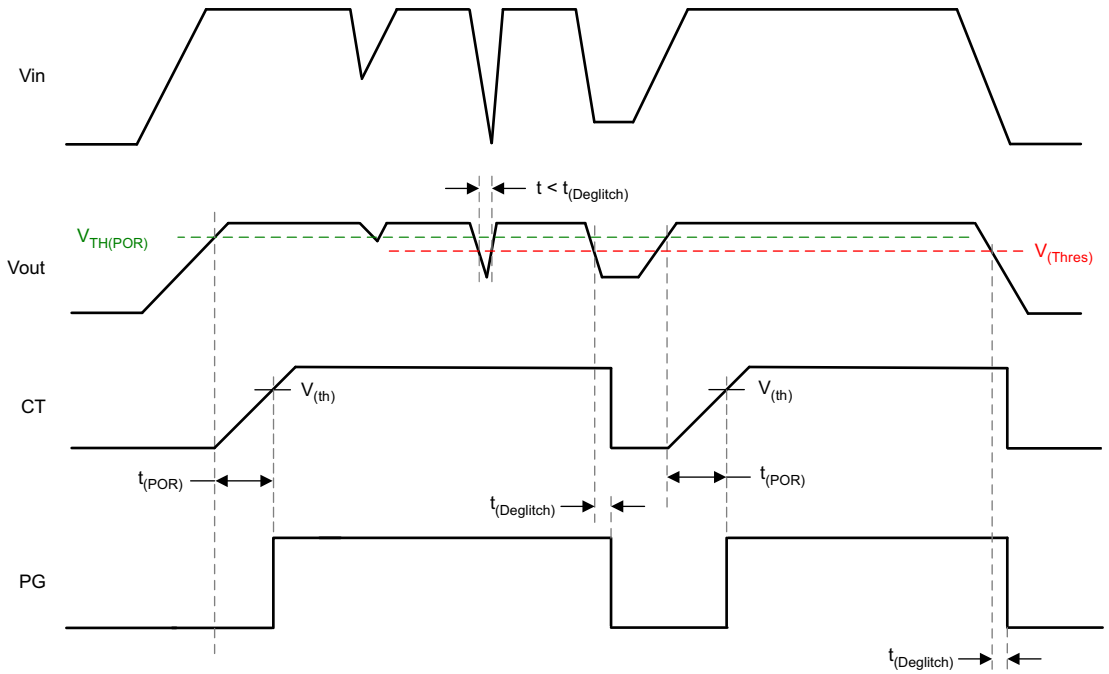


Figure 21. Conditions for Activation of Reset

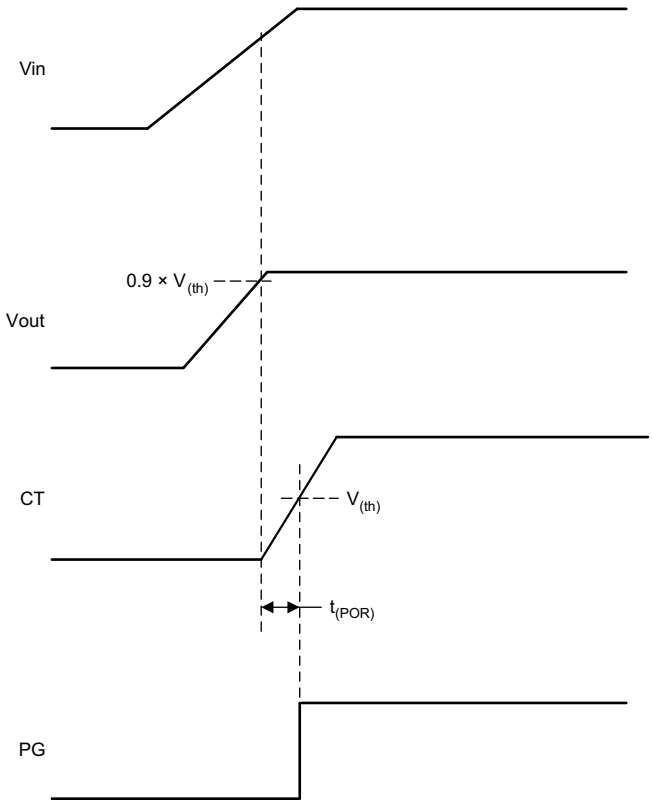


Figure 22. External Programmable Reset Delay

Feature Description (continued)

7.3.5 Sense Comparator (SI and SO for TPS7A69-Q1)

The sense comparator compares the input signal with an internal voltage reference of 1.223 V for rising and 1.123 V for falling threshold. The use of an external voltage divider makes this comparator very flexible in the application.

The device can supervise the input voltage either before or after the protection diode and give additional information to the microprocessor, like low-voltage warnings.

The regulator operates in low-power mode when the output load is below 2 mA (typical, 1-mA to 10-mA range). In this mode, the regulator output tolerance is approximately V_{OUT} ± 1%.

7.3.6 Adjustable Output Voltage (FB for TPS7A6601-Q1)

One can select an output voltage between 1.5 V and 5 V by using an external resistor divider. Calculate the output voltage using the following equation, where $V_{(FB)}$ = 1.223 V. The recommendation for R1 and R2 is that both be less than 100 kΩ.

$$V_{(Vout)} = V_{(FB)} \times \left(1 + \frac{R1}{R2}\right) \quad (2)$$

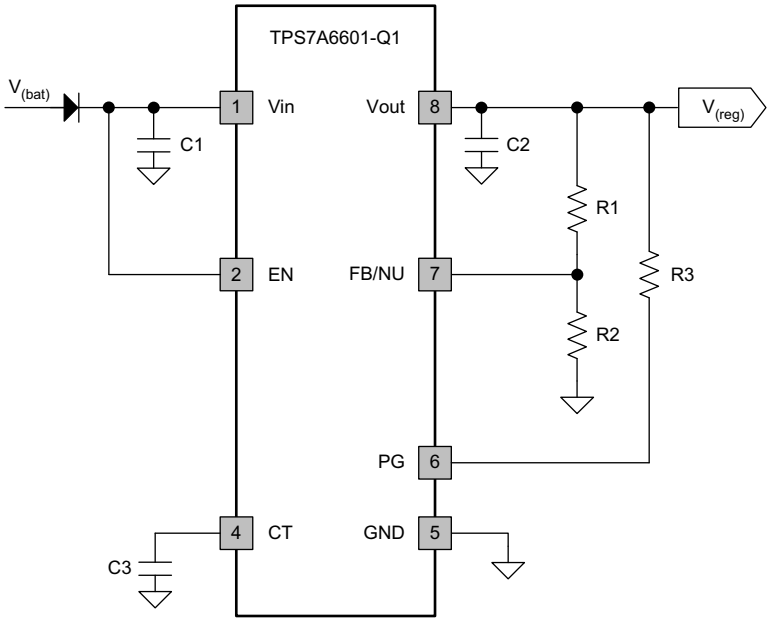


Figure 23. External Feedback Resistor Divider

7.3.7 Undervoltage Shutdown

There is an internally fixed undervoltage shutdown threshold. Undervoltage shutdown activates when the input voltage on VIN drops below $V_{(VinUVLO)}$. This ensures the regulator is not latched into an unknown state during low input supply voltage. If the input voltage has a negative transient which drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence once the input voltage is above the required levels.

7.3.8 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current (I_O) and switch resistance ($R_{(SW)}$). This allows for a smaller input capacitor and can possibly eliminate the need of using a boost convertor during cold-crank conditions.

Feature Description (continued)

7.3.9 Thermal Shutdown

These devices incorporate a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point, the output turns on again.

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. Cooling of the junction temperature to approximately 150°C enables the output circuitry. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

The purpose of the design of the internal protection circuitry of the TPS7A66-Q1, TPS7A69-Q1 is for protection against overload conditions, not as a replacement for proper heat-sinking. Continuously running the TPS7A66-Q1 or TPS7A69-Q1 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

Table 1 provides a quick comparison between the regulation, disabled, and current limit modes of operation.

Table 1. Device Functional Modes Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN(1)	I_O	T_J
Regulation(2)	$V_{IN} > V_{OUT(nom)} + V_{(dropout)}$	$V_{EN} > V_{IH}$	$I_O < I_{(Ireg-CL)}$	$T_J \le T_{J(maximum)}$
Disabled(3)	$V_{IN} < V_{(VinUVLO)}$	$V_{EN} < V_{IL}$	—	$T_J > T_{sd}$
Current limit operation	—	—	$I_O \ge I_{(Ireg-CL)}$	—

(1) EN is only required for the TPS7A66-Q1 devices.
(2) All table conditions must be met.
(3) The device is disabled when any condition is met.

7.4.1 Regulation

The device regulates the output to the nominal output voltage when all the conditions in Table 1 are met.

7.4.2 Disabled

When disabled, the pass device is turned off and the internal circuits are shut down.

7.4.3 Operation With $V_{(VinUVLO)} < V_{IN} < V_{IN(min)}$

When the input voltage is ramping up the device typically turns on when the input voltage is greater than $V_{(VinUVLO)}$ plus $V_{(UVLOhys)}$. When the input voltage is ramping down the device is specified to turn off when the input voltage becomes less than or equal to $V_{(VinUVLO)}$.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A66-Q1 and TPS7A69-Q1 devices are 150-mA low-dropout linear regulators designed for up to 40-V V_{IN} operation with only 12 µA quiescent current at no load. One can use the Pspice transient model, which is downloadable from the product folder (see *関連リンク*), for evaluating the base function of the devices. in addition, there are specific EVMs designed for these devices. Both the EVM and its user guide are available on the product folder as well.

8.2 Typical Applications

Figure 24 and Figure 26 depict typical application circuits for the TPS7A66-Q1 and TPS7A69-Q1, respectively. One may use different values of external components, depending on the end application. An application may require a larger output capacitor during fast load steps in order to prevent reset from occurring. TI recommends a low-ESR ceramic capacitor with dielectric of type X5R or X7R.

8.2.1 TPS7A66-Q1 Typical Application

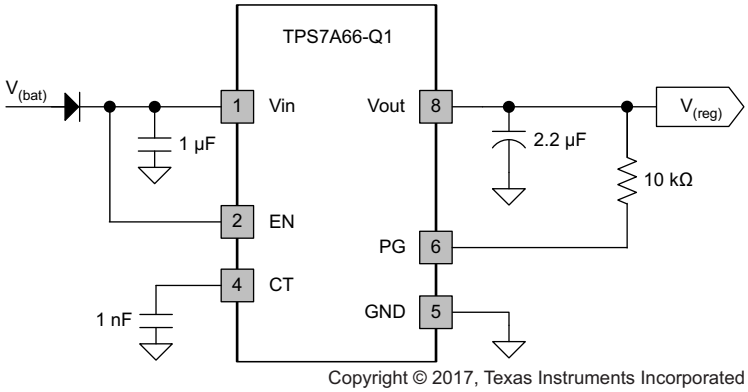


Figure 24. Typical Application Schematic for TPS7A66-Q1

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the design parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4 V to 40 V
Output voltage	3.3 V
Output current rating	150 mA
Output capacitor range	2.2 µF to 100 µF
Output capacitor ESR range	1 mΩ to 2 Ω
CT capacitor range	100 pF to 100 nF

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor
- Power-up-reset delay time

8.2.1.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 10 µF. The voltage rating must be greater than the maximum input voltage.

8.2.1.2.2 Output Capacitor

The device requires an output capacitor to stablize the output voltage. The capacitor value should be between 2.2 µF and 100 µF. The ESR range should be between 1 mΩ and 2 Ω. TI recommends to selecting a ceramic capacitor with low ESR to improve the load transient response.

8.2.1.3 Application Curve

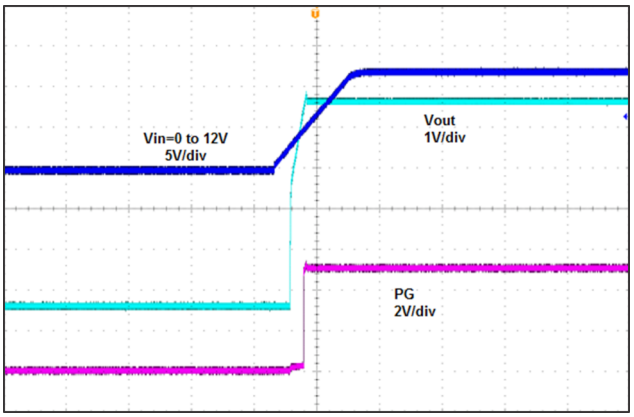


Figure 25. Power Up (5 V), 20 ms/div, I_L = 20 mA

8.2.2 TPS7A69-Q1 Typical Application

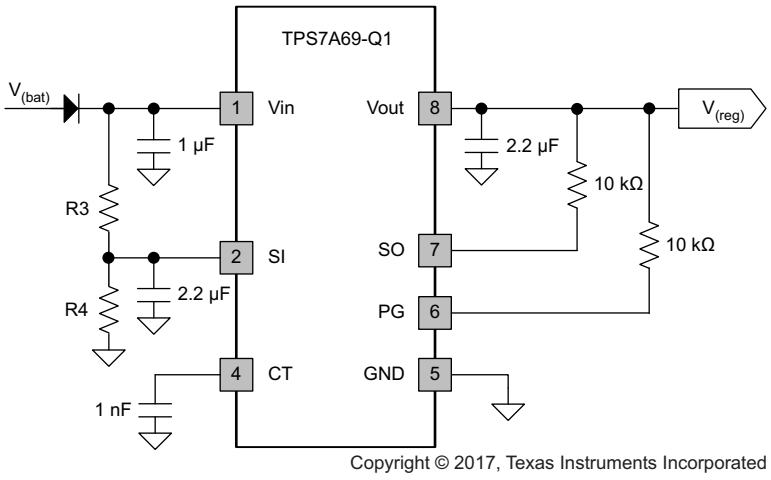


Figure 26. Typical Application Schematic for TPS7A69-Q1

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	4 V to 40 V
Output voltage	3.3 V
Output current rating	150 mA
Output capacitor range	2.2 µF to 100 µF
Output capacitor ESR range	1 mΩ to 2 Ω
CT capacitor range	100 pF to 100 nF
Low-voltage tracking threshold	6 V to 9 V

8.2.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current rating
- Input capacitor
- Output capacitor
- Power-up-reset delay time
- Low-voltage tracking threshold

8.2.2.2.1 Low-Voltage Tracking Threshold

After determining the low-voltage tracking threshold, calculate the ratio of the resistor divider connected to VIN, SI, and GND by the following equation:

$$\frac{R3}{R4} = \frac{V_{(LT)}}{1.223} - 1 \quad (3)$$

TI recommends that the values of both R3 and R4 be less than 100 kΩ.

8.2.2.3 Application Curve

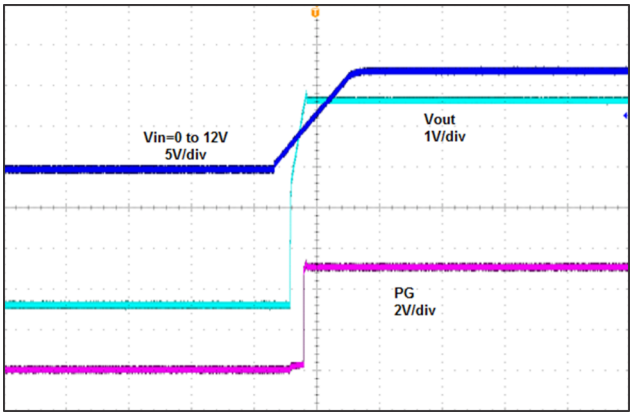


Figure 27. Power Up (5 V), 20 ms/div, I_L = 20 mA

9 Power Supply Recommendations

Design of the device is for operation from an input voltage supply with a range between 4 V and 28 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7A66-Q1 or TPS7A69-Q1 device, TI recommends adding an electrolytic capacitor with a value of 22 µF and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that may couple undesirable signals from nearby components (especially from logic and digital devices, such as microcontrollers and microprocessors); these capacitive-coupled signals may produce undesirable output voltage transients. In these cases, TI recommends the use of a fixed-voltage version of the TPS7A66-Q1, or isolation of the FB node by flooding the local PCB area with ground-plane copper to minimize any undesirable signal coupling.

10.1.1 Package Mounting

Solder pad footprint recommendations for the TPS7A66-Q1 and TPS7A69-Q1 are available at the end of this product data sheet and at www.ti.com.

10.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

For the layout of TPS7A66-Q1 and TPS7A69-Q1, place the input and output capacitors close to the devices as shown in Figure 28 and Figure 29, respectively. In order to enhance the thermal performance, TI recommends surrounding the device with some vias.

To improve ac performance such as PSRR, output noise, and transient response, TI recommends a board design with separate ground planes for VIN and VOUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Minimize equivalent series inductance (ESL) and ESR in order to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of vias and long traces because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance specified in this product data sheet, use the same layout pattern used for the TPS7A66-Q1 and TPS7A69-Q1 evaluation board, available at www.ti.com.

10.2 Layout Examples

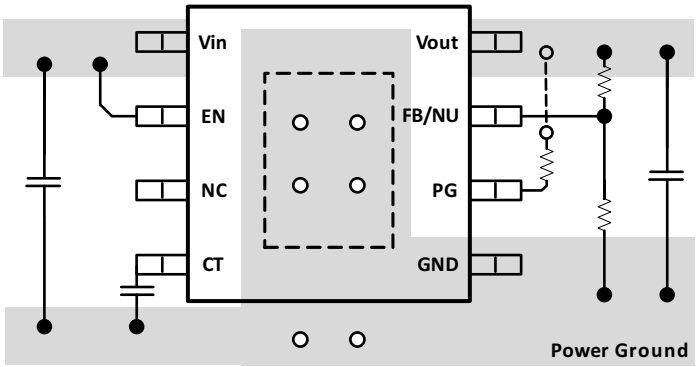


Figure 28. TPS7A66-Q1 Board Layout Diagram

Layout Examples (continued)

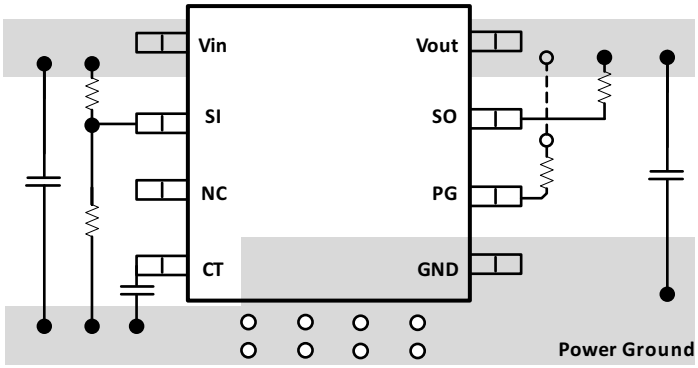


Figure 29. TPS7A69-Q1 Board Layout Diagram

10.3 Power Dissipation and Thermal Considerations

Calculate power dissipated in the device using Equation 4.

$$P_D = I_O \times (V_{(Vin)} - V_{(Vout)}) + I_{(q)} \times V_{(Vin)} \quad (4)$$

where:

P_D = continuous power dissipation
I_O = output current
V_{IN} = input voltage
V_{OUT} = output voltage

As $I_{(q)} << I_O$, therefore ignore the term $I_{(q)} \times V_{IN}$ in Equation 4.

For a device under operation at a given ambient air temperature (T_A), calculate the junction temperature (T_J) using Equation 5.

$$T_J = T_A + (R_{\theta JA} \times P_{D)}) \quad (5)$$

where:

$R_{\theta JA}$ = junction-to-ambient air thermal impedance

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_{D)}) \quad (6)$$

11 デバイスおよびドキュメントのサポート

11.1 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS7A66-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS7A69-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。***

設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.4 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A6601QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA4Q	Samples
TPS7A6633QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA2Q	Samples
TPS7A6650QDGNRQ1	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	PA1Q	Samples
TPS7A6933QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	6933	Samples
TPS7A6950QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	6950	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

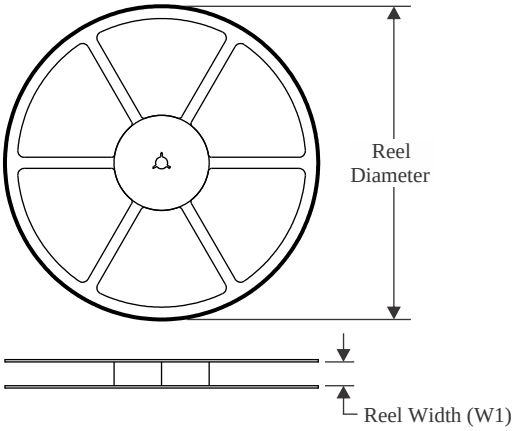
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

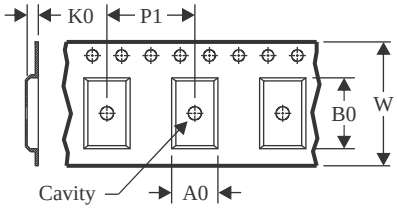
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

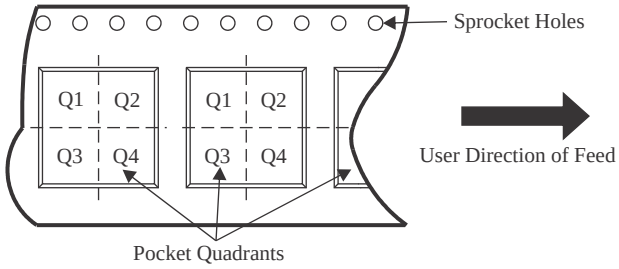


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

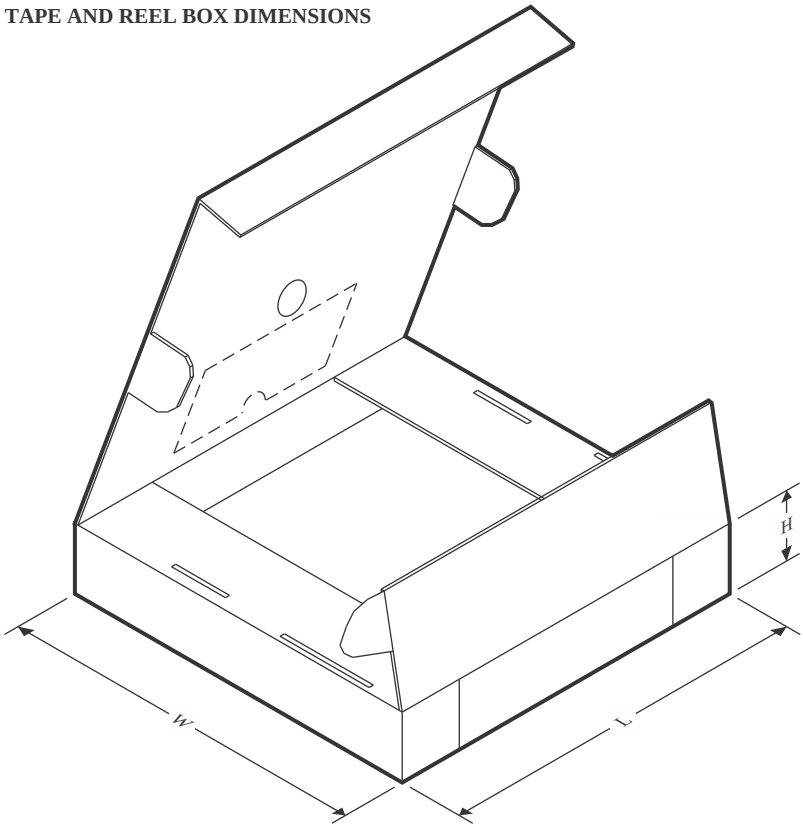
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A6601QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A6633QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A6650QDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A6933QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS7A6950QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A6601QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7A6633QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7A6650QDGNRQ1	HVSSOP	DGN	8	2500	366.0	364.0	50.0
TPS7A6933QDRQ1	SOIC	D	8	2500	356.0	356.0	35.0
TPS7A6950QDRQ1	SOIC	D	8	2500	356.0	356.0	35.0

GENERIC PACKAGE VIEW

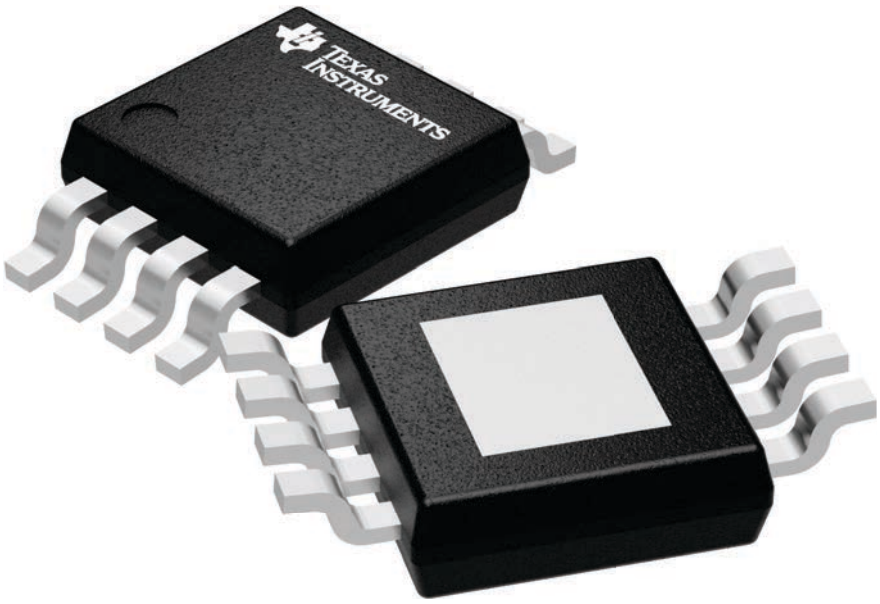
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

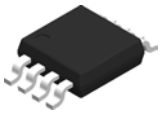
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

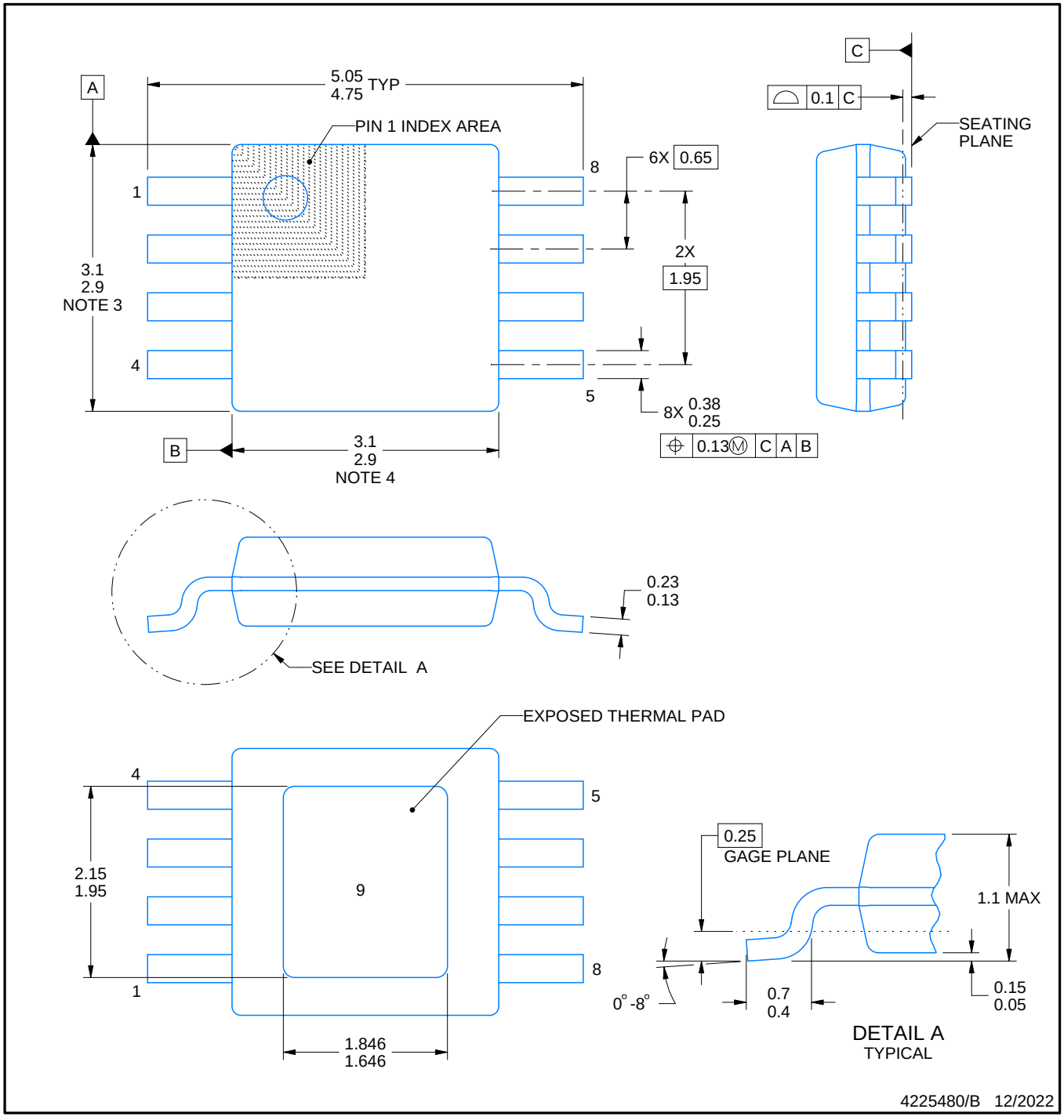
PACKAGE OUTLINE

DGN0008G



PowerPAD™ VSSOP - 1.1 mm max height

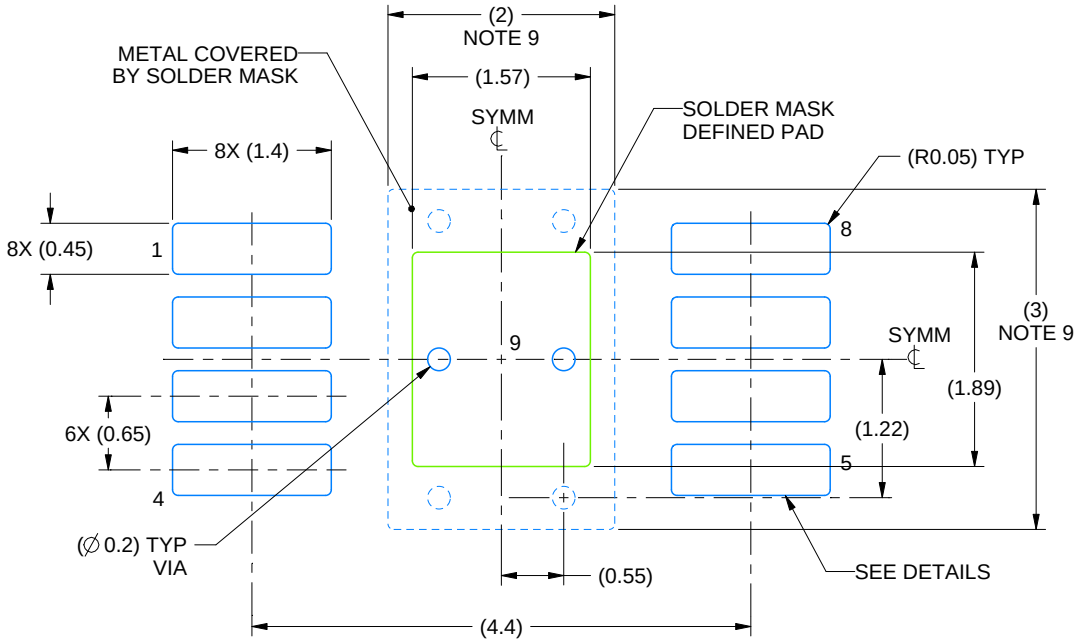
SMALL OUTLINE PACKAGE



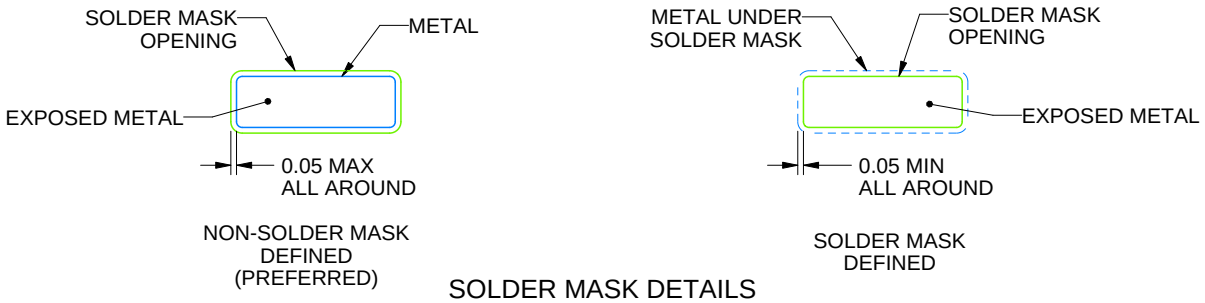
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

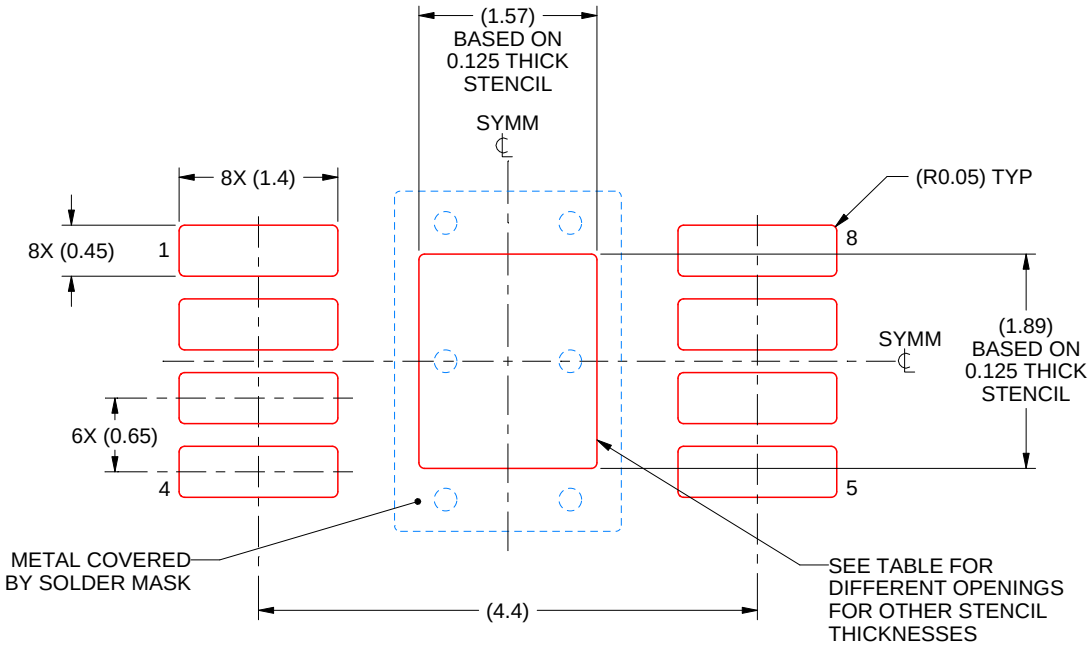


SOLDER MASK DETAILS

4225480/B 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



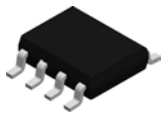
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225480/B 12/2022

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

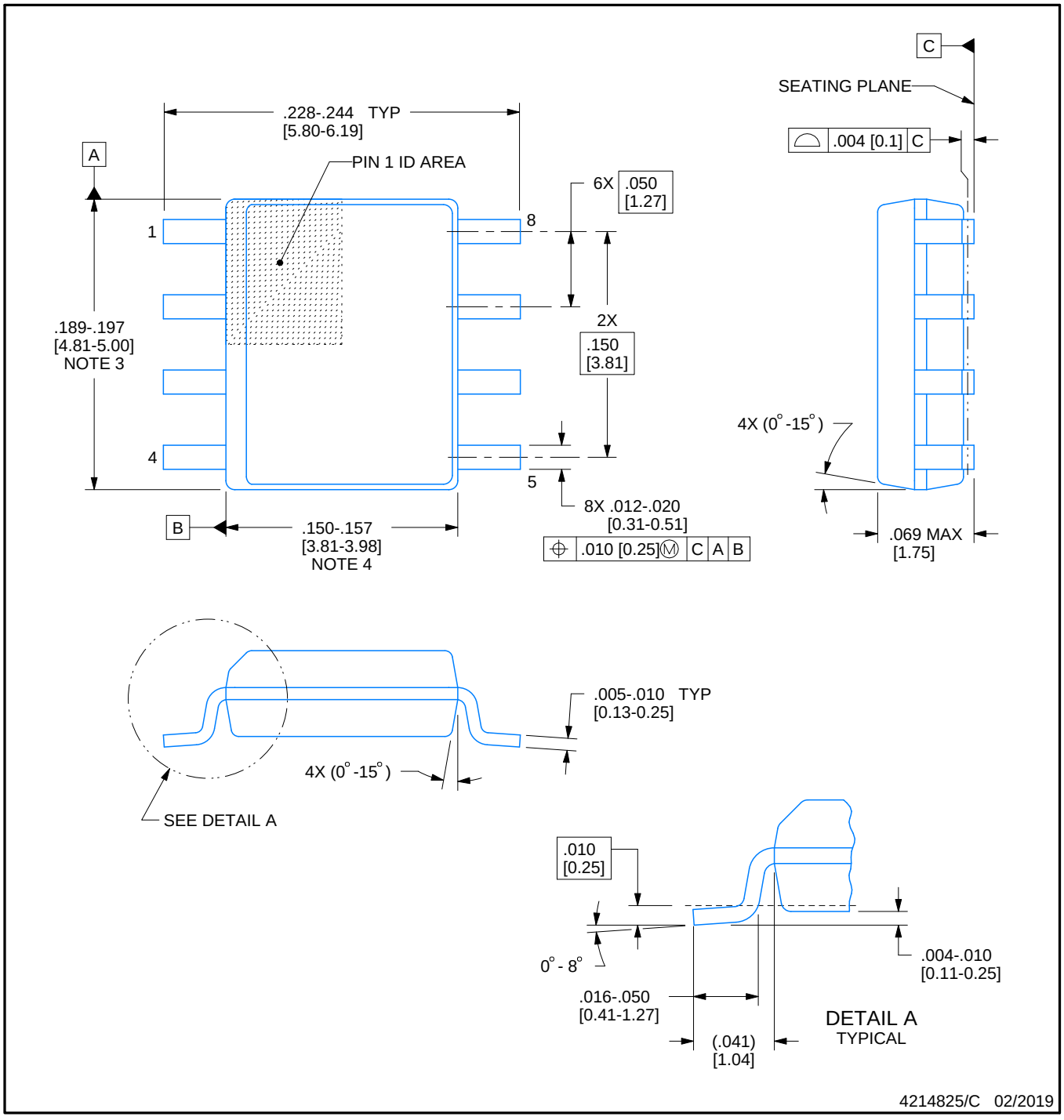


PACKAGE OUTLINE

D0008A

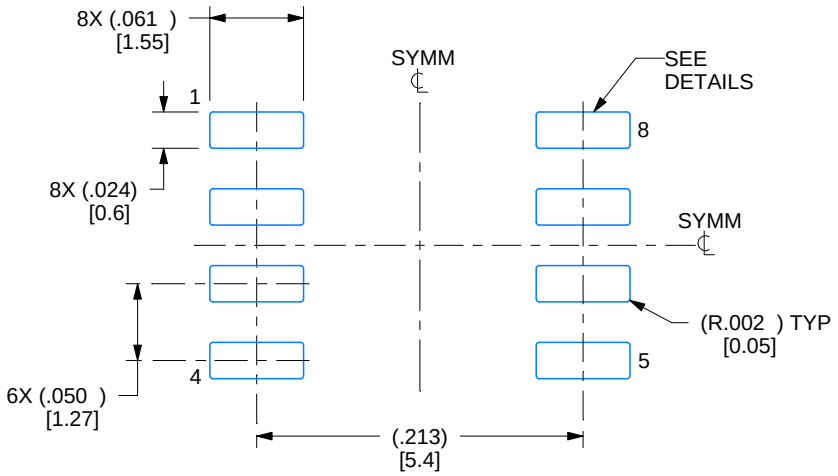
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

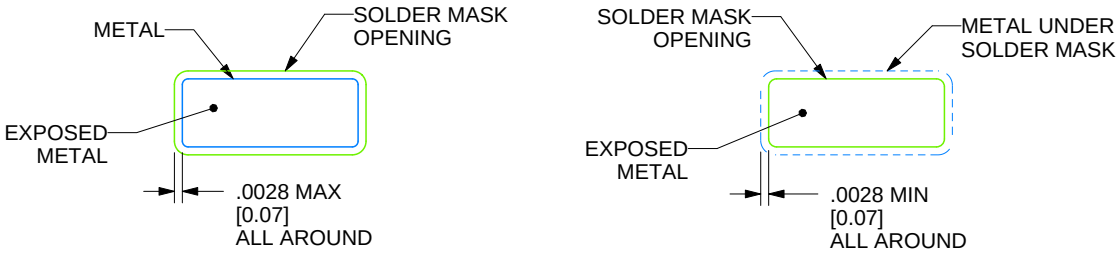


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

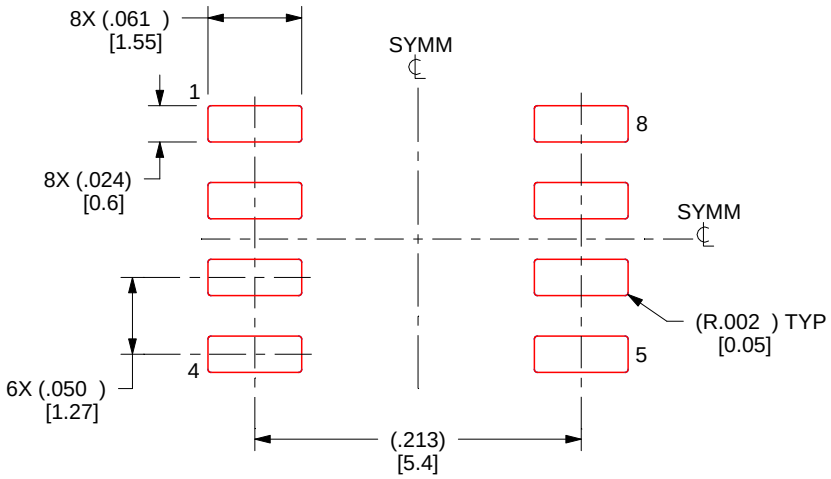
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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