OPT3001-Q1 環境光センサ(ALS)

1 特長

- 車載デバイス用にAEC-Q100認定済み
  - デバイス温度グレード 2:動作時周囲温度 -40°C～+105°C
  - デバイス温度グレード 3:動作時周囲温度 -40°C～+85°C
- 高精度の光フィルタリングにより人間の目に適合
  - IRの99%以上(標準値)を除去
- 自動フルスケール設定機能により、ソフトウェアが簡素化され、適切な構成を保証
- 測定範囲: 0.01ルクス～83kルクス
- 自動ゲイン範囲設定により、23ビットの実効ダイナミック・レンジを実現
- 12個のバイナリ重み付けフルスケール範囲設定: 範囲間の一致精度0.2%未満(標準値)
- 低い動作電流: 1.8µA (標準値)
- 動作時温度範囲 (グレード 2): -40°C～+105°C
- 動作時温度範囲 (グレード 3): -40°C～+85°C
- 機能温度範囲: -40℃～105℃
- 広い電源電圧範囲: 1.6V～3.6V
- 5.5V対応のI/O
- 柔軟な割り込みシステム
- 小さな外形: 2mm×2mm×0.65mm

2 アプリケーション

- 車載照明
- インフォテインメントおよびクラスタ
- ディスプレイのバックライト制御
- 照明制御システム
- 個人用電子機器
- レジ用電子機器
- 屋外の交通信号機および街路灯
- 家庭用照明
- カメラ

3 概要

OPT3001-Q1デバイスは可視光の強度を測定する光センサです。センサのスペクトル応答は、人間の目の明所視応答とほぼ一致し、強力な赤外線除去も備えています。

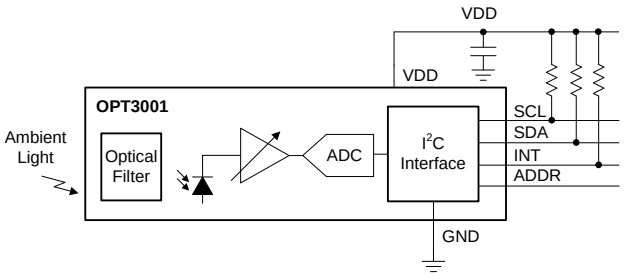
OPT3001-Q1デバイスは、人間の目の感覚に一致する照度を測定可能なシングルチップの照度計です。OPT3001-Q1デバイスは、高精度のスペクトル応答と強力なIR除去により、光源にかかわらず人間の目の感覚に一致する照度を正確に測定できます。また、強力なIR除去機能があるため、産業用のデザインで美観上の理由から暗色のガラス下にセンサを設置する必要がある場合でも、高い精度を維持できます。OPT3001-Q1デバイスは、人間の目が感じる光環境を実現するシステム向けに開発された製品です。人間の目との一致度が低く、IR除去も弱いフォトダイオード、フォトレジスタ、その他の環境光センサの代替品として理想的です。

製品情報(1)

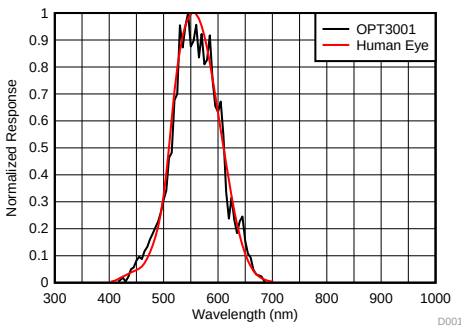
型番	パッケージ	本体サイズ(公称)
OPT3001-Q1	USON (6)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にあるパッケージ・オプションについての付録を参照してください。

ブロック図



スペクトル応答： OPT3001-Q1および肉眼



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4 改訂履歴

2017年3月 発行のものから更新 **Page**

- デバイス温度グレード 2：動作時周囲温度 -40°C～+105°C 追加 ... 1
- デバイス温度グレード 3：動作時周囲温度 -40°C～+85°C 追加 ... 1
- 追加 ... 1
- 動作時温度範囲 (グレード 2): -40°C～+105°C 追加 ... 1
- Added Operating temperature (Grade 2) to *Recommended Operating Conditions* table ... 4
- Added *Dark Response vs Temperature (Grade 2)* ... 8
- Added *Normalized Response vs Temperature (Grade 2)* ... 8
- Added *Supply Current vs Temperature (Grade 2)* ... 9
- Added *Shutdown Current vs Temperature (Grade 2)* ... 10

5 概要（続き）

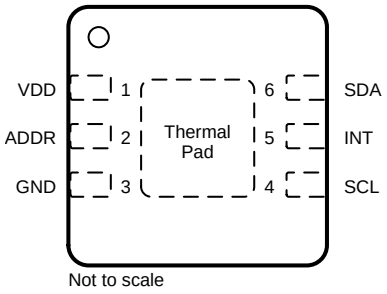
システム統合のために、柔軟なデジタル動作が可能です。連続的な測定も、単回のみの測定も実行できます。制御および割り込みシステムは自律的に動作するため、プロセッサがスリープ中でもセンサが適切なウェイクアップ・イベントを調べ、割り込みピンで通知します。デジタル出力は、I²CおよびSMBus互換の2線式シリアル・インターフェイスで通知されます。

OPT3001-Q1デバイスは消費電力が低く、電源電圧も低いため、バッテリ駆動のシステムで長時間動作可能です。

内蔵のフルスケール設定機能により、手動でフルスケール範囲を選択する必要がなく、0.01ルクスから83kルクスまでの範囲を測定できます。この機能により、23 ビットの実効ダイナミック・レンジにわたって光の測定が可能です。

6 Pin Configuration and Functions

DNP Package
6-Pin USON
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{DD}	I	Device power. Connect to a 1.6-V to 3.6-V supply.
2	ADDR	I	Address pin. This pin sets the LSBs of the I²C address.
3	GND	Power	Ground
4	SCL	I	I²C clock. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.
5	INT	O	Interrupt output, open-drain. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.
6	SDA	I/O	I²C data. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Voltage	V_{DD} to GND	–0.5	6	V
	SDA, SCL, INT, and ADDR to GND	–0.5	6	V
Current into any pin			10	mA
Temperature	Junction		150	°C
	Storage, T_{stg}	–65	150(2)	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Long exposure to temperatures higher than 105°C can cause package discoloration, spectral distortion, and measurement inaccuracy.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Operating temperature (Grade 2)	–40		105	°C
Operating temperature (Grade 3)	–40		85	°C
Operating power-supply voltage	1.6		3.6	V

7.4 Thermal Information

THERMAL METRIC(1)		OPT3001-Q1 DNP (USON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	71.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	17.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

At T_A = 25°C, V_{DD} = 3.3 V, (1), automatic full-scale range (RN[3:0] = 1100b(1)), white LED, and normal-angle incidence of light, unless otherwise specified.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPTICAL							
	Peak irradiance spectral responsivity				550		nm
	Resolution (LSB)	Lowest full-scale range, RN[3:0] = 0000b at 800 ms conversion time (1)			0.01		lux
		Lowest full-scale range, RN[3:0] = 0000b(1) at 100 ms conversion time			0.08		
	Full-scale illuminance				83 865.6		lux
	Measurement output result	0.64 lux per ADC code, 2620.80 lux full-scale (RN[3:0] = 0110)(1), 2000 lux input(2)		2812	3125	3437	ADC codes
				1800	2000	2200	lux
	Relative accuracy between gain ranges(3)				0.2%		
	Infrared response (850 nm)(2)				0.2%		
	Light source variation (incandescent, halogen, fluorescent)	Bare device, no cover glass			4%		
	Linearity	Input illuminance > 40 lux			2%		
		Input illuminance < 40 lux			5%		
	Measurement drift across temperature	Input illuminance = 2000 lux			0.01		%/°C
	Dark condition, ADC output	For Conversion Time = 800 ms			0	3	ADC codes
		For Conversion Time = 100 ms			0	1	
	Half-power angle	50% of full-power reading			47		degrees
PSRR	Power-supply rejection ratio	V_{DD} at 3.6 V and 1.6 V			0.1		%/V(4)
POWER SUPPLY							
V_{DD}	Operating range			1.6		3.6	V
V_{I^2C}	Operating range of I^2C pullup resistor	I^2C pullup resistor, $V_{DD} \le V_{I^2C}$		1.6		5.5	V
I_Q	Quiescent current	Dark	Active, V_{DD} = 3.6 V		1.8	2.5	µA
			Shutdown (M[1:0] = 00)(1), V_{DD} = 3.6 V		0.3	0.47	µA
		Full-scale lux	Active, V_{DD} = 3.6 V		3.7		µA
			Shutdown, (M[1:0] = 00)(1)		0.4		µA
POR	Power-on-reset threshold	T_A = 25°C			0.8		V
DIGITAL							
	I/O pin capacitance				3		pF
	Total integration time(5)	(CT = 1)(1), 800-ms mode, fixed lux range		720	800	880	ms
		(CT = 0)(1), 100-ms mode, fixed lux range		90	100	110	ms
V_{IL}	Low-level input voltage (SDA, SCL, and ADDR)			0		0.3 × V_{DD}	V
V_{IH}	High-level input voltage (SDA, SCL, and ADDR)			0.7 × V_{DD}		5.5	V
I_{IL}	Low-level input current (SDA, SCL, and ADDR)				0.01	0.25(6)	µA
V_{OL}	Low-level output voltage (SDA and INT)	I_{OL}= 3 mA				0.32	V
I_{ZH}	Output logic high, high-Z leakage current (SDA, INT)	Pin at V_{DD}			0.01	0.25(6)	µA
TEMPERATURE							
	Specified temperature range	Grade 2		–40		105	°C
		Grade 3		–40		85	°C

(1) Refers to a control field within the configuration register.
(2) Tested with the white LED calibrated to 2k lux and an 850-nm LED.
(3) Characterized by measuring fixed near-full-scale light levels on the higher adjacent full-scale range setting.
(4) PSRR is the percent change of the measured lux output from its current value, divided by the change in power supply voltage, as characterized by results from 3.6-V and 1.6-V power supplies.
(5) The conversion time, from start of conversion until the data are ready to be read, is the integration time plus 3 ms.
(6) The specified leakage current is dominated by the production test equipment limitations. Typical values are much smaller.

7.6 Timing Requirements(1)

		MIN	TYP	MAX	UNIT
I²C FAST MODE					
f_{SCL}	SCL operating frequency	0.01		0.4	MHz
t_{BUF}	Bus free time between stop and start	1300			ns
t_{HDSTA}	Hold time after repeated start	600			ns
t_{SUSTA}	Setup time for repeated start	600			ns
t_{SUSTO}	Setup time for stop	600			ns
t_{HDDAT}	Data hold time	20		900	ns
t_{SUDAT}	Data setup time	100			ns
t_{LOW}	SCL clock low period	1300			ns
t_{HIGH}	SCL clock high period	600			ns
t_{RC} and t_{FC}	Clock rise and fall time			300	ns
t_{RD} and t_{FD}	Data rise and fall time			300	ns
t_{TIMEO}	Bus timeout period. If the SCL line is held low for this duration of time, the bus state machine is reset.		28		ms
I²C HIGH-SPEED MODE					
f_{SCL}	SCL operating frequency	0.01		2.6	MHz
t_{BUF}	Bus free time between stop and start	160			ns
t_{HDSTA}	Hold time after repeated start	160			ns
t_{SUSTA}	Setup time for repeated start	160			ns
t_{SUSTO}	Setup time for stop	160			ns
t_{HDDAT}	Data hold time	20		140	ns
t_{SUDAT}	Data setup time	20			ns
t_{LOW}	SCL clock low period	240			ns
t_{HIGH}	SCL clock high period	60			ns
t_{RC} and t_{FC}	Clock rise and fall time			40	ns
t_{RD} and t_{FD}	Data rise and fall time			80	ns
t_{TIMEO}	Bus timeout period. If the SCL line is held low for this duration of time, the bus state machine is reset.		28		ms

(1) All timing parameters are referenced to low and high voltage thresholds of 30% and 70%, respectively, of final settled value.

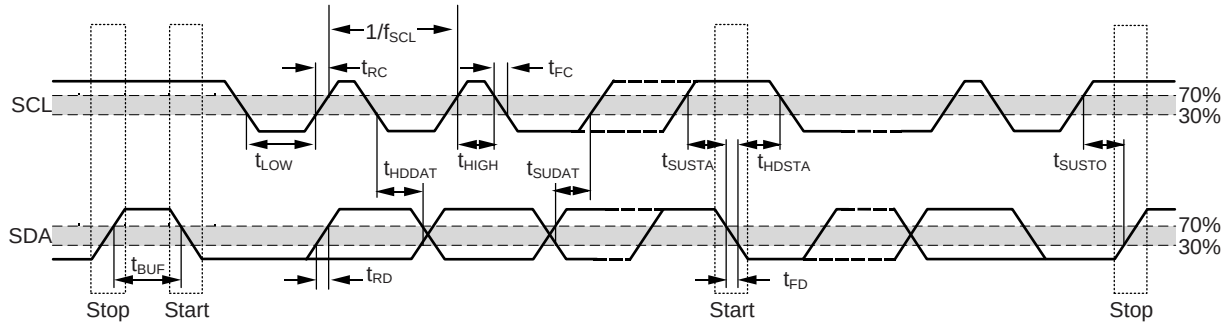


Figure 1. I²C Detailed Timing Diagram

7.7 Typical Characteristics

At T_A = 25°C, V_{DD} = 3.3 V, 800-ms conversion time (CT = 1), automatic full-scale range (RN[3:0] = 1100b), white LED, and normal-angle incidence of light, unless otherwise specified.

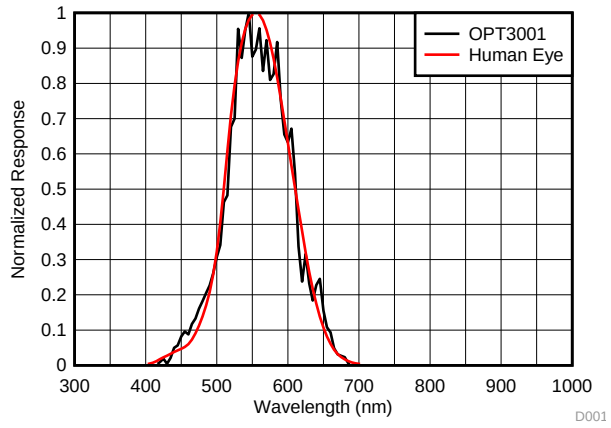


Figure 2. Spectral Response vs Wavelength

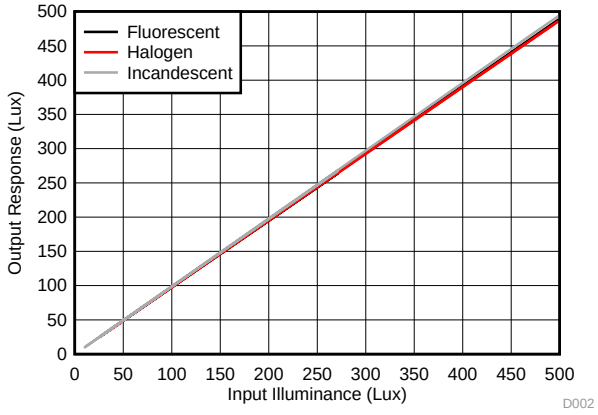


Figure 3. Output Response vs Input Illuminance, Multiple Light Sources: Fluorescent, Halogen, Incandescent

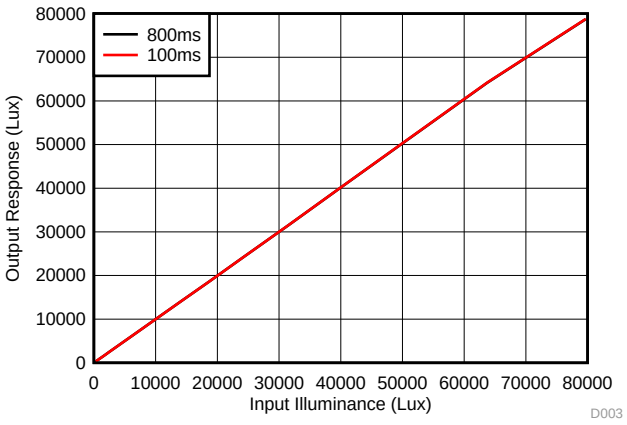


Figure 4. Output Response vs Input Illuminance: Entire Range = 0 lux to 83k lux

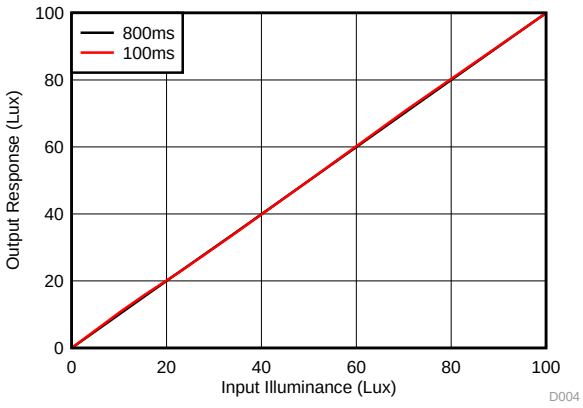


Figure 5. Output Response vs Input Illuminance: Mid Range = 0 lux to 100 lux

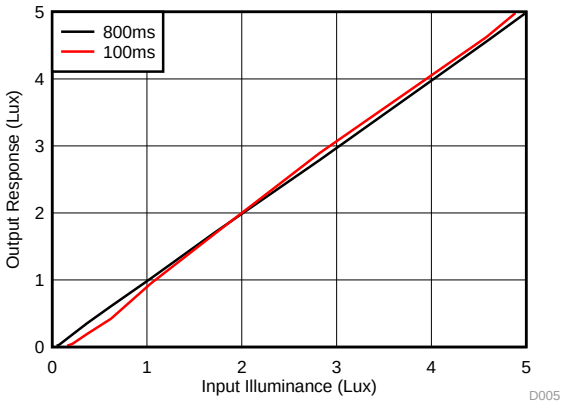
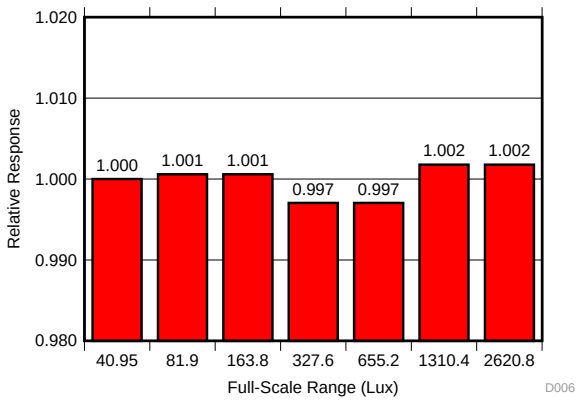


Figure 6. Output Response vs Input Illuminance: Low Range = 0 lux to 5 lux

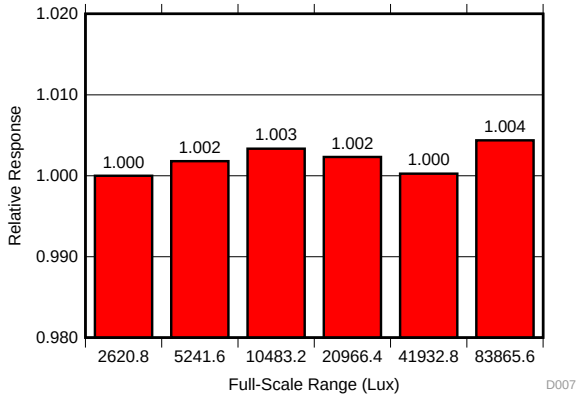


Input illuminance = 33 lux,
normalized to response of 40.95 lux full-scale

Figure 7. Full-Scale-Range Matching: Lowest 7 Ranges

Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, 800-ms conversion time (CT = 1), automatic full-scale range (RN[3:0] = 1100b), white LED, and normal-angle incidence of light, unless otherwise specified.



Input illuminance = 2490 lux,
normalized to response of 2560 lux full-scale

Figure 8. Full-Scale-Range Matching (Highest 6 Ranges)

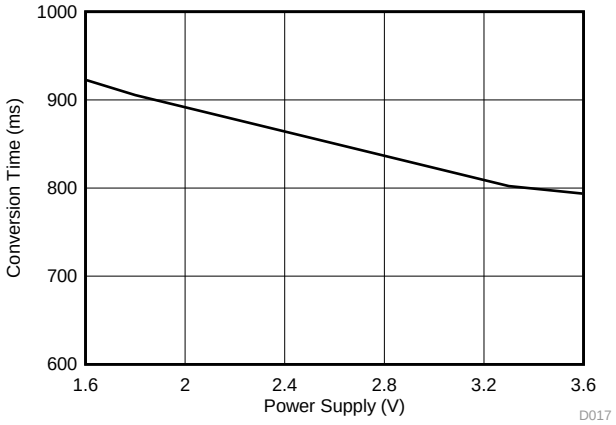
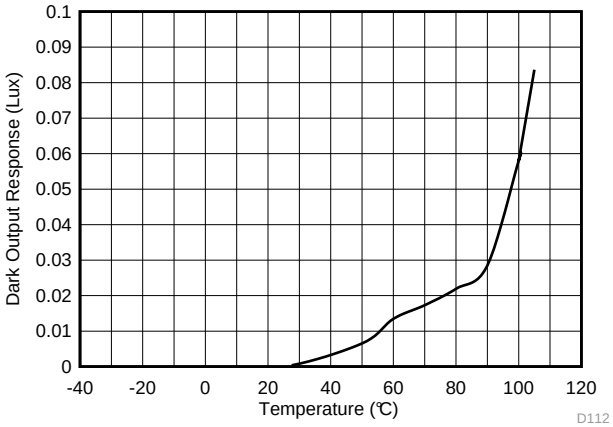
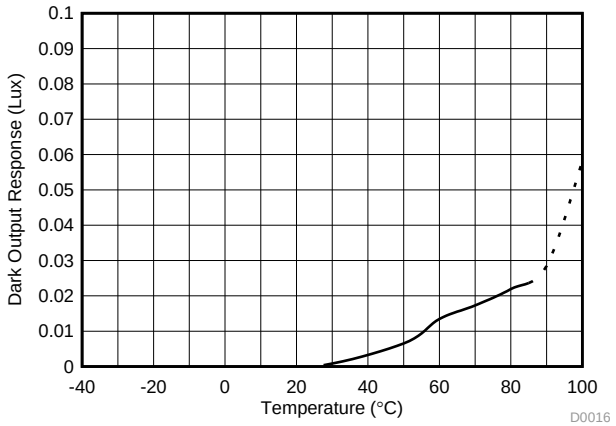


Figure 9. Conversion Time vs Power Supply



Average of 30 devices

Figure 10. Dark Response vs Temperature (Grade 2)



Average of 30 devices

Figure 11. Dark Response vs Temperature (Grade 3)

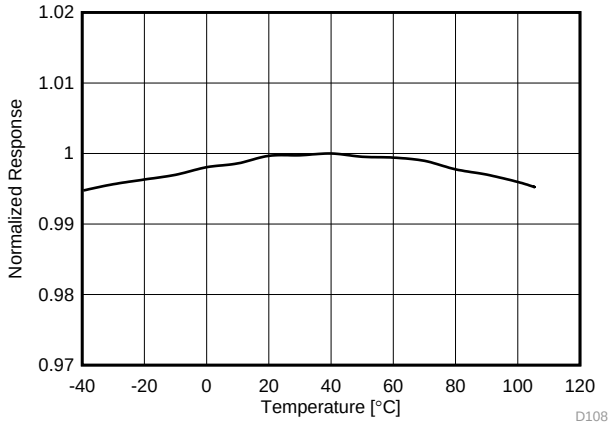


Figure 12. Normalized Response vs Temperature (Grade 2)

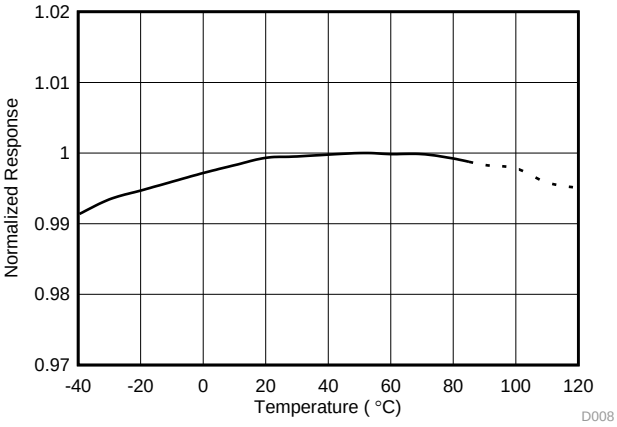


Figure 13. Normalized Response vs Temperature (Grade 3)

Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, 800-ms conversion time (CT = 1), automatic full-scale range (RN[3:0] = 1100b), white LED, and normal-angle incidence of light, unless otherwise specified.

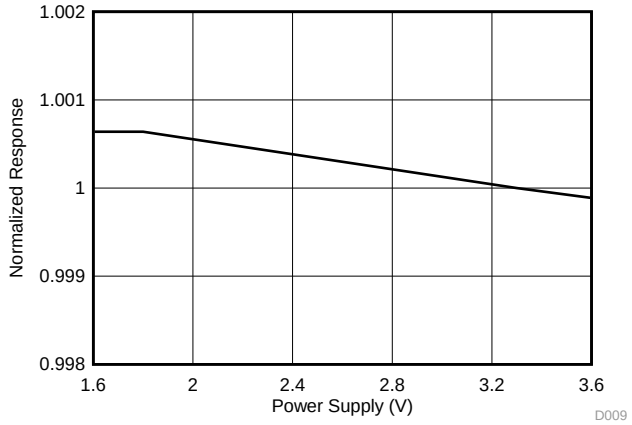


Figure 14. Normalized Response vs Power-Supply Voltage

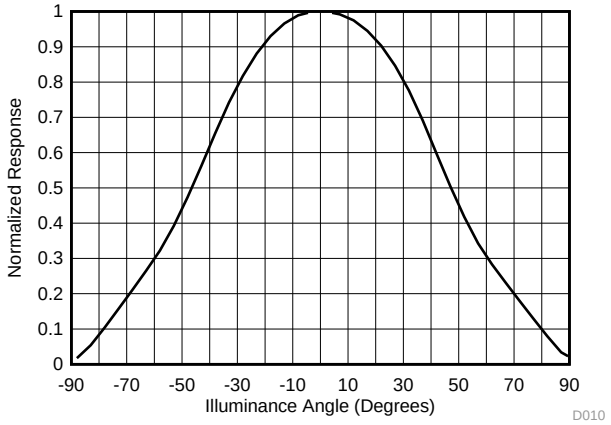
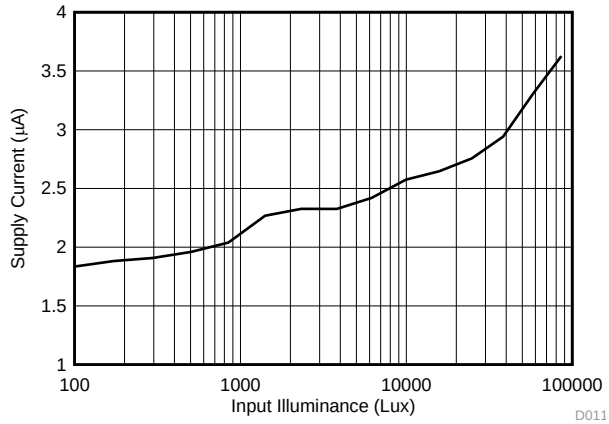
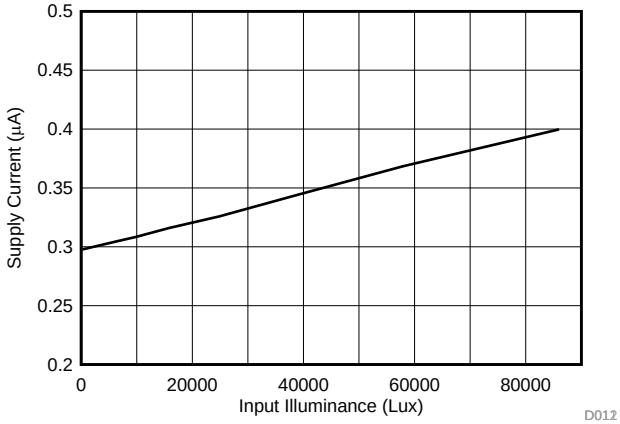


Figure 15. Normalized Response vs Illuminance Angle



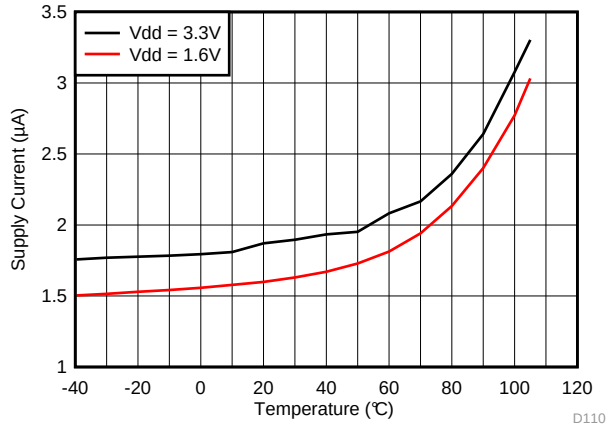
M[1:0] = 10b

Figure 16. Supply Current vs Input Illuminance



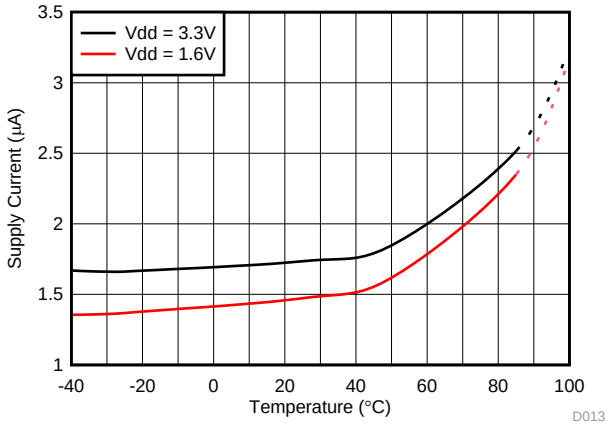
M[1:0] = 00b

Figure 17. Shutdown Current vs Input Illuminance



M[1:0] = 10b

Figure 18. Supply Current vs Temperature (Grade 2)

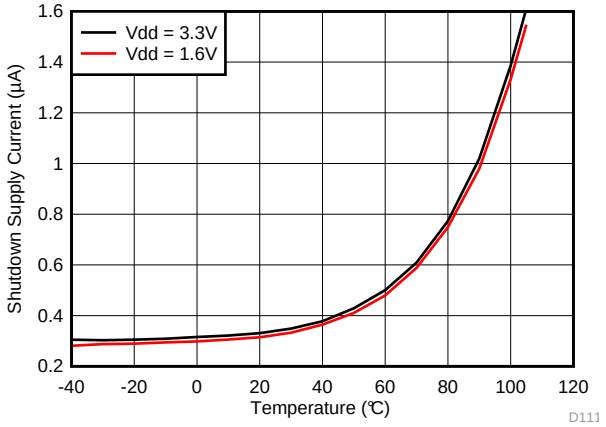


M[1:0] = 10b

Figure 19. Supply Current vs Temperature (Grade 3)

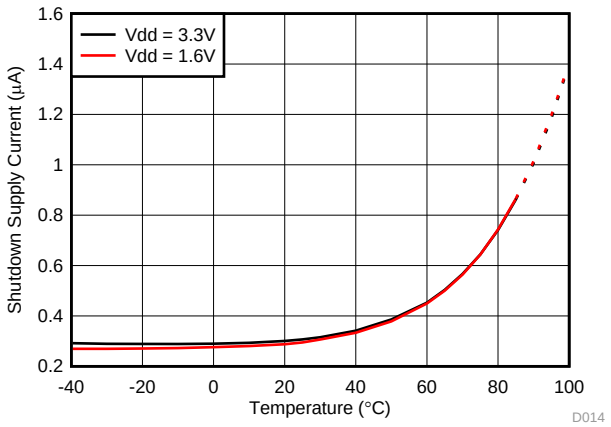
Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, 800-ms conversion time (CT = 1), automatic full-scale range (RN[3:0] = 1100b), white LED, and normal-angle incidence of light, unless otherwise specified.



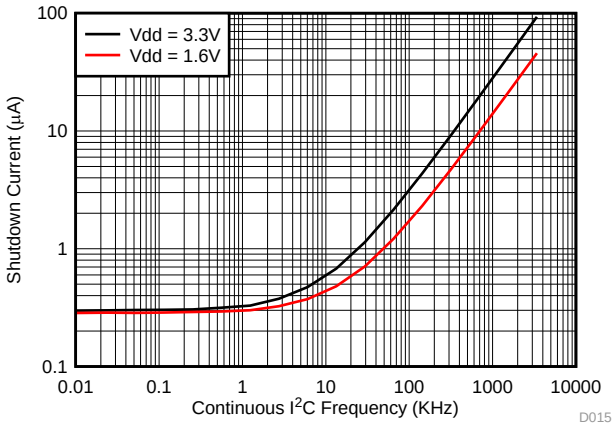
M[1:0] = 00b, input illuminance = 0 lux

Figure 20. Shutdown Current vs Temperature (Grade 2)



M[1:0] = 00b, input illuminance = 0 lux

Figure 21. Shutdown Current vs Temperature (Grade 3)



Input illuminance = 80 lux, SCL = SDA,
continuously toggled at I^2C frequency

Note: A typical application runs at a lower duty cycle and thus consumes a lower current.

Figure 22. Supply Current vs Continuous I^2C Frequency

8 Detailed Description

8.1 Overview

The OPT3001-Q1 device measures the ambient light that illuminates the device. This device measures light with a spectral response very closely matched to the human eye, and with very good infrared rejection.

Matching the sensor spectral response to that of the human eye response is vital because ambient light sensors are used to measure and help create ideal human lighting experiences. Strong rejection of infrared light, which a human does not see, is a crucial component of this matching. This matching makes the OPT3001-Q1 device especially good for operation underneath windows that are visibly dark, but infrared transmissive.

The OPT3001-Q1 device is fully self-contained to measure the ambient light and report the result in lux digitally over the I^2C bus. The result can also be used to alert a system and interrupt a processor with the INT pin. The result can also be summarized with a programmable window comparison and communicated with the INT pin.

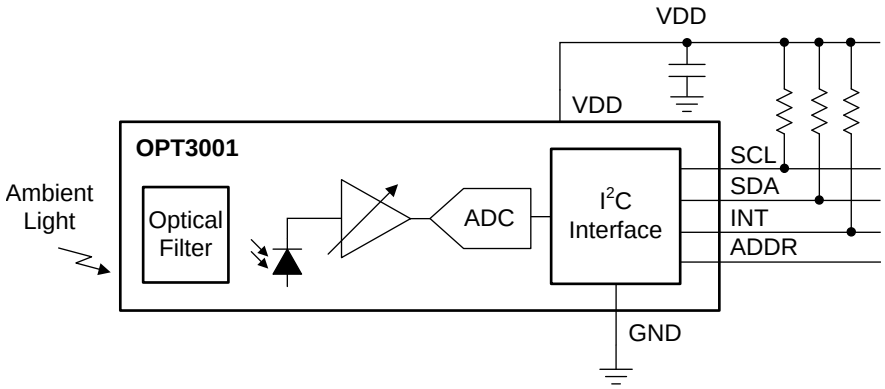
The OPT3001-Q1 device can be configured into an automatic full-scale, range-setting mode that always selects the optimal full-scale range setting for the lighting conditions. This mode frees the user from having to program their software for potential iterative cycles of measurement and readjustment of the full-scale range until optimal for any given measurement. The device can be commanded to operate continuously or in single-shot measurement modes.

The device integrates its result over either 100 ms or 800 ms, so the effects of 50-Hz and 60-Hz noise sources from typical light bulbs are nominally reduced to a minimum.

The device starts up in a low-power shutdown state, such that the OPT3001-Q1 device only consumes active-operation power after being programmed into an active state.

The OPT3001-Q1 optical filtering system is not excessively sensitive to non-ideal particles and micro-shadows on the optical surface. This reduced sensitivity is a result of the relatively minor device dependency on uniform-density optical illumination of the sensor area for infrared rejection. Proper optical surface cleanliness is always recommended for best results on all optical devices.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Human Eye Matching

The OPT3001-Q1 spectral response closely matches that of the human eye. If the ambient light sensor measurement is used to help create a good human experience, or create optical conditions that are optimal for a human, the sensor must measure the same spectrum of light that a human sees.

The device also has excellent infrared light (IR) rejection. This IR rejection is especially important because many real-world lighting sources have significant infrared content that humans do not see. If the sensor measures infrared light that the human eye does not see, then a true human experience is not accurately represented.

Furthermore, if the ambient light sensor is hidden underneath a dark window (such that the end-product user cannot see the sensor) the infrared rejection of the OPT3001-Q1 device becomes significantly more important because many dark windows attenuate visible light but transmit infrared light. This attenuation of visible light and lack of attenuation of IR light amplifies the ratio of the infrared light to visible light that illuminates the sensor. Results can still be well matched to the human eye under this condition because of the high infrared rejection of the OPT3001-Q1 device.

8.3.2 Automatic Full-Scale Range Setting

The OPT3001-Q1 device has an automatic full-scale range setting feature that eliminates the need to predict and set the optimal range for the device. In this mode, the OPT3001-Q1 device automatically selects the optimal full-scale range for the given lighting condition. The OPT3001-Q1 device has a high degree of result matching between the full-scale range settings. This matching eliminates the problem of varying results or the need for range-specific, user-calibrated gain factors when different full-scale ranges are chosen. For further details, see the *Automatic Full-Scale Setting Mode* section.

8.3.3 Interrupt Operation, INT Pin, and Interrupt Reporting Mechanisms

The device has an interrupt reporting system that allows the processor connected to the I^2C bus to go to sleep, or otherwise ignore the device results, until a user-defined event occurs that requires possible action. Alternatively, this same mechanism can also be used with any system that can take advantage of a single digital signal that indicates whether the light is above or below levels of interest.

The interrupt event conditions are controlled by the high-limit and low-limit registers, as well as the configuration register latch and fault count fields. The results of comparing the result register with the high-limit register and low-limit register are referred to as *fault events*. The fault count register dictates how many consecutive same-result fault events are required to trigger an interrupt event and subsequently change the state of the interrupt reporting mechanisms, which are the INT pin, the flag high field, and the flag low field. The latch field allows a choice between a latched window-style comparison and a transparent hysteresis-style comparison.

The INT pin has an open-drain output, which requires the use of a pull-up resistor. This open-drain output allows multiple devices with open-drain INT pins to be connected to the same line, thus creating a logical *NOR* or *AND* function between the devices. The polarity of the INT pin can be controlled with the polarity of interrupt field in the configuration register. When the POL field is set to 0, the pin operates in an active low behavior that pulls the pin low when the INT pin becomes active. When the POL field is set to 1, the pin operates in an active high behavior and becomes high impedance, thus allowing the pin to go high when the INT pin becomes active.

Additional details of the interrupt reporting registers are described in the *Interrupt Reporting Mechanism Modes* and *Internal Registers* sections.

Feature Description (continued)

8.3.4 I²C Bus Overview

The OPT3001-Q1 device offers compatibility with both I²C and SMBus interfaces. The I²C and SMBus protocols are essentially compatible with one another. The I²C interface is used throughout this document as the primary example with the SMBus protocol specified only when a difference between the two protocols is discussed.

The OPT3001-Q1 device is connected to the bus with two pins: an SCL clock input pin and an SDA open-drain bidirectional data pin. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates start and stop conditions. To address a specific device, the master initiates a start condition by pulling the data signal line (SDA) from a high logic level to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the SCL rising edge, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an acknowledge bit by pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition. When all data are transferred, the master generates a stop condition, indicated by pulling SDA from low to high while SCL is high. The OPT3001-Q1 device includes a 28-ms timeout on the I²C interface to prevent locking up the bus. If the SCL line is held low for this duration of time, the bus state machine is reset.

8.3.4.1 Serial Bus Address

To communicate with the OPT3001-Q1 device, the master must first initiate an I²C start command. Then, the master must address slave devices via a slave address byte. The slave address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

Four I²C addresses are possible by connecting the ADDR pin to one of four pins: GND, VDD, SDA, or SCL. Table 1 summarizes the possible addresses with the corresponding ADDR pin configuration. The state of the ADDR pin is sampled on every bus communication and must be driven or connected to the desired level before any activity on the interface occurs.

Table 1. Possible I²C Addresses with Corresponding ADDR Configuration

DEVICE I²C ADDRESS	ADDR PIN
1000 100	GND
1000 101	VDD
1000 110	SDA
1000 111	SCL

8.3.4.2 Serial Interface

The OPT3001-Q1 device operates as a slave device on both the I²C bus and SMBus. Connections to the bus are made via the SCL clock input line and the SDA open-drain I/O line. The OPT3001-Q1 device supports the transmission protocol for standard mode (up to 100 kHz), fast mode (up to 400 kHz), and high-speed mode (up to 2.6 MHz). All data bytes are transmitted most-significant bits first.

The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. See the *Electrical Interface* section for further details of the I²C bus noise immunity.

8.4 Device Functional Modes

8.4.1 Automatic Full-Scale Setting Mode

The OPT3001-Q1 device has an automatic full-scale-range setting mode that eliminates the need for a user to predict and set the optimal range for the device. This mode is entered when the configuration register range number field (RN[3:0]) is set to 1100b.

The first measurement that the device takes in auto-range mode is a 10-ms range assessment measurement. The device then determines the appropriate full-scale range to take its first full measurement.

For subsequent measurements, the full-scale range is set by the result of the previous measurement. If a measurement is towards the low side of full-scale, the full-scale range is decreased by one or two settings for the next measurement. If a measurement is towards the upper side of full-scale, the full-scale range is increased by one setting for the next measurement.

If the measurement exceeds the full-scale range, resulting from a fast increasing optical transient event, the current measurement is aborted. This invalid measurement is not reported. A 10-ms measurement is taken to assess and properly reset the full-scale range. Then, a new measurement is taken with this proper full-scale range. Therefore, during a fast increasing optical transient in this mode, a measurement can possibly take longer to complete and report than indicated by the configuration register conversion time field (CT).

8.4.2 Interrupt Reporting Mechanism Modes

There are two major types of interrupt reporting mechanism modes: latched window-style comparison mode and transparent hysteresis-style comparison mode. The configuration register latch field (L) (see the configuration register, bit 4) controls which of these two modes is used. An end-of-conversion mode is also associated with each major mode type. The end-of-conversion mode is active when the two most significant bits of the threshold low register are set to 11b. The mechanisms report via the flag high and flag low fields, the conversion ready field, and the INT pin.

8.4.2.1 Latched Window-Style Comparison Mode

The latched window-style comparison mode is typically selected when using the OPT3001-Q1 device to interrupt an external processor. In this mode, a fault is recognized when the input signal is above the high-limit register or below the low-limit register. When the consecutive fault events trigger the interrupt reporting mechanisms, these mechanisms are latched, thus reporting whether the fault is the result of a high or low comparison. These mechanisms remain latched until the configuration register is read, which clears the INT pin and flag high and flag low fields. The SMBus alert response protocol, described in detail in the *SMBus Alert Response* section, clears the pin but does not clear the flag high and flag low fields. The behavior of this mode, along with the conversion ready flag, is summarized in Table 2. Note that Table 2 does not apply when the two threshold low register MSBs (see the *Transparent Hysteresis-Style Comparison Mode* section for clarification on the MSBs) are set to 11b.

Device Functional Modes (continued)

Table 2. Latched Window-Style Comparison Mode: Flag Setting and Clearing Summary(1)(2)

OPERATION	FLAG HIGH FIELD	FLAG LOW FIELD	INT PIN(3)	CONVERSION READY FIELD
The result register is above the high-limit register for fault count times. See the Result Register and the High-Limit Register for further details.	1	X	Active	1
The result register is below the low-limit register for fault count times. See the Result Register and the Low-Limit Register for further details.	X	1	Active	1
The conversion is complete with fault count criterion not met	X	X	X	1
Configuration register read(4)	0	0	Inactive	0
Configuration register write, M[1:0] = 00b (shutdown)	X	X	X	X
Configuration register write, M[1:0] > 00b (not shutdown)	X	X	X	0
SMBus alert response protocol	X	X	Inactive	X

(1) X = no change from the previous state.
(2) The high-limit register is assumed to be greater than the low-limit register. If this assumption is incorrect, the flag high field and flag low field can take on different behaviors.
(3) The INT pin depends on the setting of the polarity field (POL). The INT pin is low when the pin state is active and POL = 0 (active low) or when the pin state is inactive and POL = 1 (active high).
(4) Immediately after the configuration register is read, the device automatically resets the conversion ready field to its 0 state. Thus, if two configuration register reads are performed immediately after a conversion completion, the first reads 1 and the second reads 0.

8.4.2.2 Transparent Hysteresis-Style Comparison Mode

The transparent hysteresis-style comparison mode is typically used when a single digital signal is desired that indicates whether the input light is higher than or lower than a light level of interest. If the result register is higher than the high-limit register for a consecutive number of events set by the fault count field, the INT line is set to active, the flag high field is set to 1, and the flag low field is set to 0. If the result register is lower than the low-limit register for a consecutive number of events set by the fault count field, the INT line is set to inactive, the flag low field is set to 1, and the flag high field is set to 0. The INT pin and flag high and flag low fields do not change state with configuration reads and writes. The INT pin and flag fields continually report the appropriate comparison of the light to the low-limit and high-limit registers. The device does not respond to the SMBus alert response protocol while in either of the two transparent comparison modes (configuration register, latch field = 0). The behavior of this mode, along with the conversion ready is summarized in Table 3. Note that Table 3 does not apply when the two threshold low register MSBs (LE[3:2] from Table 11) are set to 11.

Table 3. Transparent Hysteresis-Style Comparison Mode: Flag Setting and Clearing Summary(1)(2)

OPERATION	FLAG HIGH FIELD	FLAG LOW FIELD	INT PIN(3)	CONVERSION READY FIELD
The result register is above the high-limit register for fault count times. See the Result Register and the High-Limit Register for further details.	1	0	Active	1
The result register is below the low-limit register for fault count times. See the Result Register and the Low-Limit Register for further details.	0	1	Inactive	1
The conversion is complete with fault count criterion not met	X	X	X	1
Configuration register read(4)	X	X	X	0
Configuration register write, M[1:0] = 00b (shutdown)	X	X	X	X
Configuration register write, M[1:0] > 00b (not shutdown)	X	X	X	0
SMBus alert response protocol	X	X	X	X

(1) X = no change from the previous state.
(2) The high-limit register is assumed to be greater than the low-limit register. If this assumption is incorrect, the flag high field and flag low field can take on different behaviors.
(3) The INT pin depends on the setting of the polarity field (POL). The INT pin is low when the pin state is active and POL = 0 (active low) or when the pin state is inactive and POL = 1 (active high).
(4) Immediately after the configuration register is read, the device automatically resets the conversion ready field to its 0 state. Thus, if two configuration register reads are performed immediately after a conversion completion, the first reads 1 and the second reads 0.

8.4.2.3 End-of-Conversion Mode

An end-of-conversion indicator mode can be used when every measurement is desired to be read by the processor, prompted by the INT pin going active on every measurement completion. This mode is entered by setting the most significant two bits of the low-limit register (LE[3:2] from the Low-Limit Register) to 11b. This end-of-conversion mode is typically used in conjunction with the latched window-style comparison mode. The INT pin becomes inactive when the configuration register is read or the configuration register is written with a non-shutdown parameter or in response to an SMBus alert response. Table 4 summarizes the interrupt reporting mechanisms as a result of various operations.

Table 4. End-of-Conversion Mode while in Latched Window-Style Comparison Mode: Flag Setting and Clearing Summary(1)

OPERATION	FLAG HIGH FIELD	FLAG LOW FIELD	INT PIN(2)	CONVERSION READY FIELD
The result register is above the high-limit register for fault count times. See the Result Register and the High-Limit Register for further details.	1	X	Active	1
The result register is below the low-limit register for fault count times. See the Result Register and the Low-Limit Register for further details.	X	1	Active	1
The conversion is complete with fault count criterion not met	X	X	Active	1
Configuration register read(3)	0	0	Inactive	0
Configuration register write, M[1:0] = 00b (shutdown)	X	X	X	X
Configuration register write, M[1:0] > 00b (not shutdown)	X	X	X	0
SMBus alert response protocol	X	X	Inactive	X

(1) X = no change from the previous state.
(2) The INT pin depends on the setting of the polarity field (POL). The INT pin is low when the pin state is active and POL = 0 (active low) or when the pin state is inactive and POL = 1 (active high).
(3) Immediately after the configuration register is read, the device automatically resets the conversion ready field to its 0 state. Thus, if two configuration register reads are performed immediately after a conversion completion, the first reads 1 and the second reads 0.

Note that when transitioning from end-of-conversion mode to the standard comparison modes (that is, programming LE[3:2] from 11b to 00b) while the configuration register latch field (L) is 1, a subsequent write to the configuration register latch field (L) to 0 is necessary in order to properly clear the INT pin. The latch field can then be set back to 1 if desired.

8.4.2.4 End-of-Conversion and Transparent Hysteresis-Style Comparison Mode

The combination of end-of-conversion mode and transparent hysteresis-style comparison mode can also be programmed simultaneously. The behavior of this combination is shown in Table 5.

Table 5. End-Of-Conversion Mode while in Transparent Hysteresis-Style Comparison Mode: Flag Setting and Clearing Summary(1)

OPERATION	FLAG HIGH FIELD	FLAG LOW FIELD	INT PIN(2)	CONVERSION READY FIELD
The result register is above the high-limit register for fault count times. See the Result Register and the High-Limit Register for further details.	1	0	Active	1
The result register is below the low-limit register for fault count times. See the Result Register and the Low-Limit Register for further details.	0	1	Active	1
The conversion is complete with fault count criterion not met	X	X	Active	1
Configuration register read(3)	X	X	Inactive	0
Configuration register write, M[1:0] = 00b (shutdown)	X	X	X	X
Configuration register write, M[1:0] > 00b (not shutdown)	X	X	Inactive	0
SMBus alert response protocol	X	X	X	X

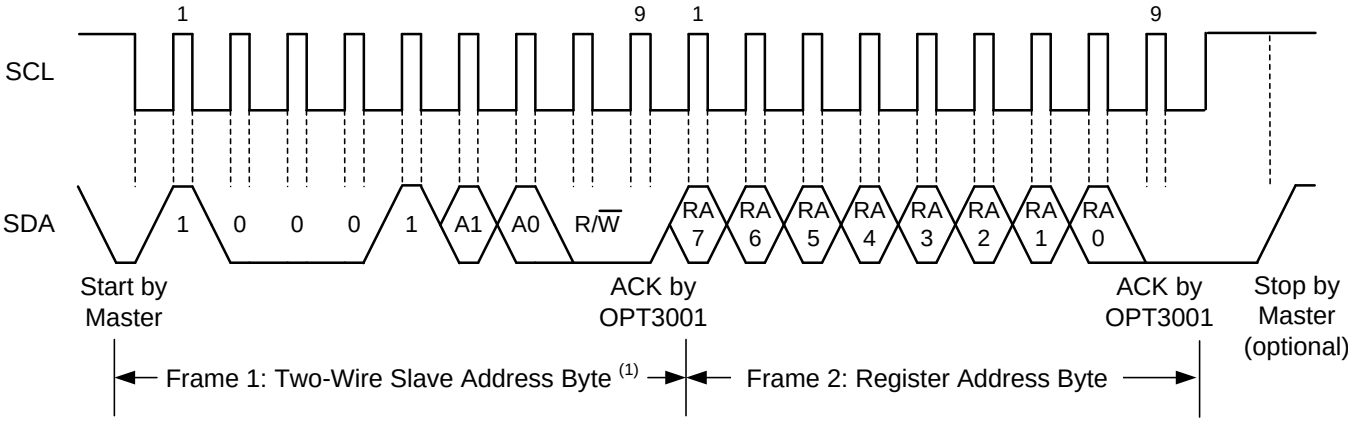
(1) X = no change from the previous state.
(2) The INT pin depends on the setting of the polarity field (POL). The INT pin is low when the pin state is active and POL = 0 (active low) or when the pin state is inactive and POL = 1 (active high).
(3) Immediately after the configuration register is read, the device automatically resets the conversion ready field to its 0 state. Thus, if two configuration register reads are performed immediately after a conversion completion, the first reads 1 and the second reads 0.

8.5 Programming

The OPT3001-Q1 device supports the transmission protocol for standard mode (up to 100 kHz), fast mode (up to 400 kHz), and high-speed mode (up to 2.6 MHz). Fast and standard modes are described as the default protocol, referred to as *F/S*. High-speed mode is described in the *High-Speed I²C Mode* section.

8.5.1 Writing and Reading

Accessing a specific register on the OPT3001-Q1 device is accomplished by writing the appropriate register address during the I²C transaction sequence. Refer to Table 6 for a complete list of registers and their corresponding register addresses. The value for the register address (as shown in Figure 23) is the first byte transferred after the slave address byte with the R/W bit low.



(1) The value of the slave address byte is determined by the ADDR pin setting; see Table 1.

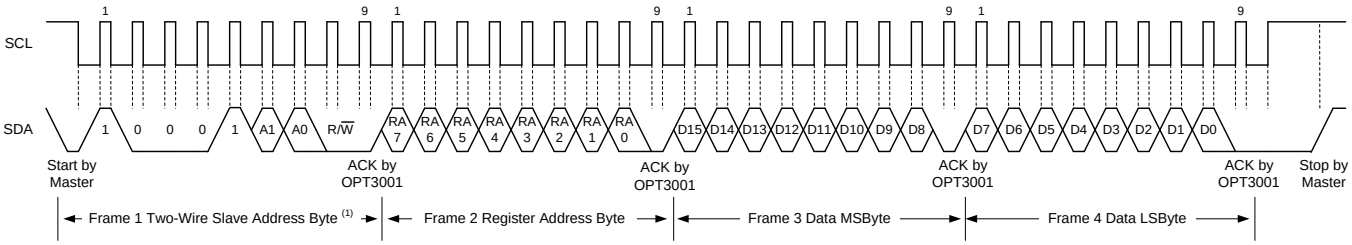
Figure 23. Setting the I²C Register Address

Writing to a register begins with the first byte transmitted by the master. This byte is the slave address with the R/W bit low. The OPT3001-Q1 device then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register that data are to be written to. The next two bytes are written to the register addressed by the register address. The OPT3001-Q1 device acknowledges receipt of each data byte. The master may terminate the data transfer by generating a start or stop condition.

When reading from the OPT3001-Q1 device, the last value stored in the register address by a write operation determines which register is read during a read operation. To change the register address for a read operation, a new partial I²C write transaction must be initiated. This partial write is accomplished by issuing a slave address byte with the R/W bit low, followed by the register address byte and a stop command. The master then generates a start condition and sends the slave address byte with the R/W bit high to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register address. This byte is followed by an acknowledge from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate the data transfer by generating a not-acknowledge after receiving any data byte, or by generating a start or stop condition. If repeated reads from the same register are desired, continually sending the register address bytes is not necessary; the OPT3001-Q1 device retains the register address until that number is changed by the next write operation.

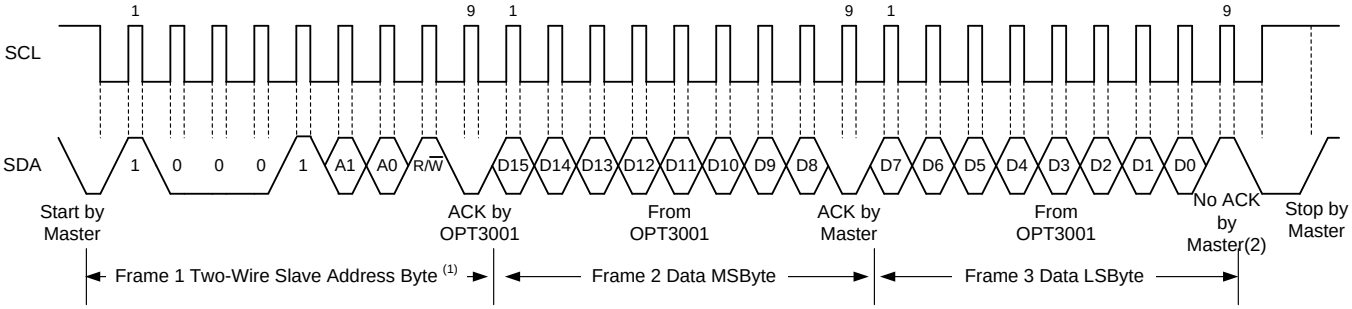
Programming (continued)

Figure 24 and Figure 25 show the write and read operation timing diagrams, respectively. Note that register bytes are sent most significant byte first, followed by the least significant byte.



(1) The value of the slave address byte is determined by the setting of the ADDR pin; see Table 1.

Figure 24. I²C Write Example



(1) The value of the slave address byte is determined by the ADDR pin setting; see Table 1.

(2) An ACK by the master can also be sent.

Figure 25. I²C Read Example

8.5.1.1 High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up resistors or active pull-up devices. The master generates a start condition followed by a valid serial byte containing the high-speed (HS) master code 0000 1XXXb. This transmission is made in either standard mode or fast mode (up to 400 kHz). The OPT3001-Q1 device does not acknowledge the HS master code but does recognize the code and switches its internal filters to support a 2.6-MHz operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.6 MHz are allowed. Instead of using a stop condition, use repeated start conditions to secure the bus in HS mode. A stop condition ends the HS mode and switches all internal filters of the OPT3001-Q1 device to support the F/S mode.

8.5.1.2 General-Call Reset Command

The I²C general-call reset allows the host controller in one command to reset all devices on the bus that respond to the general-call reset command. The general call is initiated by writing to the I²C address 0 (0000 0000b). The reset command is initiated when the subsequent second address byte is 06h (0000 0110b). With this transaction, the device issues an acknowledge bit and sets all of its registers to the power-on-reset default condition.

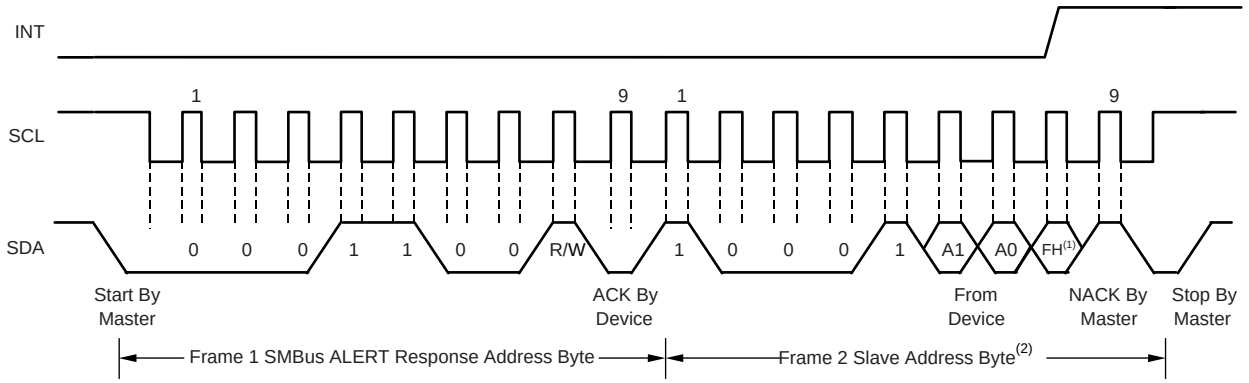
Programming (continued)

8.5.1.3 SMBus Alert Response

The SMBus alert response provides a quick identification for which device issued the interrupt. Without this alert response capability, the processor does not know which device pulled the interrupt line when there are multiple slave devices connected.

The OPT3001-Q1 device is designed to respond to the SMBus alert response address, when in the latched window-style comparison mode (configuration register, latch field = 1). The OPT3001-Q1 device does not respond to the SMBus alert response when in transparent mode (configuration register, latch field = 0).

The response behavior of the OPT3001-Q1 device to the SMBus alert response is shown in Figure 26. When the interrupt line to the processor is pulled to active, the master can broadcast the alert response slave address (0001 1001b). Following this alert response, any slave devices that generated an alert identify themselves by acknowledging the alert response and sending their respective I^2C address on the bus. The alert response can activate several different slave devices simultaneously. If more than one slave attempts to respond, bus arbitration rules apply. The device with the lowest address wins the arbitration. If the OPT3001-Q1 device loses the arbitration, the device does not acknowledge the I^2C transaction and its INT pin remains in an active state, prompting the I^2C master processor to issue a subsequent SMBus alert response. When the OPT3001-Q1 device wins the arbitration, the device acknowledges the transaction and sets its INT pin to inactive. The master can issue that same command again, as many times as necessary to clear the INT pin. See the *Interrupt Reporting Mechanism Modes* section for additional details of how the flags and INT pin are controlled. The master can obtain information about the source of the OPT3001-Q1 interrupt from the address broadcast in the above process. The flag high field (configuration register, bit 6) is sent as the final LSB of the address to provide the master additional information about the cause of the OPT3001-Q1 interrupt. If the master requires additional information, the result register or the configuration register can be queried. The flag high and flag low fields are not cleared upon an SMBus alert response.



(1) FH is the flag high field (FH) in the configuration register (see Table 10).

(2) A1 and A0 are determined by the ADDR pin; see Table 1.

Figure 26. Timing Diagram for SMBus Alert Response

8.6 Register Maps

8.6.1 Internal Registers

The device is operated over the I^2C bus with registers that contain configuration, status, and result information. All registers are 16 bits long.

There are four main registers: result, configuration, low-limit, and high-limit. There are also two ID registers: manufacturer ID and device ID. Table 6 lists these registers.

Table 6. Register Map

REGISTER	ADDRESS (Hex)(1)	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Result	00h	E3	E2	E1	E0	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0
Configuration	01h	RN3	RN2	RN1	RN0	CT	M1	M0	OVF	CRF	FH	FL	L	POL	ME	FC1	FC0
Low Limit	02h	LE3	LE2	LE1	LE0	TL11	TL10	TL9	TL8	TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
High Limit	03h	HE3	HE2	HE1	HE0	TH11	TH10	TH9	TH8	TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0
Manufacturer ID	7Eh	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Device ID	7Fh	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0

(1) Register offset and register address are used interchangeably.

8.6.1.1 Register Descriptions

NOTE

Register offset and register address are used interchangeably.

8.6.1.1.1 Result Register (offset = 00h)

This register contains the result of the most recent light to digital conversion. This 16-bit register has two fields: a 4-bit exponent and a 12-bit mantissa.

Figure 27. Result Register (Read-Only)

15	14	13	12	11	10	9	8
E3	E2	E1	E0	R11	R10	R9	R8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
R7	R6	R5	R4	R3	R2	R1	R0
R	R	R	R	R	R	R	R

LEGEND: R = Read only

Table 7. Result Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	E[3:0]	R	0h	**Exponent.** These bits are the exponent bits. Table 8 provides further details.
11:0	R[11:0]	R	000h	**Fractional result.** These bits are the result in straight binary coding (zero to full-scale).

Table 8. Full-Scale Range and LSB Size as a Function of Exponent Level

E3	E2	E1	E0	FULL-SCALE RANGE (lux)	LSB SIZE (lux per LSB)
0	0	0	0	40.95	0.01
0	0	0	1	81.90	0.02
0	0	1	0	163.80	0.04
0	0	1	1	327.60	0.08
0	1	0	0	655.20	0.16
0	1	0	1	1310.40	0.32
0	1	1	0	2620.80	0.64
0	1	1	1	5241.60	1.28
1	0	0	0	10483.20	2.56
1	0	0	1	20966.40	5.12
1	0	1	0	41932.80	10.24
1	0	1	1	83865.60	20.48

The formula to translate this register into lux is given in Equation 1:

$$lux = LSB\_Size \times R[11:0] \quad (1)$$

where:

$$LSB\_Size = 0.01 \times 2^{E[3:0]} \quad (2)$$

LSB_Size can also be taken from Table 8. The complete lux equation is shown in Equation 3:

$$lux = 0.01 \times (2^{E[3:0]}) \times R[11:0] \quad (3)$$

A series of result register output examples with the corresponding LSB weight and resulting lux are given in Table 9. Note that many combinations of exponents (E[3:0]) and fractional results (R[11:0]) can map onto the same lux result, as shown in the examples of Table 9.

Table 9. Examples of Decoding the Result Register into lux

RESULT REGISTER (Bits 15:0, Binary)	EXPONENT (E[3:0], Hex)	FRACTIONAL RESULT (R[11:0], Hex)	LSB WEIGHT (lux, Decimal)	RESULTING LUX (Decimal)
0000 0000 0000 0001b	00h	001h	0.01	0.01
0000 1111 1111 1111b	00h	FFFh	0.01	40.95
0011 0100 0101 0110b	03h	456h	0.08	88.80
0111 1000 1001 1010b	07h	89Ah	1.28	2818.56
1000 1000 0000 0000b	08h	800h	2.56	5242.88
1001 0100 0000 0000b	09h	400h	5.12	5242.88
1010 0010 0000 0000b	0Ah	200h	10.24	5242.88
1011 0001 0000 0000b	0Bh	100h	20.48	5242.88
1011 0000 0000 0001b	0Bh	001h	20.48	20.48
1011 1111 1111 1111b	0Bh	FFFh	20.48	83865.60

Note that the exponent field can be disabled (set to zero) by enabling the exponent mask (configuration register, ME field = 1) and manually programming the full-scale range (configuration register, RN[3:0] < 1100b (0Ch)), allowing for simpler operation in a manually-programmed, full-scale mode. Calculating lux from the result register contents only requires multiplying the result register by the LSB weight (in lux) associated with the specific programmed full-scale range (see Table 8). See the Low-Limit Register for details.

See the configuration register conversion time field (CT, bit 11) description for more information on lux resolution as a function of conversion time.

8.6.1.1.2 Configuration Register (offset = 01h) [reset = C810h]

This register controls the major operational modes of the device. This register has 11 fields, which are documented below. If a measurement conversion is in progress when the configuration register is written, the active measurement conversion immediately aborts. If the new configuration register directs a new conversion, that conversion is subsequently started.

Figure 28. Configuration Register

15	14	13	12	11	10	9	8
RN3	RN2	RN1	RN0	CT	M1	M0	OVF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
7	6	5	4	3	2	1	0
CRF	FH	FL	L	POL	ME	FC1	FC0
R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only

Table 10. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RN[3:0]	R/W	1100b	**Range number field (read or write).** The range number field selects the full-scale lux range of the device. The format of this field is the same as the result register exponent field (E[3:0]); see Table 8. When RN[3:0] is set to 1100b (0Ch), the device operates in automatic full-scale setting mode, as described in the *Automatic Full-Scale Setting Mode* section. In this mode, the automatically chosen range is reported in the result exponent (register 00h, E[3:0]). The device powers up as 1100 in automatic full-scale setting mode. Codes 1101b, 1110b, and 1111b (0Dh, 0Eh, and 0Fh) are reserved for future use.

Table 10. Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	CT	R/W	1b	**Conversion time field (read or write).** The conversion time field determines the length of the light to digital conversion process. The choices are 100 ms and 800 ms. A longer integration time allows for a lower noise measurement. The conversion time also relates to the effective resolution of the data conversion process. The 800-ms conversion time allows for the fully specified lux resolution. The 100-ms conversion time with full-scale ranges above 0101b for E[3:0] in the result and configuration registers also allows for the fully specified lux resolution. The 100-ms conversion time with full-scale ranges below and including 0101b for E[3:0] can reduce the effective result resolution by up to three bits, as a function of the selected full-scale range. Range 0101b reduces by one bit. Ranges 0100b, 0011b, 0010b, and 0001b reduces by two bits. Range 0000b reduces by three bits. The result register format and associated LSB weight does not change as a function of the conversion time. 0 = 100 ms 1 = 800 ms
10:9	M[1:0]	R/W	00b	**Mode of conversion operation field (read or write).** The mode of conversion operation field controls whether the device is operating in continuous conversion, single-shot, or low-power shutdown mode. The default is 00b (shutdown mode), such that upon power-up, the device only consumes operational level power after appropriately programming the device. When single-shot mode is selected by writing 01b to this field, the field continues to read 01b while the device is actively converting. When the single-shot conversion is complete, the mode of conversion operation field is automatically set to 00b and the device is shut down. When the device enters shutdown mode, either by completing a single-shot conversion or by a manual write to the configuration register, there is no change to the state of the reporting flags (conversion ready, flag high, flag low) or the INT pin. These signals are retained for subsequent read operations while the device is in shutdown mode. 00 = Shutdown (default) 01 = Single-shot 10, 11 = Continuous conversions
8	OVF	R	0b	**Overflow flag field (read-only).** The overflow flag field indicates when an overflow condition occurs in the data conversion process, typically because the light illuminating the device exceeds the programmed full-scale range of the device. Under this condition OVF is set to 1, otherwise OVF remains at 0. The field is reevaluated on every measurement. If the full-scale range is manually set (RN[3:0] field < 1100b), the overflow flag field can be set while the result register reports a value less than full-scale. This result occurs if the input light has a temporary high spike level that temporarily overloads the integrating ADC converter circuitry but returns to a level within range before the conversion is complete. Thus, the overflow flag reports a possible error in the conversion process. This behavior is common to integrating-style converters. If the full-scale range is automatically set (RN[3:0] field = 1100b), the only condition that sets the overflow flag field is if the input light is beyond the full-scale level of the entire device. When there is an overflow condition and the full-scale range is not at maximum, the OPT3001-Q1 device aborts its current conversion, sets the full-scale range to a higher level, and starts a new conversion. The flag is set at the end of the process. This process repeats until there is either no overflow condition or until the full-scale range is set to its maximum range.
7	CRF	R	0b	**Conversion ready field (read-only).** The conversion ready field indicates when a conversion completes. The field is set to 1 at the end of a conversion and is cleared (set to 0) when the configuration register is subsequently read or written with any value except one containing the shutdown mode (mode of operation field, M[1:0] = 00b). Writing a shutdown mode does not affect the state of this field; see the *Interrupt Reporting Mechanism Modes* section for more details.
6	FH	R	0b	**Flag high field (read-only).** The flag high field (FH) identifies that the result of a conversion is larger than a specified level of interest. FH is set to 1 when the result is larger than the level in the high-limit register (register address 03h) for a consecutive number of measurements defined by the fault count field (FC[1:0]). See the *Interrupt Reporting Mechanism Modes* section for more details on clearing and other behaviors of this field.
5	FL	R	0b	**Flag low field (read-only).** The flag low field (FL) identifies that the result of a conversion is smaller than a specified level of interest. FL is set to 1 when the result is smaller than the level in the low-limit register (register address 02h) for a consecutive number of measurements defined by the fault count field (FC[1:0]). See the *Interrupt Reporting Mechanism Modes* section for more details on clearing and other behaviors of this field.

Table 10. Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	L	R/W	1b	**Latch field (read or write).** The latch field controls the functionality of the interrupt reporting mechanisms: the INT pin, the flag high field (FH), and flag low field (FL). This bit selects the reporting style between a latched window-style comparison and a transparent hysteresis-style comparison. 0 = The device functions in transparent hysteresis-style comparison operation, where the three interrupt reporting mechanisms directly reflect the comparison of the result register with the high- and low-limit registers with no user-controlled clearing event. See the *Interrupt Operation, INT Pin, and Interrupt Reporting Mechanisms* section for further details. 1 = The device functions in latched window-style comparison operation, latching the interrupt reporting mechanisms until a user-controlled clearing event.
3	POL	R/W	0b	**Polarity field (read or write).** The polarity field controls the polarity or active state of the INT pin. 0 = The INT pin reports active low, pulling the pin low upon an interrupt event. 1 = Operation of the INT pin is inverted, where the INT pin reports active high, becoming high impedance and allowing the INT pin to be pulled high upon an interrupt event.
2	ME	R/W	0b	**Mask exponent field (read or write).** The mask exponent field forces the result register exponent field (register 00h, bits E[3:0]) to 0000b when the full-scale range is manually set, which can simplify the processing of the result register when the full-scale range is manually programmed. This behavior occurs when the mask exponent field is set to 1 and the range number field (RN[3:0]) is set to less than 1100b. Note that the masking is only performed to the result register. When using the interrupt reporting mechanisms, the result comparison with the low-limit and high-limit registers is unaffected by the ME field.
1:0	FC[1:0]	R/W	00b	**Fault count field (read or write).** The fault count field instructs the device as to how many consecutive fault events are required to trigger the interrupt reporting mechanisms: the INT pin, the flag high field (FH), and flag low field (FL). The fault events are described in the latch field (L), flag high field (FH), and flag low field (FL) descriptions. 00 = One fault count (default) 01 = Two fault counts 10 = Four fault counts 11 = Eight fault counts

8.6.1.1.3 Low-Limit Register (offset = 02h) [reset = C0000h]

This register sets the lower comparison limit for the interrupt reporting mechanisms: the INT pin, the flag high field (FH), and flag low field (FL), as described in the *Interrupt Reporting Mechanism Modes* section.

Figure 29. Low-Limit Register

15	14	13	12	11	10	9	8
LE3	LE2	LE1	LE0	TL11	TL10	TL9	TL8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
TL7	TL6	TL5	TL4	TL3	TL2	TL1	TL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 11. Low-Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	LE[3:0]	R/W	0h	**Exponent.** These bits are the exponent bits. Table 12 provides further details.
11:0	TL[11:0]	R/W	000h	**Result.** These bits are the result in straight binary coding (zero to full-scale).

The format of this register is nearly identical to the format of the result register described in the Result Register. The low-limit register exponent (LE[3:0]) is similar to the result register exponent (E[3:0]). The low-limit register result (TL[11:0]) is similar to result register result (R[11:0]).

The equation to translate this register into the lux threshold is given in Equation 4, which is similar to the equation for the result register, Equation 3.

$$lux = 0.01 \times (2^{LE[3:0]}) \times TL[11:0] \quad (4)$$

Table 12 gives the full-scale range and LSB size as it applies to the low-limit register. The detailed discussion and examples given in for the Result Register apply to the low-limit register as well.

Table 12. Full-Scale Range and LSB Size as a Function of Exponent Level

LE3	LE2	LE1	LE0	FULL-SCALE RANGE (lux)	LSB SIZE (lux per LSB)
0	0	0	0	40.95	0.01
0	0	0	1	81.90	0.02
0	0	1	0	163.80	0.04
0	0	1	1	327.60	0.08
0	1	0	0	655.20	0.16
0	1	0	1	1310.40	0.32
0	1	1	0	2620.80	0.64
0	1	1	1	5241.60	1.28
1	0	0	0	10483.20	2.56
1	0	0	1	20966.40	5.12
1	0	1	0	41932.80	10.24
1	0	1	1	83865.60	20.48

NOTE

The result and limit registers are all converted into lux values internally for comparison. These registers can have different exponent fields. However, when using a manually-set full-scale range (configuration register, RN < 0Ch, with mask enable (ME) active), programming the manually-set full-scale range into the LE[3:0] and HE[3:0] fields can simplify the choice of programming the register. This simplification results in the user only having to think about the fractional result and not the exponent part of the result.

8.6.1.1.4 High-Limit Register (offset = 03h) [reset = BFFFh]

The high-limit register sets the upper comparison limit for the interrupt reporting mechanisms: the INT pin, the flag high field (FH), and flag low field (FL), as described in the *Interrupt Operation, INT Pin, and Interrupt Reporting Mechanisms* section. The format of this register is almost identical to the format of the low-limit register (described in the Low-Limit Register) and the result register (described in the Result Register). To explain the similarity in more detail, the high-limit register exponent (HE[3:0]) is similar to the low-limit register exponent (LE[3:0]) and the result register exponent (E[3:0]). The high-limit register result (TH[11:0]) is similar to the low-limit result (TH[11:0]) and the result register result (R[11:0]). Note that the comparison of the high-limit register with the result register is unaffected by the ME bit.

When using a manually-set, full-scale range with the mask enable (ME) active, programming the manually-set, full-scale range into the HE[3:0] bits can simplify the choice of values required to program into this register. The formula to translate this register into lux is similar to Equation 4. The full-scale values are similar to Table 8.

Figure 30. High-Limit Register

15	14	13	12	11	10	9	8
HE3	HE2	HE1	HE0	TH11	TH10	TH9	TH8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
TH7	TH6	TH5	TH4	TH3	TH2	TH1	TH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write

Table 13. High-Limit Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	HE[3:0]	R/W	Bh	**Exponent.** These bits are the exponent bits.
11:0	TH[11:0]	R/W	FFFh	**Result.** These bits are the result in straight binary coding (zero to full-scale).

8.6.1.1.5 Manufacturer ID Register (offset = 7Eh) [reset = 5449h]

This register is intended to help uniquely identify the device.

Figure 31. Manufacturer ID Register

15	14	13	12	11	10	9	8
ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R	R	R	R	R	R	R	R

LEGEND: R = Read only

Table 14. Manufacturer ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	ID[15:0]	R	5449h	**Manufacturer ID.** The manufacturer ID reads 5449h. In ASCII code, this register reads *TI*.

8.6.1.1.6 Device ID Register (offset = 7Fh) [reset = 3001h]

This register is also intended to help uniquely identify the device.

Figure 32. Device ID Register

15	14	13	12	11	10	9	8
DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0
DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
R	R	R	R	R	R	R	R

LEGEND: R = Read only

Table 15. Device ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DID[15:0]	R	3001h	**Device ID.** The device ID reads 3001h.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Ambient light sensors are used in a wide variety of applications that require control as a function of ambient light. Because ambient light sensors nominally match the human eye spectral response, they are superior to photodiodes when the goal is to create an experience for human beings. Very common applications include display optical-intensity control and industrial or home lighting control.

There are two categories of interface to the OPT3001-Q1 device: electrical and optical.

9.1.1 Electrical Interface

The electrical interface is quite simple, as illustrated in Figure 33. Connect the OPT3001-Q1 I^2C SDA and SCL pins to the same pins of an applications processor, microcontroller, or other digital processor. If that digital processor requires an interrupt resulting from an event of interest from the OPT3001-Q1 device, then connect the INT pin to either an interrupt or general-purpose I/O pin of the processor. There are multiple uses for this interrupt, including signaling the system to wake up from low-power mode, processing other tasks while waiting for an ambient light event of interest, or alerting the processor that a sample is ready to be read. Connect pullup resistors between a power supply appropriate for digital communication and the SDA and SCL pins (because they have open-drain output structures). If the INT pin is used, connect a pullup resistor to the INT pin. A typical value for these pullup resistors is 10 kΩ. The resistor choice can be optimized in conjunction to the bus capacitance to balance the system speed, power, noise immunity, and other requirements.

The power supply and grounding considerations are discussed in the *Power Supply Recommendations* section.

Although spike suppression is integrated in the SDA and SCL pin circuits, use proper layout practices to minimize the amount of coupling into the communication lines. One possible introduction of noise occurs from capacitively coupling signal edges between the two communication lines themselves. Another possible noise introduction comes from other switching noise sources present in the system, especially for long communication lines. In noisy environments, shield communication lines to reduce the possibility of unintended noise coupling into the digital I/O lines that could be incorrectly interpreted.

9.1.2 Optical Interface

The optical interface is physically located within the package, facing away from the PCB, as specified by the *Sensor Area* in 図 41.

Physical components, such as a plastic housing and a window that allows light from outside of the design to illuminate the sensor (see Figure 34), can help protect the OPT3001-Q1 device and neighboring circuitry. Sometimes, a dark or opaque window is used to further enhance the visual appeal of the design by hiding the sensor from view. This window material is typically transparent plastic or glass.

Any physical component that affects the light that illuminates the sensing area of a light sensor also affects the performance of that light sensor. Therefore, for optimal performance, make sure to understand and control the effect of these components. Design a window width and height to permit light from a sufficient field of view to illuminate the sensor. For best performance, use a field of view of at least ±35°, or ideally ±45° or more. Understanding and designing the field of view is discussed further in application report SBEA002, *OPT3001: Ambient Light Sensor Application Guide*.

Application Information (continued)

The visible-spectrum transmission for dark windows typically ranges between 5% to 30%, but can be less than 1%. Specify a visible-spectrum transmission as low as, but no more than, necessary to achieve sufficient visual appeal because decreased transmission decreases the available light for the sensor to measure. The windows are made dark by either applying an ink to a transparent window material, or including a dye or other optical substance within the window material itself. This attenuating transmission in the visible spectrum of the window creates a ratio between the light on the outside of the design and the light that is measured by the OPT3001-Q1 device. To accurately measure the light outside of the design, compensate the OPT3001-Q1 measurement for this ratio; an example is given in *Dark Window Selection and Compensation*.

Ambient light sensors are used to help create ideal lighting experiences for humans; therefore, the matching of the sensor spectral response to that of the human eye response is vital. Infrared light is not visible to the human eye, and can interfere with the measurement of visible light when sensors lack infrared rejection. Therefore, the ratio of visible light to interfering infrared light affects the accuracy of any practical system that represents the human eye. The strong rejection of infrared light by the OPT3001-Q1 device allows measurements consistent with human perception under high-infrared lighting conditions, such as from incandescent, halogen, or sunlight sources.

Although the inks and dyes of dark windows serve their primary purpose of being minimally transmissive to visible light, some inks and dyes can also be very transmissive to infrared light. The use of these inks and dyes further decreases the ratio of visible to infrared light, and thus decreases sensor measurement accuracy. However, because of the excellent infrared rejection of the OPT3001-Q1 device, this effect is minimized, and good results are achieved under a dark window with similar spectral responses to those shown in Figure 35.

For best accuracy, avoid grill-like window structures, unless the designer understands the optical effects sufficiently. These grill-like window structures create a nonuniform illumination pattern at the sensor that make light measurement results vary with placement tolerances and angle of incidence of the light. If a grill-like structure is desired, the OPT3001-Q1 device is an excellent sensor choice because it is minimally sensitive to illumination uniformity issues disrupting the measurement process.

Light pipes can appear attractive for aiding in the optomechanical design that brings light to the sensor; however, do not use light pipes with any ambient light sensor unless the system designer fully understands the ramifications of the optical physics of light pipes within the full context of his design and objectives.

9.2 Typical Application

Measuring the ambient light with the OPT3001-Q1 device in a product case and under a dark window is described in this section. The schematic for this design is shown in Figure 33.

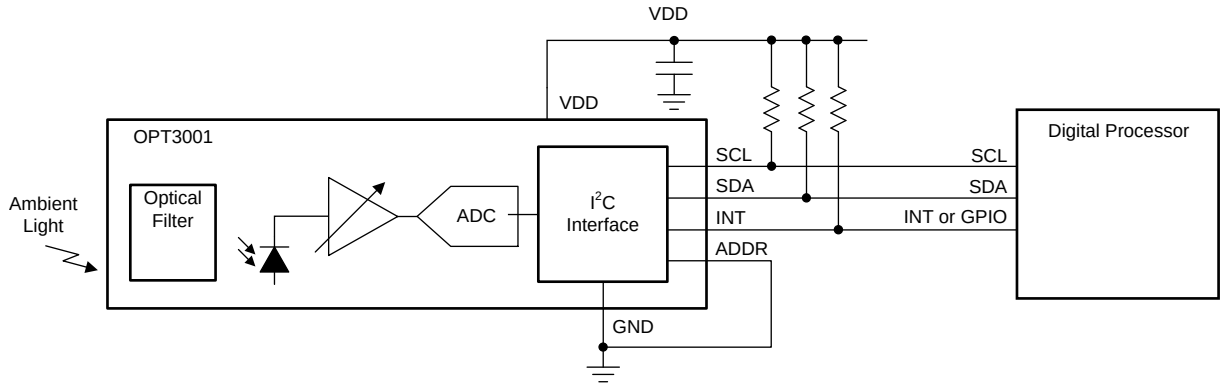


Figure 33. Measuring Ambient Light in a Product Case Behind a Dark Window

Typical Application (continued)

9.2.1 Design Requirements

The basic requirements of this design are:

- Sensor is hidden under dark glass so that sensor is not obviously visible. Note that this requirement is subjective to designer preference.
- Accuracy of measurement of fluorescent light is 15%
- Variation in measurement between fluorescent, halogen, and incandescent bulbs (also known as light source variation) is as small as possible.

9.2.2 Detailed Design Procedure

9.2.2.1 Optomechanical Design

After completing the electrical design, the next task is the optomechancial design. Design a product case that includes a window to transmit the light from outside the product to the sensor, as shown in Figure 34. Design the window width and window height to give a ±45° field of view. A rigorous design of the field of view takes into account the location of the sensor area, as shown in 図 41. The OPT3001-Q1 active sensor area is centered along one axis of the package top view, but has a minor offset on the other axis of the top view. Window sizing and placement is discussed in more rigorous detail in application report SBEA002, *OPT3001: Ambient Light Sensor Application Guide*.

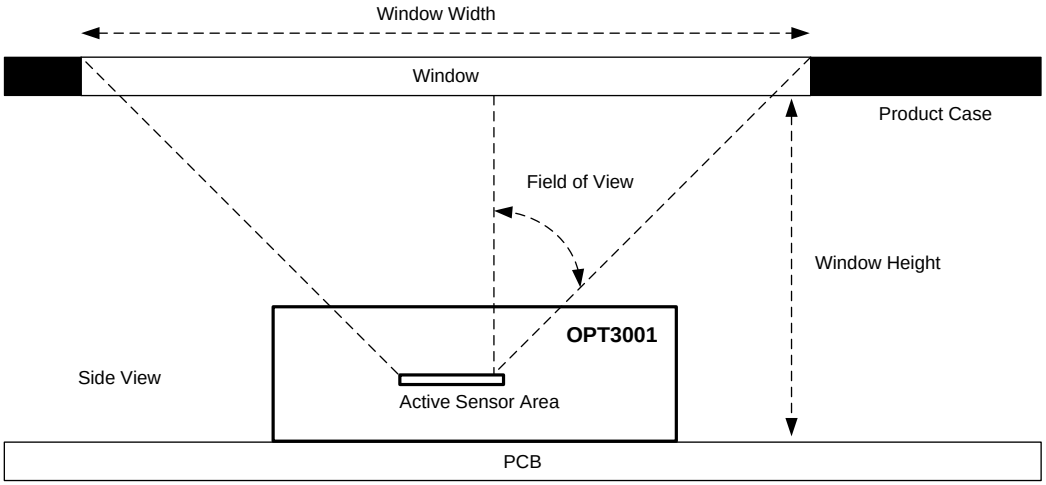


Figure 34. Product Case and Window Over the OPT3001-Q1 Device

9.2.2.2 Dark Window Selection and Compensation

There are several approaches to selecting and compensating for a dark window. One of many approaches is the method described here.

Sample several different windows with various levels of darkness. Choose a window that is dark enough to optimize the balance between the aesthetics of the device and sensor performance. Note that the aesthetic evaluation is the subjective opinion of the designer; therefore, it is more important to see the window on the physical design rather than refer to window transmission specifications on paper. Make sure that the chosen window is not darker than absolutely necessary because a darker window allows less light to illuminate the sensor and therefore impedes sensor accuracy.

The window chosen for this application example is dark and has less than 7% transmission at 550 nm. Figure 35 shows the normalized response of the spectrum. Note that the equipment used to measure the transmission spectrum is not capable of measuring the absolute accuracy (non-normalized) of the dark window sample, but only the relative normalized spectrum. Also note that the window is much more transmissive to infrared wavelengths longer than 700 nm than to visible wavelengths between 400 nm and 650 nm. This imbalance between infrared and visible light decreases the ratio of visible light to infrared light at the sensor. Although it is preferable to have the window decrease this ratio as little as possible (by having a window with a close ratio of visible transmission to infrared transmission), the OPT3001-Q1 device still performs well as shown in Figure 38.

Typical Application (continued)

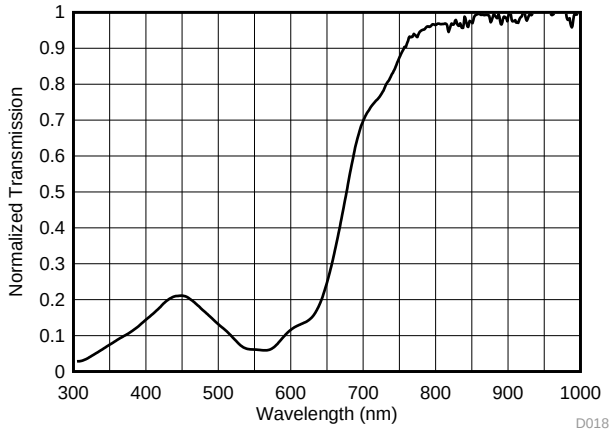


Figure 35. Normalized Transmission Spectral Response of the Chosen Dark Window

After choosing the dark window, measure the attenuating effect of the dark window for later compensation. In order to measure this attenuation, measure a fluorescent light source with a lux meter, then measure that same light with the OPT3001-Q1 device under the dark window. To measure accurately, it is important to use a fixture that can accommodate either the lux meter or the design containing the OPT3001-Q1 device and dark window, with the center of each of the sensing areas being in exactly the same *X, Y, Z* location, as shown in Figure 36. The *Z* placement of the design (distance from the light source) is the top of the window, and not the OPT3001-Q1 device itself.

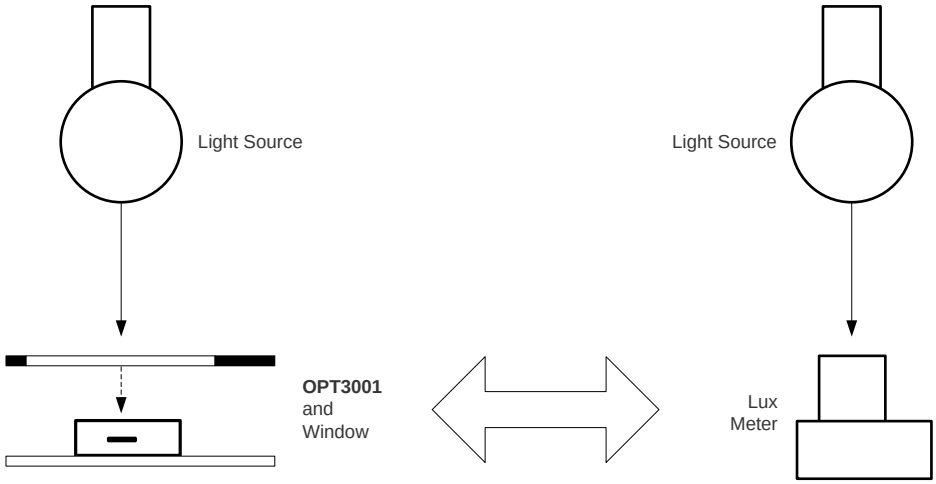


Figure 36. Fixture With One Light Source Accommodating Either a Lux Meter or the Design (Window and OPT3001-Q1 Device) in the Exact Same X,Y,Z Position

The fluorescent light in this location measures 1000 lux with the lux meter, and 73 lux with the OPT3001-Q1 device under the dark window within the application. Therefore, the window has an effective transmission of 7.3% for the fluorescent light. This 7.3% is the weighted average attenuation across the entire spectrum, weighted by the spectral response of the lux meter (or photopic response).

For all subsequent OPT3001-Q1 measurements under this dark window, the following formula is applied.

Compensated Measurement = Uncompensated Measurement / (7.3%) (5)

Typical Application (continued)

9.2.3 Application Curves

To validate that the design example now measures correctly, create a sequential number of different light intensities with the fluorescent light by using neutral density filters to attenuate the light. Different light intensities can also be created by changing the distance between the light source, and the measurement devices. However, these two methods for changing the light level have minor accuracy tradeoffs that are beyond the scope of this discussion. Measure each intensity with both the lux meter and the OPT3001-Q1 device under the window, and compensate using Equation 5. The results are displayed in Figure 37, and show that the application accurately reports results very similar to the lux meter.

To validate that the design measures a variety of light sources correctly, despite the large ratio of infrared transmission to visible light transmission of the window, measure the application with a halogen bulb and an incandescent bulb. Use the physical location and light attenuation procedures that were used for the fluorescent light. The results are shown in Figure 38.

The addition of the dark window changes the results as seen by comparing the results of the same measurement with a window (Figure 38) and without a window (Figure 3). Even after the expected change, the performance is still good. All data are both within 15% of the correct answer, and within 15% of the other bulb measurements.

Results can vary at different angles of light because the OPT3001-Q1 device does not match the lux meter at all angles of light.

If the measurement variation between the light sources is not acceptable, choose a different window that has a closer ratio of visible light transmission to infrared light transmission.

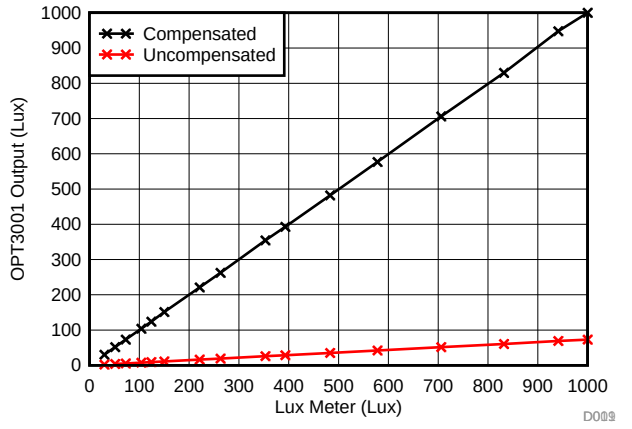


Figure 37. Uncompensated and Compensated Output of the OPT3001-Q1 Grade 3 Device Under a Dark Window Illuminated by Fluorescent Light Source

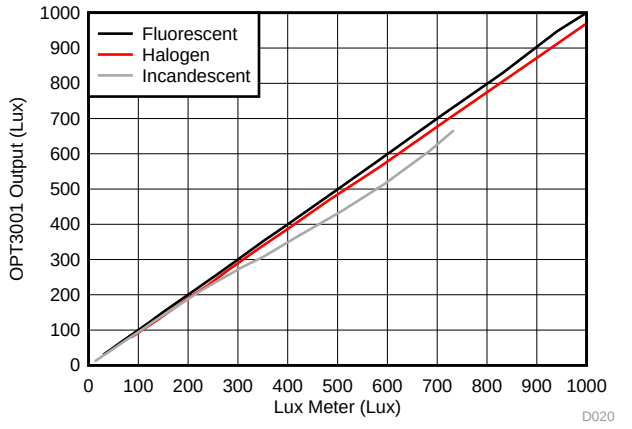


Figure 38. Compensated Output of the OPT3001-Q1 Grade 3 Device Under a Dark Window Illuminated by Fluorescent, Halogen, and Incandescent Light Sources

9.3 Do's and Don'ts

As with any optical product, special care must be taken into consideration when handling the OPT3001-Q1 device. Although the OPT3001-Q1 device has low sensitivity to dust and scratches, proper optical device handling procedures are still recommended.

The optical surface of the device must be kept clean for optimal performance in both prototyping with the device and mass production manufacturing procedures. Tweezers with plastic or rubber contact surfaces are recommended to avoid scratches on the optical surface. Avoid manipulation with metal tools when possible. The optical surface must be kept clean of fingerprints, dust, and other optical-inhibiting contaminants.

If the device optical surface requires cleaning, the use of de-ionized water or isopropyl alcohol is recommended. A few gentile brushes with a soft swab are appropriate. Avoid potentially abrasive cleaning and manipulating tools and excessive force that can scratch the optical surface.

If the OPT3001-Q1 device performs less than optimally, inspect the optical surface for dirt, scratches, or other optical artifacts.

10 Power Supply Recommendations

Although the OPT3001-Q1 device has low sensitivity to power-supply issues, good practices are always recommended. For best performance, the OPT3001-Q1 V_{DD} pin must have a stable, low-noise power supply with a 100-nF bypass capacitor close to the device and solid grounding. There are many options for powering the OPT3001-Q1 device, because the device current consumption levels are very low.

11 Layout

11.1 Layout Guidelines

The PCB layout design for the OPT3001-Q1 device requires a couple of considerations. Bypass the power supply with a capacitor placed close to the OPT3001-Q1 device. Note that optically reflective surfaces of components also affect the performance of the design. The three-dimensional geometry of all components and structures around the sensor must be taken into consideration to prevent unexpected results from secondary optical reflections. Placing capacitors and components at a distance of at least twice the height of the component is usually sufficient. The most optimal optical layout is to place all close components on the opposite side of the PCB from the OPT3001-Q1 device. However, this approach may not be practical for the constraints of every design.

Electrically connecting the thermal pad to ground is recommended. This connection can be created either with a PCB trace or with vias to ground directly on the thermal pad itself. If the thermal pad contains vias, they are recommended to be of a small diameter (< 0.2 mm) to prevent them from wicking the solder away from the appropriate surfaces.

An example PCB layout with the OPT3001-Q1 device is shown in Figure 39.

11.2 Layout Example

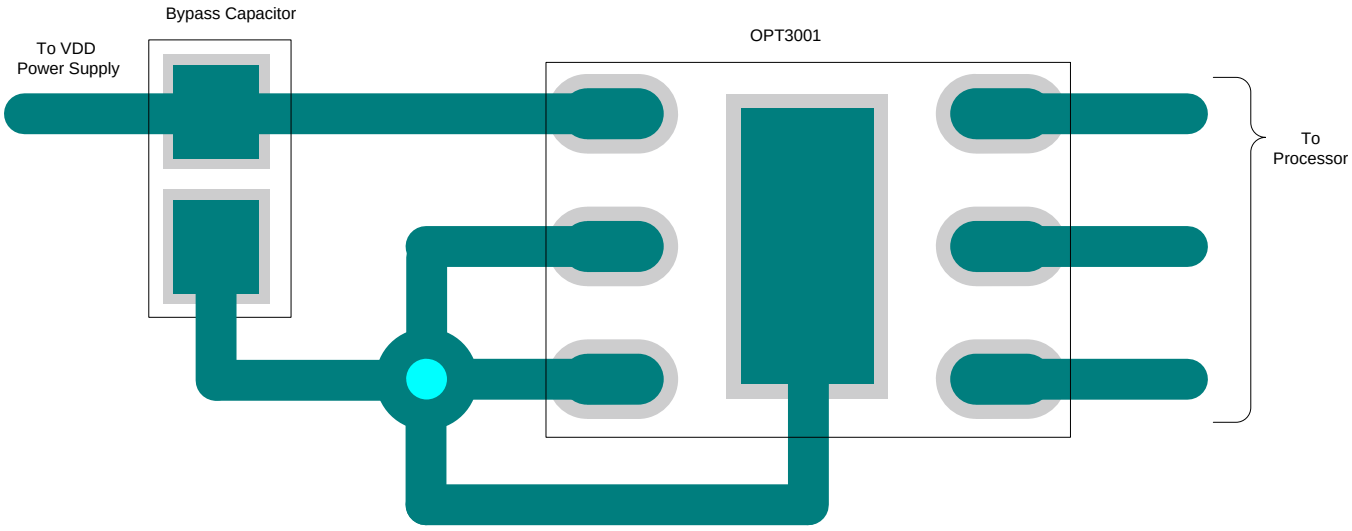


Figure 39. Example PCB Layout With the OPT3001-Q1 Device

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- *『OPT3001: 環境光センサ・アプリケーション・ガイド』*(SBEA002)
- *『OPT3001EVMユーザー・ガイド』*(SBOU134)
- *『QFN/SONのPCB実装』アプリケーション・レポート*(SLUA271)

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

12.4 商標

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12.5 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

13.1 ハンダ付けと取り扱いについての推奨事項

OPT3001-Q1デバイスは、JEDEC JSTD-020に従い、3つのハンダ付けリフロー操作について認定済みです。

過剰な熱を加えるとデバイスが変色し、光学性能に影響するおそれがあることに注意してください。

ハンダ付けの熱プロファイルや、その他の情報については、アプリケーション・レポート*『QFN/SONのPCB実装』*(SLUA271)を参照してください。OPT3001-Q1をPCBから取り外す必要がある場合、デバイスは再取り付けせず破棄してください。

ハンダ付けと取り扱いについての推奨事項 (continued)

一般的な光デバイスと同様に、OPT3001-Q1デバイスは特別な注意を払って取り扱い、受光面に汚れや傷が付かないようにしてください。詳細な推奨事項については、*Do's and Don'ts* セクションを参照してください。最高の光学性能を実現するため、ハンダ付け作業の後で、フラックスや他の破片を取り除いてください。

13.2 DNP (S-PDSO-N6)メカニカル図面

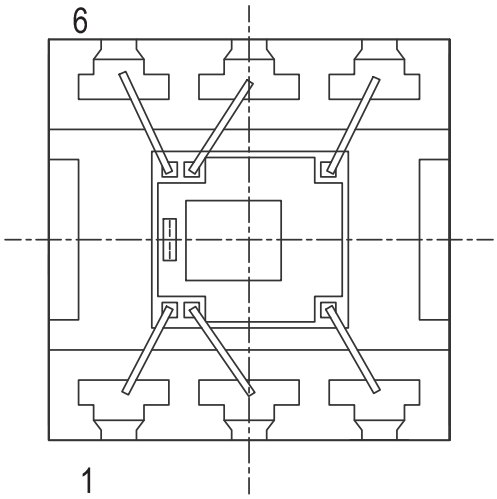


図 40. パッケージ方向: ピン1の視覚的参照図 (上面図)

DNP (S-PDSO-N6)メカニカル図面 (continued)

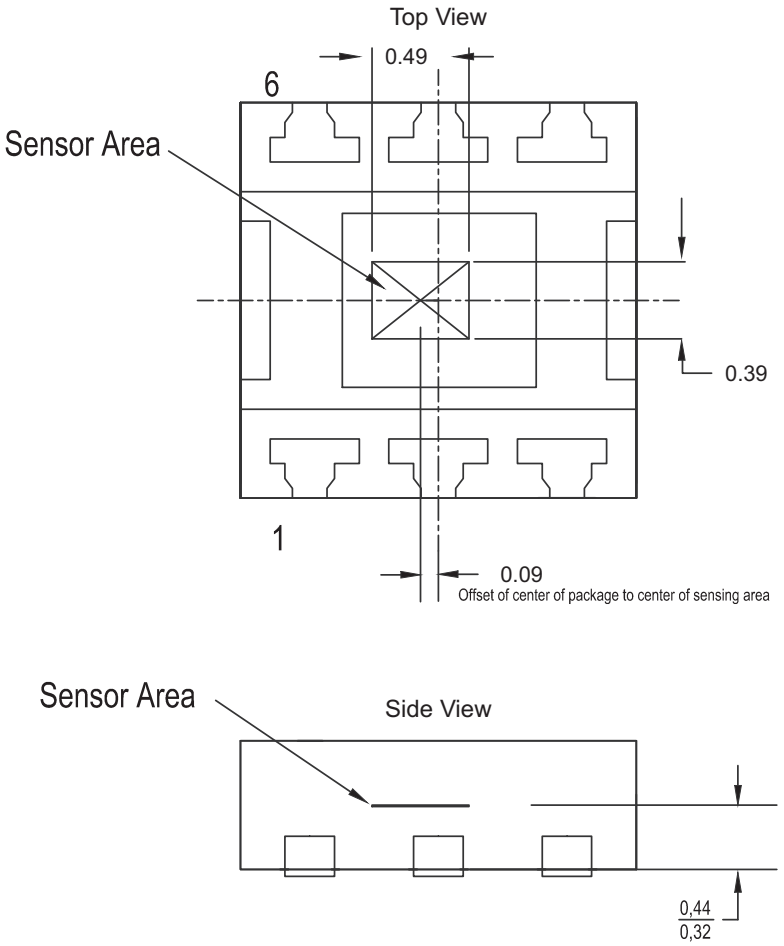


図 41. センシング部分の場所を示す機械的概略図 (上面および側面図)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPT3001DNPRQ1	ACTIVE	USON	DNP	6	3000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 105	ED	Samples
OPT3001IDNPRQ1	ACTIVE	USON	DNP	6	3000	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 85	ED	Samples
OPT3001IDNPTQ1	OBSOLETE	USON	DNP	6		TBD	Call TI	Call TI	-40 to 85	ED	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF OPT3001-Q1 :

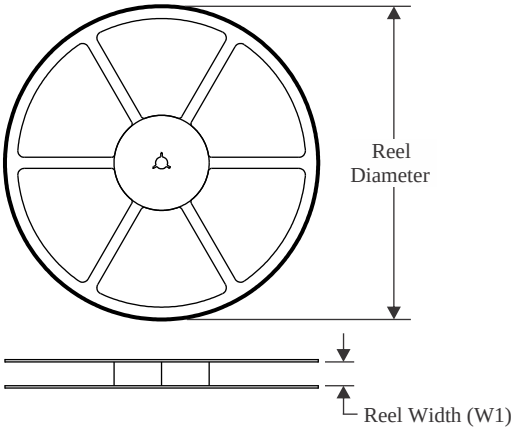
- Catalog : OPT3001

NOTE: Qualified Version Definitions:

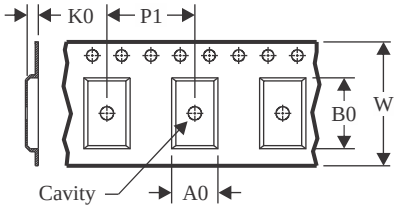
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

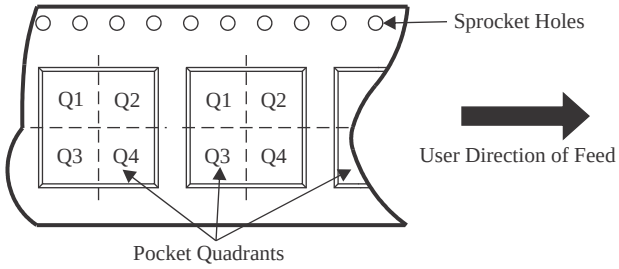


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

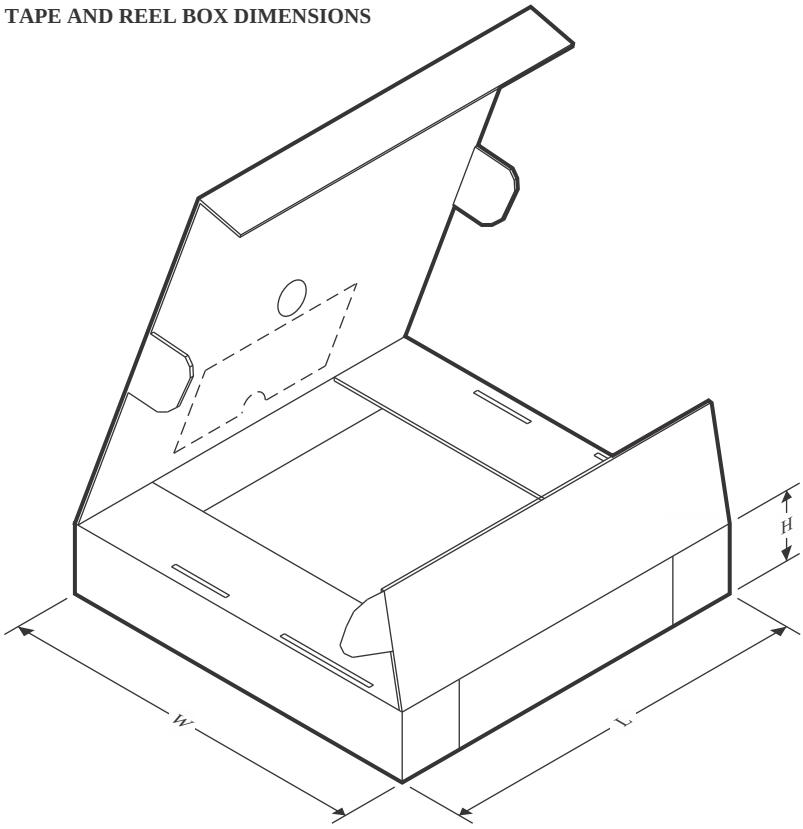
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPT3001DNPRQ1	USON	DNP	6	3000	330.0	12.4	2.3	2.3	0.9	8.0	12.0	Q1
OPT3001IDNPRQ1	USON	DNP	6	3000	330.0	12.4	2.3	2.3	0.9	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

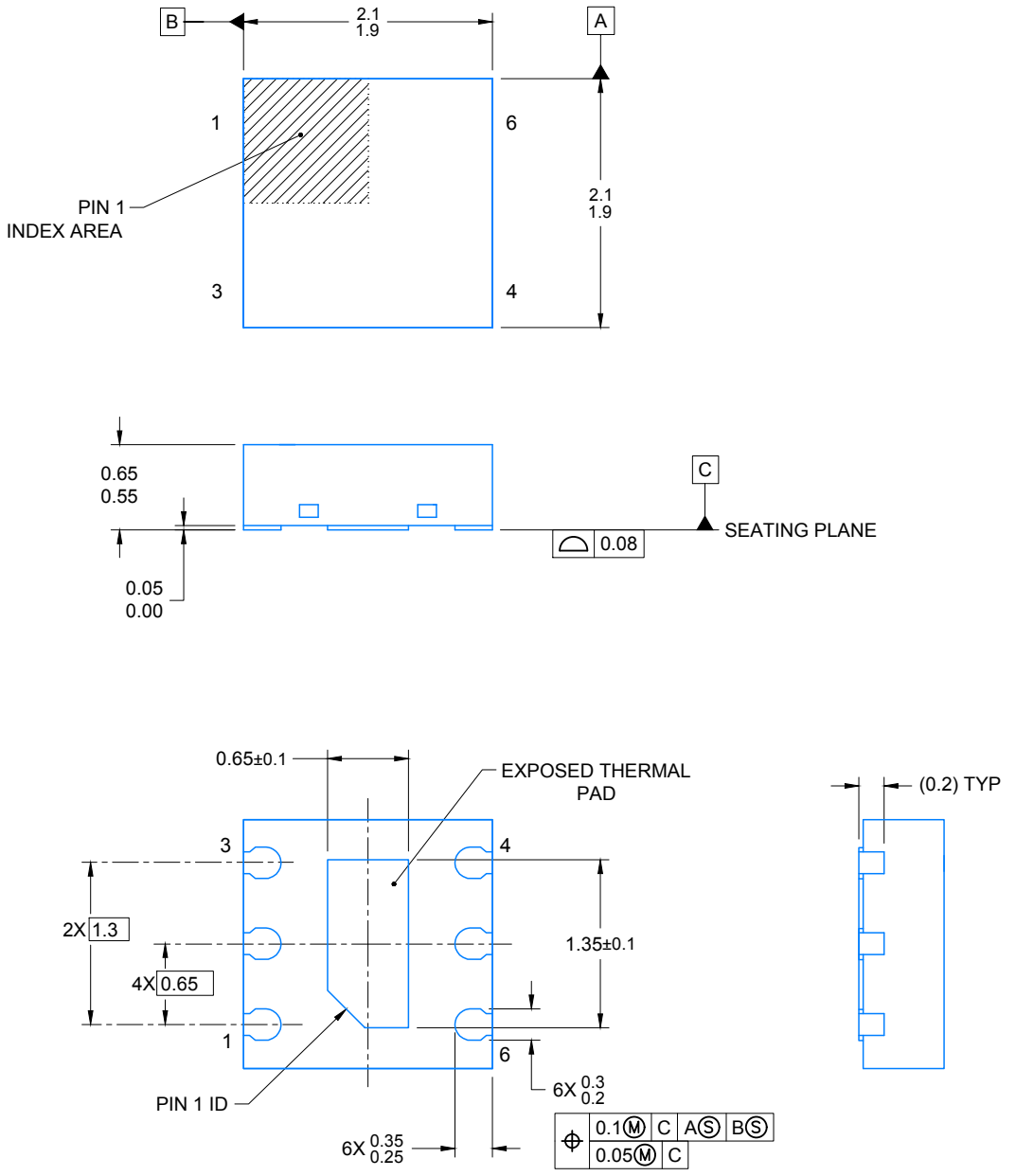
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPT3001DNPRQ1	USON	DNP	6	3000	356.0	338.0	48.0
OPT3001IDNPRQ1	USON	DNP	6	3000	356.0	338.0	48.0

PACKAGE OUTLINE

DNP0006A

USON - 0.65 mm mm max height

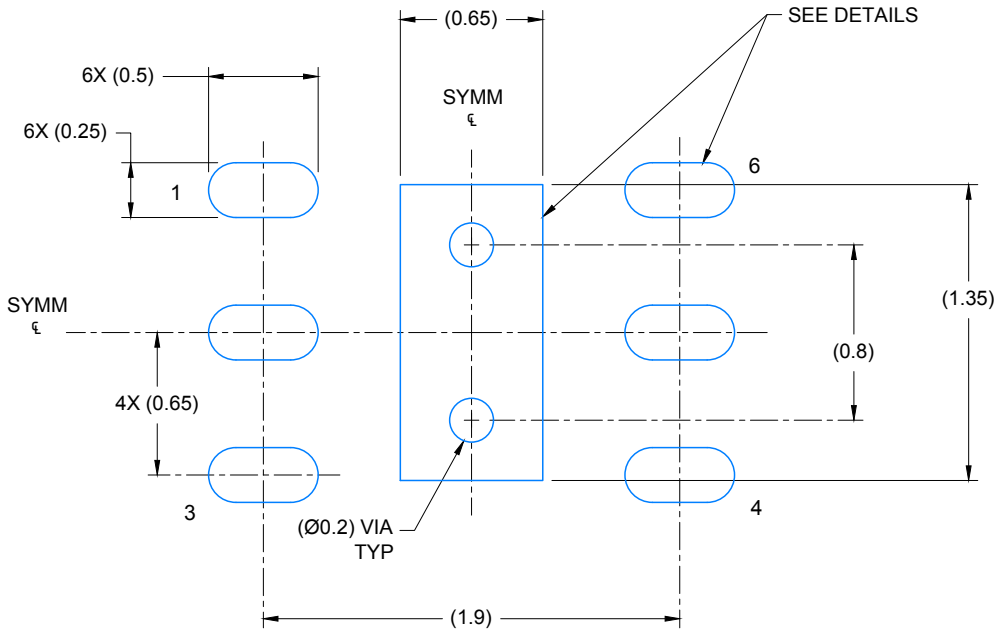
PLASTIC SMALL OUTLINE NO-LEAD



4221434/C 01/2018

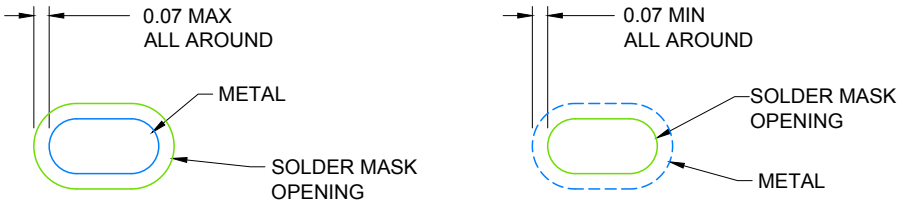
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Optical package with clear mold compound.



LAND PATTERN EXAMPLE

SCALE: 30X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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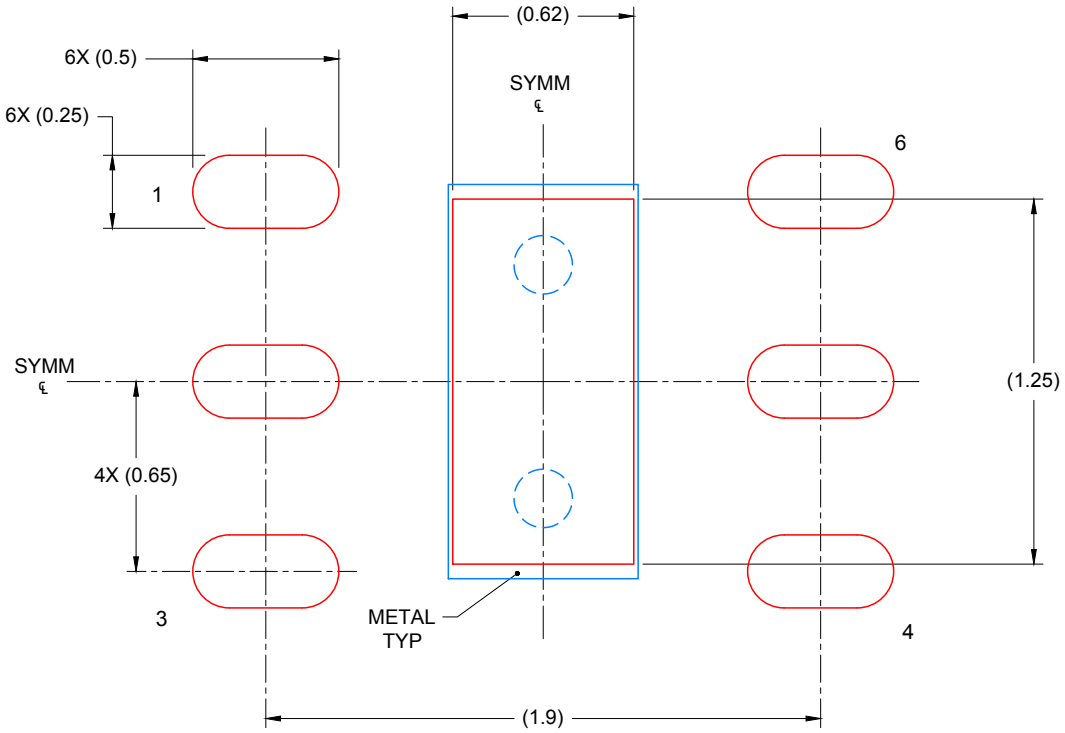
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .



SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 40X

4221434/C 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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