

## LMK60XX 高性能、低ジッタ発振器

### 1 特長

- 低ノイズ、高性能
  - ジッタ: 150fs RMS (標準値)、 $F_{out} > 100\text{MHz}$
  - PSRR:  $-60\text{dBc}$ 、堅牢な電源ノイズ耐性
- 対応出力フォーマット
  - LVPECL、LVDS、HCSL (最大400MHz)
- 合計周波数公差:  $\pm 50\text{ppm}$  (LMK60X2)、 $\pm 25\text{ppm}$  (LMK60X0)
- 動作電圧: 3.3V
- 工業用温度範囲:  $(-40^{\circ}\text{C} \sim +85^{\circ}\text{C})$
- 7mmx 5mmの6ピン・パッケージ、業界標準の7050 XOパッケージとピン互換

### 2 アプリケーション

- 水晶振動子、SAW、またはシリコン・ベースの発振器に代わる高性能の代替品
- スイッチ、ルータ、ネットワーク・ライン・カード、ベースバンド・ユニット(BBU)、サーバ、ストレージ/SAN
- 試験/測定機器
- 医療用画像処理
- FPGA、プロセッサ接続

### 3 概要

LMK60EXは低ジッタの発振器ファミリで、一般的に使用されるリファレンス・クロックを生成します。このデバイスは、任意のリファレンス・クロック周波数をサポートするよう工場であらかじめプログラムされ、出力フォーマットとしてLVPECL、LVDS、HCSLで最大400MHzをサポートします。内部的な電力コンディショニングにより、電源リップル除去(PSRR)が非常に優れているため、電力供給ネットワークのコストと複雑性を減らすことができます。単一の3.3V $\pm 5\%$ 電源で動作します。

#### 製品情報(1)

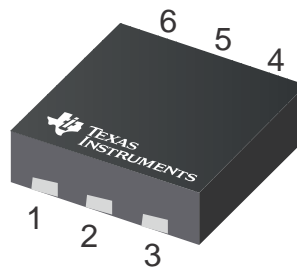
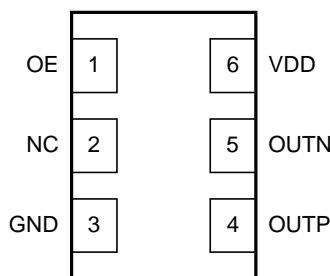
型番	パッケージ	サイズ
LMK60E2-100M	QFM (6)	7.00mmx5.00mm
LMK60E2-125M	QFM (6)	7.00mmx5.00mm
LMK60E2-156M	QFM (6)	7.00mmx5.00mm
LMK60E0-156M	QFM (6)	7.00mmx5.00mm
LMK60E0-212M	QFM (6)	7.00mmx5.00mm
LMK60I2-100M	QFM (6)	7.00mmx5.00mm
LMK60I2-322M	QFM (6)	7.00mmx5.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

#### 出力周波数オプション

型番	出力周波数(MHz)とフォーマット	総合周波数安定性(ppm)
LMK60E2-100M	100 LVPECL	$\pm 50$
LMK60E2-125M	125 LVPECL	$\pm 50$
LMK60E2-156M	156.25 LVPECL	$\pm 50$
LMK60E0-156M	156.25 LVPECL	$\pm 25$
LMK60E0-212M	212.5 LVPECL	$\pm 25$
LMK60I2-100M	100 HCSL	$\pm 50$
LMK60I2-322M	322.265625 HCSL	$\pm 50$

#### ピン配置



## 目次

1	特長	1	6.11	Power-On/Reset Characteristics (VDD)	6
2	アプリケーション	1	6.12	PSRR Characteristics	6
3	概要	1	6.13	PLL Clock Output Jitter Characteristics	6
4	改訂履歴	2	6.14	Additional Reliability and Qualification	6
5	Pin Configuration and Functions	3	7	Parameter Measurement Information	7
6	Specifications	3	7.1	Device Output Configurations	7
6.1	Absolute Maximum Ratings	3	8	Power Supply Recommendations	9
6.2	ESD Ratings	3	9	Layout	9
6.3	Recommended Operating Conditions	4	9.1	Layout Guidelines	9
6.4	Thermal Information	4	10	デバイスおよびドキュメントのサポート	11
6.5	Electrical Characteristics - Power Supply	4	10.1	ドキュメントの更新通知を受け取る方法	11
6.6	LVPECL Output Characteristics	4	10.2	コミュニティ・リソース	11
6.7	LVDS Output Characteristics	5	10.3	商標	11
6.8	HCSL Output Characteristics	5	10.4	静電気放電に関する注意事項	11
6.9	OE Input Characteristics	5	10.5	Glossary	11
6.10	Frequency Tolerance Characteristics	5	11	メカニカル、パッケージ、および注文情報	11

## 4 改訂履歴

Revision B (November 2017) から Revision C に変更	Page
• LMK60E2-100Mの新しいリリース	1

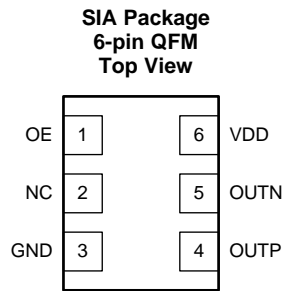
  

Revision A (June 2017) から Revision B に変更	Page
• LMK60E2-125Mの新しいリリース	1
• LMK60I2-100Mの新しいリリース	1
• LMK60I2-322Mの新しいリリース	1

2016年12月発行のものから更新	Page
• LMK60E0-156MおよびLMK60E0-212Mを追加	1

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
<b>POWER</b>			
GND	3	Ground	Device ground
VDD	6	Analog	3.3-V power supply
<b>OUTPUT BLOCK</b>			
OUTP, OUTN	4, 5	Universal	Differential output pair (LVPECL, LVDS or HCSSL).
<b>DIGITAL CONTROL / INTERFACES</b>			
NC	2	N/A	No connect
OE	1	LVC MOS	Output enable (internal pullup). When set to low, output pair is disabled and set at high impedance.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
VDD	Device supply voltage	-0.3	3.6	V
V <sub>IN</sub>	Output voltage for logic inputs	-0.3	VDD + 0.3	V
V <sub>OUT</sub>	Output voltage for clock outputs	-0.3	VDD + 0.3	V
T <sub>J</sub>	Junction temperature		150	°C
T <sub>STG</sub>	Storage temperature	-40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Device supply voltage	3.135	3.3	3.465	V
T <sub>A</sub>	Ambient temperature	-40	25	85	°C
T <sub>J</sub>	Junction temperature			105	°C
t <sub>RAMP</sub>	VDD power-up ramp time	0.1		100	ms

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		LMK60EX <sup>(2) (3) (4)</sup>		UNIT
		SIA (QFM)		
		6 PINS		
		Airflow (LFM) 0		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	74.8		°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	46.7		°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	49.0		°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	14.8		°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	48.7		°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a		°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) The package thermal resistance is calculated on a 4 layer JEDEC board.
- (3) Connected to GND with 2 thermal vias (0.3-mm diameter).
- (4) ψ<sub>JB</sub> (junction to board) is used when the main heat flow is from the junction to the GND pad. Please refer to Thermal Considerations section for more information on ensuring good system reliability and quality.

### 6.5 Electrical Characteristics - Power Supply<sup>(1)</sup>

VDD = 3.3 V ± 5%, T<sub>A</sub> = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
IDD	Device current consumption	LVPECL <sup>(2)</sup>		95	110	mA
		LVDS		85	100	
		HCSL <sup>(3)</sup>		90	105	
IDD-PD	Device current consumption when output is disabled	OE = GND		70	mA	

- (1) Refer to [Parameter Measurement Information](#) for relevant test conditions.
- (2) On-chip power dissipation should exclude 40 mW, dissipated in the 150 Ω termination resistors, from total power dissipation.
- (3) Excludes load current.

### 6.6 LVPECL Output Characteristics<sup>(1)</sup>

VDD = 3.3 V ± 5%, T<sub>A</sub> = -40°C to 85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>OUT</sub>	Output frequency <sup>(2)</sup>			400	MHz
V <sub>OD</sub>	Output voltage swing (V <sub>OH</sub> – V <sub>OL</sub> ) <sup>(2)</sup>	700	950	1200	mV
V <sub>OUT, DIFF, PP</sub>	Differential output peak-to-peak swing	2 ×  V <sub>OD</sub>			V
V <sub>OS</sub>	Output common-mode voltage	VDD – 1.45			V
t <sub>R</sub> / t <sub>F</sub>	Output rise/fall time (20% to 80%) <sup>(3)</sup>		260	350	ps
ODC	Output duty cycle <sup>(3)</sup>	45%		55%	

- (1) Refer to [Parameter Measurement Information](#) for relevant test conditions.
- (2) An output frequency over f<sub>OUT</sub> max spec is possible, but output swing may be less than V<sub>OD</sub> min spec.
- (3) Ensured by characterization.

## 6.7 LVDS Output Characteristics<sup>(1)</sup>

VDD = 3.3 V ± 5%, T<sub>A</sub> = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>OUT</sub>	Output frequency <sup>(1)</sup>				400	MHz
V <sub>OD</sub>	Output voltage swing (V <sub>OH</sub> – V <sub>OL</sub> ) <sup>(1)</sup>		300	390	480	mV
V <sub>OUT, DIFF, PP</sub>	Differential output peak-to-peak swing		2 x  V <sub>OD</sub>			V
V <sub>OS</sub>	Output common-mode voltage		1.2			V
t <sub>R</sub> / t <sub>F</sub>	Output rise/fall time (20% to 80%) <sup>(2)</sup>		260		350	ps
ODC	Output duty cycle <sup>(2)</sup>		45%		55%	
R <sub>OUT</sub>	Differential output impedance		107			Ω

(1) An output frequency over f<sub>OUT</sub> max spec is possible, but output swing may be less than V<sub>OD</sub> min spec.

(2) Ensured by characterization.

## 6.8 HCSL Output Characteristics<sup>(1)</sup>

VDD = 3.3 V ± 5%, T<sub>A</sub> = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>OUT</sub>	Output frequency				400	MHz
V <sub>OH</sub>	Output high voltage		660		900	mV
V <sub>OL</sub>	Output low voltage		-100		100	mV
V <sub>CROSS</sub>	Absolute crossing voltage <sup>(2)(3)</sup>		250		475	mV
V <sub>CROSS-DELTA</sub>	Variation of V <sub>CROSS</sub> <sup>(2)(3)</sup>		0		140	mV
dV/dt	Slew rate <sup>(4)</sup>		1		3	V/ns
ODC	Output duty cycle <sup>(4)</sup>		45%		55%	

(1) Refer to [Parameter Measurement Information](#) for relevant test conditions.

(2) Measured from -150 mV to +150 mV on the differential waveform with the 300 mVpp measurement window centered on the differential zero crossing.

(3) Ensured by design.

(4) Ensured by characterization.

## 6.9 OE Input Characteristics

VDD = 3.3 V ± 5%, T<sub>A</sub> = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IH</sub>	Input high voltage		1.4			V
V <sub>IL</sub>	Input low voltage				0.6	V
I <sub>IH</sub>	Input high current	V <sub>IH</sub> = VDD	-40		40	μA
I <sub>IL</sub>	Input low current	V <sub>IL</sub> = GND	-40		40	μA
C <sub>IN</sub>	Input capacitance			2		pF

## 6.10 Frequency Tolerance Characteristics<sup>(1)</sup>

VDD = 3.3 V ± 5%, T<sub>A</sub> = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f <sub>T</sub>	Total frequency tolerance	LMK60X2: All output formats, frequency bands and device junction temperature up to 105°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and 5-year aging at 40°C	-50		50	ppm
		LMK60X0: All output formats, frequency bands and device junction temperature up to 105°C; includes initial freq tolerance, temperature & supply voltage variation, solder reflow and 5-year aging at 40°C	-25		25	ppm

(1) Ensured by characterization.

## 6.11 Power-On/Reset Characteristics (VDD)

VDD = 3.3 V ± 5%, T<sub>A</sub> = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>THRESH</sub>	Threshold voltage <sup>(1)</sup>		2.85		3	V
V <sub>DROOP</sub>	Allowable voltage droop <sup>(2)</sup>				0.1	V
t <sub>STARTUP</sub>	Start-up time <sup>(1)</sup>	Time elapsed from VDD at 3.135 V to output enabled			10	ms
t <sub>OE-EN</sub>	Output enable time <sup>(2)</sup>	Time elapsed from OE at V <sub>IH</sub> to output enabled			50	µs
t <sub>OE-DIS</sub>	Output disable time <sup>(2)</sup>	Time elapsed from OE at V <sub>IL</sub> to output disabled			50	µs

(1) Ensured by characterization.

(2) Ensured by design.

## 6.12 PSRR Characteristics<sup>(1)</sup>

VDD = 3.3 V, T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Spurs induced by 50-mV power supply ripple <sup>(2)(3)</sup> at 156.25-MHz output, all output types	Sine wave at 50 kHz		-60		dBc
		Sine wave at 100 kHz		-60		
		Sine wave at 500 kHz		-60		
		Sine wave at 1 MHz		-60		

(1) Refer to [Parameter Measurement Information](#) for relevant test conditions.

(2) Measured max spur level with 50 mVpp sinusoidal signal between 50 kHz and 1 MHz applied on VDD pin

(3)  $DJ_{SPUR} (ps, pk-pk) = [2 \cdot 10 \cdot (SPUR/20) / (\pi \cdot f_{OUT})] \cdot 1e6$ , where PSRR or SPUR in dBc and f<sub>OUT</sub> in MHz.

## 6.13 PLL Clock Output Jitter Characteristics<sup>(1)(2)</sup>

VDD = 3.3 V ± 5%, T<sub>A</sub> = -40°C to 85°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RJ	RMS phase jitter <sup>(3)</sup> (12 kHz – 20 MHz)	f <sub>OUT</sub> ≥ 100 MHz, all output types		150	250	fs RMS

(1) Refer to [Parameter Measurement Information](#) for relevant test conditions.

(2) Phase jitter measured with Agilent E5052 signal source analyzer using a differential-to-single ended converter (balun or buffer).

(3) Ensured by characterization.

## 6.14 Additional Reliability and Qualification

PARAMETER	CONDITION / TEST METHOD
Mechanical Shock	MIL-STD-202, Method 213
Mechanical Vibration	MIL-STD-202, Method 204
Moisture Sensitivity Level	J-STD-020, MSL3

## 7 Parameter Measurement Information

### 7.1 Device Output Configurations

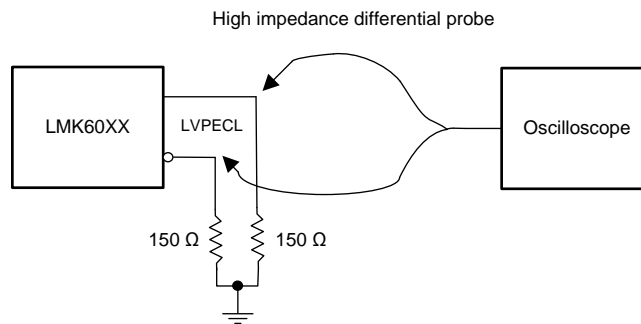


Figure 1. LVPECL Output DC Configuration During Device Test

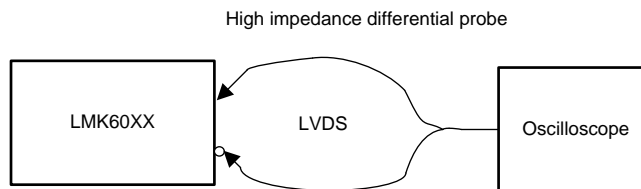


Figure 2. LVDS Output DC Configuration During Device Test

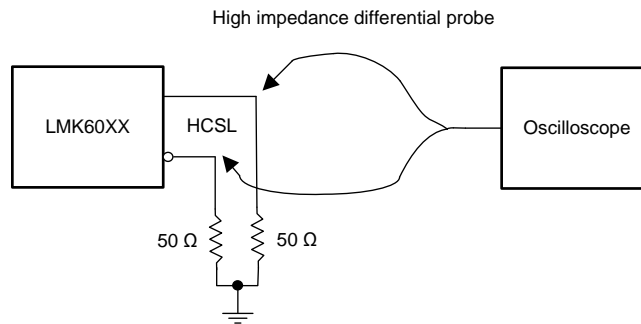


Figure 3. HCSL Output DC Configuration During Device Test <sup>(1)</sup>

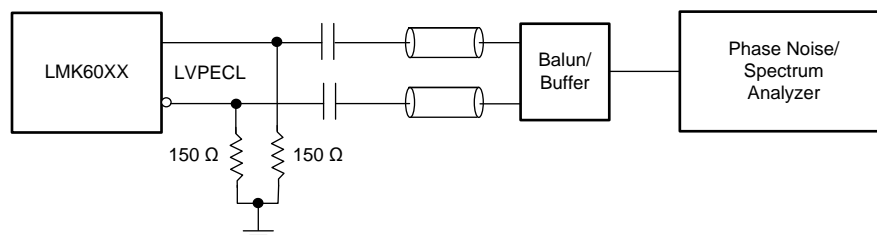
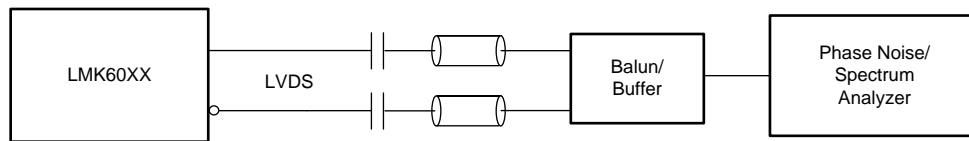


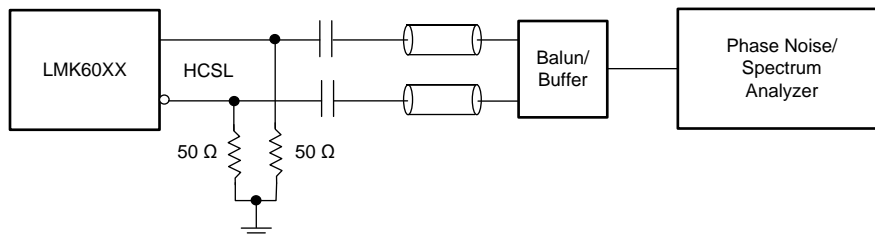
Figure 4. LVPECL Output AC Configuration During Device Test

(1) Also compatible with 85 Ω termination

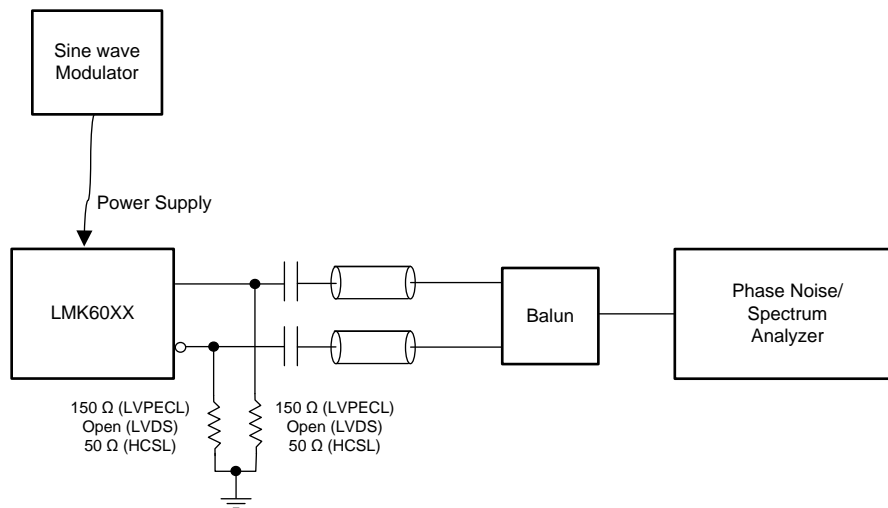
**Device Output Configurations (continued)**



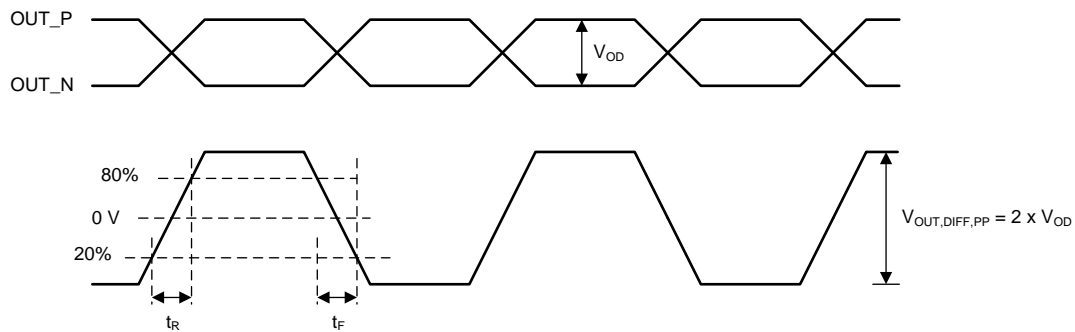
**Figure 5. LVDS Output AC Configuration During Device Test**



**Figure 6. HCSL Output AC Configuration During Device Test**



**Figure 7. PSRR Test Setup**



**Figure 8. Differential Output Voltage and Rise/Fall Time**



## 8 Power Supply Recommendations

For best electrical performance of LMK60EX, TI recommends using a combination of 10  $\mu\text{F}$ , 1  $\mu\text{F}$ , and 0.1  $\mu\text{F}$  on its power-supply bypass network. TI also recommends using component side mounting of the power-supply bypass capacitors and it is best to use 0201 or 0402 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane. [Figure 9](#) shows the layout recommendation for power supply decoupling of LMK60EX.

## 9 Layout

### 9.1 Layout Guidelines

The following sections provides recommendations for board layout, solder reflow profile, and power supply bypassing when using LMK60EX to ensure good thermal and electrical performance, along with overall signal integrity of entire system.

#### 9.1.1 Ensuring Thermal Reliability

The LMK60EX is a high-performance device. Therefore, pay careful attention to device configuration and the printed-circuit board (PCB) layout with respect to power consumption. The ground pin must be connected to the ground plane of the PCB through three vias or more, as shown in [Figure 9](#), to maximize thermal dissipation out of the package.

[Equation 1](#) describes the relationship between the PCB temperature around the LMK60EX and its junction temperature.

$$T_B = T_J - \Psi_{JB} * P$$

where

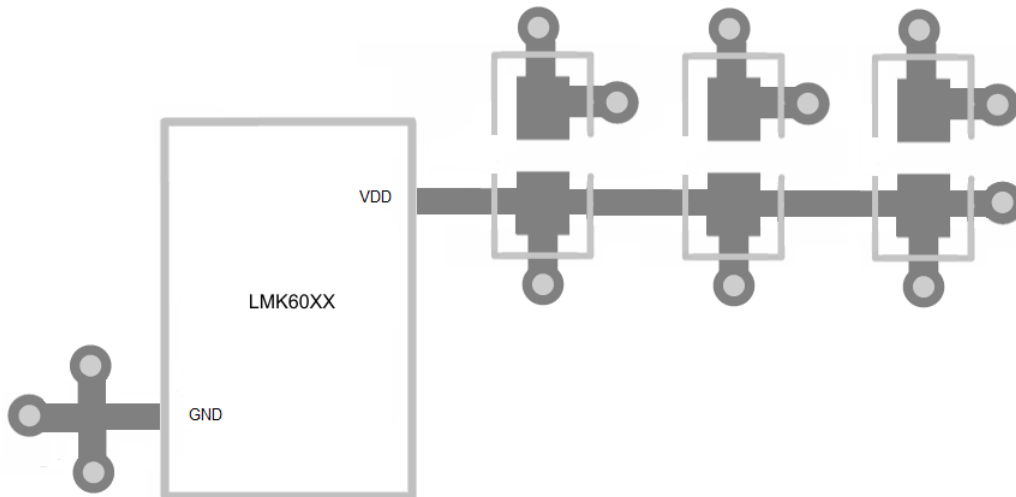
- $T_B$ : PCB temperature around the LMK60EX
  - $T_J$ : Junction temperature of LMK60EX
  - $\Psi_{JB}$ : Junction-to-board thermal resistance parameter of LMK60EX (48.7°C/W without airflow)
  - $P$ : On-chip power dissipation of LMK60EX
- (1)

To ensure that the maximum junction temperature of LMK60EX is below 105°C, it can be calculated that the maximum PCB temperature without airflow should be at 87°C or below when the device is optimized for best performance resulting in maximum on-chip power dissipation of 0.36 W.

#### 9.1.2 Best Practices for Signal Integrity

For best electrical performance and signal integrity of entire system with LMK60EX, TI recommends routing vias into decoupling capacitors and then into the LMK60EX. TI also recommends increasing the via count and width of the traces wherever possible. These steps ensure lowest impedance and shortest path for high frequency current flow. [Figure 9](#) shows the layout recommendation for LMK60EX.

## Layout Guidelines (continued)



**Figure 9. LMK60EX Layout Recommendation for Power Supply and Ground**

### 9.1.3 Recommended Solder Reflow Profile

TI recommends following the recommendations of the solder paste supplier to optimize flux activity and to achieve proper melting temperatures of the alloy within the guidelines of J-STD-20. Processing the LMK60EX to be processed with the lowest peak temperature possible while also remaining below the components peak temperature rating as listed on the MSL label is preferred. The exact temperature profile would depend on several factors including maximum peak temperature for the component as rated on the MSL label, board thickness, PCB material type, PCB geometries, component locations, sizes, densities within PCB, as well as the recommended soldering profile from the manufacturer and capability of the reflow equipment to as confirmed by the SMT assembly operation.

## 10 デバイスおよびドキュメントのサポート

### 10.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 10.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™オンライン・コミュニティ** *TIのE2E (Engineer-to-Engineer) コミュニティ*。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

**設計サポート** *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

### 10.3 商標

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 10.4 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

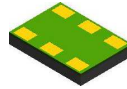
### 10.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 11 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

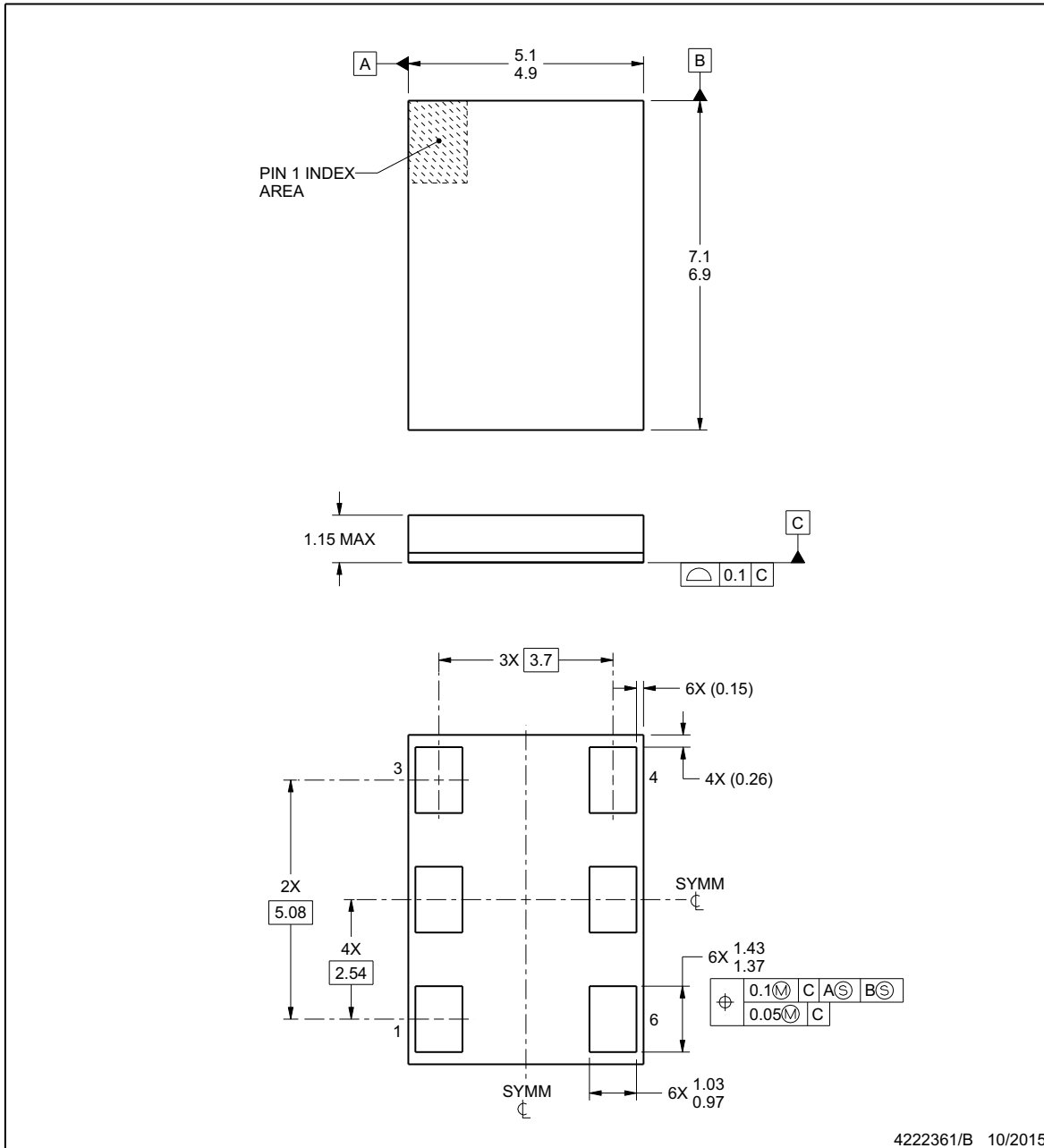


## PACKAGE OUTLINE

**SIA0006A**

**QFM - 1.15 mm max height**

QUAD FLAT MODULE



**NOTES:**

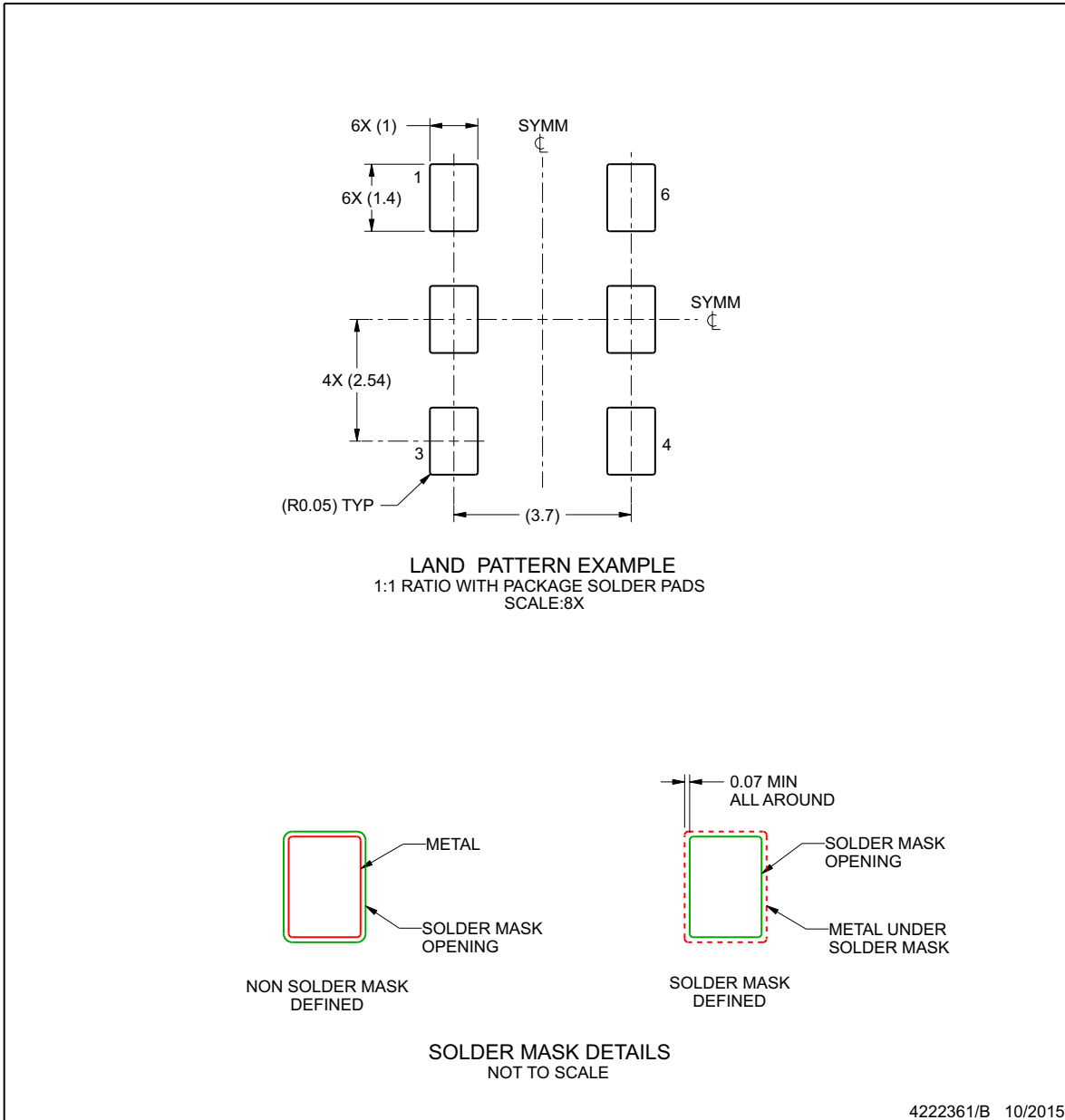
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

**EXAMPLE BOARD LAYOUT**

**SIA0006A**

**QFM - 1.15 mm max height**

QUAD FLAT MODULE



NOTES: (continued)

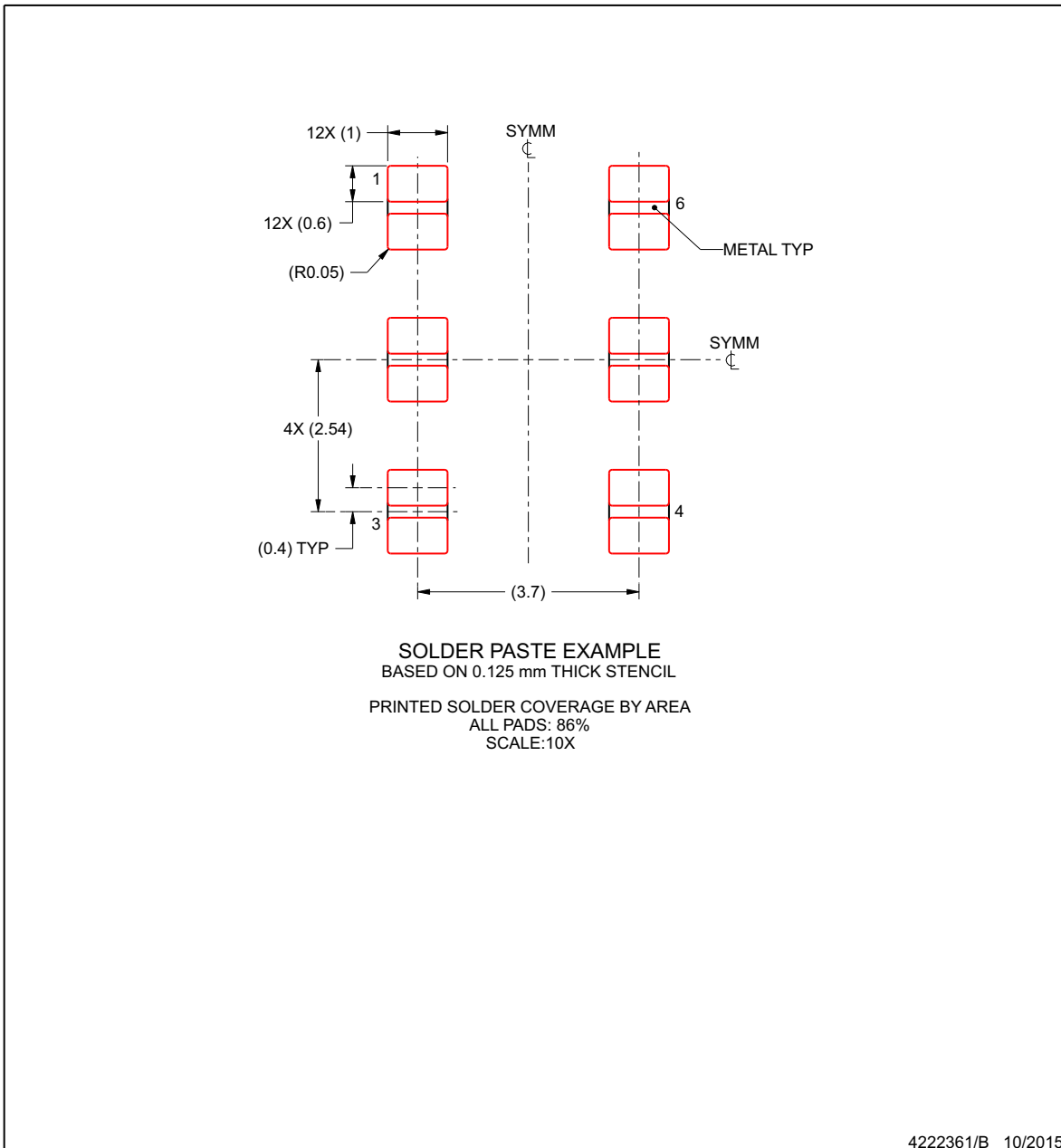
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

## EXAMPLE STENCIL DESIGN

**SIA0006A**

**QFM - 1.15 mm max height**

QUAD FLAT MODULE



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK60E0-156M25SIAR	ACTIVE	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 156M25	<a href="#">Samples</a>
LMK60E0-156M25SIAT	ACTIVE	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 156M25	<a href="#">Samples</a>
LMK60E0-212M50SIAR	NRND	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 212M50	
LMK60E0-212M50SIAT	NRND	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E0 212M50	
LMK60E2-100M00SIAR	NRND	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 100M00	
LMK60E2-100M00SIAT	NRND	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 100M00	
LMK60E2-125M00SIAR	NRND	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 125M00	
LMK60E2-125M00SIAT	NRND	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 125M00	
LMK60E2-156M25SIAR	NRND	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 156M25	
LMK60E2-156M25SIAT	NRND	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60E2 156M25	
LMK60I2-100M00SIAR	NRND	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60I2 100M00	
LMK60I2-100M00SIAT	NRND	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60I2 100M00	
LMK60I2-322M26SIAR	NRND	QFM	SIA	6	2500	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60I2 322M26	
LMK60I2-322M26SIAT	NRND	QFM	SIA	6	250	RoHS & Green	NIAU	Level-3-260C-168 HR	-40 to 85	LMK60I2 322M26	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK60E0-156M25SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E0-156M25SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E0-212M50SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E0-212M50SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E2-100M00SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E2-100M00SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E2-125M00SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E2-125M00SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E2-156M25SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60E2-156M25SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60I2-100M00SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60I2-100M00SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60I2-322M26SIAR	QFM	SIA	6	2500	330.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1
LMK60I2-322M26SIAT	QFM	SIA	6	250	178.0	16.4	5.5	7.5	1.5	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK60E0-156M25SIAR	QFM	SIA	6	2500	356.0	356.0	36.0
LMK60E0-156M25SIAT	QFM	SIA	6	250	213.0	191.0	55.0
LMK60E0-212M50SIAR	QFM	SIA	6	2500	356.0	356.0	36.0
LMK60E0-212M50SIAT	QFM	SIA	6	250	208.0	191.0	35.0
LMK60E2-100M00SIAR	QFM	SIA	6	2500	356.0	356.0	36.0
LMK60E2-100M00SIAT	QFM	SIA	6	250	208.0	191.0	35.0
LMK60E2-125M00SIAR	QFM	SIA	6	2500	356.0	356.0	36.0
LMK60E2-125M00SIAT	QFM	SIA	6	250	208.0	191.0	35.0
LMK60E2-156M25SIAR	QFM	SIA	6	2500	356.0	356.0	36.0
LMK60E2-156M25SIAT	QFM	SIA	6	250	208.0	191.0	35.0
LMK60I2-100M00SIAR	QFM	SIA	6	2500	356.0	356.0	36.0
LMK60I2-100M00SIAT	QFM	SIA	6	250	208.0	191.0	35.0
LMK60I2-322M26SIAR	QFM	SIA	6	2500	356.0	356.0	36.0
LMK60I2-322M26SIAT	QFM	SIA	6	250	208.0	191.0	35.0

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated