参考資料

AFE4300 体重および体組成測定用の低コスト統合アナログ・フロント・エンド

1 特長

- **体重計フロントエンド**
  - 4つまでの負荷セルの入力に対応
  - レシオメトリック測定用の、オンチップ負荷セルの励起電圧1.7V
  - 入力換算ノイズ68nVrms (0.1Hz～2Hz)
  - ベストフィット直線性: フルスケールの0.01%
  - 体重測定: 540µA
- **体組成フロント・エンド**
  - 3つまでの四極性複合インピーダンス測定に対応
  - 6ビット、1MSPSの正弦波を生成するデジタル/アナログ・コンバータ(DAC)
  - 247.5µArms、±20%の励起ソース
  - 2Hz BWで0.1Ωの測定RMSノイズ
  - 体組成測定: 970µA
- A/D**コンバータ**(ADC)
  - 16ビット、860SPS
  - 消費電流: 110µA

2 アプリケーション

体組成測定機能付きの体重計

3 概要

AFE4300は低コストのアナログ・フロント・エンドで、2つの独立した信号チェーンが組み込まれています。1つの信号チェーンは体重(WS)測定用で、もう1つは体組成測定(BCM)分析用です。16ビット、860SPSのアナログ/デジタル・コンバータ(ADC)が、両方のチェーン間で多重化されます。体重測定チェーンには、計装アンプ(INA)が含まれており、外付けの抵抗によりゲインが設定されます。その後に、6ビットのデジタル/アナログ・コンバータ(DAC)によるオフセット訂正と、レシオメトリック測定用の固定1.7Vで外部のブリッジ/負荷セルを駆動する回路があります。

また、AFE4300では正弦電流を身体に流すことで、体組成を測定できます。正弦電流は内部のパターン・ジェネレータと6ビット、1MSPSのDACにより生成されます。この正弦電流は、電圧から電流へのコンバータにより、2つの端子の間で人体に印加されます。身体のインピーダンスによって2つの端子間に発生する電圧が差動アンプで測定されて、整流され、16ビットのADCにより振幅が抽出されます。

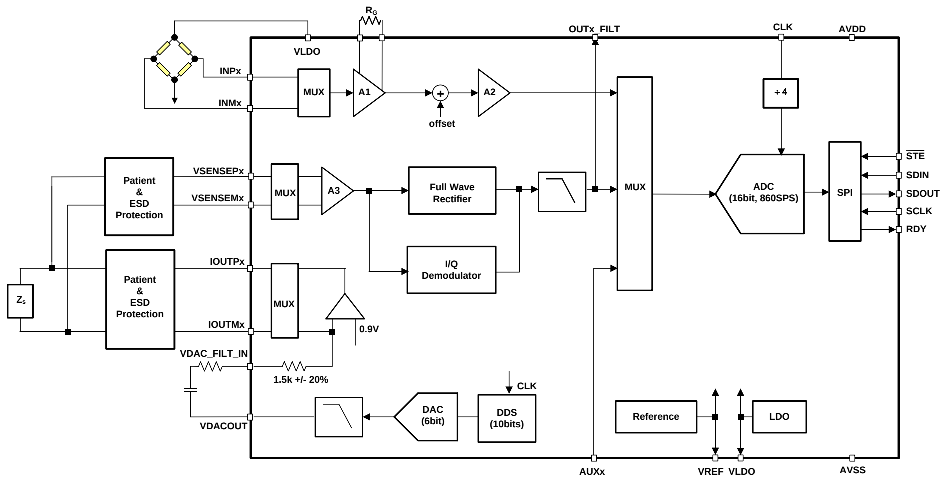
AFE4300は2V～3.6Vで動作し、0℃～+70℃で動作が規定されており、LQFP-80パッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
AFE4300	LQFP (80)	12.00mm×12.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

機能ブロック図



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4 改訂履歴

Revision B (June 2013) から **Revision C** に変更 **Page**

- 「*製品情報*」表、「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*プログラミング*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 1
- 「特長」の「*体組成*」の箇条書き項目で「*ダイナミック・レンジ*」の副項目を削除し、「*励起ソース*」副項目の「*375*」を「*247.5*」に 変更 1
- ドキュメント全体でTQFPをLQFPに変更 1
- Deleted *Package Information* section 4
- Changed *Pin Functions* table title 4
- Changed *clock* to *serial clock* in SCLK pin description of *Pin Functions* table 5
- Changed *VSENSEN* to *VSENSEM* in pins 41 and 42 in *Pin Functions* table 5
- Changed AVSS parameter name to *Ground* from *Supply voltage* in *Recommended Operating Conditions* table 6
- Changed symbol $R1$ to R_{FB1} in *Electrical Characteristics: Front-End Amplification (Weight-Scale Signal Chain)* table 7
- Changed typical specification of *DAC full-scale voltage* parameter from 1 to 1.05 in *Electrical Characteristics: Body Composition Measurement Front-End* table 8
- Changed *Electrical Characteristics: Digital Input/Output* table title 9
- Changed multiplication signs (×) to minimum and maximum specifications of *Electrical Characteristics: Digital Input/Output* table 9
- Changed x-axis unit from µArms to µApk in *BCM DAC Output Current Distribution* figure 11
- Changed Functional Block Diagram: swapped positions of RP1, RP0 and RN1, RN0 pins 12
- Changed *BCM in AC Rectifier Mode* figure: swapped positions of RP1, RP0 and RN1, RN0 pins 15
- Changed *AC Rectification* section: changed *images* to *high-frequency images* in second paragraph, *VDAC* to *VDACOUT* in Equation 5, and changed third paragraph 16
- Changed third paragraph of *AC Rectification* section: deleted*(still within the 500-µArms limit)* from fourth sentence, changed last sentence 16
- Changed *BCM in I/Q Demodulator Mode* figure: swapped positions of RP1, RP0 and RN1, RN0 pins 17
- Changed *Operating Modes* section 20

改訂履歴 (continued)

- Changed *negative input* to *output* in descriptions of IOUTP[5:0] and RP[1:0] and *output* to *negative input* in descriptions of IOUTN[5:0] and RN[1:0] in ISW_MUX register 26
- Changed bit 9 to DAC9 from 0 in BCM_DAC_FREQ register and changed bit count in bit descriptions to reflect this change 27
- Changed f_{CLK} = 1 MHz to f_{CLK} = 1.024 MHz in BCM_DAC_FREQ register........ 27
- Changed *Component Values Corresponding to Figure 12* table: changed title of second column from *Suggested Value* to *Illustrative Value*, R3, R4 illustrative value to 10 kΩ from 100 kΩ, and changed table footnote 30
- Changed 1 MHz to 1.024 MHz in *Example Value* column of *Weight Scale Design Requirements* table 32
- Deleted touch from list of possible power-up interrupts in third paragraph of *Detailed Design Procedure* section 33
- Changed first sentence of *Application Curve* section to reference Figure 15 33
- Changed *capacitor* to *capacitances* in last bullet of *Layout Guidelines* section 35

Revision A (June 2012) から Revision B に変更 **Page**

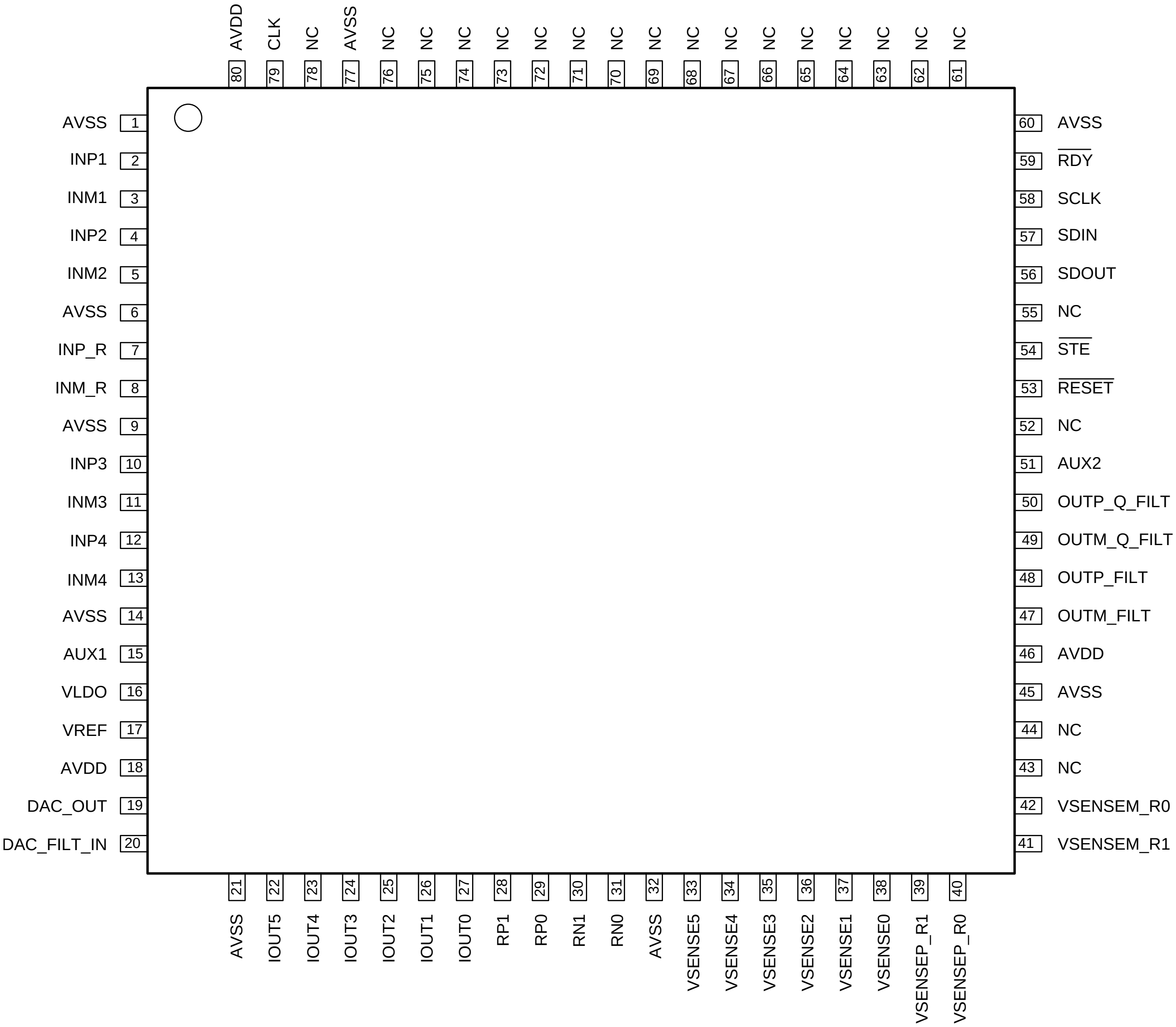
- Changed title condition for Electrical Charancteristics 7
- Changed test condition for rectifier bandwidth parameter........ 8
- Changed y-axis unit in Figure 5........ 11
- Changed R1 percentage in Functional Block Diagram 12
- Changed feedback resistor percentage in second paragraph after Figure 6........ 13
- Changed description for last row of Table 2........ 23
- Changed bit descriptions of ISW_MUX register 26
- Changed bit 9 for BCM_DAC_FREQ (Address 0x0E) 27
- Changed bit numbers for MISC_REGISTER3 (Address 0x1A)........ 29

2012年6月発行のものから更新 **Page**

- データシートを製品プレビューから量産データに変更........ 1

5 Pin Configuration and Functions

PN Package
80-Pin LQFP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NUMBER		
AAUX1	15	I	Auxiliary input to the ADC
AAUX2	51	I	Auxiliary input to the ADC
AVDD	18, 46, 80	—	Supply (3.3 V)
AVSS	1, 6, 9, 14, 21, 32, 45, 60, 77	—	Ground
CLK	79	I	1-MHz clock
DAC_FILT_IN	20	I	Current generator input. Connect ac blocking capacitor between this pin and pin 19.
DACOUT	19	O	DAC output. Connect ac blocking capacitor between this pin and pin 20.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	**NUMBER**		
INM1	3	I	Instrumentation amplifier differential inputs for each of the four weight-scale channels
INM2	5		
INM3	11		
INM4	13		
INP1	2		
INP2	4		
INP3	10		
INP4	12		
INM_R	8	—	Connection of gain setting resistor for the instrumentation amplifier
INP_R	7	—	
IOUT0	27	O	Current source output to electrodes
IOUT1	26		
IOUT2	25		
IOUT3	24		
IOUT4	23		
IOUT5	22		
NC	43, 44, 52, 55, 61-76, 78	—	Do not connect
OUTM_I_FILT	47	—	I channel demodulator low pass filter, connect 10 µF between both pins
OUTP_I_FILT	48		
OUTM_Q_FILT	49	—	Q channel demodulator low pass filter, connect 10 µF between both pins
OUTP_Q_FILT	50		
$\overline{\text{RDY}}$	59	O	Data ready
RN0	31	O	Current source output to calibration resistors
RN1	30		
RP0	29		
RP1	28		
$\overline{\text{RST}}$	53	I	Reset. 0: reset, 1: normal operation.
SCLK	58	I	Serial clock to latch input data (negative edge latch)
SDIN	57	I	Serial data input
SDOUT	56	O	Serial data output
$\overline{\text{STE}}$	54	I	SPI enable. 0: shift data in, 1: disable.
VLDO	16	O	LDO output to supply the bridges (~1.7 V), connect 470 nF to AVSS
VREF	17	O	Reference voltage (connect 470 nF to AVSS)
VSENSEM_R0	42	I	Input to differential amplifier from calibration resistors
VSENSEM_R1	41		
VSENSEP_R0	40		
VSENSEP_R1	39		
VSENSE0	38	I	Input to differential amplifier from electrode
VSENSE1	37		
VSENSE2	36		
VSENSE3	35		
VSENSE4	34		
VSENSE5	33		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range	AVDD to AVSS	–0.3	4.1	V
	Any pin	–0.3	AVDD + 0.3	
Diode current at any device pin			±2	mA
Maximum operating junction temperature, T_J max			105	°C
Storage humidity		10%	90%	Rh
Storage temperature, T_{stg}		–25	85	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
AVDD	Supply voltage	2		3.6	V
AVSS	Ground		0		V
f_{CLK}	External clock input frequency		1		MHz
T_A	Ambient temperature range	0		70	°C

6.4 Thermal Information

THERMAL METRIC(1)		AFE4300 PN (LQFP) 80 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: Front-End Amplification (Weight-Scale Signal Chain)

over operating free-air temperature range, AVDD – AVSS = 3 V, G1 = 183, and G2 = 1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	AFE4300			UNIT
			MIN	TYP	MAX	
BRIDGE SUPPLY						
$V_{(VLDO)}$	Output voltage (bridge supply voltage)			1.7		V
I_O	Output current	Current capability			20	mA
		Short-circuit protection		100		mA
t_{STBY}	Enable, disable time	With 470-nF capacitor on the VLDO pin		1		ms
AMPLIFICATION CHAIN						
	Offset error	With offset correction DAC disabled		80		µV
	Offset drift vs temperature	With offset correction DAC disabled		0.25		µV/°C
	Input bias current			±70		fA
	Input offset current			±140		fA
V_n	Noise voltage, equivalent input	G1 = 183, 0.01 Hz < f < 2 Hz		68		nVrms
I_n	Noise current, equivalent input	f = 10 Hz		100		$fA/\sqrt{Hz}$
z_{id}	Differential input impedance			100 || 4		GΩ || pF
z_{ic}	Common-mode input impedance			100 || 8		GΩ || pF
CMRR	Input common-mode rejection ratio	G1 = 183		95		dB
INL_{WS}	Gain nonlinearity	From input to digital output (including ADC)		0.01		% of FS(1)
	First-stage gain equation			$(1 + 2 \times 100k / R_G)$		V/V
t_{up}	Power-up time	From power up to valid reading		1		ms
R_{FB1}	Internal feedback resistors		95	100	105	kΩ
Gain2	Second-stage gain settings			1, 2, 3, 4		
	Total gain error			±5%		
	Offset DAC number of bits			6		Bits
I_{DAC}	Full-scale offset DAC output current			±6.5		µA

(1) FS = full-scale.

6.6 Electrical Characteristics: Body Composition Measurement Front-End

over operating free-air temperature range, AVDD – AVSSS = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	AFE4300			UNIT
			MIN	TYP	MAX	
WAVEFORM GENERATOR						
	DAC resolution			6		Bits
	DAC full-scale voltage	Common-mode voltage = 0.9 V		1.05		$V_{(PP)}$
	DAC sample rate			1		MSPS
BW_{LPF}	–3 dB bandwidth of the 2nd-order low-pass filter			150 ±30		kHz
R1	Internal current-setting resistor			1.5 ±20%		kΩ
DEMODULATION CHAIN						
	Input Impedance			50		kΩ
	Gain	From impedance to dc output of demodulator, IQ mode and FWR mode		0.72		V/kΩ
	Gain error (without calibration)	FWR mode and I/Q mode		2.5		% of FS
	Offset error (without calibration)	FWR mode and I/Q mode		±5		mV
CMRR	Common-mode rejection ratio			75		dB
	Nonlinearity	0-Ω to 1.25-kΩ range		0.15		% of FS
		0-Ω to 2.50-kΩ range		3		% of FS
BW_{DEMOD}	Rectifier bandwidth	Internal resistor = 5 kΩ, external capacitor = 4.7 µF		3.5 ±20%		Hz
	Output noise at rectifier output	20-kHz waveform, noise integrated from 0.01 Hz to 2 Hz		15		µVrms

6.7 Electrical Characteristics: Analog-to-Digital Converter

over operating free-air temperature range, AVDD – AVSS = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	AFE4300			UNIT
			MIN	TYP	MAX	
ANALOG-TO-DIGITAL CONVERTER						
	ADC input voltage range	At the input of the ADC (after PGA)		2 × V_{REF}		V
V_{IN}	Full-scale input voltage	At the input of the PGA		V_{ADC} / Gain		V
V_{REF}	Reference voltage			1.7		V
$R_{ON(mux)}$	Input multiplexer on-resistance	0 V ≤ V_{AAUX} ≤ AVDD			6	kΩ
	AAUX input impedance			4		MΩ
f_{DR}	Output data rate		8		860	SPS
	Resolution		16			Bits
E_I	Integral linearity error	Best fit, DR = 8 SPS		1		LSB
E_O	Offset error	Differential inputs		±1		LSB
		Single-ended inputs		±3		LSB
E_G	Gain error			0.05%		
V_{BAT_MON}	Battery monitor output			AVDD / 3		V
I_{BAT_MON}	Battery monitor current consumption			1.5		µA
$I_{BAT\_MON\_ACC}$	Battery monitor accuracy			±2%		
POWER CONSUMPTION						
	Supply current	Power-down current		0.25		µA
		Sleep-mode current		100		µA
		Weight-scale chain measurements		540		µA
		Body-composition measurements		970		µA
		Auxillary-channel measurements		110		µA

6.8 Electrical Characteristics: Digital Input/Output

over operating free-air temperature range, AVDD – AVSS = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		0.75 × AVDD		AVDD	V
V_{IL}	Low-level input voltage		AVSS		0.25 × AVDD	V
V_{OH}	High-level output voltage	I_{OL} = 1 mA	0.8 × AVDD			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA	GND		0.2 × AVDD	V
I_{IN}	Input current			±30		µA

6.9 Timing Requirements: Serial Interface Timing

at T_A = 0°C to +70°C and VDD = 2 V to 3.6 V (unless otherwise noted)

		MIN	NOM	MAX	UNIT
t_{CSSC}	$\overline{\text{STE}}$ low to first SCLK setup time(1)	100			ns
t_{SCLK}	SCLK period	250			ns
t_{SPWH}	SCLK pulse duration high	100			ns
t_{SPWL}	SCLK pulse duration low	100			ns
t_{DIST}	Valid SDIN to SCLK falling edge setup time	50			ns
t_{DIHD}	Valid SDIN to SCLK falling edge hold time	50			ns
t_{DOPD}	SCLK rising edge to valid new SDOUT propagation delay(2)			50	ns
t_{DOHD}	SCLK rising edge to DOUT invalid hold time	0			ns
t_{CSDOD}	$\overline{\text{STE}}$ low to SDOUT driven propagation delay	100			ns
t_{CSDOZ}	$\overline{\text{STE}}$ high to SDOUT Hi-Z propagation delay	100			ns
t_{CSH}	$\overline{\text{STE}}$ high pulse	200			ns
t_{SCCS}	Final SCLK falling edge to $\overline{\text{STE}}$ high	100			ns

(1) $\overline{\text{STE}}$ can be tied low.
(2) DOUT load = 20 pF || 100 kΩ to DGND.

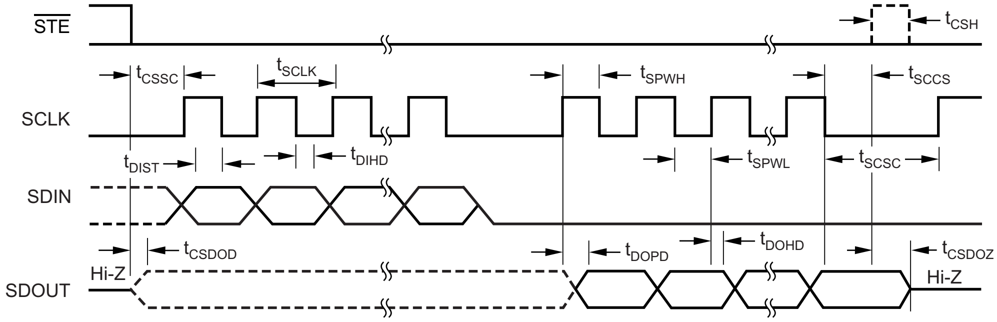


Figure 1. Serial Interface Timing

6.10 Typical Characteristics

all measurements at room temperature with AVDD = 3 V (unless otherwise specified)

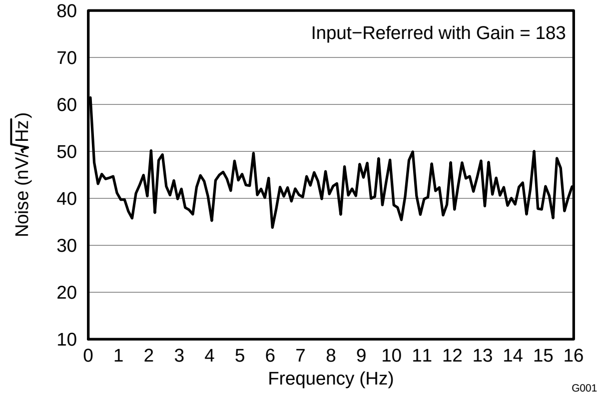


Figure 2. Weight-Scale Chain Noise vs Frequency

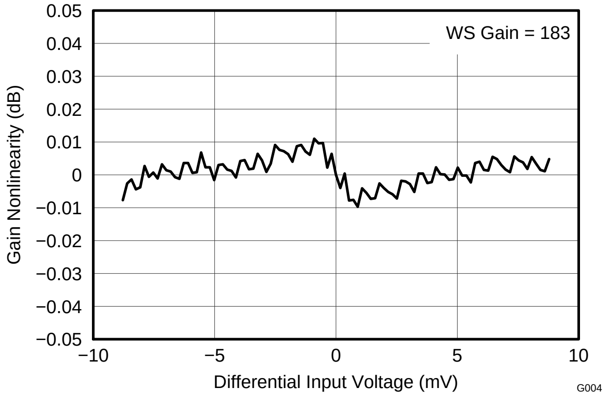


Figure 3. Weight-Scale Chain Nonlinearity

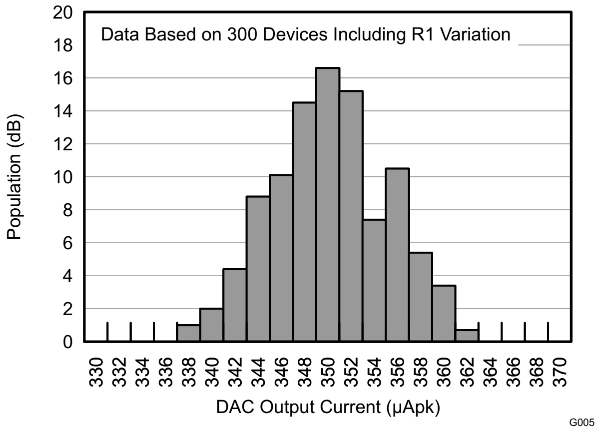


Figure 4. BCM DAC Output Current Distribution

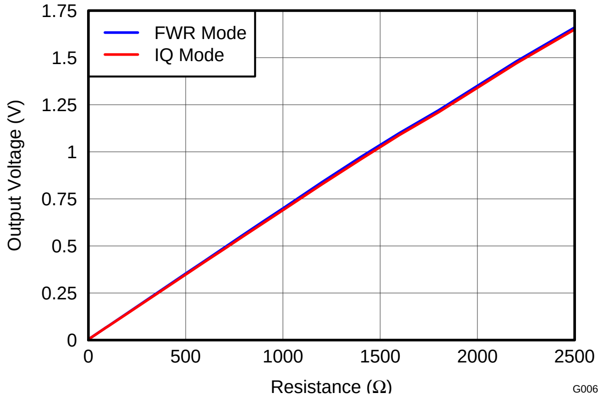


Figure 5. Body Impedance to Output Voltage Transfer Curve

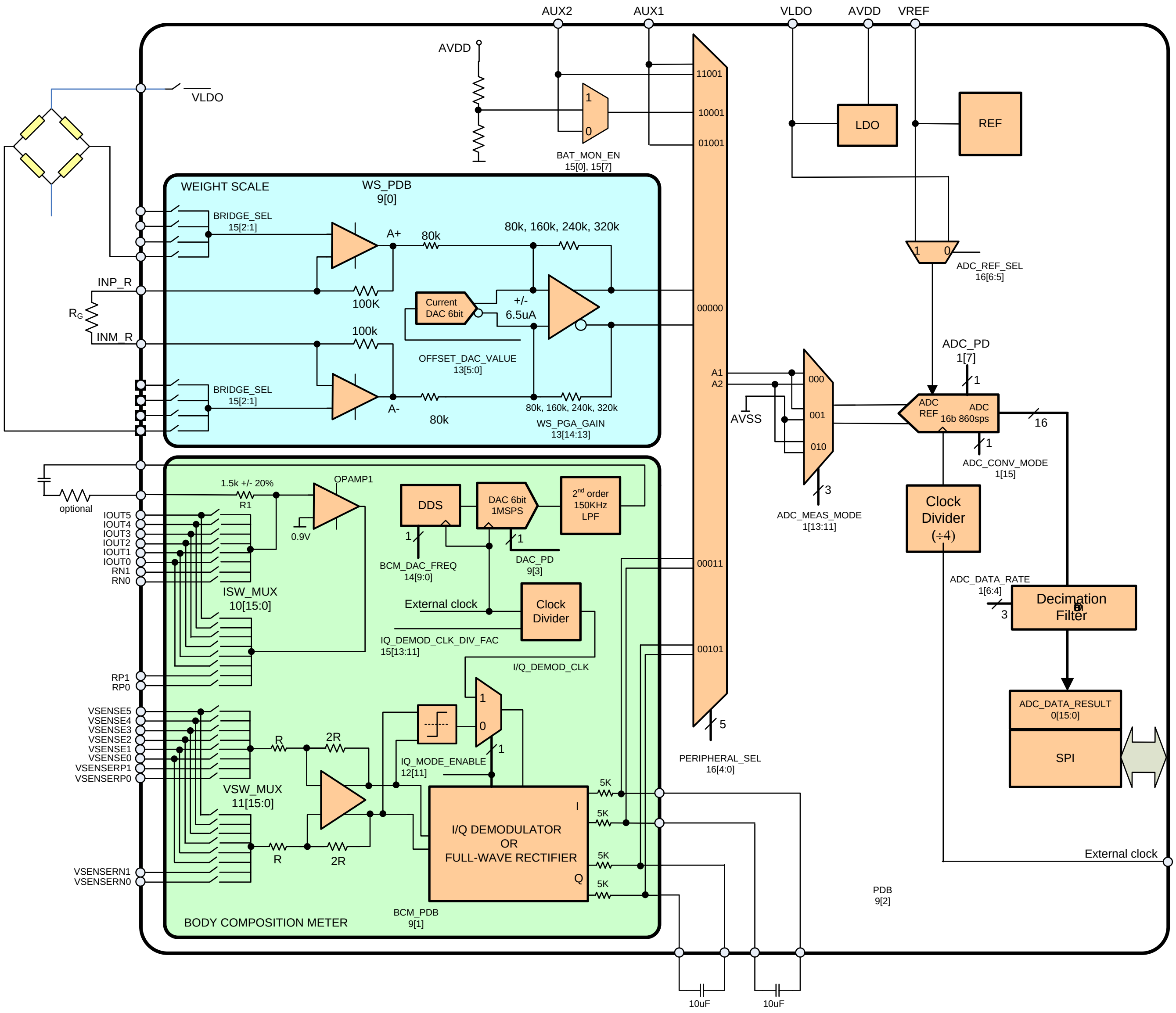
7 Detailed Description

7.1 Overview

The AFE4300 is a low-cost, integrated front-end designed for weight scales incorporating body-composition measurements. The AFE4300 integrates all the components typically used in a weight scale. The device has two signal chains: one for weight scale measurements and the other for body composition measurements. Both signal chains share a 16-bit, delta-sigma converter that operates at a data rate of up to 860 SPS. This device also integrates a reference and a low-dropout regulator (LDO) that generates a 1.7-V supply that can be used as the excitation source for the load cells, thus simplifying ratiometric measurements. Both the signal chains use a single digital-to-analog converter (DAC). The DAC is used to generate the dc signal for load-cell offset cancellation in the weight-scale chain. The same DAC is also used to generate the sine-wave modulation signal for the body-composition signal chain. Therefore, only one of the two signal chains can be activated at a time (using the appropriate register bits).

Two unique features of the AFE4300 are that the device provides an option for connecting up to four separate load cells, and supports tetrapolar measurements with I/Q measurements.

7.2 Functional Block Diagram



7.3 Feature Description

This section describes the details of the AFE4300 internal functional elements. The analog blocks are reviewed first, followed by the digital interface. The theory behind the body-composition measurement using the full-wave rectification method and the I/Q demodulation method are also described. The analog front-end is divided in two signal chains: a weight-measurement chain and a body-composition measurement front-end chain; both use the same 16-bit ADC and 6-bit DAC.

Throughout this document:

- f_{CLK} denotes the frequency of the signal at the CLK pin.
- t_{CLK} denotes the period of the signal at the CLK pin.
- f_{DR} denotes the output data rate of the ADC.
- t_{DR} denotes the time period of the output data.
- f_{MOD} denotes the frequency at which the modulator samples the input.

7.3.1 Weight-Scale Analog Front-End

Figure 6 shows a top-level view of the front-end section devoted to weight-scale measurement. The weight-scale front-end has two stages of gain, with an offset correction DAC in the second gain stage. The first-stage gain is set by the external resistor and the second-stage gain is set by progamming the internal registers. For access and programming information, see the *Register Maps* section.

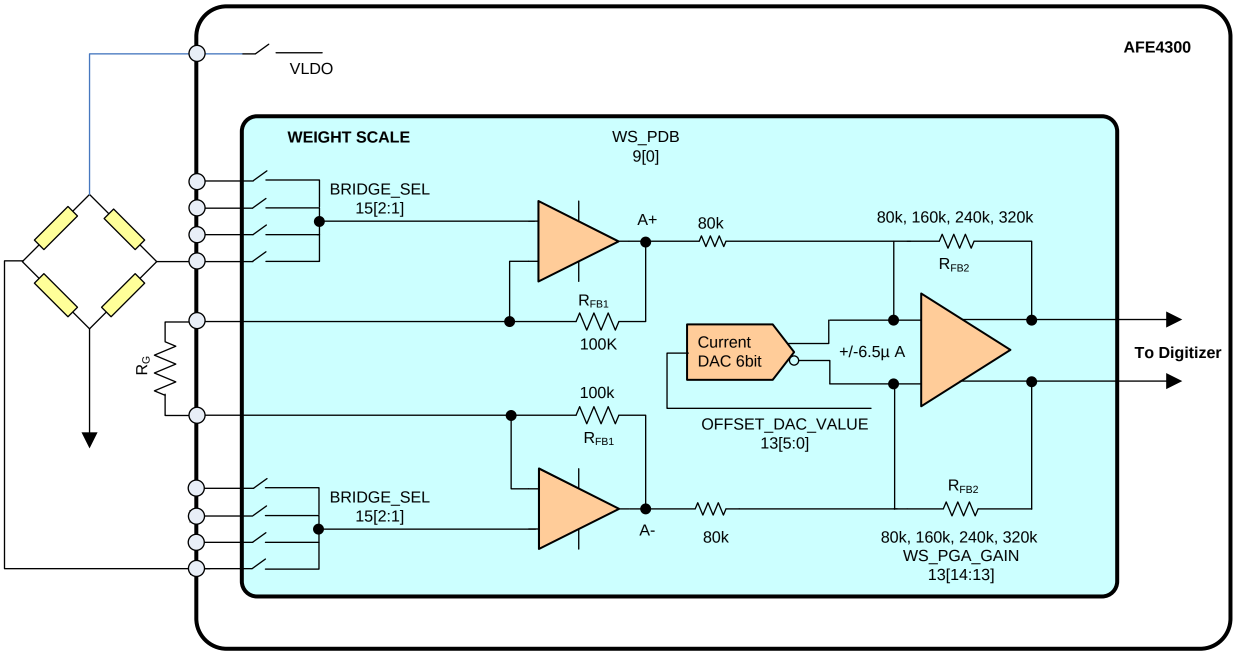


Figure 6. Weight-Scale Front-End

Though not shown in the diagram, an antialiasing network is required in front of the INA to filter out electromagnetic interference (EMI) signals or any other anticipated interference signals. A simple RC network is sufficient, combined with the attenuation provided by the on-chip decimation filter.

An internal reference source provides a constant voltage of 1.7 V at the VLDO output to drive the external bridge. The output of the bridge is connected to an INA (first stage). The first-stage gain (A_1) is set by the external resistor (R_G) and the 100-kΩ (±5%) internal feedback resistors (R_{FB1}) as shown in Equation 1:

$$A_1 = (1 + 2 \times 100k / R_G) \tag{1}$$

The second-stage gain (A_2) is controlled by feedback resistors R_{FB2}, which have four possible values: 80 kΩ, 160 kΩ, 240 kΩ, and 320 kΩ. Because the gain is R_F / 80 kΩ, the gain setting can be 1, 2, 3, or 4. See the *Register Maps* section for details on setting the appropriate register bits.

Feature Description (continued)

7.3.1.1 Input Common Mode Range

The usable input common mode range of the weight-scale front-end depends on various parameters, including the maximum differential input signal, supply voltage, and gain. The output of the first-stage amplifier must be within 250 mV of the power supply rails for linear operation. The allowed common-mode range is determined by Equation 2:

$$\mathrm{AVDD} - 0.25 - \frac{\mathrm{GAIN} \times V_{\mathrm{MAX\_DIFF}}}{2} > \mathrm{CM} > \mathrm{AVSS} + 0.25 + \frac{\mathrm{GAIN} \times V_{\mathrm{MAX\_DIFF}}}{2}$$

Where:

- V_{MAX_DIFF} = maximum differential input signal at the input of the first gain stage,
- CM = Common-mode range. (2)

For example, If AVDD = 2 V, the first stage gain = 183, and V_{MAX_DFF} = 7.5 mV (dc + signal), then:

1.06 V > CM > 0.936 V

7.3.1.2 Input Differential Dynamic Range

The max differential (INP – INN) signal depends on the analog supply, reference used in the system. This range is shown in Equation 3:

$$\mathrm{MAX(INP - INN)} < \frac{\mathrm{VREF}}{\mathrm{GAIN}}\text{; Full-Scale Range} = 2 \times \frac{\mathrm{VREF}}{\mathrm{GAIN}} \tag{3}$$

The gain in Equation 3 is the product of the gains of the INA and the second-stage gain. The full-scale input from the bridge signal typically consists of a differential dc offset from the load cell plus the actual weight signal. Having a high gain in the first stage helps minimize the effect of the noise addition from the subsequent stages. However, make sure to choose a gain that does not saturate the first stage with the full-scale signal. Also, the common-mode of the signal must fall within the range, as per Equation 2.

7.3.1.3 Offset Correction DAC

One way to increase the dynamic range of the signal chain is by calibrating the inherent offset of the load cell during the initial calibration cycle. The offset correction is implemented in the second stage with a 6-bit differential DAC, where each output is a mirror of the other and can source or sink up to 6.5 µA. The effect at the output of the second stage is an addition of up to ±6.5 µA × 2 × R_{FB2}. This effect is equivalent to a voltage at the input of the second stage (A+ / A–) of up to ±6.5 µA × 2 × 80 kΩ = ±1 V, when R_{FB2} = 80 kΩ. The first-stage saturation cannot be avoided using this DAC. Because the offset correction DAC is a 6-bit DAC, the offset compensation step is 2 V / 2^6 = 31.2 mV when referred to the input of the second stage.

7.3.1.3.1 Offset Correction Example

As an example, use a bridge powered from 1.7 V with 1.5 mV/V sensitivity and a potential offset between –4 mV and 4 mV. Worst case, the maximum signal is 4 mV of offset plus 1.7 × 1.5 mV/V = 2.55 mV of signal, for a total of 6.55 mV. The bridge common-mode voltage is ~0.85 V. The maximum excursion is 0.85 V – 0.25 V = 0.6 V (bottom rail) single-ended, on each output (A+ or A–). Therefore, ±1.2 V differentially at the output of the first stage prevents saturation. This result means that the first stage can have up to a gain of 1.2 V / 6.55 mV = 183.

Using this same example, the swing at the output of the first stage corresponding only to the potential offset range is 183 × ±4 mV = ±0.732 V. This swing can be completely removed at the output of the second stage by the offset correction (because the offset correction DAC has a ±1-V range) except for a maximum error of 31.2 mV.

Feature Description (continued)

7.3.2 Body Composition Measurement Analog Front-End

Body composition is traditionally obtained by measuring the impedance across several points on the body and matching the result in a table linking both the impedance measured and the body composition. This table is created by each manufacturer and is usually based on age group, sex, weight, and other parameters.

The body impedance that we want to measure, Z(f), is a function of the excitation frequency, and can be represented by polar or cartesian notations:

$$Z(f) = \left|Z(f)\right|.e^{j\theta(f)} = R(f) + jX(f)$$

where:

- $|Z| = \text{sqrt}(R^2 + X^2)$
- $\theta = \text{arctg}(X/R)$ (4)

The AFE4300 provides two options for body impedance measurement: ac rectification and I/Q demodulation. Both options work by injecting a sinusoidal current into the body and measuring the voltage across the body. The portion of the circuit injecting the current into the body is the same for each of those options. The difference, however, lies in how the measured voltage across the impedance is processed to obtain the final result.

7.3.2.1 AC Rectification

Figure 7 shows the portion of the AFE4300 devoted to body composition measurement in the RMS detector mode.

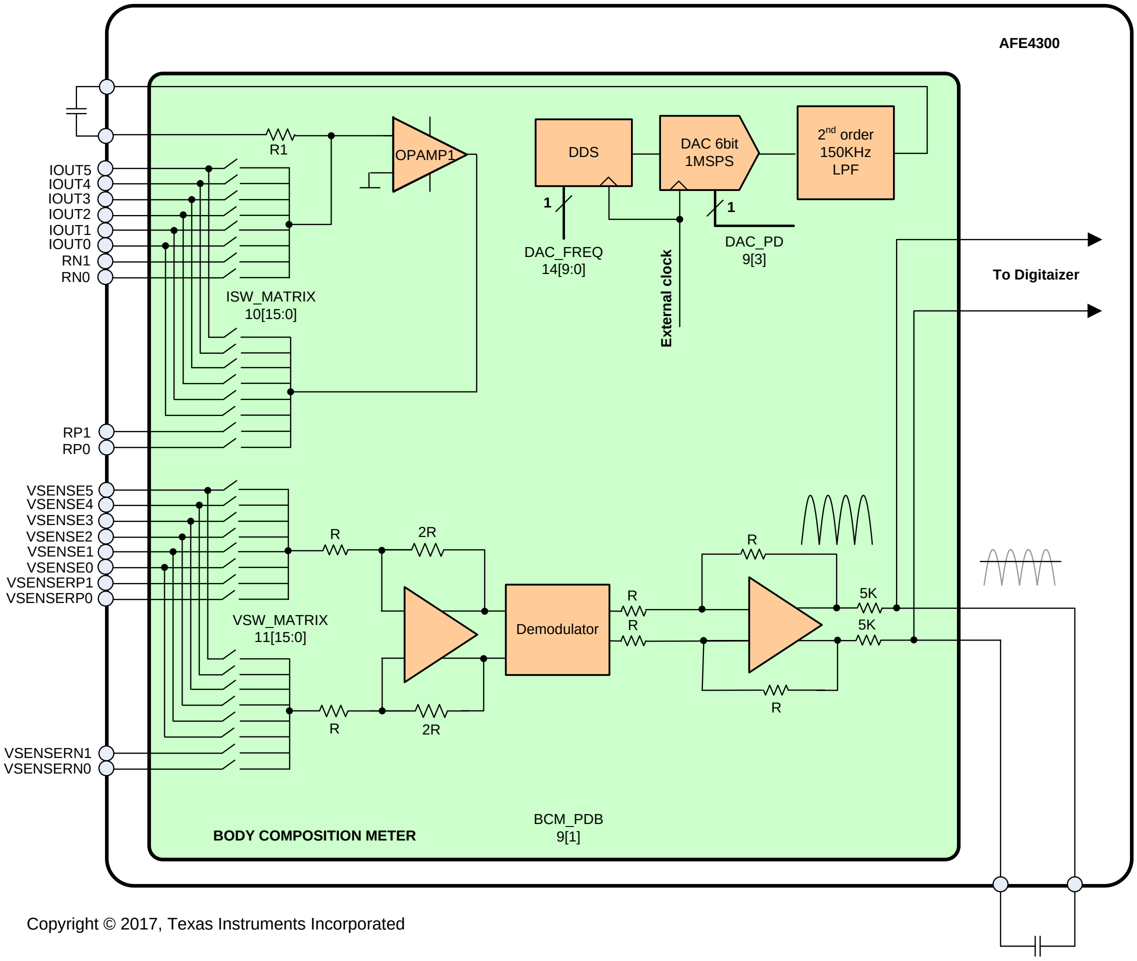


Figure 7. BCM in AC Rectifier Mode

Feature Description (continued)

The top portion of Figure 7 represents the current-injection circuit. A direct digital synthesizer (DDS) generates a sinusoidal digital pattern with a frequency obtained by dividing a 1-MHz clock with a 10-bit counter. The digital pattern drives a 6-bit, 1-MSPS DAC. The output of the DAC is filtered by a 150-kHz, second-order filter to remove the high-frequency images, followed by a series external capacitor to block the dc current and avoid any dc current injection into the body. The output of the filter (after the dc blocking capacitor) drives a resistor setting the amplitude of the current to be injected in the body, as shown in Equation 5:

$$I(t) = \mathrm{VDACOUT} / \mathrm{R1} = A \sin(w_0 t) \tag{5}$$

The nominal DACOUT voltage (VDACOUT) is 1.05 V_{PP} (371.23 µVrms). The nominal value of R1 is 1.5 kΩ. So the nominal excitation current is 247.5 µArms. R1 can have a ±20% device-to-device variation, so the highest current is close to 300 µArms (850 μA_{PP}). The maximum voltage swing for the excitation electrodes (IOUT1-IOUT0) is 1 V_{PP}. This swing limits the recommended total impedance in feedback to approximately 1175 Ω. To reduce the excitation current, place an external resistor, R_{DAC}, (between DACOUT and DAC_FILT_IN) in series with R1. For example, with a 1.5-kΩ external resistor, the currents roughly reduce by 2X, thereby extending the range of the measured impedance.

Current flows into the body through an output analog multiplexer (mux) that allows the selection of up to six different contact points on the body. The same mux allows the connection of four external impedances for calibration. The current crosses the body impedance and a second mux selects the return path (contact) on the body, closing the loop to the output of the amplifier.

At the same time that the current is injected, a second set of multiplexers connects a differential amplifier across the same body impedance in order to measure the voltage drop created by the injected current, shown by Equation 6:

$$v(t) = A|Z| \sin(\omega_0 t + \theta)$$

where Z and θ are the module and phase of the impedance at ω_0, respectively. (6)

The output of the amplifier is routed to a pair of switches that implement the demodulation at the same frequency as the excitation current source in order to drive the control of those switches. This circuit performs a full-wave rectification of the differential amplifier output and a low-pass filter at the output, recovers the dc level, and finally routes the amplifier output to the same 16-bit digitizer used in the weight-scale chain.

$$\mathrm{DC} = \frac{2}{T} \int_{T/2} A\,|\,Z\,|\, \sin(\omega_0 t + \theta)\,dt = \frac{2A|Z|}{\pi} \tag{7}$$

Ultimately, the dc output is proportional to the module of the impedance. The proportionality factor can be obtained through calibration with the four external impedances. Although, with one single frequency or measurement, only the module of the impedance can be obtained; two different frequencies could be used to obtain both the real and the imaginary parts.

Feature Description (continued)

7.3.2.2 I/Q Demodulation

The AFE4300 includes a second circuit that with a single frequency measurement, obtains both the real and the imaginary portions, as shown in Figure 8. As explained previously, the portion of the circuit injecting the current into the body is the same for both configurations. Therefore, the circuit is the same in Figure 7 and Figure 8. The difference between them is that an I/Q demodulator is used in this second approach, as shown in Figure 8.

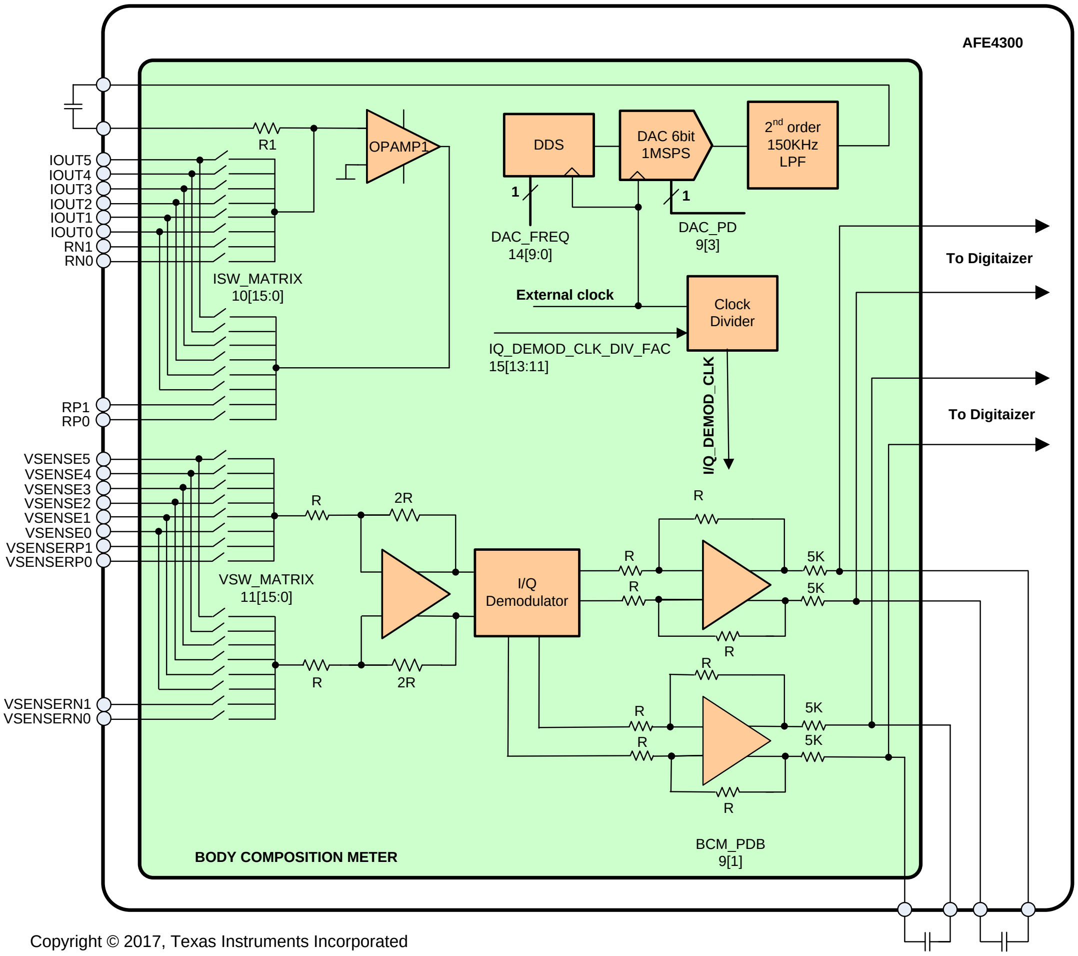


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Figure 8. BCM in I/Q Demodulator Mode

As with the case of the RMS detector, a differential amplifier measures the voltage drop across the impedance, as shown in Equation 8:

$$v(t) = A\left|Z\right|\sin(\omega_0 t + \theta)$$

where:

- Z = the module of the impedance at ω_0
- θ = phase of the impedance at ω_0 (8)

The I/Q demodulator takes the v(t) signal and outputs two dc values. These two values are used to extract the impedance module and phase with a single frequency measurement. Figure 8 shows the block diagrm of the implementation. Using the I/Q demodulator helps reduce power consumption and still yields excellent performance. The local oscillator (LO) signals for the mixers are generated from the same clock driving the DDS/DAC and are of the same phase and frequency as the sinusoidal i(t) (see Equation 5). The LO signals directly control the switches on the in-phase (I) path, and after a delay of 90° degrees, control the switches on the quadrature (Q) path. This switching results in multiplying the v(t) signal by a square signal swinging from –1 to 1.

Feature Description (continued)

Breaking down the LO signal into Fourier terms results in Equation 9:

$$LO_I(t) = \frac{4}{\pi}\left(\sin(\omega_0 t) + \frac{1}{3}\sin(3\omega_0 t) + \frac{1}{5}\sin(5\omega_0 t) + ...\right) \tag{9}$$

Therefore, the output voltage of the mixer is as shown in Equation 10:

$$I(t) = A|Z|\frac{4}{\pi}\left(\sin(\omega_0 t+\theta)\sin(\omega_0 t) + \frac{1}{3}\sin(\omega_0 t+\theta)\sin(3\omega_0 t) + \frac{1}{5}\sin(\omega_0 t+\theta)\sin(5\omega_0 t) + ...\right)$$

Where I(t) = in-phase output (not to be confused with i(t), the current injected in the impedance). (10)

Applying fundamental trigonometry gives Equation 11:

$$\sin a \ \sin b = -\frac{1}{2}\cos(a+b) + \frac{1}{2}\cos(a-b) \tag{11}$$

Each product of sinusoids can be broken up in an addition of two sinusoids. Equation 12 shows the first term:

$$\sin(\omega_0 t+\theta)\sin(\omega_0 t) = \frac{1}{2}\cos(\omega_0 t+\theta-\omega_0 t) - \frac{1}{2}\cos(\omega_0 t+\omega_0 t+\theta) = \frac{1}{2}\cos(\theta) - \frac{1}{2}\cos(2\omega_0 t+\theta) \tag{12}$$

Equation 13 shows the 2nd product:

$$\sin(\omega_0 t+\theta)\sin(3\omega_0 t) = \frac{1}{2}\cos(\omega_0 t+\theta-3\omega_0 t) - \frac{1}{2}\cos(3\omega_0 t+\omega_0 t+\theta) = \frac{1}{2}\cos(-2\omega_0 t+\theta) - \frac{1}{2}\cos(4\omega_0 t+\theta) \tag{13}$$

And so on. Performing the same analysis on the Q side, the output voltage of the mixer is shown in Equation 14:

$$Q(t) = A|Z|\frac{4}{\pi}\left(\sin(\omega_0 t+\theta)\cos(\omega_0 t) + \frac{1}{3}\sin(\omega_0 t+\theta)\cos(3\omega_0 t) + \frac{1}{5}\sin(\omega_0 t+\theta)\cos(5\omega_0 t) + ...\right) \tag{14}$$

Agiain, applying fundamental trigonometry gives Equation 15:

$$\sin a \ \cos b = \frac{1}{2}\sin(a+b) + \frac{1}{2}\sin(a-b) \tag{15}$$

Each of the products can be broken up into sums. Starting with the first product, as shown in Equation 16:

$$\sin(\omega_0 t+\theta)\cos(\omega_0 t) = \frac{1}{2}\sin(2\omega_0 t+\theta) + \frac{1}{2}\sin(\theta) \tag{16}$$

And so on. Note that on I(t) as well as on Q(t), all the terms beyond the cutoff frequency of the low-pass filter at the output of the mixers (setup by the two 1-kΩ resistors and an external capacitor) are removed, leaving only the dc terms, giving Equation 17 for I_{DC} and Equation 18 for Q_{DC}:

$$I_{DC} = \frac{2A|Z|}{\pi}\cos(\theta) = K|Z|\cos(\theta) \tag{17}$$

$$Q_{DC} = \frac{2A|Z|}{\pi}\sin(\theta) = K|Z|\sin(\theta) \tag{18}$$

In reality, the LO amplitude is not known (likely, not ±1) and affects the value of K in Equation 17 and Equation 18. Solving these two equations gives Equation 19:

$$\theta = \arctan\frac{Q_{DC}}{I_{DC}}$$

$$Z = \frac{1}{K}\sqrt{I_{DC}{}^2 + Q_{DC}{}^2} \tag{19}$$

In order to account for all the nonidealities in the system, the AFE4300 also offers four extra terminals on the driving side (two to drive, and two for the currents to return) and four extra terminals on the receive/differential-amplifier side. As with RMS mode, these spare terminals allow for connection of up to four external calibration impedances, and they also compute *K*.

Feature Description (continued)

7.3.3 Digitizer

The digitizer block includes an analog mux and a 16-bit sigma-delta ADC.

7.3.3.1 Multiplexer

There are two levels of analog mux. The first level selects from among the outputs of the weight scale, the body composition function, two auxiliary inputs, and the battery monitor. A second mux is used to obtain the measurement of the outputs coming from the first mux, either differentially or with respect to ground (single-ended). Note that when measuring single-ended inputs, the negative range of the output codes are not used. For battery or AVDD monitoring, an internal 1/3 resistor divider is included that enables the measurement using only one reference setting for any battery voltage, thus simplifying the monitoring routine.

7.3.3.2 Analog-to-Digital Converter

The 16-bit, delta-sigma, ADC operates at a modulator frequency of 250 kHz with an f_{CLK} of 1 MHz. The full-scale voltage of the ADC is set by the voltage at the reference (V_{REF}). The reference can be either the LDO output (1.7 V) for the weight-scale front-end or the internally-generated reference signal (1.7 V) for the BCM front-end.

The decimation filter at the output of the modulator is a single-order sinc filter. The decimation rate can be programmed to provide data rates from 8 SPS to 860 SPS with an f_{CLK} of 1 MHz. Refer to the ADC_CONTROL_REGISTER1 register in the *Register Maps* section for details on programming the data rates. Figure 9 shows the frequency response of the digital filter for a data rate of 8 SPS. Note that the modulator has pass band around integer multiples of the modulator sampling frequency of 250 kSPS. Set the corner frequency of the antialiasing network before the INA so that there is adequate attenuation at the first multiple of the modulator frequency.

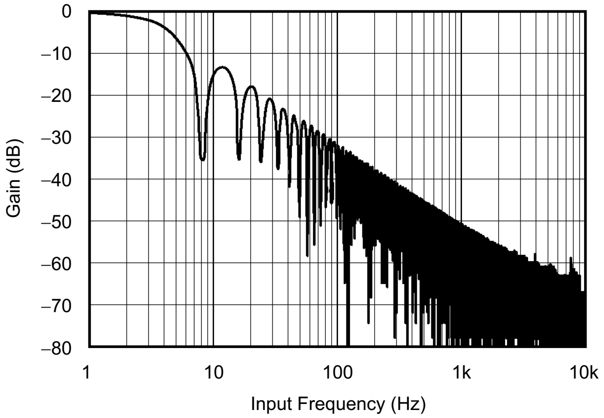


Figure 9. Frequency Response

The output format of the ADC is twos complement binary. Table 1 describes the output code versus the input signal, where full-scale (FS) is equal to the V_{REF} value.

Table 1. Input Signal Versus Ideal Output Code

INPUT SIGNAL, V_{IN} (AIN_P – AIN_N)	IDEAL OUTPUT CODE
≥ FS $(2^{15} – 1)/2^{15}$	7FFFh
$+FS/2^{15}$	0001h
0	0
$–FS/2^{15}$	FFFFh
≤ –FS	8000h

7.3.4 Reset and Power-Up

After power up, the device needs to be reset to get all the internal registers to their default state. Resetting the device is done by applying a zero pulse in the $\overline{\text{RST}}$ line for more than 20 ns after the power is stable for 5 ms. After 30 ns, the first access can be initiated (first falling edge of $\overline{\text{STE}}$). As part of the reset process, the AFE4300 sets all of the register bits to the respective default settings. Some of the register bits must be written after reset and power up for proper operation. Refer to the *Register Maps* section for more details. By default, the AFE4300 enters into a power-down state at start-up. The device interface and digital are active, but no conversion occurs until the ADC_PD bit is written to. The initial power-down state of the AFE4300 is intended to relieve systems with tight power-supply requirements from encountering a surge during power-up.

7.3.5 Duty Cycling for Low Power

For many applications, improved performance at low data rates may not be required. For these applications, the AFE4300 supports duty cycling that can yield significant power savings by periodically requesting high data-rate readings at an effectively lower data rate. For example, an AFE4300 in power-down mode with a data rate set to 860 SPS could be operated by a microcontroller that instructs a single-shot conversion every 125 ms (8 SPS). Because a conversion at 860 SPS only requires approximately 1.2 ms, the AFE4300 automatically enters power-down mode for the remaining 123.8 ms. In this configuration, the digitizer consumes about 1/100th the power of the digitizer when operated in Continuous-Conversion mode. The rate of duty cycling is completely arbitrary and is defined by the master controller.

7.4 Device Functional Modes

7.4.1 Operating Modes

The ADC operates in one of two conversion modes: Continuous-Conversion or Single-Shot conversion. The conversion mode is set using the ADC_CONV_MODE bit. In Continuous-Conversion mode, the ADC continuously performs conversions when the ADC_PD bit is set to 0. When a conversion completes, the ADC places the result in a register, issues an interrupt on the RDY pin, and immediately begins another conversion. In this mode, if ADC_PD is set to 1, then the ADC goes into a power-down state.

To get a Single-Shot conversion, the ADC_PD bit is to be first set to 1. When the ADC_CONV_MODE is subsequently set to 1, then the Single-Shot conversion is enabled. When enabled, the ADC does a single conversion and gives an interrupt on the RDY pin. To do one more Single-Shot conversion, the ADC_CONV_MODE bit must be set to 0 and then 1 again (with the ADC_PD bit at 1).

7.5 Programming

7.5.1 Serial Interface

The SPI™-compatible serial interface consists of either four signals ($\overline{\text{STE}}$, SCLK, SDIN, and SDOUT) or three signals (in which case, $\overline{\text{STE}}$ can be tied low). The interface is used to read conversion data, read from and write to registers, and control AFE4300 operation. The data packet (between falling and rising edge of $\overline{\text{STE}}$) is 24 bits long and is serially shifted into SDIN with the MSB first. The first eight bits (MSB) represent the address of the register being accessed and last 16 bits (LSB) represent the data to be stored or read from that address. For the eight bits address, the lower five bits [20:16] are the real address bits. Bit 21 is the read and write bit.

- '0' in bit 21 defines a write operation of the 16 data bits [15:0] into the register defined by the address bits [20:16].
- '1' in bit 21 triggers a read operation of the register defined by the address bits [20:16]. The data are output into SDOUT with every rising edge of SCLK, starting at the ninth rising edge. At the same time, data in SDIN are shifted inside the 16 data bits of that given register. Note that every time a register is read, the register must be rewritten except when reading the data output register.

7.5.1.1 SPI Enable ($\overline{\text{STE}}$)

The $\overline{\text{STE}}$ pin selects the AFE4300 for SPI communication. This feature is useful when multiple devices share the serial bus. $\overline{\text{STE}}$ must remain low for the duration of the serial communication. When $\overline{\text{STE}}$ is taken high, the serial interface is reset, and SCLK is ignored.

7.5.1.2 Serial Clock (SCLK)

The SCLK pin features a Schmitt-triggered input and is used to clock data on the DIN and $\overline{\text{RDY}}$ pins into and out of the AFE4300. Even though the input has hysteresis, SCLK is recommended to be kept as clean as possible to prevent glitches from accidentally shifting the data. When the serial interface is idle, hold SCLK low.

7.5.1.3 Data Input (SDIN)

The data input pin (SDIN) is used along with SCLK to send data to the AFE4300 (opcode commands and register data). The device latches data on SDIN on the falling edge of SCLK. The AFE4300 never drives the SDIN pin. Note that every time a register is read, the register must be rewritten, except when reading the data output register.

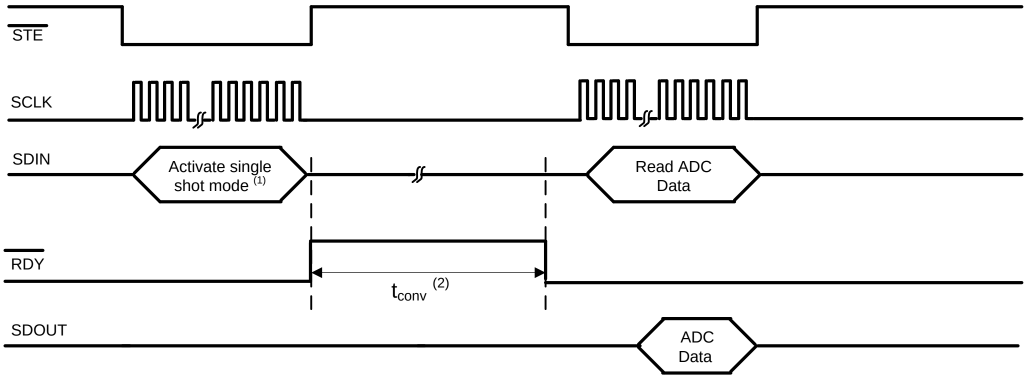
7.5.1.4 Data Output (SDOUT)

The data output and data ready pin ($\overline{\text{RDY}}$) are used with SCLK to read conversion and register data from the AFE4300. In Read Data Continuous mode, $\overline{\text{RDY}}$ goes low when conversion data are ready, and goes high 8 µs before the data ready signal. Data on $\overline{\text{RDY}}$ are shifted out on the rising edge of SCLK. If the AFE4300 does not share the serial bus with another device, $\overline{\text{STE}}$ may be tied low. Note that every time a register is read, the register must be rewritten, except when reading the data output register.

Programming (continued)

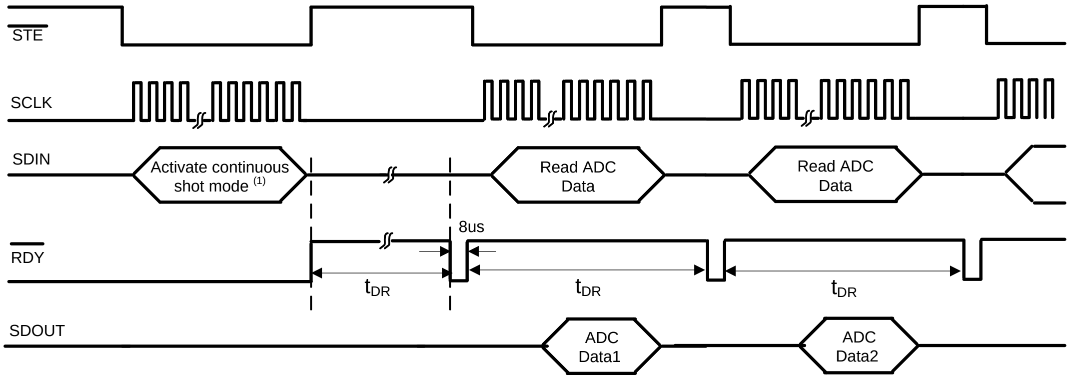
7.5.1.5 Data Ready (RDY)

RDY acts as a conversion ready pin in both Continous-Conversion mode and Single-Shot mode**.** When in Continuous-Conversion mode, the AFE4300 provides a brief (~8 μs) pulse on the RDY pin at the end of each conversion. In Single-Shot mode, the RDY pin asserts low at the end of a conversion. Figure 10 and Figure 11 show the timing diagram for these two modes.



Note 1 : Write ADC_CONTROL_REGISTER[7] = 1, ADC_CONTROL_REGISTER1[15] = 1,
Note 2 : t_{CONV} = Time to internally set ADC_CONTROL_REGISTER[15] to logic ‘0’, ADC power up, single conversion, ADC power down, ADC_CONTROL_REGISTER1[15] internally set to logic ‘1’

Figure 10. Timing for Single-Shot Mode



Note 1 : Write ADC_CONTROL_REGISTER[7] = 0

Figure 11. Timing for Continuous Mode

7.6 Register Maps

7.6.1 Register Map

Table 2 describes the registers of the AFE4300.

Table 2. Register Map

REGISTER NAME	CONTROL	ADDRESS	DESCRIPTION	DEFAULT
DEVICE CONTROLS				
DEVICE_CONTROL1	(See Description)	0x09[14:13]	Write '11' after power up and/or reset	00b
	DAC_PD	0x09[3]	Enable DAC for WS, BC measurements	0b
	PDB	0x09[2]	Chip power down	0b
	BCM_PDB	0x09[1]	Body composition measurement front-end power down	0b
	WS_PDB	0x09[0]	Weight-scale front-end power down	0b
DEVICE_CONTROL2	BAT_MON_EN1	0x0F[7]	Enables battery monitoring along with bit[0]	0b
	BAT_MON_EN2	0x0F[0]	Enables battery monitoring along with bit[7]	0b
ADC CONTROLS				
ADC_DATA_RESULT	(See Description)	0x00[15:0]	ADC data result, read only register	
ADC_CONTROL_REGISTER1	ADC_CONV_MODE	0x01[15]	Continuous-Conversion or Single-Shot mode	0b
	ADC_MEAS_MODE	0x01[13:11]	Single-Ended or Differential mode	000b
	ADC_PD	0x01[7]	ADC power down	1b
	ADC_DATA_RATE	0x01[6:4]	ADC data-rate control bits	100b
ADC_CONTROL_REGISTER2	ADC_REF_SEL	0x10[6:5]	Reference selection bits	00b
	PERIPHERAL_SEL	0x10[4:0]	Peripheral selection bits	00000b
WEIGHT-SCALE MODES				
DEVICE_CONTROL2	BRIDGE_SEL	0x0F[2:1]	Selects one of the four bridge inputs	00b
WEIGHT_SCALE_CONTROL	WS_PGA_GAIN	0x0D[14:13]	PGA gain of weight-scale front-end	00b
	OFFSET_DAC_VALUE	0x0D[5:0]	Offset DAC setting for weight-scale front-end	000000b
BCM CONTROLS				
ISW_MUX	ISW_MUXP	0x0A[15:8]	Control for switches IOUTP and RP	0x00
	ISW_MUXM	0x0A[7:0]	Control for switches IOUTN and RN	0x00
VSENSE_MUX	VSENSE_MUXP	0x0B[15:8]	Control for switches VSENSEP and VSENSEP_R	0x00
	VSENSE_MUXM	0x0B[7:0]	Control for switches VSENSEN and VSENSN_R	0x00
BCM_DAC_FREQ	DAC_FREQ	0x0E[9:0]	Sets the frequency of BCM excitation current source	0x00
IQ_MODE_ENABLE	IQ_MODE_ENABLE	0x0C[11]	Enable IQ demodulator	0b
DEVICE_CONTROL2	IQ_DEMOD_CLK_DIV_FAC	0x0F[13:11]	IQ Demodulator clock frequency	000b
MISCELLANEOUS REGISTERS				
MISC_REGISTER1	(See Description)	0x02[15:0]	Write 0x0000 after power up and/or reset	0x8000
MISC_REGISTER2	(See Description)	0x03[15:0]	Write 0xFFFF after power up and/or reset	0x7FFF
MISC_REGISTER3	(See Description)	0x1A[15:0]	Write 0x0030 after power up and/or reset	0x0000

7.6.1.1 ADC_DATA_RESULT (Address 0x00, Default 0x0000)

This register stores the most recent conversion data in twos complement format with the MSB in bit 15 and the LSB in bit 0.

7.6.1.2 ADC_CONTROL_REGISTER1 (Address 0x01, Default 0x01C3)

This register is used in conjunction with ADC_PD (bit 7). Refer to the description of the ADC_PD bit for more details.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADC_CONV_MODE	1	ADC_MEAS_MODE			0	0	1	ADC_PD	ADC_DATA _RATE			0	0	0	0

Bit 15 **ADC_CONV_MODE:** ADC conversion mode/ADC single-shot conversion start.

This bit determines the operational status of the device. This bit can only be written when in the ADC power-down mode. When read, this bit gives the status report of the conversion.

For a write status:
0 : No effect (default)
1 : Single-shot conversion mode

For a read status:
0 : Device currently performing a conversion
1 : Device not currently performing a conversion

Bit 14 **Always write '1'.**

Bits[13:11] **ADC_MEAS_MODE:** ADC measurement mode selection.

These bits set the ADC measurements to be either single-ended or differential.

ADC_MEAS_MODE	ADC AINP, AINM
000 (default)	A1, A2 = differential (default)
001	A1, AVSS = single-ended
010	A2, AVSS = single-ended

Bits[10:8] Always write '001'

Bit 7 **ADC_PD:** ADC Powerdown

This bit powers down the ADC_PGA and the ADC. By default, the ADC is powered down (ADC_PDN = '1').
For continuous conversion mode, this bit must to set to '0'.
For single-shot mode, this bit must be set to '1' along with bit 15. During single-shot conversion mode, the device automatically powers up the ADC, triggers one ADC conversion, and then powers down the ADC.

ADC_CONV_MODE (Bit 15)	ADC_PDN (Bit 7)	MODE
X	**0**	**Continuous conversion**
0	**1 (default)**	**ADC PD**
1	**1 (default)**	**Single-shot**

Bits[6:4] **ADC_DATA_RATE:** Conversion rate select bits.

These bits select one of eight different ADC conversion rates. The data rates shown assume a master clock of 1 MHz.

000: 8 SPS
001: 16 SPS
010: 32 SPS
011: 64 SPS
100: 128 SPS (default)
101: 250 SPS
110: 475 SPS
111: 860 SPS

Bits[3:0] **Always write '0000'.** At power up, these bits are set as '0011'.

7.6.1.3 MISC_REGISTER1 (Address 0x02, Default 0x8000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit 15	**Always write ‘0’.** At power up, this bit is set as '1'.
Bits[14:0]	**Not used, always write ‘0’.** At power up, these bits are set as '0'.

7.6.1.4 MISC_REGISTER2 (Address 0x03, Default 0x7FFF)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit 15	**Always write ‘1’.** At power up, this bit is set as '0'.
Bits[14:0]	**Always write ‘1’.** At power up, these bits are set as '1'.

7.6.1.5 DEVICE_CONTROL1 (Address 0x09, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	0	0	0	0	0	DAC_PD	PDB	BCM_PDB	WS_PDB

Bits[15]	**Not used. Always write '0'.**
Bits[14:13]	**Not used. Always write '1'.**
Bits[12:4]	**Not used. Always write '0'.**
Bit 3	**DAC_PDB:** Power down DAC. This bit powers down the weight-scale front-end offset correction DAC and the BCM front-end current source DAC. 0: Power up DAC (default) 1: Power down DAC
Bit 2	**PDB**: Power down device. This bit in conjunction with the other power-down bits determines the power state of the device. 0: Power down (default) 1: Power up of front-end
Bit 1	**BCM_PDB:** Body composition measurement front-end power-down bit. 0: Power down body compositionmeasurement front-end (default) 1: Power up body composition measurement front-end. Power down the weight scale when powering up the BCM.
Bit 0	**WS_PDB:** Weight-scale front-end power-down bit. 0: Power down weight-scale front-end (default) 1: Power up weight-scale front-end. Power down BCM when powering up the weight scale.

Table 3 shows the available power-down modes.

Table 3. Power-Down Modes

DAC_PDB (Bit3)	PDB (Bit 2)	BCM_PDB (Bit 1)	WS_PDB (Bit 0)	ADC_PD (Bit 7, ADC Control Register)	MODE
X	0	0	0	1	Full device power down
1	1	0	0	1	Sleep mode
0	1	1	0	0	Weight-scale power down, body composition measurement
0	1	0	1	0	Body composition measurement power down, weight-scale measurement
0	1	0	0	0	Weight-scale and body composition measurement power down (aux/battery measurement)

7.6.1.6 ISW_MUX (Address 0x0A, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOUTP5	IOUTP4	IOUTP3	IOUTP2	IOUTP1	IOUTP0	RP1	RP0	IOUTN5	IOUTN4	IOUTN3	IOUTN2	IOUTN1	IOUTN0	RN1	RN0

Bits[15:10]	**IOUTP[5:0]** These bits close the switches routing IOUTPx to the output of OPAMP1. 0: Switch is open (default) 1: Switch is closed
Bits[9:8]	**RP[1:0]** These bits close the switches routing the calibration signal to the output of OPAMP1. 0: Switch is open (default) 1: Switch is closed
Bits[7:2]	**IOUTN[5:0]** These bits close the switches routing IOUTNx to the negative input of OPAMP1. 0: Switch is open (default) 1: Switch is closed
Bits[1:0]	**RN[1:0]** These bits close the switches routing the calibration signal to the negative input of OPAMP1. 0: Switch is open (default) 1: Switch is closed

7.6.1.7 VSENSE_MUX (Address 0x0B, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSENSEP5	VSENSEP4	VSENSEP3	VSENSEP2	VSENSEP1	VSENSEP0	VSENSEP_R1	VSENSEP_R0	VSENSEN5	VSENSEN4	VSENSEN3	VSENSEN2	VSENSEN1	VSENSEN0	VSENSEM_R1	VSENSEM_R0

Bits[15:10]	**VSENSEPx[5:0]** These bits close the switches routing VSENSEPx to the positive input of the receive amplifier. 0: Switch is open (default) 1: Switch is closed
Bits[9:8]	**VSENSEP_Rx[1:0]** These bits close the switches routing the calibration signal to the positive input of the receive amplifier. 0: Switch is open (default) 1: Switch is closed
Bits[7:2]	**VSENSENx[5:0]** These bits close the switches routing VSENSENx to the negative input of the receive amplifier. 0: Switch is open (default) 1: Switch is closed
Bits[1:0]	**VSENSEM_Rx[1:0]** These bits close the switches routing the calibration signal to the negative input of the receive amplifier. 0: Switch is open (default) 1: Switch is closed

7.6.1.8 IQ_MODE_ENABLE (Address 0x0C, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	IQ_MODE_ ENABLE	0	0	0	0	0	0	0	0	0	0	0

Bits[15:12] **Not used. Always write '0'.**

Bit 11 **IQ_MODE_ENABLE:** Enable the I/Q demodulator.

This bit sets the impedece measurement mode to either full-wave rectifier mode or I/Q demodulator mode. For I/Q Demodulator mode, the DAC_FREQ bits of the BCM_DAC_FREQ register and the IQ_DEMOD_CLK_DIV_FAC bits of the DEVICE_CONTROL2 register must be set appropriately. Refer to the respective register section for more details.

0: Full-Wave Rectifier mode (default)
1: I/Q Demodulator mode

Bits[10:0] **Not used. Always write '0'.**

7.6.1.9 WEIGHT_SCALE_CONTROL (Address 0x0D, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	WS_PGA_ GAIN		0	0	0	0	0	0	0	OFFSET_DAC_VALUE					

Bit 15 **Not used. Always write '0'.**

Bits[14:13] **WS_PGA_GAIN:** Sets the second-stage gain of the weight-scale front-end.

00: Gain = 1 (default)
01: Gain = 2
10: Gain = 3
11: Gain = 4

Bits[12:6] **Not used. Always write '0'.**

Bit[5:0] **OFFSET_DAC_VALUE:** Offset correction DAC setting.

These bits set the value for the DAC used to correct the input offset of the weight-scale front-end. The correction is made at the second stage. The offset correction at the output of the first stage is given by OFFSET_DAC_VALUE × 31.2 mV. Note that OFFSET_DAC_VALUE is a number from –32 to 31, in twos complement; default is '000000'.

7.6.1.10 BCM_DAC_FREQ (Address 0x0E, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	DAC9	DAC8	DAC7	DAC6	DAC5	DAC4	DAC3	DAC2	DAC1	DAC0

Bits[15:910] **Not used. Always write '0'.**

Bits[9:0] **DAC[9:0]:** Sets the frequency of the BCM excitation current source.

The DAC output frequency is given by DAC[9:0] × f_{CLK} / 1024, where f_{CLK} is the frequency of the device input clock (pin 79). All combinations of the DAC frequency can be used for the full-wave rectifier mode. However, only certain combinations of the DAC frequency can be used for the IQ demodulator mode. Refer to the description of the DEVICE_CONTROL2 register for more details.

For example, with f_{CLK} = 1.024 MHz:
DAC = 0x00FF → 255 kHz
DAC = 0x0001 → 1 kHz

7.6.1.11 DEVICE_CONTROL2 (Address 0x0F, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	IQ_DEMOD_CLK_DIV_FAC			0	0	0	BAT_MON_EN1	0	0	0	0	BRIDGE_SEL		BAT_MON_EN0

Bits[15:14]	**Not used. Always write '0'.**
Bits[13:11]	**IQ_DEMOD_CLK_DIV_FAC:** I/Q demodulator clock frequency. The clock for the IQ demodulator (IQ_DEMOD_CLK signal) is internally generated from the device input clock (f_{CLK}) by a divider controlled by this register. Note that the IQ_DEMOD_CLK must be four times the BCM_DAC_FREQ so that the phases for the mixers can be generated (that is, IQ_DEMOD_CLK = f_{CLK} / (IQ_DEMOD_CLK_DIV_FAC) = BCM_DAC_FREQ × 4) 000: Divide by 1 (default) 001: Divide by 2 010: Divide by 4 011: Divide by 8 100: Divide by 16 Others: Divide by 32
Bit 7	**BAT_MON_EN1:** This bit (along with BAT_MON_EN0, bit 0) enables battery monitoring. When disabled, the battery monitoring block is powered down to save power. See the description of BAT_MON_EN0, bit 0.
Bits[6:3]	**Not used. Always write '0'.**
Bits[2:1]	**BRIDGE_SEL:** Selects one of the four input pairs to be routed to the weight-scale front-end. 00: Bridge 1 (INP1, INM1) connected to the weight-scale front-end (default) 01: Bridge 2 (INP2, INM2) connected to the weight-scale front-end 10: Bridge 3 (INP3, INM3) connected to the weight-scale front-end 11: Bridge 4 (INP4, INM4) connected to the weight-scale front-end.
Bit 0	**BAT_MON_EN0:** This bit along with BAT_MON_EN1 (Bit[7]) enables battery monitoring. 00: Monitor disabled (default) 11: Monitor enabled (AVDD / 3) **NOTE:** The PERIPHERAL_SEL bits of the ADC_CONTROL_REGISTER2 must be set to '10001' in order to route the battey monitor output to the ADC.

7.6.1.12 ADC_CONTROL_REGISTER2 (Address 0x10, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	ADC_REF_SEL		PERIPHERAL_SEL				

Bits[15:7]	**Not used. Always write '0'.**
Bits[6:5]	**ADC_REF_SEL[1:0]:** Selects the reference for the ADC. 00: ADCREF connected to VLDO. Used for ratiometric weight-scale measurement (default). 01, 10: Do not use 11: ADCREF connected to VREF (internal voltage reference generator). Used for impedance measurement.
Bits[4:0]	**PERIPHERAL_SEL[4:0]:** Selects the signals that are connected to the ADC. 00000: Output of the weight-scale front-end (default) 00011: Output of the body composition measurement front-end (OUTP_FILT/OUTM_FILT) 00101: Output of the body composition measurement front-end (OUTP_Q_FILT/OUTM_Q_FILT) 01001: AUX1 signal for single-ended measurement. Also set bit[13:11] of the ADC_CONTROL_REGISTER1 to '001'. 10001: AUX2 signal for single-ended measurement. Also set bit[13:11] of the ADC_CONTROL_REGISTER1 to '010'. 11001: AUX2 and AUX1 signal for differential measurement (AUX2-AUX1). Also set bit[13:11] of the ADC_CONTROL_REGISTER1 to 000. **NOTE:** All other bit combinations are invalid.

7.6.1.13 MISC_REGISTER3 (Address 0x1A, Default 0x0000)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0

Bits[15:6]	**Not used. Always write '0'.**
Bits[5:4]	**Always write '1'.**
Bits[3:0]	**Not used. Always write '0'.**

8 Application and Implementation

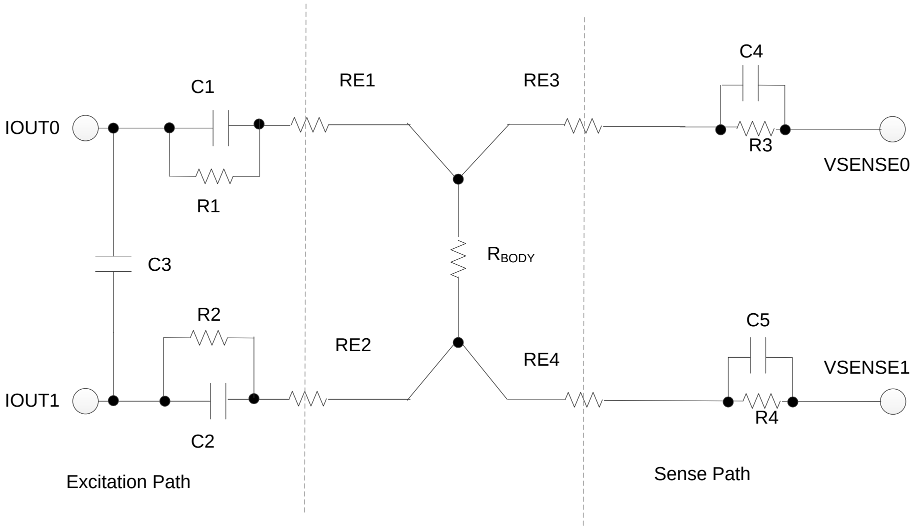
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 BCM Channel Connections

The suggested connections of the BCM excitation and sense electrodes to the device pins are shown in Figure 12. The circuit shows an electrical model of the body impedance being measured (R_{BODY}) along with models for the electrode contact impedances. The components connecting the electrodes to the IOUTx and VSENSEx pins are meant to be replicated in the path of the calibration impedances as well. Suggestions for the component values are shown in Table 4.



RE1, RE2, RE3, and RE4 model the electrode contact impedance.

R_{BODY} models the body impedance (replaced by the calibration resistance in the calibration path).

Figure 12. Connection of BCM Pins to Electrodes

Table 4. Component Values Corresponding to Figure 12[(1)]

COMPONENT	ILLUSTRATIVE VALUE	COMMENTS
R1, R2	10 kΩ	Provides a dc feedback for the excitation op amp.
C1, C2	1 µF	Low-impedance path for the 50-kHz excitation, high impedance for dc currents.
C3	47 pF	Optional shunt capacitor across the excitation op amp to improve stability.
R3, R4	10 kΩ	Sets the dc voltage at the VSENSEx pins.
C4, C5	1 µF	Low-impedance path for the 50-kHz excitation, high impedance for dc currents (patient safety).

(1) The indicated component values are only for illustration. The actual choice of circuit configuration and component values in a product can be governed by other considerations (such as patient safety and so forth).

8.1.2 Handling Oscillation of the Excitation Amplifier

The phase margin of the excitation amplifier can degrade if there is high capacitance at the input and output terminals. High capacitances can result can result from the capacitances from the electrodes, from protection diodes (for instance, ESD diodes), as well as the capacitance presented by the human body. Degradation of phase margin resulting from high capacitances can result in oscillations leading to reduced measurement accuracy. One way to improve the phase margin of the excitation amplifier is to introduce a series R-C at the output of the excitation amplifier in every measurement. This process is done using the components R_{CM} = 1 kΩ and C_{CM} = 1 nF in the simplistic model shown in Figure 13. This illustration is for a case where IOUT0 and IOUT1 are switched to the input and output of the excitation amplifier, respectively.

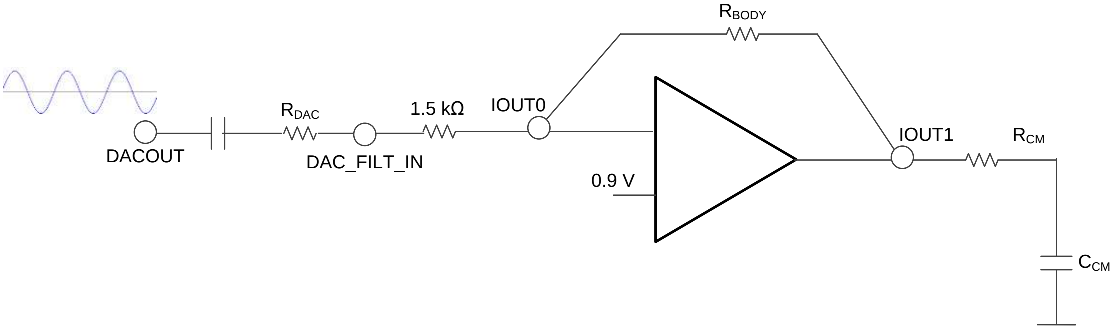


Figure 13. Oscillation Fix of the Excitation Amplifier

Such a scheme can be implemented in one of two methods:

1. A separate R_{CM}-C_{CM} for every IOUTx and RPx pin that gets switched to the excitation amplifier output.
2. A single R_{CM}-C_{CM} on one of the RPx pins that gets switched to the excitation amplifier output during calibration. When not using this RPx pin, still switch the same RPx pin to the output of the excitation amplifier (in addition to whichever other pin is switched to the output) so that the R_{CM}-C_{CM} still gets connected to the output of the excitation amplifier.

Method 2 is preferable because this method involves only one R_{CM} and one C_{CM}.

8.1.3 Achieving Deterministic Phase in the IQ Mode

The DAC frequency generator (DDS) is initialized on the register update of the DAC frequency register. The IQ demod clock divider is updated on the divider register value. Because the registers are written through the SPI interface (that is, asynchronous to the device clock), every time either of these registers are written, the phase relation between the DAC output and the I-Q demod clock can get altered. This alteration in phase relation can cause the phase of the I-Q measurement to be non-deterministic.

Two ways of circumventing this issue are:

1. Do a fresh calibration (measuring all the calibration impedances) each time the registers are reprogrammed for a new excitation frequency
2. Use an SPI clock synchronous with the device clock and follow the sequence below whenever the DACOUT frequency is to be changed:
   1. Write 0 to register 15 (set the IQ divider to 1)
   2. Write 0 to register 14 (DACOUT frequency is cleared)
   3. Write the required DAC frequency to register 14
   4. Write the required IQ_DEMOD_CLK_DIV to register 15

8.2 Typical Application

A typical application of the AFE4300 is a weight scale, as shown in Figure 14, that includes a weight measurement as well as a body impedance measurement with the architecture.

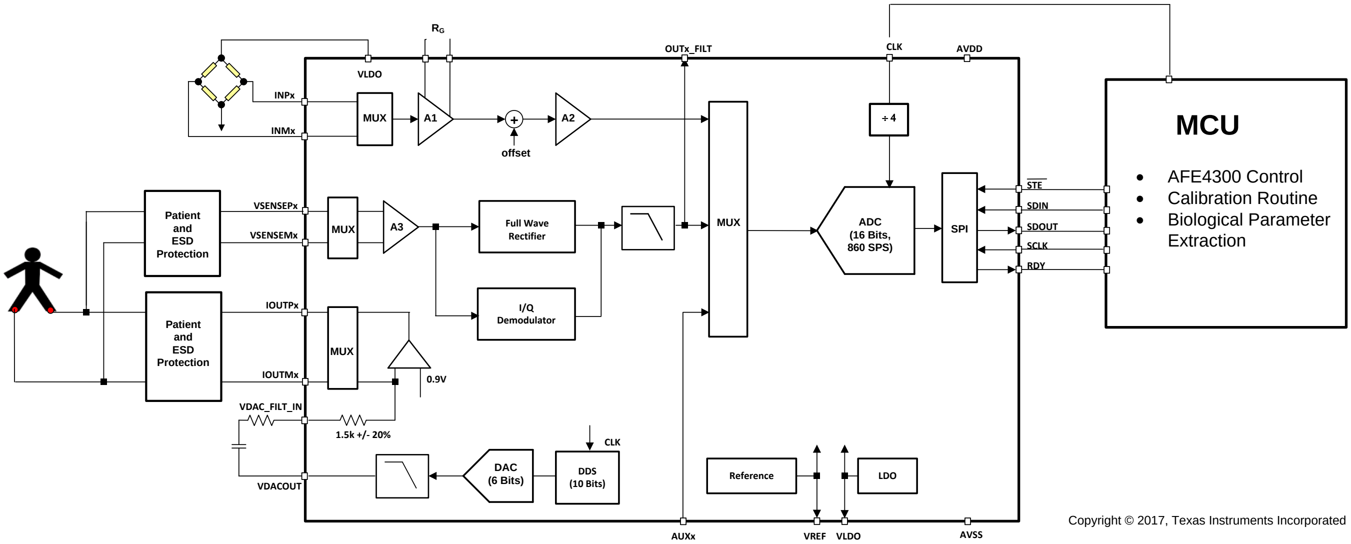


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Figure 14. Weight Scale Application

The weight applied on a load-cell generates the differential voltage that is converted by the weight scale signal chain of the AFE. For the body impedance measurement, a sinusoidal current (most commonly at a frequency of 50 kHz) is injected into a pair of electrodes that make contact with the human body. Two more electrodes serve as sense electrodes and the differential voltage developed across the sense electrodes is measured and digitized by the AFE. The whole system is clocked using an external clock source.

8.2.1 Design Requirements

Table 5 shows the typical requirements of a weight scale design using the AFE.

Table 5. Weight Scale Design Requirements

PARAMETER	EXAMPLE VALUE	COMMENTS
AVDD	3.3 V	Have enough margin for the dc inaccuracy and minimize ripple. For the battery-operated device, an LDO can be used to derive AVDD. Place decoupling capacitors close to the AFE.
Load-cell excitation voltage	1.7 V	V_{LDO} is generated by the AFE and must be used as the load-cell excitation source. Because V_{LDO} is used as the reference for the ADC in the weight scale signal chain, using V_{LDO} as the excitation voltage for the load-cell makes the measurement ratio-metric and compensates errors resulting from variation in V_{LDO}.
External clock frequency	1.024 MHz	—
BCM excitation frequency	50 kHz (set by programming the AFE)	For single-frequency body impedance analysis, the most commonly used frequency is 50 kHz.
Skin-electrode contact impedance	A few 100 Ω or lower	The electrodes must have a big enough contact area with the body in order to minimize the electrode-skin contact impedance (ac value at the excitation frequency).

8.2.2 Detailed Design Procedure

A body impedance measurement is usually performed using four electrodes: a pair of excitation electrodes and a pair of sense electrodes. Body contact to each electrode involves a series impedance resulting from the skin-electrode interface. On the excitation side, this contact impedances come in series with the body impedance and cause the voltage swing on the excitation terminals of the AFE to increase. Excessive contact impedances on the excitation electrodes can therefore cause the excitation amplifier to saturate even while measuring normal ranges of body impedance. On the sense electrodes, the input impedance of the receiver is 50 kΩ. As a result, the contact impedances on the sense electrodes cause a small attenuation in the effective signal input to the receiver. For these reasons, the ac contact impedance at the excitation frequency must be minimized on both the excitation and sense electrodes.

To deduce an accurate impedance value from the AFE output in the body impedance measurement requires calibration relative to known impedances. Calibration is usually performed by measuring two or more known impedances and by constructing a piece-wise linear curve between the AFE output and the impedance.

To conserve power when not used, the AFE can be put in a sleep mode in which all signal chains are powered down. This mode reduces the average power consumption significantly. When the user issues a power-up interrupt (pressing a button or so forth) to the system, the AFE can be programmed to come out of sleep mode, perform the measurement, and go back to sleep again. To account for drifts with time, TI recommends that calibration be done every time the AFE is woken up. For the BCM measurement, TI recommends measuring the calibration impedances before every fresh measurement of body impedance. For the weight scale measurement, TI recommends measuring the channel offset (the AFE output without any load) before the measurement of the load. Also after every wake-up, provide sufficient time for the signal chain to settle before doing any measurements.

To meet product-level ESD requirements, additional external ESD protection diodes may need to be used to protect the AFE pins that interface with the electrodes.

8.2.3 Application Curve

Figure 15 shows the linearity of the BCM up to 2.5 kΩ. As seen the figure, the maximum impedance that can be measured for the default configuration using the AFE4300 is typically 2.5 kΩ. However for better performance, TI suggests limiting the impedance to 1175 Ω. If higher impedance must be measured, the excitation current can be reduced by placing an external resistor of 1.5 kΩ (between DACOUT and DAC_FILT_IN), which increases the range by roughly 2x.

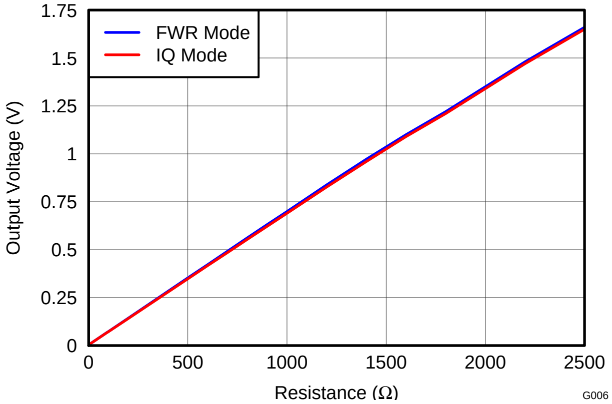

Figure 15. Body Impedance to Output Voltage Transfer Curve

9 Power Supply Recommendations

9.1 Power-Supply Recommendation and Initialization

The device has an analog supply (AVDD). Drive these pins with a clean supply and connect bypass capacitors close to the pins. After power up, the device must be reset to set all internal registers to their default state. Resetting the device is done by applying an active low pulse on the $\overline{\text{RST}}$ pin after the power supplies stabilize. As part of the reset process, the AFE4300 sets all register bits to the respective default settings.

Some register bits must be written to values different from their default values after reset for proper operation. By default, the AFE4300 enters into a power-down state at start-up. The startup and initialization for the device is shown in Figure 16 and Table 6 lists the recommended timing values.

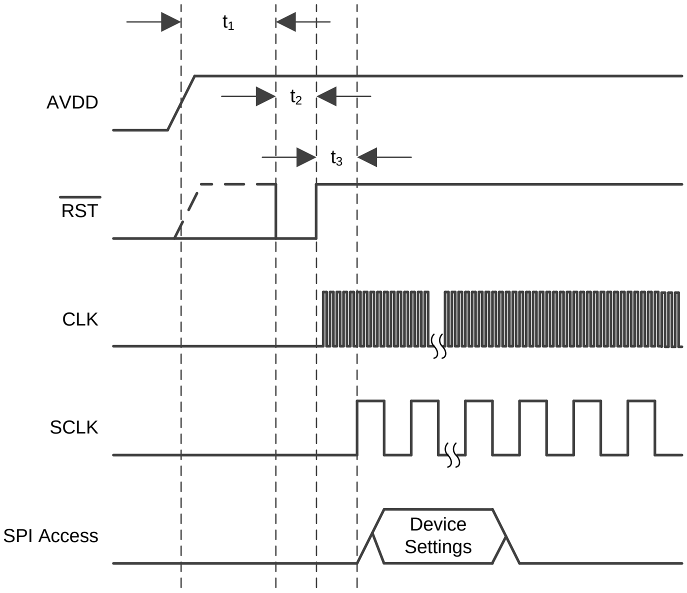

Figure 16. Power-Up and Initialization

Table 6. Timing Parameters for Figure 16

		NOM	UNIT
t_1	Time between supplies turning on and an active $\overline{\text{RST}}$	> 10	ms
t_2	Active $\overline{\text{RST}}$ duration	> 50	µs
t_3	Time between $\overline{\text{RST}}$ and register writes	> 1	ms

10 Layout

10.1 Layout Guidelines

The following points must be considered during layout:

- All input signals (INPx, INMx, VSENSEx, IOUTs) must be routed differentially with equal length
- Input signals must be isolated from high-frequency signals using a ground plane or a ground trace
- Special care (such as avoiding vias, test points, and so forth) must be given to minimize the parasitic capacitances in the input circuit of the BCM

10.2 Layout Example

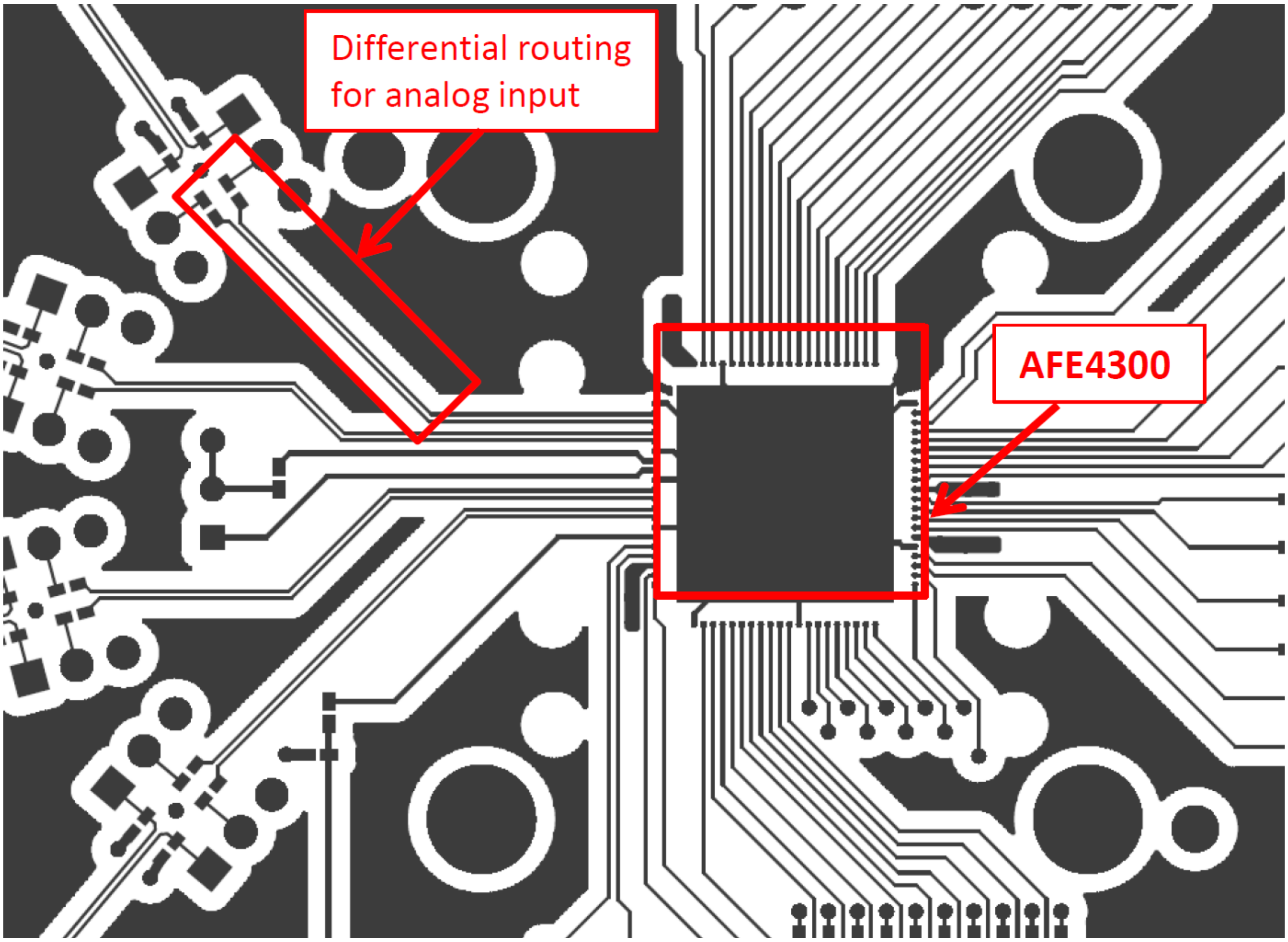

Figure 17. Example Layout

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.3 商標

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11.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE4300PN	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	AFE4300	Samples
AFE4300PNR	ACTIVE	LQFP	PN	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	AFE4300	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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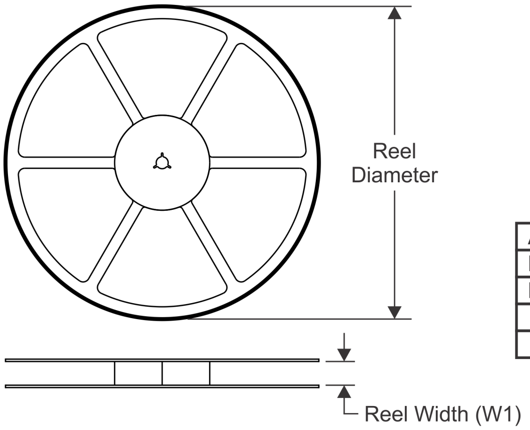
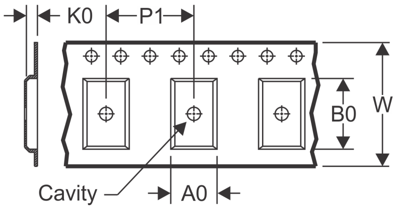
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

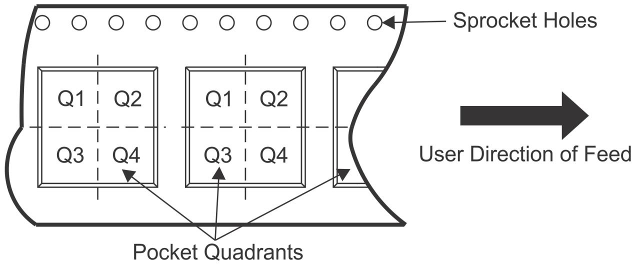


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

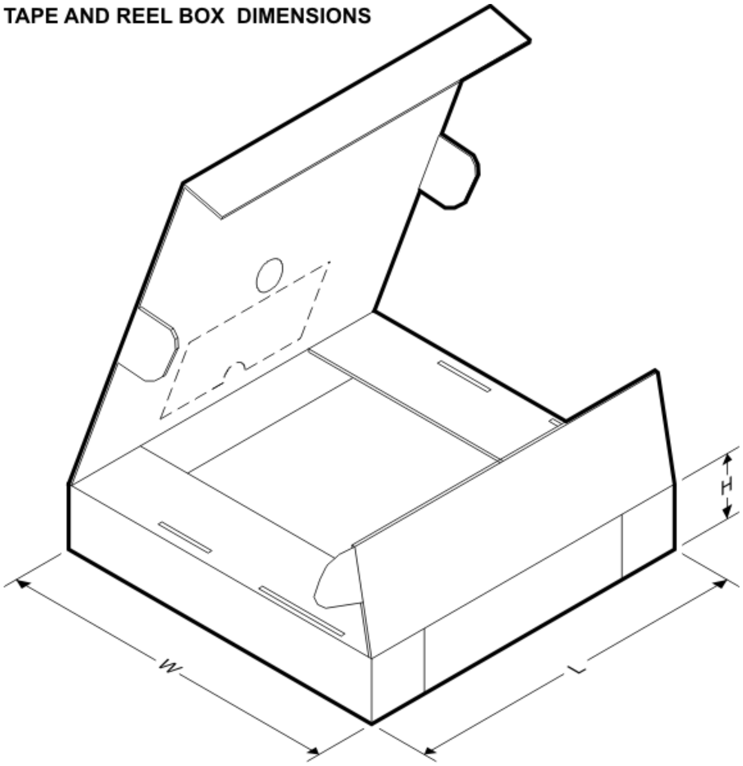
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE4300PNR	LQFP	PN	80	1000	330.0	24.4	16.0	16.0	2.0	24.0	24.0	Q2

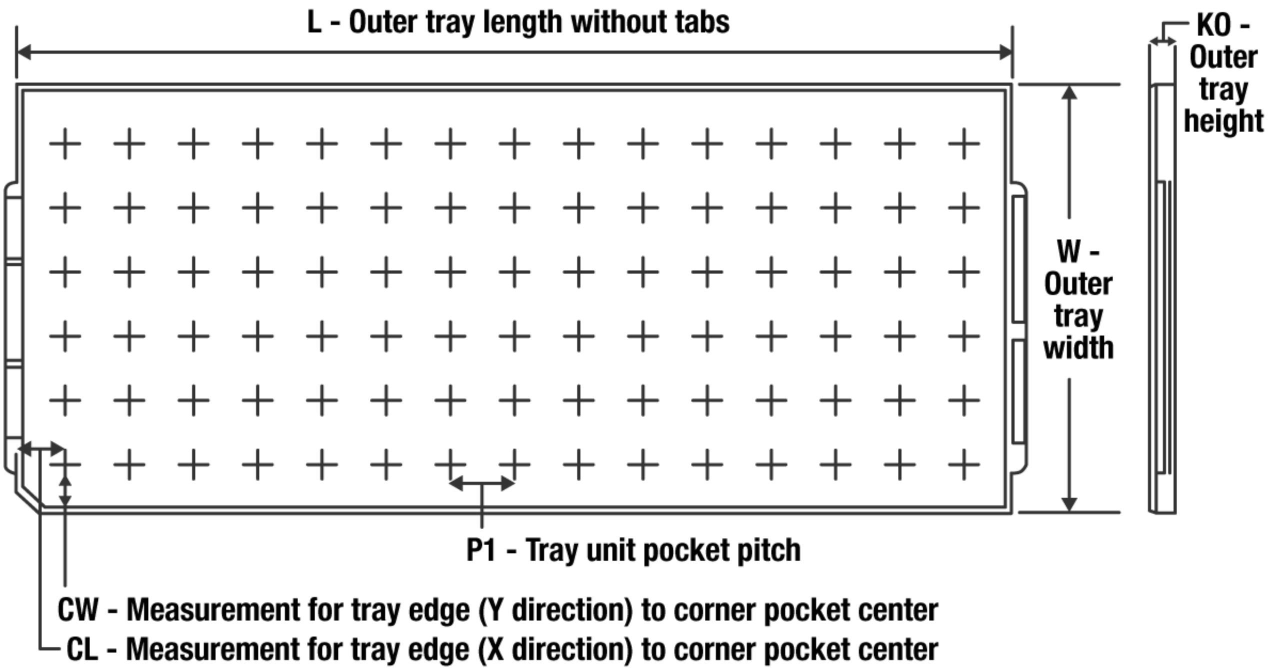
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE4300PNR	LQFP	PN	80	1000	367.0	367.0	55.0

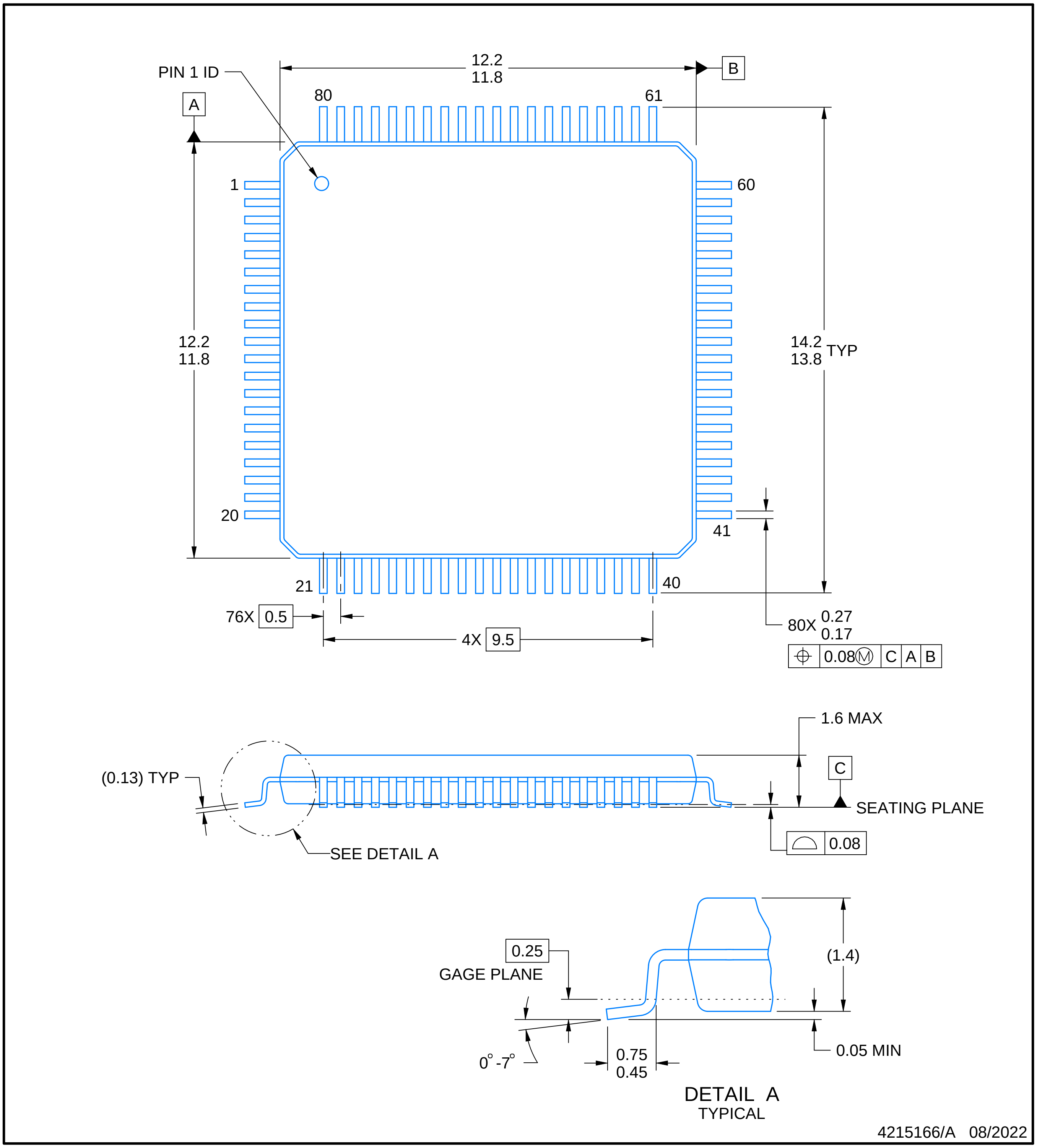
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

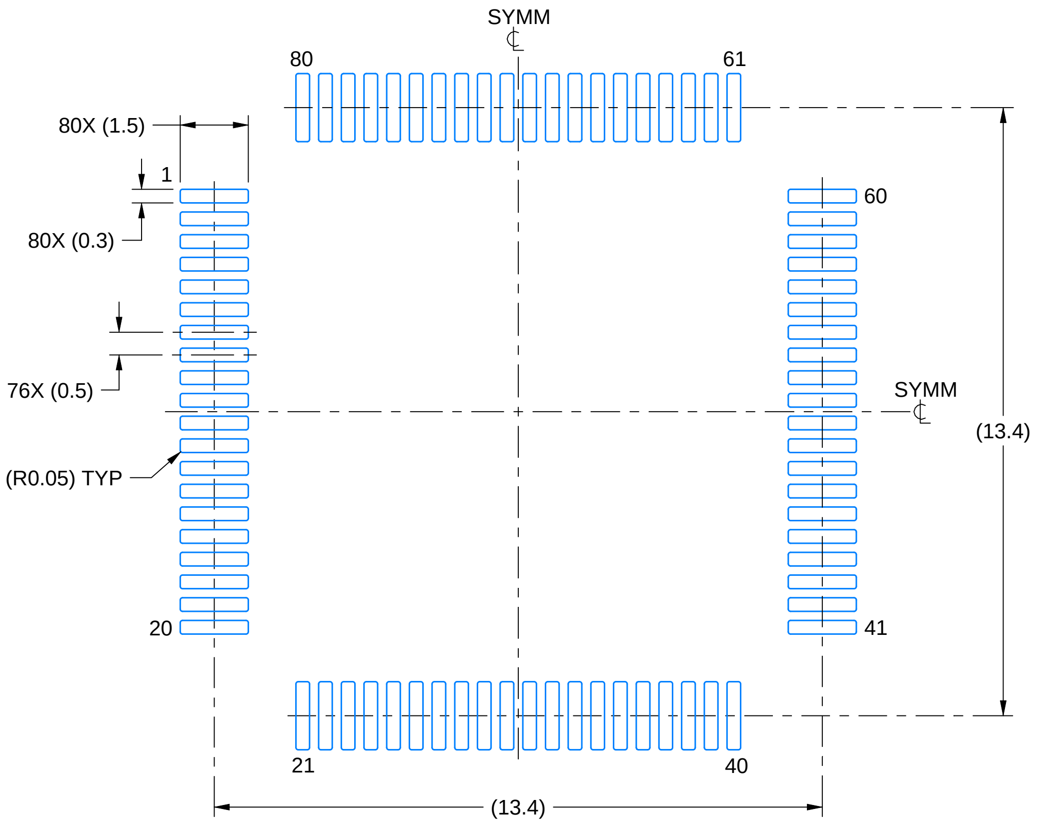
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE4300PN	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95



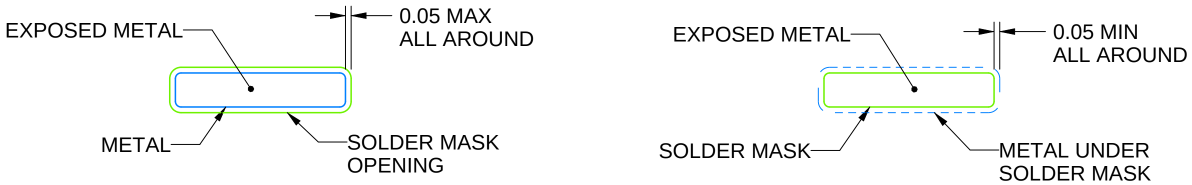
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



NON SOLDER MASK DEFINED

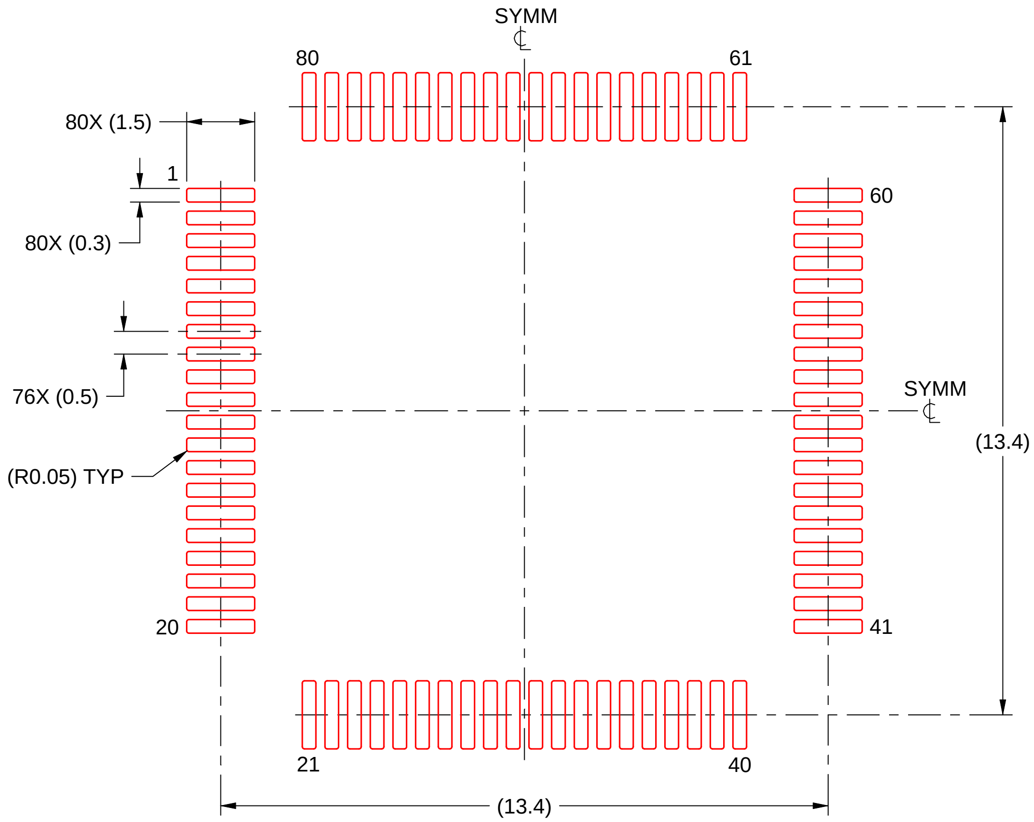
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4215166/A 08/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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