

# LMT85 1.8V、SC70/TO-92/TO-92S、 アナログ温度センサ

## 1 特長

- LMT85LPG (TO-92Sパッケージ)は高速な熱時定数、標準値10s (エアフロー1.2m/s)
- 非常に正確:  $\pm 0.4^{\circ}\text{C}$  (標準値)
- 低電圧1.8Vでの動作
- 平均センサ・ゲイン:  $-8.2\text{mV}/^{\circ}\text{C}$
- 低い静止電流:  $5.4\mu\text{A}$
- 広い温度範囲:  $-50^{\circ}\text{C}\sim 150^{\circ}\text{C}$
- 出力の短絡保護
- 駆動能力 $\pm 50\mu\text{A}$ のプッシュプル出力
- 業界標準のLM20/19およびLM35温度センサとフットプリント互換
- コスト効率に優れたサーミスタの代替

## 2 アプリケーション

- 車載用
- インフォテインメントおよびクラスA
- パワートレイン・システム
- 煙および熱感知器
- ドローン
- 家電製品

## 3 概要

LMT85は高精度のCMOS温度センサで、標準精度は $\pm 0.4^{\circ}\text{C}$  (最大値 $\pm 2.7^{\circ}\text{C}$ )で、リニアなアナログ出力電圧を持ち、この電圧は温度に反比例します。1.8Vの電源電圧で動作し、静止電流が $5.4\mu\text{A}$ 、パワーオン時間が $0.7\text{ms}$ で、効果的なパワーサイクリング・アーキテクチャを実現し、ドローンやセンサ・ノードなどバッテリー駆動のアプリケーションで消費電力を最小化できます。LMT85LPGスルーホールTO-92Sパッケージは熱時定数が高速で、煙および熱感知器など、オフボードで時間-温度の感度が高いアプリケーションに対応できます。広い動作範囲にわたる精度や、その他の特長から、LMT85はサーミスタの優れた代替となります。

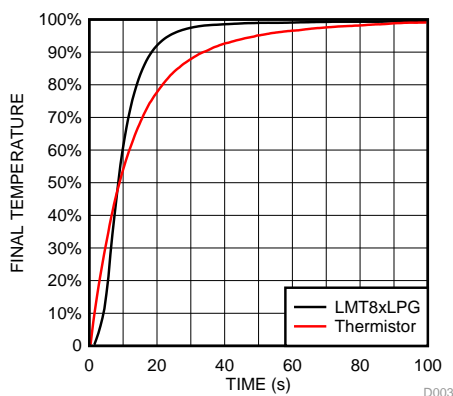
異なる平均センサ・ゲインおよび類似の精度を持つデバイスについては、「[類似の代替デバイス](#)」で、LMT8xファミリの他のデバイスを参照してください。

### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
LMT85	SOT (5)	2.00mm×1.25mm
	TO-92 (3)	4.30mm×3.50mm
	TO-92S (3)	4.00mm×3.15mm

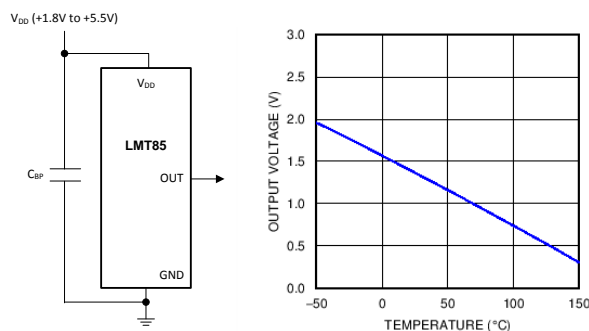
(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### 熱時定数



\* 高速な熱応答NTC

### 出力電圧と温度との関係



Copyright © 2016, Texas Instruments Incorporated



## 目次

1	特長	1	8.3	Feature Description	9
2	アプリケーション	1	8.4	Device Functional Modes	11
3	概要	1	<b>9</b>	<b>Application and Implementation</b>	<b>13</b>
4	改訂履歴	2	9.1	Application Information	13
5	Device Comparison Tables	3	9.2	Typical Applications	13
6	Pin Configuration and Functions	4	<b>10</b>	<b>Power Supply Recommendations</b>	<b>14</b>
7	Specifications	5	<b>11</b>	<b>Layout</b>	<b>15</b>
7.1	Absolute Maximum Ratings	5	11.1	Layout Guidelines	15
7.2	ESD Ratings	5	11.2	Layout Example	15
7.3	Recommended Operating Conditions	5	<b>12</b>	<b>デバイスおよびドキュメントのサポート</b>	<b>16</b>
7.4	Thermal Information	5	12.1	ドキュメントの更新通知を受け取る方法	16
7.5	Accuracy Characteristics	6	12.2	コミュニティ・リソース	16
7.6	Electrical Characteristics	6	12.3	商標	16
7.7	Typical Characteristics	7	12.4	静電気放電に関する注意事項	16
<b>8</b>	<b>Detailed Description</b>	<b>9</b>	12.5	Glossary	16
8.1	Overview	9	<b>13</b>	<b>メカニカル、パッケージ、および注文情報</b>	<b>16</b>
8.2	Functional Block Diagram	9			

## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (June 2017) から Revision E に変更	Page
• 車載用デバイスを単独のデータシート(SNIS200)に移動	1
• Changed TO-92 GND pin number from: 1 to: 3	4
• Changed TO-92 V <sub>DD</sub> pin number from: 3 to: 1	4

Revision C (October 2015) から Revision D に変更	Page
• データシートのテキストを最新のドキュメントおよび翻訳標準に更新	1
• 「特長」の箇条書きにAEC-Q100車載用認定の項目を追加	1
• 時定数のグラフを追加	1
• 「アプリケーション」からディスク・ドライバ、ゲーム、ワイヤレス・トランシーバ、携帯電話を削除	1
• Added LPG (TO-92S) package	4
• Added <a href="#">Figure 10</a> to <i>Typical Characteristics</i>	7

Revision B (May 2014) から Revision C に変更	Page
• TO-126パッケージへのすべての言及 削除	1
• Added TO-92 LPM pin configuration graphic	4
• Changed Handling Ratings to ESD Ratings and moved Storage Temperature to Absolute Maximum Ratings table	5
• Changed KV to V	5
• Added TO-92 LP and LPM layout recommendations	15

Revision A (June 2013) から Revision B に変更	Page
• 新しいTI標準に準拠するようデータシートのフローとレイアウトを変更。「アプリケーションと実装」、「電源に関する推奨事項」、「レイアウト」、「デバイスおよびドキュメントのサポート」、「メカニカル、パッケージ、および注文情報」の各セクションを追加変更	1
• ドキュメント全体を通してTO-92およびTO-126パッケージの情報を追加	1

- Changed from 450°C/W to 275 °C/W. New specification is derived using TI 's latest methodology. .... 5
- Changed Temperature Accuracy Conditions from 70°C to 20°C and V<sub>DD</sub> from 1.9V to 1.8V..... 6
- Deleted Note: The input current is leakage only and is highest at high temperature. It is typically only 0.001 µA. The 1 µA limit is solely based on a testing limitation and does not reflect the actual performance of the part..... 6

## 5 Device Comparison Tables

**Table 1. Available Device Packages**

ORDER NUMBER <sup>(1)</sup>	PACKAGE	PIN	BODY SIZE (NOM)	MOUNTING TYPE
LMT85DCK	SOT (AKA <sup>(2)</sup> : SC70, DCK)	5	2.00 mm × 1.25 mm	Surface Mount
LMT85LP	TO-92 (AKA <sup>(2)</sup> : LP)	3	4.30 mm × 3.50 mm	Through-hole; straight leads
LMT85LPG	TO-92S (AKA <sup>(2)</sup> : LPG)	3	4.00 mm × 3.15 mm	Through-hole; straight leads
LMT85LPM	TO-92 (AKA <sup>(2)</sup> : LPM)	3	4.30 mm × 3.50 mm	Through-hole; formed leads
LMT85DCK-Q1	SOT (AKA <sup>(2)</sup> : SC70, DCK)	5	2.00 mm × 1.25 mm	Surface Mount

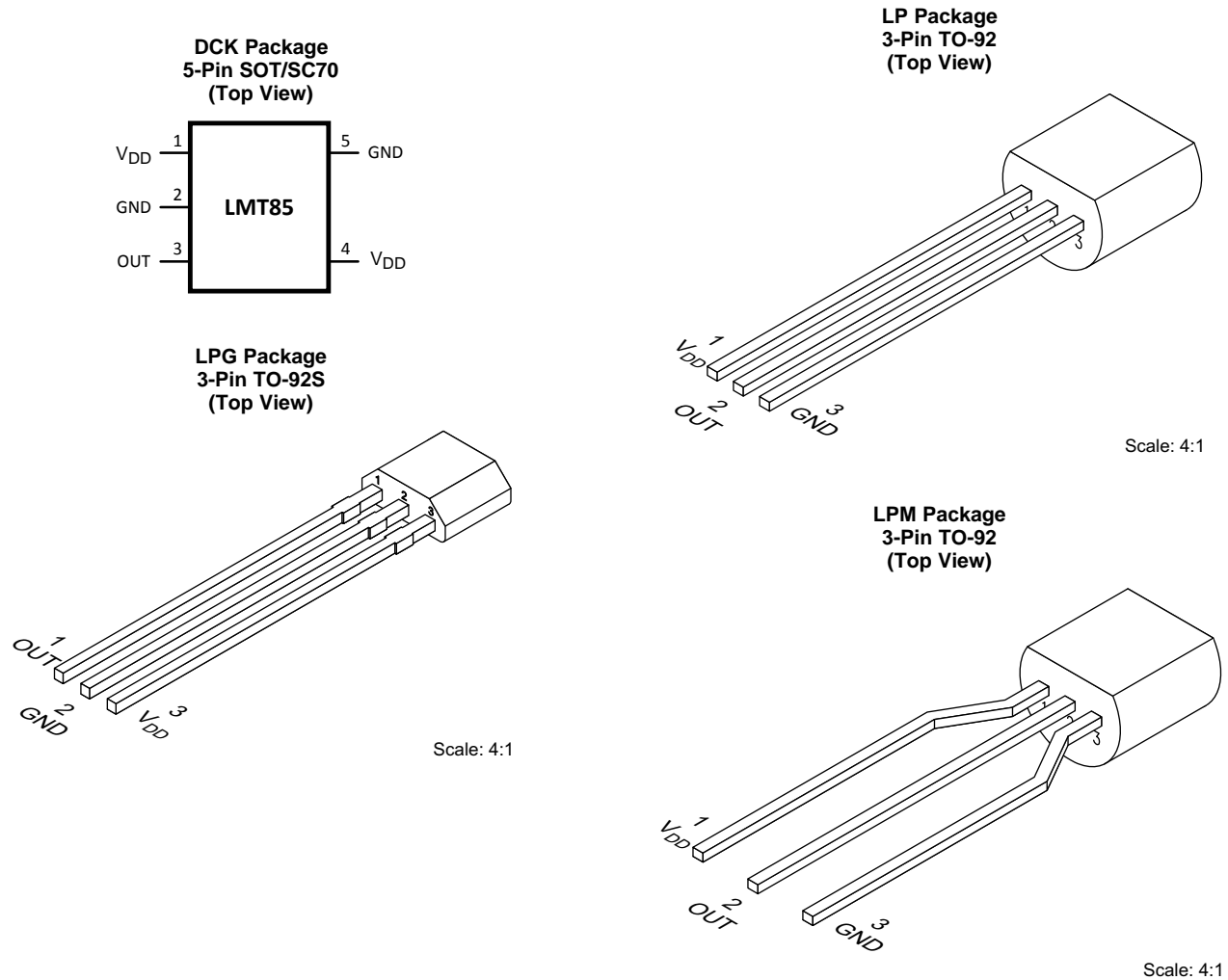
(1) For all available packages and complete order numbers, see the Package Option addendum at the end of the data sheet.

(2) AKA = Also Known As

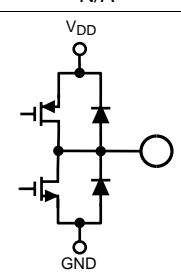
**Table 2. Comparable Alternative Devices**

DEVICE NAME	AVERAGE OUTPUT SENSOR GAIN	POWER SUPPLY RANGE
<a href="#">LMT84</a>	-5.5 mV/°C	1.5 V to 5.5 V
<a href="#">LMT85</a>	-8.2 mV/°C	1.8 V to 5.5 V
<a href="#">LMT86</a>	-10.9 mV/°C	2.2 V to 5.5 V
<a href="#">LMT87</a>	-13.6 mV/°C	2.7 V to 5.5 V

## 6 Pin Configuration and Functions



### Pin Functions

NAME	PIN			TYPE	DESCRIPTION	
	SOT (SC70)	TO-92	TO-92S		EQUIVALENT CIRCUIT	FUNCTION
GND	2 <sup>(1)</sup> , 5	3	2	Ground	N/A	Power Supply Ground
OUT	3	2	1	Analog Output		Outputs a voltage that is inversely proportional to temperature
V <sub>DD</sub>	1, 4	1	3	Power	N/A	Positive Supply Voltage

(1) Direct connection to the back side of the die

## 7 Specifications

### 7.1 Absolute Maximum Ratings

See <sup>(1)(2)</sup>

	MIN	MAX	UNIT
Supply voltage	-0.3	6	V
Voltage at output pin	-0.3	(V <sub>DD</sub> + 0.5)	V
Output current	-7	7	mA
Input current at any pin <sup>(3)</sup>	-5	5	mA
Maximum junction temperature (T <sub>JMAX</sub> )		150	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Soldering process must comply with Reflow Temperature Profile specifications. Refer to [www.ti.com/packaging](http://www.ti.com/packaging).
- (3) When the input voltage (V<sub>I</sub>) at any pin exceeds power supplies (V<sub>I</sub> < GND or V<sub>I</sub> > V), the current at that pin should be limited to 5 mA.

### 7.2 ESD Ratings

			VALUE	UNIT
LMT85LP in TO-92/TO-92S package				
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)(2)</sup>	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(3)</sup>	±1000	
LMT85DCK in SC70 package				
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per JESD22-A114 <sup>(2)</sup>	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(3)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
- (3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Specified temperature	T <sub>MIN</sub> ≤ T <sub>A</sub> ≤ T <sub>MAX</sub>		°C
	-50 ≤ T <sub>A</sub> ≤ 150		°C
Supply voltage (V <sub>DD</sub> )	1.8	5.5	V

### 7.4 Thermal Information<sup>(1)</sup>

THERMAL METRIC <sup>(2)</sup>	LMT85/ LMT85-Q1	LMT85LP	LMT85LPG	UNIT
	DCK (SOT/SC70)	LP/LPM (TO-92)	LPG (TO-92S)	
	5 PINS	3 PINS	3 PINS	
R <sub>θJA</sub> Junction-to-ambient thermal resistance <sup>(3)(4)</sup>	275	167	130.4	°C/W
R <sub>θJC(top)</sub> Junction-to-case (top) thermal resistance	84	90	64.2	°C/W
R <sub>θJB</sub> Junction-to-board thermal resistance	56	146	106.2	°C/W
ψ <sub>JT</sub> Junction-to-top characterization parameter	1.2	35	14.6	°C/W
ψ <sub>JB</sub> Junction-to-board characterization parameter	55	146	106.2	°C/W

- (1) For information on self-heating and thermal response time, see section [Mounting and Thermal Conductivity](#).
- (2) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report.
- (3) The junction to ambient thermal resistance (R<sub>θJA</sub>) under natural convection is obtained in a simulation on a JEDEC-standard, High-K board as specified in JESD51-7, in an environment described in JESD51-2. Exposed pad packages assume that thermal vias are included in the PCB, per JESD 51-5.
- (4) Changes in output due to self-heating can be computed by multiplying the internal dissipation by the thermal resistance.

## 7.5 Accuracy Characteristics

These limits do not include DC load regulation. These stated accuracy limits are with reference to the values in [Table 3](#).

PARAMETER	TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
Temperature accuracy <sup>(3)</sup>	$T_A = T_J = 20^\circ\text{C}$ to $150^\circ\text{C}$ ; $V_{DD} = 1.8\text{ V}$ to $5.5\text{ V}$	-2.7	±0.4	2.7	°C
	$T_A = T_J = 0^\circ\text{C}$ to $150^\circ\text{C}$ ; $V_{DD} = 1.9\text{ V}$ to $5.5\text{ V}$	-2.7	±0.7	2.7	°C
	$T_A = T_J = 0^\circ\text{C}$ to $150^\circ\text{C}$ ; $V_{DD} = 2.6\text{ V}$ to $5.5\text{ V}$		±0.3		°C
	$T_A = T_J = -50^\circ\text{C}$ to $0^\circ\text{C}$ ; $V_{DD} = 2.3\text{ V}$ to $5.5\text{ V}$	-2.7	±0.7	2.7	°C
	$T_A = T_J = -50^\circ\text{C}$ to $0^\circ\text{C}$ ; $V_{DD} = 2.9\text{ V}$ to $5.5\text{ V}$		±0.25		°C

- (1) Limits are specific to TI's AOQL (Average Outgoing Quality Level).
- (2) Typical values are at  $T_J = T_A = 25^\circ\text{C}$  and represent most likely parametric norm.
- (3) Accuracy is defined as the error between the measured and reference output voltages, tabulated in the Transfer Table at the specified conditions of supply gain setting, voltage, and temperature (expressed in °C). Accuracy limits include line regulation within the specified conditions. Accuracy limits do not include load regulation; they assume no DC load.

## 7.6 Electrical Characteristics

Unless otherwise noted, these specifications apply for  $V_{DD} = +1.8\text{V}$  to  $+5.5\text{V}$ . MIN and MAX limits apply for  $T_A = T_J = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted; typical values apply for  $T_A = T_J = 25^\circ\text{C}$ .

PARAMETER	TEST CONDITIONS	MIN <sup>(1)</sup>	TYP <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
Average sensor gain (output transfer function slope)	-30°C and 90°C used to calculate average sensor gain		-8.2		mV/°C
Load regulation <sup>(3)</sup>	Source $\leq 50\ \mu\text{A}$ , $(V_{DD} - V_{OUT}) \geq 200\text{ mV}$	-1	-0.22		mV
	Sink $\leq 50\ \mu\text{A}$ , $V_{OUT} \geq 200\text{ mV}$		0.26	1	mV
Line regulation <sup>(4)</sup>			200		μV/V
$I_S$ Supply current	$T_A = T_J = 30^\circ\text{C}$ to $150^\circ\text{C}$ , $(V_{DD} - V_{OUT}) \geq 100\text{ mV}$		5.4	8.1	μA
	$T_A = T_J = -50^\circ\text{C}$ to $150^\circ\text{C}$ , $(V_{DD} - V_{OUT}) \geq 100\text{ mV}$		5.4	9	μA
$C_L$ Output load capacitance			1100		pF
Power-on time <sup>(5)</sup>	$C_L = 0\text{ pF}$ to $1100\text{ pF}$		0.7	1.9	ms
Output drive	$T_A = T_J = 25^\circ\text{C}$	-50		+50	μA

- (1) Limits are specific to TI's AOQL (Average Outgoing Quality Level).
- (2) Typical values are at  $T_J = T_A = 25^\circ\text{C}$  and represent most likely parametric norm.
- (3) Source currents are flowing out of the LMT85. Sink currents are flowing into the LMT85.
- (4) Line regulation (DC) is calculated by subtracting the output voltage at the highest supply voltage from the output voltage at the lowest supply voltage. The typical DC line regulation specification does not include the output voltage shift discussed in [Output Voltage Shift](#).
- (5) Specified by design and characterization.

### 7.7 Typical Characteristics

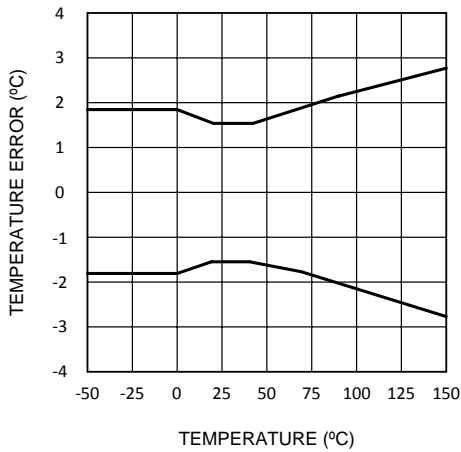


Figure 1. Temperature Error vs Temperature

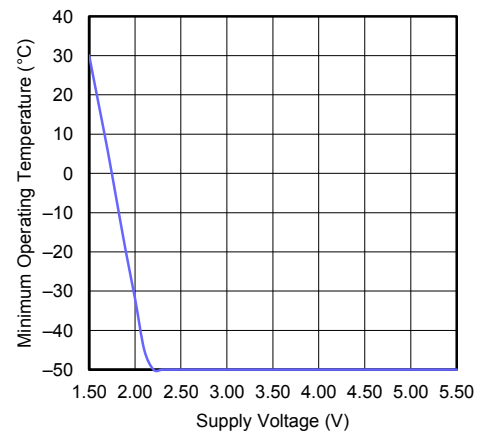


Figure 2. Minimum Operating Temperature vs Supply Voltage

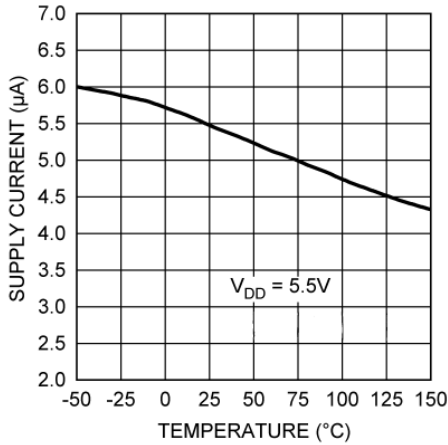


Figure 3. Supply Current vs Temperature

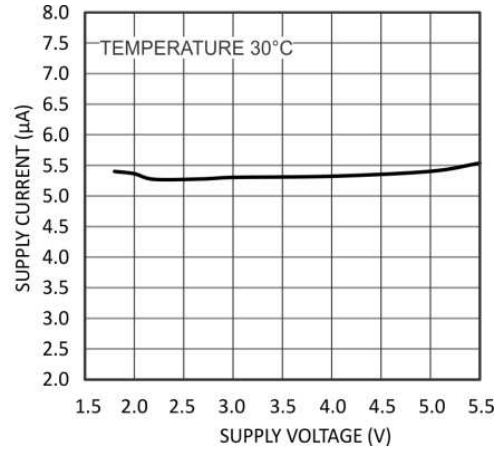


Figure 4. Supply Current vs Supply Voltage

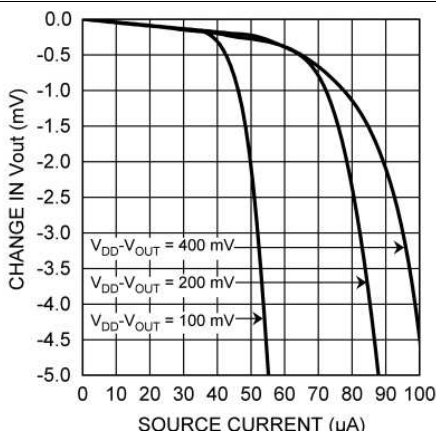


Figure 5. Load Regulation, Sourcing Current

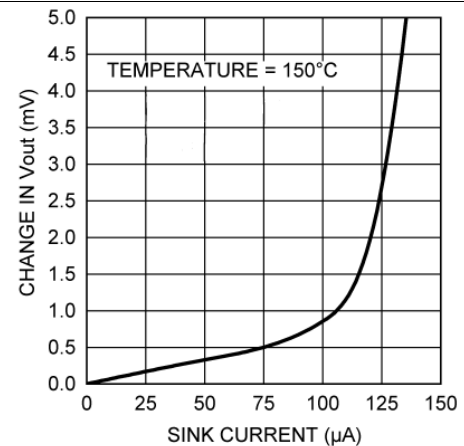


Figure 6. Load Regulation, Sinking Current

Typical Characteristics (continued)

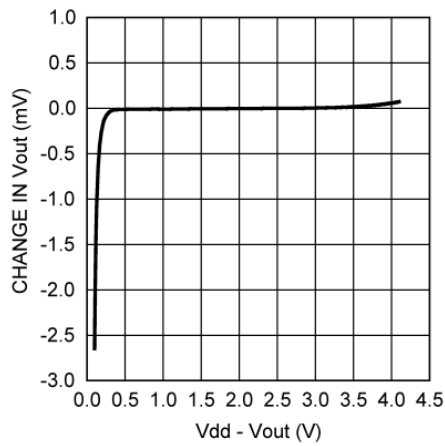


Figure 7. Change in Vout vs Overhead Voltage

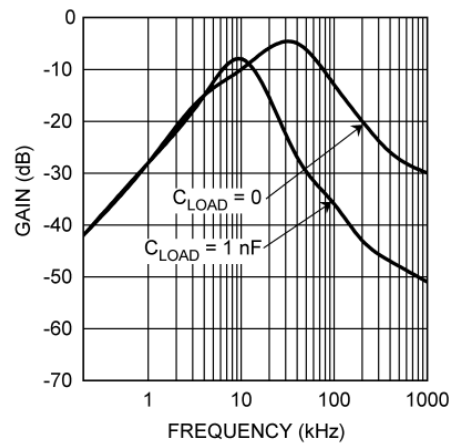


Figure 8. Supply-Noise Gain vs Frequency

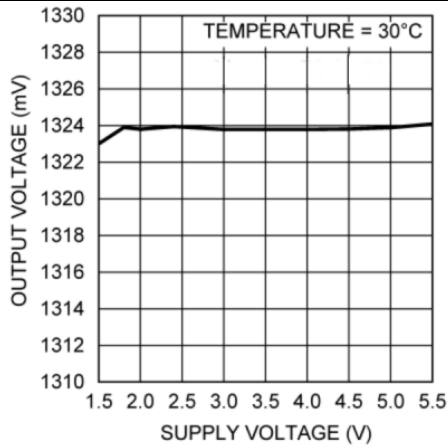


Figure 9. Output Voltage vs Supply Voltage

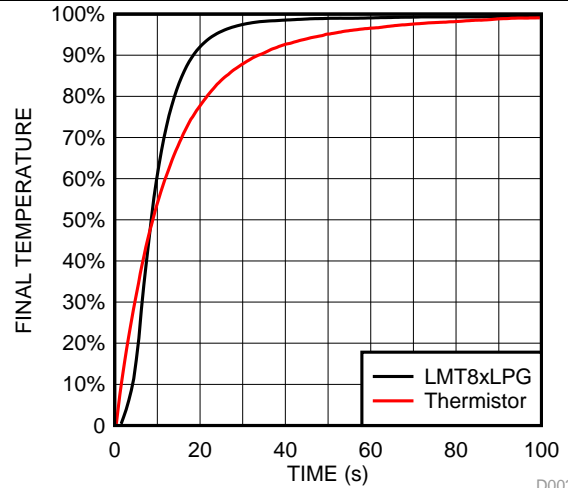


Figure 10. LMT85LPG Thermal Response vs Common Leaded Thermistor With 1.2-m/s Airflow



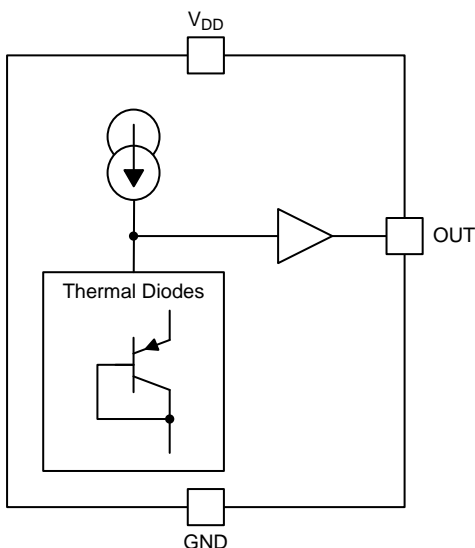
## 8 Detailed Description

### 8.1 Overview

The LMT85 is an analog output temperature sensor. The temperature sensing element is comprised of a simple base emitter junction that is forward biased by a current source. The temperature-sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage thus providing a low impedance output source.

### 8.2 Functional Block Diagram

Full-Range Celsius Temperature Sensor (–50°C to 150°C).



### 8.3 Feature Description

#### 8.3.1 LMT85 Transfer Function

The output voltage of the LMT85, across the complete operating temperature range, is shown in [Table 3](#). This table is the reference from which the LMT85 accuracy specifications (listed in the [Accuracy Characteristics](#) section) are determined. This table can be used, for example, in a host processor look-up table. A file containing this data is available for download at the [LMT85](#) product folder under *Tools and Software Models*.

**Table 3. LMT85 Transfer Table**

TEMP (°C)	V <sub>OUT</sub> (mV)	TEMP (°C)	V <sub>OUT</sub> (mV)	TEMP (°C)	V <sub>OUT</sub> (mV)	TEMP (°C)	V <sub>OUT</sub> (mV)	TEMP (°C)	V <sub>OUT</sub> (mV)
-50	1955	-10	1648	30	1324	70	991	110	651
-49	1949	-9	1639	31	1316	71	983	111	642
-48	1942	-8	1631	32	1308	72	974	112	634
-47	1935	-7	1623	33	1299	73	966	113	625
-46	1928	-6	1615	34	1291	74	957	114	617
-45	1921	-5	1607	35	1283	75	949	115	608
-44	1915	-4	1599	36	1275	76	941	116	599
-43	1908	-3	1591	37	1267	77	932	117	591
-42	1900	-2	1583	38	1258	78	924	118	582
-41	1892	-1	1575	39	1250	79	915	119	573
-40	1885	0	1567	40	1242	80	907	120	565
-39	1877	1	1559	41	1234	81	898	121	556
-38	1869	2	1551	42	1225	82	890	122	547

Feature Description (continued)

Table 3. LMT85 Transfer Table (continued)

TEMP (°C)	V <sub>OUT</sub> (mV)	TEMP (°C)	V <sub>OUT</sub> (mV)	TEMP (°C)	V <sub>OUT</sub> (mV)	TEMP (°C)	V <sub>OUT</sub> (mV)	TEMP (°C)	V <sub>OUT</sub> (mV)
-37	1861	3	1543	43	1217	83	881	123	539
-36	1853	4	1535	44	1209	84	873	124	530
-35	1845	5	1527	45	1201	85	865	125	521
-34	1838	6	1519	46	1192	86	856	126	513
-33	1830	7	1511	47	1184	87	848	127	504
-32	1822	8	1502	48	1176	88	839	128	495
-31	1814	9	1494	49	1167	89	831	129	487
-30	1806	10	1486	50	1159	90	822	130	478
-29	1798	11	1478	51	1151	91	814	131	469
-28	1790	12	1470	52	1143	92	805	132	460
-27	1783	13	1462	53	1134	93	797	133	452
-26	1775	14	1454	54	1126	94	788	134	443
-25	1767	15	1446	55	1118	95	779	135	434
-24	1759	16	1438	56	1109	96	771	136	425
-23	1751	17	1430	57	1101	97	762	137	416
-22	1743	18	1421	58	1093	98	754	138	408
-21	1735	19	1413	59	1084	99	745	139	399
-20	1727	20	1405	60	1076	100	737	140	390
-19	1719	21	1397	61	1067	101	728	141	381
-18	1711	22	1389	62	1059	102	720	142	372
-17	1703	23	1381	63	1051	103	711	143	363
-16	1695	24	1373	64	1042	104	702	144	354
-15	1687	25	1365	65	1034	105	694	145	346
-14	1679	26	1356	66	1025	106	685	146	337
-13	1671	27	1348	67	1017	107	677	147	328
-12	1663	28	1340	68	1008	108	668	148	319
-11	1656	29	1332	69	1000	109	660	149	310
								150	301

Although the LMT85 is very linear, its response does have a slight umbrella parabolic shape. This shape is very accurately reflected in Table 3. The Transfer Table can be calculated by using the parabolic equation (Equation 1).

$$V_{TEMP} (mV) = 1324.0mV - \left[ 8.194 \frac{mV}{^{\circ}C} (T - 30^{\circ}C) \right] - \left[ 0.00262 \frac{mV}{^{\circ}C^2} (T - 30^{\circ}C)^2 \right] \tag{1}$$

The parabolic equation is an approximation of the transfer table and the accuracy of the equation degrades slightly at the temperature range extremes. Equation 1 can be solved for T resulting in:

$$T = \frac{8.194 - \sqrt{(-8.194)^2 + 4 \times 0.00262 \times (1324 - V_{TEMP} (mV))}}{2 \times -0.00262} + 30 \tag{2}$$

For an even less accurate linear transfer function approximation, a line can easily be calculated over the desired temperature range using values from the Table and a two-point equation (Equation 3):

$$V - V_1 = \left( \frac{V_2 - V_1}{T_2 - T_1} \right) \times (T - T_1)$$

where

- V is in mV,
  - T is in °C,
  - T<sub>1</sub> and V<sub>1</sub> are the coordinates of the lowest temperature,
  - and T<sub>2</sub> and V<sub>2</sub> are the coordinates of the highest temperature.
- (3)

For example, if the user wanted to resolve this equation, over a temperature range of 20°C to 50°C, they would proceed as follows:

$$V - 1405 \text{ mV} = \left( \frac{1159 \text{ mV} - 1405 \text{ mV}}{50^\circ\text{C} - 20^\circ\text{C}} \right) \times (T - 20^\circ\text{C}) \quad (4)$$

$$V - 1405 \text{ mV} = (-8.20 \text{ mV} / ^\circ\text{C}) \times (T - 20^\circ\text{C}) \quad (5)$$

$$V = (-8.20 \text{ mV} / ^\circ\text{C}) \times T + 1569 \text{ mV} \quad (6)$$

Using this method of linear approximation, the transfer function can be approximated for one or more temperature ranges of interest.

## 8.4 Device Functional Modes

### 8.4.1 Mounting and Thermal Conductivity

The LMT85 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface.

To ensure good thermal conductivity, the backside of the LMT85 die is directly attached to the GND pin. The temperatures of the lands and traces to the other leads of the LMT85 will also affect the temperature reading.

Alternatively, the LMT85 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LMT85 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. If moisture creates a short circuit from the output to ground or  $V_{DD}$ , the output from the LMT85 will not be correct. Printed-circuit coatings are often used to ensure that moisture cannot corrode the leads or circuit traces.

The thermal resistance junction to ambient ( $R_{\theta JA}$  or  $\theta_{JA}$ ) is the parameter used to calculate the rise of a device junction temperature due to its power dissipation. Use [Equation 7](#) to calculate the rise in the LMT85 die temperature:

$$T_J = T_A + \theta_{JA} [(V_{DD}I_S) + (V_{DD} - V_{OUT}) I_L]$$

where

- $T_A$  is the ambient temperature,
- $I_S$  is the supply current,
- $I_L$  is the load current on the output,
- and  $V_O$  is the output voltage. (7)

For example, in an application where  $T_A = 30^\circ\text{C}$ ,  $V_{DD} = 5 \text{ V}$ ,  $I_S = 5.4 \mu\text{A}$ ,  $V_{OUT} = 1324 \text{ mV}$ , and  $I_L = 2 \mu\text{A}$ , the junction temperature would be  $30.014^\circ\text{C}$ , showing a self-heating error of only  $0.014^\circ\text{C}$ . Because the junction temperature of the LMT85 is the actual temperature being measured, take care to minimize the load current that the LMT85 is required to drive. [Thermal Information](#) shows the thermal resistance of the LMT85.

### 8.4.2 Output and Noise Considerations

A push-pull output gives the LMT85 the ability to sink and source significant current. This is beneficial when, for example, driving dynamic loads like an input stage on an analog-to-digital converter (ADC). In these applications the source current is required to quickly charge the input capacitor of the ADC. The LMT85 device is ideal for this and other applications which require strong source or sink current.

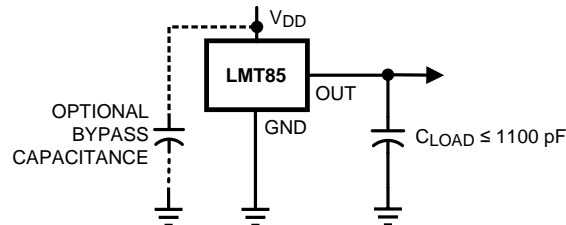
The LMT85 supply-noise gain (the ratio of the AC signal on  $V_{OUT}$  to the AC signal on  $V_{DD}$ ) was measured during bench tests. The typical attenuation is shown in [Figure 8](#) found in the [Typical Characteristics](#). A load capacitor on the output can help to filter noise.

For operation in very noisy environments, some bypass capacitance should be present on the supply within approximately 5 centimeters of the LMT85.

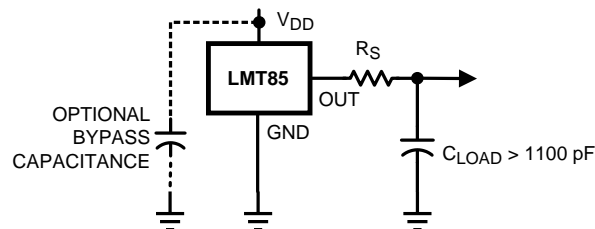
## Device Functional Modes (continued)

### 8.4.3 Capacitive Loads

The LMT85 handles capacitive loading well. In an extremely noisy environment, or when driving a switched sampling input on an ADC, it may be necessary to add some filtering to minimize noise coupling. Without any precautions, the LMT85 can drive a capacitive load less than or equal to 1100 pF as shown in [Figure 11](#). For capacitive loads greater than 1100 pF, a series resistor may be required on the output, as shown in [Figure 12](#).



**Figure 11. LMT85 No Decoupling Required for Capacitive Loads Less Than 1100 pF**



**Figure 12. LMT85 with Series Resistor for Capacitive Loading Greater Than 1100 pF**

**Table 4. Recommended Series Resistor Values**

$C_{LOAD}$	MINIMUM $R_S$
1.1 nF to 99 nF	3 k $\Omega$
100 nF to 999 nF	1.5 k $\Omega$
1 $\mu$ F	800 $\Omega$

### 8.4.4 Output Voltage Shift

The LMT85 is very linear over temperature and supply voltage range. Due to the intrinsic behavior of an NMOS/PMOS rail-to-rail buffer, a slight shift in the output can occur when the supply voltage is ramped over the operating range of the device. The location of the shift is determined by the relative levels of  $V_{DD}$  and  $V_{OUT}$ . The shift typically occurs when  $V_{DD} - V_{OUT} = 1$  V.

This slight shift (a few millivolts) takes place over a wide change (approximately 200 mV) in  $V_{DD}$  or  $V_{OUT}$ . Because the shift takes place over a wide temperature change of 5°C to 20°C,  $V_{OUT}$  is always monotonic. The accuracy specifications in the [Accuracy Characteristics](#) table already include this possible shift.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The LMT85 features make it suitable for many general temperature-sensing applications. It can operate down to 1.8-V supply with 5.4- $\mu$ A power consumption, making it ideal for battery powered devices. Package options like the through-hole TO-92 package allow the LMT85 to be mounted onboard, off-board, to a heat sink, or on multiple unique locations in the same application.

### 9.2 Typical Applications

#### 9.2.1 Connection to an ADC

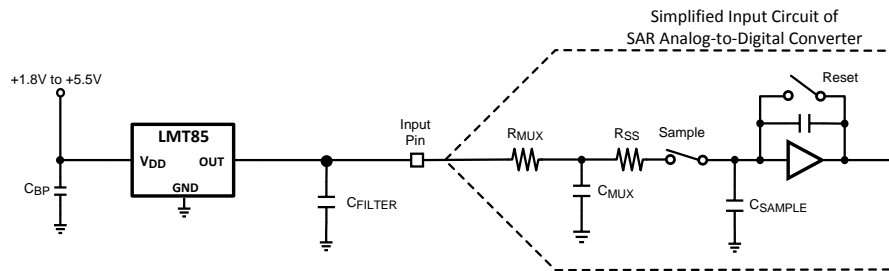


Figure 13. Suggested Connection to a Sampling Analog-to-Digital Converter Input Stage

##### 9.2.1.1 Design Requirements

Most CMOS ADCs found in microcontrollers and ASICs have a sampled data comparator input structure. When the ADC charges the sampling cap, it requires instantaneous charge from the output of the analog source such as the LMT85 temperature sensor and many op amps. This requirement is easily accommodated by the addition of a capacitor ( $C_{FILTER}$ ).

##### 9.2.1.2 Detailed Design Procedure

The size of  $C_{FILTER}$  depends on the size of the sampling capacitor and the sampling frequency. Because not all ADCs have identical input stages, the charge requirements will vary. This general ADC application is shown as an example only.

##### 9.2.1.3 Application Curve

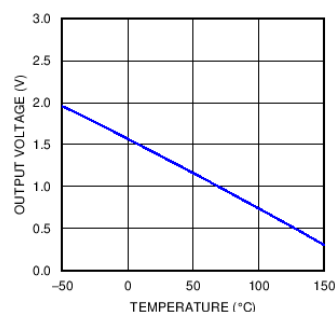


Figure 14. Analog Output Transfer Function

## Typical Applications (continued)

### 9.2.2 Conserving Power Dissipation With Shutdown

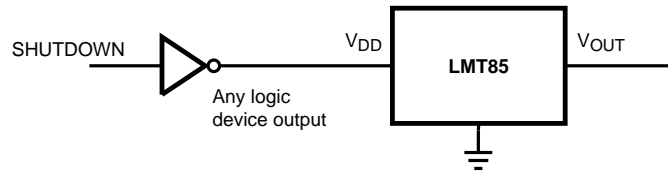


Figure 15. Simple Shutdown Connection of the LMT85

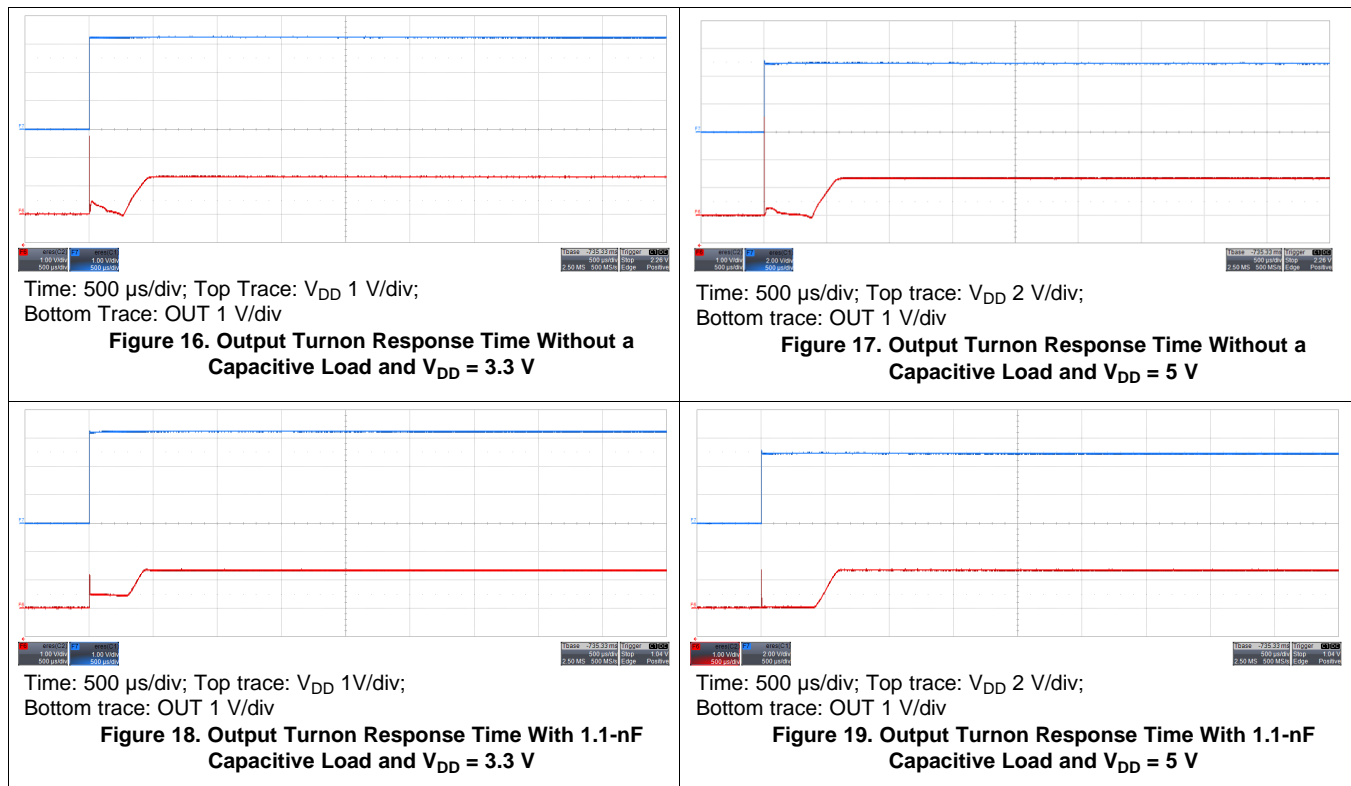
#### 9.2.2.1 Design Requirements

Because the power consumption of the LMT85 is less than 9  $\mu\text{A}$ , it can simply be powered directly from any logic gate output and therefore not require a specific shutdown pin. The device can even be powered directly from a micro controller GPIO. In this way, it can easily be turned off for cases such as battery-powered systems where power savings are critical.

#### 9.2.2.2 Detailed Design Procedure

Simply connect the V<sub>DD</sub> pin of the LMT85 directly to the logic shutdown signal from a microcontroller.

#### 9.2.2.3 Application Curves



## 10 Power Supply Recommendations

The low supply current and supply range (1.8 V to 5.5 V) of the LMT85 allow the device to easily be powered from many sources. Power supply bypassing is optional and is mainly dependent on the noise on the power supply used. In noisy systems it may be necessary to add bypass capacitors to lower the noise that is coupled to the output of the LMT85.

## 11 Layout

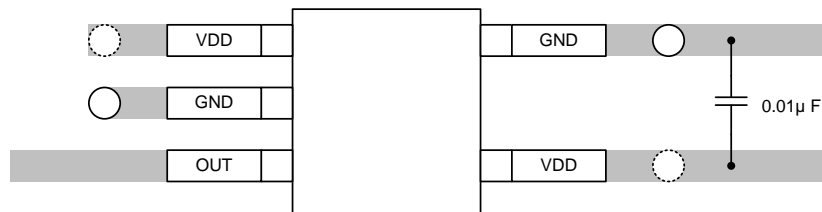
### 11.1 Layout Guidelines

The LMT85 is extremely simple to layout. If a power-supply bypass capacitor is used, it should be connected as shown in the [Layout Example](#)

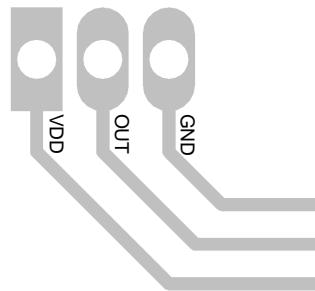
### 11.2 Layout Example

○ VIA to ground plane

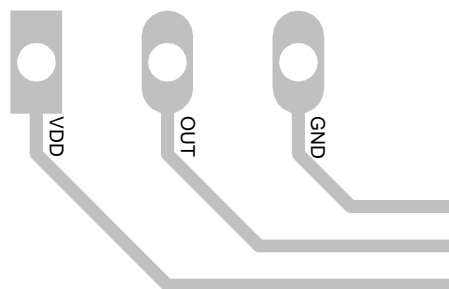
○ VIA to power plane



**Figure 20. SC70 Package Recommended Layout**



**Figure 21. TO-92 LP Package Recommended Layout**



**Figure 22. TO-92 LPM Package Recommended Layout**

## 12 デバイスおよびドキュメントのサポート

### 12.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™オンライン・コミュニティ** *TIのE2E (Engineer-to-Engineer) コミュニティ*。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

**設計サポート** *TIの設計サポート* 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

### 12.3 商標

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 静電気放電に関する注意事項



これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMT85DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-50 to 150	BPA	<a href="#">Samples</a>
LMT85LP	ACTIVE	TO-92	LP	3	1800	RoHS & Green	SN	N / A for Pkg Type	-50 to 150	LMT85	<a href="#">Samples</a>
LMT85LPG	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-50 to 150	LMT85	<a href="#">Samples</a>
LMT85LPGM	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-50 to 150	LMT85	<a href="#">Samples</a>
LMT85LPM	ACTIVE	TO-92	LP	3	2000	RoHS & Green	SN	N / A for Pkg Type	-50 to 150	LMT85	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF LMT85 :**

- Automotive : [LMT85-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMT85DCKR	SC70	DCK	5	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMT85DCKR	SC70	DCK	5	3000	208.0	191.0	35.0

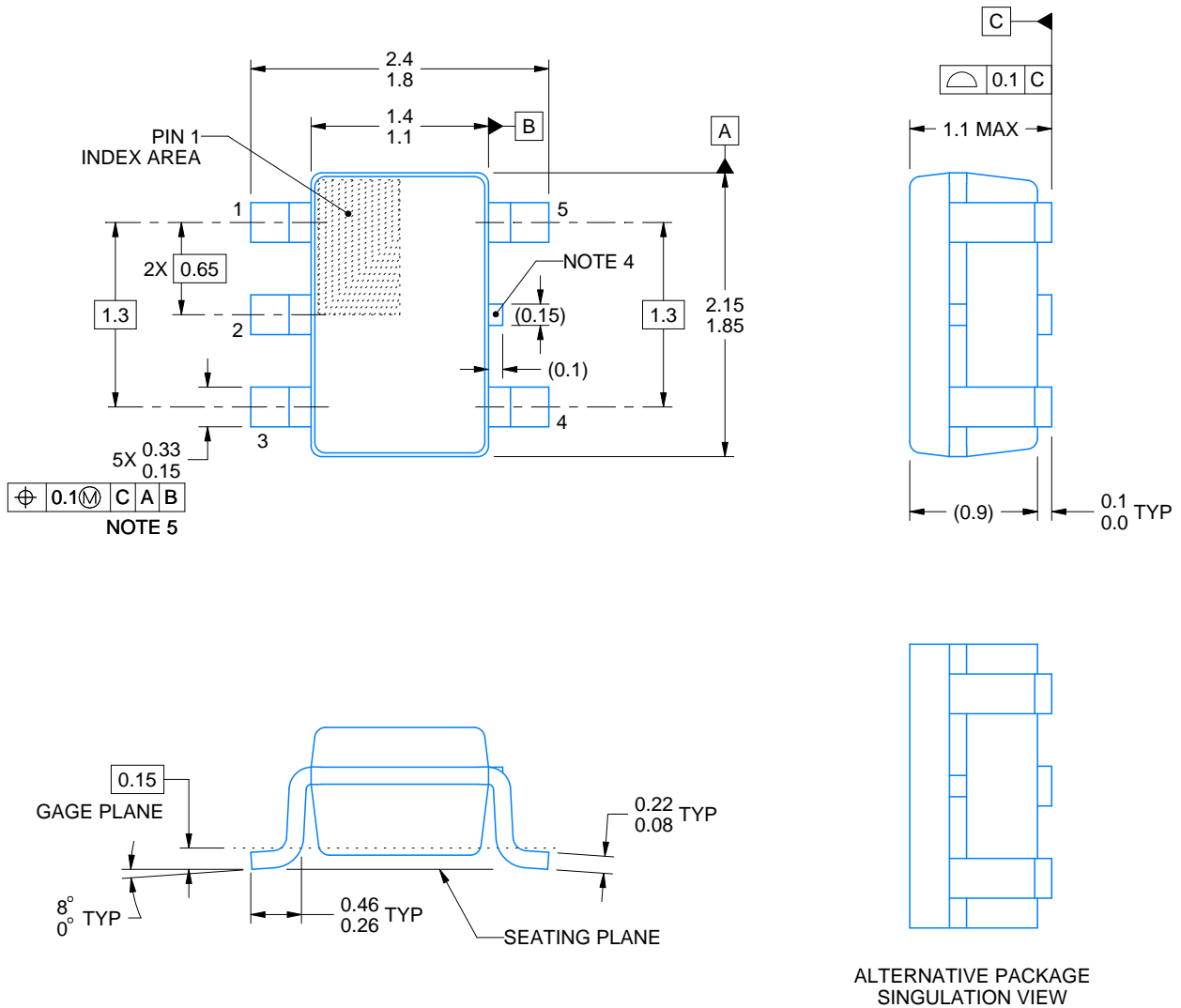
# DCK0005A



## PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/E 06/2024

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/E 06/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE: 18X

4214834/E 06/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

# LPG0003A



# PACKAGE OUTLINE

## TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



4221343/C 01/2018

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



# EXAMPLE BOARD LAYOUT

LPG0003A

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



LAND PATTERN EXAMPLE  
NON-SOLDER MASK DEFINED  
SCALE:20X

4221343/C 01/2018



## GENERIC PACKAGE VIEW

LP 3

TO-92 - 5.34 mm max height

TRANSISTOR OUTLINE



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040001-2/F

LP0003A



# PACKAGE OUTLINE

TO-92 - 5.34 mm max height

TO-92



4215214/B 04/2017

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within this area.
4. Reference JEDEC TO-226, variation AA.
5. Shipping method:
  - a. Straight lead option available in bulk pack only.
  - b. Formed lead option available in tape and reel or ammo pack.
  - c. Specific products can be offered in limited combinations of shipping medium and lead options.
  - d. Consult product folder for more information on available options.



LAND PATTERN EXAMPLE  
STRAIGHT LEAD OPTION  
NON-SOLDER MASK DEFINED  
SCALE:15X



LAND PATTERN EXAMPLE  
FORMED LEAD OPTION  
NON-SOLDER MASK DEFINED  
SCALE:15X

# TAPE SPECIFICATIONS

LP0003A

TO-92 - 5.34 mm max height

TO-92



FOR FORMED LEAD OPTION PACKAGE

4215214/B 04/2017

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated