UCC24612 高周波同期整流コントローラ

1 特長

- アクティブ・クランプ・フライバック、QR、DCM、CCMフライバック、LLCなどのトポロジをサポート
- 最大230VのMOSFET V_{DS}センシング
- 最高1MHzの動作周波数
  - UCC24612-1で1MHz
  - UCC24612-2で800kHz
- VDD範囲が広いため、5V～28Vの出力システムからダイレクト・バイアスが可能
- 4Aシンク、1Aソースの比例ゲート駆動能力を備えたゲート・ドライバ
- 適応型最小オフ時間制御によりノイズ耐性が向上
- サイクル制限プリターンオフによりCCMの効率が向上
- ハイサイド/ローサイドの構成が可能
- 軽負荷/スリープ・モードを自動的に管理、スタンバイ電流320µA
- ターンオフ伝搬遅延: 16ns (標準値)
- 9.5Vのゲート駆動クランプにより駆動損失を低減

2 アプリケーション

- AC/DCアダプタ
- USB Type-C/Power Delivery ACアダプタ
- サーバー/通信機器電源
- AC/DC補助電源

3 概要

UCC24612は、標準および論理レベルNチャネルMOSFETパワー・デバイス向けの高性能同期整流コントローラ/ドライバです。ほぼ理想的なダイオード・エミュレーションを実装しているため、出力整流器の損失を低減し、間接的に1次側の損失を低減することができます。ドレイン-ソース間(V_{DS})センシング制御方式により、アクティブ・クランプ・フライバック、QR/DCM/CCMフライバック、LLCなど、複数のトポロジを使用できます。

内蔵された機能により、設計が簡単な上、さまざまなアプリケーションや周波数で優れた性能を発揮します。動作VDDおよびVD電圧範囲が広いことから、28Vまでの出力のシステムに簡単に実装でき、適応型最小オフ時間制御により、効率性およびノイズ耐性も向上しています。UCC24612-1とUCC24612-2では、ノイズ耐性の向上をもたらす最小オン時間が異なります。比例ゲート駆動およびCCMサイクル制限プリターンオフにより、連続導通モード(CCM)での安定動作もさらに向上しています。

UCC24612には、効率性を高めるさまざまな機能が搭載されています。伝搬遅延が短い高速コンパレータによりスイッチング損失が低減され、9.5Vのゲート駆動クランプによりMOSFETの駆動損失が低減されます。周波数に依存するスタンバイ・モードでは、スタンバイ消費電力をさらに削減できます。このような機能を備えたUCC24612を採用することで、DoE (米国エネルギー省)のレベルVIやCoC (欧州委員会の行動規範)のティア2といった厳しい効率基準を満たす優れたシステムを構築できます。

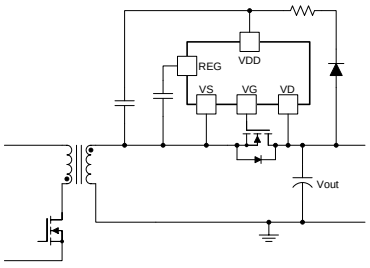
UCC24612はSOT23-5パッケージで供給されます。

製品情報(1)

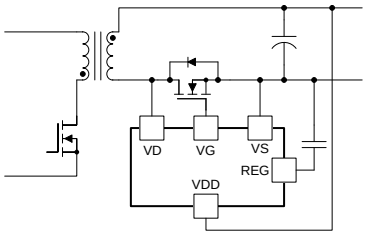
型番	パッケージ	本体サイズ(公称)
UCC24612	SOT23 (5)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ハイサイドSRによるフライバック



ローサイドSRによるフライバック



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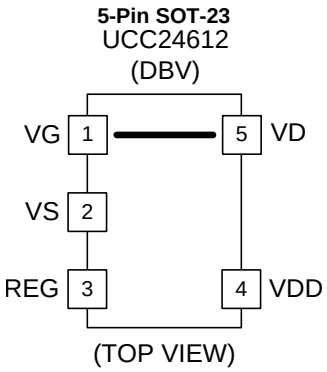
4 改訂履歴

日付	改訂内容	注
2018年2月	A	初版

Table 1. Device Comparison

ORDERABLE PART NUMBER	TURN ON PROPAGATION DELAY	MINIMUM ON TIME	MAXIMUM SWITCHING FREQUENCY	BEST SUITABLE TOPOLOGIES
UCC24612-1	80 ns	375 ns	1 MHz	CCM/DCM/QR Flyback, Active Clamp Flyback using GaN MOSFET as primary-side switch
UCC24612-2	170 ns	540 ns	800 kHz	LLC, Active Clamp Flyback using Si MOSFET as primary-side switch

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
REG	3	O	REG is the device bias pin. An internal linear regulator from VDD to REG generates a well regulated 9.5-V voltage. It is recommend to put a 2.2-µF bypass capacitor from REG pin to VS pin.
VD	5	I	MOSFET drain voltage sensing input. Connect this pin to SR MOSFET drain pin. The layout should avoid sharing the VD pin trace with the power path to minimize the impact of parasitic inductance.
VDD	4	I	Internal linear regulator input. Connect this pin to the output voltage when in low-side SR configuration. Use R-C-D circuit or other circuits to generate bias voltage from SR MOSFET drain when using high-side SR configuration, referring to Power Supply Recommendations for details.
VG	1	O	VG (controlled MOSFET gate drive), connect VG to the gate of the controlled MOSFET through a small series resistor using short PC board tracks to achieve optimal switching performance. The VG output can achieve >1-A peak source current when High and >4-A peak sink current when Low when connected to a large N-channel power MOSFET. Due to the weak internal pull up after initial fast turn on, avoid putting a resistor less than 50 kΩ between VG to VS .
VS	2	-	VS is the internal ground reference of the UCC24612. It is also used to sense the voltage drop across the SR MOSFET. The layout should avoid sharing the VS pin trace with the power path to minimize the impact of parasitic inductance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage (2)	VDD	–0.3	30	V
	VD	–0.7	230	V
	VG	–0.3	V_{REG}	V
	VD for I_{VD} ≤ –10 mA	–1.0	230	V
	REG		12	V
Output current, peak	VG (3) pulsed, t_{PULSE} ≤ 4 ms, duty cycle ≤ 1%		±4	A
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input voltages more negative than indicated may exist on any listed pin without excess stress or damage to the device if the pin's input current magnitude is limited to less than -10mA.
(3) In normal use, VG is connected to the gate of a power MOSFET through a small resistor. When used this way, VG current is limited by the UCC24612 and no absolute maximum output current considerations are required. The series resistor shall be selected to minimize overshoot and ringing due to series inductance of the VG output and power-MOSFET gate-drive loop. Continuous VG current is subject to the maximum operating junction temperature limitation.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins, except pin 5 (1)	±2,000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, pin 5 (1)	±1,500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VDD}	VDD input voltage	4		28	V
C_{VDD}	VDD bypass capacitor	1			µF
C_{REG}	REG bypass capacitor	1.5	2.2		µF
T_J	Junction temperature	–40		125	°C
f_{S_MAX}	Maximum switching frequency UCC24612-1	770		1000	kHz
	Maximum switching frequency UCC24612-2	625		800	

6.4 Thermal Information

THERMAL METRIC(1)		UCC24612 DBV (SOT23-5) 5 PINs	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	206.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	97.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *the Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At VDD = 12 V_{DC}, C_{VG} = 0 pF, C_{REG} = 2.2 µF, −40°C ≤ T_J = T_A ≤ +125°C, all voltages are with respect to VS, and currents are positive into and negative out of the specified terminal, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS SUPPLY						
$IVDD_{START}$	VDD current, REG undervoltage	VDD = 4 V, VD = 0 V	50	105	150	µA
$IVDD_{RUN}$	VDD current, run	VDD = 12 V	0.5	0.92	1.5	mA
		VDD = 5 V	0.5	0.9	1.5	mA
$IVDD_{STBY}$	VDD current, standby mode	VDD = 12 V, VD = 1 V	200	390	650	µA
		VDD = 5 V, VD = 1 V	200	320	500	µA
UNDERVOLTAGE LOCKOUT (UVLO)						
$VREG_{ON}$	REG turn-on threshold	Turn-on detected by IVDD rising	4.15	4.5	4.87	V
$VREG_{OFF}$	REG turn-off threshold	Turn-off detected by IVDD falling	3.65	4	4.25	V
$VREG_{HYST}$	UVLO hysteresis	$VREG_{HYST}$ = $VREG_{ON}$ – $VREG_{OFF}$	0.425	0.5	0.575	V
MOSFET VOLTAGE SENSING						
V_{THVGON}	VG turn-on threshold	VD falling, T_J = 25°C	–300	–240	–175	mV
$V_{THVGOFF}$	VG turn-off threshold	VD rising, T_J = 25°C	–20	-9	–2	mV
		VD rising, –40°C ≤T_J ≤ 125°C	–30	–9	–2	
V_{THARM}	VG re-arming threshold	VD rising	0.4	0.5	0.6	V
I_{VDBIAS_ON}	VD pin bias current when VG is high (SR is on)	V_{VD} = –50 mV, V_{VG} = VG_H	–1	0	1	µA
I_{VDBIAS_OFF}	VD pin bias current when VG is low (SR is off)	V_{VD} = –150 mV, V_{VG} = VG_L, T_J = 25°C	–6	–2		µA
		V_{VD} = –150 mV, V_{VG} = VG_L, –40°C ≤T_J ≤ 125°C	–10			
I_{VDLK}	VD pin leakage current	V_{VD} = 200 V		0.06	2	µA
GATE DRIVER						
R_{SOURCE}	VG pull-up resistance	I_{VG} = –20 mA		5.7	10	Ω
R_{SINK}	VG pull-down resistance	I_{VG} = 100 mA		0.45	1	Ω
VG_H	VG clamp level		8.55	9.4	10.26	V
VG_L	VG output low voltage	I_{VG} = 100 mA, VDD = 12 V		60	150	mV
V_{OLGUV}	VG output low voltage in UVLO	I_{VG} = 25 mA, VDD = 4 V			0.7	V
IVG_{PU}	Gate driver maximum source current			1 (1)		A
IVG_{PD}	Gate driver maximum sink current	(1)		4		A
REG SUPPLY						
V_{REG}	REG pin regulation level	I_{LOAD_REG} = 0 mA	8.55	9.4	10.26	V
$VREG_{LG}$	Load regulation on REG	I_{LOAD_REG}= 10 mA to 0 mA		0.016	0.1	V
$VREG_{DO}$	REG drop-out on pass-through mode	VDD = 5 V, I_{LOAD_REG}= 10 mA		0.28	0.45	V
$IREG_{SC}$	REG short-circuit current	V_{REG} = 0 V	1	5.2	15	mA
$IREG_{LIM}$	REG current limit	V_{REG} = 8 V	25	42	62	mA

(1) Specified by design

6.6 Timing Requirements

At VDD = 12 V_{DC}, C_{VG} = 0 pF, C_{REG} = 2.2 µF, −40°C ≤ T_J = T_A ≤ +125°C, all voltages are with respect to VS, and currents are positive into and negative out of the specified terminal, unless otherwise noted. Typical values are at T_J = +25°C.

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
MOSFET VOLTAGE SENSING						
td_{VGON}	Gate turn-on propagation delay	VD transitions from 4.7 V to –0.3 V in 5 ns, UCC24612-1, T_J = 25°C, see curve for more information	40	80	120	ns
		VD transitions from 4.7 V to –0.3 V in 5 ns, UCC24612-2, T_J = 25°C, see curve for more information	120	170	225	
td_{VGOFF}	Gate turn-off propagation delay	VD moves from -0.3 V to 4.7 V in 5 ns		16	35	ns
MINIMUM ON-TIME						
$t_{ON(min)}$	Minimum SR conduction time	UCC24612 -1	245	375	475	ns
		UCC24612 -2	350	540	670	ns
Adaptive MINIMUM OFF-TIME						
t_{OFF_ABSMIN}	Absolute minimum SR off-time	UCC24612-1	200	400	595	ns
		UCC24612-2	160	360	545	
t_{OFF_MAX}	Maximum SR off-blanking time		2.65	3.68	4.65	µs
GATE DRIVER						
t_{r_VG}	VG rise time	10% to 90%, C_{VG} = 6.8 nF	10	32	65	ns
t_{f_VG}	VG fall time,	90% to 10%, C_{VG} = 6.8 nF	5	16	35	ns
LIGHTLOAD / STANDBY						
t_{STBY_DET}	Standby mode detection time		3	4.5	6	ms
f_{SLEEP}	Average frequency entering standby mode		8	12	16	kHz
f_{WAKE}	Average frequency coming out of standby mode		10	15	20	kHz
f_{STB_HYS}	Average frequency hysteresis for standby mode		2	3	4	kHz
PROTECTION						
T_{TSD}	Thermal shut-down threshold		130 (1)	165		ºC
T_{HYS}	Thermal shut-down recovery hysteresis			15		ºC

(1) Specified by design

6.7 Typical Characteristics

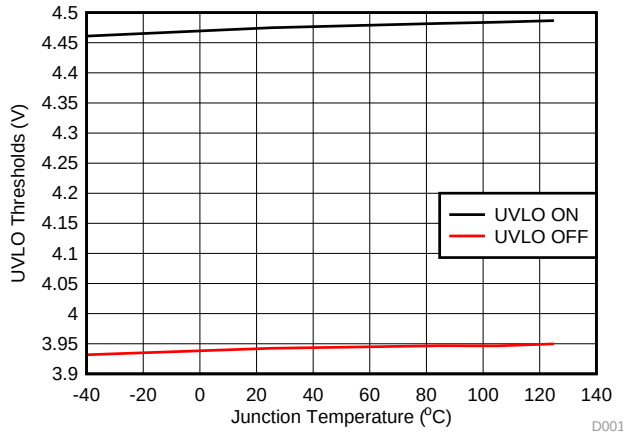


Figure 1. UVLO Threshold Voltage vs Temperature

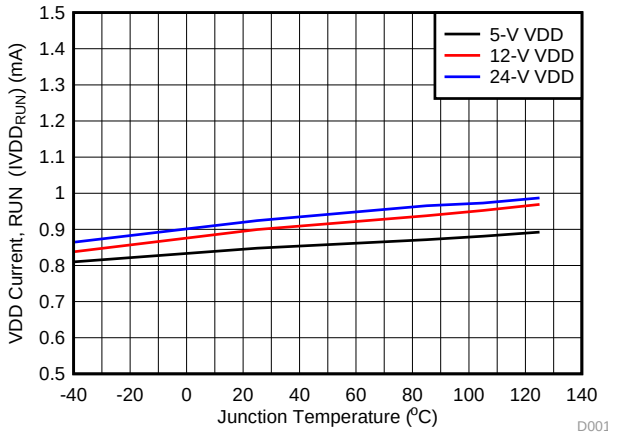


Figure 2. Bias Supply Current vs. Temperature (C_{VG}= 0 pF, V_{VD} = 1 V and No Switching)

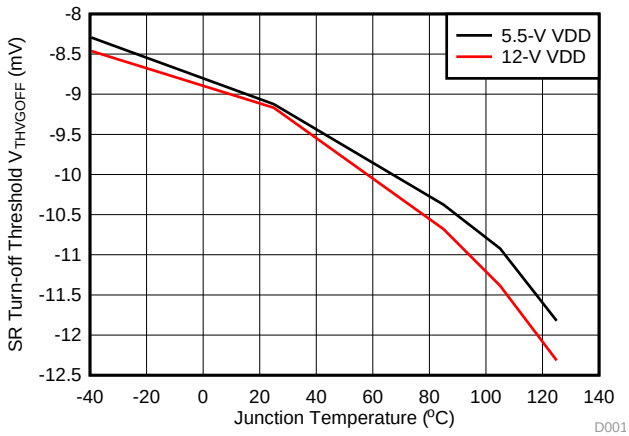


Figure 3. SR Turn-off Threshold Voltages vs Temperature

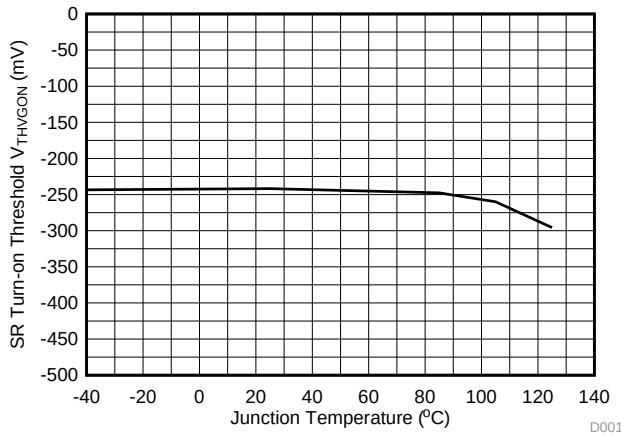


Figure 4. SR Turn-on Threshold Voltage vs Temperature

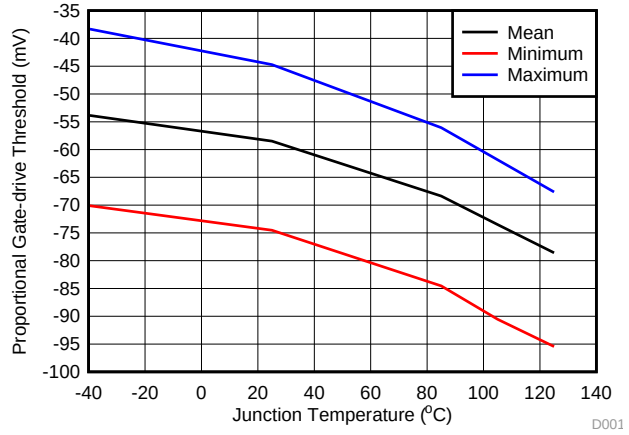


Figure 5. Proportional Gate-drive Threshold vs Temperature

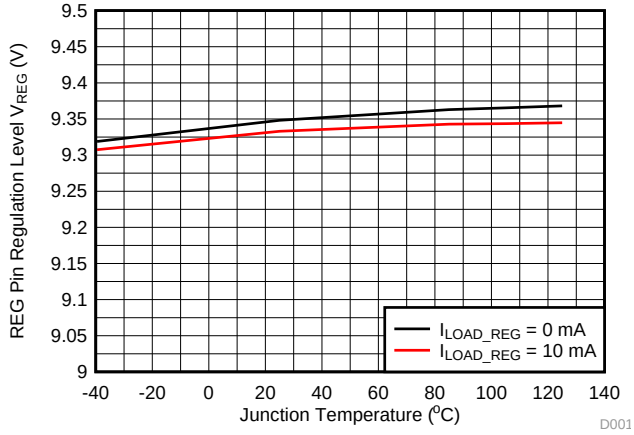


Figure 6. REG Pin Voltage vs Temperature at Different Loading Conditions

Typical Characteristics (continued)

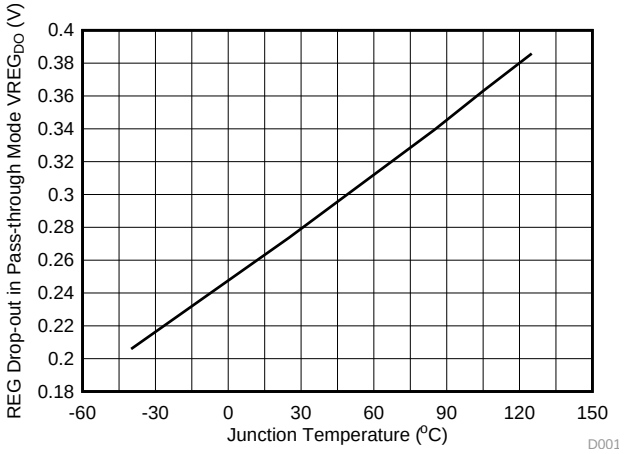


Figure 7. REG Drop-out in Pass-through Mode vs Temperature, I_{LOAD_REG} = 10 mA

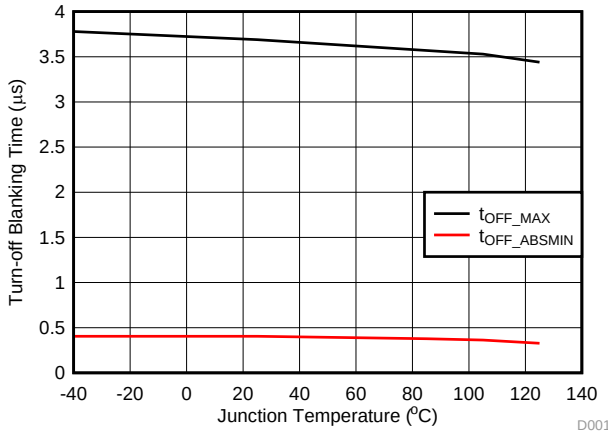


Figure 8. Abs. Minimum Turn-off Blanking Time and Maximum Turn-off Blanking Time vs Temperature

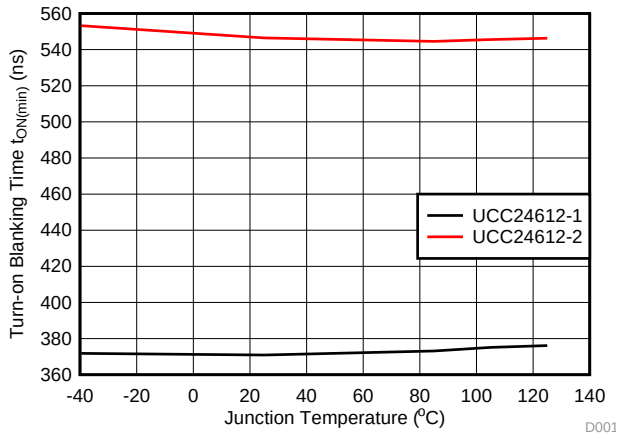


Figure 9. Turn-On Blanking Time vs Temperature

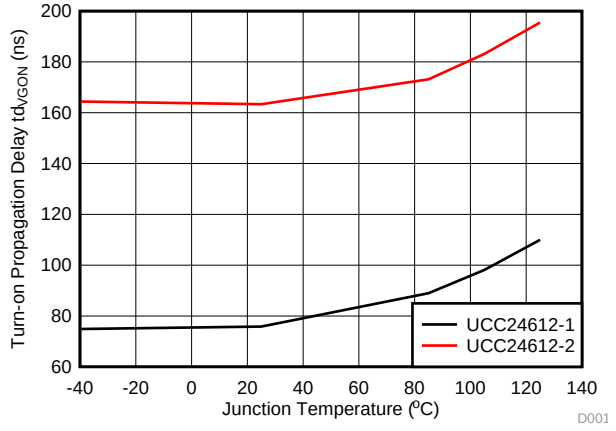


Figure 10. SR Turn-on Delay Time vs Temperature

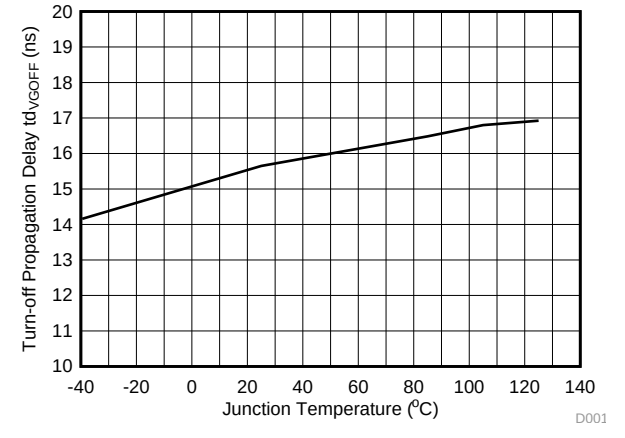


Figure 11. SR Turn-off Propagation Delay vs Temperature

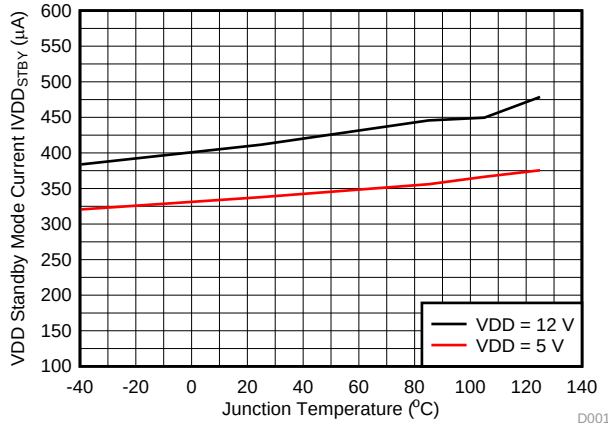


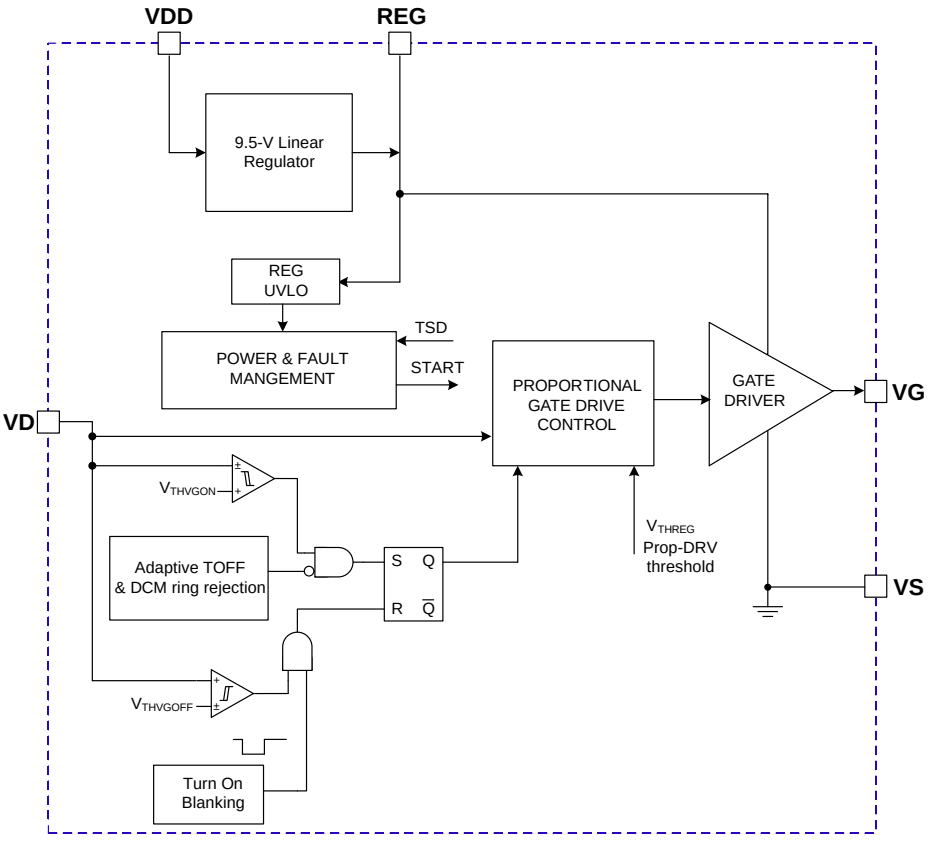
Figure 12. Standby Current vs Temperature

7 Detailed Description

7.1 Overview

The UCC24612 synchronous rectifier (SR) controller uses drain-to-source voltage sensing to determine the SR MOSFET conduction interval. The SR MOSFET is turned on when V_{DS} exceeds turn-on threshold V_{THVGON}, and is turned off when V_{DS} falls below $V_{THVGOFF}$. The SR conduction voltage drop is continuously monitored and regulated to minimize the conduction loss while allowing the SR to pre-turn-off when operating in continuous conduction mode (CCM) . The extremely fast turn-off comparator and driving circuit ensures the fast turn-off of the SR MOSFET, even in CCM condition. Fixed minimum on-time ($t_{ON(min)}$) allows the controller to operate up to 1-MHz switching frequency (1 MHz for UCC24612-1, 800 kHz for UCC24612-2). The adaptive minimum off-time control simplifies the design, making the controller suitable for a wide range of applications and switching frequencies, with good immunity to noise caused by parasitic ringing. To minimize the standby power, automatic light-load mode disables the VG pulses when the average switching frequency of the converter becomes lower than f_{SLEEP} (12 kHz typical). When the load increases such that the average switching frequency increases above f_{WAKE} (15 kHz typical), the controller resumes normal SR operation. The wide VDD range and gate driver clamp make the controller ideal for wide output voltage range applications such as USB Power Delivery (USB-PD) adapters, for example.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power Management

The UCC24612 SR controller is powered from REG pin through the internal linear regulator between VDD pin and REG pin. This configuration allows optimal design of the gate driver stage to achieve fast driving speed, low driving loss and higher noise immunity.

In low-side SR configuration, as shown in Figure 13, the UCC24612 is powered from the output voltage directly.

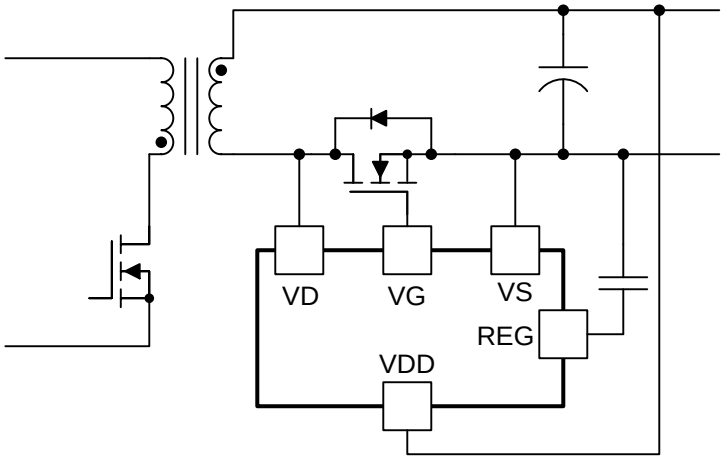


Figure 13. UCC24612 Used in Low-side SR Configuration

During start up, the output voltage rises from zero. With the rising of output voltage, the internal linear regulator operates in a pass-through mode, and the REG pin voltage rises together with the output voltage. The UVLO function of UCC24612 monitors the voltage on the REG pin instead of the VDD pin. Before REG pin voltage rises above UVLO on threshold $VREG_{ON}$, UCC24612 consumes the minimum current $IVDD_{START}$. Once the REG voltage rises above $VREG_{ON}$, the device starts to consume the full operating current and controls the switching of the SR MOSFET.

When VDD voltage is above 9.5 V, the internal linear regulator operates in regulator mode. The REG pin is well regulated at 9.5 V. This voltage level is chosen to give a good compromise between SR conduction loss and gate drive loss. The internal regulator is rated at 10 mA of average load regulation capability for higher switching frequency operation. It is required to have a sufficient bypass capacitor on the REG pin to ensure stable operation of the linear regulator. A 2.2-µF bypass capacitor is recommended.

When VDD voltage is below 9.5 V, the internal linear regulator operates in pass-through mode. Depending on the load current, the regulator has a voltage drop of approximately 0.2 V. The UCC24612 continues to operate during this mode until the REG pin voltage drops below UVLO turn off level $VREG_{OFF}$.

A typical timing diagram of VDD and REG pin voltage can be found in Figure 14.

Feature Description (continued)

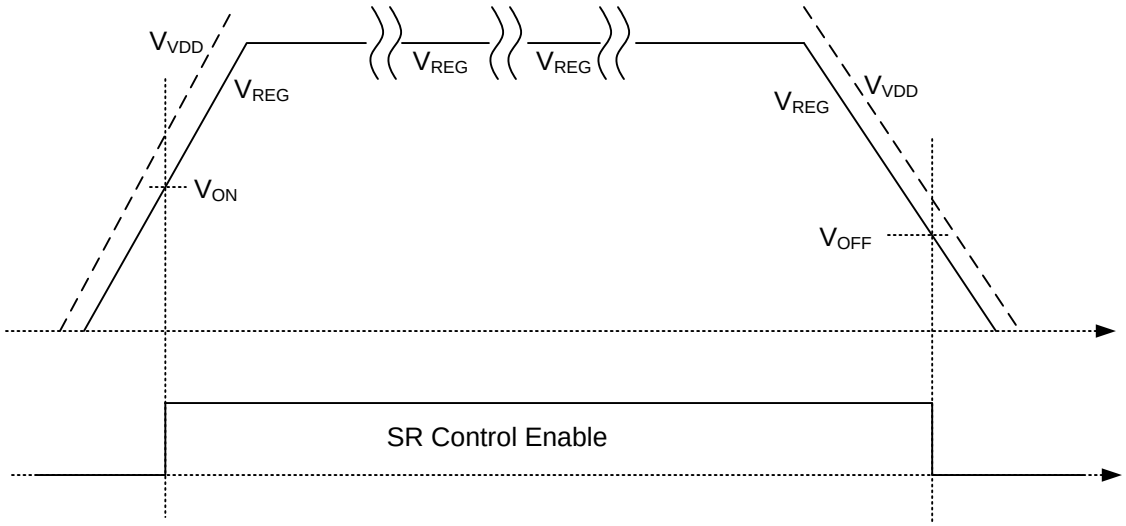


Figure 14. Timing Diagram for VDD and REG in Low-side SR Configuration

In some applications, such as USB chargers, the converter is required to deliver the full output current when the output is over loaded and output voltage drops below the regulation level. In 5-V applications, the output voltage could drop too low to adequately turn on the SR. In this case, the UCC24612 can be powered through a simple external R-C-D circuit, as shown in Figure 15. Due to the wide voltage range handling capability, this simple circuit provides power from the SR drain voltage. Even though this method easily powers up the device, this is a very inefficient way of powering the controller. A more efficient way would be to use an auxiliary winding to provide the power.

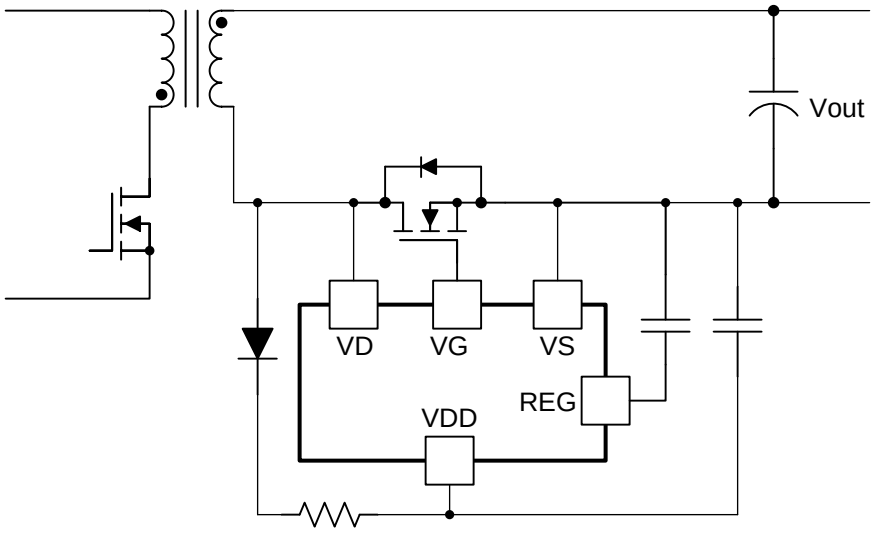


Figure 15. UCC24612 Used in Low-side and Low Output Voltage Condition

The same biasing method can also maintain the SR controller operation in high-side SR configuration, as shown in Figure 16. More details about biasing UCC24612 can be found in Power Supply Recommendations.

Feature Description (continued)

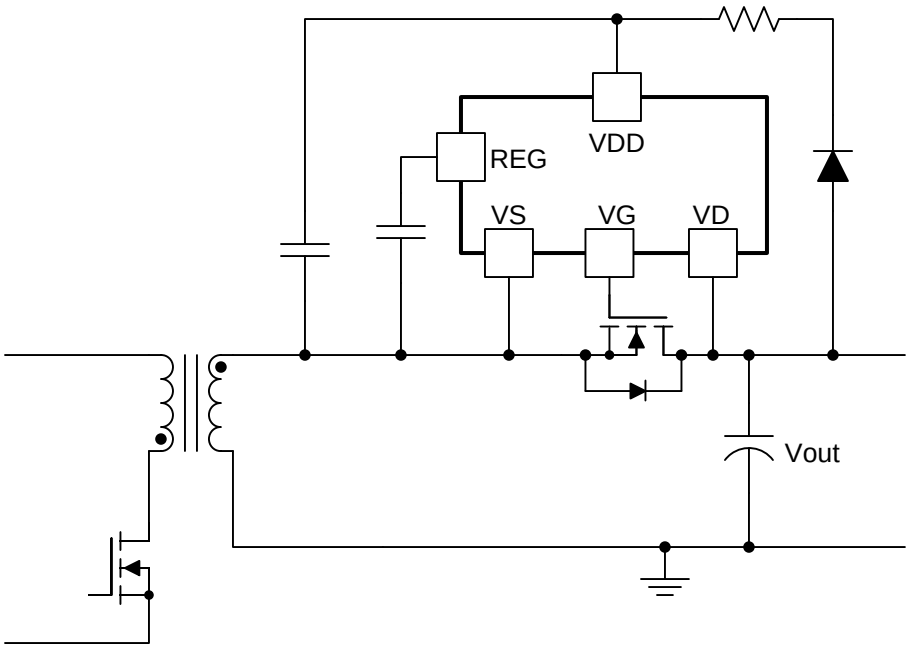


Figure 16. UCC24612 Used in High-Side SR Configuration

7.3.2 Synchronous Rectifier Control

The UCC24612 SR controller determines the conduction time of the SR-MOSFET by comparing the drain-to-source voltage (Vds) of the MOSFET against a turn-on threshold and a turn-off threshold. The VG output is driven high when V_{DS} of the MOSFET falls below V_{THVGON} and is driven low when V_{DS} rises above $V_{THVGOFF}$ as illustrated in Figure 17. Since when SR is conducting, its drain to source voltage (V_{DS}) is negative, more negative voltage drop means higher SR current.

Feature Description (continued)

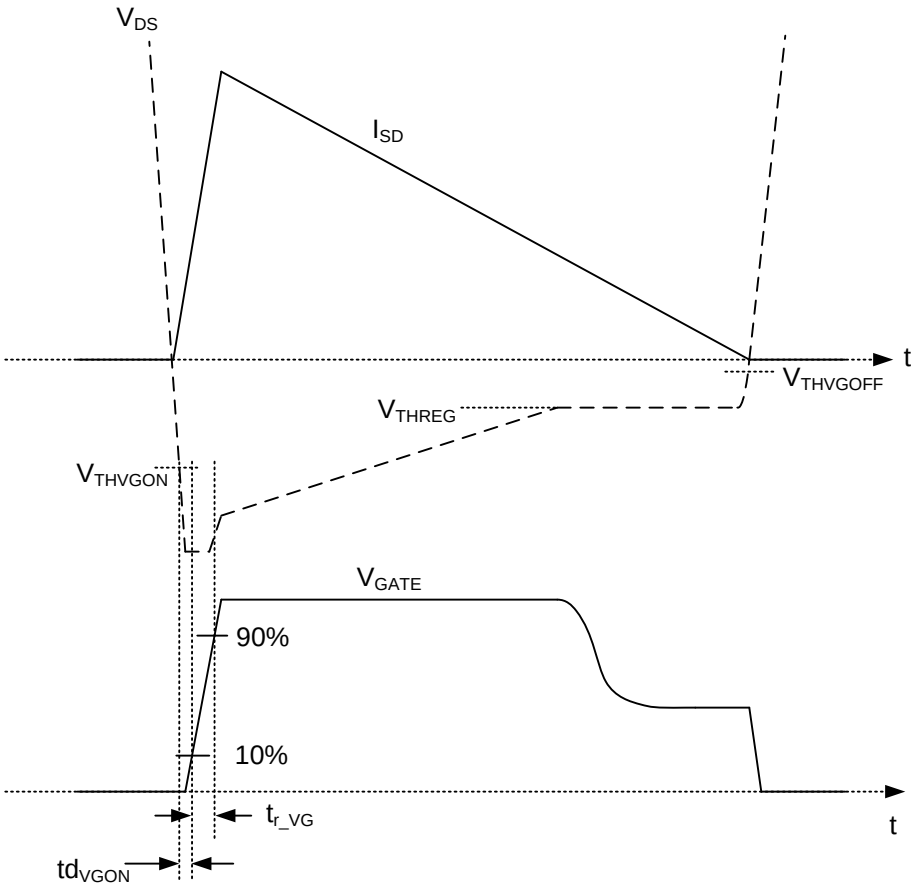


Figure 17. VG Output With Respect to V_{DS}

NOTE

Because of finite propagation delay and rise times, the body diode of the SR-MOSFET may conduct briefly after V_{THVGON} has been exceeded. A waveform similar to that depicted in Figure 17 can be observed during SR operation in a simple Flyback circuit.

It should be noted that before the SR turns on, there is a small delay caused by the internal comparator delay and the gate driver delay. During the delay time, the SR MOSFET body diode is conducting. For a Flyback converter, the SR current is at its maximum value during this delay time. It is desirable to have minimum delay. The gate driver design should avoid long turn-on delay.

For certain applications, this delay is essential for correct operation. In Active Clamp Flyback converters, especially when the primary-side switches are using Si-based super-junction MOSFETs, due to the large nonlinear junction capacitance, the SR often sees a leading spike current, followed by the real conduction current. Typically, a longer minimum on-time can override this spike to make the circuit operate normally. However, this forced minimum on-time can allow current that transfers the energy from output to input and reduces the overall converter efficiency. In UCC24612, two different versions are available. UCC24612-1 has an inherently short turn-on propagation delay (80 ns typical) and can be used with the converters that need shorter delay, such as standard Flyback converters or Active Clamp Flyback converters using GaN MOSFETs as main switches. UCC24612-2 has a longer 170-ns turn-on delay, to further ignore the leading edge spike and can be used with Active Clamp Flyback using Si-based super-junction MOSFETs as the main switch or LLC converters. Due to the longer turn-on delay, UCC24612-2 also increases its minimum on time-to 540ns to allow further enhancement on dealing with resonant-shape current, which makes a better choice for Si-based super-junction MOSFETs as the main switch or LLC converters.

Feature Description (continued)

When the SR body diode is conducting, the VD pin becomes negative with respect to the VS pin, by a body-diode drop. The connections of VD and VS pins should be tracked directly to the SR MOSFET pins, to avoid any overlap of sensing and power paths, minimizing the negative voltage and ringing caused by the parasitic inductances. Low package inductance MOSFETs are preferred to minimize this effect.

Besides the simple comparator, UCC24612 also includes a proportional gate driver for the SR. For conventional SR control, the SR MOSFET is always driven to the full driving voltage. This minimizes the conduction loss. However, this method has some major drawbacks. The turn-off threshold is often a fixed value, to prevent shoot-through, so that the SR is turned off before its current reaches zero. This causes SR body diode conduction and actually increases the conduction loss. Another issue is associated with operation in continuous conduction mode (CCM) condition. When a Flyback converter operates in CCM, the SR current slope (di/dt) at turn-off could be as high as 150 A/µs. This high current slope could cause large negative current due to long propagation delay. Furthermore, the delay caused by discharging the SR MOSFET gate from full voltage to its threshold level introduces another delay, further increasing the negative current.

Instead of keeping the SR MOSFET turned on with full gate driver voltage, UCC24612 reduces its gate driver voltage when the voltage drop across SR drain-to-source reaches -50 mV (current approaching zero). During this time, UCC24612 tries to regulate the SR voltage drop to -50 mV. This brings two major benefits to the application: a) Preventing the SR premature turn-off, avoiding extra loss associated with body diode conduction and reverse recovery, b) Shorter turn-off delay since the SR MOSFET gate voltage is already reduced close to the threshold level and the SR can be turned off with virtually no further delay. Since the -150 mV is the maximum level that can be achieved by the UCC24612, the SR MOSFET selection should allow the -150-mV threshold to be activated when operating in deep CCM condition.

In certain applications, such as telecom DC/DC bricks, due to the lower input and output voltages, operation in deep CCM mode (low inductor current ripple) gives the benefit of less conduction loss. In these applications, the SR turn-off current is high and the SR MOSFET voltage drop can still be less than the -50-mV threshold. UCC24612 decreases the -50-mV threshold to -150 mV to force proportional drive activation and reduction of the gate driver voltage for a fast turn-off. The timing to decrease the threshold is based on previous cycle SR conduction time. Because the regular proportional gate drive and the turn-off mechanism are kept functional continuously, the UCC24612 can still provide correct SR control even for a large SR conduction time change within two switching cycles. The forced proportional gate drive mechanism can be shown in Figure 18. In Figure 18, the turn on delay was ignored to simplify the illustration.

Feature Description (continued)

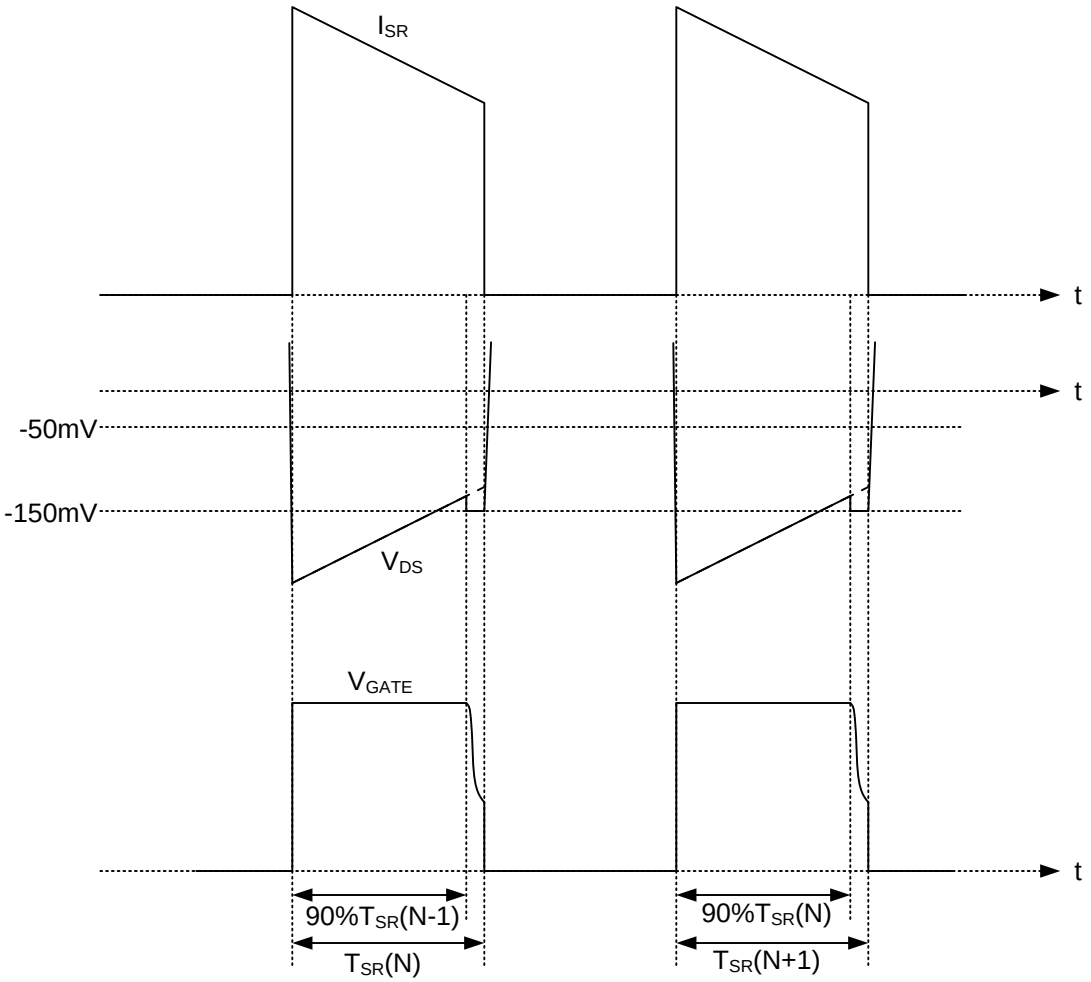


Figure 18. Forced Proportional Gate-Drive for Deep CCM Operation

For Flyback converters, the SR current starts from its maximum amplitude and keeps reducing. Proportional gate drive is only enabled at the later part of the SR current conduction period. However, for other topologies such as LLC or Active Clamp Flyback, the SR current starts from lower amplitude and then increases to a higher amplitude. To prevent the proportional gate drive from being enabled at the beginning of the conduction period, proportional drive is disabled for the first 50% of the SR conduction time, based on the previous cycle SR conduction time. In this way, the proportional drive is always enabled on the current falling slope and minimizes impact on the conduction loss.

Feature Description (continued)

7.3.3 Adaptive Blanking Time

In power converters, the sensed the voltage across the SR is often noisy, caused by the parasitic ringing. This parasitic ringing is often associated with the SR and the primary-side switch turning on and off. Blanking time is used to deal with the parasitic ringing to prevent SR false turn on and off. Figure 19 shows more realistic waveforms and the internal control timing which accommodates them.

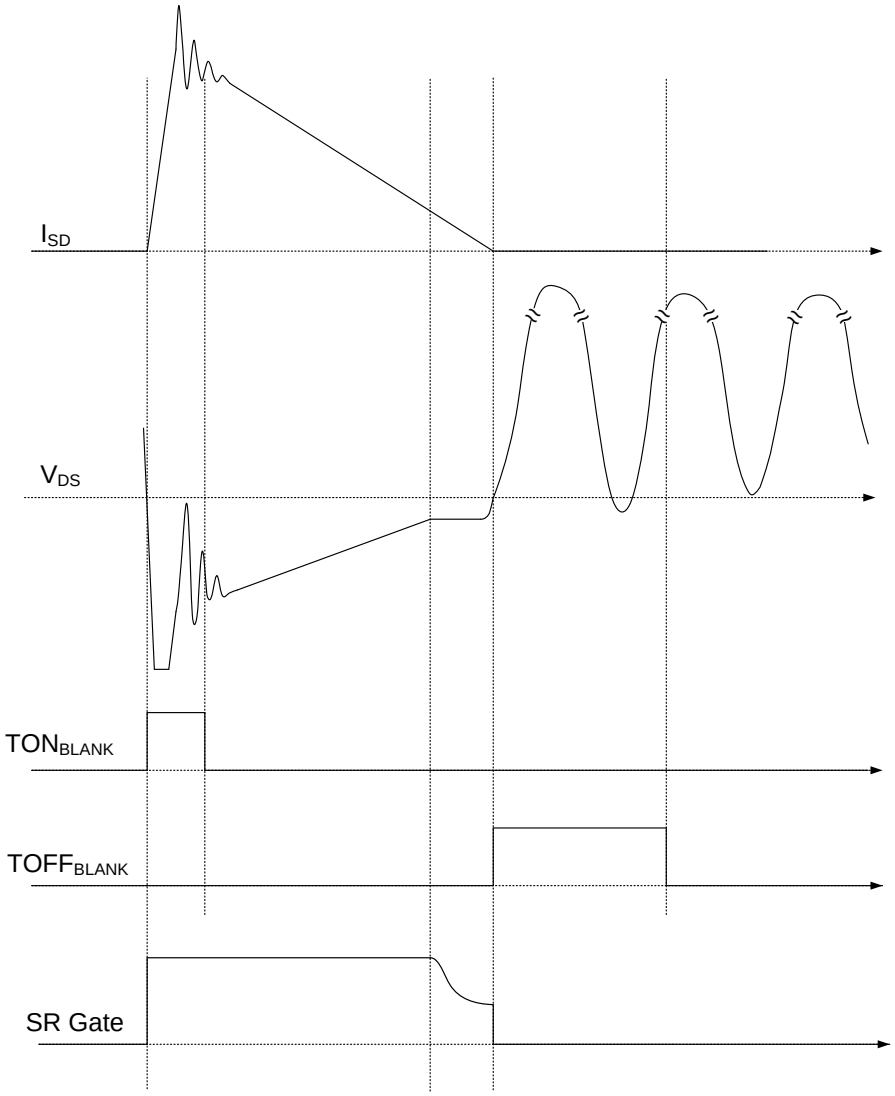


Figure 19. Parasitic Ringing Associated with DCM Operation

Feature Description (continued)

7.3.3.1 Turn-On Blanking Timer (Minimum On Time)

Right after SR turn-on, for some topologies, such as Flyback, the SR starts to conduct with its maximum current. Due to the parasitic ringing, SR sensed voltage drop may trip the turn-off threshold and prematurely turn off the SR. This is largely caused by the ringing due to the package inductance of the SR MOSFET. The ringing voltage can be managed through appropriate snubbing and use of low package inductance MOSFETs. To further improve the noise immunity, UCC24612-1 blanks the turn-off comparator with a fixed 360-ns (540 ns for UCC24612-2) minimum on-time timer. The SR needs to conduct a minimum of 360 ns (540 ns for UCC24612-2) regardless of its turn-off comparator state. The minimum on-time is short enough to allow the UCC24612 to be used at up to 1 MHz switching frequency (1 MHz for UCC24612-1 and 800kHz for UCC24612-2), while still maintaining good noise immunity. Due to the different applications, the minimum on-time is set up differently for UCC24612-1 and UCC24612-2. For UCC24612-1, the minimum on-time is 360 ns and for UCC24612-2, the minimum on-time is 540 ns.

7.3.3.2 Turn-Off Blanking Timer

When the converter operates in discontinuous conduction mode (DCM) or burst mode, after SR turn-off, there is a large parasitic DCM ring caused by the primary inductance and the switch node capacitance. For the first couple of ringing cycles, there is a possibility that the drain voltage can resonate below the SR turn-on threshold. The SR could be falsely turned on at these instances and introduce extra loss and EMI noise.

The DCM ringing is blanked by an off blanking timer. It is often called minimum off-time. Due to the range of switching frequencies and power levels, the parasitic ringing frequency can vary substantially. The programmable off blanking timer provides maximum flexibility for the circuit design and avoids false triggering. However, there are some limitations associated with this method. Firstly, the need for a programming pin can force a higher pin count package, which increases the overall cost and difficulty of layout. Secondly, a fixed off blanking timer might not work well for the entire range of line and load conditions. For example, for a quasi-resonant (QR) Flyback, in light load mode, it enters DCM operation. In this case, the off blanking timer should be long to avoid DCM ringing induced SR false turn on. However, at high input voltage, when the converter operates in QR mode, the primary side MOSFET conduction time is quite short, and long minimum off-time might cut into the conduction time of the SR, introducing extra conduction loss.

In UCC24612, instead of a fixed off blanking timer, an adaptive off blanking timer is used to blank the parasitic ringing and avoid false turn-on. The off blanking timer $TOFF_{blank}$is determined by the maximum value of three timings, the absolute minimum off blanking time of 400 ns (t_{OFF_ABSMIN}), the recorded DCM ring cycle time t_{DCM} and the previous cycle's SR off time t_{OFF}.

UCC24612 sets up the off blanking timer based on the previous cycle SR off time. By choosing 70% of previous switching cycle's SR off time, the off blanking timer is maximized to prevent any false triggering.

However, the off blanking timer minimum value is clamped by the 400-ns absolute minimum value and recorded DCM ringing cycle.

The adaptive off-time blanking operation principle is illustrated in Figure 20.

Feature Description (continued)

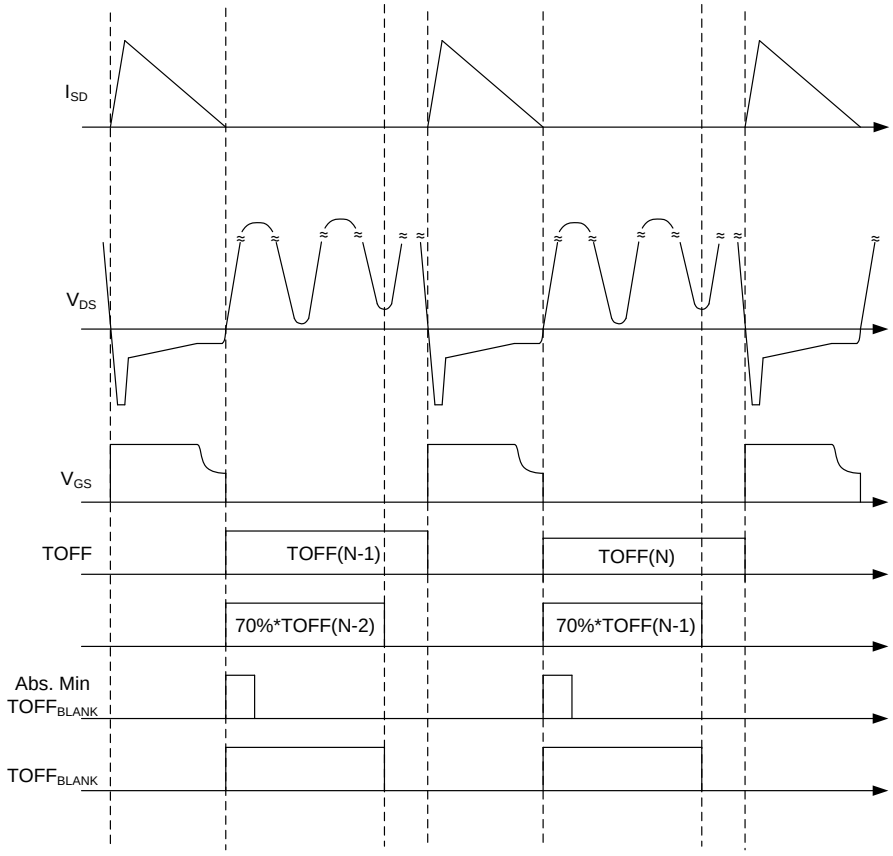


Figure 20. Operation Principle of Adaptive off-blanking

After SR turn-off, if the off blanking time is not sufficient, the SR could be turned on again by a DCM ring. Because of the DCM ring, the SR conduction time is limited by its minimum on-time. By looking at the SR conduction time and comparing it with the minimum on time, UCC24612 is able to determine if the conduction is a real SR conduction or a false turn on triggered by the DCM ring. A real SR conduction should demand the conduction time longer than the minimum on-time. Once the false turn-on is captured, the time duration between previous SR turn-off and the SR false turn-on is recorded as the DCM ring cycle. For the next switching cycle, the off blanking timer is clamped to 2.2 times of the recorded DCM ring cycle. This clamp replaces the 350-ns clamp as the new minimum clamp for the adaptive-off blanking. This adaptive off-blanking timer allows UCC24612 achieving the noise immunity without a dedicated programming pin. The DCM ring clamp is illustrated in Figure 21.

Feature Description (continued)

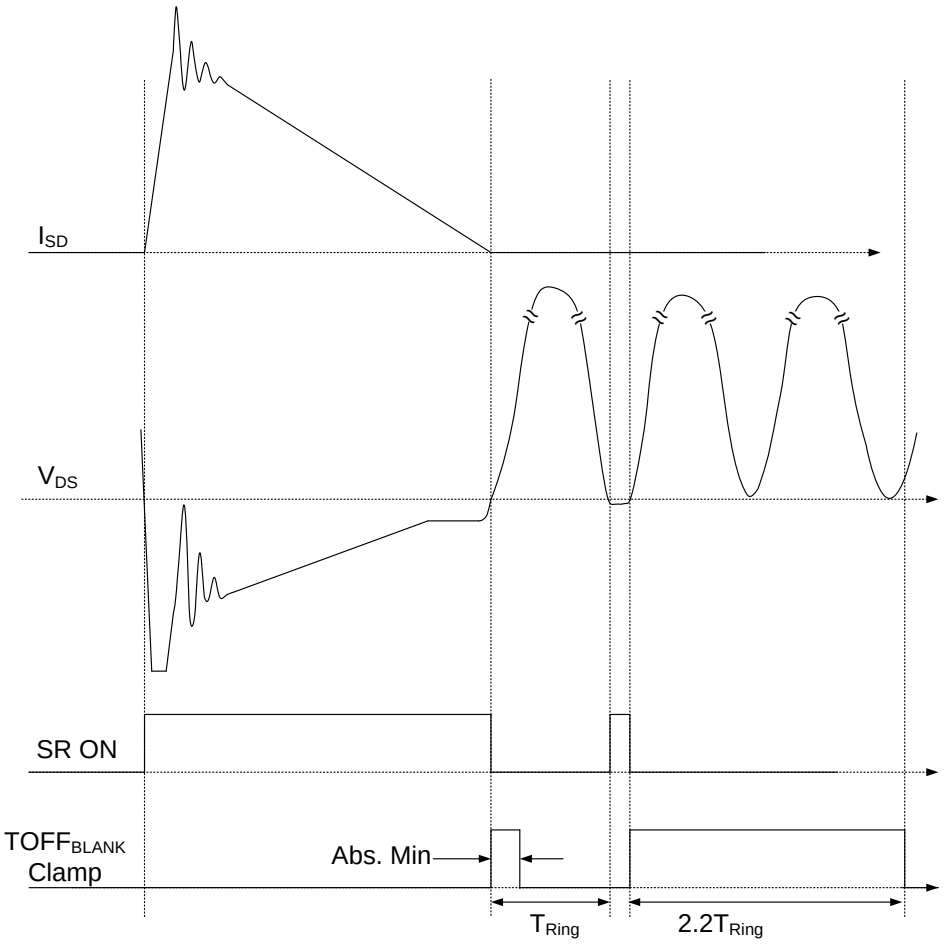


Figure 21. Adaptive Off-Time Blanking with DCM Ring Clamp

For some conditions, as mentioned earlier, the off blanking timer suitable for DCM operation might be too long for high-line QR operation. In this case, the off blanking timer clamp needs to be reset to the correct value. UCC24612 continuously monitors the SR body diode conduction time during minimum off-time. If the body diode conduction time is longer than the minimum on-time, this means the minimum off blanking time clamp setting is too long and needs to be reduced. UCC24612 resets the minimum off blanking time clamp to the absolute minimum of 400 ns to allow full conduction of the SR on the subsequent cycles.

If for any reason the off blanking time expires after the SR body diode conduction, the SR turn-on is skipped for the switching cycle. This is because when the SR conducts, it conducts with a minimum on-time, if the blanking time expires at the end of the SR conduction time and converter operates in the CCM condition, there is a good chance to cause shoot-through and endanger the converter.

The off blanking time has a maximum value of t_{OFF_MAX} at 3.68 µs.

Feature Description (continued)

7.3.3.3 SR Turn-on Re-arm

The VG output may only turn on when the controller has been armed for the next switching cycle. The controller is armed for each successive SR cycle only after $TOFF_{BLANK}$ expires. The $TOFF_{BLANK}$ timer only starts after VD pin voltage rises 500 mV above the VS pin.

7.3.4 Gate Voltage Clamping

With the wide VDD voltage range capability, UCC24612 clamps the gate driver voltage to a maximum level of 9.5 V to allow fast driving speed, low driving loss and compatibility with different MOSFETs. The 9.5-V level is chosen to minimize the conduction loss for the non-logic level MOSFETs.

The gate driver voltage clamp is achieved through the regulated REG pin voltage. When VDD voltage is above 9.5 V, the linear regulator regulates the REG pin voltage to be 9.5 V, which is also the power supply of the gate driver stage. This way, the MOSFET gate is clamped at 9.5 V, regardless of how high the VDD voltage is. When the VDD voltage is close to or below the programmed REG pin regulation voltage, UCC24612 can no longer regulate the REG pin voltage. Instead, it enters a pass-through mode where the REG pin voltage follows the VDD pin voltage with slight voltage drop out ($VREG_{DO}$). During this time, the gate driver voltage is lower than its programmed value but still provides SR driving capability. The UCC24612 is disabled once the REG pin voltage drops below its UVLO level.

7.3.5 Standby Mode

With more stringent efficiency standards such as Department of Energy (DoE) level VI, external power supplies are expected to maintain very low standby power at no-load conditions. It is essential for the SR controller to enter the low-power standby mode to help save standby power.

During standby mode, the power converter loss allocation is quite different compared to heavy load. At heavier load, both conduction loss and switching loss are quite high. However, at light load, the conduction loss becomes insignificant and switching loss dominates. To help improve standby power, modern power supply controllers often enter burst mode to save switching loss. Furthermore, in each burst switching cycle, the energy delivered is maximized to minimize the number of switching cycles needed and further reduce the switching loss.

Traditionally, the SR controller monitors the SR conduction time to distinguish normal operating modes from standby mode. This criterion is no longer suitable for the modern power supply controller designed for delivering minimum standby power.

Instead, in UCC24612, a frequency based standby mode detection is used. UCC24612 continuously monitors the average switching frequency of the SR. Once the average switching frequency of the SR controller drops below 12 kHz, the UCC24612 enters standby mode and reduces its current consumption to $IVDD_{STBY}$. During standby mode, the VG pin is kept low while the SR switching cycle is continuously monitored. Once the average switching frequency is more than 15 kHz over a 4.5-ms window, the SR operation is enabled again. UCC24612 ignores the first six SR switching cycles after coming out of standby mode to make sure the SR isn't turned on in the middle of the switching cycle.

7.4 Device Functional Modes

7.4.1 UVLO Mode

UCC24612 uses the REG pin voltage to detect UVLO instead of the VDD pin voltage. When the REG voltage to the device has not yet reached the V_{REGON} threshold, or has fallen below the UVLO threshold V_{REGOFF}, the device operates in the low-power UVLO mode. In this mode, most internal functions are disabled and VDD current is $IVDD_{start}$, typically less than 120 µA. If the REG pin is above 2 V, there is an active pull-down from VG to VS to prevent SR turn-on due to noise. When the REG pin voltage is less than 2 V, there is a weak pull down from VG to VS and this also helps prevent false turn on of the SR MOSFET. The device exits UVLO mode when REG increases above the V_{REGON} threshold.

7.4.2 Standby Mode

Standby mode is a low-power operating mode to help achieve low standby power for the entire power supply. UCC24612 detects the operating frequency of the SR MOSFET and enters or exits standby mode operation automatically. REG current reduces to $IVDD_{STBY}$ level. During standby mode, the majority of the SR control functions are disabled, except the switching frequency monitoring, REG monitoring and the active pull-down on the gate driver.

7.4.3 Run Mode

Run mode is the normal operating mode of the controller when not in UVLO mode or standby mode. In this mode, REG current is higher because all internal control and timing functions are operating and the VG output is driving the MOSFET for synchronous rectification. REG current is the sum of $IVDD_{RUN}$ plus the average current necessary to drive the load on the VG output. The VG voltage is automatically adjusted based on the SR MOSFET drain to source voltage according to the proportional gate drive operation.

8 Application and Implementation

NOTE

Information in the following application sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC24612 synchronous rectifier controller is designed to control an SR MOSFET to replace a lossy diode rectifier to improve the efficiency in various topologies, such as Active Clamp Flyback, Flyback operating in DCM, QR or CCM mode, as well as LLC resonant converters.

8.2 Typical Application

The following application information is applied to the UCC24612 Evaluation Module (EVM), which is used as a rectifier stage in a 20-V, 60-W DCM Flyback design. The controller used in this design is a UCC28740 secondary side regulated, variable-frequency Flyback controller that has a maximum switching frequency of 85 kHz. Please refer to the UCC28740 data sheet for further details.

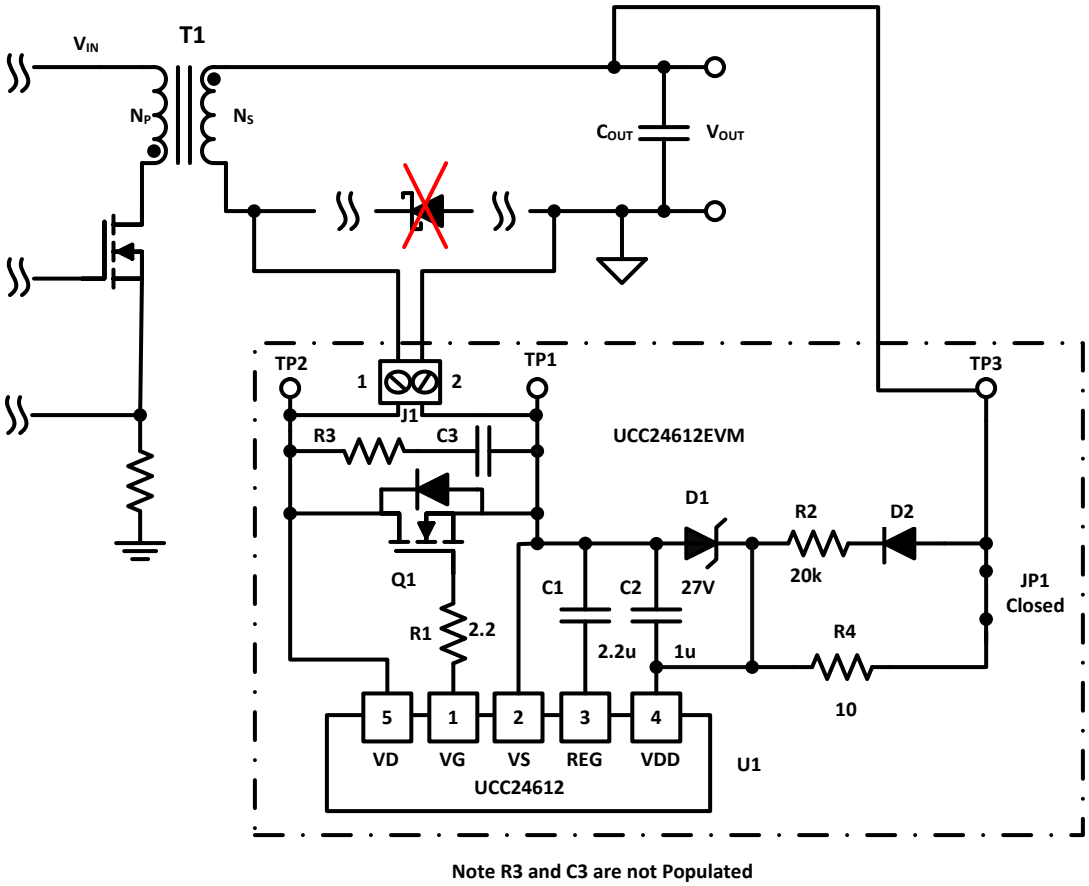


Figure 22. UCC24612 Typical Application Example

Typical Application (continued)

8.2.1 Design Requirements

Table 2. 60-W DCM Flyback Design Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CHARACTERISTICS						
V_{IN}	Input voltage		85		265	V_{RMS}
OUTPUT CHARACTERISTICS						
V_{OUT}	Output voltage, average	V_{IN} = 85 V_{RMS} to 265 V_{RMS}, I_{OUT} = 0 A to 3 A	19	20	21	V
I_{OUT}	Output current	V_{IN} = 85 V_{RMS} to 265 V_{RMS}	0		3	A

8.2.2 Detailed Design Procedure

8.2.2.1 SR MOSFET Selection

UCC24612 can be paired with an appropriate MOSFET to replace the diode rectifier on existing designs and demonstrate significant conduction loss reduction. The SR MOSFET selection should consider the tradeoff between cost and performance. Lower on-state resistance gives lower conduction loss, while it reduces the efficiency at light load. Due to the unique implementation of proportional gate drive, the benefit of lower on-state resistance is diminished. It is recommended to select the MOSFET on-state resistance so that the proportional gate drive operates for less than 50% of the full load SR conduction time.

According to UCC28740 datasheet, for 3-A output DCM Flyback design, the secondary side peak current should be about 14 A. To allow the proportional gate drive operating less than 50% of the SR conduction time, SR MOSFET Rdson should be more than 7 mΩ , according to .

$$Rdson > \frac{50mV}{14A/2} \approx 7m\Omega \tag{1}$$

The MOSFET breakdown voltage should be higher than the maximum voltage the SR MOSFET sees under maximum input voltage. For this design, the transformer turns ratio is 3.5, the voltage stress on the SR can be calculated as in Equation 2.

$$Vds(\max) = \frac{\sqrt{2}V_{IN\max}}{N_{PS}} + V_{OUT} = \frac{\sqrt{2}\times 265V}{3.5} + 20V = 127V \tag{2}$$

In this EVM, a 150-V, 19-mΩ MOSFET is used to get a balance between the cost and performance.

8.2.2.2 Bypass Capacitor Selection

UCC24612 needs a sufficient external bypass capacitance to ensure the internal regulator stability. Referring to the power supply recommendation section, a 2.2-µF 50-V ceramic capacitor was chosen as the bypass capacitor on REG pin. For the VDD pin, it is normally powered by the output voltage and there is plenty of capacitor there. A 0.1-µF ceramic capacitor is still recommended to be placed close to the IC to provide high frequency current.

8.2.2.3 Snubber design

It is required for the user to setup snubber components C3 and R3 to get the best performance when using the UCC24612EVM.

To setup these components will require knowledge of the Flyback transformer secondary leakage inductance (Lslk) and measuring the secondary resonant ring frequency (fr) in circuit. It is recommended that the SR is not driven while doing this to simplify the process. It is also recommended to do this test at partial load to avoid creating too much heat on the SR body diode because the conduction loss is much higher. TP3 should be disconnected from the Flyback converter to ensure FET Q1 is turned off while setting up the snubber.

The secondary winding capacitance (Cs) then needs to be calculated based on the following equation. Please note for a transformer with a secondary winding leakage inductance of 3.8 µH and a ring frequency of 2 MHz, the parasitic capacitance would be 1.7 nF, for example.

$$C_S = \frac{1}{(2 \times \pi \times f_r)^2 \times Lslk} = \frac{1}{(2 \times \pi \times 2MHz)^2 \times 3.8\mu H} = 1.7nF \quad (3)$$

Based on the calculated Cs, Lslk and fr, the snubber resistor R3 can be set to critically dampen the ringing on the secondary, which requires setting the Q of the circuit equal to 1.

$$R3 = \frac{1}{Q}\sqrt{\frac{Lslk}{Cs}} = \frac{1}{1}\sqrt{\frac{3.8\mu H}{1.7nF}} \approx 47\Omega \quad (4)$$

Capacitor C3 is used to limit the time the snubber resistor is applied to the aux winding during the switching cycle. It is recommended to set the snubber capacitor C3 with the following equation based on the Flyback converters switching frequency (f_{SW}). For a Flyback converter switching at 85 kHz in the example would require a C3 of roughly 497 pF.

$$C3 = \frac{0.01}{5 \times fsw \times R3} = \frac{0.01}{5 \times 85kHz \times 47\Omega} \approx 497\,pF \quad (5)$$

Please note that the calculations for R3 and C3 are just starting points and should be adjusted based on individual preference, performance and efficiency requirements. More snubber design information can be found in "Snubber Circuits Theory, Design and Application".

8.2.2.4 High-Side Operation

To use the UCC24612EVM to replace a high-side rectifier requires removing jumper JP1 and connecting the EVM as shown in Figure 23. Please note that the EVM comes with a default VDD filtering resistor (R2) of 20 kΩ. However, resistor R2 needs to be adjusted based on your individual application.

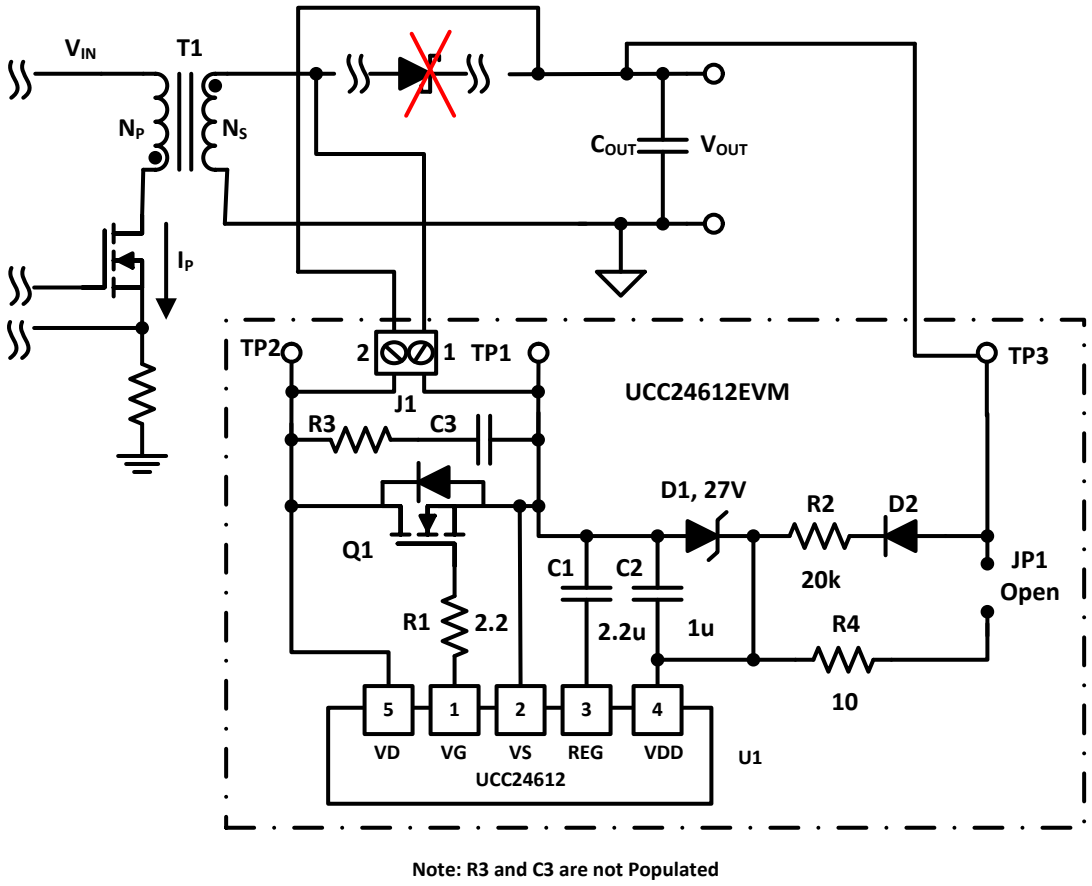


Figure 23. UCC24612-1EVM Used in High-Side Rectifier Application

If the magnitude of the voltage from TP2 to TP1 is less than 28 V, remove R2 that is populated on the EVM (20 kΩ) and set R2 to 0 to 10 ohms and remove 27-V Zener diode D1 from the board.

If TP2 to TP1 is greater than 28 V use resistor R2 to setup an averaging filter to lower the DC voltage applied to VDD.

The RC filter formed by C2 and R2 should set the filter pole frequency to one-hundredth of the converter's maximum switching frequency. In this example the converter's maximum switching frequency (f_{SW}) is 85 kHz. Note that the switching frequency will vary based on design and preference.

$$R2 > \frac{1}{2\pi \times C1 \times \frac{fsw}{100}} = \frac{1}{2\pi \times 1\mu F \times \frac{85kHz}{100}} \approx 187\Omega \tag{6}$$

When the RC filter circuit is used, it is recommended that the VDD voltage should be between 4 V to 28 V to provide enough energy and voltage to the gate driver. This range can be determined in a fixed frequency Flyback converter with the following equations. D_{MAX} is the maximum duty cycle of the converter and D_{MIN} is the minimum duty cycle of the converter. N_P is the Flyback transformer (T1) primary number of turns and N_S is the transformer secondary number of turns. Please refer to Figure 23 for details.

Maximum VDD voltage ($V_{VDD(MAX)}$):

$$V_{VDD(MAX)} = \left(V_{OUT} + V_{IN(MAX)} \times \frac{N_S}{N_P}\right) \times D_{MAX} = \left(20V + 375V \times \frac{1}{13}\right) \times 0.5 = 24.4V \tag{7}$$

Minimum VDD voltage ($V_{VDD(MIN)}$):

$$V_{VDD(MIN)} = \left(V_{OUT} + V_{IN(MIN)} \times \frac{N_S}{N_P}\right) \times D_{MIN} = \left(20V + 72V \times \frac{1}{13}\right) \times 0.36 = 9.2V \tag{8}$$

8.2.3 Application Curves

The UCC24612EVM is used as a synchronous rectifier in both a high-side and low-side configuration in an offline (VIN = 85 V to 265 V RMS), 20-V (VOUT), 60-W application. The primary-side controller used in this design is a UCC28740 secondary-side regulated, variable-frequency Flyback controller that had a maximum switching frequency of roughly 85 kHz. Please refer to the UCC28740 data sheet for further details.

8.2.3.1 Steady State Testing Low-Side Configuration

- Snubber Components, R2 = 1.02 kΩ, R3 = 51.1Ω , C3 = 470 pF
- CH1 = VG, CH2 = Q1 drain (TP2), CH3 = VOUT Voltage Ripple (TP3)

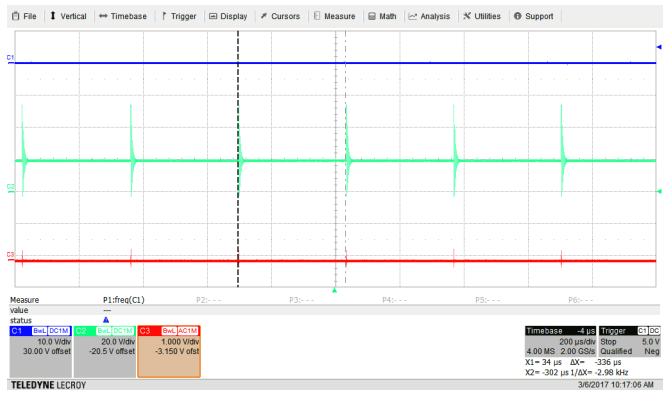


Figure 24. 85-V_{AC}, 0-A Load

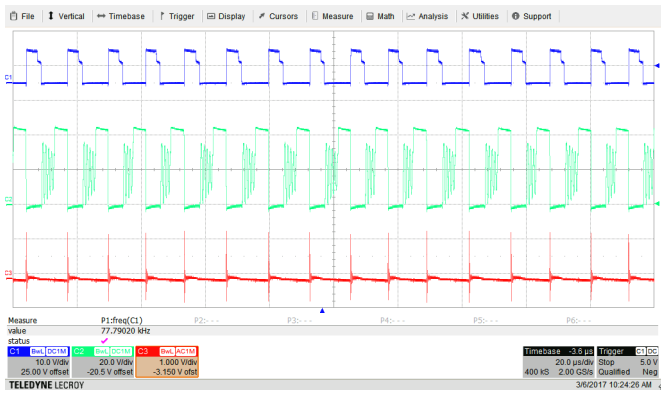


Figure 25. 85-V_{AC}, 3-A Load

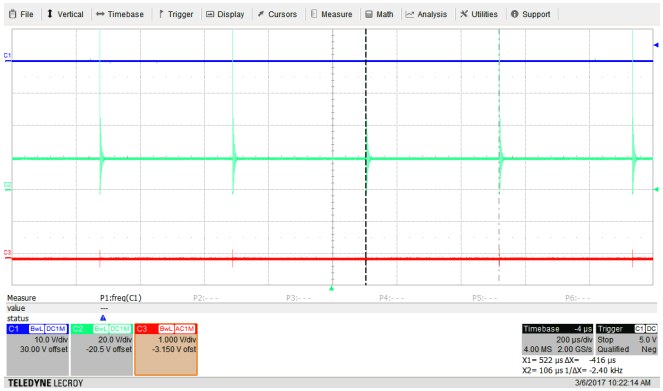


Figure 26. 265-V_{AC}, 0-A Load

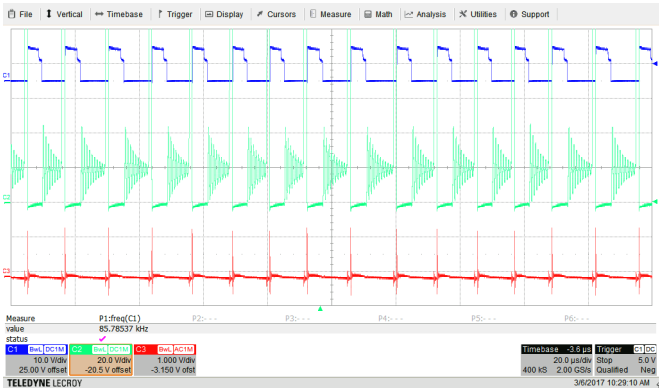


Figure 27. 265-V_{AC}, 3-A Load

8.2.3.2 Steady State Testing High-Side Configuration

- Snubber Components, R2 = 1.02 kΩ, R3 = 51.1 Ω , C3 = 470 pF
- CH1 = VG, CH2 = Q1 drain (TP2), CH3 = VOUT Voltage Ripple (TP3)

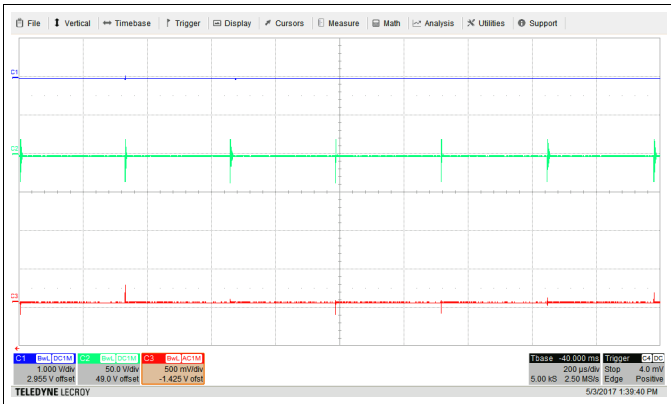


Figure 28. 85-V_{AC}, 0-A Load

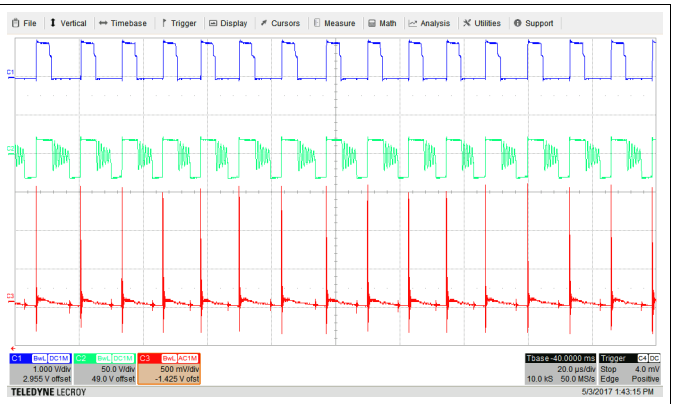


Figure 29. 85-V_{AC}, 3-A Load

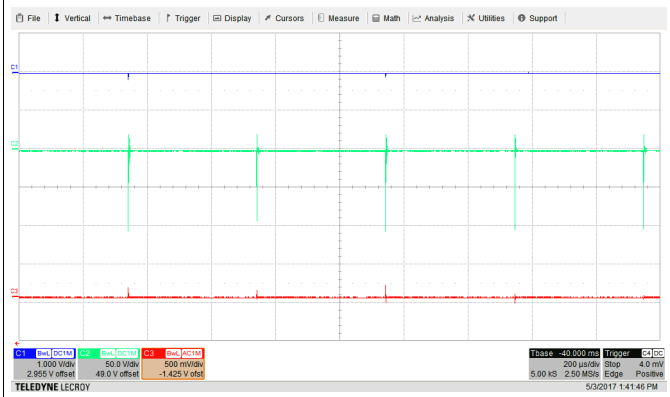


Figure 30. 265-V_{AC}. 0-A Load

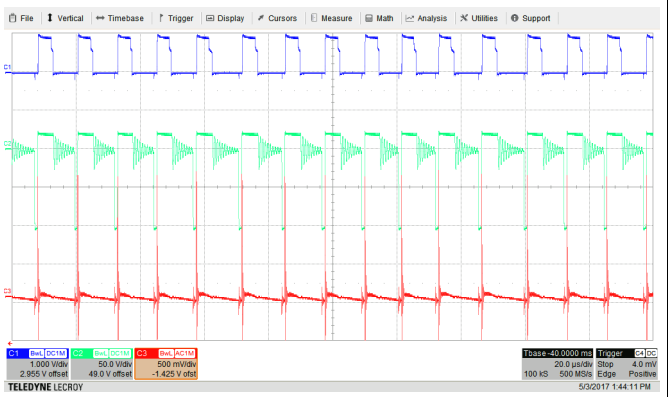


Figure 31. 265-V_{AC}, 3-A Load

9 Power Supply Recommendations

UCC24612 internal circuits are powered from the REG pin only. There is an internal LDO between VDD pin and REG pin to provide a well-regulated REG pin voltage when VDD voltage is above 9.5 V. This allows the device to have better bypassing and better gate driver performance.

It is important to have sufficient bypass cap on REG pin. A minimum of 1.5-µF bypass capacitor is required. When the average gate charge current is higher than 5mA, it is required to have at least 2.2-µF bypass capacitor on REG pin.

VDD pin is the main power source of the device. The voltage on VDD pin should be kept between 4.5 V and 28 V for normal operation. Refer to the electrical characteristics table for the tolerances on the REG pin UVLO ON and OFF levels.

When UCC24612 is used in low-side SR configuration, VDD can be directly tied to the output voltage if the output voltage is between 4.5 V to 28 V.

When the UCC24612 is used in high-side SR configuration, VDD can be powered through three different ways, with a trade off between cost and performance.

a. Power the device through secondary-side auxiliary winding
b. Power the device through simple R-C filter
c. Power the device through depletion mode FET

By using the secondary-side auxiliary winding, as shown in Figure 32, UCC24612 is equivalently powered by the output voltage because of the transformer coupling effect. This provides the best efficiency solution. However, this solution is often limited by the transformer construction and cost constraints.

The UCC24612 can be powered by using a diode and RC filter on VDD pin, as shown in Figure 33. This allows the device to get power from the SR drain voltage. Due to the wide range of VD voltage variation (for example, VD voltage is the sum of reflected input voltage and output voltage in Flyback converter), this may not be acceptable for some applications due to the limit of absolute maximum VDD voltage rating. However, this provides a simple and low cost solution.

A more universal solution without changing the transformer is to provide the VDD through SR drain using a diode and depletion mode MOSFET, as shown in Figure 34. This allows a well regulated VDD voltage throughout the entire operation range of the converter. Even though it still reducess the efficiency because the device is powered up from a high voltage source, this provides a simple solution without changing the transformer design.

The three different configurations are summarized in Figure 32, Figure 33 and Figure 34.

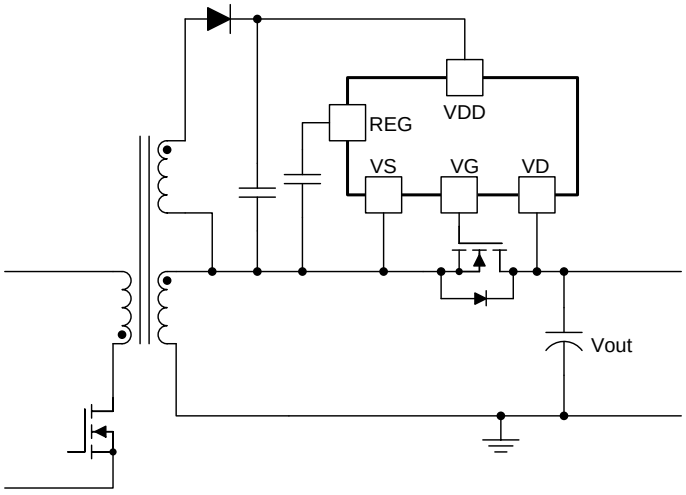


Figure 32. Power UCC24612 Using Auxiliary Winding

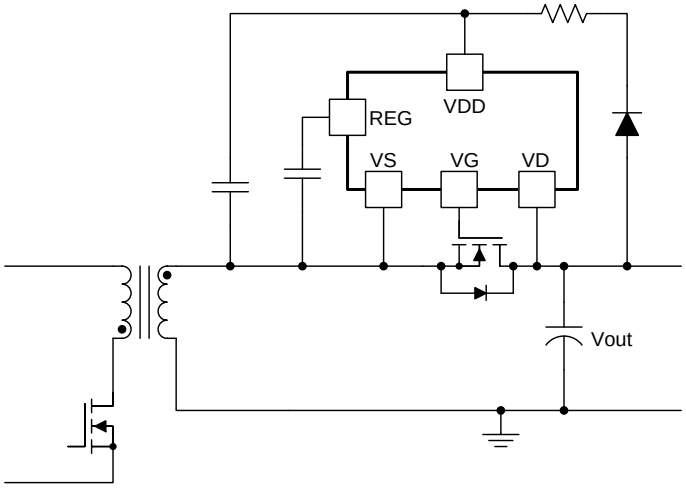


Figure 33. Power UCC24612 Using R-C-D

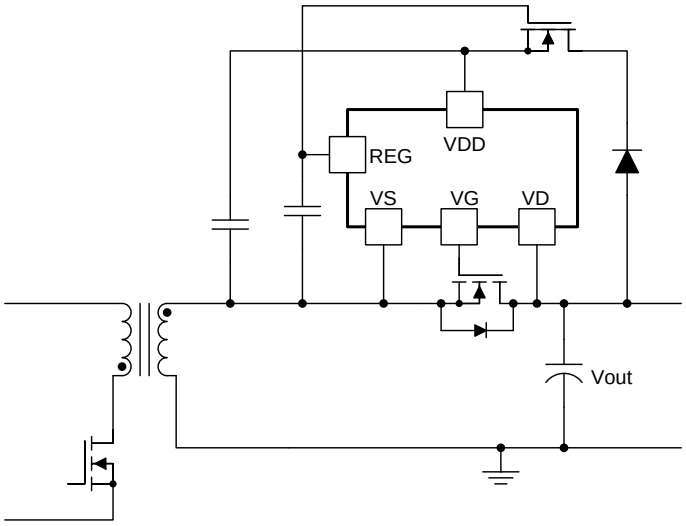


Figure 34. Powering UCC24612 Using Depletion Mode MOSFET

10 PCB Layout

10.1 Layout Guidelines

The printed circuit board (PCB) requires careful layout to minimize current loop areas and track lengths, especially when using single-sided PCBs.

- Place a ceramic MLCC bypass capacitor as close as possible between VDD and VS, and between REG and VS.
- Avoid connecting VD and VS sense points at locations where stray inductance is added to the SR MOSFET package inductance, as this will tend to turn off the SR prematurely.
- Run a track from the VD pin directly to the MOSFET drain pad to avoid sensing voltage across the stray inductance in the SR drain current path.
- Run a track from the VS pin directly to the MOSFET source pad to avoid sensing voltage across the stray inductance in the SR source current path. Because this trace shares both the gate driver path and the MOSFET voltage sensing path, it is recommended to make this trace as short as possible.
- Run parallel tracks from VG and VS to the SR MOSFET. Include a series gate resistor between VG and SR MOSFET gate pin to dampen ringing if it is needed.

10.2 Layout Example

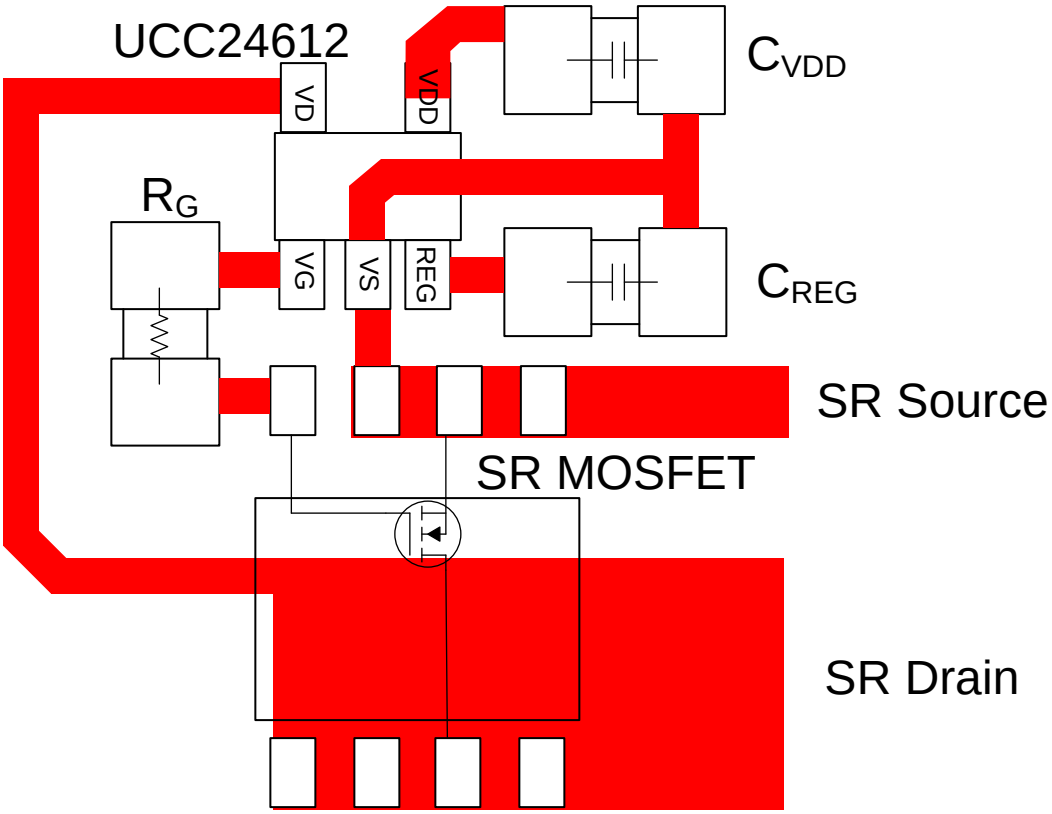


Figure 35. PCB Layout for Driving an SR with SO-8 Package

11 デバイスおよびドキュメントのサポート

11.1 コミュニティ・リソース

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11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC24612-1DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6121	Samples
UCC24612-1DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6121	Samples
UCC24612-2DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6122	Samples
UCC24612-2DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6122	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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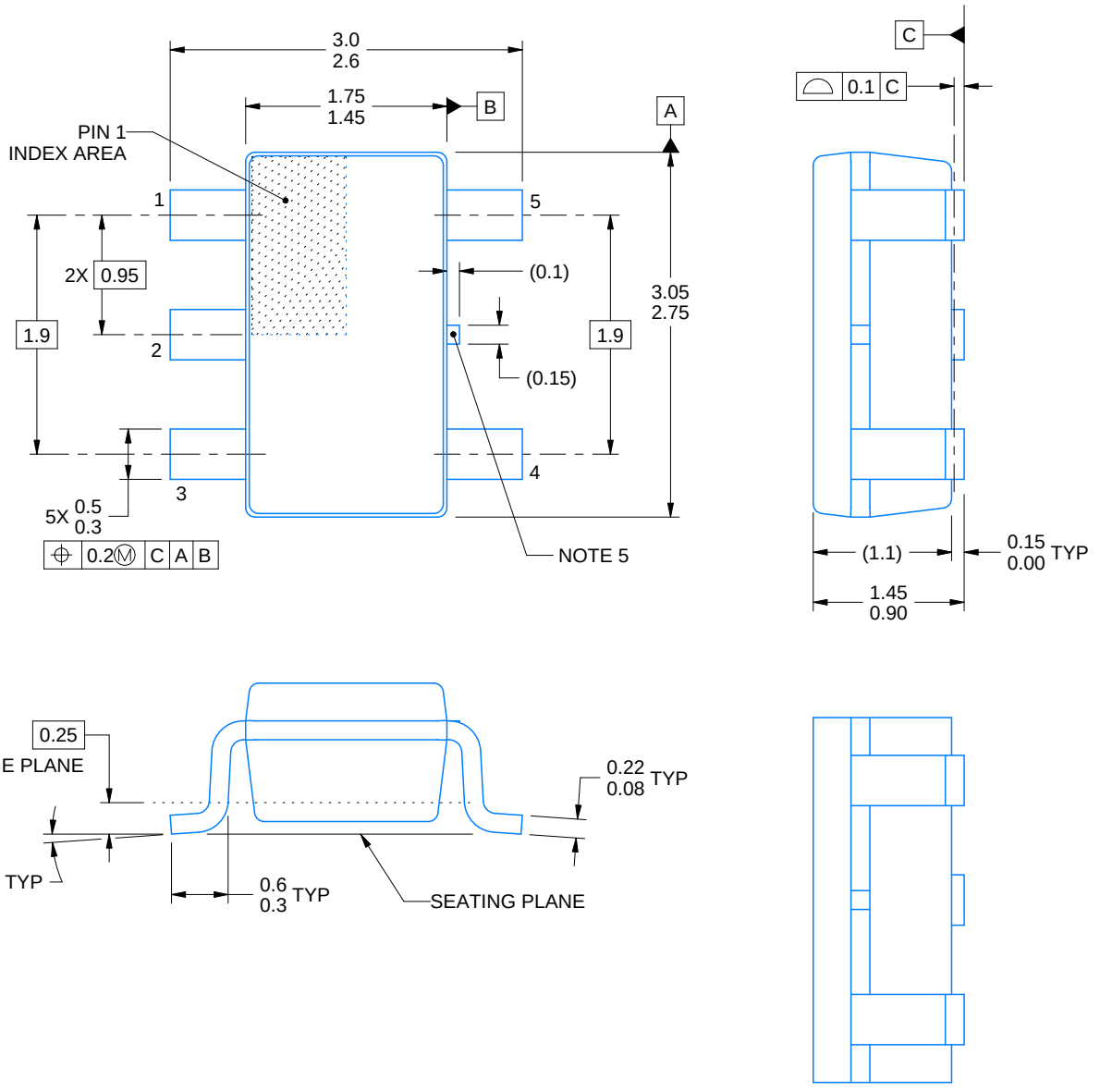
PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

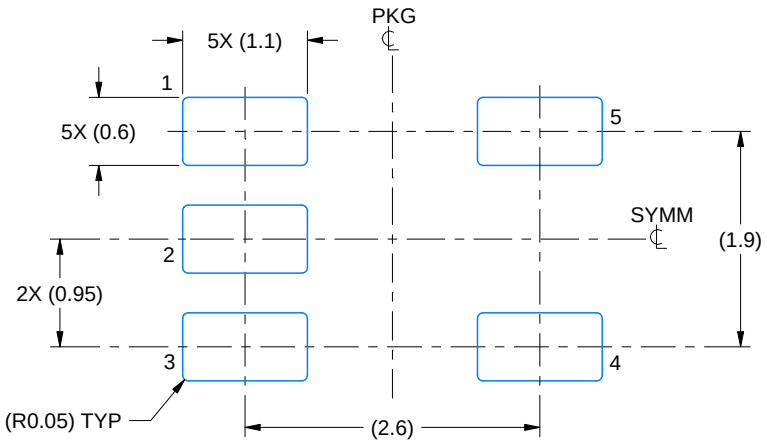


ALTERNATIVE PACKAGE SINGULATION VIEW

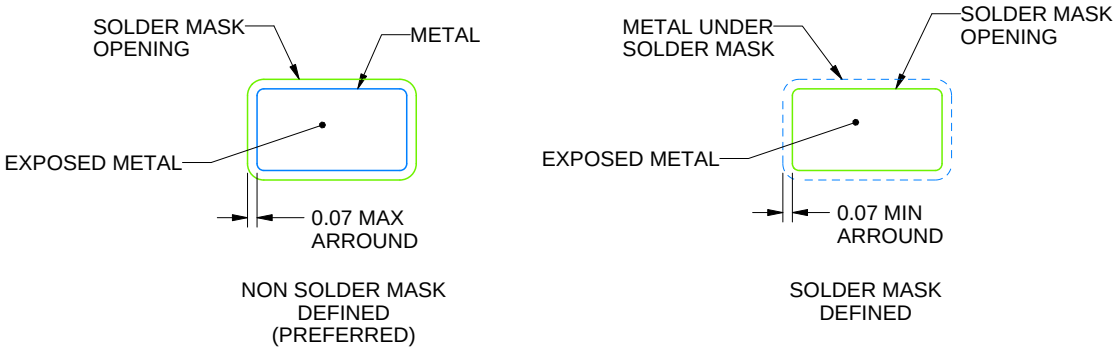
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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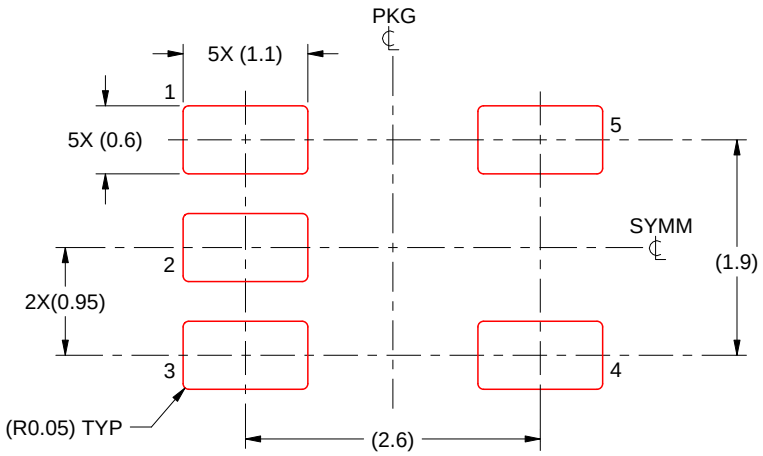
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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