LM26420-Q1 デュアル2A、車載用認定済み、高効率同期整流 DC/DCコンバータ

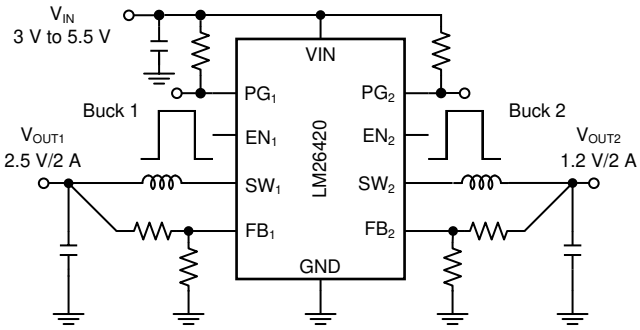
1 特長

- 車載アプリケーションに対応
- 以下の結果でAEC Q100認定済み
  - デバイス温度グレード0 (Q0): 動作時周囲温度範囲-40℃～+150℃
  - デバイス温度グレード1 (Q1): 動作時周囲温度範囲-40℃～+125℃
- CISPR25 Class 5 伝導エミッションに準拠
- 入力電圧範囲：3V～5.5V
- 出力電圧範囲：0.8V～4.5V
- レギュレータごとに 2A の出力電流
- 2.2MHz 固定のスイッチング周波数
- 0.8V、1.5% 精度の内部基準電圧
- 内部ソフト・スタート
- 出力ごとに独立のパワー・グッドと高精度のイネーブル
- 電流モード、PWM 動作
- サーマル・シャットダウン
- 過電圧保護
- 出力負荷をプリバイアスして起動可能
- レギュレータは 180°の位相差
- WEBENCH® Power Designer により、LM26420-Q1 を使用するカスタム設計を作成

2 アプリケーション

- 車載用ヘッド・ユニットおよびクラスタ
- ADAS カメラ・システム
- 車載用レーダー・システム
- 高度に統合された POL 電源

LM26420デュアル降圧DC/DCコンバータ



3 概要

LM26420-Q1レギュレータはモノリシック、高効率のデュアルPWM降圧型DC/DCコンバータです。このデバイスは、最先端のBICMOSテクノロジを使用して、内蔵の75mΩ PMOS上部スイッチと、内蔵の50mΩ NMOS下部スイッチにより2つの2A負荷を駆動し、可能な最高の電力密度を実現しています。世界最高レベルの制御回路により、最短で30nsのオン時間が可能なため、3V～5.5Vの入力動作範囲全体から、最小出力電圧の0.8Vへ、非常に高周波の変換が可能です。

動作周波数が高いにもかかわらず、93%までの高い効率を簡単に実現できます。外部からのシャットダウン機能を備えており、非常に低いスタンバイ電流が特長です。LM26420-Q1は電流モード制御と内部補償を活用して、広範な動作条件にわたって高性能のレギュレーションを行います。

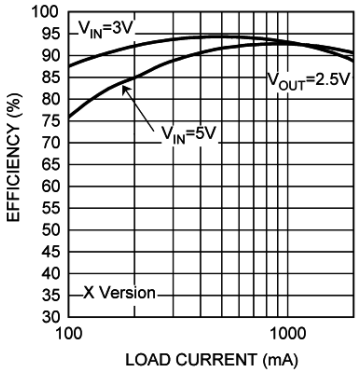
LM26420-Q1はスイッチング周波数が2MHzを超えることが保証されているため、AM周波数帯域に干渉を引き起こすおそれなしに車載用アプリケーションで使用できます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
LM26420-Q1	HTSSOP (20)	6.50mm×4.40mm
	WQFN (16)	4.00mm×4.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

LM26420の効率(最高93%)



目次

4 改訂履歴

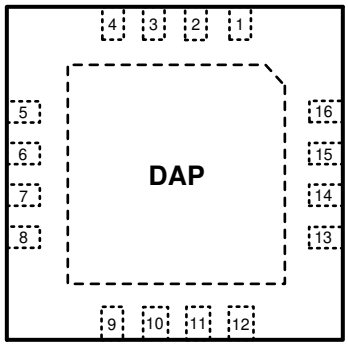
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年5月発行のものから更新 **Page**

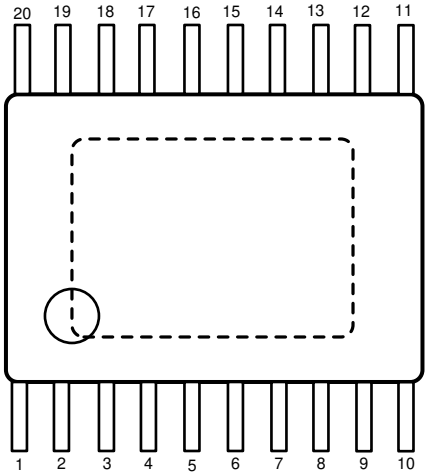
- Updated Power Supply Recommendations ... 28

5 Pin Configuration and Functions

RUM Package
16-Pin WQFN
Top View



PWP Package
20-Pin HTSSOP
Top View



Pin Functions: 16-Pin WQFN

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1,2	$VIND_1$	P	Power input supply for Buck 1.
3	SW_1	P	Output switch for Buck 1. Connect to the inductor.
4	$PGND_1$	G	Power ground pin for Buck 1.
5	FB_1	A	Feedback pin for Buck 1. Connect to external resistor divider to set output voltage.
6	PG_1	G	Power Good Indicator for Buck 1. Pin is connected through a resistor to an external supply (open drain output).
7	PG_2	G	Power Good Indicator for Buck 2. Pin is connected through a resistor to an external supply (open drain output).
8	FB_2	A	Feedback pin for Buck 2. Connect to external resistor divider to set output voltage.
9	$PGND_2$	G	Power ground pin for Buck 2.
10	SW_2	P	Output switch for Buck 2. Connect to the inductor.
11, 12	$VIND_2$	A	Power Input supply for Buck 2.
13	EN_2	A	Enable control input. Logic high enable operation for Buck 2. Do not allow this pin to float or be greater than V_{IN} + 0.3 V.
14	AGND	G	Signal ground pin. Place the bottom resistor of the feedback network as close as possible to pin.
15	VINC	A	Input supply for control circuitry.
16	EN_1	A	Enable control input. Logic high enable operation for Buck 1. Do not allow this pin to float or be greater than V_{IN} + 0.3 V.
DAP	Die Attach Pad	—	Connect to system ground for low thermal impedance and as a primary electrical GND connection.

Pin Functions 20-Pin HTSSOP

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
1	VINC	A	Input supply for control circuitry.
2	EN_1	A	Enable control input. Logic high enable operation for Buck 1. Do not allow this pin to float or be greater than V_{IN} + 0.3 V.
3, 4	$VIND_1$	A	Power Input supply for Buck 1.
5	SW_1	P	Output switch for Buck 1. Connect to the inductor.
6,7	$PGND_1$	G	Power ground pin for Buck 1.
8	FB_1	A	Feedback pin for Buck 1. Connect to external resistor divider to set output voltage.
9	PG_1	G	Power Good Indicator for Buck 1. Pin is connected through a resistor to an external supply (open drain output).
10, 11, DAP	Die Attach Pad	—	Connect to system ground for low thermal impedance, but it cannot be used as a primary GND connection.
12	PG_2	G	Power Good Indicator for Buck 2. Pin is connected through a resistor to an external supply (open drain output).
13	FB_2	A	Feedback pin for Buck 2. Connect to external resistor divider to set output voltage.
14, 15	$PGND_2$	G	Power ground pin for Buck 2.
16	SW_2	P	Output switch for Buck 2. Connect to the inductor.
17, 18	$VIND_2$	A	Power Input supply for Buck 2.
19	EN_2	A	Enable control input. Logic high enable operation for Buck 2. Do not allow this pin to float or be greater than V_{IN} + 0.3 V.
20	AGND	G	Signal ground pin. Place the bottom resistor of the feedback network as close as possible to pin.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltages	VIN	–0.5	7	V
	FB	–0.5	3	
	EN	–0.5	7	
Output voltages	SW	–0.5	7	V
Infrared or convection reflow (15 sec)	Soldering Information		220	°C
Storage temperature T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	Other pins	±750	
			Corner pins 1, 10, 11, and 20	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{IN}	3	5.5	V
Junction temperature (Q1)	–40	125	°C
Junction temperature (Q0)	–40	150	

6.4 Thermal Information

THERMAL METRIC(1)		LM26420-Q1		UNIT
		PWP (HTSSOP)	RUM (WQFN)	
		20 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.5	36.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case thermal resistance	21.0	32.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.9	14.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.7	14.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	4.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics Per Buck

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Feedback Voltage		0.788	0.8	0.812	V
$\Delta V_{FB}/V_{IN}$	Feedback Voltage Line Regulation	V_{IN} = 3 V to 5.5 V		0.05		%/V
I_B	Feedback Input Bias Current			0.4	100	nA
UVLO	Undervoltage Lockout	V_{IN} Rising		2.628	2.9	V
		V_{IN} Falling	2	2.3		V
	UVLO Hysteresis			330		mV
F_{SW}	Switching Frequency		2.01	2.2	2.65	MHz
F_{FB}	Frequency Foldback			300		kHz
D_{MAX}	Maximum Duty Cycle		86%	91.5%		
R_{DSON_TOP}	TOP Switch On Resistance	WQFN-16 Package		75	135	mΩ
		HTSSOP-20 Package		70	135	
R_{DSON_BOT}	BOTTOM Switch On Resistance	WQFN-16 Package		55	100	mΩ
		TSSOP-20 Package		45	80	
I_{CL_TOP}	TOP Switch Current Limit	V_{IN} = 3.3 V	2.4	3.3		A
I_{CL_BOT}	BOTTOM Switch Reverse Current Limit	V_{IN} = 3.3 V	0.4	0.75		A
$\Delta\Phi$	Phase Shift Between SW_1 and SW_2		160	180	200	°
V_{EN_TH}	Enable Threshold Voltage		0.97	1.04	1.12	V
	Enable Threshold Hysteresis			0.15		
I_{SW_TOP}	Switch Leakage			–0.7		µA
I_{EN}	Enable Pin Current	Sink/Source		5		nA
$V_{PG\text{-}TH\text{-}U}$	Upper Power Good Threshold	FB Pin Voltage Rising	848	925	1,008	mV
	Upper Power Good Hysteresis			40		mV
$V_{PG\text{-}TH\text{-}L}$	Lower Power Good Threshold	FB Pin Voltage Rising	656	710	791	mV
	Lower Power Good Hysteresis			40		mV
I_{QVINC}	VINC Quiescent Current (non-switching) with both outputs on	V_{FB} = 0.9 V		3.3	5	mA
	VINC Quiescent Current (switching) with both outputs on	V_{FB} = 0.7 V		4.7	6.2	
	VINC Quiescent Current (shutdown)	V_{EN} = 0 V		0.05		µA
I_{QVIND}	VIND Quiescent Current (non-switching)	V_{FB} = 0.9 V		0.9	1.5	mA
	VIND Quiescent Current (switching)	V_{FB} = 0.7 V		11	15	
I_{QVIND}	VIND Quiescent Current (switching)	LM26420Q0 V_{FB} = 0.7 V		11	18	mA
I_{QVIND}	VIND Quiescent Current (shutdown)	V_{EN} = 0 V		0.1		µA
T_{SD}	Thermal Shutdown Temperature			165		°C

6.6 Typical Characteristics

All curves taken at V_{IN} = 5 V with configuration in typical application circuits shown in *Application and Implementation*. T_J = 25°C, unless otherwise specified.

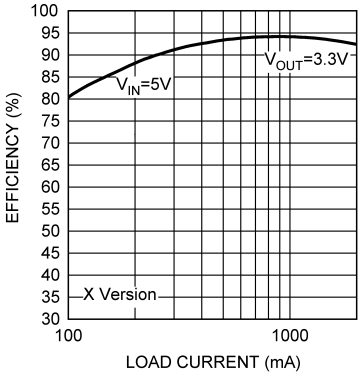


Figure 1. Efficiency vs Load

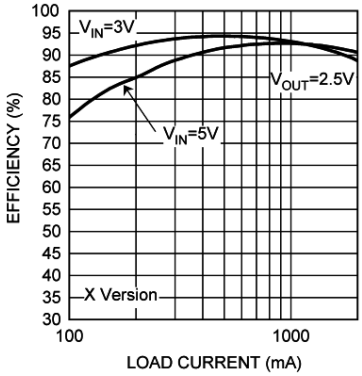


Figure 2. Efficiency vs Load

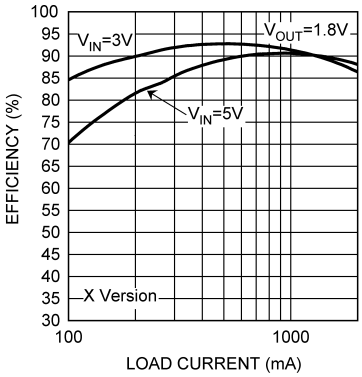


Figure 3. Efficiency vs Load

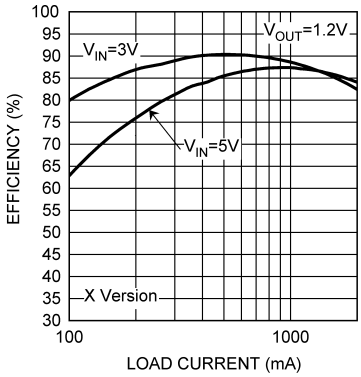


Figure 4. Efficiency vs Load

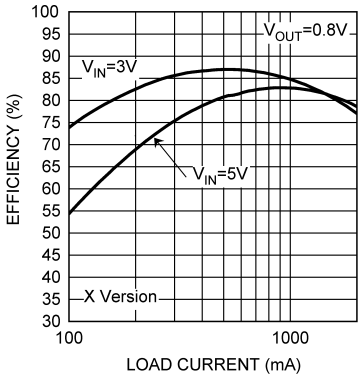


Figure 5. Efficiency vs Load

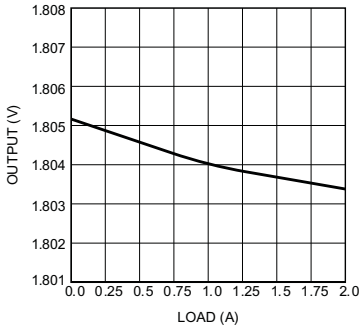
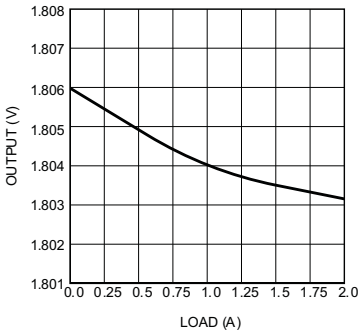


Figure 6. Load Regulation

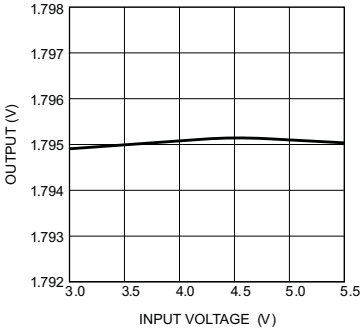
Typical Characteristics (continued)

All curves taken at V_{IN} = 5 V with configuration in typical application circuits shown in *Application and Implementation*. T_J = 25°C, unless otherwise specified.



V_{IN} = 3 V V_{OUT} = 1.8 V

Figure 7. Load Regulation



V_{OUT} = 1.8 V I_{OUT} = 1000 mA

Figure 8. Line Regulation

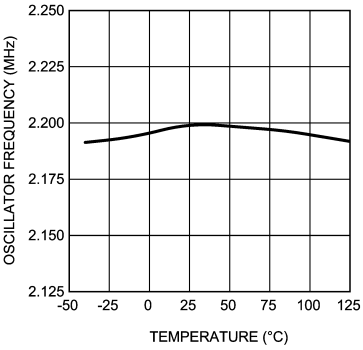


Figure 9. Oscillator Frequency vs Temperature,

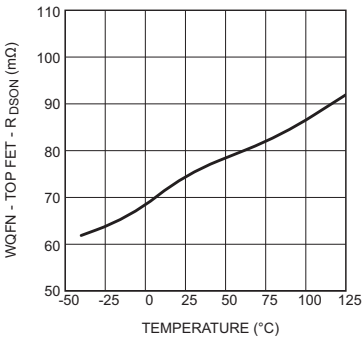


Figure 10. R_{DSON} Top Vs Temperature (WQFN-16 Package)

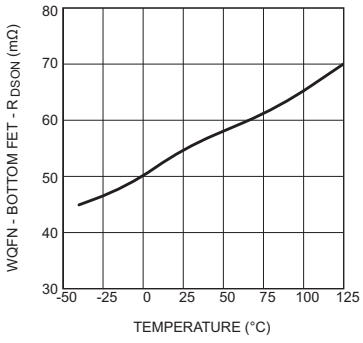


Figure 11. R_{DSON} Bottom Vs Temperature (WQFN-16 Package)

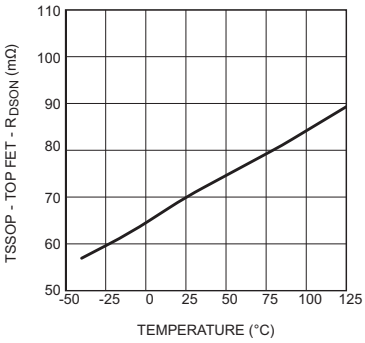


Figure 12. R_{DSON} Top Vs Temperature (TSSOP-20 Package)

Typical Characteristics (continued)

All curves taken at V_{IN} = 5 V with configuration in typical application circuits shown in *Application and Implementation*. T_J = 25°C, unless otherwise specified.

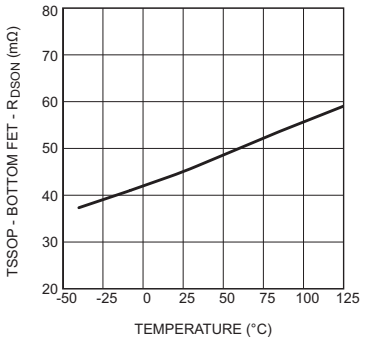


Figure 13. R_{DSON} Bottom vs Temperature (TSSOP-20 Package)

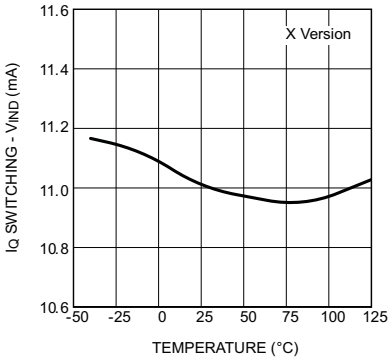


Figure 14. I_Q (Quiescent Current Switching)

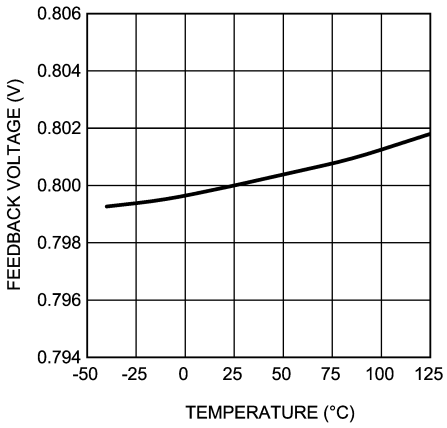
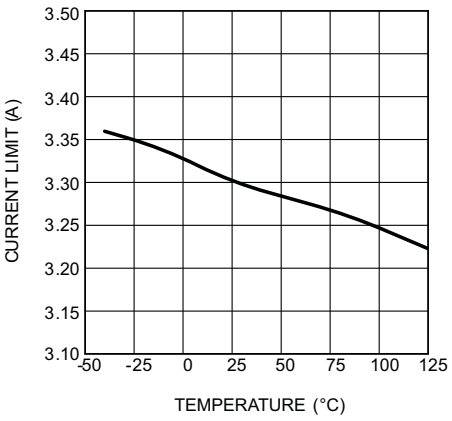


Figure 15. V_{FB} vs Temperature



V_{IN} = 5 V and 3.3 V

Figure 16. Current Limit vs Temperature

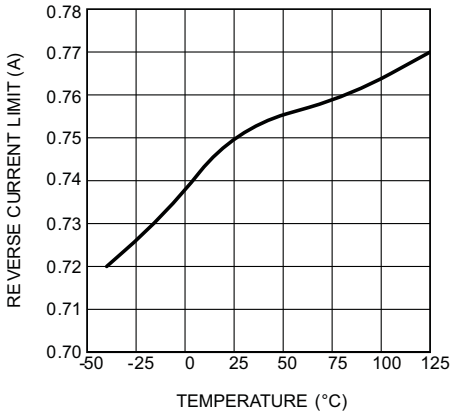


Figure 17. Reverse Current Limit vs Temperature

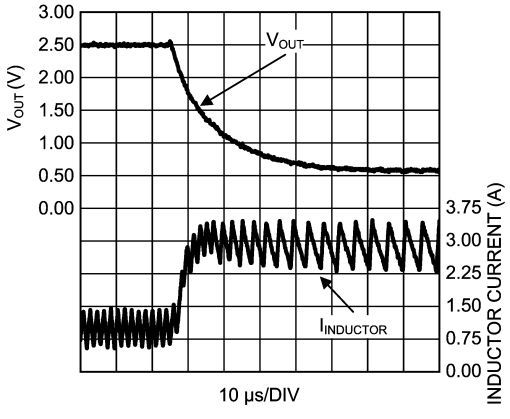


Figure 18. Short Circuit Waveforms

Typical Characteristics (continued)

All curves taken at V_{IN} = 5 V with configuration in typical application circuits shown in *Application and Implementation*. T_J = 25°C, unless otherwise specified.

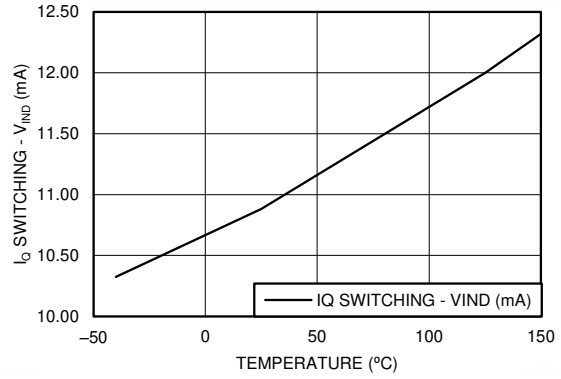


Figure 19. I_Q (Quiescent Current) vs Temperature (Q0 Grade)

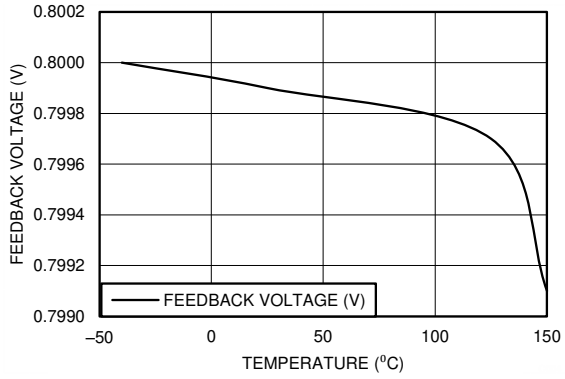


Figure 20. V_{FB} vs Temperature (Q0 Grade)

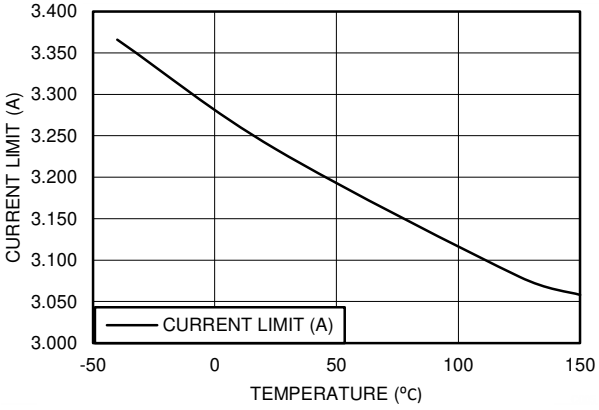


Figure 21. Current Limit vs Temperature (Q0 Grade)

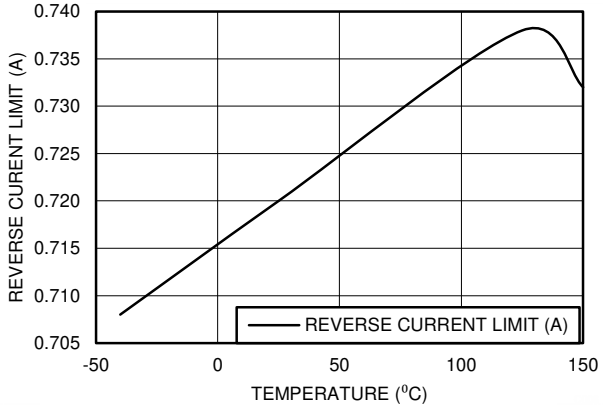


Figure 22. Reverse Current Limit vs Temperature (Q0 Grade)

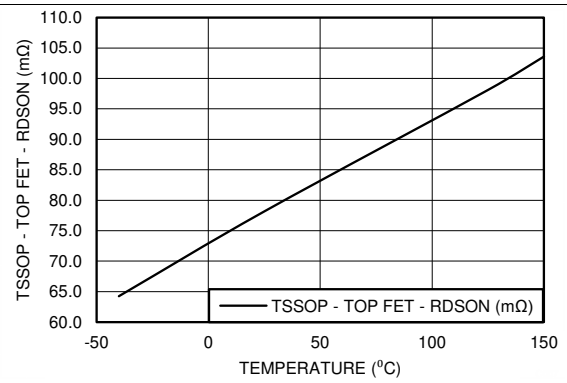


Figure 23. R_{DSON} Top vs Temperature (Q0 Grade)

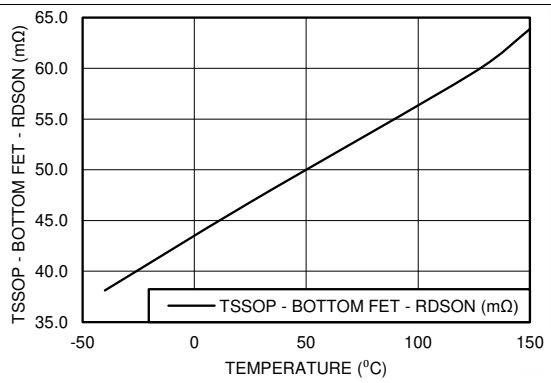


Figure 24. R_{DSON} Bottom vs Temperature (Q0 Grade)

Typical Characteristics (continued)

All curves taken at V_{IN} = 5 V with configuration in typical application circuits shown in *Application and Implementation*. T_J = 25°C, unless otherwise specified.

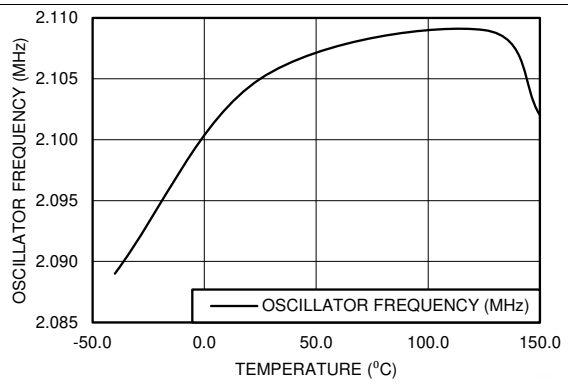


Figure 25. Oscillator Frequency vs Temperature (Q0 Grade)

7 Detailed Description

7.1 Overview

The LM26420-Q1 is a constant frequency dual PWM buck synchronous regulator device that can supply two loads at up to 2 A each. The regulator has a preset switching frequency of 2.2 MHz. This high frequency allows the LM26420-Q1 to operate with small surface mount capacitors and inductors, resulting in a DC/DC converter that requires a minimum amount of board space. The LM26420-Q1 is internally compensated, so it is simple to use and requires few external components. The LM26420-Q1 uses current-mode control to regulate the output voltage. The following operating description of the LM26420-Q1 refers to the *Functional Block Diagram*, which depicts the functional blocks for one of the two channels, and to the waveforms in Figure 26. The LM26420-Q1 supplies a regulated output voltage by switching the internal PMOS and NMOS switches at constant frequency and variable duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal clock. When this pulse goes low, the output control logic turns on the internal PMOS control switch (TOP Switch). During this on-time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (I_L) increases with a linear slope. I_L is measured by the current sense amplifier, which generates an output proportional to the switch current. The sense signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage and V_{REF}. When the PWM comparator output goes high, the TOP Switch turns off and the NMOS switch (BOTTOM Switch) turns on after a short delay, which is controlled by the Dead-Time-Control Logic, until the next switching cycle begins. During the top switch off-time, inductor current discharges through the BOTTOM Switch, which forces the SW pin to swing to ground. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage.

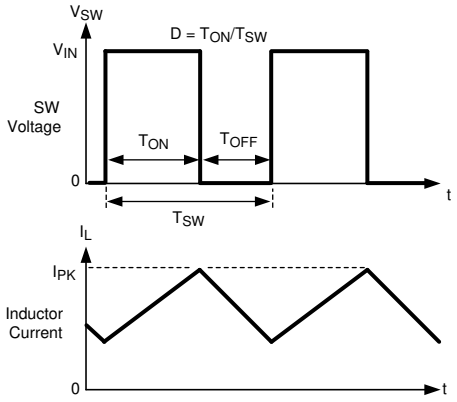
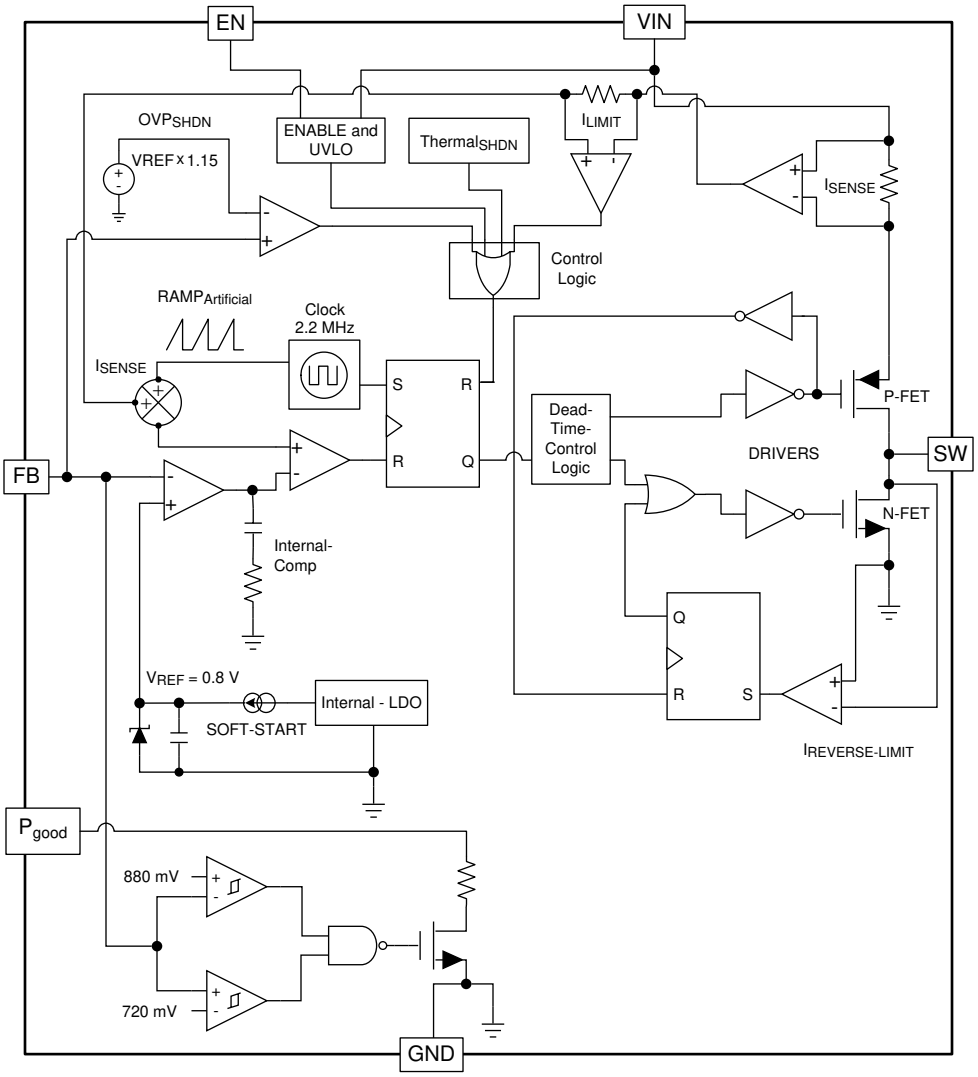


Figure 26. LM26420-Q1 Basic Operation of the PWM Comparator

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft Start

This function forces V_{OUT} to increase at a controlled rate during start-up in a controlled fashion, which helps reduce inrush current and eliminate overshoot on V_{OUT}. During soft start, reference voltage of the error amplifier ramps from 0 V to its nominal value of 0.8 V in approximately 600 µs. If the converter is turned on into a pre-biased load, then the feedback begins ramping from the prebias voltage but at the same rate as if it had started from 0 V. The two outputs start up ratiometrically if enabled at the same time, see Figure 27 below.

Feature Description (continued)

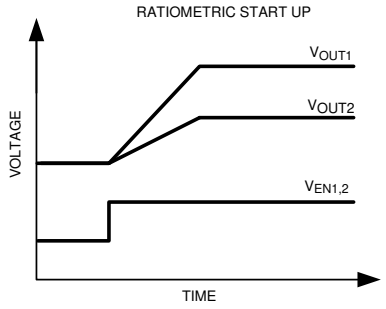


Figure 27. LM26420 Soft-Start

7.3.2 Power Good

The LM26420-Q1 features an open drain power good (PG) pin to sequence external supplies or loads and to provide fault detection. This pin requires an external resistor (R_{PG}) to pull PG high when the output is within the PG tolerance window. Typical values for this resistor range from 10 kΩ to 100 kΩ.

7.3.3 Precision Enable

The LM26420-Q1 features independent precision enables that allow the converter to be controlled by an external signal. This feature allows the device to be sequenced either by a external control signal or the output of another converter in conjunction with a resistor divider network. It can also be set to turn on at a specific input voltage when used in conjunction with a resistor divider network connected to the input voltage. The device is enabled when the EN pin exceeds 1.04 V and has a 150-mV hysteresis.

7.4 Device Functional Modes

7.4.1 Output Overvoltage Protection

The overvoltage comparator compares the FB pin voltage to a voltage that is approximately 15% greater than the internal reference V_{REF}. Once the FB pin voltage goes 15% above the internal reference, the internal PMOS switch is turned off, which allows the output voltage to decrease toward regulation.

7.4.2 Undervoltage Lockout

Undervoltage lockout (UVLO) prevents the LM26420-Q1 from operating until the input voltage exceeds 2.628 V (typical). The UVLO threshold has approximately 330 mV of hysteresis, so the device operates until V_{IN} drops below 2.3 V (typical). Hysteresis prevents the part from turning off during power up if V_{IN} is non-monotonic.

7.4.3 Current Limit

The LM26420-Q1 uses cycle-by-cycle current limiting to protect the output switch. During each switching cycle, a current limit comparator detects if the output switch current exceeds 3.3 A (typical), and turns off the switch until the next switching cycle begins.

7.4.4 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the output switch when the device junction temperature exceeds 165°C. After thermal shutdown occurs, the output switch does not turn on until the junction temperature drops to approximately 150°C.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Programming Output Voltage

The output voltage is set using Equation 1 where R2 is connected between the FB pin and GND, and R1 is connected between V_{OUT} and the FB pin. A good value for R2 is 10 kΩ. When designing a unity gain converter (V_{OUT} = 0.8 V), R1 must be between 0 Ω and 100 Ω, and R2 must be on the order of 5 kΩ to 50 kΩ. 10 kΩ is the suggested value where R1 is the top feedback resistor and R2 is the bottom feedback resistor.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 \quad (1)$$

$$V_{REF} = 0.80V \quad (2)$$

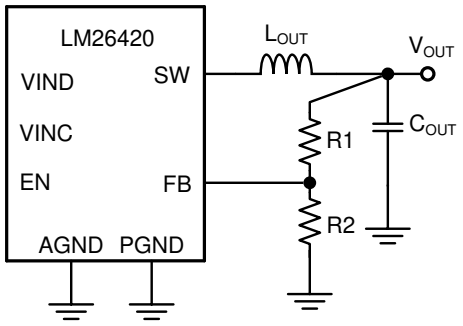


Figure 28. Programming V_{OUT}

To determine the maximum allowed resistor tolerance, use Equation 3:

$$\sigma = \left(\frac{1}{1 + 2x\frac{1 - \frac{V_{FB}}{V_{OUT}}}{TOL - \phi}}\right) \quad (3)$$

where

- TOL is the set point accuracy of the regulator, is the tolerance of V_{FB}.

Example:

V_{OUT} = 2.5 V, with a setpoint accuracy of ±3.5%.

$$\sigma = \left(\frac{1}{1 + 2x\frac{1 - \frac{0.8V}{2.5V}}{3.5\% - 1.5\%}}\right) = 1.4\% \quad (4)$$

Choose 1% resistors. If R2 = 10 kΩ, then R1 is 21.25 kΩ.

Application Information (continued)

8.1.2 VINC Filtering Components

Additional filtering is required between VINC and AGND in order to prevent high frequency noise on VIN from disturbing the sensitive circuitry connected to VINC. A small RC filter can be used on the VINC pin as shown in Figure 29.

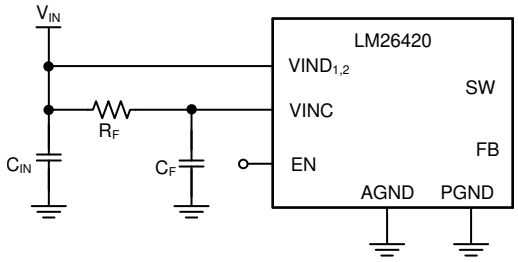


Figure 29. RC Filter On VINC

In general, R_F is typically between 1 Ω and 10 Ω so that the steady state voltage drop across the resistor due to the VINC bias current does not affect the UVLO level. C_F can range from 0.22 µF to 1 µF in X7R or X5R dielectric, where the RC time constant should be at least 2 µs. C_F must be placed as close to the device as possiblewith a direct connection from VINC and AGND.

8.1.3 Using Precision Enable and Power Good

The LM26420-Q1 device precision EN and PG pins address many of the sequencing requirements required in today's challenging applications. Each output can be controlled independently and have independent power good. This allows for a multitude of ways to control each output. Typically, the enables to each output are tied together to the input voltage and the outputs ratiometrically ramp up when the input voltage reaches above UVLO rising threshold. There may be instances where it is desired that the second output (V_{OUT2}) does not turn on until the first output (V_{OUT1}) has reached 90% of the desired setpoint. This is easily achieved with an external resistor divider attached from V_{OUT1} to EN_2, see Figure 30.

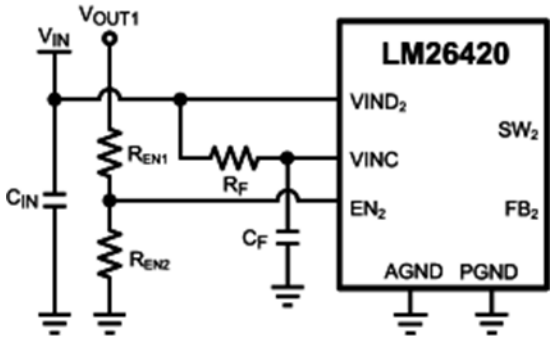


Figure 30. V_{OUT1} Controlling V_{OUT2} with Resistor Divider

If it is not desired to have a resistor divider to control V_{OUT2} with V_{OUT1}, then the PG_1 can be connected to the EN_2 pin to control V_{OUT2}, see Figure 31. R_{PG1} is a pullup resistor on the range of 10 kΩ to 100 kΩ, 50 kΩ is the suggested value. This turns on V_{OUT2} when V_{OUT1} is approximately 90% of the programmed output.

NOTE

This also turns off V_{OUT2} when V_{OUT1} is outside the ±10% of the programmed output.

Application Information (continued)

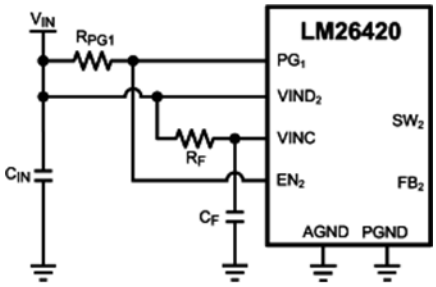


Figure 31. PG_1 Controlling V_{OUT2}

Another example might be that the output is not to be turned on until the input voltage reaches 90% of desired voltage setpoint. This verifies that the input supply is stable before turning on the output. Select R_{EN1} and R_{EN2} such that the voltage at the EN pin is greater than 1.12 V when reaching the 90% desired set-point.

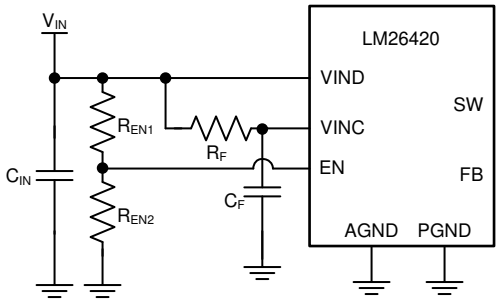


Figure 32. V_{OUT} Controlling V_{IN}

The power good feature of the LM26420-Q1 is designed with hysteresis in order to ensure no false power good flags are asserted during large transient. Once power good is asserted high, it is not pulled low until the output voltage exceeds ±14% of the setpoint for a during of approximately 7.5 µs (typical), see Figure 33.

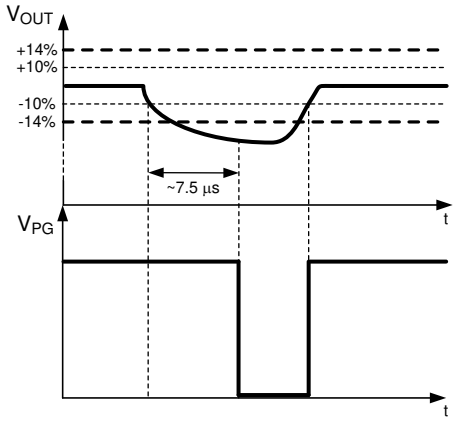


Figure 33. Power Good Hysteresis Operation

Application Information (continued)

8.1.4 Overcurrent Protection

When the switch current reaches the current limit value, it is turned off immediately. This effectively reduces the duty cycle and therefore the output voltage dips and continues to droop until the output load matches the peak current limit inductor current. As the FB voltage drops below 480 mV the operating frequency begins to decrease until it hits full on frequency foldback, which is set to approximately 300 kHz. Frequency foldback helps reduce the thermal stress in the device by reducing the switching losses and to prevent runaway of the inductor current when the output is shorted to ground.

It is important to note that when recovering from a overcurrent condition the converter does not go through the soft-start process. There may be an overshoot due to the sudden removal of the overcurrent fault. The reference voltage at the non-inverting input of the error amplifier always sits at 0.8 V during the overcurrent condition, therefore when the fault is removed the converter bring the FB voltage back to 0.8 V as quickly as possible. The overshoot depend on whether there is a load on the output after the removal of the overcurrent fault, the size of the inductor, and the amount of capacitance on the output. The smaller the inductor and the larger the capacitance on the output the smaller the overshoot.

NOTE

Overcurrent protection for each output is independent.

8.2 Typical Applications

8.2.1 2.2-MHz, 0.8-V Typical High-Efficiency Application Circuit

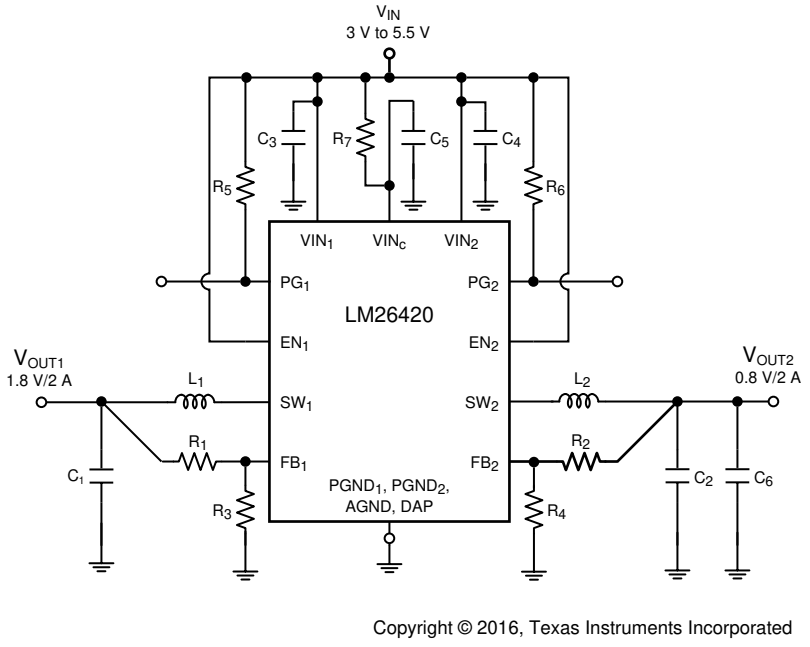


Figure 34. LM26420-Q1 (2.2 MHz): V_{IN} = 5 V, V_{OUT1} = 1.8 V at 2 A and V_{OUT2} = 0.8 V at 2 A

Typical Applications (continued)

8.2.1.1 Design Requirements

Example requirements for typical synchronous DC/DC converter applications:

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
V_{OUT}	Output voltage
V_{IN} (minimum)	Maximum input voltage
V_{IN} (maximum)	Minimum input voltage
I_{OUT} (maximum)	Maximum output current
f_{SW}	Switching frequency

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM26420-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

Table 2. Bill Of Materials

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2-A buck regulator	TI	LM26420-Q1
C3, C4	15 µF, 6.3 V, 1206, X5R	TDK	C3216X5R0J156M
C1	33 µF, 6.3 V, 1206, X5R	TDK	C3216X5R0J336M
C2, C6	22 µF, 6.3 V, 1206, X5R	TDK	C3216X5R0J226M
C5	0.47 µF, 10 V, 0805, X7R	Vishay	VJ0805Y474KXQCW1BC
L1	1.0 µH, 7.9 A	TDK	RLF7030T-1R0M6R4
L2	0.7 µH, 3.7 A	Coilcraft	LPS4414-701ML
R3, R4	10.0 kΩ, 0603, 1%	Vishay	CRCW060310K0F
R5, R6	49.9 kΩ, 0603, 1%	Vishay	CRCW060649K9F
R1	12.7 kΩ, 0603, 1%	Vishay	CRCW060312K7F
R7, R2	4.99 Ω, 0603, 1%	Vishay	CRCW06034R99F

8.2.1.2.2 Inductor Selection

The duty cycle (D) can be approximated as the ratio of output voltage (V_{OUT}) to input voltage (V_{IN}):

$$D = \frac{V_{OUT}}{V_{IN}} \tag{5}$$

The voltage drop across the internal NMOS (SW_BOT) and PMOS (SW_TOP) must be included to calculate a more accurate duty cycle. Calculate D by using the following formulas:

$$D = \frac{V_{OUT} + V_{SW\_BOT}}{V_{IN} + V_{SW\_BOT} - V_{SW\_TOP}} \tag{6}$$

V_{SW_TOP} and V_{SW_BOT} can be approximated by:

$$V_{SW\_TOP} = I_{OUT} \times R_{DSON\_TOP} \tag{7}$$

$$V_{SW\_BOT} = I_{OUT} \times R_{DSON\_BOT} \tag{8}$$

The inductor value determines the output ripple voltage. Smaller inductor values decrease the size of the inductor, but increase the output ripple voltage. An increase in the inductor value decreases the output ripple current.

One must ensure that the minimum current limit (2.4 A) is not exceeded, so the peak current in the inductor must be calculated. The peak current (I_{LPK}) in the inductor is calculated by:

$$I_{LPK} = I_{OUT} + \Delta i_L \tag{9}$$

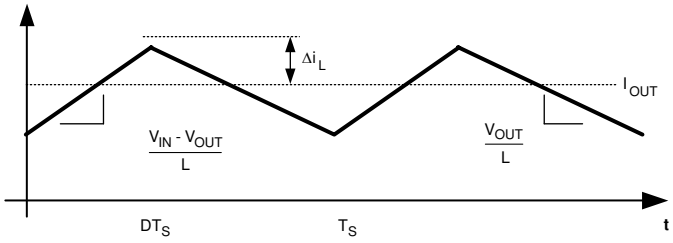


Figure 35. Inductor Current

$$\frac{V_{IN} - V_{OUT}}{L} = \frac{2\Delta i_L}{DT_S} \tag{10}$$

In general,

$$\Delta i_L = 0.1 \times (I_{OUT}) \rightarrow 0.2 \times (I_{OUT}) \tag{11}$$

If Δi_L = 20% of 2 A, the peak current in the inductor is 2.4 A. The minimum ensured current limit over all operating conditions is 2.4 A. One can either reduce Δi_L, or make the engineering judgment that zero margin is safe enough. The typical current limit is 3.3 A.

The LM26420-Q1 operates at frequencies allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing output ripple voltage. See *Output Capacitor* section for more details on calculating output voltage ripple. Now that the ripple current is determined, the inductance is calculated by:

$$L = \left(\frac{DT_S}{2\Delta i_L}\right) \times (V_{IN} - V_{OUT}) \tag{12}$$

Where

$$T_S = \frac{1}{f_S} \tag{13}$$

When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation results in a sudden reduction in inductance and prevent the regulator from operating correctly. The peak current of the inductor is used to specify the maximum output current of the inductor and saturation is not a concern due to the exceptionally small delay of the internal current limit signal. Ferrite based inductors are preferred to minimize core losses when operating with the frequencies used by the LM26420-Q1. This presents little restriction because the variety of ferrite-based inductors is huge. Lastly, inductors with lower series resistance (R_{DCR}) provides better operating efficiency. For recommended inductors see Table 2.

8.2.1.2.3 Input Capacitor Selection

The input capacitors provide the AC current needed by the nearby power switch so that current provided by the upstream power supply does not carry a lot of AC content, generating less EMI. To the buck regulator in question, the input capacitor also prevents the drain voltage of the FET switch from dipping when the FET is turned on, therefore providing a healthy line rail for the LM26420-Q1 to work with. Because typically most of the AC current is provided by the local input capacitors, the power loss in those capacitors can be a concern. In the case of the LM26420-Q1 regulator, because the two channels operate 180° out of phase, the AC stress in the input capacitors is less than if they operated in phase. The measure for the AC stress is called input ripple RMS current. It is strongly recommended that at least one 10µF ceramic capacitor be placed next to each of the VIND pins. Bulk capacitors such as electrolytic capacitors or OSCON capacitors can be added to help stabilize the local line voltage, especially during large load transient events. As for the ceramic capacitors, use X7R or X5R types. They maintain most of their capacitance over a wide temperature range. Try to avoid sizes smaller than 0805. Otherwise significant drop in capacitance may be caused by the DC bias voltage. See *Output Capacitor* section for more information. The DC voltage rating of the ceramic capacitor should be higher than the highest input voltage.

Capacitor temperature is a major concern in board designs. While using a 10-µF or higher MLCC as the input capacitor is a good starting point, it is a good idea to check the temperature in the real thermal environment to make sure the capacitors are not overheated. Capacitor vendors may provide curves of ripple RMS current vs. temperature rise, based on a designated thermal impedance. In reality, the thermal impedance may be very different. So it is always a good idea to check the capacitor temperature on the board.

Because the duty cycles of the two channels may overlap, calculation of the input ripple RMS current is a little tedious — use Equation 14:

$$I_{irrms} = \sqrt{(I_1 - I_{av})^2 d1 + (I_2 - I_{av})^2 d2 + (I_1 + I_2 - I_{av})^2 d3}$$

where

- I_1 is Channel 1's maximum output current
- I_2 is Channel 2's maximum output current
- d1 is the non-overlapping portion of Channel 1's duty cycle D_1
- d2 is the non-overlapping portion of Channel 2's duty cycle D_2
- d3 is the overlapping portion of the two duty cycles.
- I_{av} is the average input current

(14)

$I_{av} = I_1 \times D_1 + I_2 \times D_2$. To quickly determine the values of d1, d2 and d3, refer to the decision tree in Figure 36. To determine the duty cycle of each channel, use $D = V_{OUT}/V_{IN}$ for a quick result or use the following equation for a more accurate result.

$$D = \frac{V_{OUT} + V_{SW\_BOT} + I_{OUT} \times R_{DC}}{V_{IN} + V_{SW\_BOT} - V_{SW\_TOP}}$$

where

- R_{DC} is the winding resistance of the inductor.

(15)

Example:

V_{IN} = 5 V, V_{OUT1} = 3.3 V, I_{OUT1} = 2 A, V_{OUT2} = 1.2 V, I_{OUT2} = 1.5 A, R_{DS} = 170 mΩ, R_{DC} = 30 mΩ. (I_{OUT1} is the same as I_1 in the input ripple RMS current equation, I_{OUT2} is the same as I_2).

First, find out the duty cycles. Plug the numbers into the duty cycle equation and we get D1 = 0.75, and D2 = 0.33. Next, follow the decision tree in Figure 36 to find out the values of d1, d2 and d3. In this case, d1 = 0.5, d2 = D2 + 0.5 – D1 = 0.08, and d3 = D1 – 0.5 = 0.25. $I_{av} = I_{OUT1} \times D1 + I_{OUT2} \times D2 = 1.995$ A. Plug all the numbers into the input ripple RMS current equation and the result is $I_{IR(rms)}$ = 0.77 A.

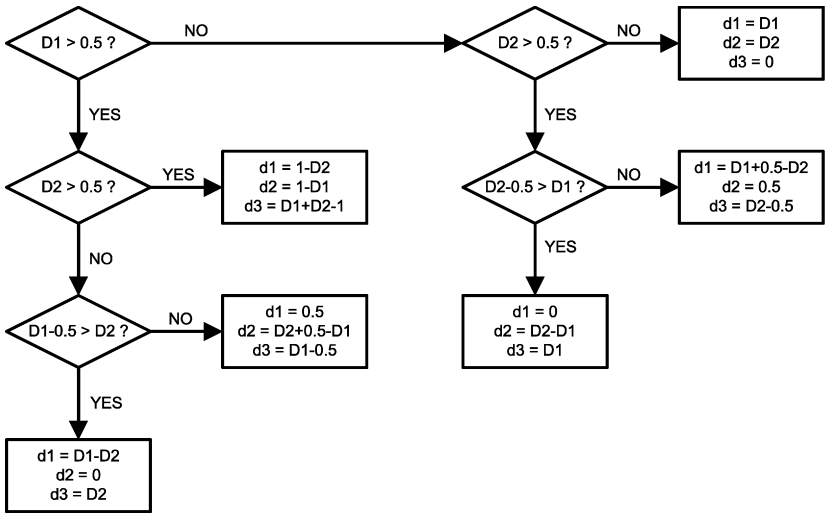


Figure 36. Determining D1, D2, And D3

8.2.1.2.4 Output Capacitor

The output capacitor is selected based upon the desired output ripple and transient response. The initial current of a load transient is provided mainly by the output capacitor. The output ripple of the converter is approximately:

$$\Delta V_{OUT} = \Delta I_L \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}} \right) \quad (16)$$

When using MLCCs, the ESR is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple is approximately sinusoidal and 90° phase shifted from the switching action. Given the availability and quality of MLCCs and the expected output voltage of designs using the LM26420-Q1, there is really no need to review any other capacitor technologies. Another benefit of ceramic capacitors is their ability to bypass high frequency noise. A certain amount of switching edge noise couples through parasitic capacitances in the inductor to the output. A ceramic capacitor bypasss this noise while a tantalum capacitor does not. Because the output capacitor is one of the two external components that control the stability of the regulator control loop, most applications require a minimum of 22 µF of output capacitance. Capacitance often, but not always, can be increased significantly with little detriment to the regulator stability. Like the input capacitor, recommended multilayer ceramic capacitors are X7R or X5R types.

8.2.1.2.5 Calculating Efficiency and Junction Temperature

The complete LM26420-Q1 DC/DC converter efficiency can be estimated in the following manner.

$$\eta = \frac{P_{OUT}}{P_{IN}} \quad (17)$$

Or

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \quad (18)$$

Calculations for determining the most significant power losses follow here. Other losses totaling less than 2% are not discussed.

Power loss (P_{LOSS}) is the sum of two basic types of losses in the converter: switching and conduction. Conduction losses usually dominate at higher output loads, whereas switching losses remain relatively fixed and dominate at lower output loads. The first step in determining the losses is to calculate the duty cycle (D):

$$D = \frac{V_{OUT} + V_{SW\_BOT}}{V_{IN} + V_{SW\_BOT} - V_{SW\_TOP}} \quad (19)$$

V_{SW_TOP} is the voltage drop across the internal PFET when it is on, and is equal to:

$$V_{SW\_TOP} = I_{OUT} \times R_{DSON\_TOP} \quad (20)$$

V_{SW_BOT} is the voltage drop across the internal NFET when it is on, and is equal to:

$$V_{SW\_BOT} = I_{OUT} \times R_{DSON\_BOT} \quad (21)$$

If the voltage drop across the inductor (V_{DCR}) is accounted for, the equation becomes:

$$D = \frac{V_{OUT} + V_{SW\_BOT} + V_{DCR}}{V_{IN} + V_{SW\_BOT} + V_{DCR} - V_{SW\_TOP}} \quad (22)$$

Another significant external power loss is the conduction loss in the output inductor. The equation can be simplified to:

$$P_{IND} = I_{OUT}^2 \times R_{DCR} \quad (23)$$

The LM26420-Q1 conduction loss is mainly associated with the two internal FETs:

$$P_{COND\_TOP} = (I_{OUT}^2 \text{ x } D)\left(1 + \frac{1}{3} \text{ x } \left(\frac{\Delta i_L}{I_{OUT}}\right)^2\right) R_{DSON\_TOP}$$

$$P_{COND\_BOT} = (I_{OUT}^2 \text{ x } (1\text{-}D))\left(1 + \frac{1}{3} \text{ x } \left(\frac{\Delta i_L}{I_{OUT}}\right)^2\right) R_{DSON\_BOT} \quad (24)$$

If the inductor ripple current is fairly small, the conduction losses can be simplified to:

$$P_{COND\_TOP} = (I_{OUT}^2 \times R_{DSON\_TOP} \times D) \quad (25)$$

$$P_{COND\_BOT} = (I_{OUT}^2 \times R_{DSON\_BOT} \times (1\text{-}D)) \quad (26)$$

$$P_{COND} = P_{COND\_TOP} + P_{COND\_BOT} \quad (27)$$

Switching losses are also associated with the internal FETs. They occur during the switch on and off transition periods, where voltages and currents overlap resulting in power loss. The simplest means to determine this loss is to empirically measuring the rise and fall times (10% to 90%) of the switch at the switch node.

Switching Power Loss is calculated as follows:

$$P_{SWR} = 1/2(V_{IN} \times I_{OUT} \times F_{SW} \times T_{RISE}) \quad (28)$$

$$P_{SWF} = 1/2(V_{IN} \times I_{OUT} \times F_{SW} \times T_{FALL}) \quad (29)$$

$$P_{SW} = P_{SWR} + P_{SWF} \quad (30)$$

Another loss is the power required for operation of the internal circuitry:

$$P_Q = I_Q \times V_{IN} \quad (31)$$

I_Q is the quiescent operating current, and is typically around 8.4 mA (I_{QVINC} = 4.7 mA + I_{QVIND} = 3.7 mA) for the 550-kHz frequency option.

Due to Dead-Time-Control Logic in the converter, there is a small delay (~4 nsec) between the turn ON and OFF of the TOP and BOTTOM FET. During this time, the body diode of the BOTTOM FET is conducting with a voltage drop of V_{BDIODE} (~0.65 V). This allows the inductor current to circulate to the output, until the BOTTOM FET is turned ON and the inductor current passes through the FET. There is a small amount of power loss due to this body diode conducting and it can be calculated as follows:

$$P_{BDIODE} = 2 \times (V_{BDIODE} \times I_{OUT} \times F_{SW} \times T_{BDIODE}) \quad (32)$$

Typical Application power losses are:

$$P_{LOSS} = \Sigma P_{COND} + P_{SW} + P_{BDIODE} + P_{IND} + P_Q \quad (33)$$

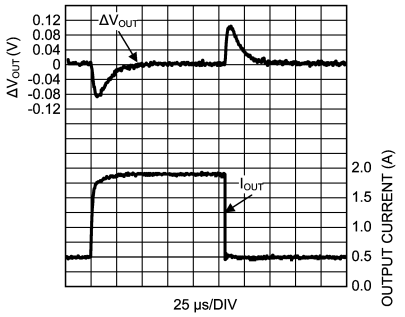
$$P_{INTERNAL} = \Sigma P_{COND} + P_{SW} + P_{BDIODE} + P_Q \quad (34)$$

Table 3. Power Loss Tabulation

DESIGN PARAMETER	VALUE	DESIGN PARAMETER	VALUE
V_{IN}	5 V	V_{OUT}	1.2 V
I_{OUT}	2 A	P_{OUT}	2.4 W
F_{SW}	550 kHz		
V_{BDIODE}	0.65 V	P_{BDIODE}	5.7 mW
I_Q	8.4 mA	P_Q	42 mW
T_{RISE}	1.5 nsec	P_{SWR}	4.1 mW
T_{FALL}	1.5 nsec	P_{SWF}	4.1 mW
R_{DSON_TOP}	75 mΩ	P_{COND_TOP}	81 mW
R_{DSON_BOT}	55 mΩ	P_{COND_BOT}	167 mW
IND_{DCR}	20 mΩ	P_{IND}	80 mW
D	0.262	P_{LOSS}	384 mW
η	86.2%	$P_{INTERNAL}$	304 mW

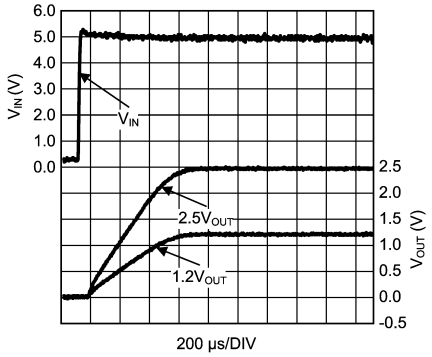
These calculations assume a junction temperature of 25°C. The R_{DSON} values are larger due to internal heating; therefore, the internal power loss ($P_{INTERNAL}$) must be first calculated to estimate the rise in junction temperature.

8.2.1.3 Application Curves



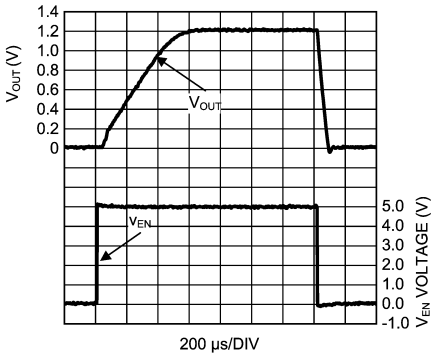
V_{OUT} = 1.2 V 25-100% Load Transient

Figure 37. Load Transient Response



V_{IN} = 5 V V_{OUT} = 1.8 V at 1 A

Figure 38. Start-Up (Soft Start)



V_{IN} = 5 V V_{OUT} = 1.8 V at 1 A

Figure 39. Enable - Disable

8.2.2 2.2-MHz, 1.8-V Typical High-Efficiency Application Circuit

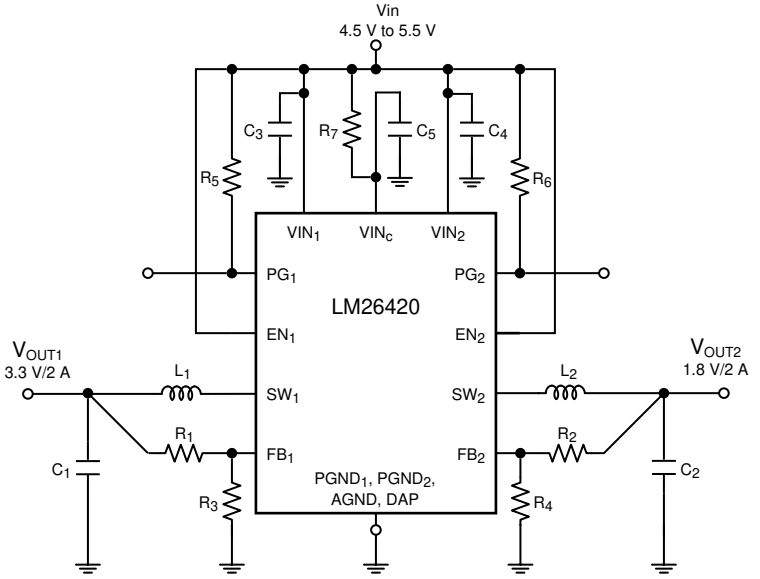


Figure 40. LM26420-Q1 (2.2 MHz): V_{IN} = 5 V, V_{OUT1} = 3.3 V at 2 A and V_{OUT2} = 1.8 V at 2 A

8.2.2.1 Design Requirements

See *Design Requirements* above.

8.2.2.2 Detailed Design Procedure

Table 4. Bill Of Materials

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2-A Buck Regulator	TI	LM26420-Q1
C3, C4	15 µF, 6.3 V, 1206, X5R	TDK	C3216X5R0J156M
C1	22 µF, 6.3 V, 1206, X5R	TDK	C3216X5R0J226M
C2	33 µF, 6.3 V, 1206, X5R	TDK	C3216X5R0J336M
C5	0.47 µF, 10 V, 0805, X7R	Vishay	VJ0805Y474KXQCW1BC
L1, L2	1.0 µH, 7.9 A	TDK	RLF7030T-1R0M6R4
R3, R4	10.0 kΩ, 0603, 1%	Vishay	CRCW060310K0F
R2	12.7 kΩ, 0603, 1%	Vishay	CRCW060312K7F
R5, R6	49.9 kΩ, 0603, 1%	Vishay	CRCW060649K9F
R1	31.6 kΩ, 0603, 1%	Vishay	CRCW060331K6F
R7	4.99 Ω, 0603, 1%	Vishay	CRCW06034R99F

Also see *Detailed Design Procedure* above.

8.2.2.3 Application Curves

See *Application Curves* above.

8.2.3 LM26420-Q12.2-MHz, 2.5-V Typical High-Efficiency Application Circuit

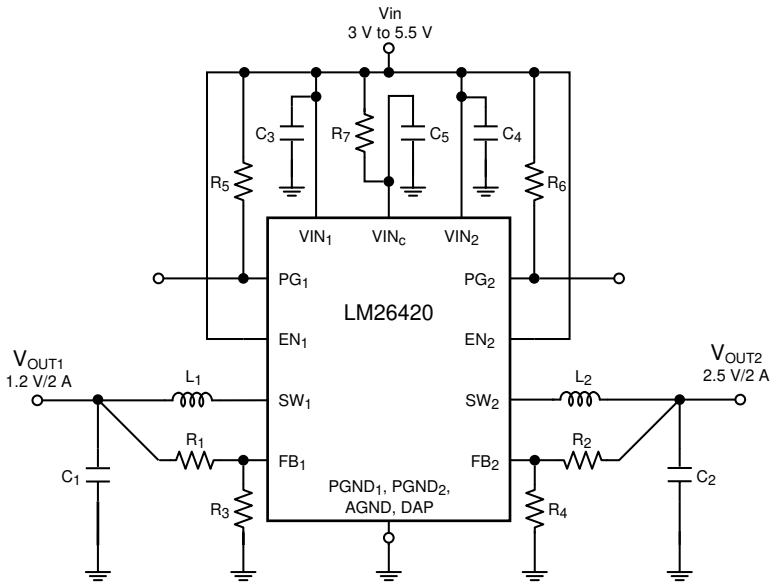


Figure 41. LM26420-Q1 (2.2 MHz): V_{IN} = 5 V, V_{OUT1} = 1.2 V at 2 A and V_{OUT2} = 2.5 V at 2 A

8.2.3.1 Design Requirements

See *Design Requirements* above.

8.2.3.2 Detailed Design Procedure

Table 5. Bill Of Materials

PART ID	PART VALUE	MANUFACTURER	PART NUMBER
U1	2-A buck regulator	TI	LM26420-Q1
C3, C4	15 µF, 6.3 V, 1206, X5R	TDK	C3216X5R0J156M
C1	33 µF, 6.3 V, 1206, X5R	TDK	C3216X5R0J336M
C2	22 µF, 6.3 V, 1206, X5R	TDK	C3216X5R0J226M
C5	0.47 µF, 10 V, 0805, X7R	Vishay	VJ0805Y474KXQCW1BC
L1	1.0 µH, 7.9A	TDK	RLF7030T-1R0M6R4
L2	1.5 µH, 6.5A	TDK	RLF7030T-1R5M6R1
R3, R4	10.0 kΩ, 0603, 1%	Vishay	CRCW060310K0F
R1	4.99 kΩ, 0603, 1%	Vishay	CRCW06034K99F
R5, R6	49.9 kΩ, 0603, 1%	Vishay	CRCW060649K9F
R2	21.5 kΩ, 0603, 1%	Vishay	CRCW060321K5F
R7	4.99 Ω, 0603, 1%	Vishay	CRCW06034R99F

Also see *Detailed Design Procedure* above.

8.2.3.3 Application Curves

See *Application Curves* above.

9 Power Supply Recommendations

The LM26420-Q1 is designed to operate from an input voltage supply range between 3 V and 5.5 V. This input supply must be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LM26420-Q1 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LM26420-Q1, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-μF or 100-μF electrolytic capacitor is a typical choice.

LM26420-Q1 contains a high side PMOS FET and a low side NMOS FET as shown in Figure 42. The source nodes of the high side PMOS FETs are connected to $VIND_1$ and $VIND_2$ respectively. VINC is the power source for the high and low side gate drivers. Ideally, VINC is connected to $VIND_1$ and $VIND_2$ by an RC filter as detailed in VINC Filtering Components . If VINC is allowed to be lower than $VIND_1$ or $VIND_2$, the high side PMOS FETs may be turned on regardless of the state of the respective gate drivers. Under this condition, shoot through will occur when the low side NMOS FET is turned on and permanent damage may result. When applying input voltage to VINC, $VIND_1$ and $VIND_2$, VINC must not be less than $VIND_{1,2} – V_{TH}$ to avoid shoot through and FET damage.

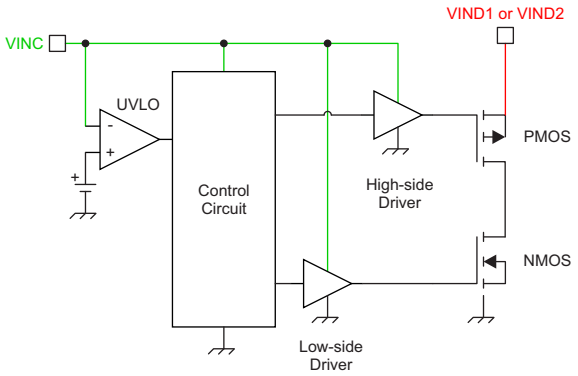


Figure 42. VINC, $VIND_1$ and $VIND_2$ Connection

10 Layout

10.1 Layout Guidelines

When planning layout there are a few things to consider when trying to achieve a clean, regulated output. The most important consideration is the close coupling of the GND connections of the input capacitor and the PGND pin. These ground ends must be close to one another and be connected to the GND plane with at least two through-holes. Place these components as close to the device as possible. Next in importance is the location of the GND connection of the output capacitor, which must be near the GND connections of VIND and PGND. There must be a continuous ground plane on the bottom layer of a two-layer board except under the switching node island. The FB pin is a high impedance node, and care must be taken to make the FB trace short to avoid noise pickup and inaccurate regulation. The feedback resistors must be placed as close to the device as possible, with the GND of R1 placed as close to the GND of the device as possible. The VOUT trace to R2 must be routed away from the inductor and any other traces that are switching. High AC currents flow through the VIN, SW, and VOUT traces, so they must be as short and wide as possible. However, making the traces wide increases radiated noise, so the designer must make this trade-off. Radiated noise can be decreased by choosing a shielded inductor. The remaining components must also be placed as close as possible to the device. See *AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines* for further considerations, and the LM26420-Q1 demo board as an example of a four-layer layout.

Layout Guidelines (continued)

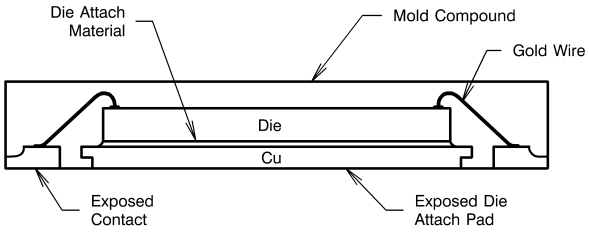


Figure 43. Internal Connection

For certain high power applications, the PCB land may be modified to a *dog bone* shape (see Figure 44). By increasing the size of ground plane, and adding thermal vias, the $R_{\theta JA}$ for the application can be reduced.

10.2 Layout Example

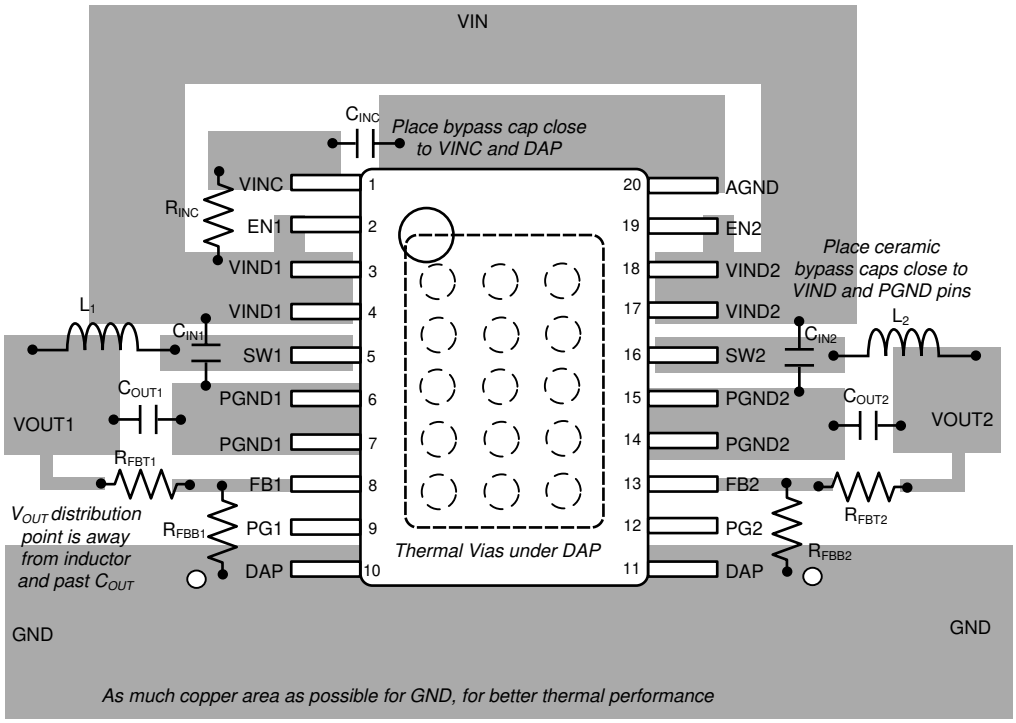


Figure 44. Typical Layout For DC/DC Converter

10.3 Thermal Considerations

T_J = Chip junction temperature

T_A = Ambient temperature

$R_{\theta JC}$ = Thermal resistance from chip junction to device case

$R_{\theta JA}$ = Thermal resistance from chip junction to ambient air

Heat in the LM26420-Q1 due to internal power dissipation is removed through conduction and/or convection.

Conduction: Heat transfer occurs through cross sectional areas of material. Depending on the material, the transfer of heat can be considered to have poor to good thermal conductivity properties (insulator vs conductor).

Heat Transfer goes as:

Thermal Considerations (continued)

Silicon → package → lead frame → PCB

Convection: Heat transfer is by means of airflow. This could be from a fan or natural convection. Natural convection occurs when air currents rise from the hot device to cooler air.

Thermal impedance is defined as:

$$R_\theta = \frac{\Delta T}{\text{Power}} \tag{35}$$

Thermal impedance from the silicon junction to the ambient air is defined as:

$$R_{\theta JA} = \frac{T_J - T_A}{P_{INTERNAL}} \tag{36}$$

The PCB size, weight of copper used to route traces and ground plane, and number of layers within the PCB can greatly affect $R_{\theta JA}$. The type and number of thermal vias can also make a large difference in the thermal impedance. Thermal vias are necessary in most applications. They conduct heat from the surface of the PCB to the ground plane. Five to eight thermal vias must be placed under the exposed pad to the ground plane if the WQFN package is used. Up to 12 thermal vias must be used in the HTSSOP-20 package for optimum heat transfer from the device to the ground plane.

Thermal impedance also depends on the thermal properties of the application's operating conditions (V_{IN}, V_{OUT}, I_{OUT}, etc.), and the surrounding circuitry.

10.3.1 Method 1: Silicon Junction Temperature Determination

To accurately measure the silicon temperature for a given application, two methods can be used. The first method requires the user to know the thermal impedance of the silicon junction to top case temperature.

Some clarification needs to be made before we go any further.

$R_{\theta JC}$ is the thermal impedance from silicon junction to the exposed pad.

$R_{\theta JT}$ is the thermal impedance from top case to the silicon junction.

In this data sheet $R_{\theta JT}$ is used so that it allows the user to measure top case temperature with a small thermocouple attached to the top case.

$R_{\theta JT}$ is approximately 20°C/W for the 16-pin WQFN package with the exposed pad. Knowing the internal dissipation from the efficiency calculation given previously, and the case temperature, which can be empirically measured on the bench we have:

$$R_{\theta JT} = \frac{T_J - T_T}{P_{INTERNAL}} \tag{37}$$

Therefore:

$$T_J = (R_{\theta JT} \times P_{INTERNAL}) + T_C \tag{38}$$

From the previous example:

$$T_J = 20°C/W \times 0.304W + T_C \tag{39}$$

10.3.2 Thermal Shutdown Temperature Determination

The second method, although more complicated, can give a very accurate silicon junction temperature.

The first step is to determine $R_{\theta JA}$ of the application. The LM26420-Q1 has over-temperature protection circuitry. When the silicon temperature reaches 165°C, the device stops switching. The protection circuitry has a hysteresis of about 15°C. Once the silicon junction temperature has decreased to approximately 150°C, the device starts to switch again. Knowing this, the $R_{\theta JA}$ for any application can be characterized during the early stages of the design one may calculate the $R_{\theta JA}$ by placing the PCB circuit into a thermal chamber. Raise the ambient temperature in the given working application until the circuit enters thermal shutdown. If the SW pin is monitored, it is obvious when the internal FETs stop switching, indicating a junction temperature of 165°C. Knowing the internal power dissipation from the above methods, the junction temperature, and the ambient temperature $R_{\theta JA}$ can be determined.

Thermal Considerations (continued)

$$R_{\theta JA} = \frac{165° - T_A}{P_{INTERNAL}} \quad (40)$$

Once this is determined, the maximum ambient temperature allowed for a desired junction temperature can be found.

An example of calculating $R_{\theta JA}$ for an application using the LM26420-Q1 WQFN demonstration board is shown below.

The four layer PCB is constructed using FR4 with 1 oz copper traces. The copper ground plane is on the bottom layer. The ground plane is accessed by eight vias. The board measures 3 cm × 3 cm. It was placed in an oven with no forced airflow. The ambient temperature was raised to 152°C, and at that temperature, the device went into thermal shutdown.

From the previous example:

$$P_{INTERNAL} = 304 \text{ mW} \quad (41)$$

$$R_{\theta JA} = \frac{165^oC - 152^oC}{304 \text{ mW}} = 42.8^o \text{ C/W} \quad (42)$$

If the junction temperature was to be kept below 125°C, then the ambient temperature could not go above 112°C.

$$T_J – (R_{\theta JA} \times P_{INTERNAL}) = T_A \quad (43)$$

$$125°C – (42.8°C/W \times 304 \text{ mW}) = 112.0°C \quad (44)$$

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

11.1.2 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designerにより、LM26420-Q1デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

11.2 ドキュメントのサポート

11.2.1 関連資料

『AN-1229 SIMPLE SWITCHER®のPCBレイアウト・ガイドライン』(SNVA054)

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商標

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM26420Q0XMH/NOPB	ACTIVE	HTSSOP	PWP	20	73	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM26420 Q0XMH	Samples
LM26420Q0XMHX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM26420 Q0XMH	Samples
LM26420Q1XMH/NOPB	ACTIVE	HTSSOP	PWP	20	73	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM26420 Q1XMH	Samples
LM26420Q1XMHX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM26420 Q1XMH	Samples
LM26420Q1XSQ/NOPB	ACTIVE	WQFN	RUM	16	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L26420Q	Samples
LM26420Q1XSQX/NOPB	ACTIVE	WQFN	RUM	16	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L26420Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

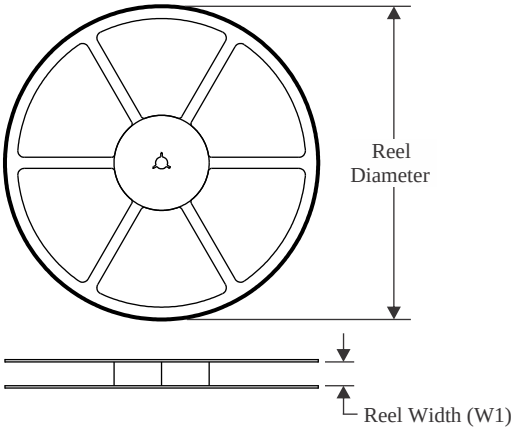
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

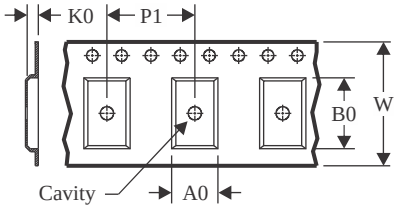
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

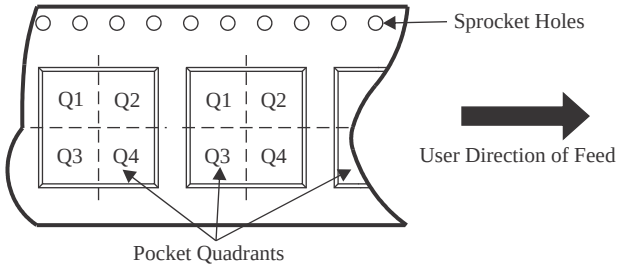


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

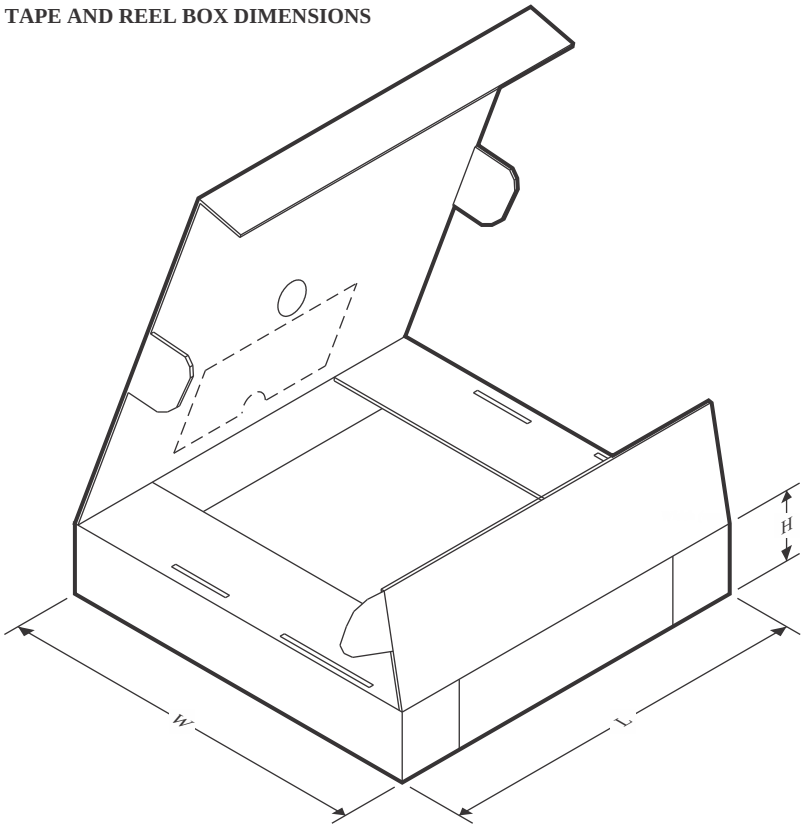
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM26420Q0XMHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
LM26420Q1XMHX/NOPB	HTSSOP	PWP	20	2500	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
LM26420Q1XSQ/NOPB	WQFN	RUM	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LM26420Q1XSQX/NOPB	WQFN	RUM	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

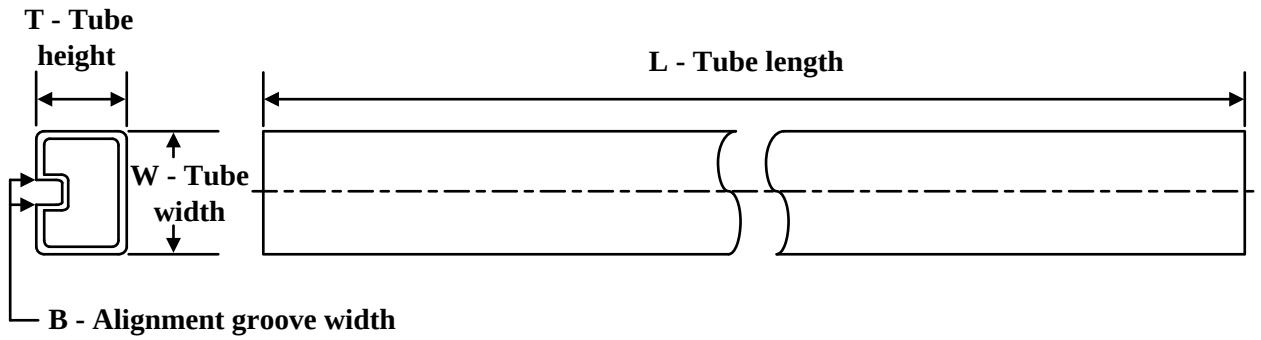
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM26420Q0XMHX/NOPB	HTSSOP	PWP	20	2500	367.0	367.0	35.0
LM26420Q1XMHX/NOPB	HTSSOP	PWP	20	2500	356.0	356.0	35.0
LM26420Q1XSQ/NOPB	WQFN	RUM	16	1000	208.0	191.0	35.0
LM26420Q1XSQX/NOPB	WQFN	RUM	16	4500	356.0	356.0	36.0

TUBE



*All dimensions are nominal

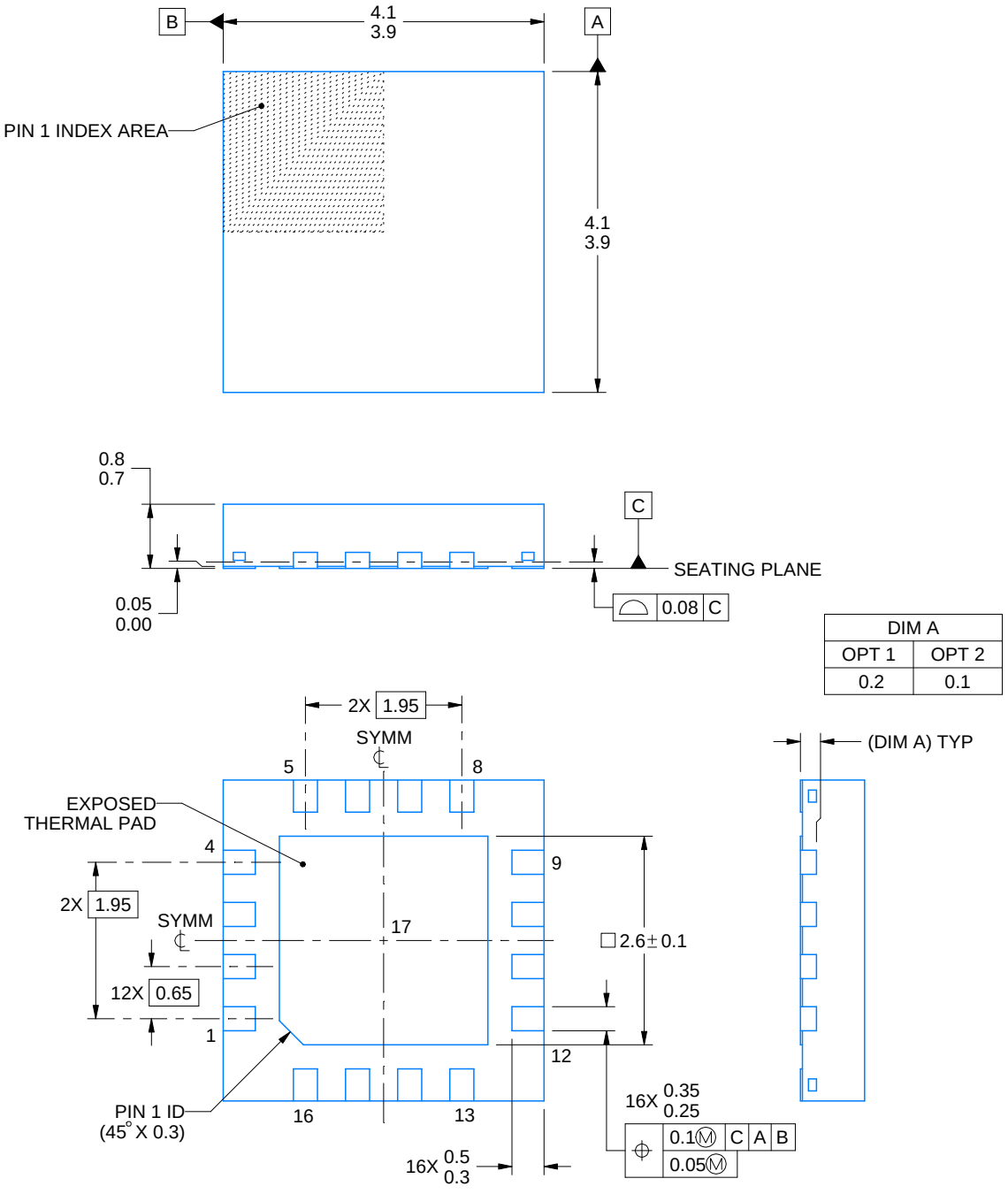
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM26420Q0XMH/NOPB	PWP	HTSSOP	20	73	495	8	2514.6	4.06
LM26420Q1XMH/NOPB	PWP	HTSSOP	20	73	495	8	2514.6	4.06

RUM0016A

PACKAGE OUTLINE

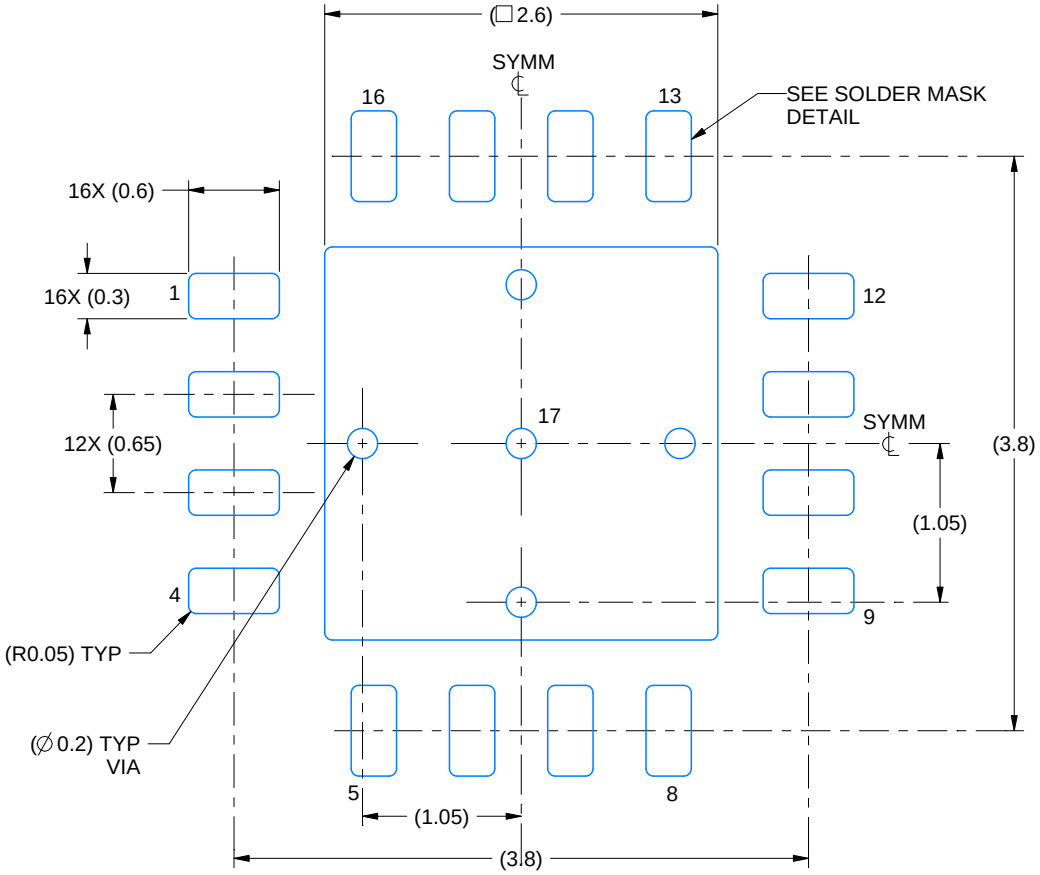
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

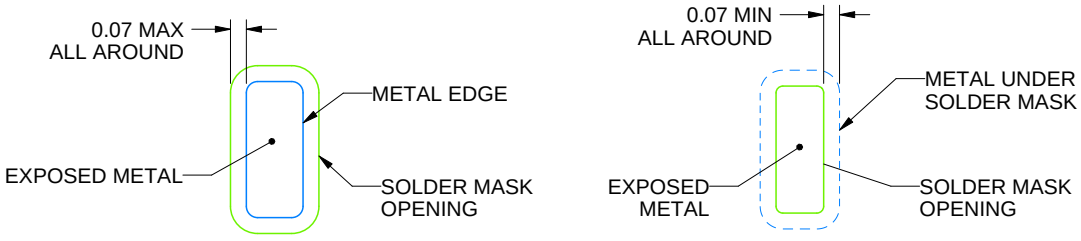


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214998/A 11/2021

NOTES: (continued)

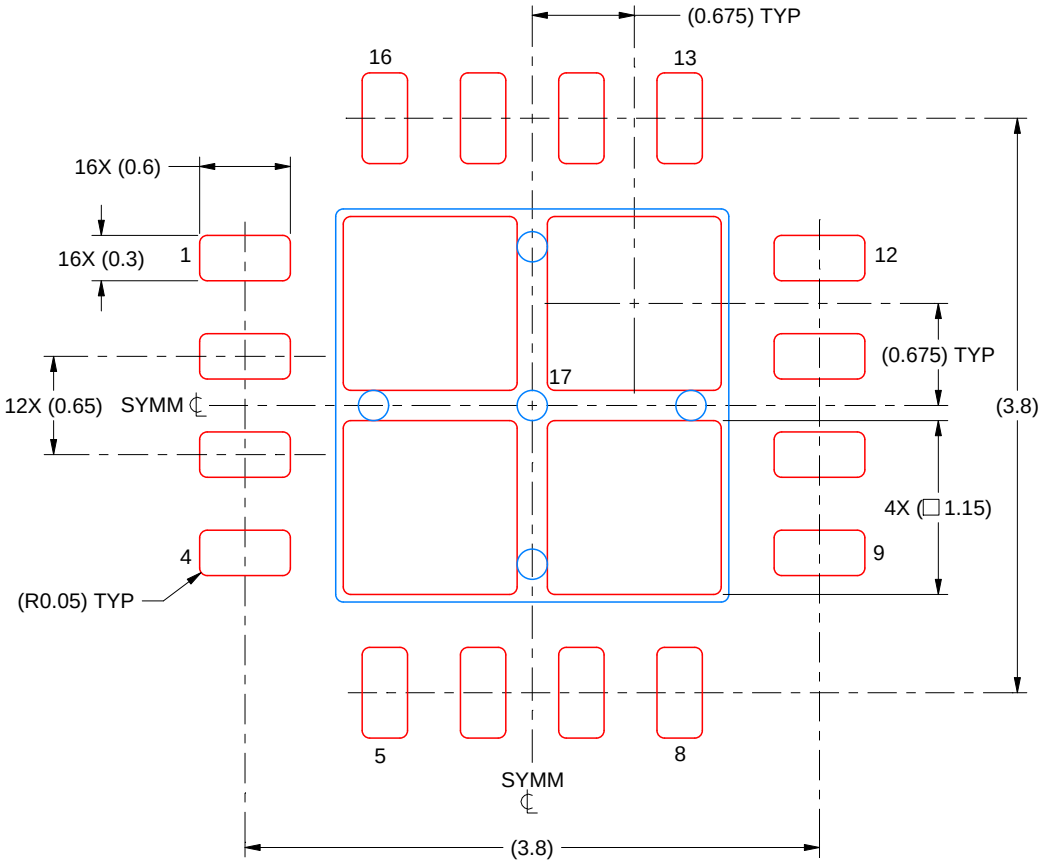
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RUM0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

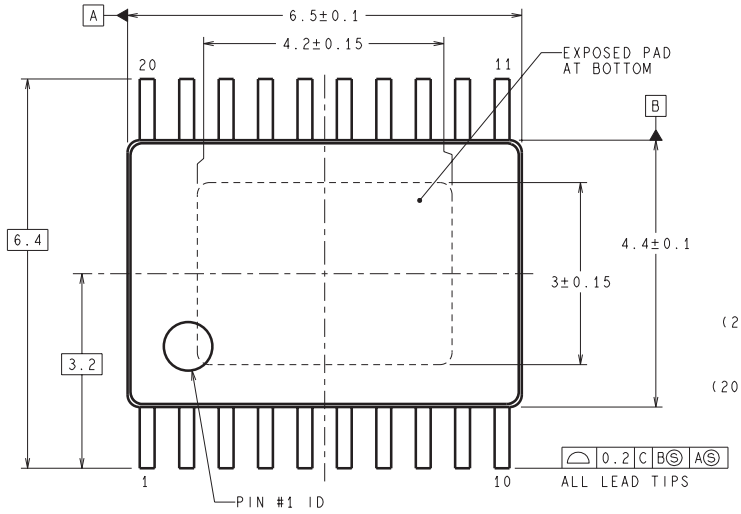
EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

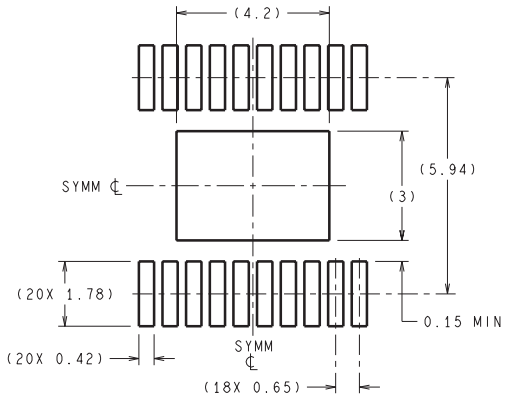
4214998/A 11/2021

NOTES: (continued)

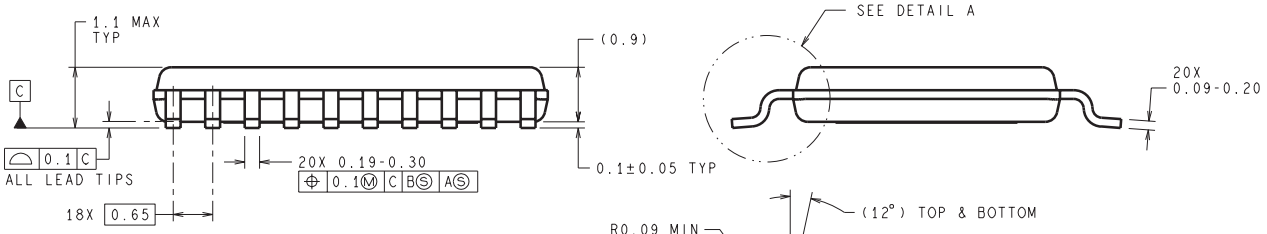
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

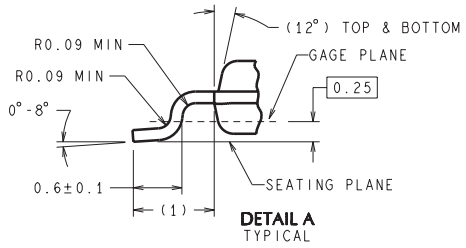
PWP0020A





RECOMMENDED LAND PATTERN





DETAIL A
TYPICAL

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

MXA20A (Rev C)

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265