TEXAS INSTRUMENTS
TPD3S014-Q1
JAJSJE7C – MARCH 2016 – REVISED AUGUST 2020

TPD3S014-Q1 車載 USB ホスト・ポート向け、電流制限スイッチと D+/D– ESD 保護機能

1 特長

- AEC-Q100 認定済み (グレード 2)
  - 周囲温度範囲:–40℃～+105℃
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 定格連続電流:0.5A
- 固定の定電流制限:0.85A (標準値)
- 高速な過電流応答:2µs (標準値)
- 出力放電内蔵
- 逆電流保護
- 短絡保護
- 過熱保護、自動再起動付き
- ソフトスタート機能内蔵
- IEC 61000-4-2 レベル 4 ESD 保護 (外部ピン)
  - 接触放電 ±12kV (IEC 61000-4-2)
  - エアギャップ放電 ±15kV (IEC 61000-4-2)
- ISO 10605 330pF、330Ω ESD 保護 (外部ピン)
  - 接触放電 ±8kV
  - エアギャップ放電 ±15kV
- 6 ピン SOT-23 パッケージ (2.90mm × 1.60mm)

2 アプリケーション

- 最終製品:
  - ヘッド・ユニット
  - リアシート用エンターテイメント
  - テレマティクス
  - USB ハブ
  - ナビゲーション・モジュール
- インターフェイス:
  - USB 2.0
  - USB 3.0

3 概要

TPD3S014-Q1 は、USB インターフェイス向けに電流制限型ロード・スイッチと 2 チャネル過渡電圧サプレッサ (TVS) ベースの静電気放電 (ESD) 保護ダイオード・アレイを内蔵した統合型デバイスです。

TPD3S014-Q1 デバイスは、USB のように短絡が発生する可能性の高い容量性の大負荷を駆動するアプリケーションを想定しています。TPD3S014-Q1 は、短絡保護機能と過電流保護機能を実装しています。TPD3S014-Q1 は、出力負荷が電流制限スレッショルドを上回ったとき定電流モードで動作することにより、出力電流を安全なレベルに制限します。高速な過負荷応答を達成していることから、出力の短絡が発生したときに電力を迅速に安定化して、メインの 5V 電源にかかる負荷を軽減します。電流制限スイッチの立ち上がり時間と立ち下がり時間は、デバイスをオンおよびオフにするときの電流サージを最小化するように制御されます。

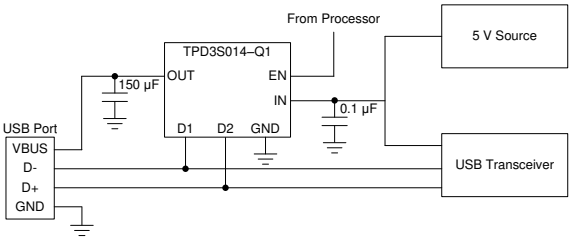
TPD3S014-Q1 は、 0.5A の連続電流を許容します。TVS ダイオード・アレイは、IEC 61000-4-2 国際規格で規定されている最大レベルを上回る ESD のエネルギーを吸収するように定格が設定されています。

高い統合レベルと、取り回しの容易な DBV パッケージの組み合わせにより、このデバイスは、ヘッド・ユニット、USB ハブ、メディア・インターフェイスなどのアプリケーションで、USB インターフェイスの優れた保護回路として利用できます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
TPD3S014-Q1	SOT-23 (6)	2.90mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (April 2016) to Revision C (August 2020) — **Page**

- *「特長」*セクションに機能安全のリンクを追加 ... 1
- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1

Changes from Revision A (April 2016) to Revision B (April 2016) — **Page**

- *電気的特性*の表を変更:*$–40°C \le T_A \le 105°C$*T_A を 125℃から 105℃に変更 ... 1
- *「消費電力および接合部温度」*セクションで温度を 125℃から 105℃に変更 ... 1

Changes from Revision * (March 2016) to Revision A (April 2016) — **Page**

- *デバイスのステータスを製品プレビューから量産データへ変更* ... 1

5 Pin Configuration and Functions

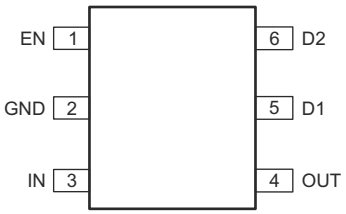


図 5-1. DBV Package 6-Pin SOT-23 Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
D1	5	I/O	USB data+ or USB data–
D2	6		
EN	1	I	Enable input, logic high turns on power switch
GND	2	—	Ground
IN	3	I	Input voltage and power-switch drain; Connect a 0.1-µF or greater ceramic capacitor from IN to GND close to the IC
OUT	4	O	Power-switch output, connect to load

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1) (2)

		MIN	MAX	UNIT
Input voltage(3)	V_{IN}	–0.3	6	V
	V_{OUT}	–0.3	6	
	EN	–0.3	6	
	D1	–0.3	6	
	D2	–0.3	6	
Voltage from V_{IN} to V_{OUT}		–6	6	V
Junction temperature	T_J	Internally limited		
Storage temperature	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltages are with respect to GND unless otherwise noted.
(3) See the *Input and Output Capacitance* section.

6.2 ESD Ratings—AEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2, V_{OUT}, Dx pins	Contact discharge(1)	±12000	V
			Air-gap discharge(1)	±15000	

(1) V_{OUT} was tested on a PCB with input and output bypassing capacitors of 0.1 µF and 120 µF, respectively.

6.4 ESD Ratings—ISO Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ISO 10605 330 pF, 330 Ω, V_{OUT}, Dx pins	Contact discharge(1)	±8000	V
			Air-gap discharge(1)	±15000	

(1) V_{OUT} was tested on a PCB with input and output bypassing capacitors of 0.1 µF and 120 µF, respectively.

6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	4.5	5.5	V
V_{EN}	Input voltage, EN	0	5.5	V
V_{IH}	High-level Input voltage, EN	2		V
V_{IL}	Low-level Input voltage, EN		0.7	V
C_{IN}	Input decoupling capacitance, IN to GND	0.1		µF
I_{OUT} (1)	Continuous output current (TPD3S014-Q1)		0.5	A
T_J	Operating junction temperature	–40	125	°C

(1) Package and current ratings may require an ambient temperature derating of 85°C

6.6 Thermal Information

THERMAL METRIC[1]		TPD3S014-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	124.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	23.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W
$R_{\theta JA}$ (Custom)	See the *Power Dissipation and Junction Temperature* section	120.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.7 Electrical Characteristics: $T_J = T_A = 25°C$

V_{IN} = 5 V, $V_{EN} = V_{IN}$, I_{OUT} = 0 A (unless otherwise noted). Parameters over a wider operational range are shown in *Electrical Characteristics: –40°C ≤ TA ≤ 105°C* table.

PARAMETER		TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
POWER SWITCH						
$R_{DS(on)}$	Input – Output resistance			97	120	mΩ
		–40°C ≤ (T_J, T_A) ≤ +85°C		97	140	
CURRENT LIMIT						
I_{OS} [2]	Current limit, see 図 8-3		0.67	0.85	1.01	A
SUPPLY CURRENT						
I_{SD}	Supply current, switch disabled	I_{OUT} = 0 A		0.02	1	µA
		–40°C ≤ (T_J, T_A) ≤ +85°C, V_{IN} = 5.5 V, I_{OUT} = 0 A			2	
I_{SE}	Supply current, switch enabled	I_{OUT} = 0 A		66	74	µA
		–40°C ≤ (T_J, T_A) ≤ +85°C, V_{IN} = 5.5 V, I_{OUT} = 0 A			85	
I_{REV}	Reverse leakage current	V_{OUT} = 5 V, V_{IN} = 0 V, Measure I_{VOUT}		0.2	1	µA
		–40°C ≤ (T_J, T_A) ≤ +85°C, V_{OUT} = 5 V, V_{IN} = 0 V, Measure I_{VOUT}			5	
OUTPUT DISCHARGE						
R_{PD}	Output pull-down resistance[3]	$V_{IN} = V_{OUT}$ = 5 V, disabled	400	456	600	Ω
ESD PROTECTION						
ΔC_{IO}	Differential capacitance between the D1, D2 lines	f = 1 MHz, V_{IO} = 2.5 V		0.02		pF
C_{IO}	(D1, D2 to GND)	f = 1 MHz, V_{IO} = 2.5 V		1.4		pF
R_{DYN}	Dynamic on-resistance D1, D2 IEC clamps[4]	Dx to GND		0.2		Ω
		GND to Dx		0.2		Ω

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature
(2) See the *Current Limit* for explanation of this parameter.
(3) These Parameters are provided for reference only, and do not constitute a part of TI's published device specifications for purposes of TI's product warranty.
(4) RDYN was extracted using the least squares first of the TLP characteristics between I = 20 A and I = 30 A.

6.8 Electrical Characteristics: –40°C ≤ T_A ≤ 105°C

4.5 V ≤ V_{IN} ≤ 5.5 V, V_{EN} = V_{IN}, I_{OUT} = 0 A, typical values are at 5 V and 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
POWER SWITCH						
$R_{DS(on)}$	Input – output resistance			97	164	mΩ
ENABLE INPUT (EN)						
	Threshold	Input rising	1	1.45	2	V
	Hysteresis			0.13		V
	Leakage current	V_{EN} = 0 V	–1	0	1	µA
t_{ON}	Turnon time	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, EN ↑ See 図 8-2	1	1.6	2.2	ms
t_{OFF}	Turnoff time	V_{IN} = 5 V, C_L = 1 µF, R_L = 100 Ω, EN ↓ See 図 8-2	1.7	2.1	2.7	ms
t_R	Rise time, output	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 5 V, See 図 8-1	0.4	0.64	0.9	ms
t_F	Fall time, output	C_L = 1 µF, R_L = 100 Ω, V_{IN} = 5 V, See 図 8-1	0.25	0.4	0.8	ms
CURRENT LIMIT						
I_{OS} [2]	Current limit, see 図 8-3		0.65	0.85	1.05	A
t_{IOS}	Short-circuit response time[2]	V_{IN} = 5 V (see 図 8-3) One Half full load → R_{SHORT} = 50 mΩ Measure from application to when current falls below 120% of final value		2		µs
SUPPLY CURRENT						
I_{SD}	Supply current, switch disabled	I_{OUT} = 0 A		0.02	10	µA
I_{SE}	Supply current, switch enabled	I_{OUT} = 0 A		66	94	µA
I_{REV}	Reverse leakage current	V_{OUT} = 5.5 V, V_{IN} = 0 V, Measure I_{VOUT}		0.2	20	µA
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	Rising threshold	V_{IN} ↑	3.5	3.77	4	V
	Hysteresis	V_{IN} ↓		0.14		V
OUTPUT DISCHARGE						
R_{PD}	Output pull-down resistance	V_{IN} = 4 V, V_{OUT} = 5 V, Disabled	350	545	1200	Ω
		V_{IN} = 5 V, V_{OUT} = 5 V, Disabled	300	456	800	
THERMAL SHUTDOWN						
T_{SHDN}	Rising threshold (T_J)	In current limit	135			°C
		Not in current limit	155			
	Hysteresis[3]			20		°C
ESD PROTECTION						
I_I	Input leakage current (D1, D2)	V_I = 3.3 V		0.02	1	µA
V_D	Diode forward voltage (D1, D2); Lower clamp diode	I_O = 8 mA			0.95	V
V_{BR}	Breakdown voltage (D1, D2)	I_{BR} = 1 mA	6			V

(1) Pulsed testing techniques maintain junction temperature approximately equal to ambient temperature
(2) See the *Current Limit* section for explanation of this parameter.
(3) These parameters are provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty.

6.9 Typical Characteristics

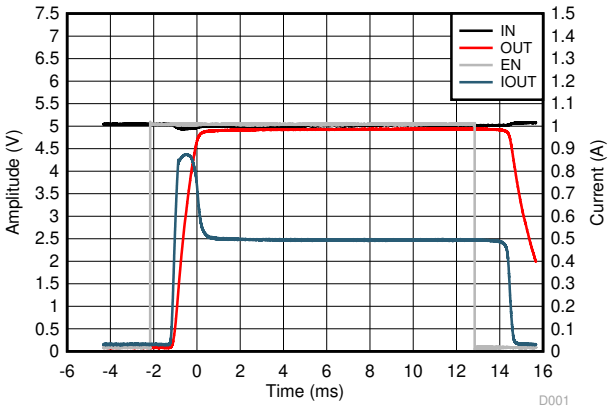


図 6-1. Turn ON into 10 Ω

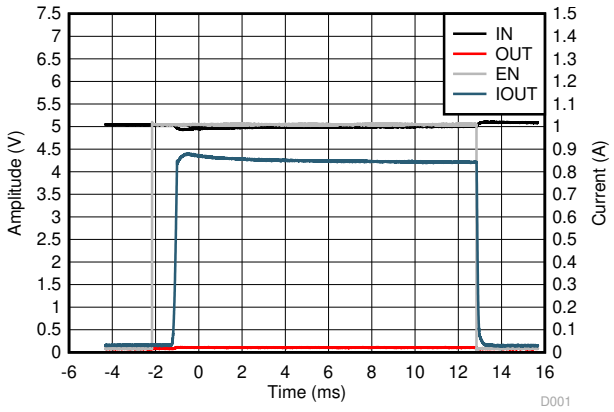


図 6-2. Enable into Short

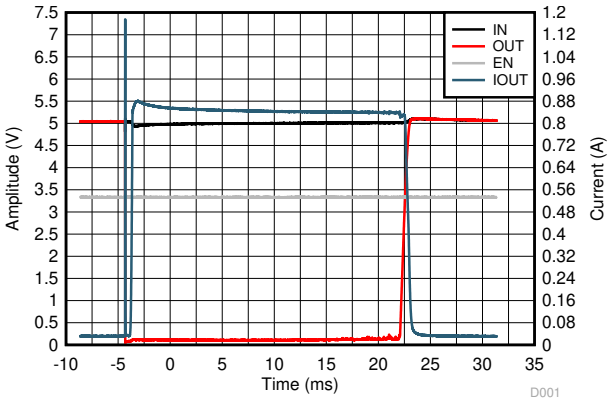


図 6-3. Pulsed Output Short

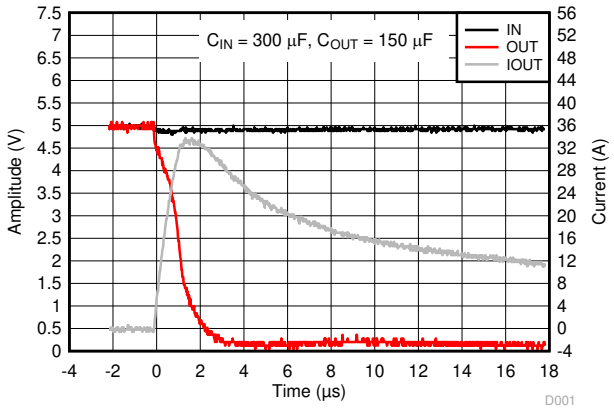


図 6-4. Short Applied

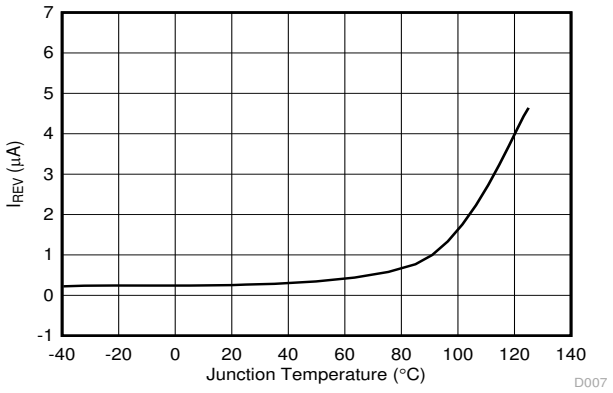


図 6-5. Reverse Leakage Current (I_{REV}) vs Temperature

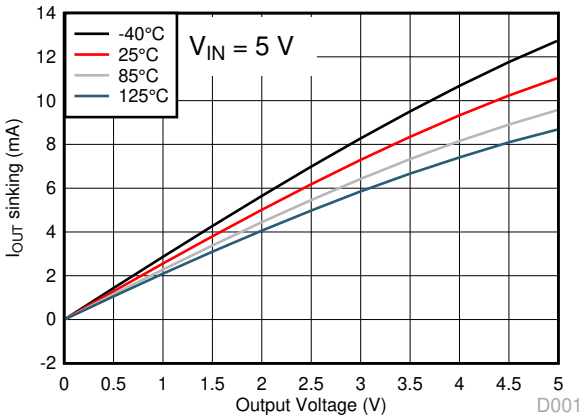


図 6-6. Output Discharge Current vs Output Voltage

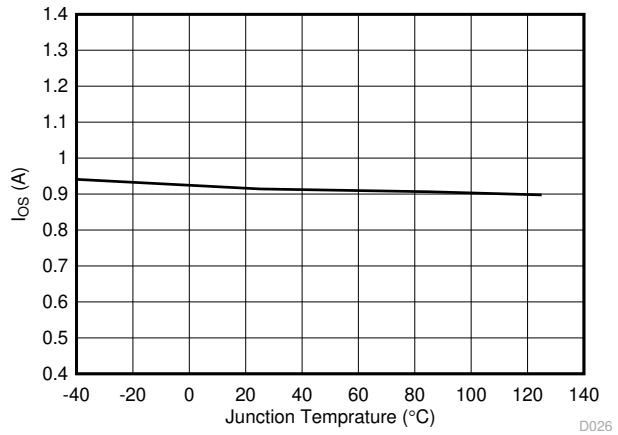


図 6-7. Short Circuit Current (I_{OS}) vs Temperature

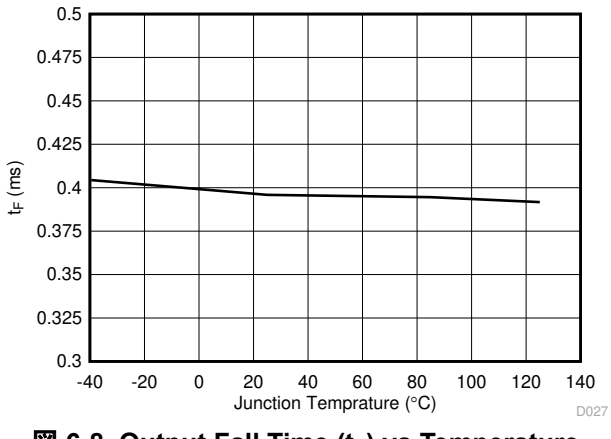


図 6-8. Output Fall Time (t_F) vs Temperature

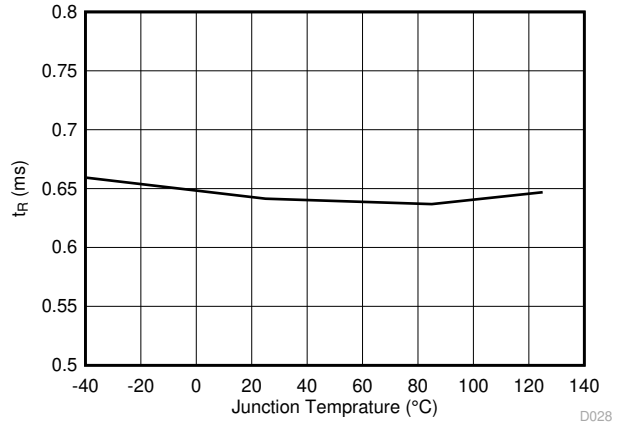


図 6-9. Output Rise Time (t_R) vs Temperature

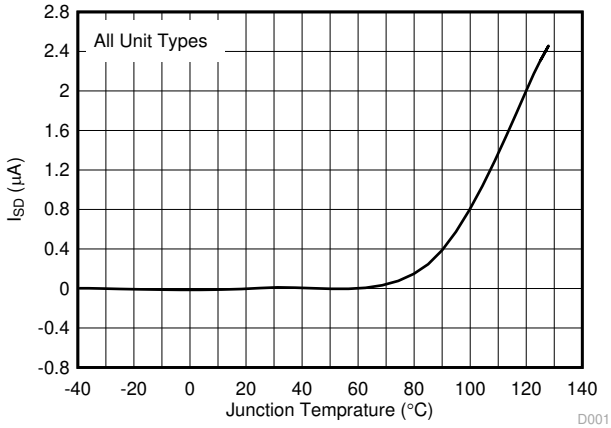


図 6-10. Disabled Supply Current (I_{SD}) vs Temperature

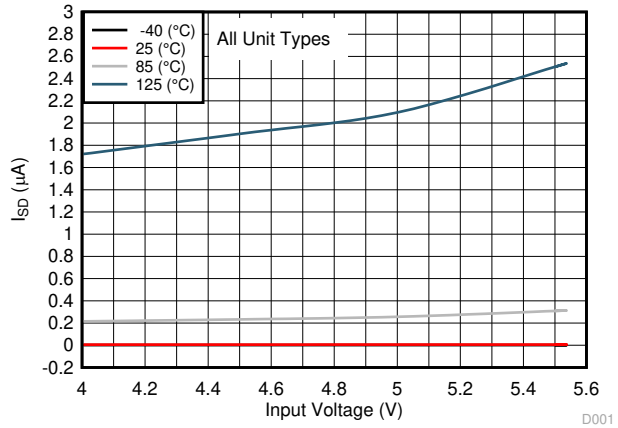


図 6-11. Disabled Supply Current (I_{SD}) vs Input Voltage

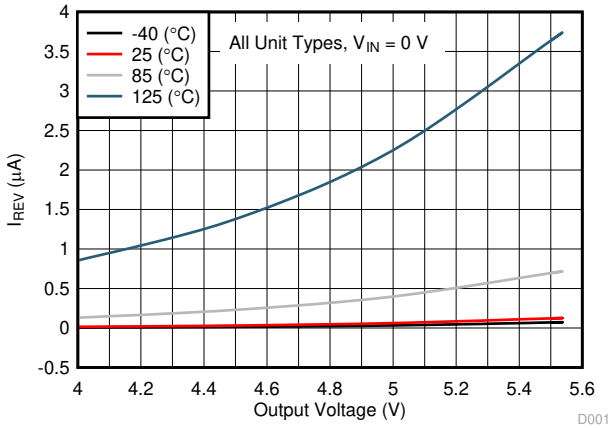


図 6-12. Reverse Leakage Current (I_{REV}) vs Output Voltage

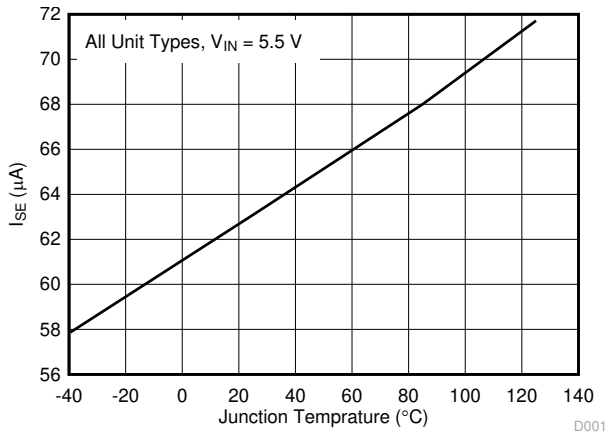


図 6-13. Enabled Supply Current (I_{SE}) vs Temperature

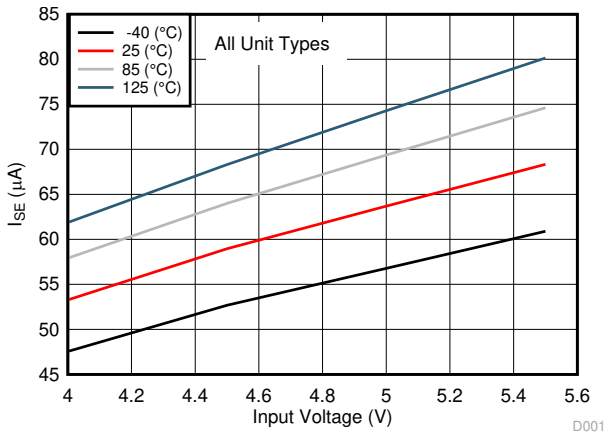


図 6-14. Enabled Supply Current (I_{SE}) vs Input Voltage

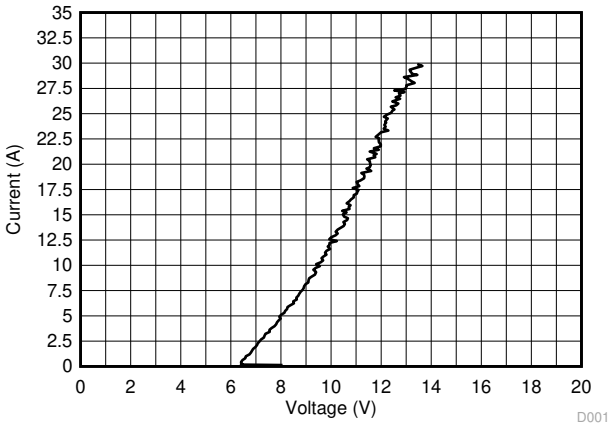


図 6-15. D1/D2 Positive TLP Curve

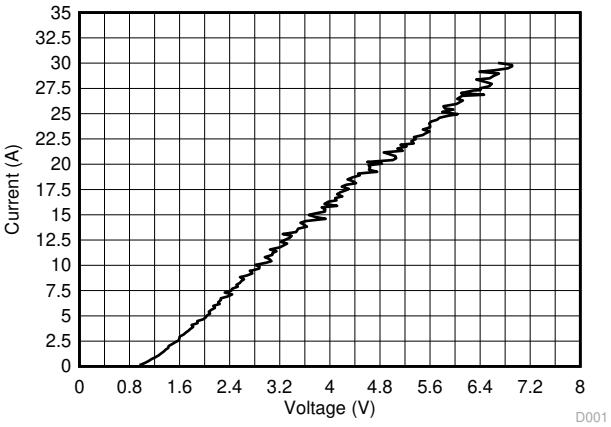


図 6-16. D1/D2 Negative TLP Curve

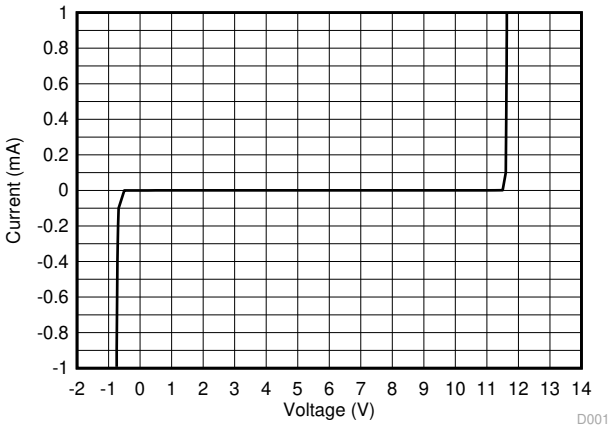


図 6-17. D1/D2 I-V Curve

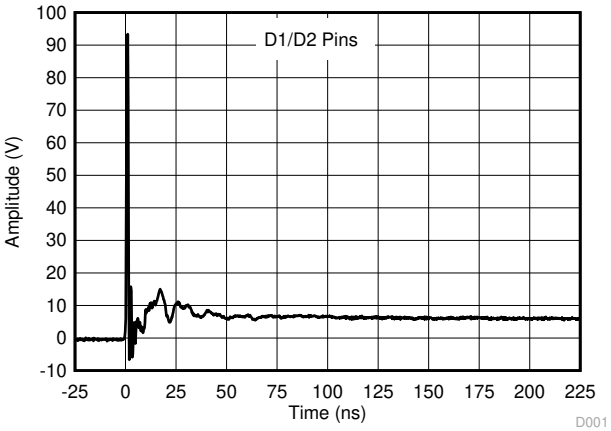


図 6-18. D1/D2 IEC 61000-4-2 8-kV Contact

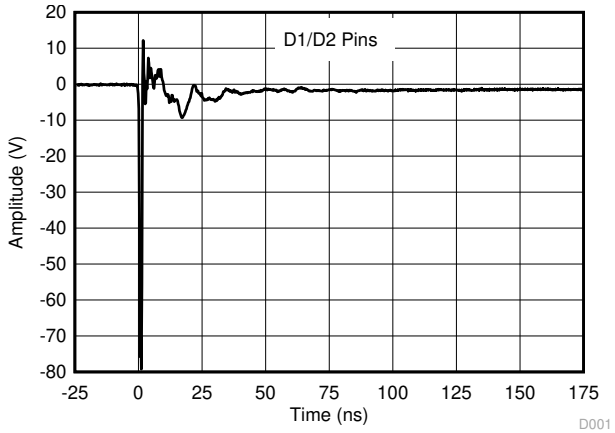
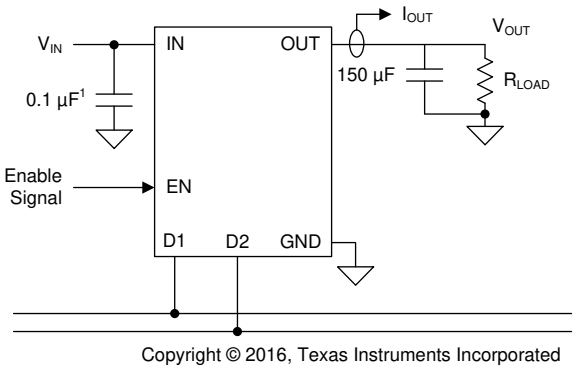


図 6-19. D1/D2 IEC 61000-4-2 –8-kV Contact

7 Parameter Measurement Information



A. During the short applied tests, 300 µF is used because of the use of an external supply.

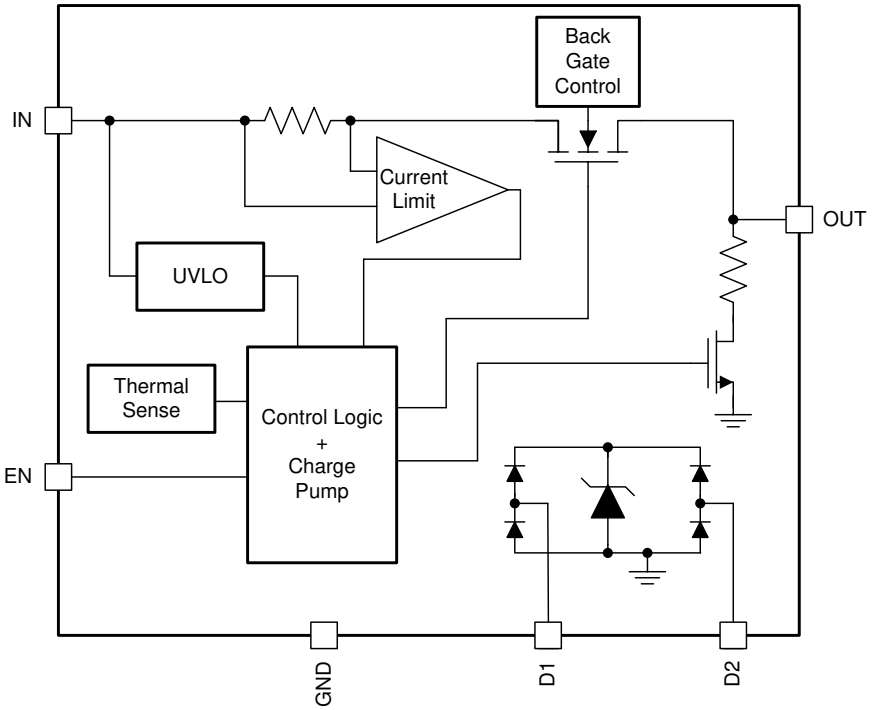
図 7-1. Test Circuit for System Operation

8 Detailed Description

8.1 Overview

The TPD3S014-Q1 is a highly integrated device that features a current limited load switch and a two-channel TVS based ESD protection diode array for USB interfaces. The TPD3S014-Q1 provides 0.5 A of continuous load current in 5 V circuits. This part uses N-channel MOSFETs for low resistance, maintaining voltage regulation to the load. It is designed for applications where short circuits or heavy capacitive loads will be encountered. Device features include enable, reverse blocking when disabled, output discharge pull-down, over-current protection, and over-temperature protection. Finally, with two channels of TVS ESD protection diodes integrated, the TPD3S014-Q1 provides system level ESD protection to all the pins of the USB port.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Undervoltage Lockout (UVLO)

The UVLO circuit disables the power switch until the input voltage reaches the UVLO turnon threshold. Built-in hysteresis prevents unwanted on and off cycling becuase of input voltage drop from large current surges.

8.3.2 Enable

The logic enable input (EN) controls the power switch, bias for the charge pump, driver, and other circuits. The supply current is reduced to less than 1 µA when the TPD3S014-Q1 is disabled. The enable input is compatible with both TTL and CMOS logic levels.

The turnon and turnoff times (t_{ON}, t_{OFF}) are composed of a delay and a rise or fall time (t_R, t_F). The delay times are internally controlled. The rise time is controlled by both the TPD3S014-Q1 and the external loading (especially capacitance). The TPD3S014-Q1 fall time is controlled by the loading (R and C), and the output discharge (R_{PD}). An output load consisting of only a resistor experiences a fall time set by the TPD3S014-Q1. An output load with parallel R and C elements experiences a fall time determined by the (R × C) time constant if it is longer than the TPD3S014-Q1 t_F. See 図 8-1 and 図 8-2 showing t_R, t_F, t_{ON}, and t_{OFF}. The enable must not be left open; it may be tied to V_{IN}.

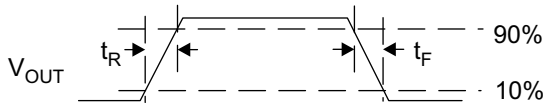


図 8-1. Power-On and Power-Off Timing

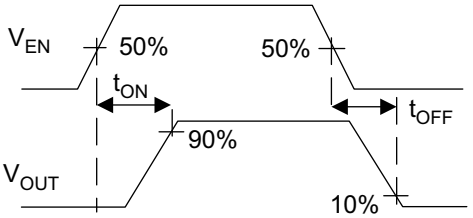


図 8-2. Enable Timing, Active-High Enable

8.3.3 Internal Charge Pump

The TPD3S014-Q1 incorporates an internal charge pump and gate drive circuitry necessary to drive the N-channel MOSFET. The charge pump supplies power to the gate driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The driver incorporates circuitry that controls the rise and fall times of the output voltage to limit large current and voltage surges on the input supply, and provides built-in soft-start functionality. The MOSFET power switch blocks current from OUT to IN when turned off by the UVLO or disabled.

8.3.4 Current Limit

The TPD3S014-Q1 responds to overloads by limiting output current to the static current-limit (IOS) levels shown in the *Electrical Characteristics: T_J = T_A = 25°C* table. When an overload condition is present, the device maintains a constant output current, with the output voltage determined by (I_{OS} × R_{LOAD}). Two possible overload conditions can occur.

The first overload condition occurs when either:

1. The input voltage is first applied, enable is true, and a short circuit is present (load which draws I_{OUT} > I_{OS})
   or
2. The input voltage is present and the TPD3S014-Q1 is enabled into a short circuit.

The output voltage is held near zero potential with respect to ground and the TPD3S014-Q1 ramps the output current to IOS. The TPD3S014-Q1 limits the current to IOS until the overload condition is removed or the device begins to thermal cycle. The device subsequently cycles current off and on as the thermal protection engages.

The second condition is when an overload occurs while the device is enabled and fully turned on. The device responds to the overload condition within t_{IOS} when the specified overload (per *Electrical Characteristics: T_J = T_A = 25°C*, Electrical Characteristics: –40°C ≤ T_A ≤ 105°C tables) is applied (See 図 8-3 and 図 8-4). The response speed and shape varies with the overload level, input circuit, and rate of application. The current-limit response varies between simply settling to I_{OS}, or turnoff and controlled return to I_{OS}. Similar to the previous case, the TPD3S014-Q1 limits the current to I_{OS} until the overload condition is removed or the device begins to thermal cycle.

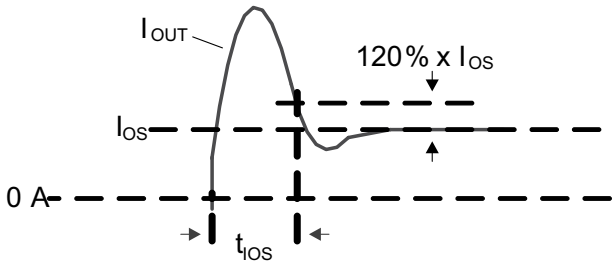


図 8-3. Output Short Circuit Parameters

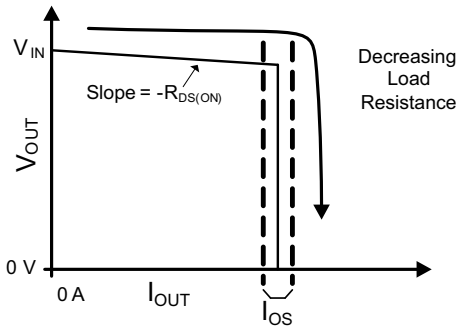


図 8-4. Output Characteristic Showing Current Limit

The TPD3S014-Q1 thermal cycles if an overload condition is present long enough to activate thermal limiting in any of the cases shown in 図 8-3 and 図 8-4. This is because of the relatively large power dissipation [(V_{IN} – V_{OUT}) × I_{OS}] driving the junction temperature up. The devices turn off when the junction temperature exceeds 135°C (minimum) while in current limit. The devices remains off until the junction temperature cools down to 20°C and then restarts.

There are two kinds of current limit profiles typically available in TI switch products similar to the TPD3S014-Q1. Many older designs have an output I vs V characteristic similar to the plot labeled "Current Limit with Peaking" in 図 8-5. This type of limiting can be characterized by two parameters, the current limit corner (I_{OC}), and the short circuit current (I_{OS}). I_{OC} is often specified as a maximum value. The TPD3S014-Q1 part does not present noticeable peaking in the current limit, corresponding to the characteristic labeled "Flat Current Limit" in 図 8-5. This is why the I_{OC} parameter is not present in the *Electrical Characteristics: T_J = T_A = 25°C*, Electrical Characteristics: –40°C ≤ T_A ≤ 105°C tables.

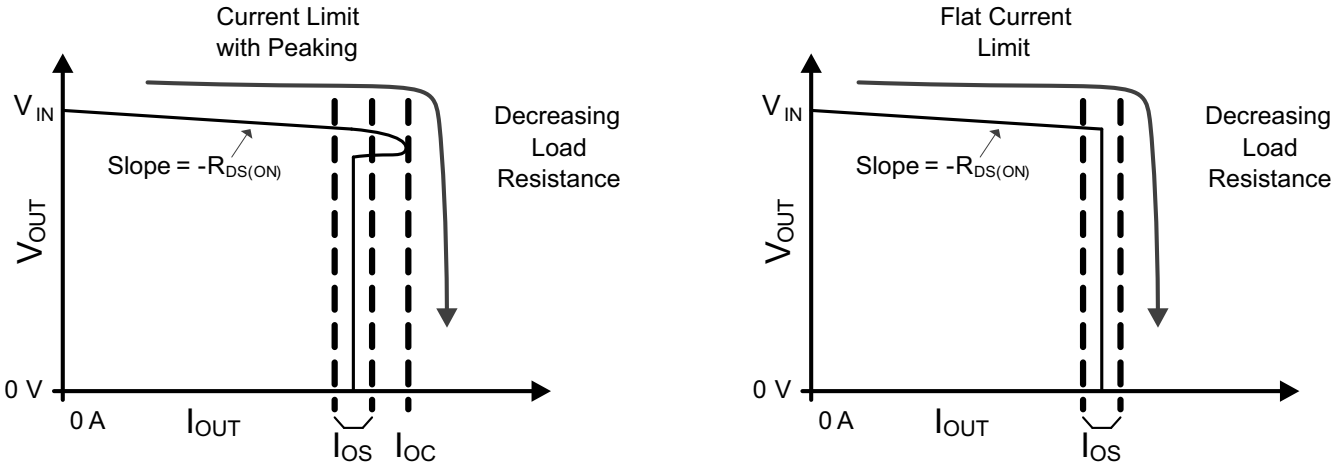


図 8-5. Current Limit Profiles

8.3.5 Output Discharge

A 470 Ω (typical) output discharge resistance dissipates stored charge and leakage current on OUT when the TPD3S014-Q1 is in UVLO or disabled. The pull-down circuit loses bias gradually as V_{IN} decreases, causing a rise in the discharge resistance as V_{IN} falls towards 0 V.

8.3.6 Input and Output Capacitance

Input and output capacitance improves the performance of the device; the actual capacitance must be optimized for the particular application. For all applications, a 0.1 µF or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.

All protection circuits such as the TPD3S014-Q1 has the potential for input voltage overshoots and output voltage undershoots.

Input voltage overshoots can be caused by either of two effects. The first cause is an abrupt application of input voltage in conjunction with input power bus inductance and input capacitance when the IN terminal is high impedance (before turnon). Theoretically, the peak voltage is 2 times the applied. The second cause is because of the abrupt reduction of output short circuit current when the TPD3S014-Q1 turns off and energy stored in the input inductance drives the input voltage high. Input voltage droops may also occur with large load steps and as the TPD3S014-Q1 output is shorted. Applications with large input inductance (for example, connecting the evaluation board to the bench power-supply through long cables) may require large input capacitance reduce the voltage overshoot from exceeding the absolute maximum voltage of the device. The fast current-limit speed of the TPD3S014-Q1 to hard output short circuits isolates the input bus from faults. However, ceramic input capacitance in the range of 1 µF to 22 µF adjacent to the TPD3S014-Q1 input aids in both speeding the response time and limiting the transient seen on the input power bus. Momentary input transients to 6.5 V are permitted.

Output voltage undershoot is caused by the inductance of the output power bus just after a short has occurred and the TPD3S014-Q1 has abruptly reduced OUT current. Energy stored in the inductance drives the OUT voltage down and potentially negative as it discharges. Applications with large output inductance (such as from a cable) benefit from use of a high-value output capacitor to control the voltage undershoot. When implementing USB standard applications, a 120-µF minimum output capacitance is required. Typically a 150- µF electrolytic capacitor is used, which is sufficient to control voltage undershoots. However, if the application does not require 120 µF of capacitance, and there is potential to drive the output negative, a minimum of 10-µF ceramic capacitance on the output is recommended. The voltage undershoot must be controlled to less than 1.5 V for 10 µs.

8.4 Device Functional Modes

8.4.1 Operation With V_{IN} < 4 V (Minimum V_{IN})

These devices operate with input voltages above 4 V. The maximum UVLO voltage on IN is 4 V and the devices will operate at input voltages above 4 V. Any voltage below 4 V may not work with these devices. The minimum UVLO is 3.5 V, so some devices may work between 3.5 V and 4 V. At input voltages below the actual UVLO voltage, these devices will not operate.

8.4.2 Operation With EN Control

The enable rising edge threshold voltage is 1.45 V typical and 2 V maximum. With EN held below that voltage the device is disabled and the load switch will be open. The IC quiescent current is reduced in this state. When the EN pin is above its rising edge threshold and the input voltage on the IN pin is above its UVLO threshold, the device becomes active. The load switch is closed, and the current limit feature is enabled. The output voltage on OUT ramps up with the soft start value T_{ON} in order to prevent large inrush current surges on V_{BUS} because of a heavy capacitive load. When EN voltage is lowered below is falling edge threshold, the device output voltage also ramps down with soft turnoff value T_{OFF} to prevent large inductive voltages being presented to the system in the case a large load current is following through the device.

8.4.3 Operation of Level 4 IEC 61000-4-2 ESD Protection

Regardless of which functional mode the devices are in, the TPD3S014-Q1 provides Level 4 IEC 61000-4-2 ESD Protection on the pins of the USB connector.

9 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The TPD3S014-Q1 is a device that features a current limited load switch and a two-channel TVS based ESD protection diode array. It is typically used to provide a complete protection solution for USB host ports. USB host ports are required by the USB specification to provide a current limit on the VBUS path in order to protect the system from overcurrent conditions on the port that could lead to system damage and user injury. Additionally, USB ports typically require system level IEC ESD protection because of direct end-user interaction. The following design procedure can be used to determine how to properly implement the TPD3S014-Q1 in your systems to provide a complete, one-chip solution for your USB ports.

9.2 Typical Application

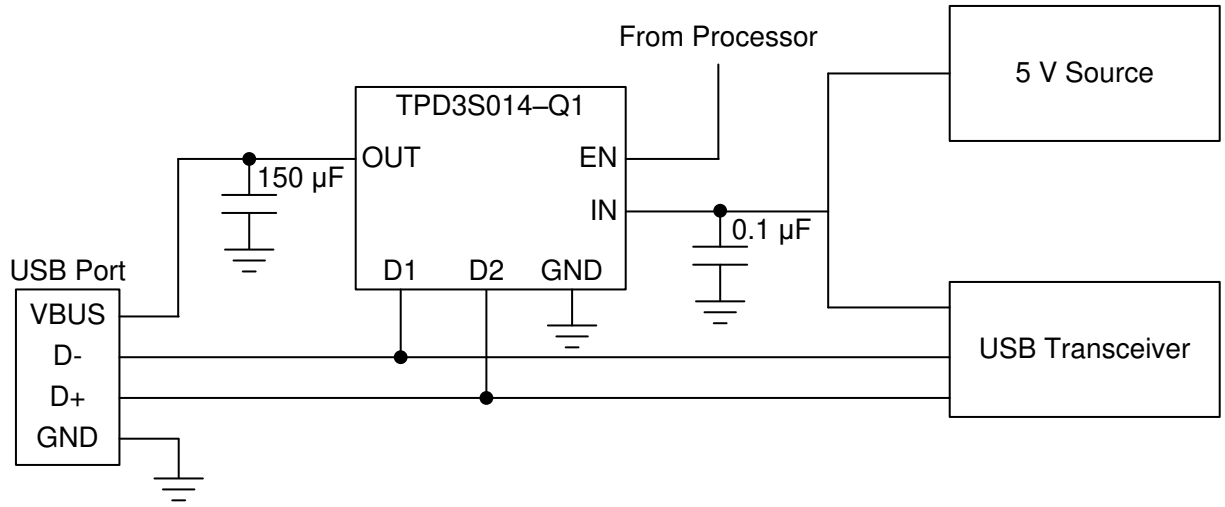


図 9-1. USB2.0 Application Schematic

9.2.1 Design Requirements

For this design example, design parameters shown in 表 9-1 are used.

表 9-1. Design Parameters

DESIGN PARAMETER	VALUE
USB port type	Standard downstream port
Signal voltage range on V_{BUS}	0 V to 5.25 V
Current range on V_{BUS}	0 mA to 500 mA
Drive EN low (disabled)	0 V to 0.7 V(1)
Drive EN high (enabled)	2 V to 5.5 V(1)
Maximum voltage droop allowed on adjacent USB port	330 mV
Maximum data rate	480 Mbps

(1) If active low logic is desired, see the *Implementing Active Low Logic* section.

9.2.2 Detailed Design Procedure

To properly implement your USB port with the TPD3S014-Q1, the first step is to determine what type of USB port is implemented in the system, whether it be a Standard Downstream Port (SDP), Charging Downstream Port (CDP), or Dedicated Charging Port (DCP); this informs us what maximum continuous operating current will be on VBUS. In our example, we are implementing an SDP port, so the maximum continuous current allowed to be pulled by a device is 500 mA. Therefore, we must choose a current limit switch that is 5.25 V tolerant, can handle 500 mA continuous DC current, and has a current limit point is above 500 mA so it will not current limit during normal operation. The TPD3S014-Q1 is therefore the best choice for this application, as it has these features, and in fact was specifically designed for this application.

The next decision point is choosing the input and output capacitors for the current limit switch. A minimum of 0.1 µF is always recommended on the IN pin. For the OUT pin on VBUS, USB standard requires a minimum of 120 µF; typically a 150 µF capacitor is used. The purpose of the capacitance requirement on the VBUS line in the USB specification is to prevent the adjacent USB port's VBUS voltage from dropping more than 330 mV during a hot-plug or fault occurrence on the VBUS pin of one USB port. Hot-plugs and fault conditions on one USB port must not disturb the normal operation of an adjacent USB port; therefore, it is possible to use an output capacitance lower than 120 µF if the system is able to keep voltage droops on adjacent USB ports less than or equal to 330 mV. For example, if the DC/DC powering VBUS has a fast transient response, 120 µF may not be required.

If the USB port is powered from a shared system 5 V rail, a system designer may desire to use an input capacitor larger than 0.1 µF on the IN pin. This is largely dependent on the PCB layout and parasitics, as well as your maximum tolerated voltage droop on the shared rail during transients. For more information on choosing input and output capacitors, see the *Input and Output Capacitance* section.

The EN pin controls the on and off state of the device, and typically is connected to the system processor for power sequencing. However, the EN pin can also be shorted to the IN pin to always have the TPD3S014-Q1 on when 5 V power supply on; this also saves a GPIO pin on your processor.

For a USB port with High-Speed 480 Mbps operation, low capacitance TVS ESD protection diodes are required to protect the D+ and D– lines in the event of system level ESD event. The TPD3S014-Q1 has 2-channels of low capacitance TVS ESD protection diodes integrated. When placed near the USB connector, the TPD3S014-Q1 offers little or no signal distortion during normal operation. The TPD3S014-Q1 also ensures that the core system circuitry is protected in the event of an ESD strike. PCB layout is critical when implementing TVS ESD protection diodes in your system. See the *Layout* section for proper guidelines on routing your USB lines with the TPD3S014-Q1.

9.2.3 Implementing Active Low Logic

For active low logic, a transistor can be used with the TPD3S014-Q1 EN Pin. 図 9-2 shows how to implement Active low logic for EN pin.

Using an nFET transistor, when the Processor sends a low signal, the transistor is switched off, and V_{LOGIC} pulls up EN through R_1. When the Processor sends a “high” signal, the nFET is switched on and sinks current from the EN Pin and R_1. For 5 V V_{LOGIC}, with the appropriate on-resistance (R_{ON}) value in the nFET and resistance for R_1, the V_{IL} for EN can be met. For example, with a transistor with R_{ON} of 3 Ω, a pull-up resistor as low as 11 Ω provides a logic level of 0.7 V. For power-budgeting concerns, a better choice is R_1 of 40 kΩ which provides 0.25 V for EN when the Processor asserts high, and 4.96 V when the Processor asserts low.

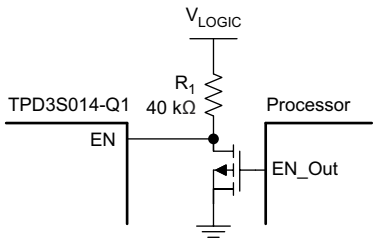


図 9-2. Implementing Active Low Logic for EN Pin

9.2.4 Application Curves

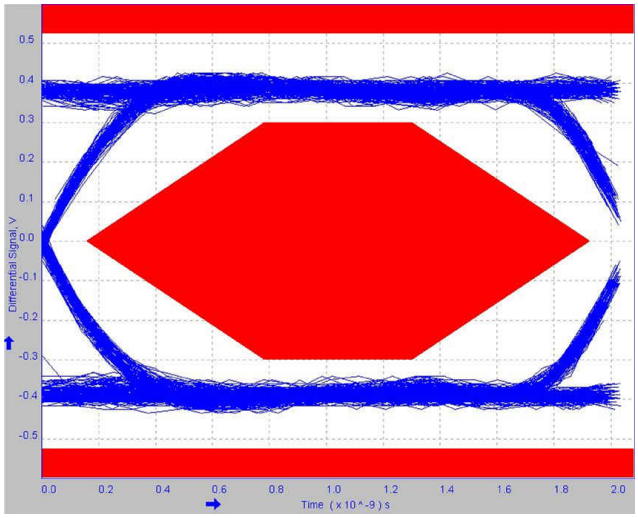


図 9-3. Eye-Diagram Without EVM

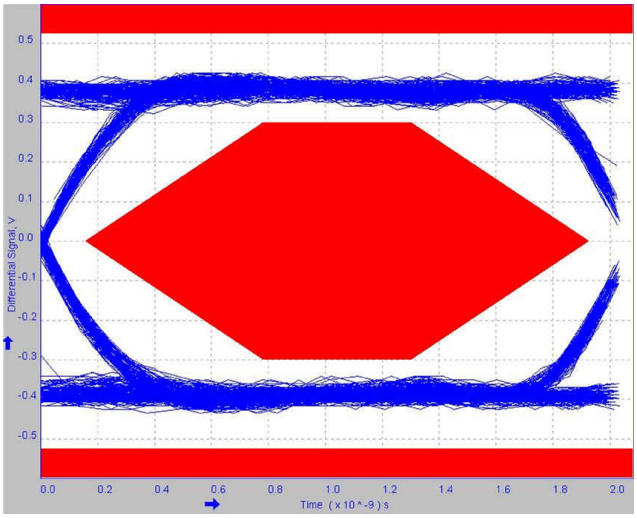


図 9-4. Eye-Diagram With EVM, Without TPD3S014-Q1

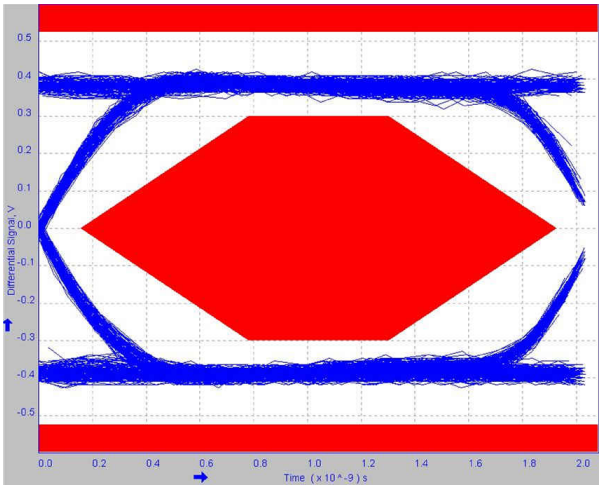


図 9-5. Eye-Diagram of TPD3S014-Q1 on EVM

10 Power Supply Recommendations

The TPD3S014-Q1 is designed to operate from a 5-V input voltage supply. This input must be well regulated. If the input supply is located more than a few inches away from the TPD3S014-Q1, additional bulk capacitance may be required in addition to the recommended minimum 0.1-µF bypass capacitor on the IN pin to keep the input rail stable during fault events.

11 Layout

11.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

11.2 Layout Example

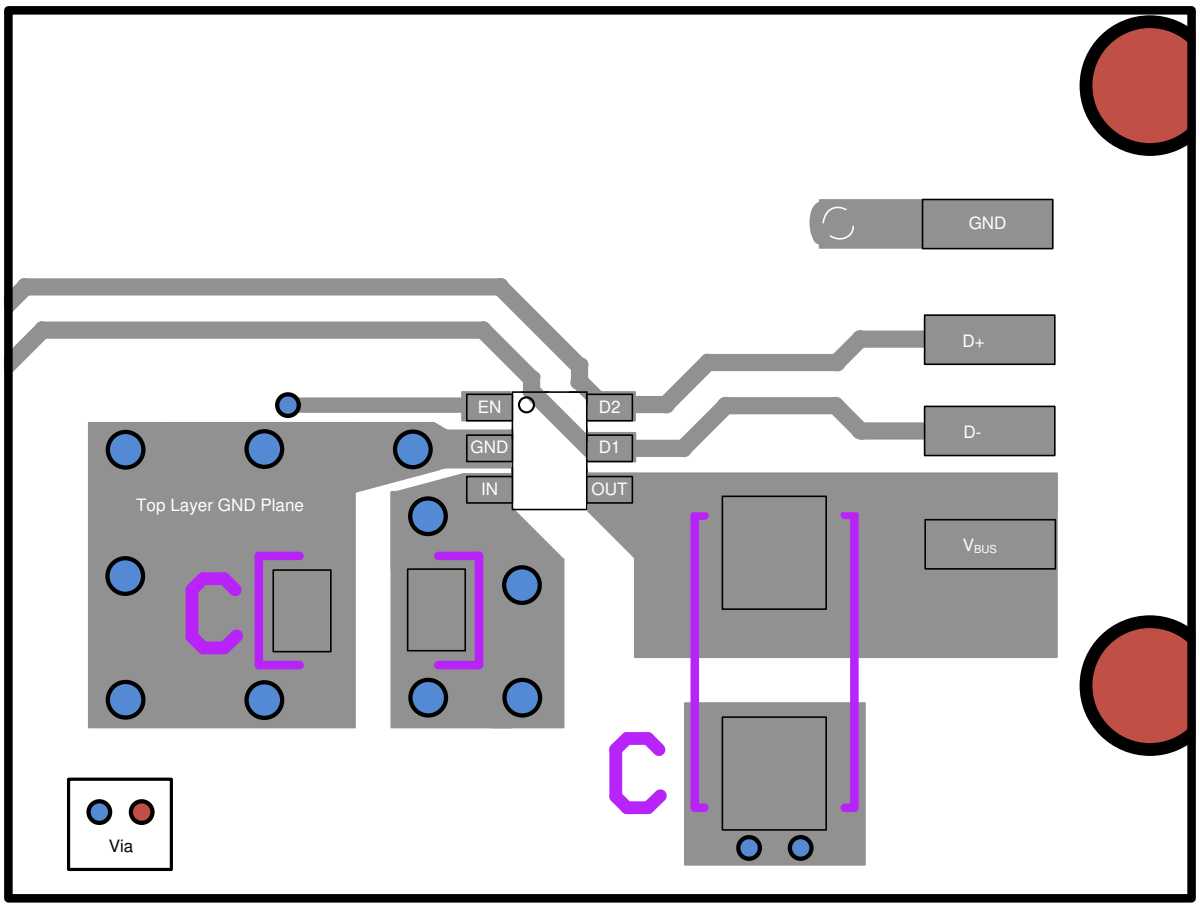


図 11-1. USB2.0 Type A TPD3S014-Q1 Board Layout

11.3 Power Dissipation and Junction Temperature

anged Temperature from 125°C to 105°C in Power Dissipation and Junction Temperature section

It is good design practice to estimate power dissipation and maximum expected junction temperature of the TPD3S014-Q1. The system designer can control choices of the devices proximity to other power dissipating devices and printed circuit board (PCB) design based on these calculations. These have a direct influence on maximum junction temperature. Other factors, such as airflow and maximum ambient temperature, are often determined by system considerations. It is important to remember that these calculations do not include the effects of adjacent heat sources, and enhanced or restricted air flow. Addition of extra PCB copper area around these devices is recommended to reduce the thermal impedance and maintain the junction temperature as low as practical. In particular, connect the GND pin to a large ground plane for the best thermal dissipation. The following PCB layout example in 図 11-2 was used to determine the $R_{\theta JA}$ Custom thermal impedances noted in the *Thermal Information* table. It is based on the use of the JEDEC high-k circuit board construction with 4, 1 oz. copper weight layers (2 signal and 2 plane).

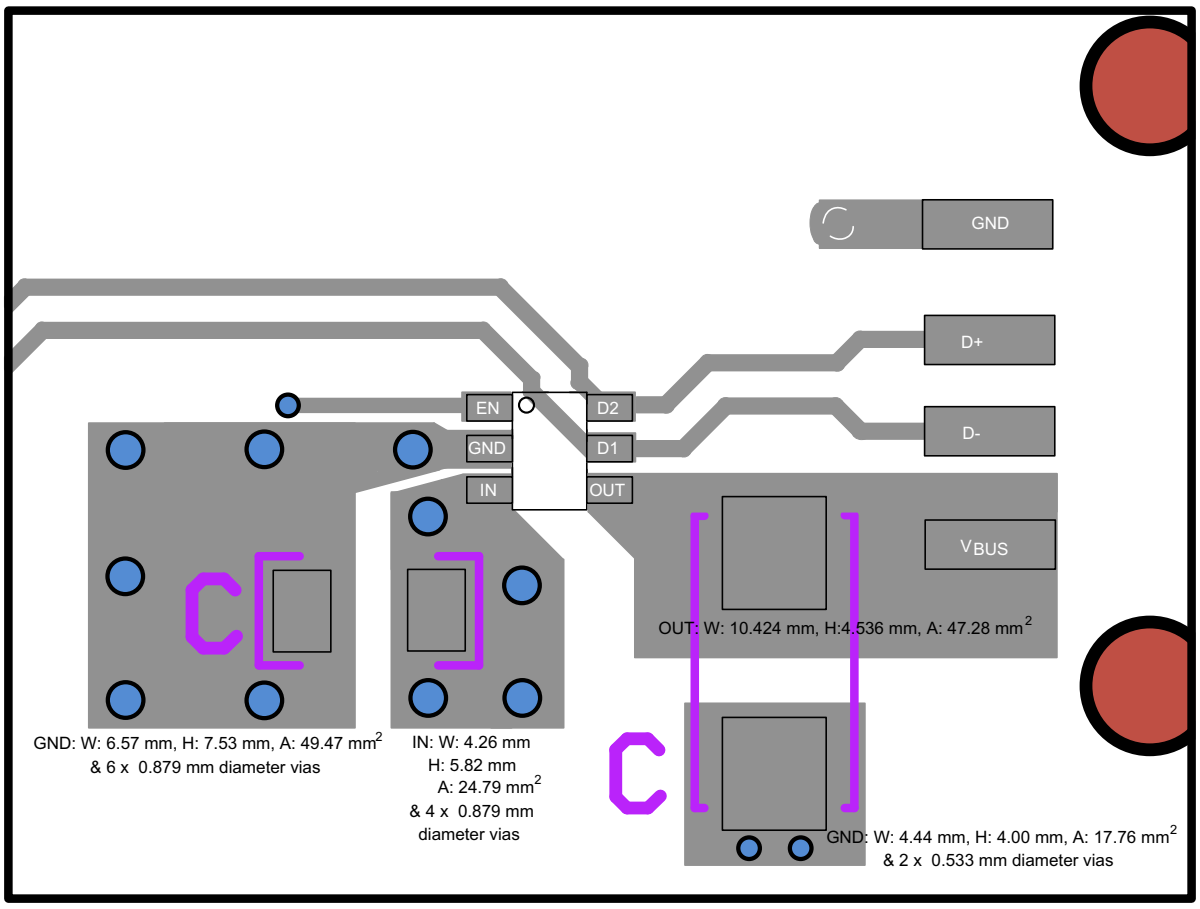


図 11-2. PCB Layout Example

The following procedure requires iteration a power loss is because of the internal MOSFET $I^2 \times R_{DS(ON)}$, and $R_{DS(ON)}$ is a function of the junction temperature. See 式 1. As an initial estimate, use the $R_{DS(ON)}$ at 105°C from the *Typical Characteristics*, and the preferred package thermal resistance for the preferred board construction from the *Thermal Information* table.

$$T_J = T_A + [(I_{OUT}{}^2 \times R_{DS(ON)}) \times R_{\theta JA}] \quad (1)$$

where

- I_{OUT} = Rated OUT pin current (A)
- $R_{DS(ON)}$ = Power switch on-resistance at an assumed T_J (Ω)
- T_A = Maximum ambient temperature (°C)
- T_J = Maximum junction temperature (°C)

- $R_{\theta JA}$ = Thermal resistance (°C/W)

If the calculated T_J is substantially different from the original assumption, estimate a new value of $R_{DS(ON)}$ using the typical characteristic plot and recalculate.

If the resulting T_J is not less than 125°C, try a PCB construction with a lower $R_{\theta JA}$. The junction temperature derating curve based on the TI standard reliability duration is shown in 図 11-3.

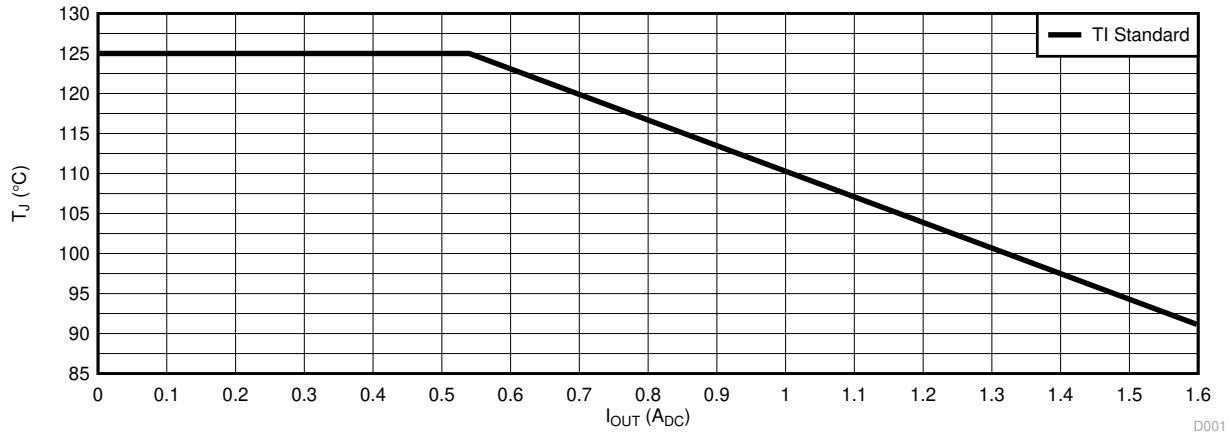


図 11-3. Junction Temperature Derating Curve

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

TPD3S014-Q1EVM User's Guide, SLVUAQ0.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

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12.4 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD3S014TDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 105	13WW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

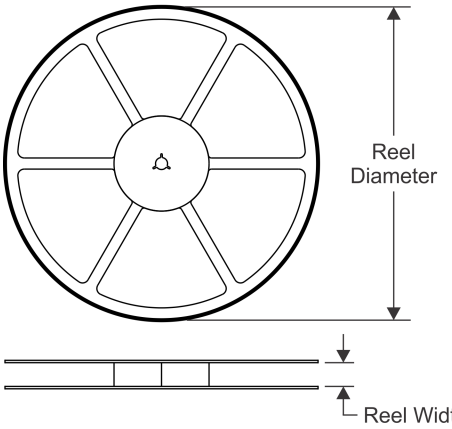
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

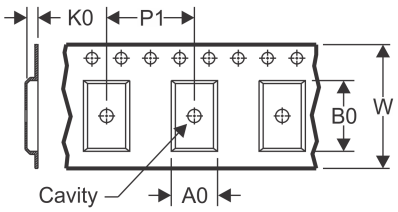
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

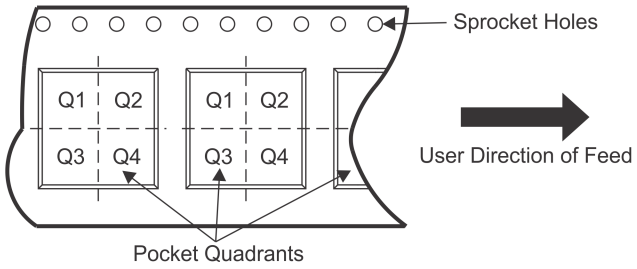


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

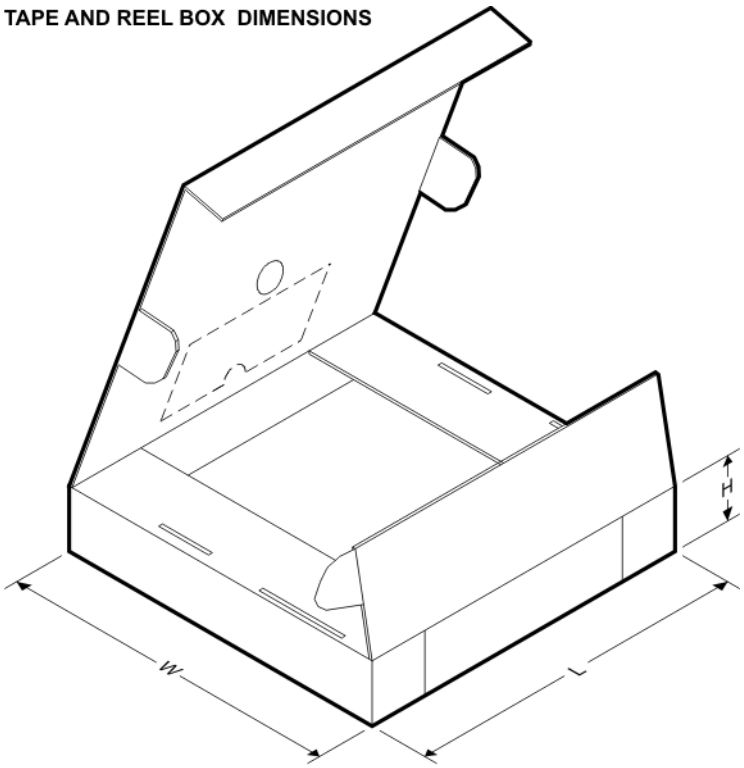
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD3S014TDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

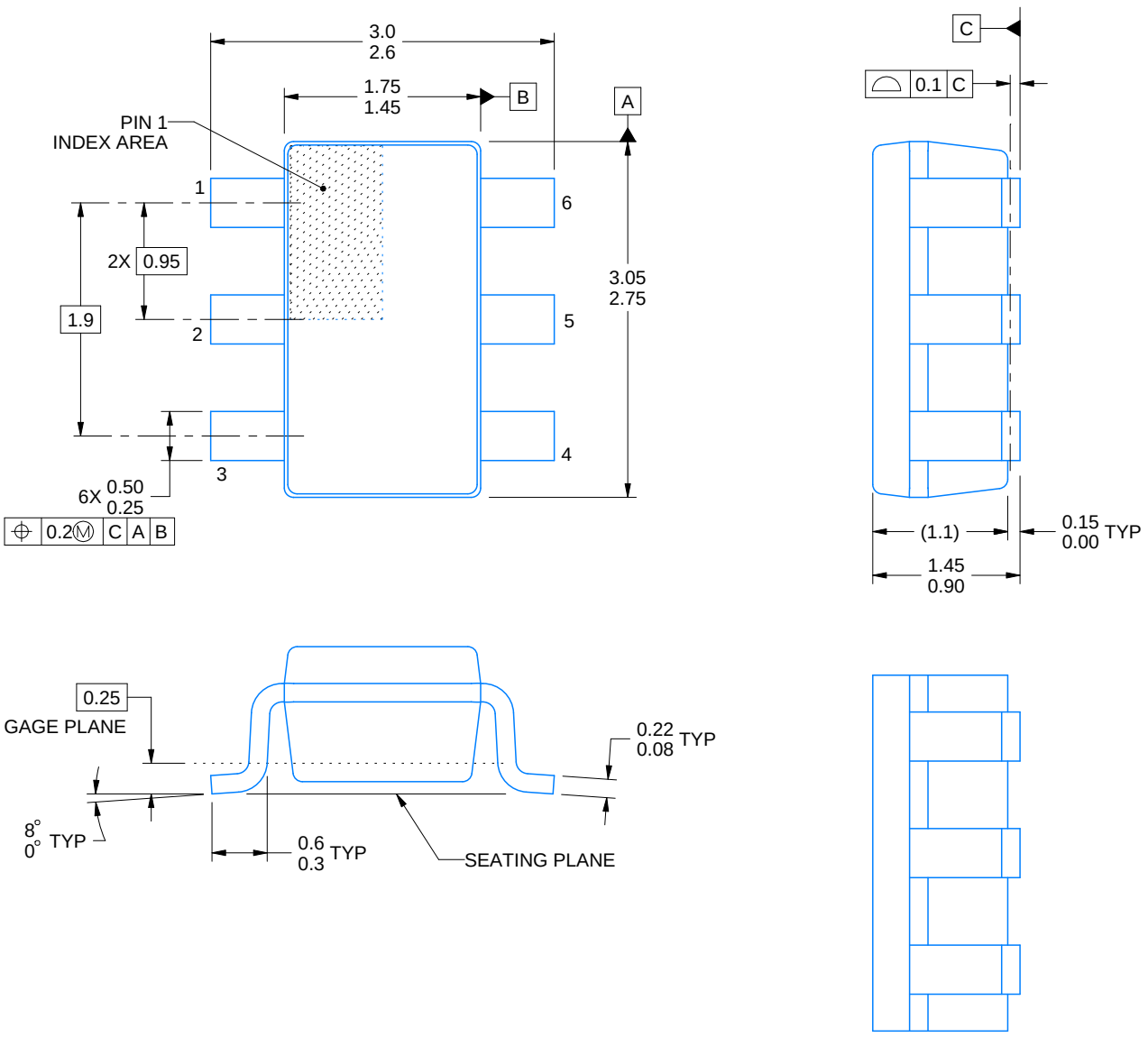
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD3S014TDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

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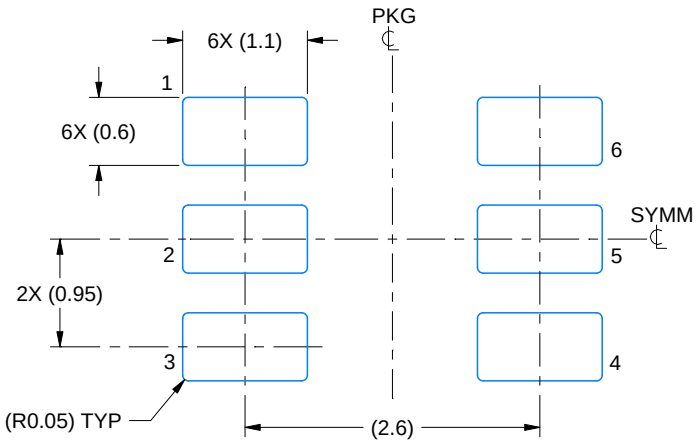
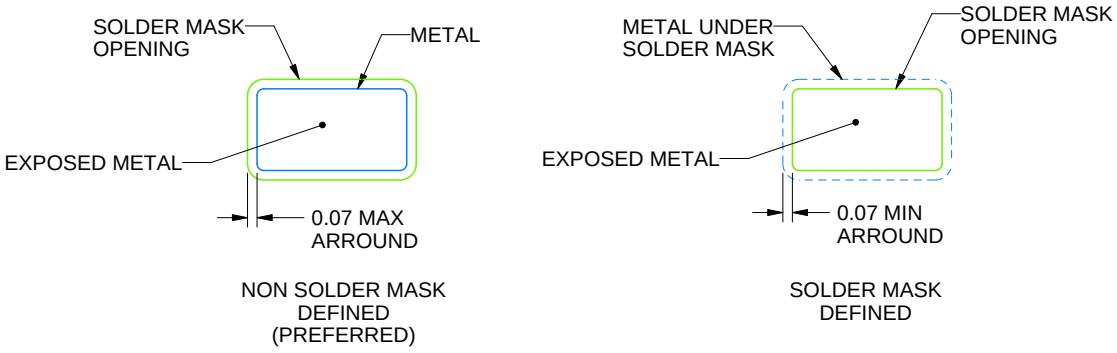
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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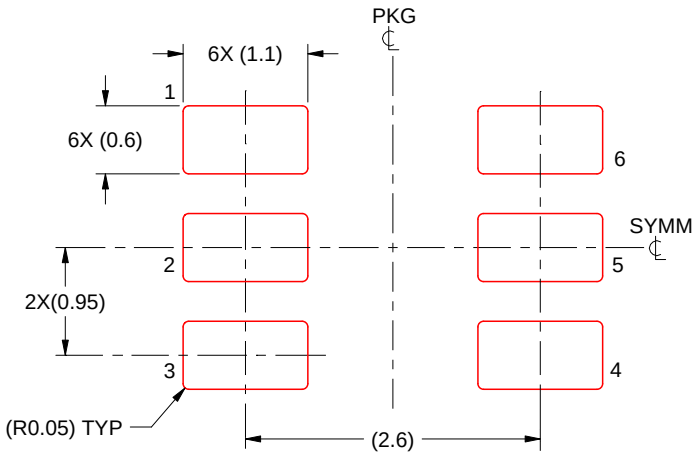
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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