LM73100 2.7～23V、5.5A の統合型理想ダイオード、入力逆極性および過電圧保護機能付き

1 特長

- 広い動作時入力電圧範囲:2.7V～23V
  - 絶対最大定格:28V
  - -15V までの負の電圧に対応
- 低いオン抵抗を持つバック・ツー・バック FET を内蔵: R_{ON} = 28.4mΩ (標準値)
- 真の逆電流ブロックによる理想ダイオード動作
- 高速過電圧保護
  - 応答時間 1.2µs (標準値)
  - 調整可能な過電圧誤動作防止 (OVLO)
- 定常状態での過渡過電流に対する高速トリップ応答
  - 応答時間 500ns (標準値)
  - フォルト後のラッチオフ
- アナログ負荷電流のモニタ出力 (IMON)
  - 電流範囲:0.5A～5.5A
  - 精度:±15% (最大値) (I_{OUT} ≧ 1A)
- アクティブ High のイネーブル入力、低電圧誤動作防止 (UVLO) スレッショルドを設定可能
- 可変の出力スルーレート (dVdt) 制御
- 過熱保護
- 可変スレッショルド (PGTH) 付きのパワー・グッド表示 (PG)
- 小型サイズ:QFN 2mm × 2mm (0.45mm ピッチ)

2 アプリケーション

- パワー・マルチプレクサ / OR 接続
- アダプタの入力保護
- セット・トップ・ボックス / スマート・スピーカ
- USB PD ポート保護回路
- PC / ノート PC / モニタ / ドック
- 電動工具 / 充電器
- POS 端末

3 概要

LM73100 は、小型のパッケージに回路保護と電源管理の機能を高密度に統合した製品です。本デバイスは、非常に少数の外付け部品で複数の保護モードを提供し、電圧サージ、逆極性、逆電流、および過剰な突入電流に対して堅牢な保護を行います。

バック・ツー・バック FET の内蔵により、出力から入力への逆電流フローが常にブロックされるので、本デバイスはパワー・マルチプレクサ / OR 接続アプリケーションに最適です。このデバイスは、リニア OR 接続ベースの方式を採用し、DC 逆電流がほぼ 0 であるため、順方向電圧降下と消費電力が最小限の理想ダイオードの動作をエミュレートできます。

特定の突入電流要件を持つアプリケーションでは、1 つの外付けコンデンサにより出力スルーレートを設定できます。入力が過電圧スレッショルド (調整可能) を上回った場合は、出力を遮断することにより負荷を入力過電圧状態から保護します。また、このデバイスは、定常状態での過渡過電流イベントに対する高速トリップ応答も実現します。

このデバイスは、アナログ電流モニタ・ピンの出力負荷電流を正確に検出します。

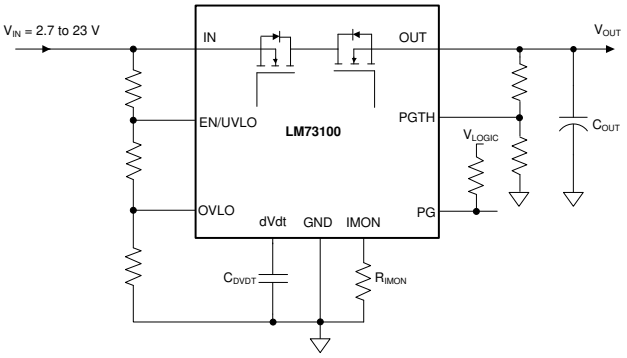
本デバイスは、2mm × 2mm、10 ピンの HotRod QFN パッケージで供給され、放熱性能の向上とシステムのフットプリント削減に役立ちます。

本デバイスは、-40℃～+125℃の接合部温度範囲で動作が規定されています。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
LM73100RPW	QFN (10)	2mm × 2mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (October 2020) to Revision A (December 2020)	Page
• ステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

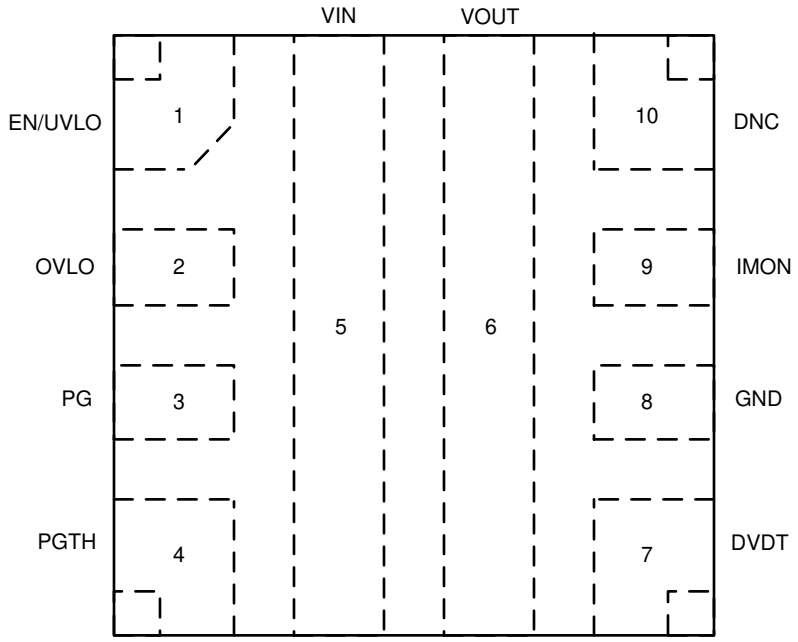


図 5-1. LM73100 RPW Package 10-Pin QFN Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN/UVLO	1	Analog Input	Active High Enable for the device. A Resistor Divider on this pin from input supply to GND can be used to adjust the Undervoltage Lockout threshold. **Do not leave floating.** Refer to セクション 7.3.2 for more details.
OVLO	2	Analog Input	A Resistor Divider on this pin from supply to GND can be used to adjust the Overvoltage Lockout threshold. This pin can also be used as an Active Low Enable for the device. **Do not leave floating.** Refer to セクション 7.3.3 for more details.
PG	3	Digital Output	Power Good indication. This is an Open Drain signal which is asserted High when the internal powerpath is fully turned ON and PGTH input exceeds a certain threshold. Refer to セクション 7.3.9 for more details.
PGTH	4	Analog Input	Power Good Threshold. Refer to セクション 7.3.9 for more details.
IN	5	Power	Power Input.
OUT	6	Power	Power Output.
DVDT	7	Analog Output	A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest turn on slew rate. Refer to セクション 7.3.4.1 for more details.
GND	8	Ground	This is the ground reference for all internal circuits and must be connected to system GND.
IMON	9	Analog Output	Analog load current monitor. The pin voltage can be used to monitor the output load current. An external resistor from this pin to ground sets the current monitor gain. Recommended to connect external clamp to limit the voltage below abs max rating in case of large current spikes. Connect to ground if not used. **Do not leave floating.** Refer to セクション 7.3.5 for more details.
DNC	10	X	Internal test pin. Do not connect anything on this pin.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range, –40 °C ≤ T_J ≤ 125 °C	IN	max (–15, V_{OUT} - 21)	28	V
	Maximum Input Voltage Range, –10 °C ≤ T_J ≤ 125 °C		max (–15, V_{OUT} - 22)	28	V
V_{OUT}	Maximum Output Voltage Range, –40 °C ≤ T_J ≤ 125 °C	OUT	–0.3	min (28, V_{IN} + 21)	
	Maximum Output Voltage Range, –10 °C ≤ T_J ≤ 125 °C		–0.3	min (28, V_{IN} + 22)	
$V_{OUT,PLS}$	Minimum Output Voltage Pulse (< 1 µs)	OUT	–0.8		
$V_{EN/UVLO}$	Maximum Enable Pin Voltage Range (2)	EN/UVLO	–0.3	6.5	V
V_{OVLO}	Maximum OVLO Pin Voltage Range (2)	OVLO	–0.3	6.5	V
V_{dVdT}	Maximum dVdT Pin Voltage Range	dVdt	Internally Limited		V
V_{PGTH}	Maximum PGTH Pin Voltage Range (2)	PGTH	–0.3	6.5	V
V_{PG}	Maximum PG Pin Voltage Range	PG	–0.3	6.5	V
V_{IMON}	Maximum IMON Pin Voltage Range	IMON		1.8	V
I_{MAX}	Maximum Continuous Switch Current	IN to OUT	5.5		A
T_J	Junction temperature		Internally Limited		°C
T_{LEAD}	Maximum Lead Temperature			300	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If this pin has a pull-up up to V_{IN}, it is recommended to use a resistance of 350 kΩ or higher to limit the current under conditions where IN can be exposed to reverse polarity.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input Voltage Range	IN	2.7	23	V
V_{OUT}	Output Voltage Range	OUT		min (23, V_{IN} + 20)	V
$V_{EN/UVLO}$	Enable Pin Voltage Range	EN/UVLO		5 (2)	V
V_{OVLO}	OVLO Pin Voltage Range	OVLO	0.5	1.5	V
V_{dVdT}	dVdT Capacitor Voltage Rating	dVdt	V_{IN} + 5 V (1)		V
V_{PGTH}	PGTH Pin Voltage Range	PGTH		5 (3)	V
V_{PG}	PG Pin Voltage Range	PG		5 (3)	V
V_{IMON}	IMON Pin Voltage	IMON		1.5	V
I_{MAX}	Continuous Switch Current, , T_J ≤ 125 ℃	IN to OUT		5.5	A
T_J	Junction temperature		–40	125	°C

(1) In a PowerMUX/ORing scenario with unequal supplies, the dVdt capacitor rating for each device should be chosen based on the highest of the 2 rails.
(2) For supply voltages below 5V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 5V or systems which can be exposed to reverse polarity on input supply, it is recommended to use a pull-up resistor with a minimum value of 350 kΩ.
(3) For systems which can be exposed to reverse polarity on input supply, if this pin is referred to input supply, it is recommended to use a pull-up resistor with a minimum value of 350 kΩ to limit the current through the pin.

6.4 Thermal Information

THERMAL METRIC (1)		LM73100 RPW (QFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.7 (2)	°C/W
		74.5 (3)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20 (2)	°C/W
		27.6 (3)	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Based on simulations conducted with the device mounted on a custom 4-layer PCB (2s2p) with 8 thermal vias under device
(3) Based on simulations conducted with the device mounted on a JEDEC 4-layer PCB (2s2p) with no thermal vias under device

6.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V, dVdT = Open, R_{IMON} = 549 Ω, PGTH = Open, PG = Open, OUT = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)					
$V_{UVP(R)}$	IN supply UVP rising threshold	2.44	2.53	2.64	V
$V_{UVP(F)}$	IN supply UVP falling threshold	2.35	2.42	2.55	V
$I_{Q(ON)}$	IN supply quiescent current, V_{IN} = 2.7 V		347	492	µA
	IN supply quiescent current, V_{IN} = 12 V		426	509	µA
	IN supply quiescent current, V_{IN} = 23 V		459	612	µA
$I_{Q(RCB)}$	IN supply quiescent current during RCB, V_{OUT} > V_{IN}		189.7	234	µA
$I_{Q(OFF)}$	IN supply disabled state current ($V_{SD(F)}$ < V_{EN} < $V_{UVLO(R)}$)		74.5	97.6	µA
I_{SD}	IN supply shutdown current (V_{EN} < $V_{SD(F)}$)		4.6	8.2	µA
$I_{Q(OVLO)}$	IN supply OFF state current (OVLO condition), V_{OUT} > V_{IN}		191		µA
$I_{INLKG(IRPP)}$	IN supply leakage current (V_{IN} = –14 V, V_{OUT} = 0 V)		-3.5		µA
ON RESISTANCE (IN - OUT)					
R_{ON}	V_{IN} = 12 V, I_{OUT} = 3 A, T_J = 25 ℃		28.4		mΩ
	2.7 ≤ V_{IN} ≤ 23 V, –40 ℃ ≤ T_J ≤ 125 ℃			44.85	mΩ
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)					
$V_{UVLO(R)}$	EN/UVLO rising threshold	1.183	1.2	1.223	V
$V_{UVLO(F)}$	EN/UVLO falling threshold	1.076	1.09	1.116	V
$V_{SD(F)}$	EN/UVLO falling threshold for lowest shutdown current	0.45	0.74		V
I_{ENLKG}	EN/UVLO leakage current	–0.1		0.1	µA
OVERVOLTAGE LOCKOUT (OVLO)					
$V_{OV(R)}$	OVLO rising threshold	1.183	1.2	1.223	V
$V_{OV(F)}$	OVLO falling threshold	1.076	1.09	1.116	V
I_{OVLKG}	OVLO pin leakage current, 0.5 V < V_{OVLO} < 1.5 V	–0.1		0.1	µA
$I_{OUTLKG(OVLO)}$	OUT leakage current (OVLO condition), V_{OUT} > V_{IN}		317		µA
FIXED FAST-TRIP (OUT)					
I_{FT}	Fixed fast-trip current threshold		21.9		A
OUTPUT LOAD CURRENT MONITOR (IMON)					
G_{IMON}	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 0.5 A to 1 A	144	181	216	µA/A
	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 1 A to 5.5 A	153	181	207	µA/A
REVERSE CURRENT BLOCKING (IN - OUT)					
V_{FWD}	(V_{IN} - V_{OUT}) forward regulation voltage, I_{OUT} = 10 mA	4.8	16.4	28.4	mV
V_{REVTH}	(V_{OUT} - V_{IN}) threshold for fast BFET turn off (enter reverse current blocking)	22.7	29.3	36.5	mV
V_{FWDTH}	(V_{IN} - V_{OUT}) threshold for fast BFET turn on (exit reverse current blocking)	85.9	105.8	125	mV
$I_{REVLKG(OFF)}$	Reverse leakage current (unpowered condition), V_{OUT} = 12 V, V_{IN} = 0 V		4.8		µA
I_{REVLKG}	Reverse leakage current, (V_{OUT} - V_{IN}) = 21.5 V		10.10	15.86	µA
$I_{OUTLKG(RCB)}$	OUT leakage current during RCB state while ON, (V_{OUT} - V_{IN}) = 1 V		247.6	322	µA

6.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V, dVdT = Open, R_{IMON} = 549 Ω, PGTH = Open, PG = Open, OUT = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
POWER GOOD INDICATION (PG)					
V_{PGD}	PG pin low voltage while de-asserted, V_{IN} < $V_{UVP(F)}$, V_{EN} < V_{SD}, I_{PG} = 26 µA		0.67	0.9	V
	PG pin low voltage while de-asserted, V_{IN} < $V_{UVP(F)}$, V_{EN} < V_{SD}, I_{PG} = 242 µA		0.78	1	V
	PG pin low voltage while de-asserted, V_{IN} > $V_{UVP(R)}$			0.6	V
I_{PGLKG}	PG pin leakage current while asserted		0.5	2	µA
POWERGOOD THRESHOLD (PGTH)					
$V_{PGTH(R)}$	PGTH rising threshold	1.183	1.2	1.223	V
$V_{PGTH(F)}$	PGTH falling threshold	1.076	1.09	1.116	V
$I_{PGTHLKG}$	PGTH leakage current	–1		1	µA
OVERTEMPERATURE PROTECTION (OTP)					
TSD	Thermal shutdown rising threshold, T_J ↑		154		°C
TSD_{HYS}	Thermal shutdown hysteresis, T_J ↓		10		°C
DVDT					
I_{dVdt}	dVdt pin charging current	1.15	2.34	3.66	µA

6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVLO}	Overvoltage lock-out response time	V_{OVLO} > $V_{OV(R)}$ to V_{OUT} ↓		1.1		µs
t_{FT}	Fixed fast-trip response time	I_{OUT} > I_{FT} to I_{OUT} ↓		500		ns
t_{SWRCB}	Reverse Current Blocking recovery time	(V_{IN} - V_{OUT}) > V_{FWDTH} to V_{OUT} ↑		50		µs
t_{RCB}	Reverse Current Blocking fast comparator response time	(V_{OUT} - V_{IN}) > 1.3 x V_{REVTH} to BFET OFF		1		µs
t_{PGA}	PG Assertion de-glitch			12		µs
t_{PGD}	PG De-assertion de-glitch			12		µs

6.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled.Typical Values are taken at T_J = 25°C unless specifically noted otherwise. R_L = 100 Ω, C_{OUT} = 1 µF

PARAMETER		V_{IN}	C_{dVdt} = Open	C_{dVdt} = 1800 pF	C_{dVdt} = 3300 pF	UNIT
SR_{ON}	Output Rising slew rate	2.7 V	12.14	0.87	0.5	V/ms
		12 V	28.1	1.09	0.61	
		23 V	44.78	1.25	0.71	
$t_{D,ON}$	Turn on delay	2.7 V	0.09	0.6	0.97	ms
		12 V	0.1	1.32	2.35	
		23 V	0.11	1.99	3.69	
t_R	Rise time	2.7 V	0.17	2.51	4.33	ms
		12 V	0.35	8.1	15.37	
		23 V	0.40	14.4	25.89	
t_{ON}	Turn on time	2.7 V	0.27	3.11	5.31	ms
		12 V	0.45	10.08	17.72	
		23 V	0.50	16.41	29.57	
$t_{D,OFF}$	Turn off delay	2.7 V	64.44	64.44	64.44	µs
		12 V	25.32	25.32	25.32	
		23 V	23.02	23.02	23.02	

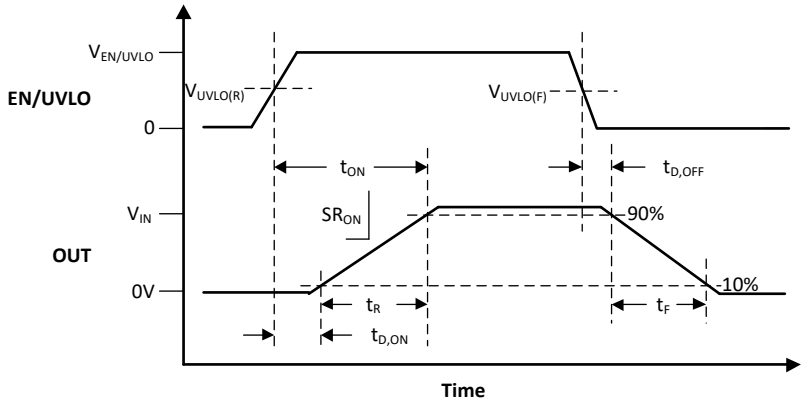


図 6-1. LM73100 Switching Times

6.8 Typical Characteristics

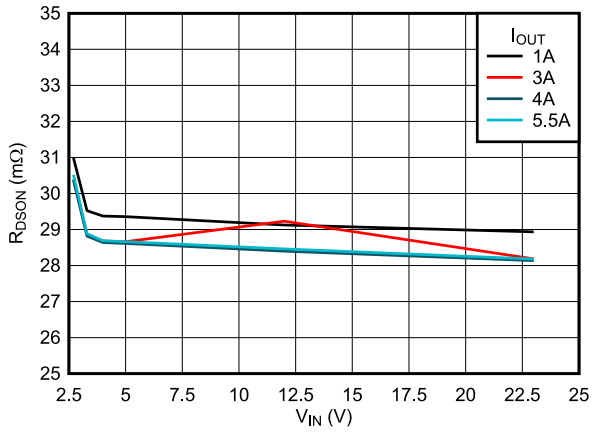


図 6-2. ON-Resistance vs Supply Voltage

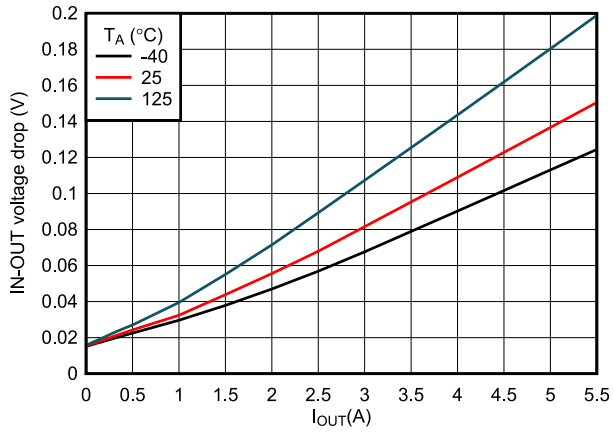


図 6-3. Forward Voltage Drop vs Load Current

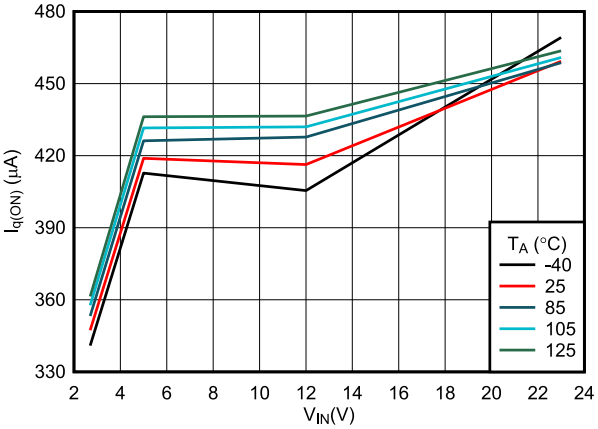


図 6-4. IN Quiescent Current vs Supply Voltage

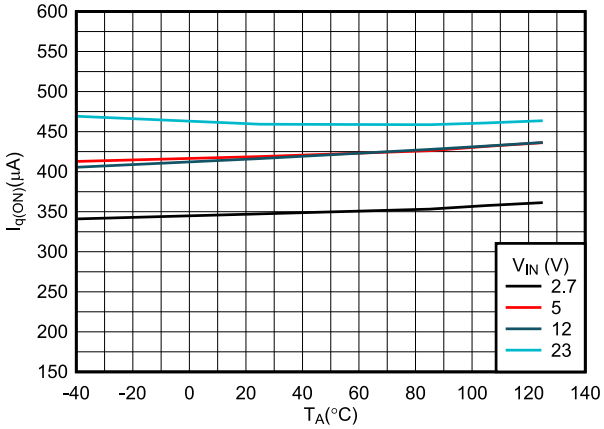


図 6-5. IN Quiescent Current vs Temperature

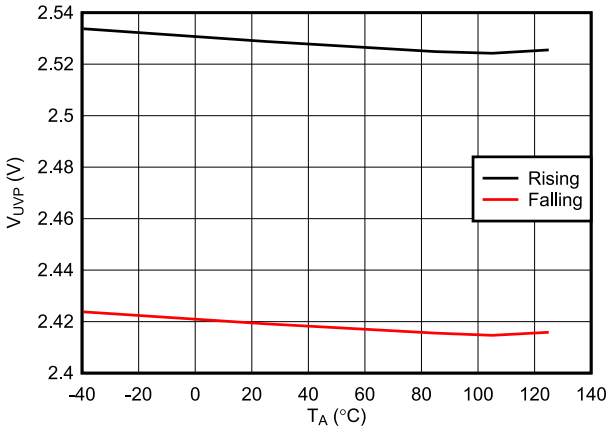


図 6-6. IN Undervoltage Threshold vs Temperature

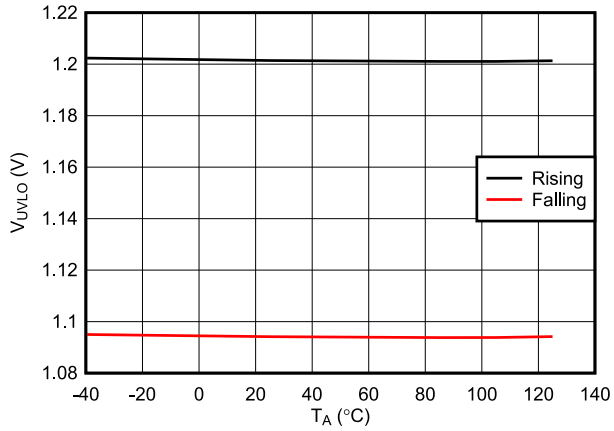


図 6-7. EN/UVLO Threshold vs Temperature

6.8 Typical Characteristics (continued)

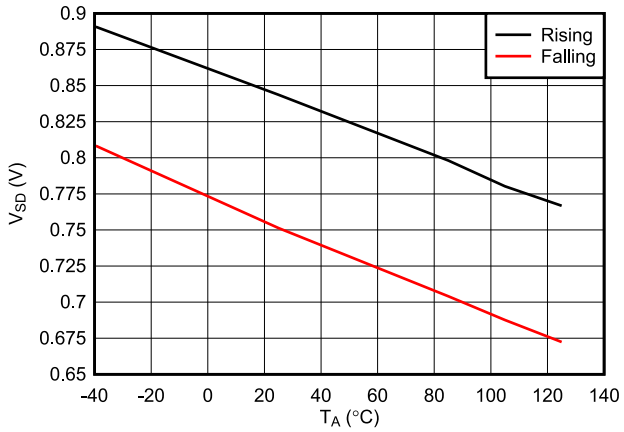


図 6-8. EN/UVLO Shutdown Threshold vs Temperature

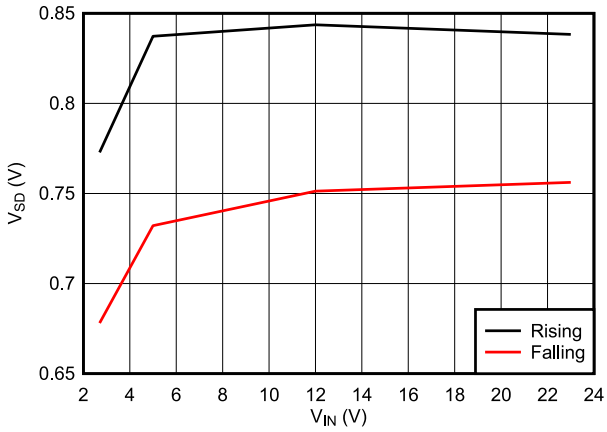


図 6-9. EN/UVLO Shutdown Threshold vs Supply Voltage

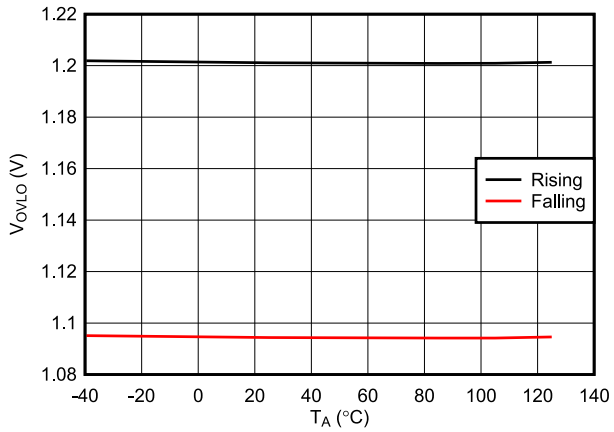


図 6-10. OVLO Threshold vs Temperature

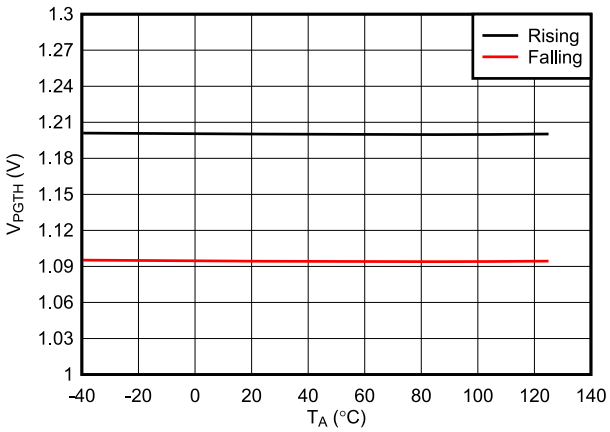


図 6-11. PGTH Threshold vs Temperature

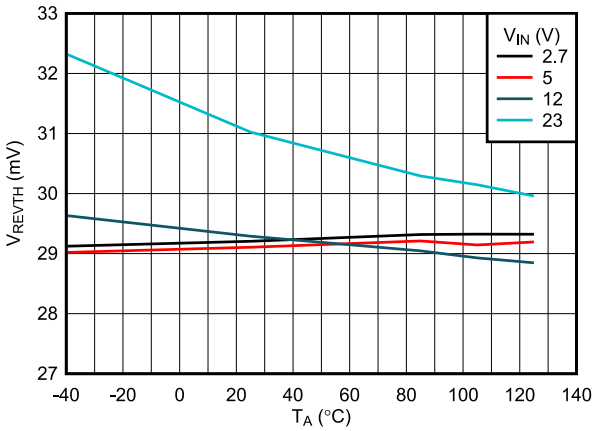


図 6-12. Reverse Comparator Threshold vs Temperature

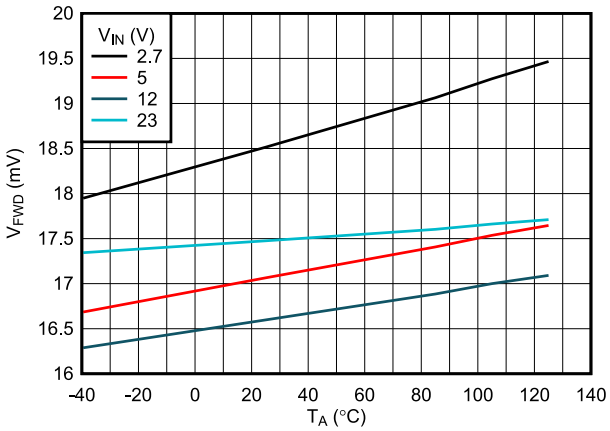


図 6-13. Forward Regulation Voltage vs Temperature

6.8 Typical Characteristics (continued)

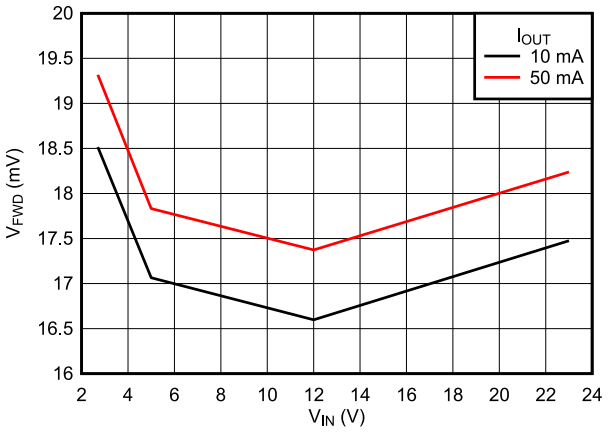


図 6-14. Forward Regulation Voltage vs Supply Voltage

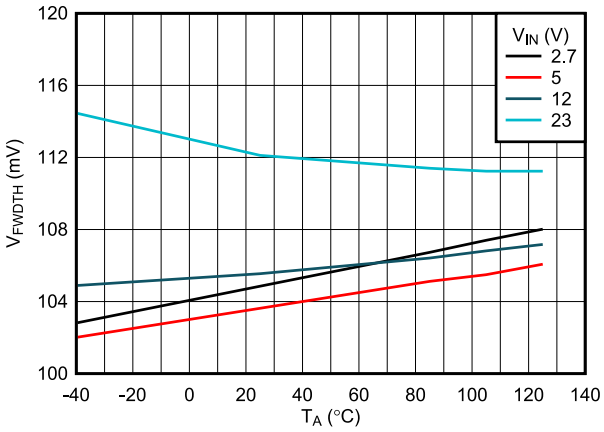


図 6-15. Forward Comparator Threshold vs Temperature

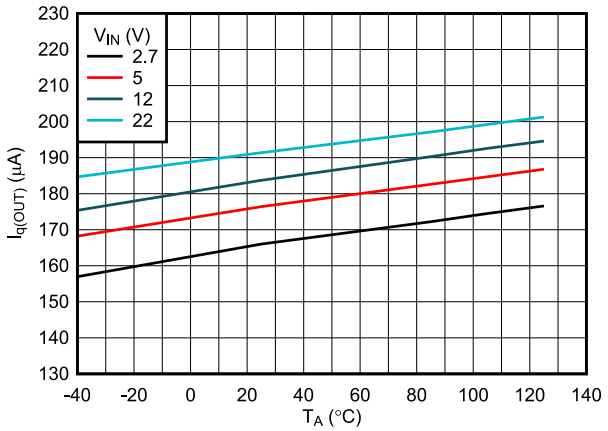


図 6-16. OUT Leakage Current During ON-State Reverse Current Blocking

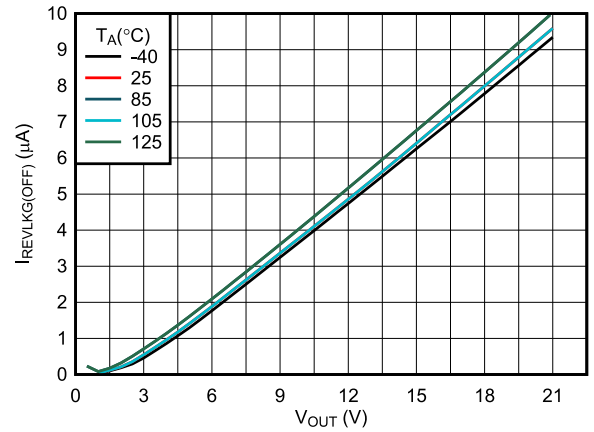


図 6-17. Reverse Leakage Current During OFF-State

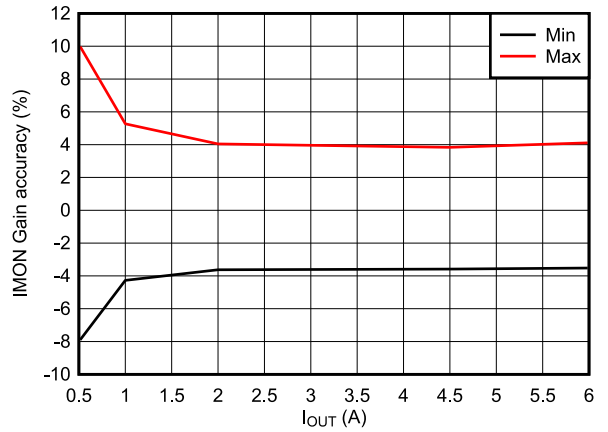


図 6-18. Analog Current Monitor Gain Accuracy

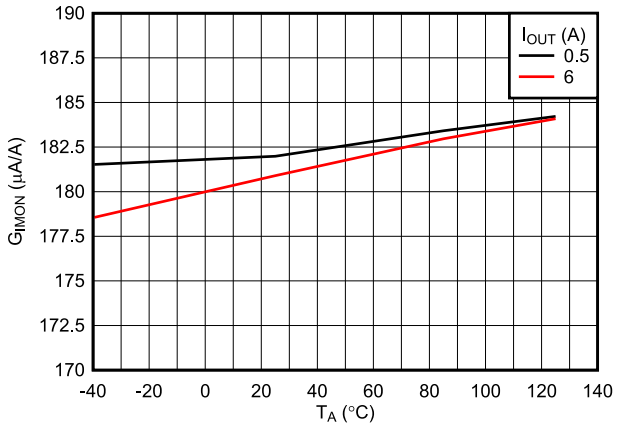


図 6-19. Analog Current Monitor gain vs Temperature

6.8 Typical Characteristics (continued)

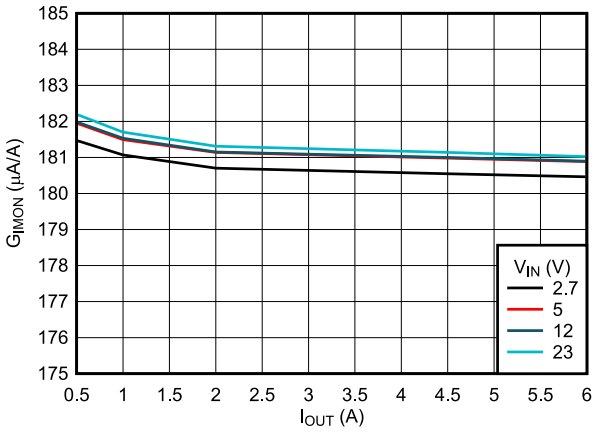


図 6-20. Analog Current Monitor Gain vs Load Current

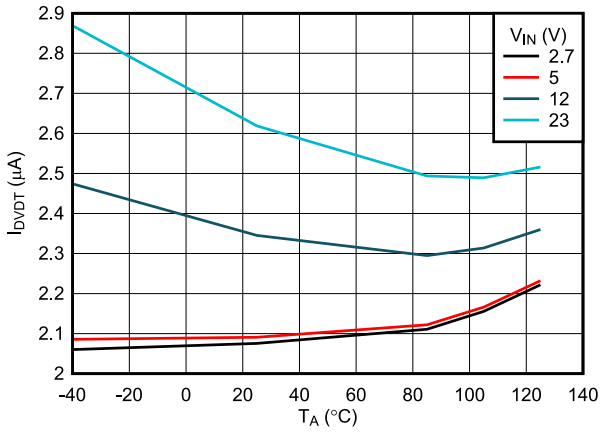


図 6-21. DVDT Charging Current vs Temperature

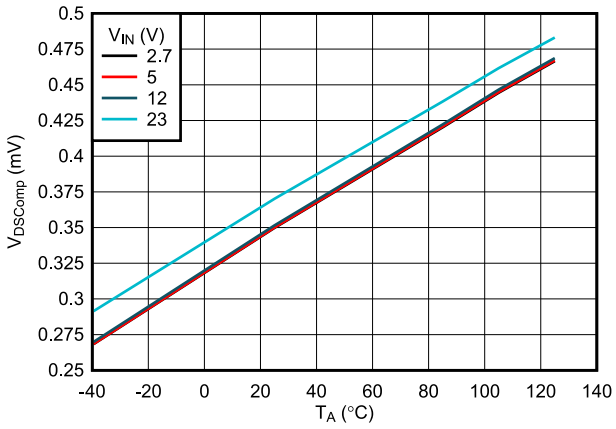


図 6-22. Steady State Fast-Trip Comparator Threshold vs Temperature

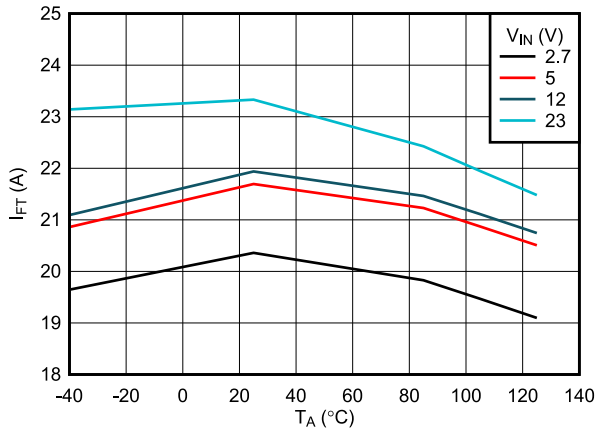


図 6-23. Steady State Fast-Trip Current Threshold vs Temperature

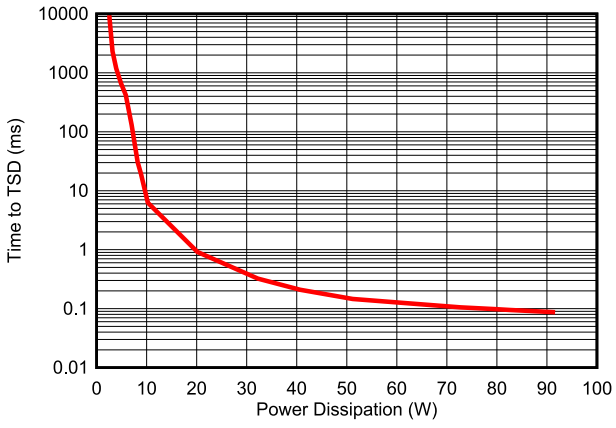


図 6-24. Time to Thermal Shut-Down During Inrush State

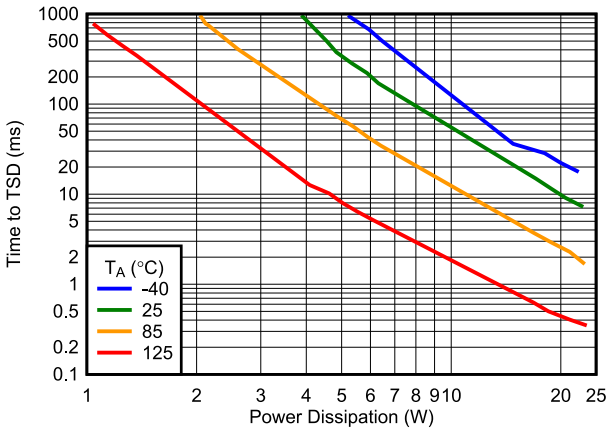
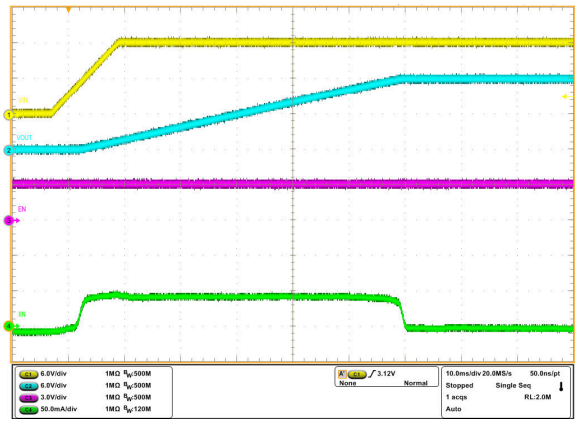


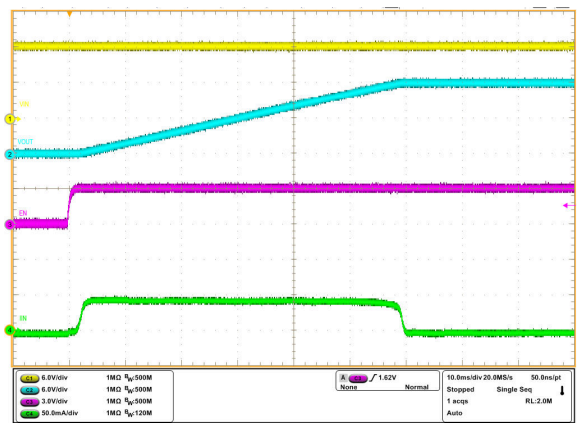
図 6-25. Time to thermal Shut-Down During Steady State

6.8 Typical Characteristics (continued)



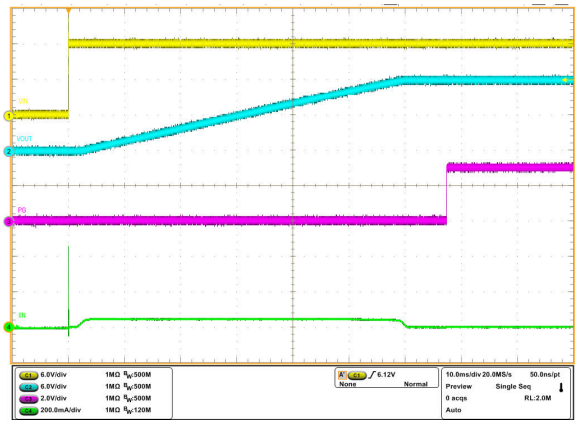
$V_{EN/UVLO}$ = 3 V, C_{OUT} = 220 µF, C_{dVdt} = 10 nF, V_{IN} ramped up to 12 V

図 6-26. Start Up with IN Supply



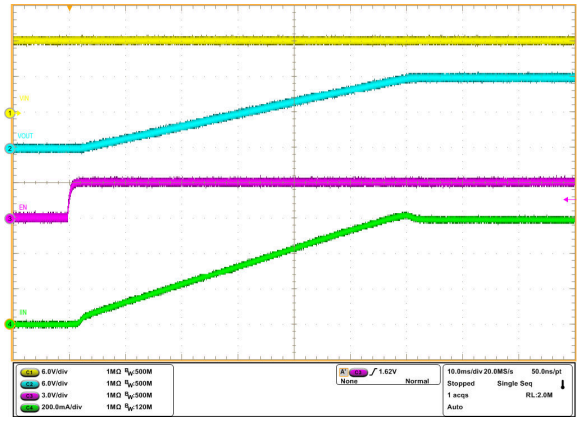
V_{IN} = 12 V, C_{OUT} = 220 µF, C_{dVdt} = 10 nF, $V_{EN/UVLO}$ stepped up to 3 V

図 6-27. Start Up with EN



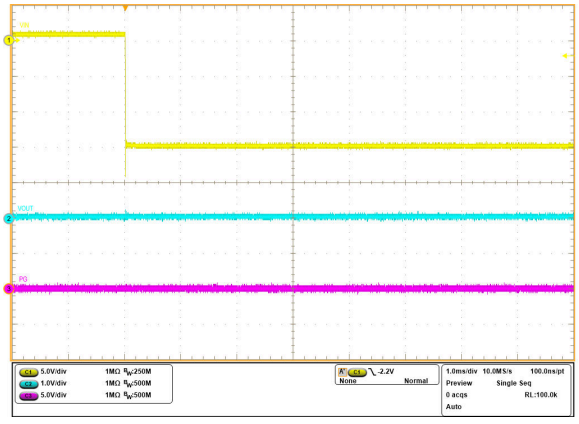
C_{OUT} = 220 µF, C_{dVdt} = 10 nF, EN/UVLO connected to IN through resistor ladder, 12 V hot-plugged to IN

図 6-28. Input Hot-Plug



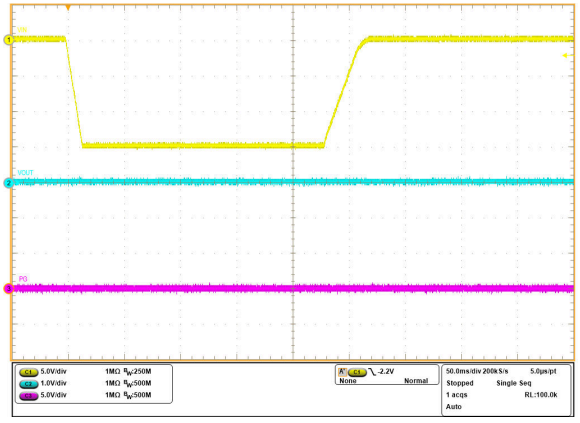
V_{IN} = 12 V, R_{OUT} = 20 Ω, C_{OUT} = 220 µF, C_{dVdt} = 10 nF, $V_{EN/UVLO}$ stepped up to 3 V

図 6-29. Inrush Current with RC Load



C_{OUT} = 220 µF, PG pulled up to 3 V, -15 V hot-plugged to IN

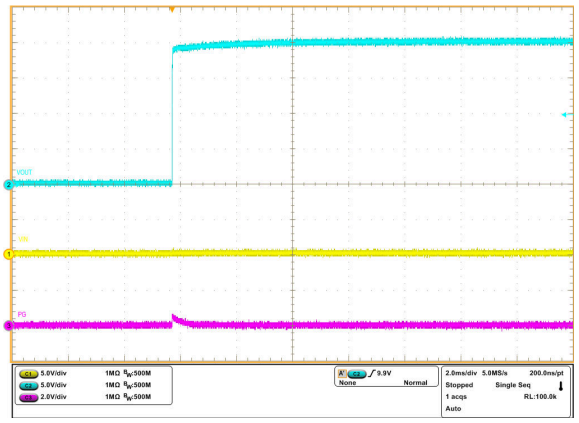
図 6-30. Input Reverse Polarity Protection - Fast Ramp



C_{OUT} = 220 µF, PG pulled up to 3 V, V_{IN} ramped down from 0 V to -15 V and then ramped up to 0 V

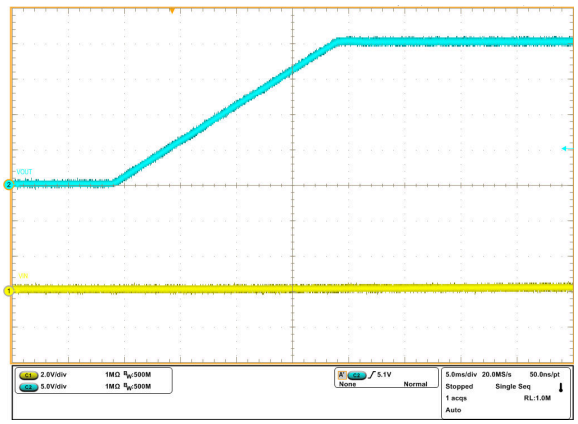
図 6-31. Input Reverse Polarity Protection - Slow Ramp

6.8 Typical Characteristics (continued)



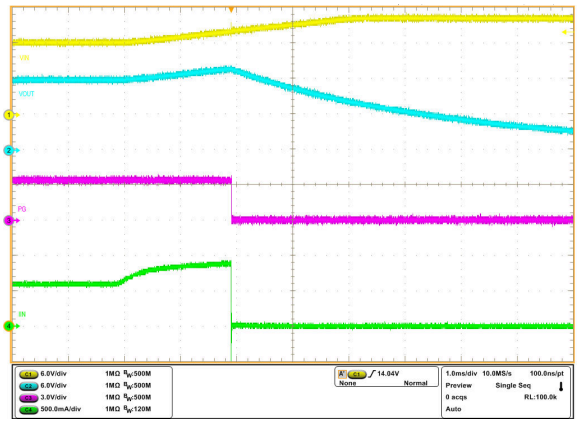
IN= Open, C_{OUT} = 220 µF, PG pulled up to 3 V, 20 V hot-plugged to OUT

図 6-32. Reverse Current Blocking Response in OFF State



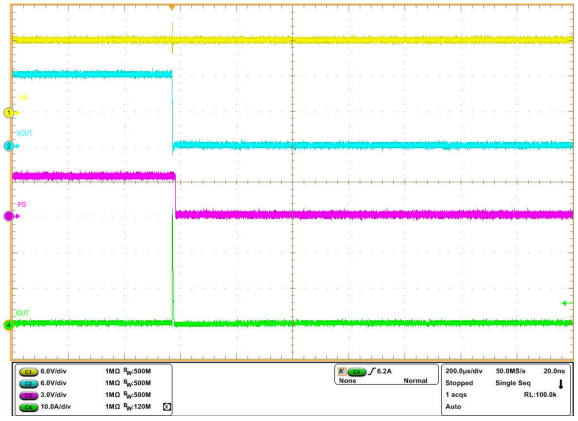
IN= Open, C_{OUT} = 220 µF, PG pulled up to 3 V, V_{OUT} ramped up from 0 V to 20 V

図 6-33. Reverse Current Blocking Response in OFF State



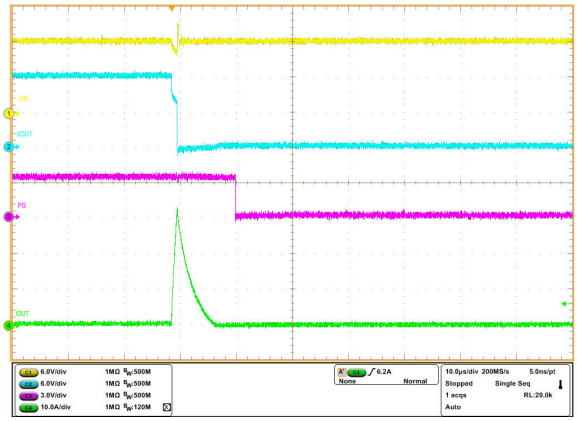
C_{OUT} = 220 µF, R_{OUT} = 20 Ω, OVLO threshold = 13.2 V, V_{IN} ramped up from 12 V to 16 V

図 6-34. Input Overvoltage Protection



V_{IN} = 12 V, C_{OUT} = Open, OUT stepped from Open → Short-circuit to GND

図 6-35. Fast-Trip Response During Steady State



V_{IN} = 12 V, C_{OUT} = Open, OUT stepped from Open → Short-circuit to GND

図 6-36. Fast-Trip Response During Steady State - Zoomed In

7 Detailed Description

7.1 Overview

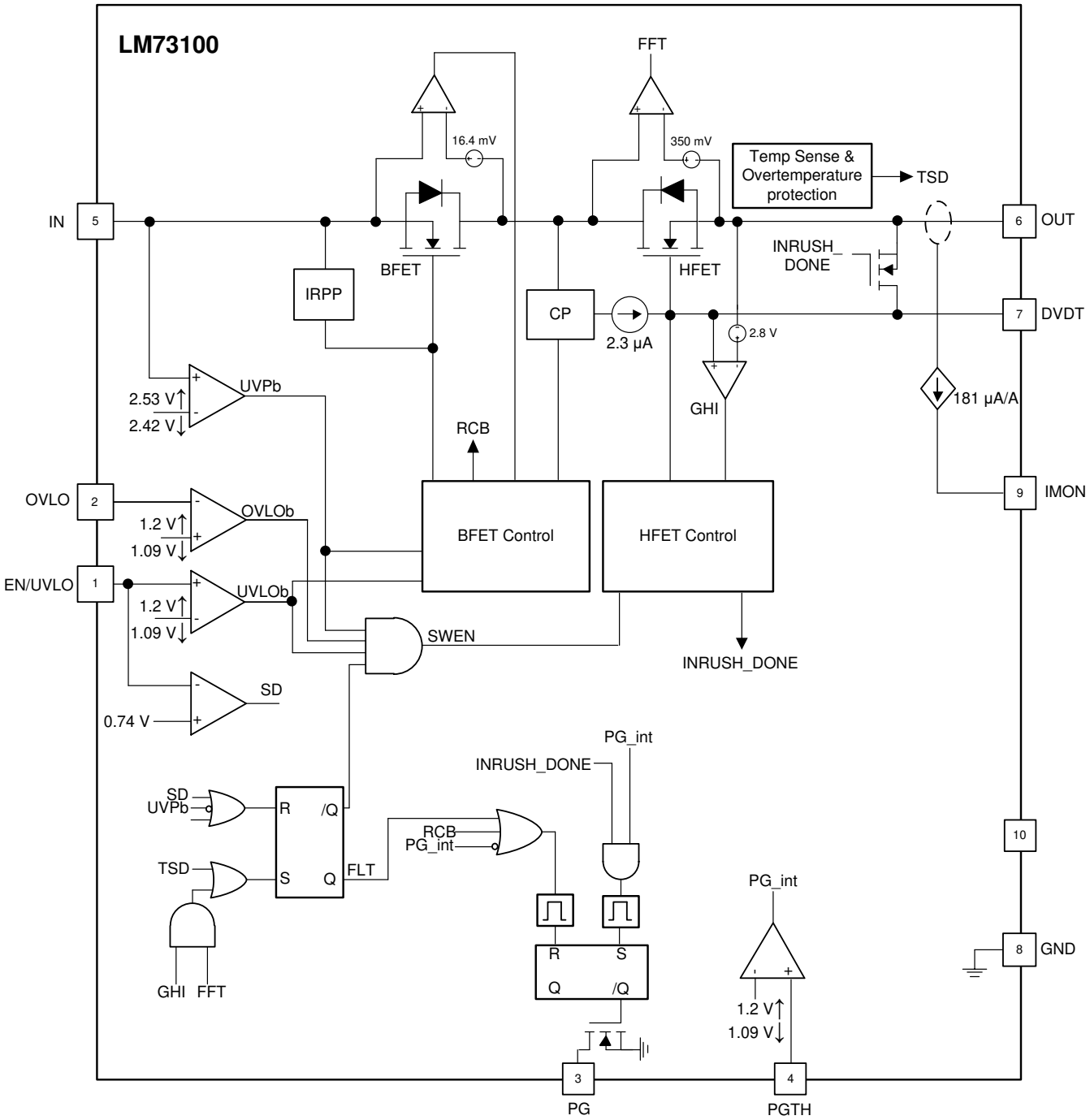
The LM73100 is an integrated ideal diode that is used to ensure safe power delivery in a system. The device starts its operation by monitoring the IN bus. When the input supply voltage (V_{IN}) exceeds the undervoltage protection threshold (V_{UVP}), the device samples the EN/UVLO pin. A high level (> $V_{UVLO(R)}$) on this pin enables the internal power path (BFET+HFET) to start conducting and allow current to flow from IN to OUT. When EN/UVLO pin is held low (< $V_{UVLO(F)}$), the internal power path is turned off. In case of reverse voltages appearing at the input, the power path remains OFF thereby protecting the output load.

After a successful start-up sequence, the device now actively monitors its load current and input voltage, and controls the internal HFET to ensure that the fast-trip threshold (I_{FT}) is not exceeded and overvoltage spikes are cut-off once they cross the user adjustable overvoltage lockout threshold (V_{OVLO}). This helps to keep the system safe from harmful levels of voltage and current.

The device has integrated reverse current blocking FET (BFET) which operates like an ideal diode. The BFET is linearly regulated to maintain a small constant forward drop (V_{FWD}) in forward conduction mode and turned off completely to block reverse current from OUT to IN if output voltage exceeds the input voltage.

The device also has a built-in thermal sensor based shutdown mechanism to protect itself in case the device temperature (T_J) exceeds the recommended operating conditions.

7.2 Functional Block Diagram



7.3 Feature Description

The LM73100 integrated ideal diode is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults.

7.3.1 Input Reverse Polarity Protection

The LM73100 device is internally protected against transient and steady state negative voltages applied at the input supply pin. The device blocks the negative voltage from appearing at the output, thereby protecting the load circuits. There's no reverse current flowing from output to the input in this condition. The maximum negative voltage the device can handle at the input is limited to -15 V or V_{OUT} – 21 V, whichever is higher. It's also recommended that all signal pins (e.g. EN/UVLO, OVLO, PGTH) which are derived from input supply should have a sufficiently large pull-up resistor to limit the current flowing out of these pins during reverse polarity conditions. Please refer to *Absolute Maximum Ratings* table for more details.

7.3.2 Undervoltage Protection (UVLO & UVP)

The LM73100 implements undervoltage protection on IN in case the applied voltage becomes too low for the system or device to properly operate. The undervoltage protection has a default lockout threshold of V_{UVP} which is fixed internally. Apart from that, the UVLO comparator on the EN/UVLO pin allows the undervoltage Protection threshold to be externally adjusted to a user defined value. The 図 7-1 and 式 1 below show how a resistor divider can be used to set the UVLO set point for a given voltage supply.

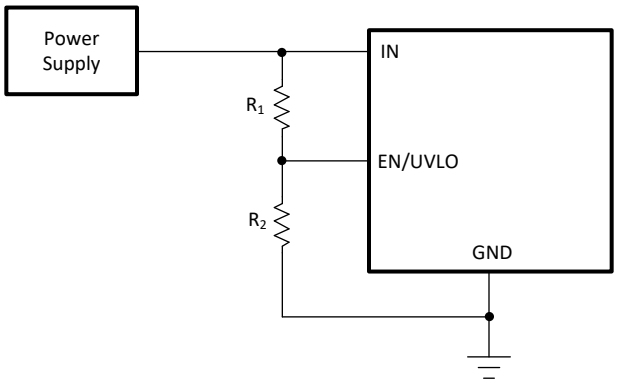


図 7-1. Adjustable Undervoltage Protection

$$V_{IN(UV)} = \frac{V_{UVLO} \times (R1 + R2)}{R2} \quad (1)$$

7.3.3 Overvoltage Lockout (OVLO)

The LM73100 allows the user to implement overvoltage lockout to protect the load from input overvoltage conditions. The OVLO comparator on the OVLO pin allows the overvoltage protection threshold to be adjusted to a user defined value. Once the voltage at the OVLO pin crosses the OVLO rising threshold $V_{OV(R)}$, the device turns off the power to the output. Thereafter, the devices wait for the voltage at the OVLO pin to fall below the OVLO falling threshold $V_{OV(F)}$ before the output power is turned ON again. The rising and falling thresholds are slightly different to provide hysterisis. The 図 7-2 and 式 2 below show how a resistor divider can be used to set the OVLO set point for a given input supply voltage.

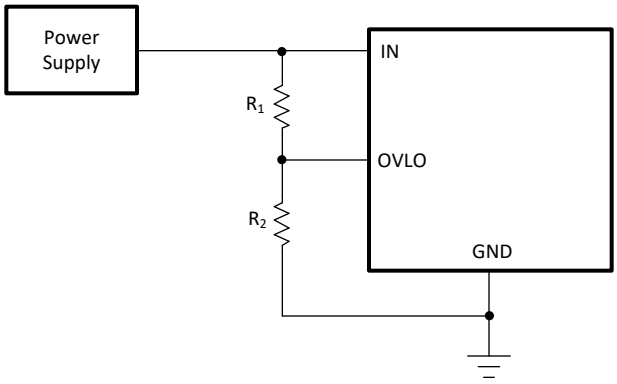


図 7-2. Adjustable Overvoltage Protection

$$V_{IN(OV)} = \frac{V_{OV} \times (R1 + R2)}{R2} \quad (2)$$

While recovering from an overvoltage event, the LM73100 starts up with inrush control (dVdt).

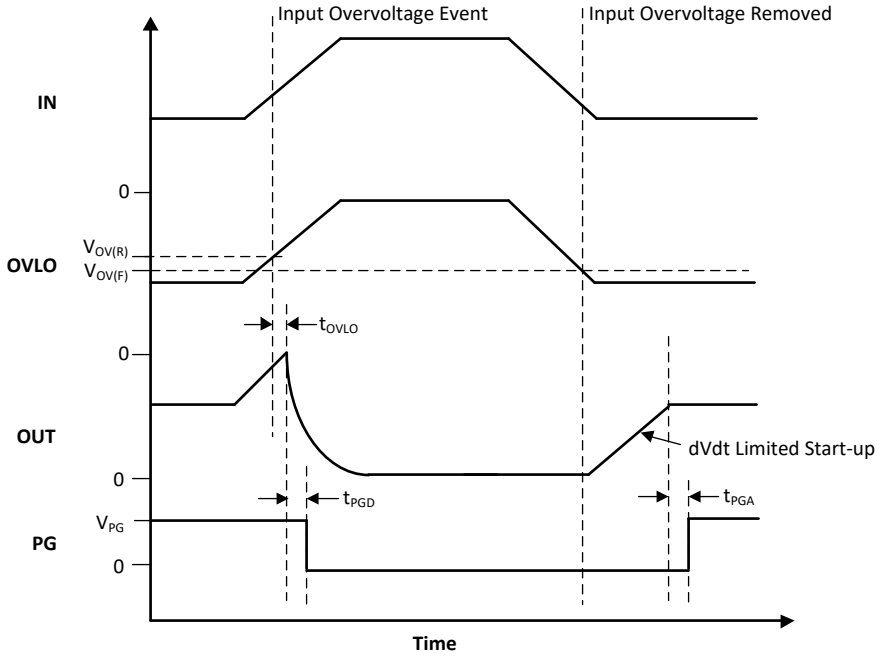


図 7-3. LM73100 Overvoltage Lockout and Recovery

7.3.4 Inrush Current control and Fast-trip

LM73100 incorporates 2 mechanisms to handle overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control
2. Fixed threshold (I_{FT}) for fast-trip response to transient overcurrent events during steady-state

7.3.4.1 Slew Rate (dVdt) and Inrush Current Control

During hot-plug events or while trying to charge a large output capacitance at start-up, there can be a large inrush current. If the inrush current is not managed properly, it can damage the input connectors and/or cause the system power supply to droop leading to unexpected restarts elsewhere in the system. The inrush current during turn on is directly proportional to the load capacitance and rising slew rate. 式 3 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{OUT}):

$$\mathrm{SR\,(V/ms)} = \frac{\mathrm{I_{INRUSH}\,(mA)}}{\mathrm{C_{OUT}\,(\mu F)}} \tag{3}$$

A capacitor can be connected to the dVdt pin to control the rising slew rate and lower the inrush current during turn on. The required C_{dVdt} capacitance to produce a given slew rate can be calculated using the following equation:

$$\mathrm{C_{dVdt}\,(pF)} = \frac{2000}{\mathrm{SR\,(V/ms)}} \tag{4}$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

注

For C_{dVdt} > 10 nF, it's recommended to add a 100-Ω resistor in series with the capacitor on the dVdt pin.

7.3.4.2 Fast-Trip During Steady State

During certain system faults, the current through the device can increase very rapidly. In such events, the device provides fast-trip response with a fixed threshold (I_{FT}) during steady state. Once the current exceeds I_{FT}, the HFET is turned off completely within t_{FT}. Thereafter, the device remains latched-off until it's power cycled or re-enabled by toggling the EN/UVLO pin.

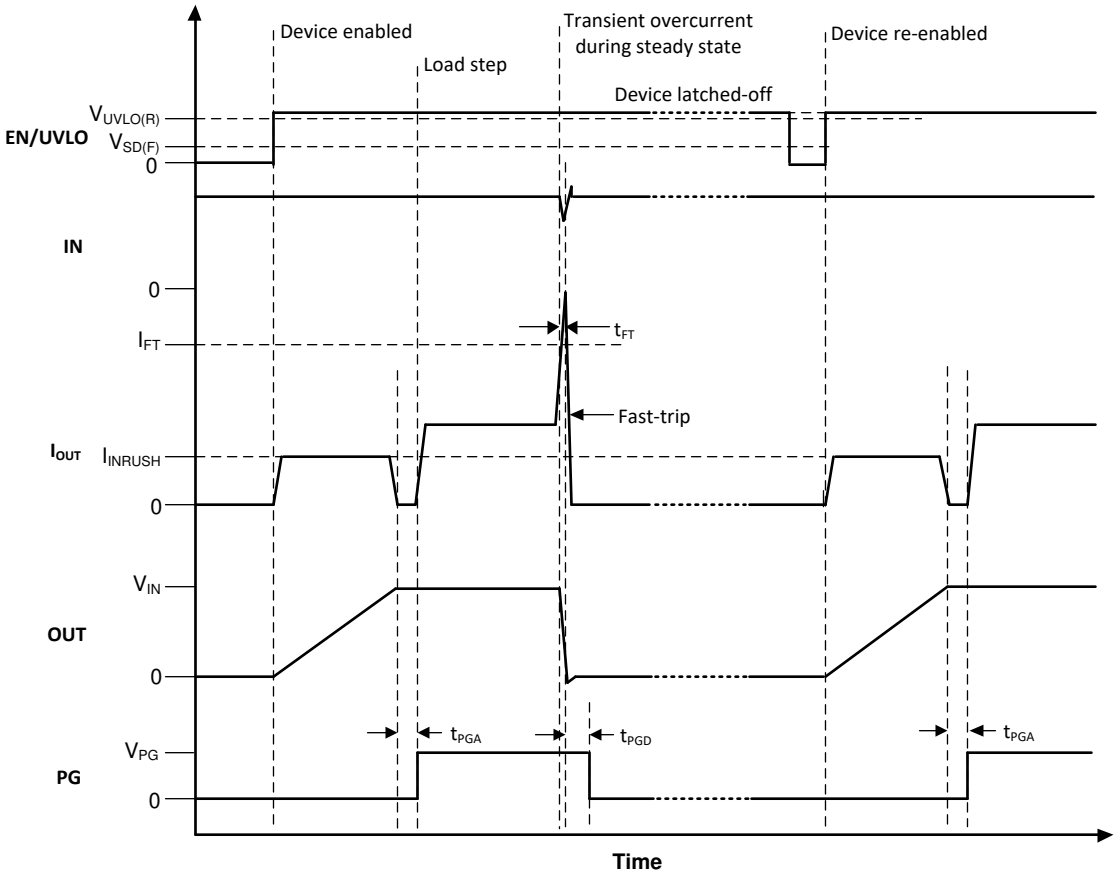


図 7-4. LM73100 Fast-Trip Response

注

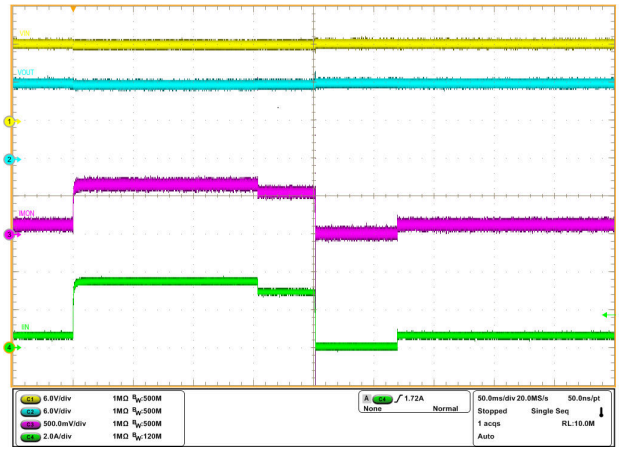
The LM73100 fast-trip response is active only during steady state and offers one level of fast response to severe overcurrents of transient nature. However, for systems which may experience persistent faults such as short-circuits or overloads, it's recommended to use an additional level of overcurrent protection in series for safety.

7.3.5 Analog Load Current Monitor Output

The device allows the system to accurately monitor the output load current by providing an analog current sense output on the IMON pin which is proportional to the current through the FET. The user can sense the voltage (V_{IMON}) across the R_{IMON} to get a measure of the output load current.

$$I_{OUT}\,(A) = \frac{V_{IMON}\,(V) \times 10^{-6}}{R_{IMON}\,(\Omega) \times G_{IMON}\,(\mu A/A)} \quad (5)$$

The waveform below shows the IMON signal response to a dynamically varying load profile at the output.



V_{IN} = 12 V, C_{OUT} = 22 µF, R_{IMON} = 1.15 kΩ, I_{OUT} varied dynamically between 0 A and 3.5 A

図 7-5. Analog Load Current Monitor Output Response

注

1. It's recommended to choose R_{IMON} such that V_{IMON} ≤ 1.5 V at the maximum DC load current.
2. It's also recommended to add a zener diode on the IMON pin to clamp the voltage below 1.8 V during high current transients.
3. Connect IMON pin to GND if not used. Do not leave the pin floating.

7.3.6 Reverse Current Protection

The LM73100 functions like an ideal diode and blocks reverse current flow from OUT to IN under all conditions. The device has integrated back-to-back MOSFETs connected in a common drain configuration. The voltage drop between the IN and OUT pins is constantly monitored and the gate drive of the blocking FET (BFET) is adjusted as needed to regulate the forward voltage drop at V_{FWD}. This closed loop regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures there's no DC reverse current flow.

The device also uses a conventional comparator (V_{REVTH}) based reverse blocking mechanism to provide fast response to transient reverse currents.Once the device enters reverse current blocking condition, it waits for the (V_{IN} - V_{OUT}) forward drop to exceed the V_{FWDTH} before it performs a fast recovery to reach full forward conduction state. This provides sufficient hysterisis to prevent supply noise or ripple from affecting the reverse current blocking response. The recovery from reverse current blocking is very fast (t_{SWRCB}). This ensures minimum supply droop which is helpful in applications such as power MUX/ORing.

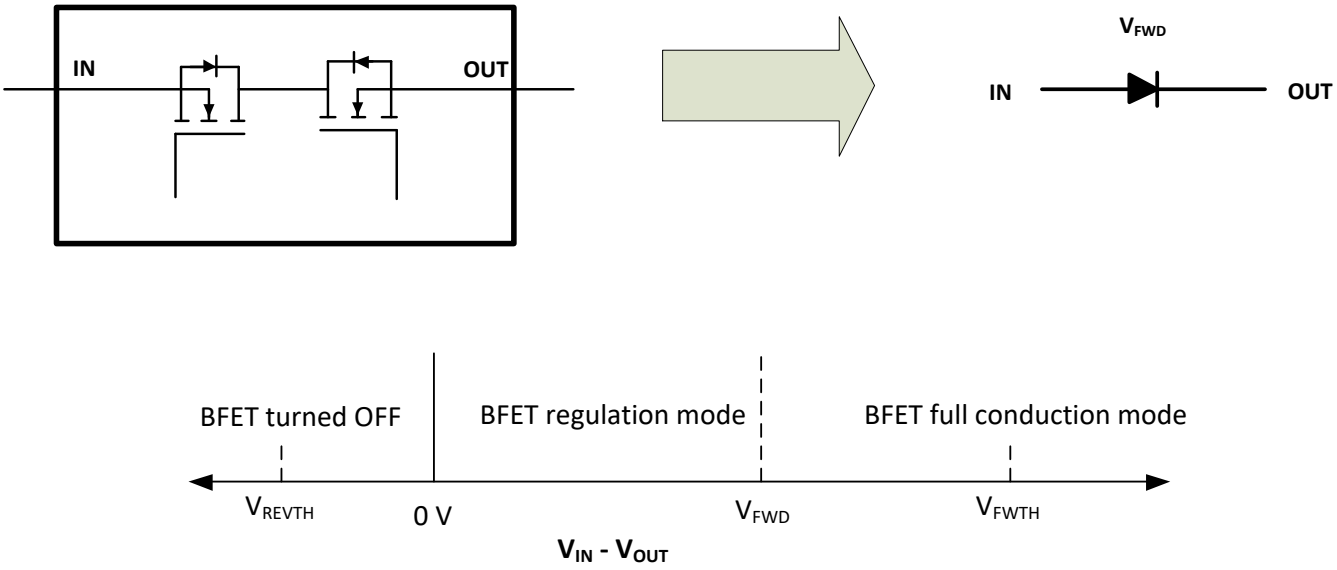


図 7-6. Reverse Current Blocking Response

The waveforms below illustrate the reverse current blocking performance in various scenarios.

During fast voltage step at output (e.g. hot-plug), the fast comparator based reverse blocking mechanism ensures minimum jump/glitch on the input rail.

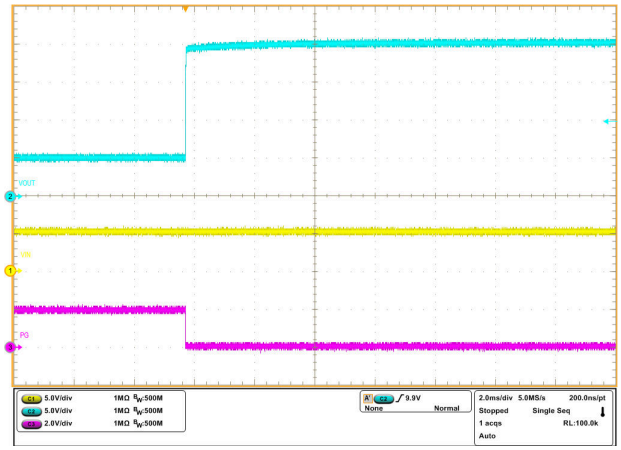


図 7-7. Reverse Current Blocking Performance During Fast Voltage Step at Output

During slow voltage ramp at output, the linear ORing based reverse blocking mechanism ensures there's no DC current flow from OUT to IN, thereby avoiding input rail from getting slowly charged up to output voltage.

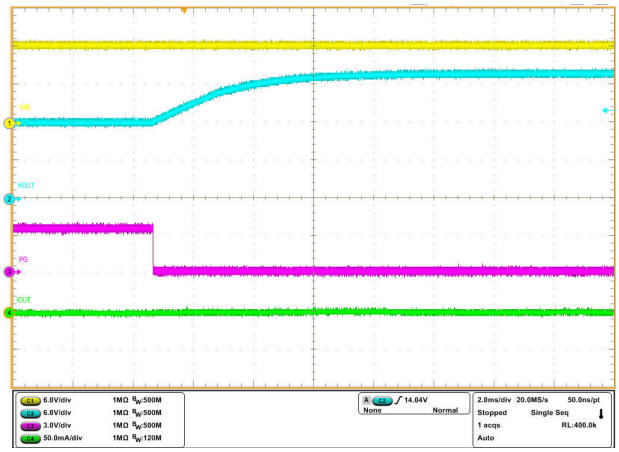


図 7-8. Reverse Current Blocking Performance During Slow Voltage Ramp at Output

When the input supply droops or gets disconnected while the output storage element (capacitor bank or super capacitor) is charged to the full voltage, the linear ORing scheme minimizes the self-discharge from OUT to IN. This ensures maximum hold-up time for the output storage element in critical power back-up applications.

It also prevents incorrect supply presence indication in applications which sense the input voltage to detect if the supply is connected.

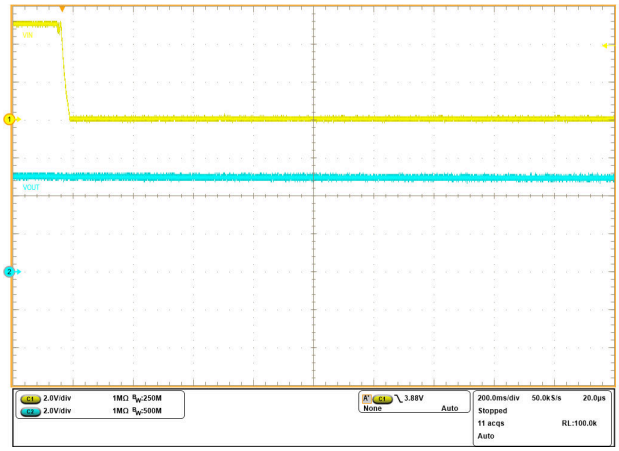


図 7-9. Reverse Current Blocking Performance During Input Supply Failure

7.3.7 Overtemperature Protection (OTP)

The LM73100 monitors the internal die temperature (T_J) at all times and shuts down the part as soon as the temperature exceeds a safe operating level (TSD) thereby protecting the device from damage. The device will not turn back on until the junction cools down sufficiently, that is the die temperature falls below (TSD - TSD_{HYS}).

When the device detects thermal overload, it will shut down and remain latched-off until the device is power cycled or re-enabled by toggling the EN/UVLO pin.

表 7-1. Thermal Shutdown

Enter TSD	Exit TSD
$T_J \geq$ TSD	$T_J <$ TSD - TSD_{HYS} V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ OR EN/UVLO toggled below $V_{SD(F)}$

7.3.8 Fault Response

The following table summarizes the LM73100 response to various fault conditions.

表 7-2. Fault Summary

Event	Protection Response	Fault Latched Internally
Overtemperature	Shutdown	Y
Undervoltage (UVP or UVLO)	Shutdown	N
Input Reverse Polarity	Shutdown	N
Overvoltage	Shutdown	N
Reverse Current	Reverse Current Blocking	N
Transient overcurrent during steady state	Shutdown	Y

Faults which are not latched internally are automatically cleared once the trigger condition goes away and thereafter the device recovers without any external intervention. Faults which are latched internally can be cleared either by power cycling the part (pulling V_{IN} to 0 V and then above $V_{UVP(R)}$) or by pulling the EN/UVLO pin voltage below $V_{SD(F)}$.

After a latched fault, pulling the EN/UVLO just below the UVLO threshold ($V_{UVLO(F)}$) has no impact on the device.

7.3.9 Power Good Indication (PG)

The LM73100 provides an active high digital output (PG) which serves as a power good indication signal and is asserted high depending on the voltage at the PGTH pin along with the device state information. The PG is an open-drain pin and needs to be pulled up to an external supply.

After power up, PG is pulled low initially. The device initiates a inrush sequence in which the HFET is turned on in a controlled manner. When the HFET gate voltage reaches the full overdrive indicating that the inrush sequence is complete and the voltage at PGTH is above $V_{PGTH(R)}$, the PG is asserted after a de-glitch time (t_{PGA}).

PG is de-asserted if at any time during normal operation, the voltage at PGTH falls below $V_{PGTH(F)}$, or the device detects a fault. The PG de-assertion de-glitch time is t_{PGD}.

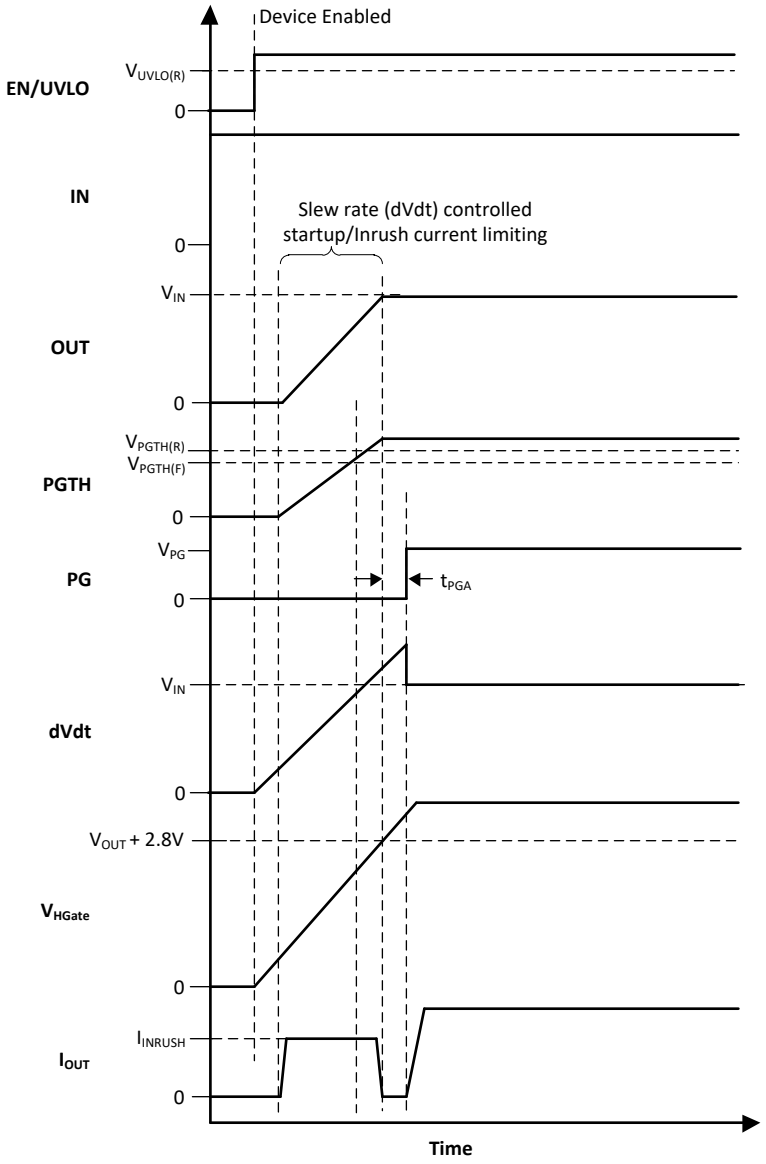


図 7-10. LM73100 PG Timing Diagram

表 7-3. LM73100 PG Indication Summary

Event	Protection Response	PG Pin	PG Delay
Undervoltage (UVP or UVLO)	Shutdown	L	
Input Reverse Polarity	Shutdown	L	
Overvoltage (OVLO)	Shutdown	L	t_{PGD}
Steady State	N/A	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Transient overcurrent during steady state	Fast-trip	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Reverse current ((V_{OUT} - V_{IN}) > V_{REVTH})	Reverse current blocking	L	t_{PGD}
Overtemperature	Shutdown	L	t_{PGD}

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pull-down in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pull-up supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

7.4 Device Functional Modes

The device has one mode of operation that applies when operated within the Recommended Operating Conditions.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The LM73100 is an integrated 5.5-A ideal diode that is typically used for power rail monitoring and protection applications . It operates from 2.7 V to 23 V with adjustable overvoltage and undervoltage protection. It provides ability to control inrush current and protection against input reverse polarity as well as reverse current conditions. It also has integrated analog load current monitoring and digital power good indication with adjustable threshold. It can be used in a variety of systems such as set-top boxes, smart speakers, handheld power tools/chargers, PC/notebooks and Retail ePOS (Point-of-sale) terminals.

The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool LM73100 Design Calculator is available in the web product folder.

8.2 Single Device, Self-Controlled

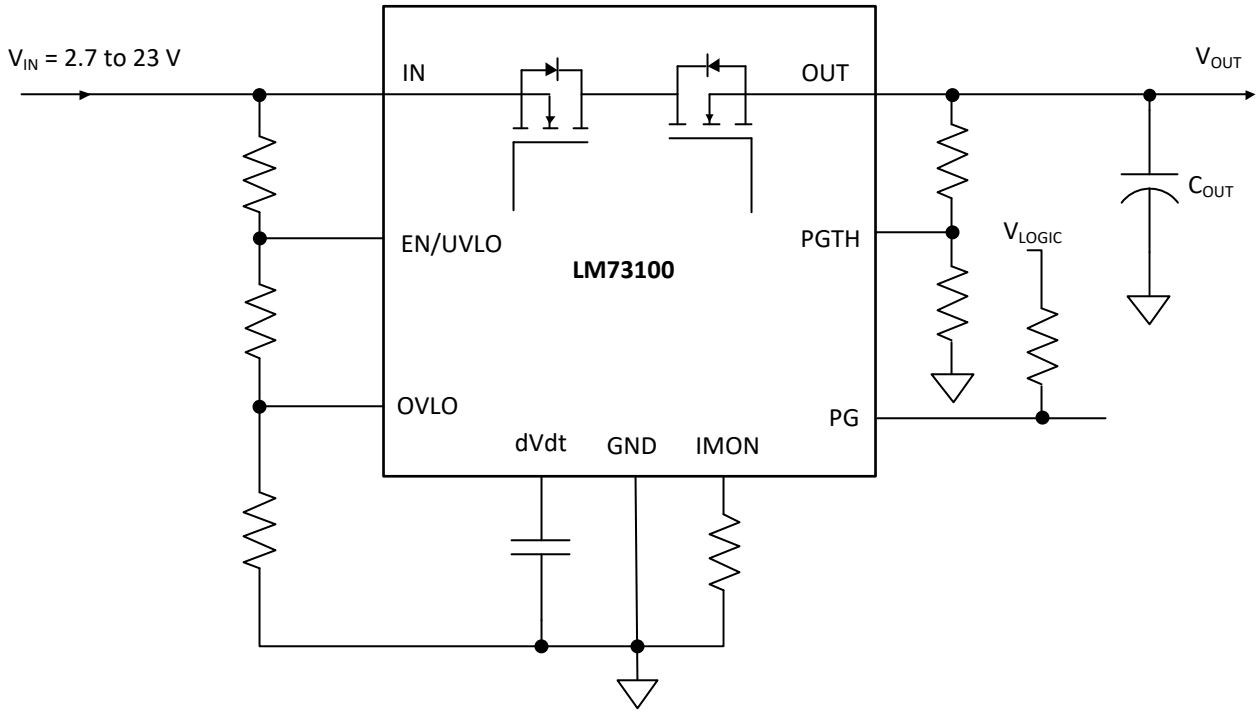


図 8-1. Single Device, Self-Controlled

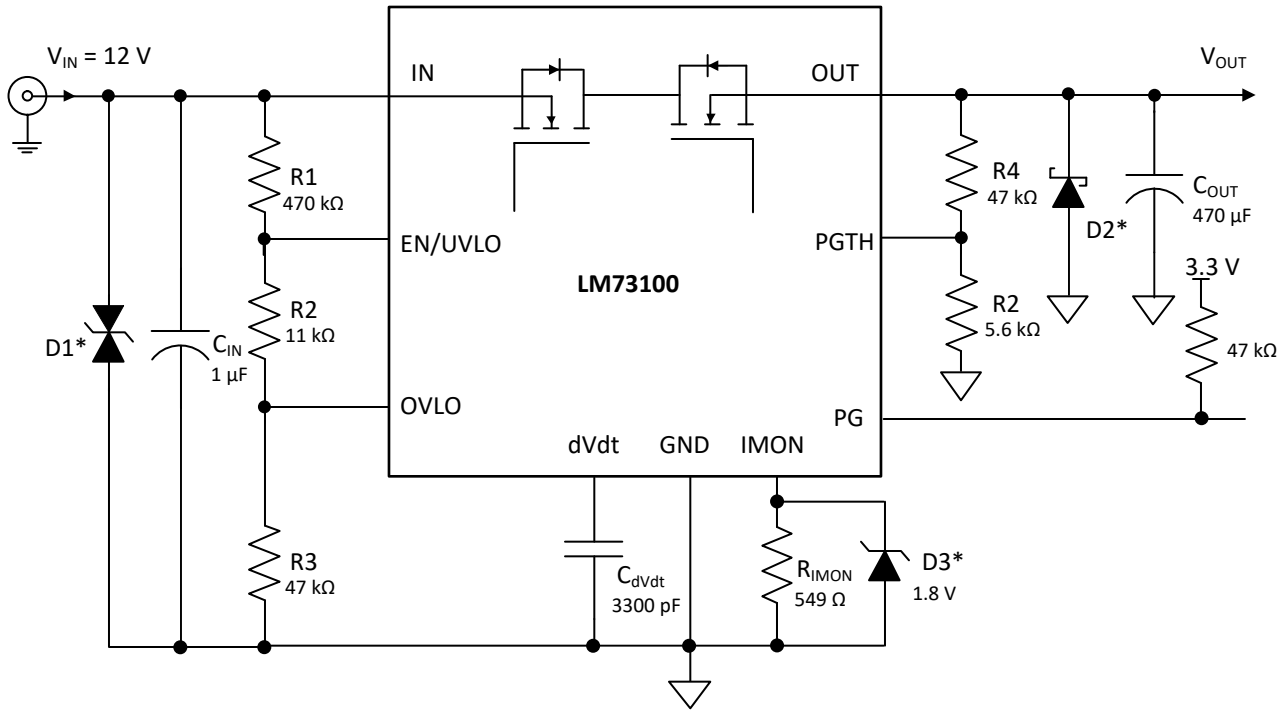
Other variations:

In a Host MCU controlled system, EN/UVLO or OVLO can also be driven from the host GPIO to control the device.

IMON pin can be connected to the MCU ADC input for current monitoring purpose.

Either V_{IN} or V_{OUT} can be used to drive the PGTH resistor divider depending on which supply needs to be monitored for power good indication.

8.2.1 Typical Application



* Optional circuit components needed for transient protection depending on input and output inductance. Please refer to *Transient Protection* section for details.

図 8-2. AC-DC Adapter Powered System - Barrel Jack Input Protection

8.2.1.1 Design Requirements

表 8-1. Design Parameters

PARAMETER	VALUE
Adapter nominal output voltage (V_{IN})	12 V
Maximum input reverse voltage	–12 V
Undervoltage threshold ($V_{IN(UV)}$)	10.8 V
Overvoltage threshold ($V_{IN(OV)}$)	13.2 V
Output Power Good threshold (V_{PG})	11.4 V
Max continuous current (I_{OUTmax})	5 A
Analog load current monitor voltage range ($V_{IMONmax}$)	0.5 V
Output capacitance (C_{OUT})	470 µF
Output rise time (t_R)	20 ms

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Setting Undervoltage and Overvoltage Thresholds

The supply undervoltage and overvoltage thresholds are set using the resistors R1, R2 & R3 whose values can be calculated using 式 6 and 式 7:

$$V_{IN(UV)} = \frac{V_{UVLO(R)} \text{ x } (R1 + R2 + R3)}{R2 + R3} \tag{6}$$

$$V_{IN(OV)} = \frac{V_{OV(R)} \text{ x } (R1 + R2 + R3)}{R3} \tag{7}$$

Where $V_{UVLO(R)}$ is the UVLO rising threshold and $V_{OV(R)}$ is the OVLO rising threshold . Because R1, R2 and R3 leak the current from input supply V_{IN}, these resistors must be selected based on the acceptable leakage current from input power supply V_{IN}. The current drawn by R1, R2 and R3 from the power supply is IR123 = V_{IN} / (R1 + R2 + R3). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR123 must be chosen to be 20 times greater than the leakage current expected on the EN/UVLO and OVLO pins.

From the device electrical specifications, both the EN/UVLO and OVLO leakage currents are 0.1 µA (max), $V_{OV(R)}$ = 1.2 V and $V_{UVLO(R)}$ = 1.2 V. From design requirements, $V_{IN(OV)}$ = 13.2 V and $V_{IN(UV)}$ = 10.8 V. To solve the equation, first choose the value of R1 = 470 kΩ and use the above equations to solve for R2 = 10.7 kΩ and R3= 48 kΩ.

Using the closest standard 1% resistor values, we get R1 = 470 kΩ, R2 = 11 kΩ, and R3 = 47 kΩ.

8.2.1.2.2 Setting Output Voltage Rise Time (t_R)

The slew rate (SR) needed to achieve the desired output rise time can be calculated as:

$$SR\,(V/ms) = \frac{V_{IN}\,(V)}{t_R\,(ms)} = \frac{12\text{ V}}{20\text{ ms}} = 0.6\text{ V/ms} \tag{8}$$

The C_{dVdt} needed to achieve this slew rate can be calculated as:

$$C_{dVdt}\,(pF) = \frac{2000}{SR\,(V/ms)} = \frac{2000}{0.6} = 3333\text{ pF} \tag{9}$$

Choose the nearest standard capacitor value as 3300 pF.

For this slew rate, the inrush current can be calculated as:

$$I_{INRUSH}\,(mA) = SR\,(V/ms) \text{ x } C_{OUT}\,(\mu F) = 0.6 \text{ x } 470 = 282\text{ mA} \tag{10}$$

The average power dissipation inside the part during inrush can be calculated as:

$$PD_{INRUSH}\,(W) = \frac{I_{INRUSH}\,(A)\ x\ V_{IN}\,(V)}{2} = \frac{0.282 \text{ x } 12}{2} = 1.69\text{ W} \tag{11}$$

The power dissipation is below the allowed limit for a successful start-up without hitting thermal shut-down within the target rise time as shown in the 図 8-3.

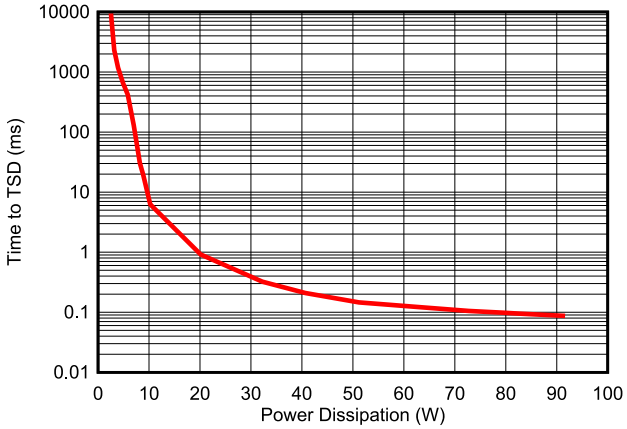


図 8-3. Thermal shut-down plot during inrush

8.2.1.2.3 Setting Power Good Assertion Threshold

The Power Good assertion threshold can be set using the resistors R4 & R5 connected to the PGTH pin whose values can be calculated as:

$$V_{PG} = \frac{V_{PGTH(R)} \text{ x } (R4 + R5)}{R5} \tag{12}$$

Because R4 and R5 leak the current from the output rail V_{OUT}, these resistors must be selected to minimize the leakage current. The current drawn by R4 and R5 from the power supply is IR45 = V_{OUT} / (R4 + R5). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR123 must be chosen to be 20 times greater than the PGTH leakage current expected.

From the device electrical specifications, PGTH leakage current is 1 µA (max), $V_{PGTH(R)}$ = 1.2 V and from design requirements, V_{PG} = 11.4 V. To solve the equation, first choose the value of R4 = 47 kΩ and calculate R5 = 5.52 kΩ. Choose nearest 1% standard resistor value as R5 = 5.6 kΩ.

8.2.1.2.4 Setting Analog Current Monitor Voltage (IMON) Range

The analog current monitor voltage range can be set using the R_{IMON} resistor whose value can be calculated as:

$$R_{IMON}\,(\Omega) = \frac{V_{IMONmax}\,(V) \text{ x } 10^{-6}}{I_{OUTmax}(A) \text{ x } G_{IMON}\,(\mu A/A)} = \frac{0.5 \text{ x } 10^{-6}}{5 \text{ x } 182} = 549.5\ \Omega \tag{13}$$

Choose nearest 1% standard resistor value as 549 Ω.

注

An additional 1.8 V zener may be needed in parallel with the R_{IMON} in applications which expect large transient currents. Please refer to the *Analog Load Current Monitor* section for more details.

8.2.1.3 Application Curves

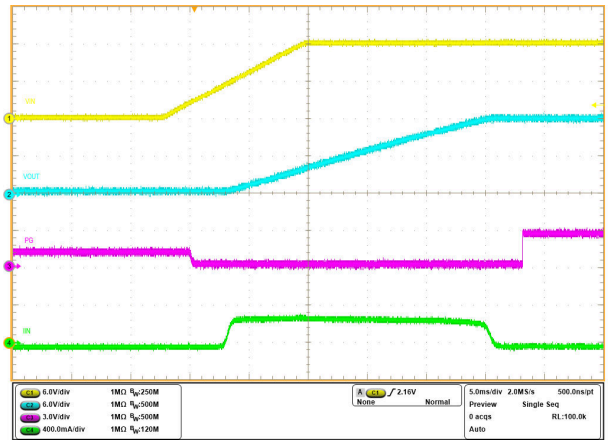


図 8-4. Power up

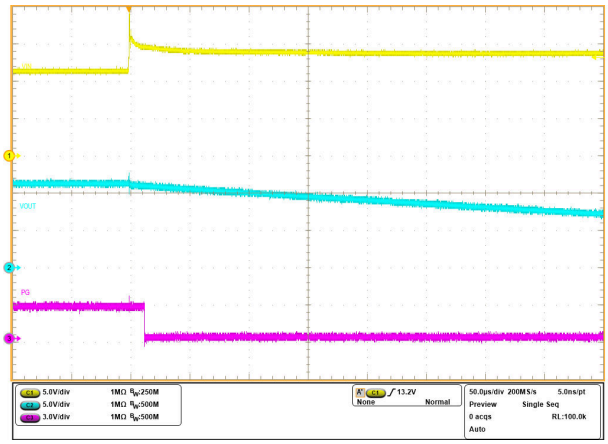


図 8-5. Overvoltage protection

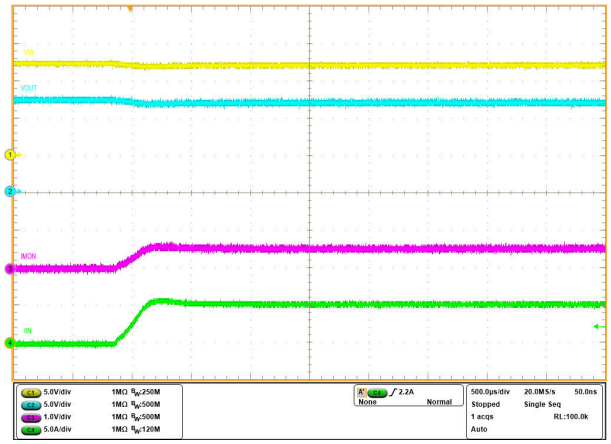


図 8-6. Analog Load Current Monitor Output

8.3 Active ORing

A typical redundant power supply configuration is shown in 図 8-7 below. Schottky ORing diodes have been popular for connecting parallel power supplies, such as parallel operation of wall adapter with a battery or a hold-up storage capacitor. Similar ORing requirements can be seen in end equipements such as PC, Notebook, Docking stations, Monitors etc.. which can take power from multiple USB ports and/or power adapter. The disadvantage of using ORing diodes is high voltage drop and associated power loss. The LM73100 with integrated, low-ohmic, back-to-back FETs provides a simple and efficient solution. Figure below shows the Active ORing implementation using the devices.

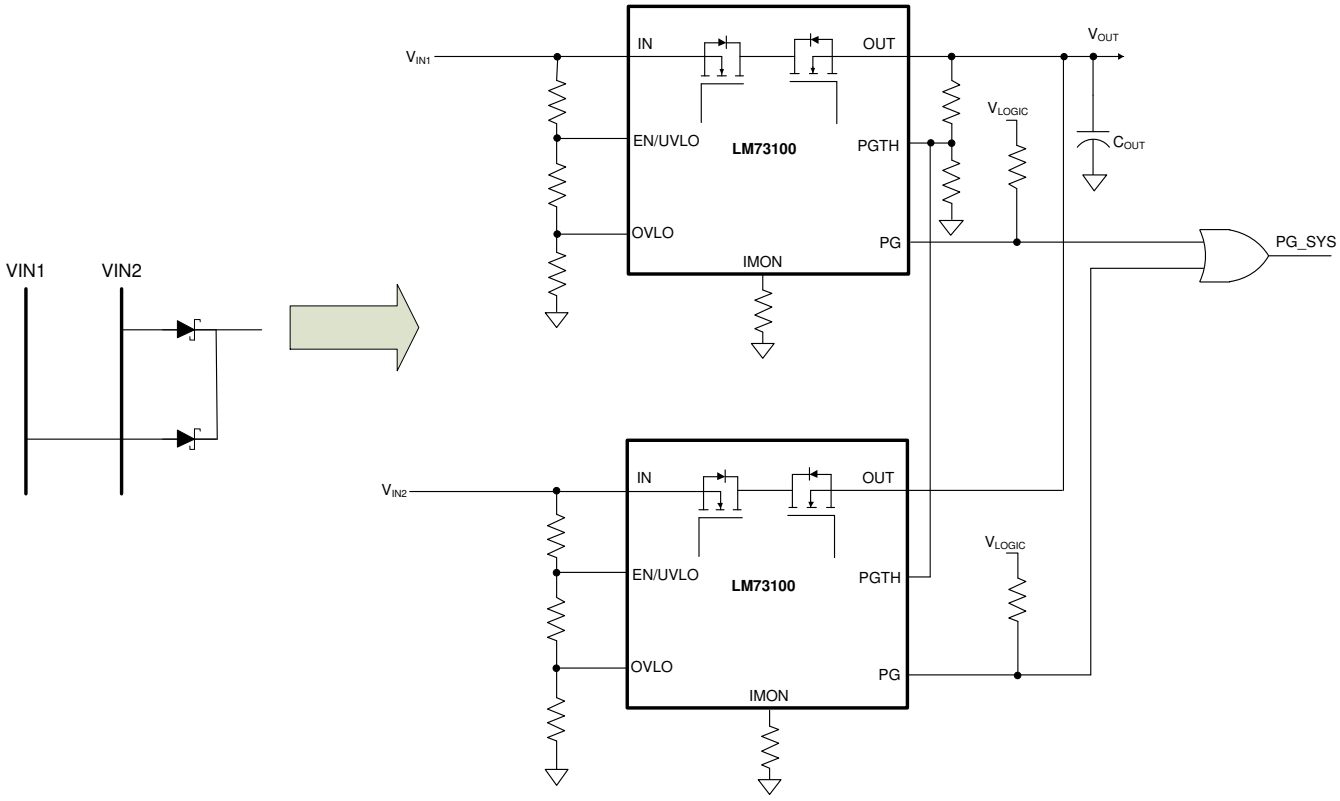
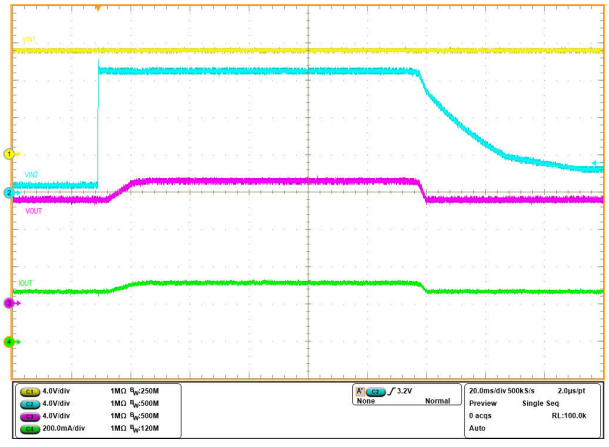


図 8-7. Two Devices, Active ORing Configuration

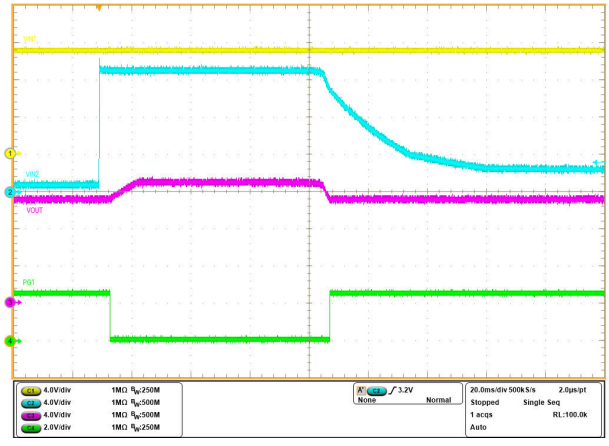
The linear ORing mechanism in LM73100 ensures that there's no reverse current flowing from one power source to the other during fast or slow ramp of either supply.

The following waveforms illustrate the active ORing behavior.



V_{IN1} = 12 V, R_{OUT} = 25 Ω, C_{OUT} = 440 µF, IN2 stepped up to 13 V and then ramped down

図 8-8. Active ORing Response



V_{IN1} = 12 V, R_{OUT} = 25 Ω, C_{OUT} = 440 µF, IN2 stepped up to 13 V and then ramped down

図 8-9. Active ORing Response

When bus voltages (IN1 and IN2) are matched, device in each rail sees a forward voltage drop and is ON delivering the load current. During this period, current is shared between the rails in the ratio of differential voltage drop across each device.

In addition to supply ORing, the devices protect the system from overvoltage, excessive inrush current and transient overcurrent events during steady state.

注

1. ORing can be done either between two similar rails (such as 12 V & 12 V; 3.3 V & 3.3 V) or between dissimilar rails (such as 12 V & 5 V).
2. For ORing cases with skewed voltage combinations, care must be taken to design circuit components on PGTH, EN/UVLO & OVLO pins for the lower voltage channel device such that the absolute maximum ratings on those pins are not exceeded when higher voltage is present on the other channel. Also, the dVdt pin capacitor rating should be chosen based on the highest of the 2 supplies. Refer to *Absolute Maximum Ratings* and *Recommended Operating Conditions* tables for more details.

8.4 Priority Power MUXing

Applications having two or more power sources such as POS terminals, Tablets and other portable battery powered equipment require preference of one source to another. For example, mains power (wall-adapter) has the priority over the internal battery back-up power. These applications demand for switchover from mains power to backup power only when main input voltage falls below a user defined threshold. The LM73100 devices provide a simple solution for priority power multiplexing needs.

図 8-10 below shows a typical priority power multiplexing implementation using LM73100 devices. When the primary (priority) power source (IN1) is present and above the undervoltage (UVLO) threshold, the primary path device path powers the OUT bus irrespective of whether auxiliary supply voltage condition. The device in auxiliary path is held in off condition by forcing its OVLO pin to high using the EN/UVLO signal of the primary path device.

Once the primary supply voltage falls below the user-defined undervoltage threshold (UVLO), the primary path device is turned off. At the same the auxiliary, the auxiliary path device turns on and starts delivering power to the load.

In this configuration, supply overvoltage protection is not available on both channels.

The PG pins of the devices can be used as a digital indication to identify which of the 2 supplies is active and delivering power to the load.

A key consideration in power MUXing applications is the minimum voltage the output bus droops to during the switchover from one supply to another. This in turn depends on multiple factors including the output load current (I_{LOAD}), output bus hold-up capacitance (C_{OUT}) and switchover time (t_{SW}).

While switching from one supply rail to the other, the minimum bus voltage can be calculated using 式 14 below. Here, the maximum switchover time (t_{SW}) is the time taken by the device to turn on and start delivering power to the load, which is equal to the device turn on time (t_{ON}), which in turn includes the turn on delay ($t_{D,ON}$) and rise time (t_R) determined by the dVdt capacitor (C_{dVdt}) and bus voltage.

$$V_{OUT(min)}(V) = \min\left(V_{IN1}, V_{IN2}\right) - \frac{t_{SW}(\mu s) \times I_{LOAD}(A)}{C_{OUT}(\mu F)} \quad (14)$$

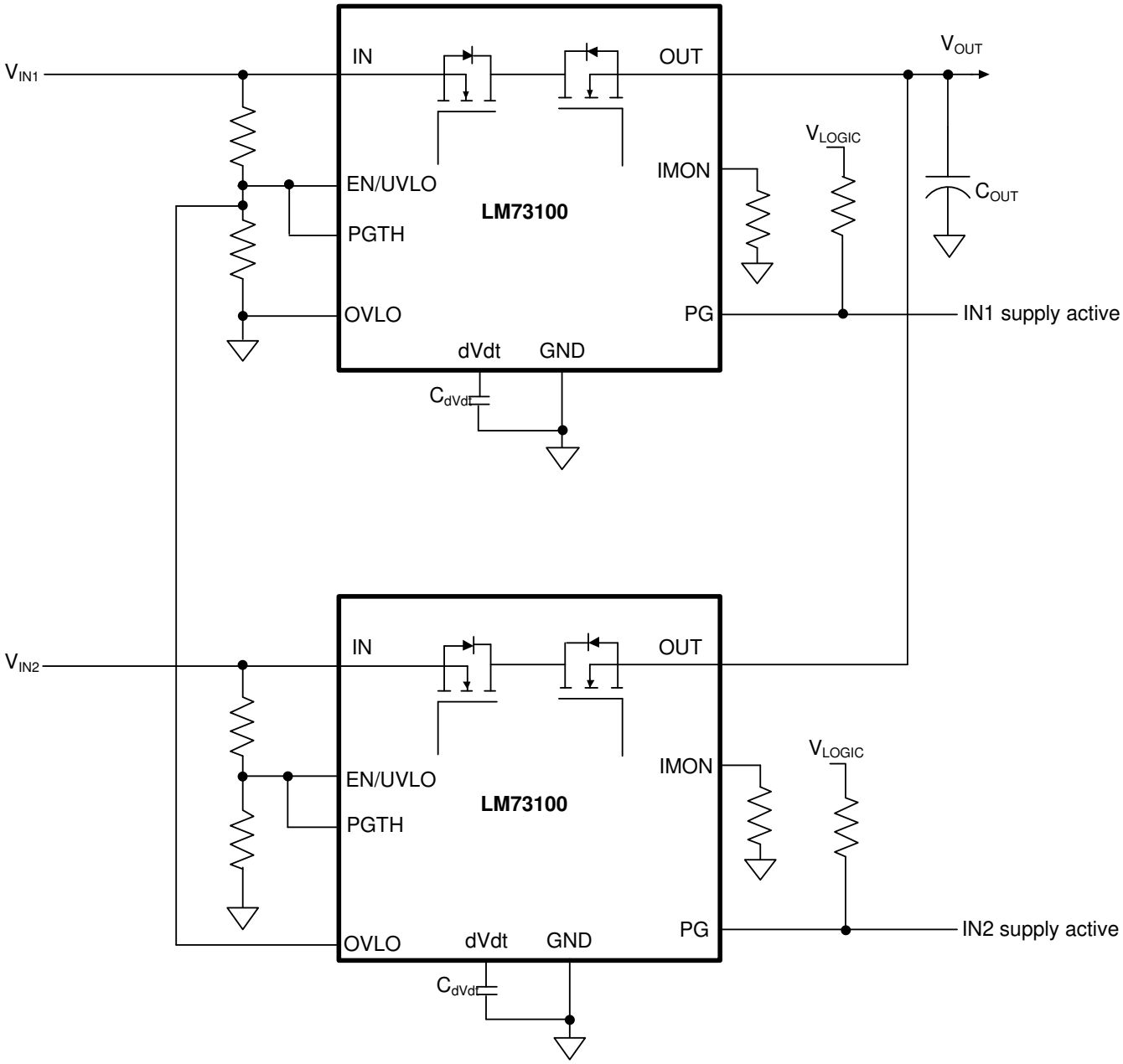


図 8-10. Two Devices, Priority Power MUX Configuration

注

1. Power MUXing can be done either between two similar rails (such as 12-V Primary & 12-V Aux; 3.3-V Primary & 3.3-V Aux) or between dissimilar rails (such as 12 V-Primary & 5-V Aux or vice versa).
2. For Power MUXing cases with skewed voltage combinations, care must be taken to design circuit components on PGTH, EN/UVLO & OVLO pins for the lower voltage channel devices such that the absolute maximum ratings on those pins are not exceeded when higher voltage is present on the other channel. Also, the dVdt pin capacitor rating should be chosen based on the highest of the 2 supplies. Refer to *Absolute Maximum Ratings* and *Recommended Operating Conditions* tables for more details.

8.5 USB PD Port Protection

End equipments like PC, Notebooks, Docking Stations, Monitors etc. have USB PD ports which can be configured as DFP (Source), UFP (Sink) or DRP (Source+Sink). LM73100 can be used independently or in conjunction with TPS259470x to handle the power path protection requirements of USB PD ports as shown in 図 8-11 below.

LM73100 provides overvoltage protection on the sink path, while blocking reverse current from internal sink rail to the port.

TPS259470x provides overcurrent & short-circuit protection in the source path, while blocking any reverse current from the port to the internal source power rail. The fast recovery from reverse current blocking ensures minimum supply droop during Fast Role Swap (FRS) events. The PD controller can also use the OVLO pin as an active low enable signal to control the power path. Holding the OVLO pin high keeps the device in OFF state in sink mode and blocks current in both directions. Once the PD controller determines the need to start sourcing power, it can pull the OVLO pin low to trigger a fast recovery from OFF to ON state, meeting the FRS timing requirements.

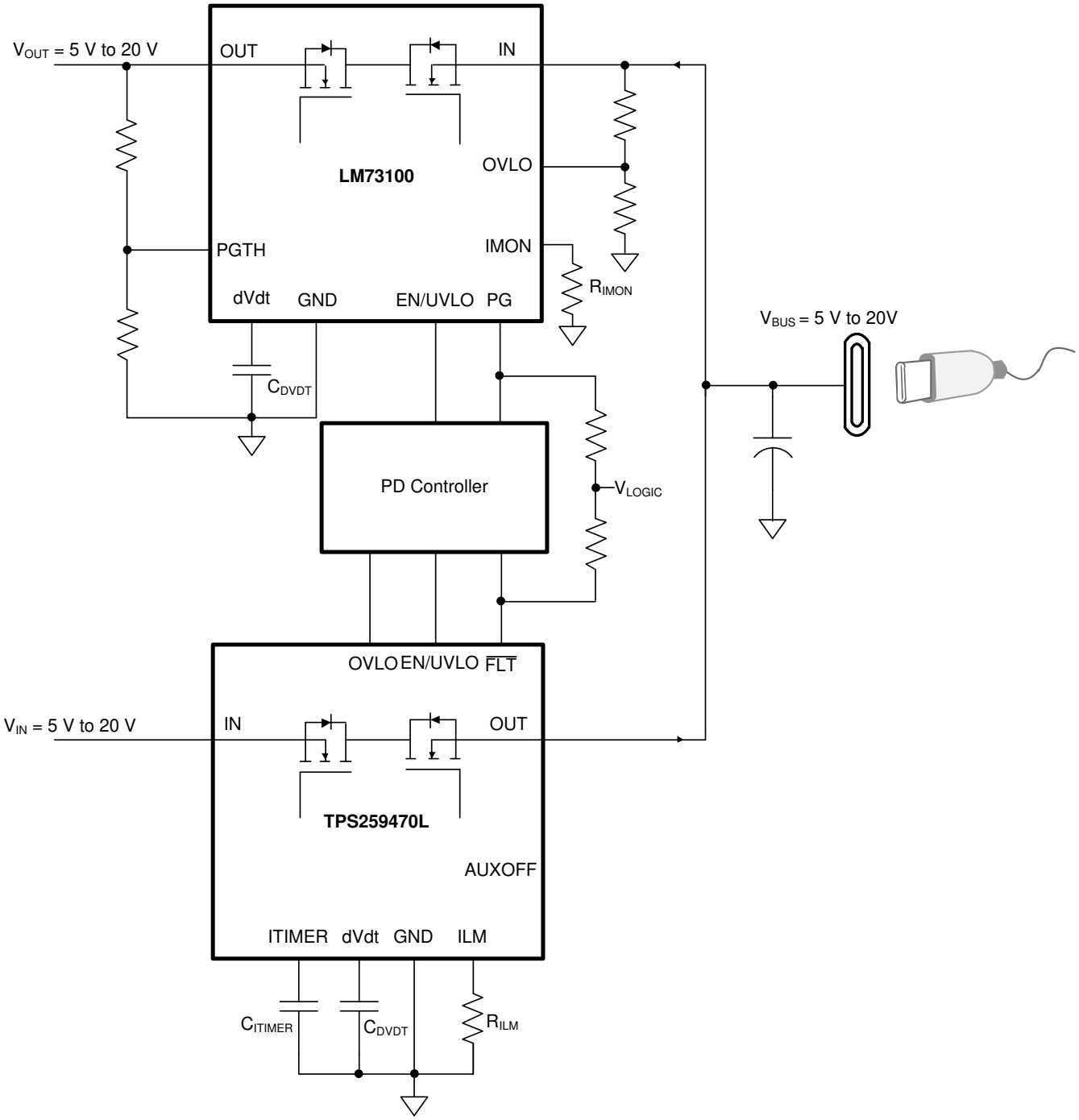


図 8-11. USB PD Port Protection

The linear ORing mechanism in TPS259470x & LM73100 ensures that there's no reverse current flowing from one power source to the other during fast or slow ramp of either supply.

The following waveforms illustrate the LM73100 reverse current blocking behavior in USB applications.

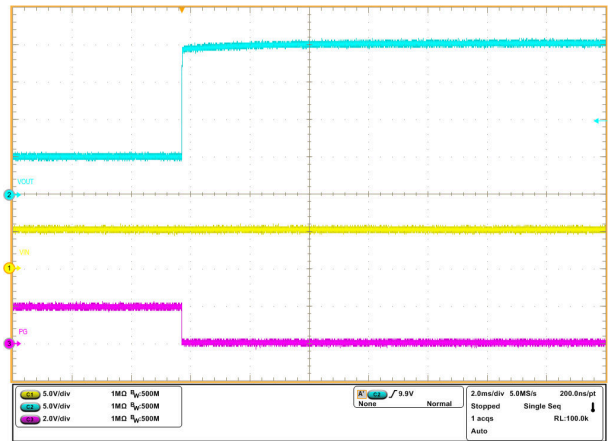


図 8-12. LM73100 Reverse Current Protection During 20-V Hot-Plug at Output

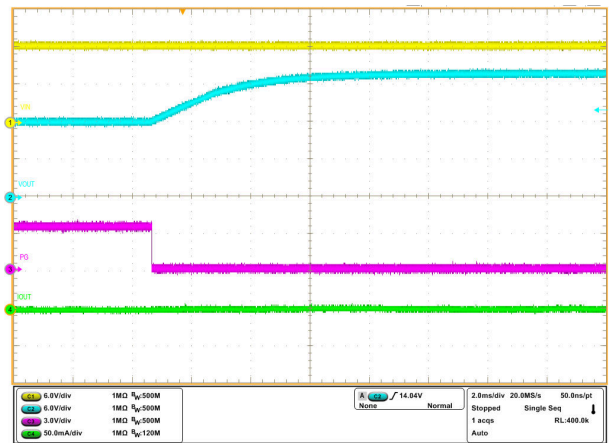


図 8-13. LM73100 Reverse Current Protection During 20-V Voltage Ramp at Output

8.6 Parallel Operation

Applications which need higher steady state current can use multiple LM73100 devices connected in parallel as shown in 図 8-14 below. In this configuration, the first device turns on initially to provide the inrush current limiting. The second device is held in an OFF state by driving its EN/UVLO pin low by the PG signal of the first device. Once the inrush sequence is complete, the first device asserts its PG pin high, allowing the second device to turn. The second device asserts its PG signal to indicate that it has turned on fully, thereby indicating to the system that the parallel combination is ready to deliver the full steady state current.

Once in steady state, the devices share current nearly equally. There could be a slight skew in the currents depending on the part-to-part variation in the R_{ON} as well as the PCB trace resistance mismatch.

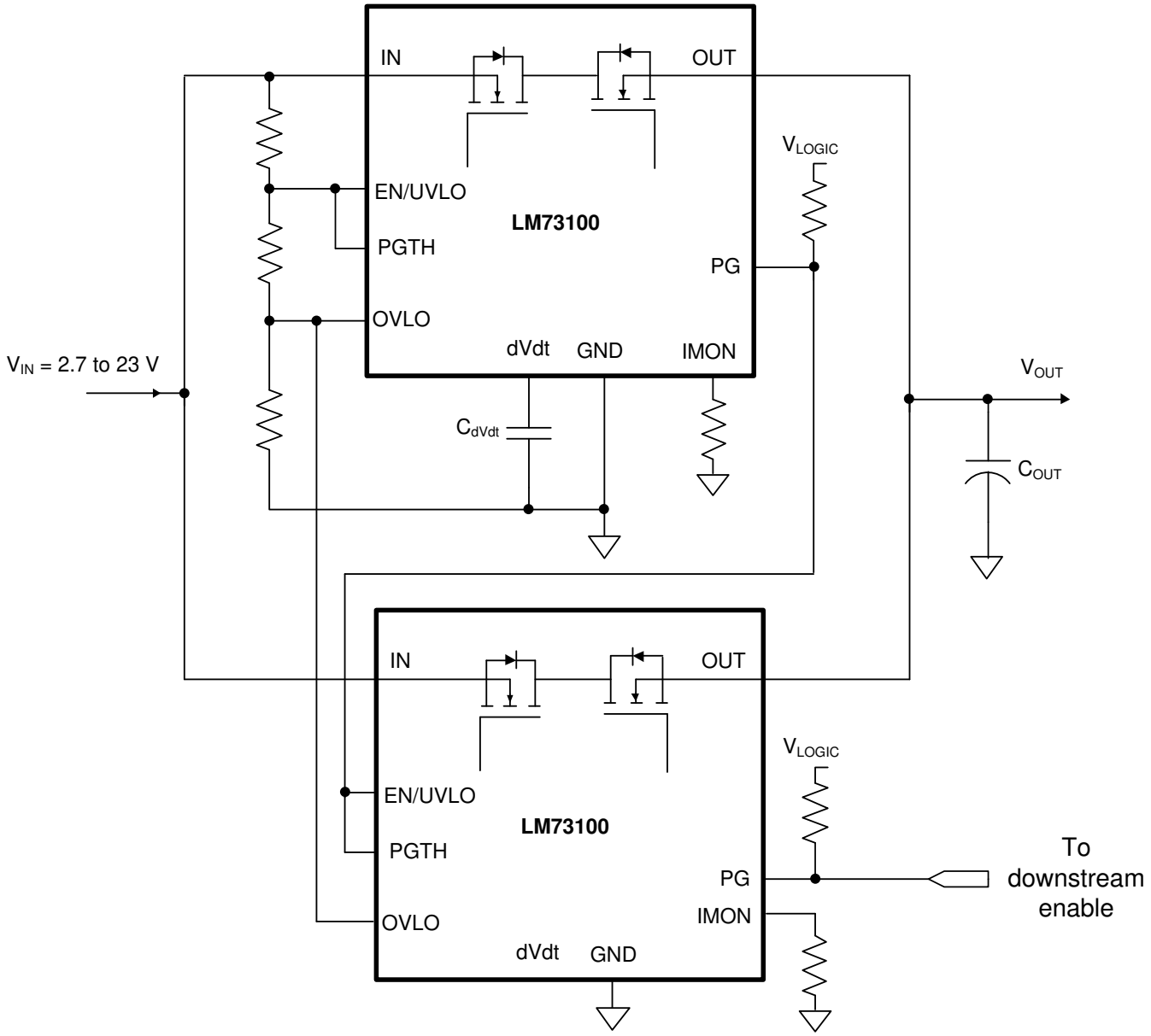


図 8-14. Two Devices Connected in Parallel for Higher Steady State Current Capability

9 Power Supply Recommendations

The LM73100 devices are designed for a supply voltage range of 2.7 V ≤ V_{IN} ≤ 23 V. An input ceramic bypass capacitor higher than 0.1 µF is recommended if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

The maximum negative voltage the device can handle at the input is limited to -15 V or V_{OUT} – 21 V, whichever is higher. Any low voltage signals (e.g. EN/UVLO, OVLO, PGTH) derived from the input supply must have a sufficiently large pull-up resistor to limit the current through those pins to < 10 µA during reverse polarity conditions. Please refer to *Absolute Maximum Ratings* table for more details.

9.1 Transient Protection

When the device interrupts current flow in the case of a fast-trip event or during normal switch off, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor of value greater than 1 µF at the OUT pin very close to the device.
- Use a low-value ceramic capacitor C_{IN} = 1 µF to absorb the energy and dampen the transients. The capacitor voltage rating should be atleast twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

The approximate value of input capacitance can be estimated with 式 15:

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (15)$$

where

- V_{IN} is the nominal supply voltage.
- I_{LOAD} is the load current.
- L_{IN} equals the effective inductance seen looking into the source.
- C_{IN} is the capacitance present at the input.

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

注

If there's a likelihood of input reverse polarity in the system, it's recommended to use a bi-directional TVS, or a reverse blocking diode in series with the TVS.

The circuit implementation with optional protection components is shown in 図 9-1.

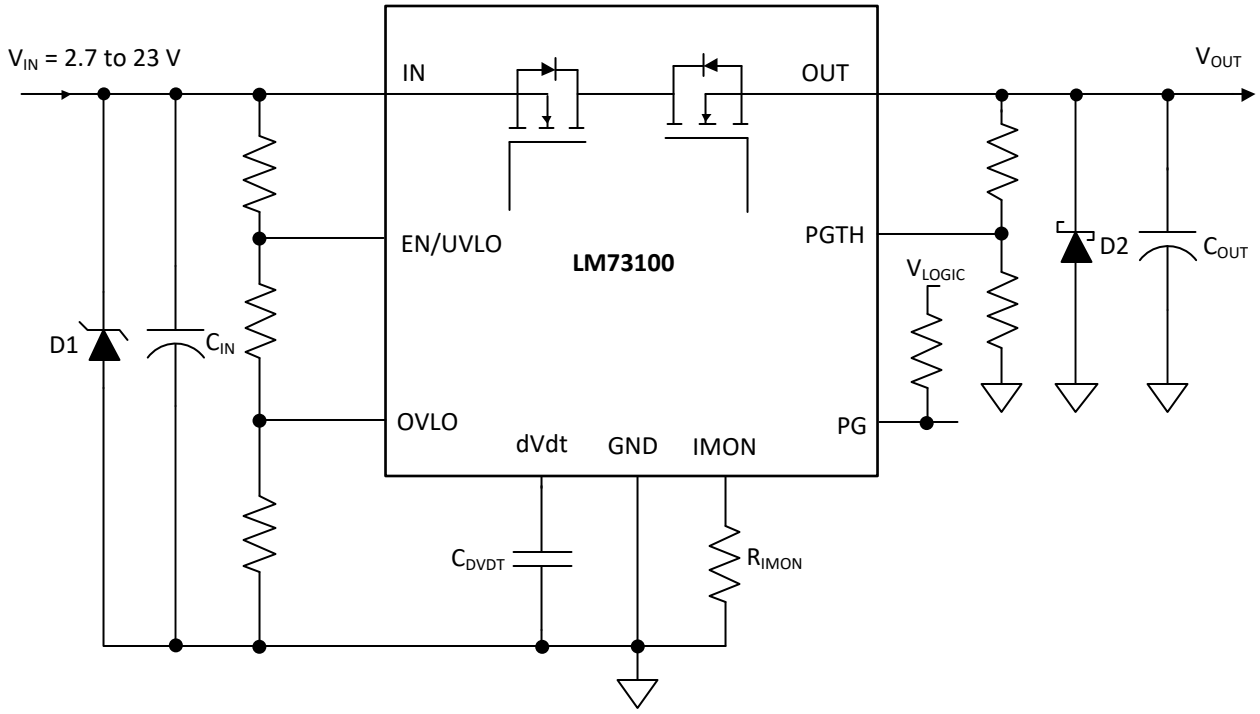


図 9-1. Circuit Implementation with Optional Protection Components

10 Layout

10.1 Layout Guidelines

- For all applications, a ceramic decoupling capacitor of 0.1 µF or greater is recommended between the IN terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN pin and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN pin and the GND terminal of the IC.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal of the device must be tied to the PCB ground plane at the terminal of the IC with the shortest possible trace. The PCB ground must be a copper plane or island on the board. It's recommended to have a separate ground plane island for the device. This plane doesn't carry any high currents and serves as a quiet ground reference for all the critical analog signals of the device. The device ground plane should be connected to the system power ground plane using a star connection.
- The IN and OUT pins are used for heat dissipation. Connect to as much copper area on top and bottom PCB layers using as possible with thermal vias. The vias under the device also help to minimize the voltage gradient accross the IN and OUT pads and distribute current unformly through the device, which is essential to achieve the best on-resistance and current sense accuracy.
- Locate the following support components close to their connection pins:
  - R_{IMON}
  - C_{dVdT}
  - Resistors for the EN/UVLO, OVLO and PGTH pins
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the C_{dVdt} must be as short as possible to reduce parasitic effects on the soft-start timing. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended between OUT terminal and GND terminal to address negative transients due to switching of inductive loads. It's also recommended to add a ceramic decoupling capacitor of 1 µF or greater between OUT and GND. These components must be physically close to the OUT pins. Care must be taken to minimize the loop area formed by the Schottky diode/bypass-capacitor connection, the OUT pin and the GND terminal of the IC.

10.2 Layout Example

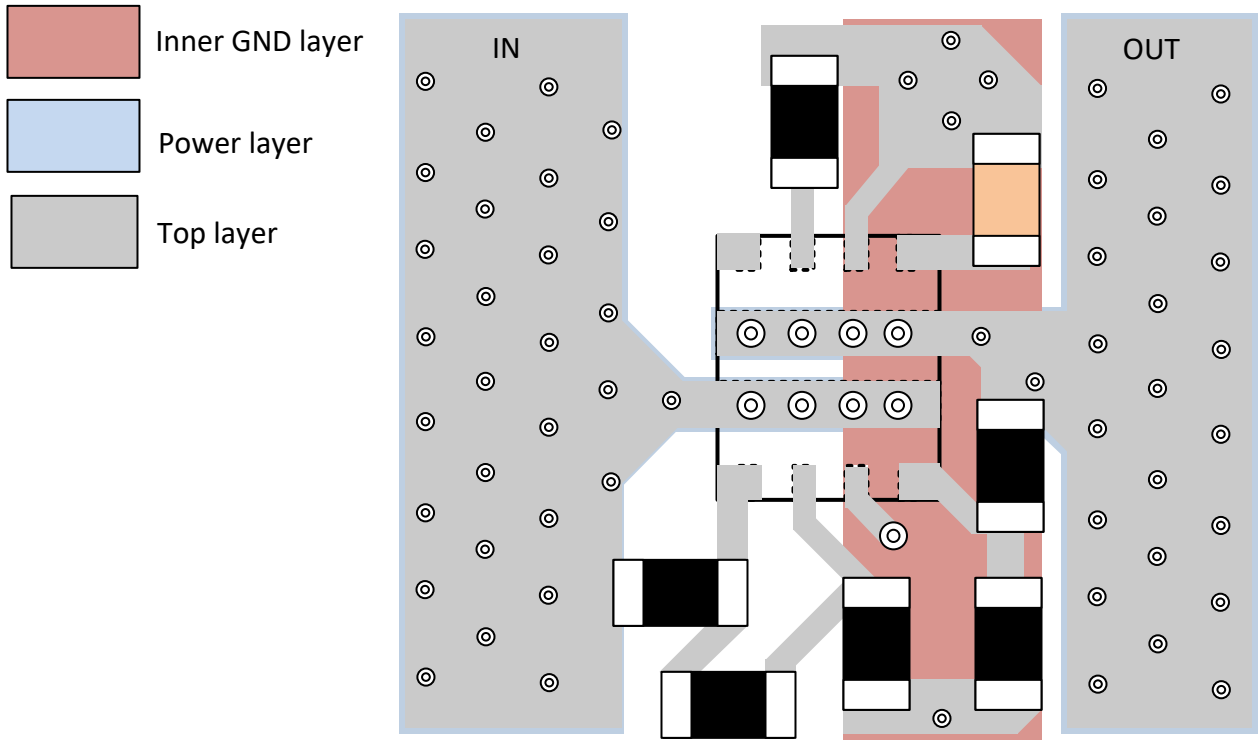


図 10-1. Layout Example - Single LM73100 with PGTH Referred to OUT

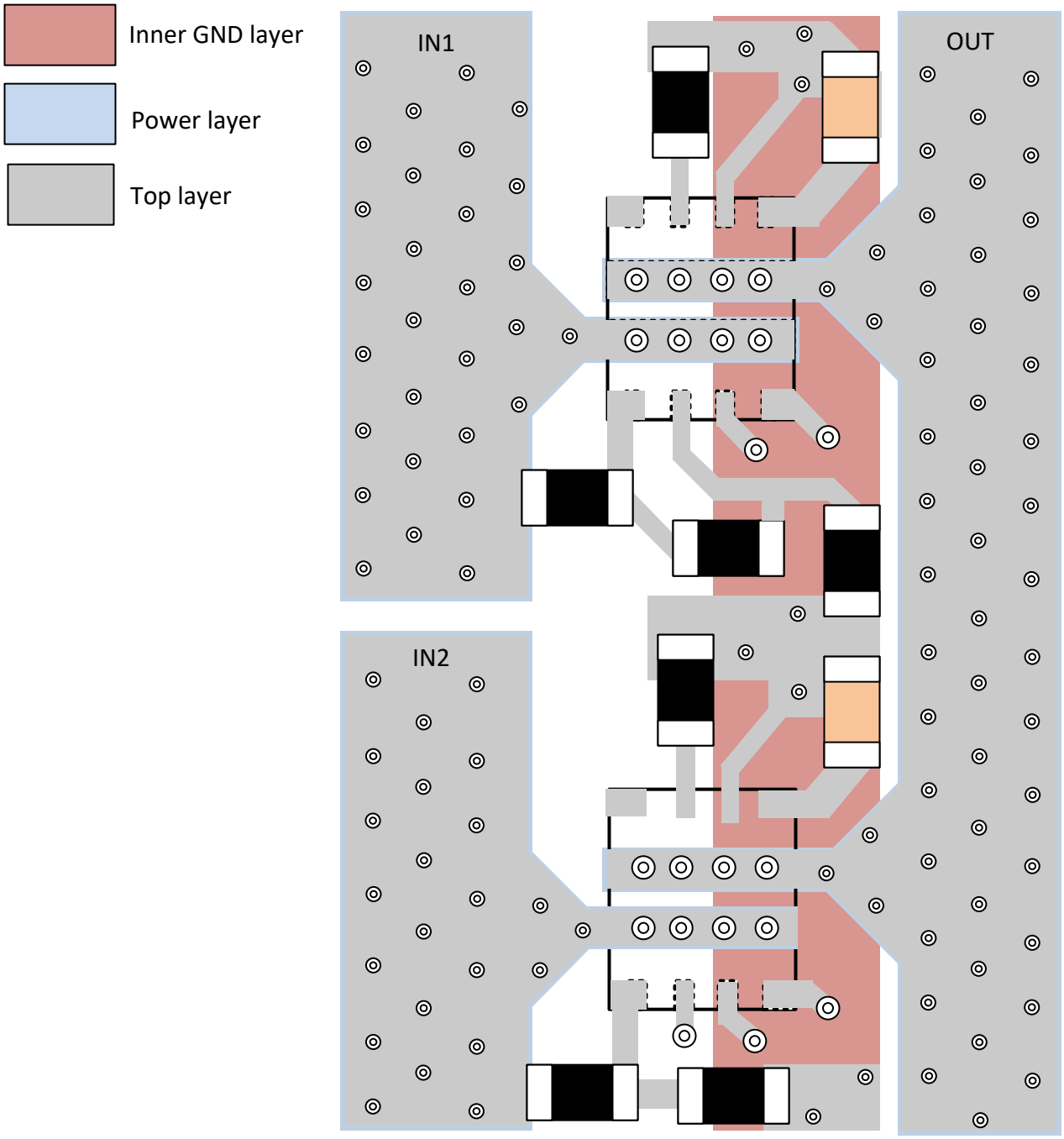


図 10-2. Layout Example - 2 x LM73100 in ORing Configuration

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *LM73100EVM Ideal Diode Evaluation Board*
- *Application note - eFuses for USB Type-C protection*
- *LM73100 Design Calculator*

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。*「更新の通知を受け取る」をクリック*して登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

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11.4 商標

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11.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい ESD 対策をとらないと、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

TI 用語集　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM73100RPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	Call TI | SN	Level-2-260C-1 YEAR	-40 to 125	2AEH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

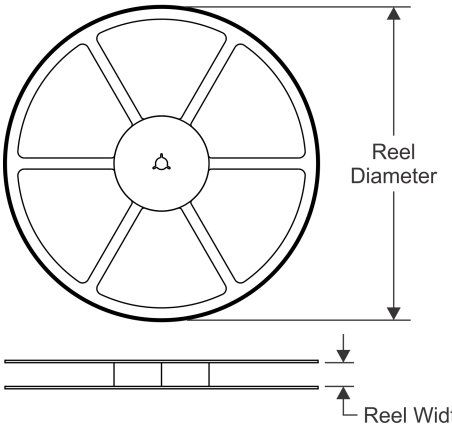
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

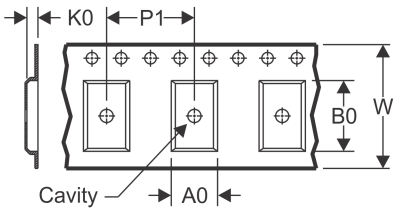
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

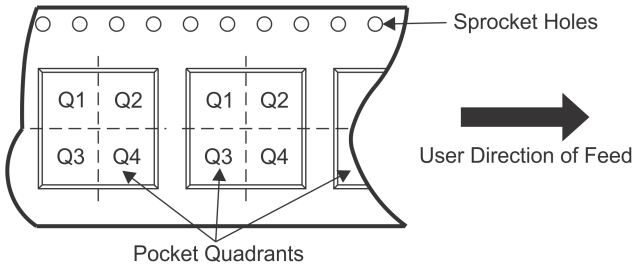


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

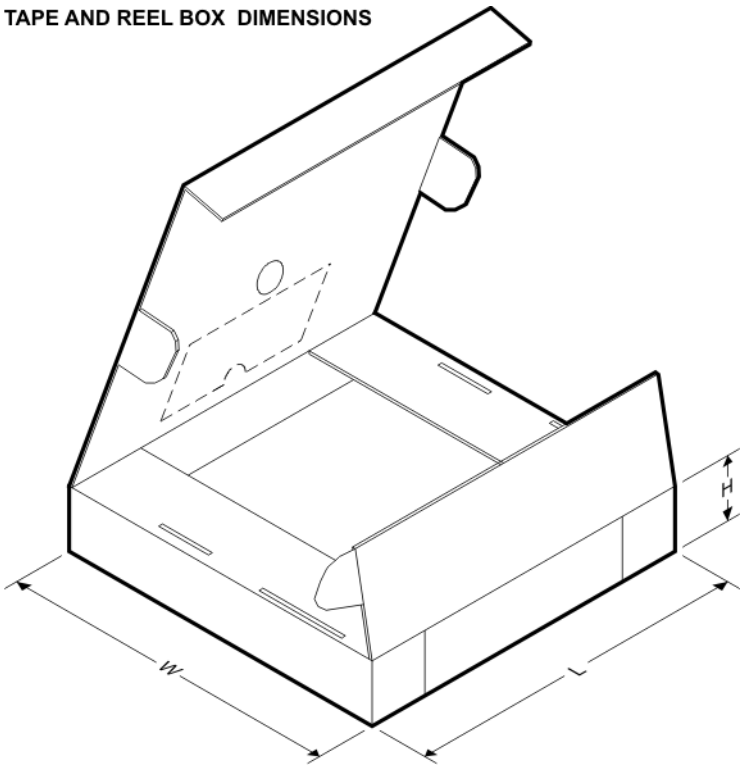
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM73100RPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

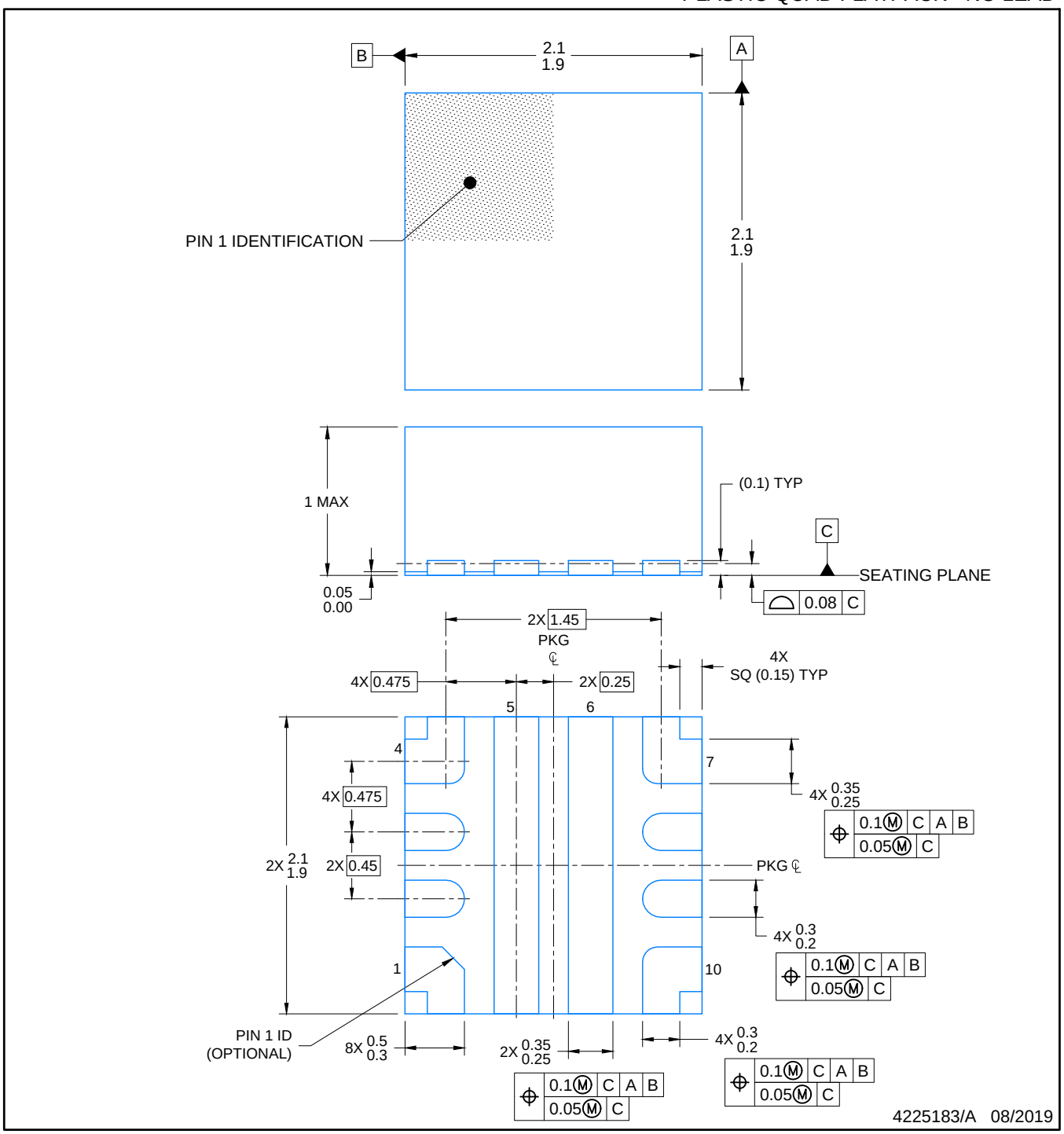
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM73100RPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RPW0010A

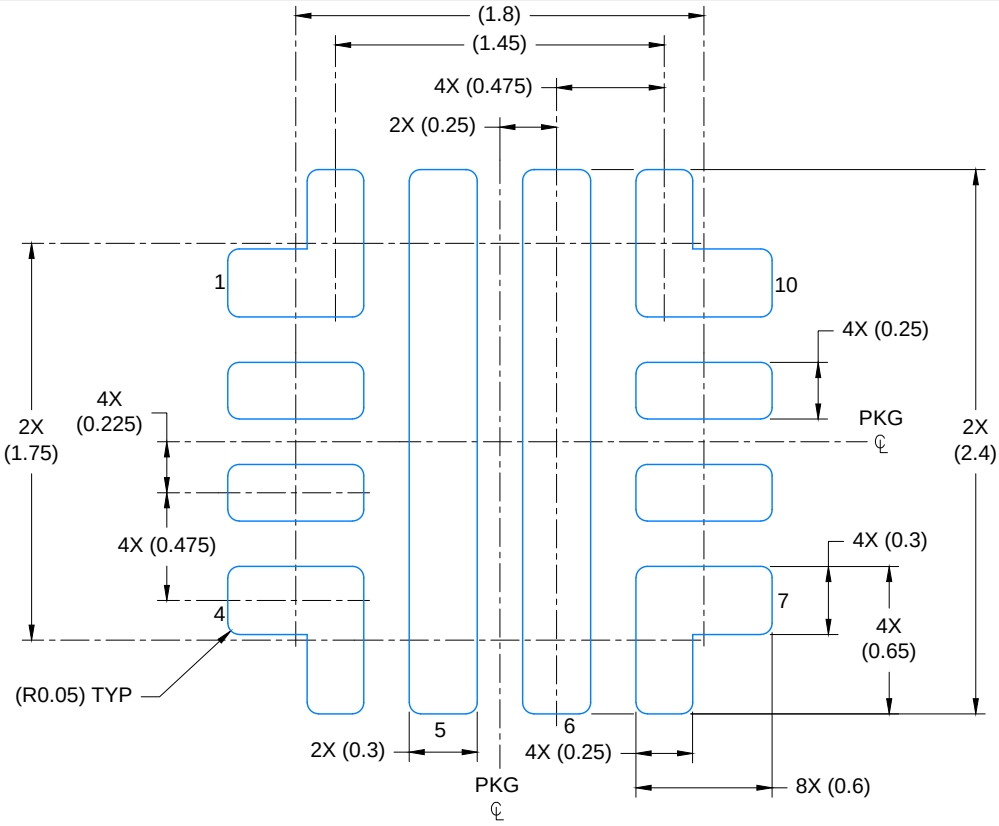
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



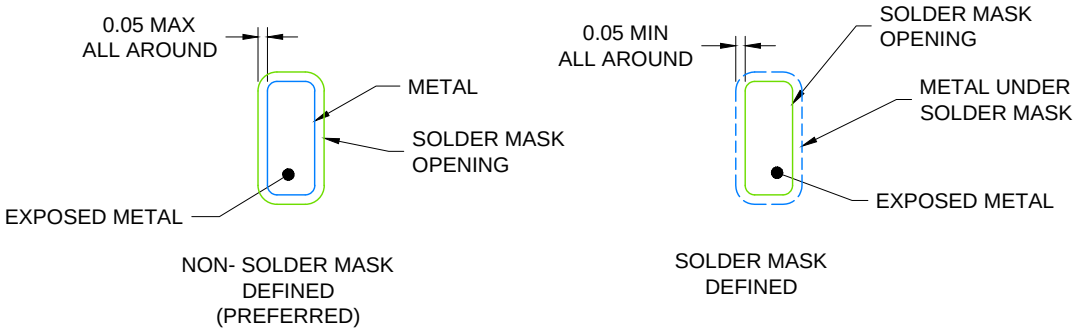
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 30X



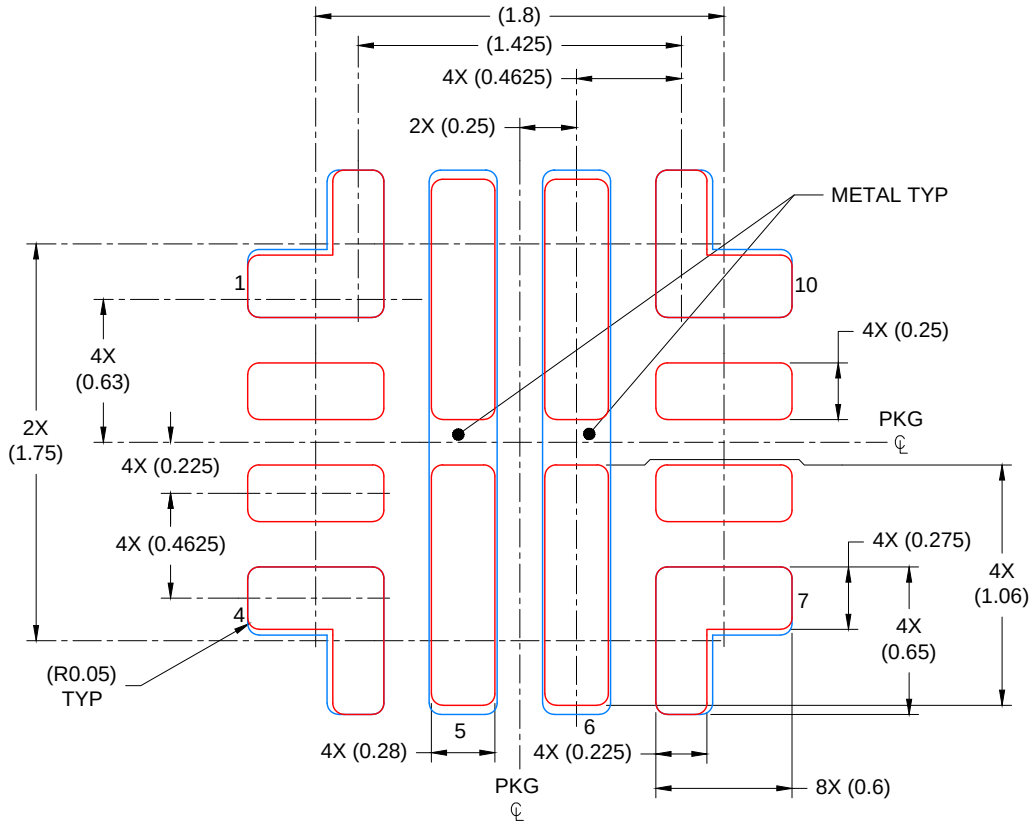
SOLDER MASK DETAILS

NOT TO SCALE

4225183/A 08/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL

PADS 1, 4,7 & 10: 93%; PADS 5 & 6: 82%
SCALE: 30X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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