TCA39306 デュアル双方向 I²C バス / SMBus 電圧レベル・シフタ

1 特長

- 混在モードの I²C アプリケーションで、SDA および SCL ライン用の 2 ビット双方向トランスレータ
- 標準モード、ファースト・モード、ファースト・モード・プラスの I²C および SMBus と互換
- I³C 互換 (12.5MHz 対応)
- 次の電圧レベル変換が可能
  - 0.9V の V_{REF1} と、1.8V、2.5V、3.3V、5V の V_{REF2}
  - 1.2V の V_{REF1} と、1.8V、2.5V、3.3V、5V の V_{REF2}
  - 1.8V の V_{REF1} と、2.5V、3.3V、5V の V_{REF2}
  - 2.5V の V_{REF1} と、3.3V または 5V の V_{REF2}
  - 3.3V の V_{REF1} と、5V の V_{REF2}
- 方向ピンを必要としない双方向電圧レベル変換
- オン状態での入力と出力ポート間の低抵抗により信号の歪みを低減
- オープン・ドレインの I²C I/O ポート (SCL1、SDA1、SCL2、SDA2)
- 5V 許容の I²C I/O ポートにより、混在モード信号動作をサポート
- EN = LOW のとき、SCL1、SDA1、SCL2、SDA2 ピンが高インピーダンス
- EN = LOW のとき、絶縁のためのロックアップ・フリー動作
- フロースルー・ピン配置によりプリント基板の配線を簡素化
- JESD 22 を超える ESD 保護
  - 人体モデル 2000V (A114-A)
  - デバイス帯電モデル 1000V (C101)

2 アプリケーション

- I²C、SMBus、PMBus、MDIO、UART、低速 SDIO、GPIO、その他の 2 信号インターフェイス
- サーバー
- ルーター (テレコム・スイッチング機器)
- パーソナル・コンピュータ
- 産業用オートメーション

3 概要

TCA39306 は、I²C、SMBus、I³C と互換性のあるデュアル双方向電圧レベル・シフタであり、イネーブル (EN) 入力付きで、0.9V～3.3V の V_{REF1} と、1.8V～5.5V の V_{REF2} で動作します。

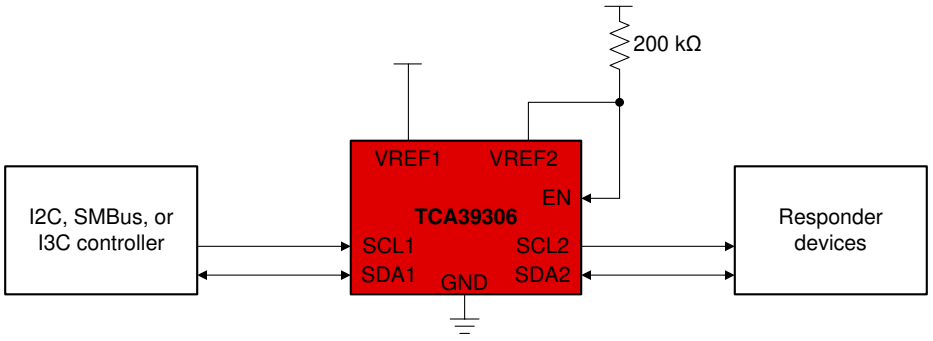
このデバイスは、方向ピンを使用せず、0.85V と 5V の間の電圧を双方向に変換できます。スイッチのオン抵抗 (R_{ON}) が低いため、最小の伝播遅延で接続が可能です。EN を HIGH にすると、トランスレータ・スイッチがオンになり、SCL1 および SDA1 I/O がそれぞれ SCL2 および SDA2 I/O に接続され、ポート間の双方向データ・フローが可能になります。EN が LOW のとき、トランスレータ・スイッチはオフになり、ポート間は高インピーダンス状態になります。

電圧変換に加えて、TCA39306 は、EN ピンを制御してファーストモード通信中に低速なバスを切断することにより、高速なバスを低速なバスから分離できます。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
TCA39306	VSSOP (8)	2.30mm × 2.00mm
	SOT-23 (8)	2.90mm × 1.60mm
	X2SON (8)	1.35mm × 0.80mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



アプリケーション概略図

Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Conditions ... 4
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 5
6.6 Switching Characteristics ... 6
6.7 Typical Characteristics ... 8
7 Parameter Measurement Information ... 9
8 Detailed Description ... 11
8.1 Overview ... 11
8.2 Functional Block Diagram ... 16
8.3 Feature Description ... 16
8.4 Device Functional Modes ... 16
9 Application and Implementation ... 17
9.1 Application Information ... 17
9.2 Typical Application ... 17
9.3 Systems Examples: I3C Usage Considerations ... 20
9.4 Power Supply Recommendations ... 22
9.5 Layout ... 22
10 Device and Documentation Support ... 24
10.1 Receiving Notification of Documentation Updates ... 24
10.2 サポート・リソース ... 24
10.3 Trademarks ... 24
10.4 静電気放電に関する注意事項 ... 24
10.5 用語集 ... 24
11 Mechanical, Packaging, and Orderable Information ... 24

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (August 2021) to Revision B (March 2023) **Page**

- 「製品情報」表の SOT-23 から「製品プレビュー」の注を削除 ... 1
- Added DDF (SOT-23) to the *Thermal Information* table ... 5

Changes from Revision * (June 2021) to Revision A (August 2021) **Page**

- ドキュメントのステータスを「*事前情報*」から「*量産データ*」に変更 ... 1

5 Pin Configuration and Functions

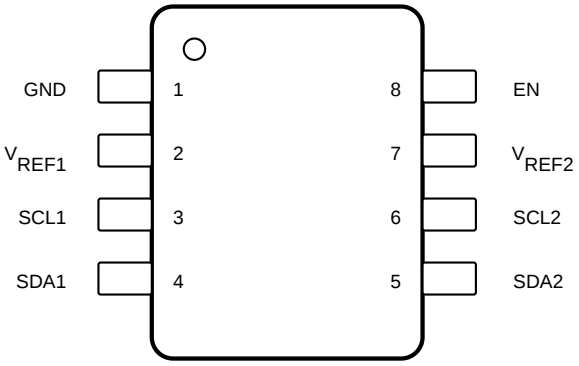


図 5-1. DDF Package, 8-Pin SOT, Top View

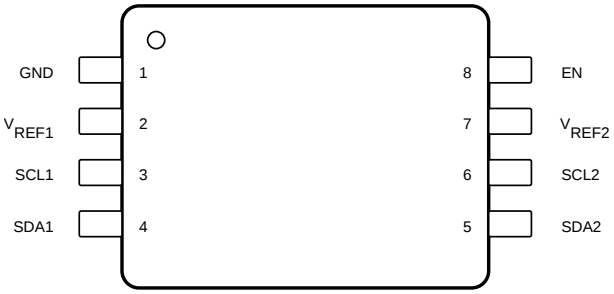
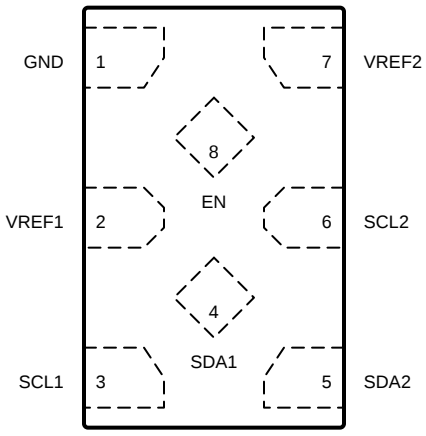


図 5-2. DCU Package, 8-Pin VSSOP, Top View



Not to scale

図 5-3. DTM Package, 8-Pin X2SON, Top View

表 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	DCU, DDF	DTM		
EN	8	8	I	Switch enable input
GND	1	1	—	Ground, 0 V
SCL1	3	3	I/O	Serial clock, low-voltage side
SCL2	6	6	I/O	Serial clock, high-voltage side
SDA1	4	4	I/O	Serial data, low-voltage side
SDA2	5	5	I/O	Serial data, high-voltage side
V_{REF1}	2	2	I	Low-voltage-side reference supply voltage for SCL1 and SDA1
V_{REF2}	7	7	I	High-voltage-side reference supply voltage for SCL2 and SDA2

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{REF1}	DC reference voltage range	–0.5	7	V
V_{REF2}	DC reference bias voltage range	–0.5	7	V
V_I	Input voltage range (2)	–0.5	7	V
$V_{I/O}$	Input-output voltage range (2)	–0.5	7	V
	Continuous channel current		128	mA
I_{IK}	Input Clamp Current (V_I < 0)		–50	mA
$T_{J(Max)}$	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) *Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.*
(2) The input and input-output negative voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
$V_{I/O}$	Input-output voltage	SCL1, SDA1, SCL2, SDA2	0	5.5	V
V_{REF1} (1)	Reference Voltage		0	5.5	V
V_{REF2} (1)	Reference Voltage		0	5.5	V
EN-Switch(2)	Switch mode enable voltage (Switch mode enable voltage)		1.5	5.5	V
EN	Enable input voltage		0	5.5	V
I_{PASS}	Pass switch current			64	mA
T_A	Ambient temperature		–40	125	°C

(1) To support translation, V_{REF1} supports 0.85 V to VREF2 - 0.6 V. V_{REF2} must be between VREF1 + 0.6 V to 5.5 V. See Typical Application for more information.
(2) To support switching, V_{REF1} and V_{REF2} Do not need to be connected. EN pin should use a voltage not less than 1.5V when the switch mode is to be enabled. Enabled voltage on this pin should be equal to 1.5V or I/O supply voltage, whichever is higher.

6.4 Thermal Information

THERMAL METRIC[1]		TCA39306			UNIT
		DCU	DDF	DTM	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	275.5	273.0	289.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	127.1	180.7	185.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	186.9	188.4	193.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	65.7	47.8	27.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	185.9	187.8	193.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP (1)	MAX	UNIT
V_{IK}	Input clamp voltage		I_I = -18 mA	EN = 0 V		-1.2		0	V
I_{IH}	Input leakage current		V_I = 5 V, V_O = 0V	EN = 0 V				5	µA
V_T	Threshold voltage		I_O = 500 µA	V_I = 0.1 V, V_O = 0 V, Find V_{EN} where IO = 500 µA			0.7	1.0	V
$C_{I(EN)}$	Input capacitance		V_I = 3 V or 0 V				11		pF
$C_{IO(off)}$	Off capacitance	SCLn, SDAn	V_O = 3 V or 0 V	EN = 0 V			4	6	pF
$C_{IO(on)}$	On capacitance	SCLn, SDAn	V_O = 3 V or 0 V	EN = 3 V			10.5	12.5	pF
R_{ON} [2]	On-state resistance	SCLn, SDAn (-40 to 125C)	V_I = 0 V[3]	I_O = 64 mA	EN = 4.5 V		3.5	5.5	Ω
			V_I = 0 V[3]	I_O = 64 mA	EN = 3 V		4.7	7	Ω
			V_I = 0 V[3]	I_O = 64 mA	EN = 2.3 V		6.3	9.5	Ω
			V_I = 0 V[3]	I_O = 15 mA	EN = 1.5 V		25.5	32	Ω
			V_I = 2.4 V[4]	I_O = 15 mA	EN = 4.5 V	1	6	15	Ω
			V_I = 2.4 V[4]	I_O = 15 mA	EN = 3 V	20	50	75	Ω
			V_I = 1.7 V[4]	I_O = 15 mA	EN = 2.3 V	20	55	75	Ω

6.5 Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS			MIN	TYP (1)	MAX	UNIT
R_{ON}	On-state resistance	SCLn, SDAn	V_I = 0 V, VCC2 = 5 V(5)	I_O = 64 mA	VCC1 = 1 V		5	25	Ω
					VCC1 = 1.8 V		4	10	
					VCC1 = 2.5 V		3	8	
					VCC1 = 3.3 V		3	7	
				I_O = 32 mA	VCC1 = 1 V		5	10	Ω
					VCC1 = 1.8 V		4	9	
					VCC1 = 2.5 V		3	8	
					VCC1 = 3.3 V		3	7	
			V_I = 1.8 V, VCC2 = 5 V(5)	I_O = 15 mA	VCC1 = 3.3 V		4	13	Ω
			V_I = 1 V, VCC2 = 3.3 V(5)	I_O = 10 mA	VCC1 = 1.8 V		7	24	Ω
			V_I = 0 V, VCC2 = 3.3 V(5)	I_O = 10 mA	VCC1 = 1 V		5	18	Ω
			V_I = 0 V, VCC2 = 1.8 V(5)	I_O = 10 mA	VCC1 = 1 V		6	19	Ω

(1) All typical values are at T_A = 25°C.
(2) Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals, at the indicated current through the switch. Minimum ON-state resistance is determined by the lowest voltage of the two terminals.
(3) Measured in current source configuration only. See 図 7-1
(4) Measured in current sink configuration only. See 図 7-1
(5) Measured in application connected current source configuration only. See 図 7-2

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{PLH}	Low-to-high propagation delay(1)	V_{CC1} = 0.85 V, V_{CC2} = 1.98 V, R_{L_Input} = 1.35 kΩ	C_L = 15 pF			13	ns
			C_L = 50 pF			32	
		V_{CC1} = 0.85 V, V_{CC2} = 3.6 V, R_{L_Input} = 1.35 kΩ	C_L = 15 pF			15	ns
			C_L = 50 pF			45	
		V_{CC1} = 0.85 V, V_{CC2} = 5.5 V, R_{L_Input} = 1.35 kΩ	C_L = 15 pF			20	ns
			C_L = 50 pF			46	
		V_{CC1} = 1.65 V, V_{CC2} = 3.6 V, R_{L_Input} = 1.35 kΩ	C_L = 15 pF			8	ns
			C_L = 50 pF			20	
		V_{CC1} = 1.65 V, V_{CC2} = 5.5 V, R_{L_Input} = 1.35 kΩ	C_L = 15 pF			15	ns
			C_L = 50 pF			35	
		V_{CC1} = 3 V, V_{CC2} = 5.5 V, R_{L_Input} = 1.35 kΩ	C_L = 15 pF			2	ns
			C_L = 50 pF			5	

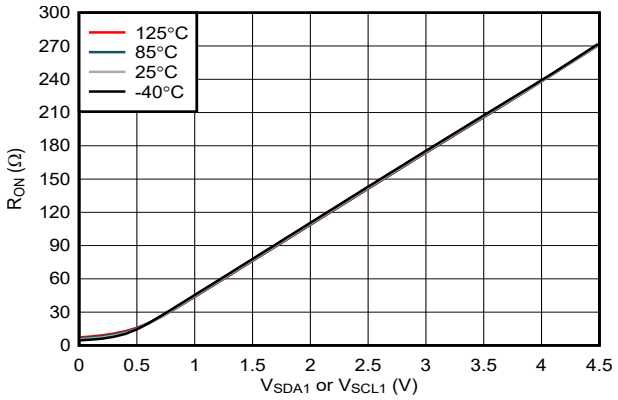
6.6 Switching Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{PHL}	High-to-low propagation delay(1)	V_{CC1} = 0.85 V, V_{CC2} = 1.98 V, R_{L_Input} = 1.35 kΩ	C_L = 15 pF			3	ns
			C_L = 50 pF			4	
		V_{CC1} = 0.85 V, V_{CC2} = 3.6 V, R_{L_Input} = 1.35 kΩ	C_L = 15 pF			3	ns
			C_L = 50 pF			5	
		V_{CC1} = 0.85 V, V_{CC2} = 5.5 V, R_{L_Input} = 1.35 kΩ	C_L = 15 pF			3	ns
			C_L = 50 pF			5	
		V_{CC1} = 1.65 V, V_{CC2} = 3.6 V, R_{L_Input} = 1.35 kΩ	C_L = 15 pF			2	ns
			C_L = 50 pF			3	
		V_{CC1} = 1.65 V, V_{CC2} = 5.5 V, R_{L_Input} = 1.35 kΩ	C_L = 15 pF			3	ns
			C_L = 50 pF			3	
		V_{CC1} = 3 V, V_{CC2} = 5.5 V, R_{L_Input} = 1.35 kΩ	C_L = 15 pF			1.5	ns
			C_L = 50 pF			2	

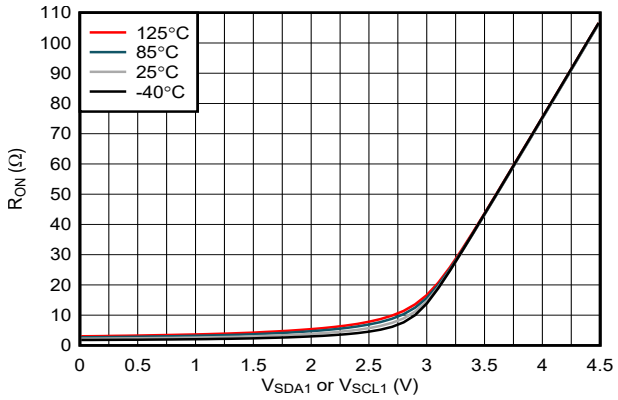
(1) Measured with an application propagation delay setup. See 図 7-3

6.7 Typical Characteristics



V_{EN} = 1.5 V I_I = 15 mA

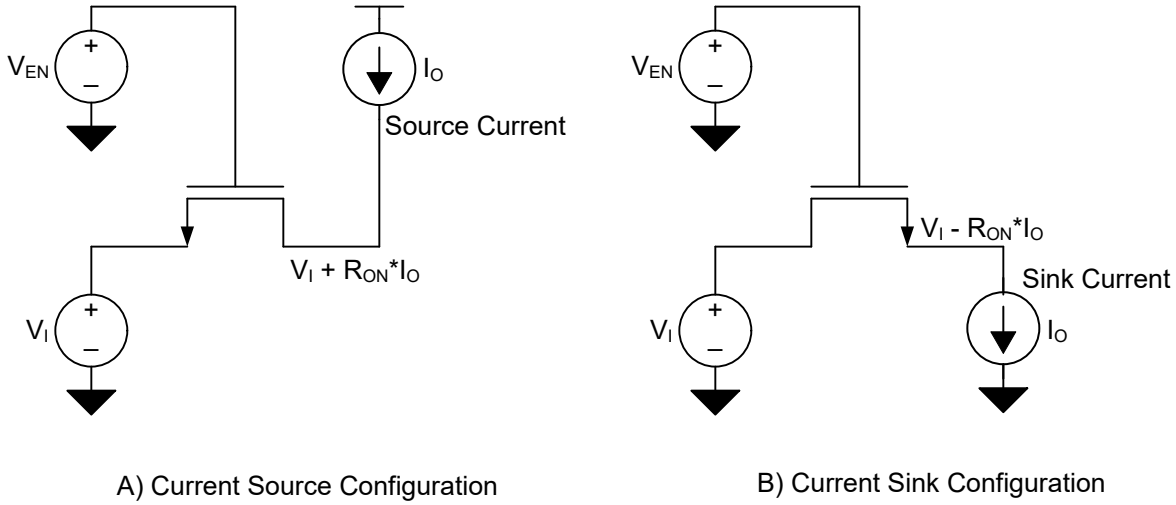
図 6-1. On-Resistance (R_{ON}) vs Input Voltage (V_{SDA1} or V_{SCL1})



V_{EN} = 4.5 V I_I = 15 mA

図 6-2. On-Resistance (R_{ON}) vs Input Voltage (V_{SDA1} or V_{SCL1})

7 Parameter Measurement Information



A) Current Source Configuration

B) Current Sink Configuration

図 7-1. Current Source and Current Sink Configurations for Direct R_{ON} Measurements

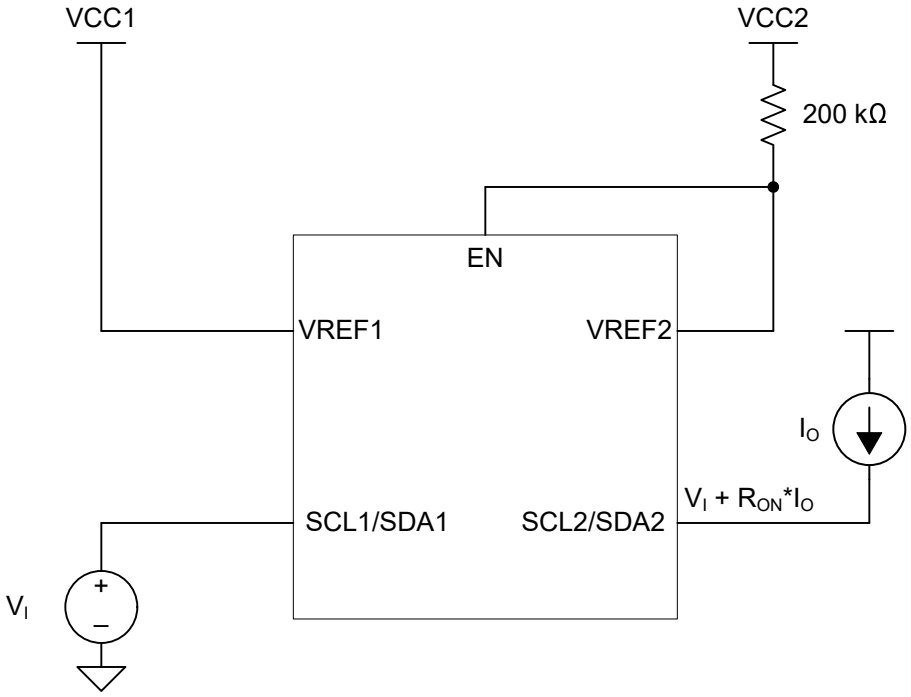


図 7-2. Application Setup for R_{ON} Delay

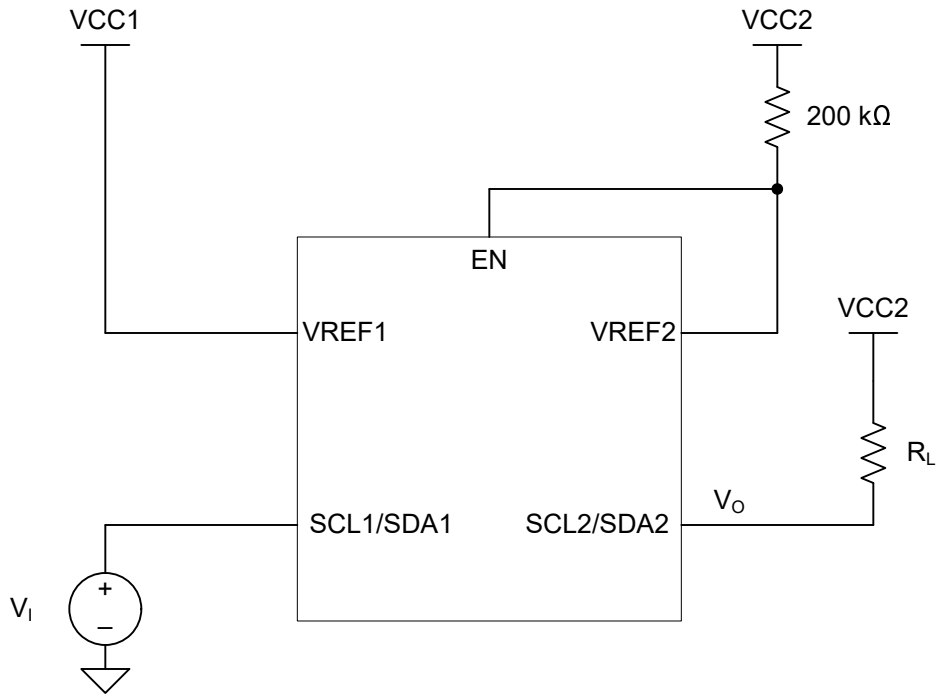
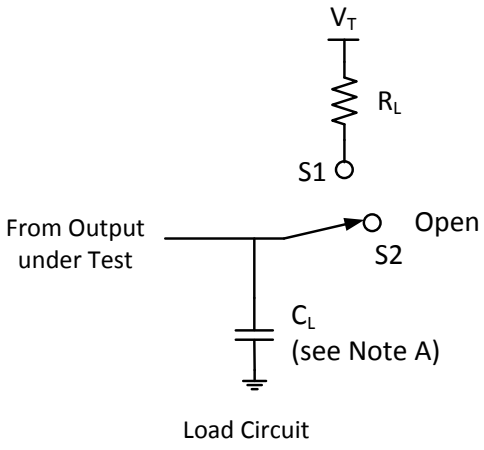
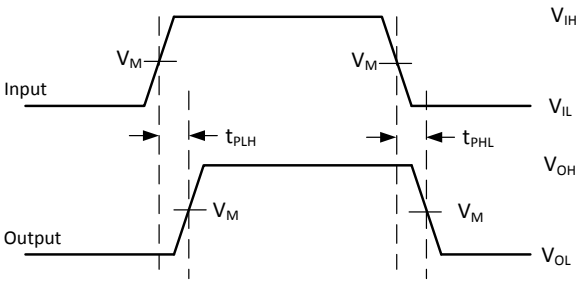


図 7-3. Application Setup for Propagation Delays Delay

USAGE	SWITCH
Translating up	S1
Translating down	S2





NOTES: A. C_L includes probe and jig capacitance
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω , t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

図 7-4. Load Circuit for Outputs

8 Detailed Description

8.1 Overview

The TCA39306 is a dual bidirectional voltage-level translator compatible with I^2C, SMBus, and I^3C with an enable (EN) input, and is operational from 0.9-V to 3.3-V V_{REF1} and 1.8-V to 5.5-V V_{REF2}.

The device allows bidirectional voltage translations between 0.85 V and 5 V, without the use of a direction pin. The low ON-state resistance (R_{ON}) of the switch allows connections to be made with minimal propagation delay. When EN is high, the translator switch is ON, and the SCL1 and SDA1 I/O are connected to the SCL2 and SDA2 I/O, respectively, allowing bidirectional data flow between ports. When EN is low, the translator switch is off, and a high-impedance state exists between ports.

In addition to voltage translation, the TCA39306 can be used to isolate a higher speed bus from a lower speed bus by controlling the EN pin to disconnect the slower bus during fast-mode communication.

In I^2C applications, the bus capacitance limit of 400 pF for Standard and Fast Modes, 550 pF for Fast Mode Plus restricts the number of devices and bus length. The capacitive load on both sides of the device must be taken into account when approximating the total load of the system, specifying the sum of both sides is under 400/550 pF.

Both the SDA and SCL channels of the device have the same electrical characteristics, and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete-transistor voltage-translation solutions, because the fabrication of the switch is symmetrical.

8.1.1 Definition of threshold voltage

This document references a threshold voltage denoted as V_{th}, which appears multiple times throughout this document when discussing the NFET between V_{REF1} and V_{REF2}. The value of V_{th} is approximately 0.6 V at room temperature.

8.1.2 Correct Device Set Up

In a normal set up shown in 図 8-1, the enable pin and V_{REF2} are shorted together and tied to a 200-kΩ resistor, and a reference voltage equal to V_{REF1} plus the FET threshold voltage is established. This reference voltage is used to help pass lows from one side to another more effectively while still separating the different pull up voltages on both sides.

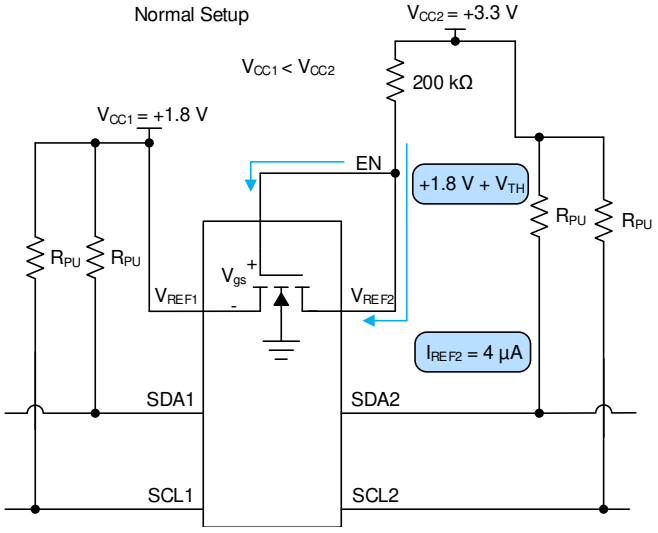


図 8-1. Normal Setup

Care should be taken to make sure V_{REF2} has an external resistor tied between it and V_{CC2}. If V_{REF2} is tied directly to the V_{CC2} rail without a resistor, then there is no external resistance from the V_{CC2} to V_{CC1} to limit the

current such as in 図 8-2. This effectively looks like a low impedance path for current to travel through and potentially break the pass FET if the current flowing through the pass FET is larger than the absolute maximum continuous channel current specified in the Absolute Maximum Ratings. The continuous channel current is larger with a higher voltage difference between V_{CC1} and V_{CC2}.

図 8-2 shows an improper set up. If V_{CC2} is larger than V_{CC1} but less than V_{th}, the impedance between V_{CC1} and V_{CC2} is high resulting in a low drain to source current, which does not cause damage to the device. Concern arises when V_{CC2} becomes larger than V_{CC1} by V_{th}. During this event, the NFET turns on and begin to conduct current. This current is dependent on the gate to source voltage and drain to source voltage.

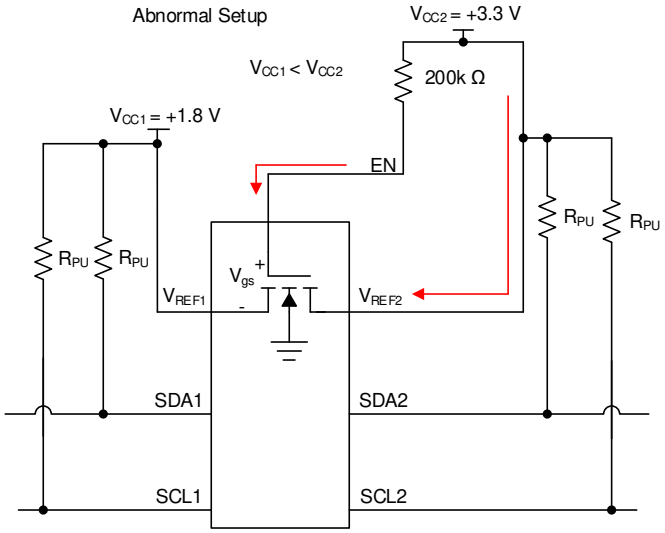


図 8-2. Abnormal Setup

8.1.3 Disconnecting a Responder from the Main Bus Using the EN Pin

TCA39306 can be used as a switch to disconnect one side of the device from the main bus, whether isolating I3C and I2C devices or different speed groups. This can be advantageous in multiple situations. One instance of this situation is if there are devices on the I2C bus which only supports fast mode (400 kHz) while other devices on the bus support fast mode plus (1 MHz). An example of this is displayed in 図 8-3.

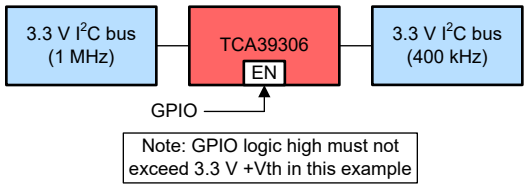


図 8-3. Example of an I2C bus with multiple supported frequencies

In this situation, if the controller is on the 1 MHz side then communicating at 1 MHz should not be attempted if TCA39306 were enabled. It needs to be disabled for the device to avoid possibly glitching state machines in devices which were designed to operate correctly at 400 kHz or slower. When the device is disabled, the controller can communicate with the 1 MHz devices without disturbing the 400 kHz bus. When the device is enabled, communication across both sides at 400 kHz is acceptable.

8.1.4 Supporting Remote Board Insertion to Backplane with TCA39306

Another situation where TCA39306 is advantageous when using its enable feature is when a remote board with I2C lines needs to be attached to a main board (backplane) with an I^2C bus such as in 図 8-4. If connecting a remote board to a backplane is not done properly, the connection could result in data corruption during a transaction or the insertion could generate an unintended pulse on the SCL line. Which could glitch an I^2C device state machine causing the I^2C bus to get stuck.

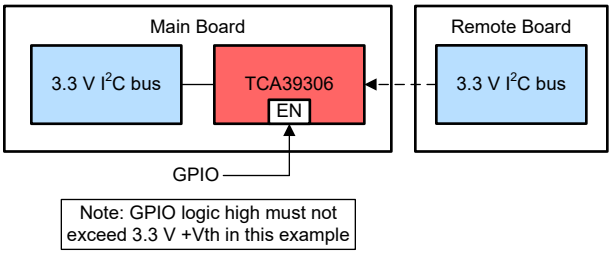


図 8-4. An example of connecting a remote board to a main board (backplane)

TCA39306 can be used to support this application because it can be disabled while making the connection. Then it is enabled once the remote board is powered on and the buses on both sides are IDLE.

8.1.5 Switch Configuration

TCA39306 has the capability of being used with its V_{REF1} voltage equal to V_{REF2}. This essentially turns the device from a translator to a device which can be used as a switch, and in some situations this can be useful. The switch configuration is shown in 図 8-5 and translation mode is shown in 図 8-6.

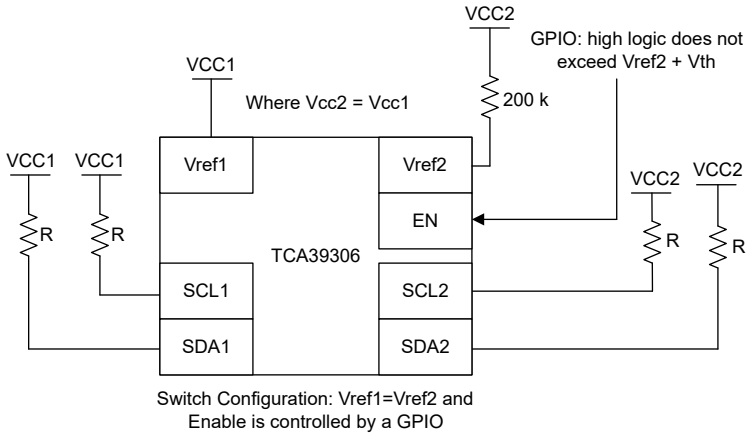


図 8-5. Switch Configuration

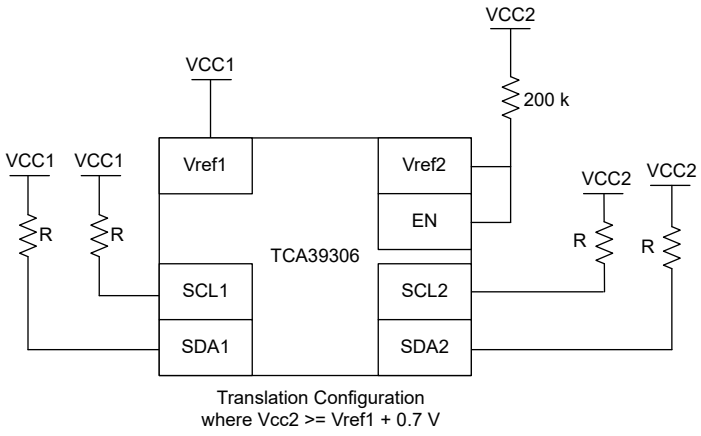


図 8-6. Translation Configuration

When TCA39306 is in the switch configuration (V_{REF1} = V_{REF2}), the propagation delays are different compared to the translator configuration. Taking a look at the propagation delays, if the pull up resistance and capacitance on both sides of the bus are equal, then in switch mode the device has the same propagation delay from side one to two and side two to one. The propagation delays become lower when V_{CC1}/V_{CC2} is larger. For example, the propagation delay at 1.8 V is longer than at 5 V in the switching configuration. When the device is in translation

mode, side one propagate lows to side two faster than side two can propagate lows to side 1. This time difference becomes larger the larger the difference between V_{CC2} and V_{CC1} becomes.

8.1.6 Controller on Side 1 or Side 2 of Device

I2C and SMBus are bidirectional protocol meaning devices on the bus can both transmit and receive data. TCA39306 was designed to allow for signals to be able to be transmitted from either side, thus allowing for the controller to be able to place on either side of the device. 図 8-7 shows the controller on side two as opposed to the diagram on page 1 of this data sheet.

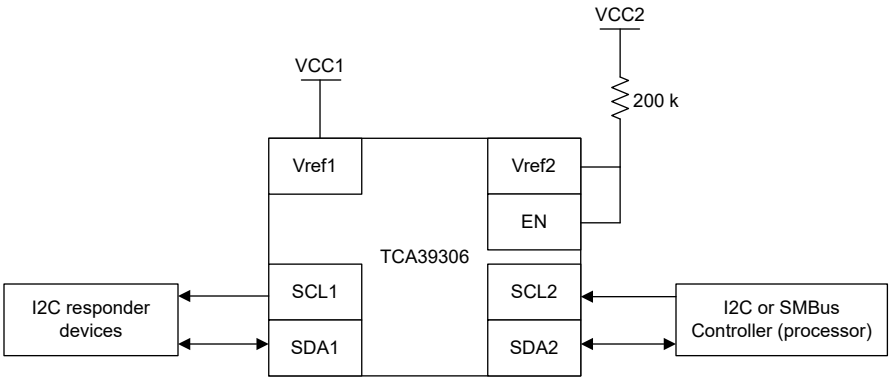


図 8-7. Controller on side 2

8.1.7 LDO and TCA39306 Concerns

The V_{REF1} pin can be supplied by a low-dropout regulator (LDO), but in some cases the LDO may lose its regulation because of the bias current from V_{REF2} to V_{REF1}. If the LDO cannot sink the bias current, then the current has no other paths to ground and instead charges up the capacitance on the V_{REF1} node (both external and parasitic). This results in an increase in voltage on the V_{REF1} node. If no other paths for current to flow are established (such as back biasing of body diodes or clamping diodes through other devices on the V_{REF1} node), then the V_{REF1} voltage ends up stabilizing when V_{gs} of the pass FET is equal to V_{th}. This means V_{REF1} node voltage is V_{CC2} - V_{th}. Note that any secondary or primaries running off of the LDO now see the V_{CC2} - V_{th} voltage which may cause damage to those secondary or primaries if they are not rated to handle the increased voltage.

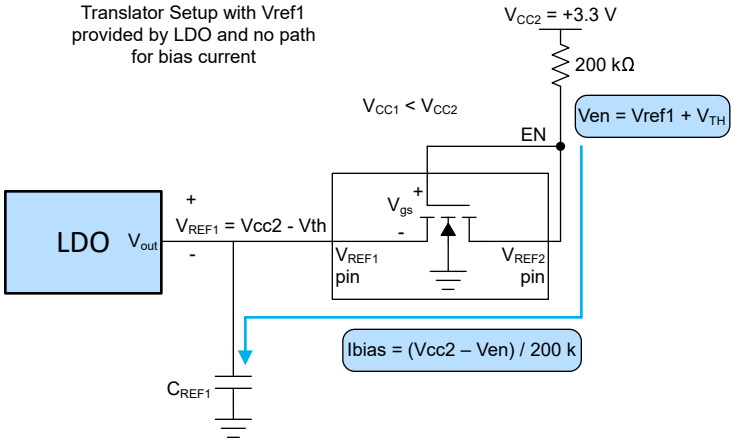


図 8-8. Example of no leakage current path when using LDO

To make sure the LDO does not lose regulation due to the bias current of TCA39306, a weak pull down resistor can be placed on V_{REF1} to ground to provide a path for the bias current to travel. The recommended pull down resistor is calculated by 式 4 where 0.75 gives about 25% margin for error incase bias current increases during operation.

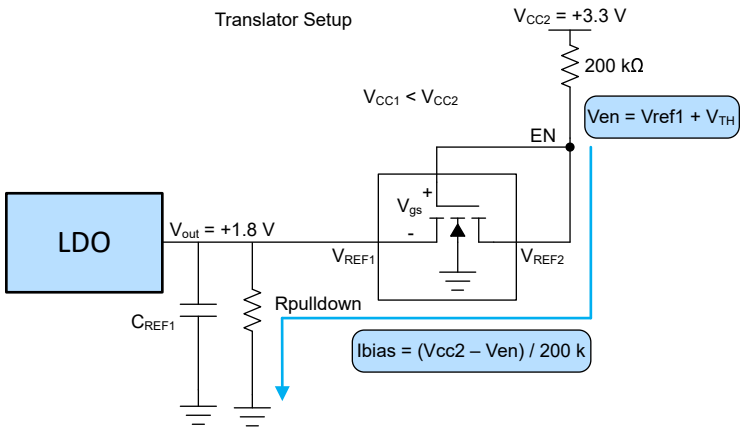


図 8-9. Example with Leakage current path when using an LDO

$$V_{en} = V_{REF1} + V_{th} \quad (1)$$

where

- V_{th} is approximately 0.6 V

$$I_{bias} = (V_{CC2} - V_{en})/200\ k \quad (2)$$

$$R_{pulldown} = V_{OUT}/I_{bias} \quad (3)$$

$$\text{Recommended } R_{pulldown} = R_{pulldown} \times 0.75 \quad (4)$$

8.1.8 Current Limiting Resistance on V_{REF2}

The resistor is used to limit the current between V_{REF2} and V_{REF1} (denoted as R_{CC}) and helps to establish the reference voltage on the enable pin. The 200k resistor can be changed to a lower value; however, the bias current proportionally increases as the resistor decreases.

$$I_{bias} = (V_{CC2} - V_{en})/R_{CC} : V_{en} = V_{REF1} + V_{th} \quad (5)$$

where

- V_{th} is approximately 0.6 V

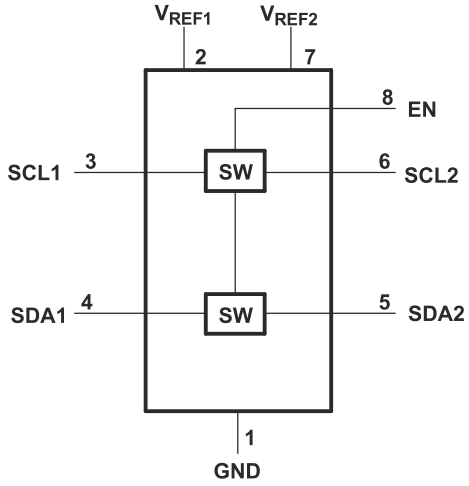
Keep in mind R_{CC} should not be sized low enough that I_{CC} exceeds the absolute maximum continuous channel current specified in the *Absolute Maximum Ratings* which is described in 式 6.

$$R_{CC}(min) \geq (V_{CC2} - V_{en})/0.128 : V_{en} = V_{REF1} + V_{th} \quad (6)$$

where

- V_{th} is approximately 0.6 V

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Enable (EN) Pin

The device is a double-pole, single-throw switch in which the gate of the transistors is controlled by the voltage on the EN pin. In 図 9-1, the device is always enabled when power is applied to V_{REF2}. In 図 9-2, the device is enabled when a control signal from a processor is in a logic-high state.

8.3.2 Voltage Translation

The primary feature of the device is translating voltage from an I^2C bus referenced to V_{REF1} up to an I^2C bus referenced to V_{DPU}, to which V_{REF2} is connected through a 200-kΩ pullup resistor. Translation on a standard, open-drain I^2C bus is achieved by simply connecting pullup resistors from SCL1 and SDA1 to V_{REF1} and connecting pullup resistors from SCL2 and SDA2 to V_{DPU}. Information on sizing the pullup resistors can be found in the *Sizing Pullup Resistors* section.

8.4 Device Functional Modes

INPUT EN(1)	TRANSLATOR FUNCTION
H	Logic Lows are propagated from one side to the other, Logic Highs blocked (independent pull up resistors passively drive the line high)
L	Disconnect

(1) The SCL switch conducts if EN is ≥ 0.6 V higher than SCL1 or SCL2. The same is true of SDA.

9 Application and Implementation

注

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9.1 Application Information

9.1.1 General Applications of I^2C

As with the standard I^2C system, pullup resistors are required to provide the logic-high levels on the translator bus. The size of these pullup resistors depends on the system, but each side of the repeater must have a pullup resistor. The device is designed to work with standard-mode and fast-mode I^2C devices in addition to SMBus devices. Standard-mode I^2C devices only specify 3 mA in a generic I^2C system where standard-mode devices and multiple controllers are possible. Under certain conditions, high termination currents can be used. When the SDA1 or SDA2 port is low, the clamp is in the ON state, and a low-resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is high, the voltage on the SDA1 port is limited to the voltage set by V_{REF1}. When the SDA1 port is high, the SDA2 port is pulled to the pullup supply voltage of the drain (V_{DPU}) by the pullup resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control. The SCL1-SCL2 channel also functions in the same way as the SDA1-SDA2 channel.

9.2 Typical Application

図 9-1 and 図 9-2 show how these pullup resistors are connected in a typical application, as well as two options for connecting the EN pin.

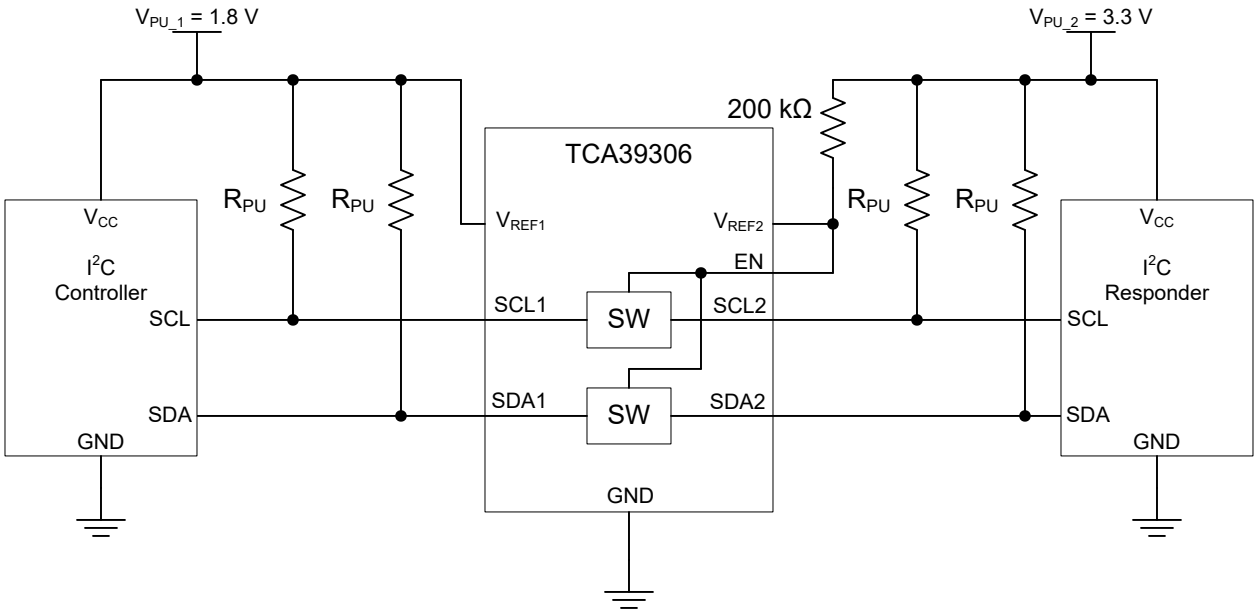


図 9-1. Typical Application Circuit (Switch Always Enabled)

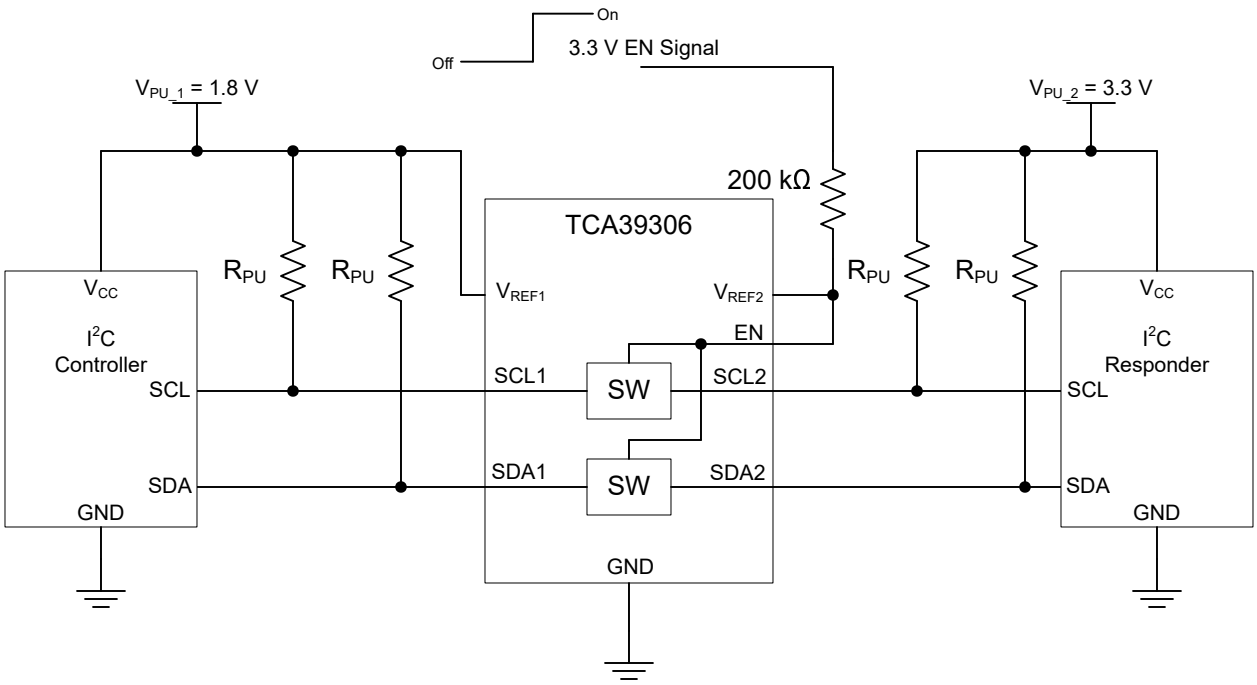


図 9-2. Typical Application Circuit (Switch Enable Control)

9.2.1 Design Requirements

		MIN	TYP(1)	MAX	UNIT
V_{REF2}	Reference voltage	V_{REF1} + 0.6	2.1	5	V
EN	Enable input voltage	V_{REF1} + 0.6	2.1	5	V
V_{REF1}	Reference voltage	0.9	1.5	4.4	V
I_{PASS}	Pass switch current		6		mA
I_{REF}	Reference-transistor current		5		µA

(1) All typical values are at T_A = 25°C.

9.2.2 Detailed Design Procedure

9.2.2.1 Bidirectional Voltage Translation

For the bidirectional clamping configuration (higher voltage to lower voltage or lower voltage to higher voltage), the EN input must be connected to V_{REF2} and both pins pulled to high-side V_{DPU} through a pullup resistor (typically 200 kΩ). This allows V_{REF2} to regulate the EN input. A 100-pF filter capacitor connected to V_{REF2} is recommended. The I^2C bus controller output can be push-pull or open-drain (pullup resistors may be required) and the I^2C bus device output can be open-drain (pullup resistors are required to pull the SCL2 and SDA2 outputs to V_{DPU}). However, if either output is push-pull, data must be unidirectional or the outputs must be 3-state capable and be controlled by some direction-control mechanism to prevent high-to-low contentions in either direction. If both outputs are open-drain, no direction control is needed.

9.2.2.2 Sizing Pullup Resistors

To get an estimate for the range of values that can be used for the pullup resistor, please refer to the application note SLVA689. 図 9-3 and 図 9-4 respectively show the maximum and minimum pullup resistance allowable by the I^2C specification for standard-mode (100 kHz) and fast-mode (400 kHz) operation.

9.2.2.3 Bandwidth

The maximum frequency of the device depends on the application. The device can operate at speeds of > 100 MHz given the correct conditions. The maximum frequency is dependent upon the loading of the application.

However, this is an analog type of measurement. For digital applications, the signal should not degrade up to the fifth harmonic of the digital signal. The frequency bandwidth should be at least five times the maximum digital clock rate. This component of the signal is important in determining the overall shape of the digital signal. In the case of the device, digital clock frequency of >100 MHz can be achieved.

The device does not provide any drive capability like the TCA9517 or other buffered translators. Therefore, higher-frequency applications require higher drive strength from the host side. No pullup resistor is needed on the host side (3.3 V) if the device is being driven by standard CMOS push-pull output driver. Ideally, it is best to minimize the trace length from device on the sink side (1.8 V) to minimize signal degradation.

You can then use a simple formula to compute the maximum *practical* frequency component or the *knee* frequency (f_{knee}). All fast edges have an infinite spectrum of frequency components. However, there is an inflection (or *knee*) in the frequency spectrum of fast edges where frequency components higher than f_{knee} are insignificant in determining the shape of the signal.

To calculate f_{knee}:

$$f_{knee} = 0.5 / RT (10\%–90\%) \quad (7)$$

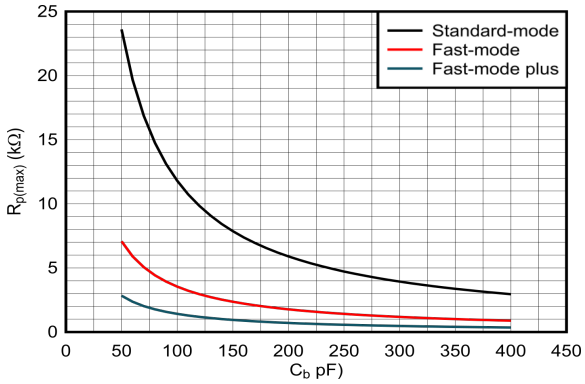
$$f_{knee} = 0.4 / RT (20\%–80\%) \quad (8)$$

For signals with rise-time characteristics based on 10- to 90-percent thresholds, f_{knee} is equal to 0.5 divided by the rise time of the signal. For signals with rise-time characteristics based on 20- to 80-percent thresholds, which is very common in many current device specifications, f_{knee} is equal to 0.4 divided by the rise time of the signal.

Some guidelines to follow that help maximize the performance of the device:

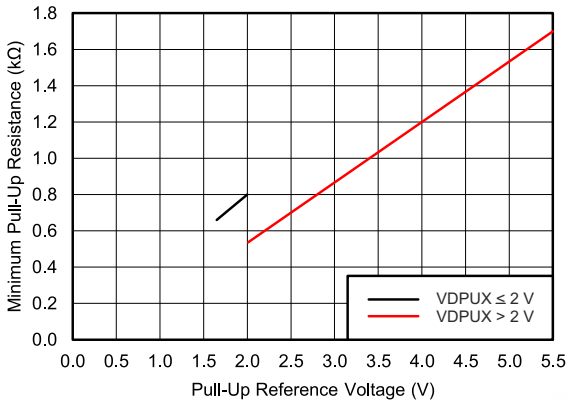
- Keep trace length to a minimum by placing the device close to the I^2C output of the processor.
- The trace length should be less than half the time of flight to reduce ringing and line reflections or non-monotonic behavior in the switching region.
- To reduce overshoots, a pullup resistor can be added on the 1.8 V side; be aware that a slower fall time is to be expected.

9.2.3 Application Curve



Standard mode	Fast mode	Fast mode plus
(f_{SCL} = 100 kHz, t_r = 1 µs)	(f_{SCL} = 400 kHz, t_r = 300 ns)	(f_{SCL} = 1000 kHz, t_r = 120 ns)

図 9-3. Maximum Pullup Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2 x V_{DPUX} , I_{OL} = 2 mA when V_{DPUX} ≤ 2 V
V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{DPUX} > 2 V

図 9-4. Minimum Pullup Resistance ($R_{p(min)}$) vs Pullup Reference Voltage (V_{DPUX})

9.3 Systems Examples: I3C Usage Considerations

The TCA39306 has bandwidth to support the high speeds needed for I3C, but there are special considerations which are required. Since I3C uses both push-pull and open-drain, it may not be possible to support all I3C applications with a FET-based translator.

9.3.1 I3C Bus Switching

Bus switching is when the bus path is enabled or disabled, but does not translate the bus voltage. External pull-up resistors are not needed for I3C, because the controller enables or disables the pull-up resistor on the SDA line. This presents a unique challenge for FET-based translators, like the TCA39306, because they rely on a pull-up resistor to pull the output side of the switch all the way to supply. For the switching use case, there is no translation, but the enable voltage must be high enough for the switch to stay on for the entire voltage range of the bus (0 V to bus voltage).

R_{ON} must be low enough for the full push-pull voltage range. The EN voltage must be at least 1 V_t (~0.6 V) above the maximum desired pass-voltage. This comes out to $V_{EN} \geq V_{BUS}$ + 0.6 V. Since the switch enable voltage is being directly controlled, the V_{REF1} and V_{REF2} pins are not needed, and can be shorted to ground to improve power consumption.

It is possible to control the EN pin with a voltage equal to V_{BUS}, but external pull-up resistors on the downstream side are a requirement to ensure the bus is pulled entirely to V_{BUS}.

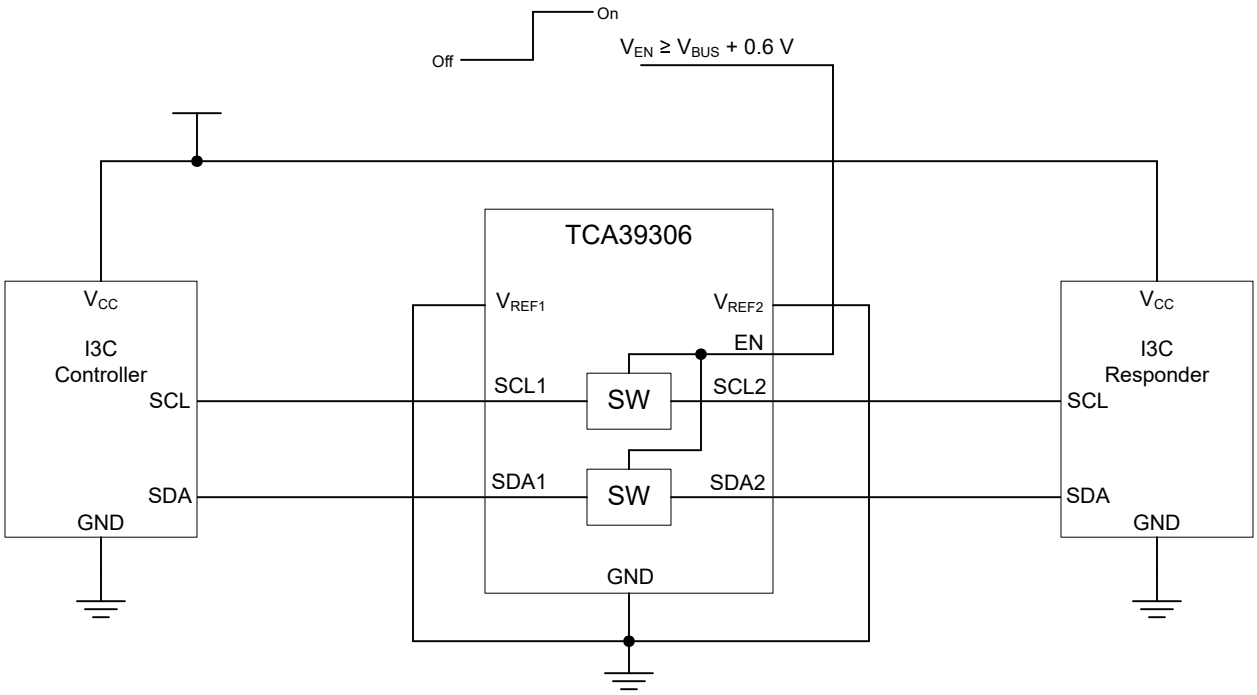


図 9-5. I3C Bus Switching Application (Without Pull-up Resistors)

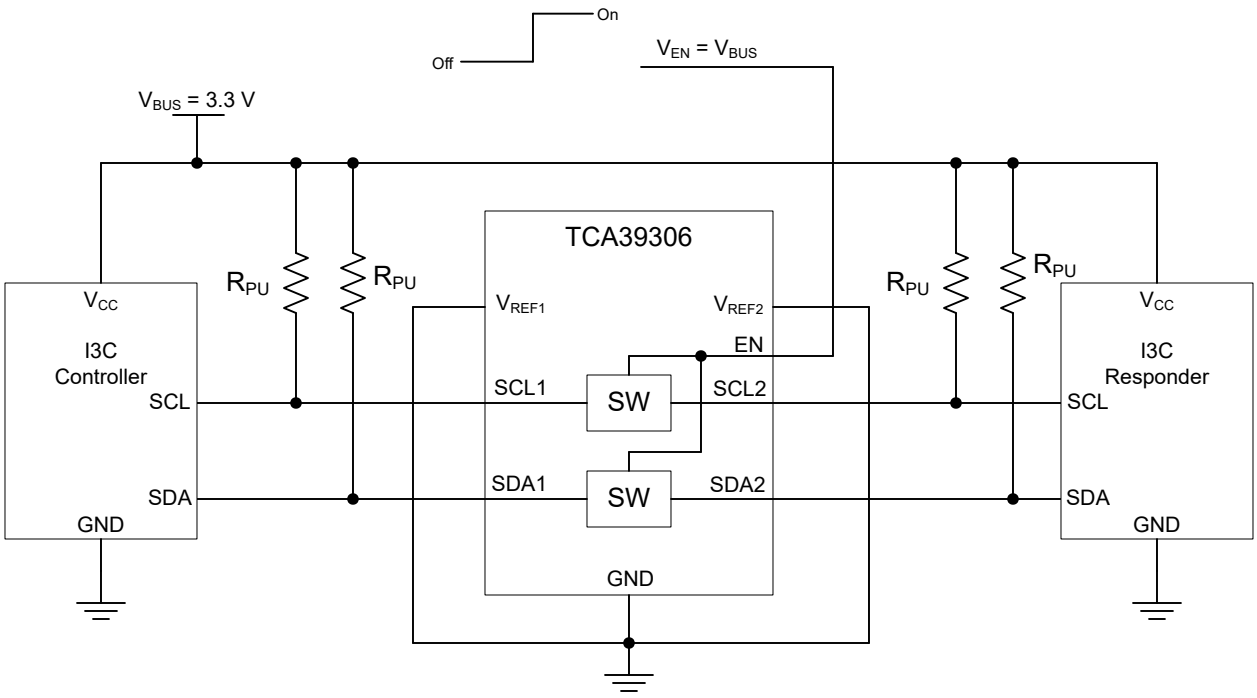


図 9-6. I3C Bus Switching Application (With Pull-up Resistors)

9.3.2 I3C Bus Voltage Translation

Bus voltage translation is when the bus voltage is translated up or down. This presents a unique challenge with I3C for FET-based translators, like the TCA39306, because they rely on a pull-up resistor to translate the voltage up from the low-voltage side. The pull-up resistor selected must be strong enough to meet the timing requirements (based on bus capacitance and translation voltages), but not so strong to violate the V_{IL} requirements of the I3C devices.

The pull-up resistors are needed on both sides. The reason for this is that with the normal translation setup, the switch is "on" when either side's bus voltage drops to roughly V_{PU_1}. This means that the pull-up resistors are required to pull the bus voltage on the high-voltage side from V_{PU_1} to V_{PU_2}. When the device on the high-voltage side is controlling the bus, the switch will turn off at V_{PU_1}. The pull-up resistors on the low-voltage side are used to bleed off any additional current that might "leak" through the switch.

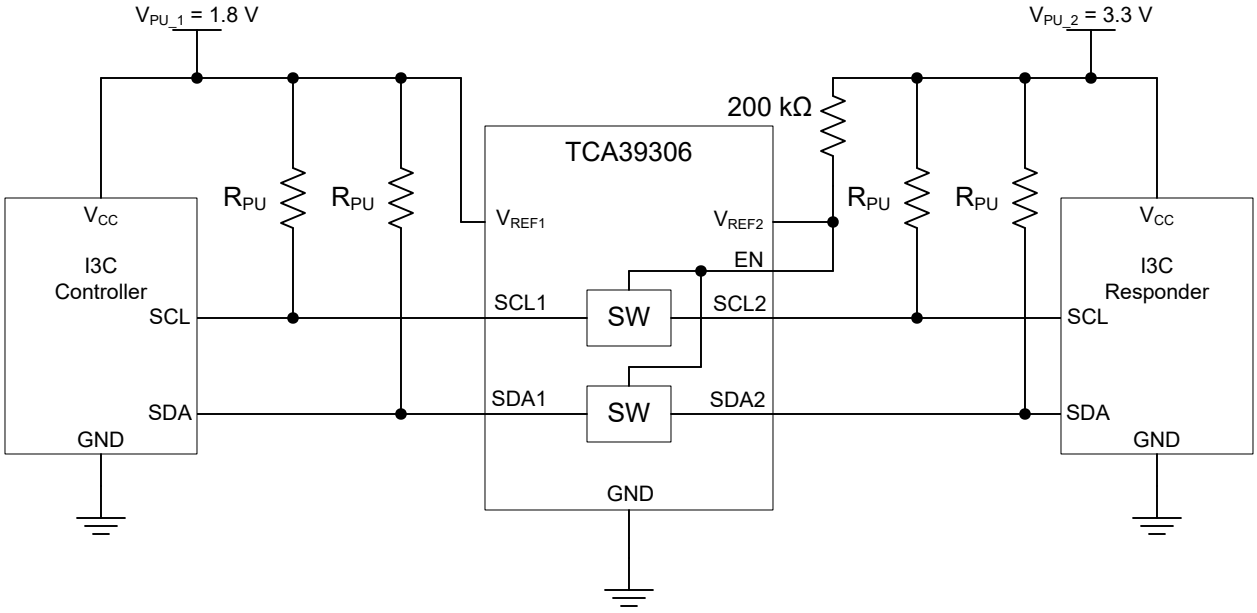


図 9-7. I3C Bus Translation

9.4 Power Supply Recommendations

For supplying power to the device, the V_{REF1} pin can be connected directly to a power supply. The V_{REF2} pin must be connected to the V_{DPU} power supply through a 200-kΩ resistor. Failure to have a high-impedance resistor between V_{REF2} and V_{DPU} results in excessive current draw and unreliable device operation. It is also worth noting, that in order to support voltage translation, the device must have the EN and VREF2 pins shorted and then pulled up to V_{DPU} through a high-impedance resistor.

9.5 Layout

9.5.1 Layout Guidelines

For printed-circuit board (PCB) layout of the device, common PCB layout practices should be followed, but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other on leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. The 100-pF filter capacitor should be placed as close to V_{REF2} as possible. A larger decoupling capacitor can also be used, but a longer time constant of two capacitors and the 200-kΩ resistor results in longer turnon and turnoff times for the TCA39306 device. These best practices are shown in 図 9-8.

For the layout example provided in 図 9-8, it would be possible to fabricate a PCB with only two layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a four-layer board is preferable for boards with higher-density signal routing. On a four-layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface-mount component pad, which must attach to V_{CC} or GND, and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace must be routed to the opposite side of the board, but this technique is not demonstrated in 図 9-8.

9.5.2 Layout Example

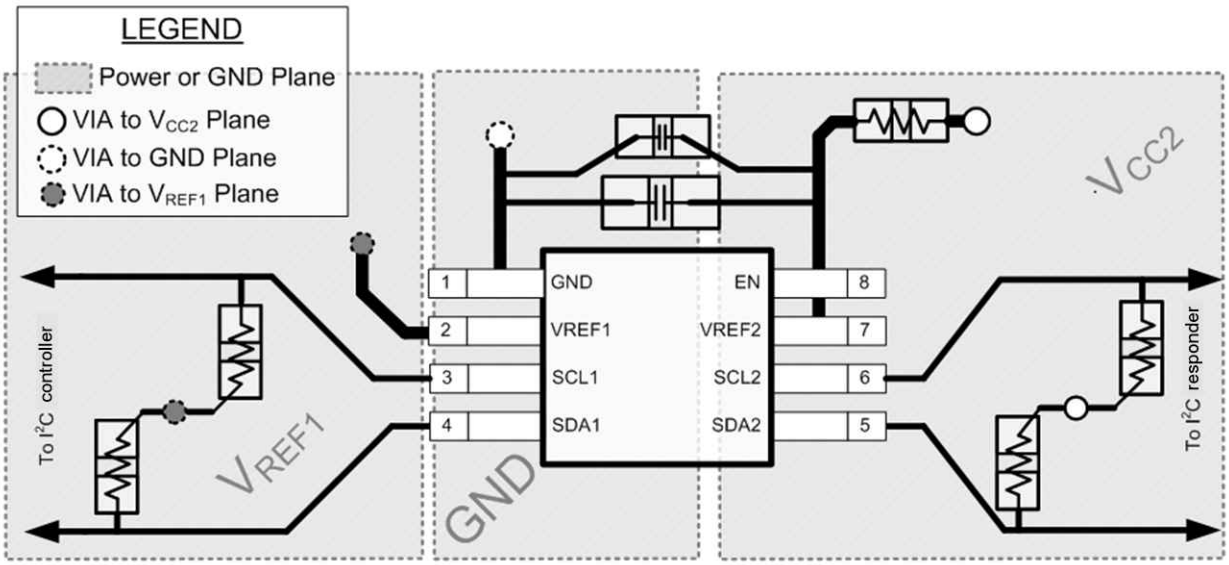


図 9-8. Layout Example

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

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10.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA39306DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	(2GPT, 2GVI)	Samples
TCA39306DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	2M9H	Samples
TCA39306DTMR	ACTIVE	X2SON	DTM	8	5000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1IH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TCA39306 :

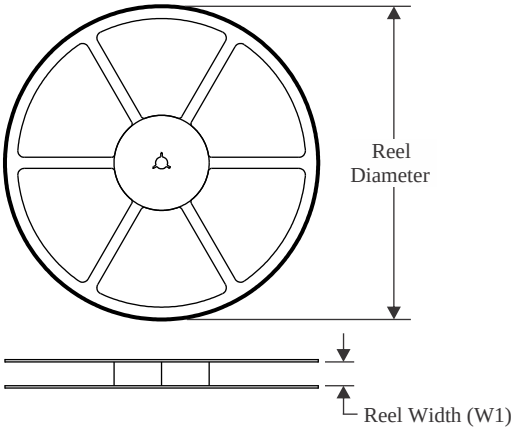
- Automotive : TCA39306-Q1

NOTE: Qualified Version Definitions:

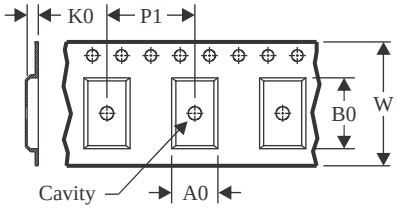
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

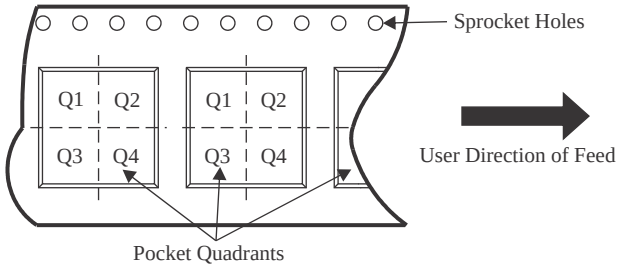


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

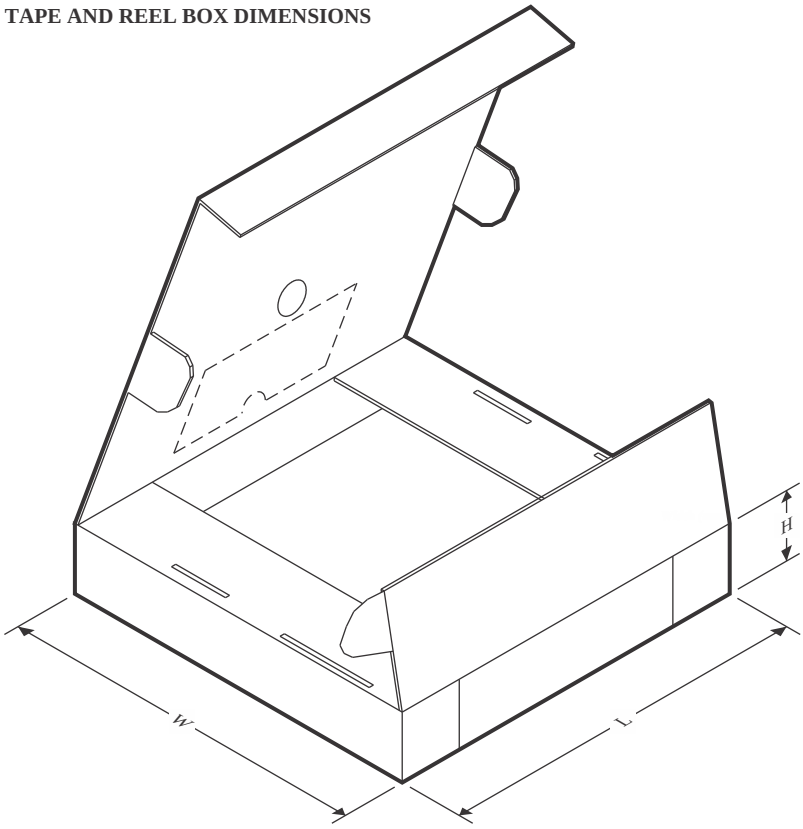
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA39306DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
TCA39306DTMR	X2SON	DTM	8	5000	178.0	8.4	0.93	1.49	0.43	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

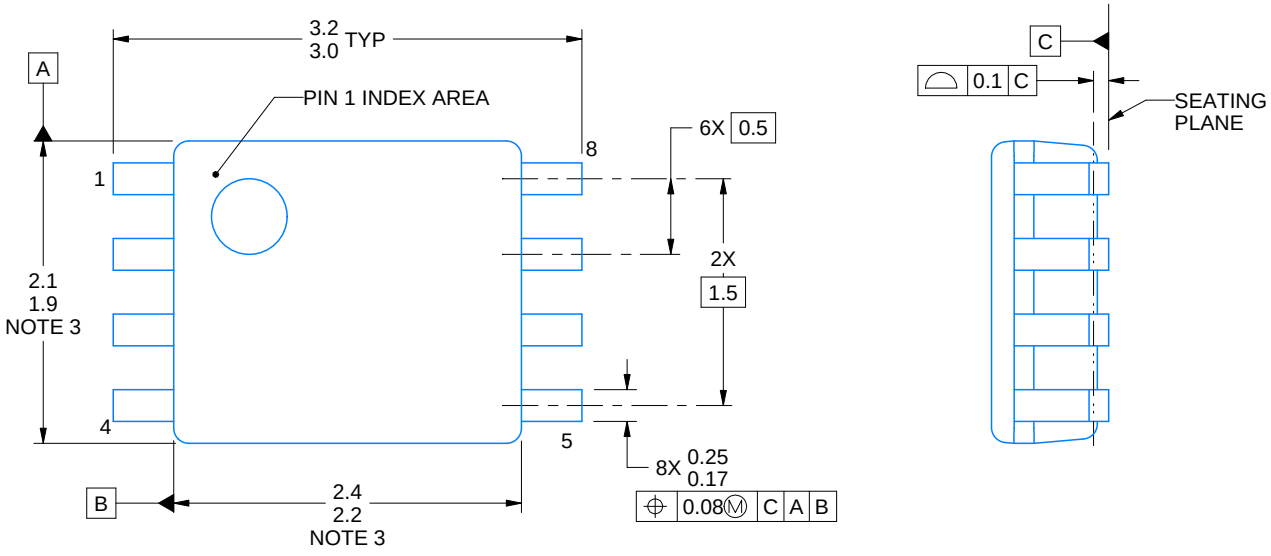
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA39306DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
TCA39306DTMR	X2SON	DTM	8	5000	205.0	200.0	33.0

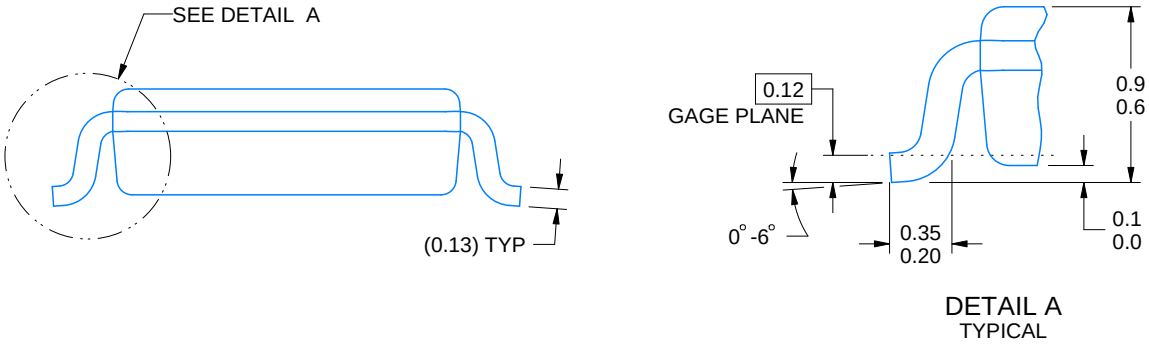
DCU0008A

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

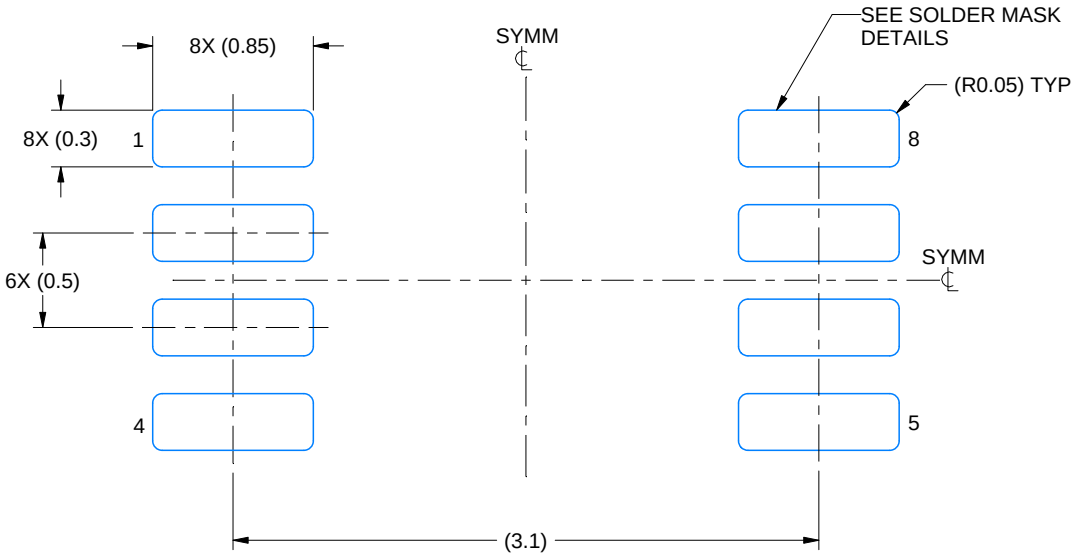




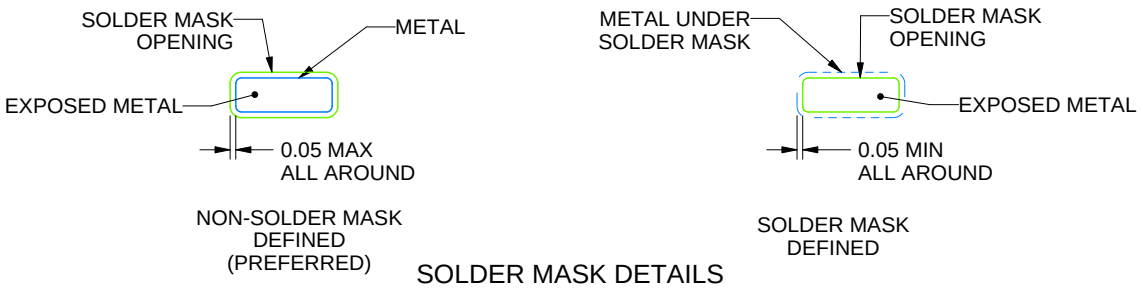
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

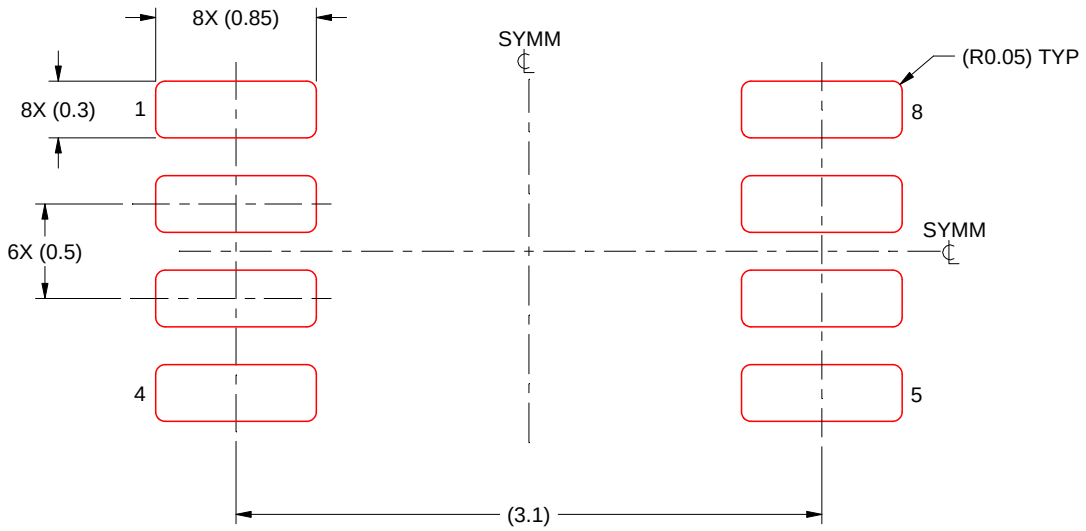


SOLDER MASK DETAILS

4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

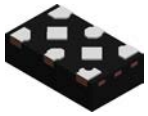


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

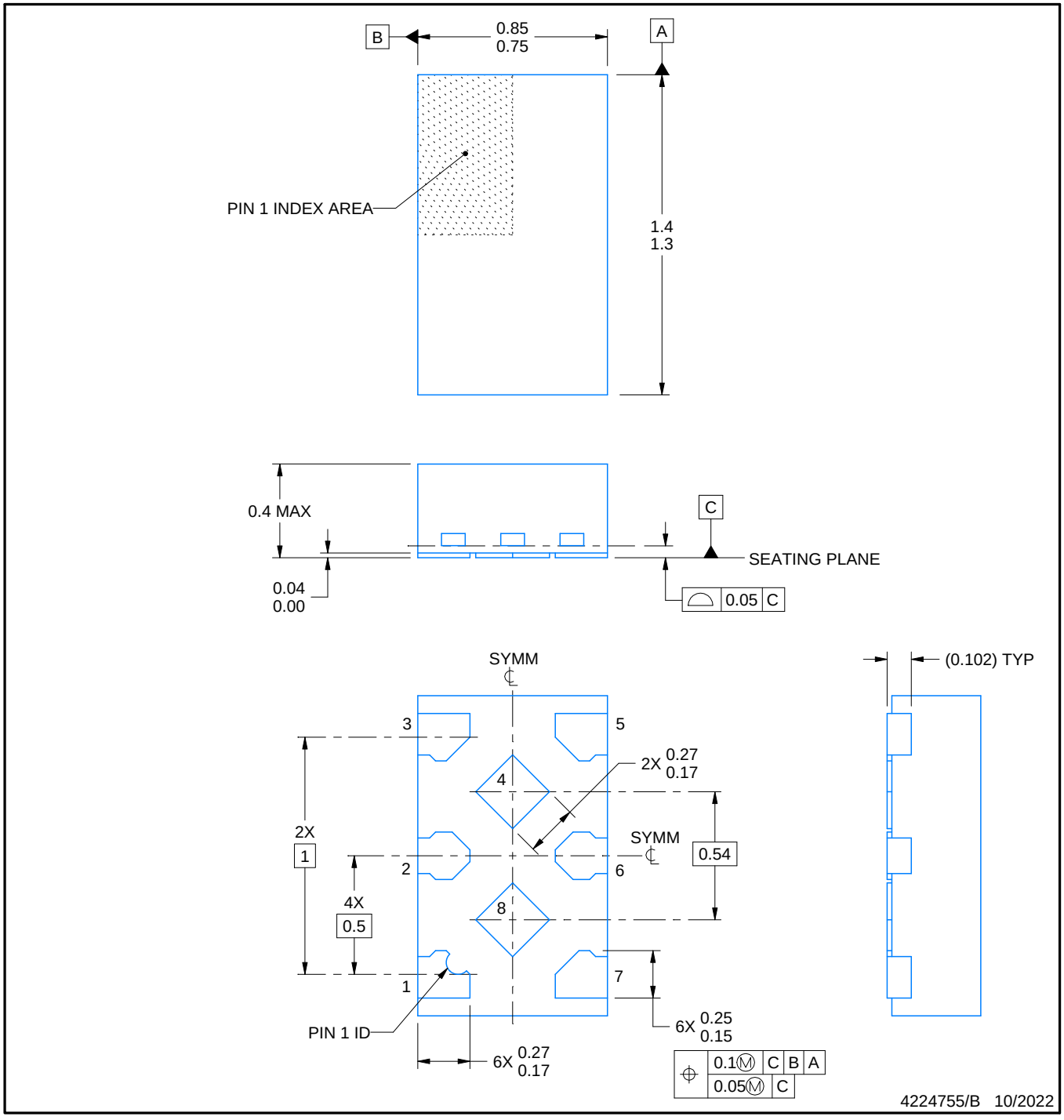


PACKAGE OUTLINE

DTM0008A

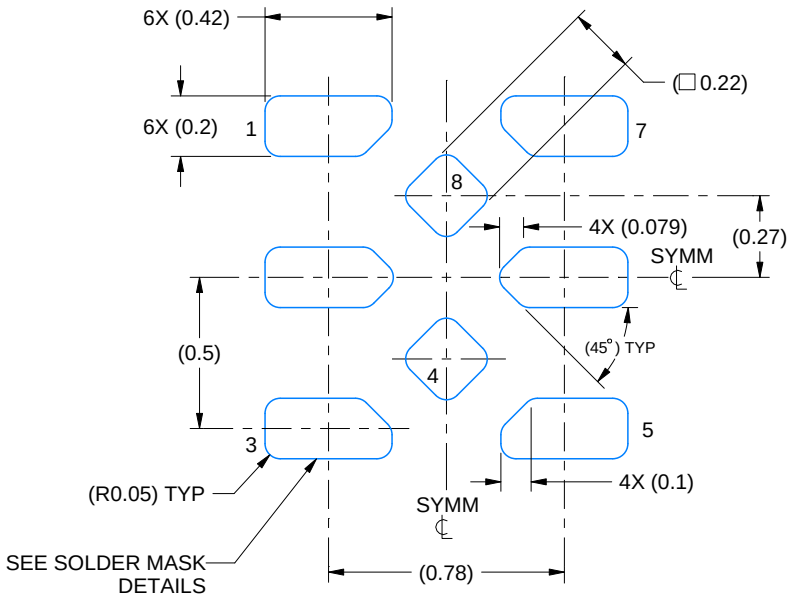
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad(s) must be soldered to the printed circuit board for thermal and mechanical performance.



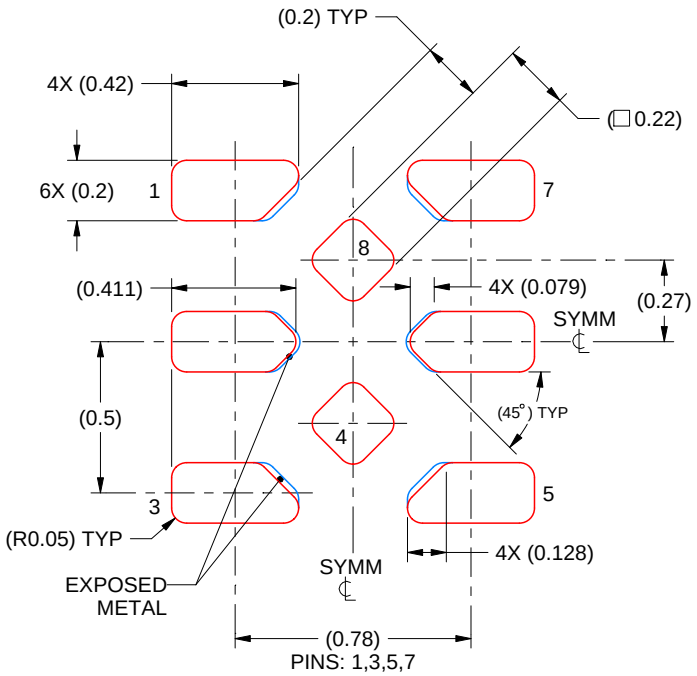
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:40X

SOLDER MASK DETAILS

4224755/B 10/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE

BASED ON 0.075 mm THICK STENCIL

SCALE: 40X

4224755/B 10/2022

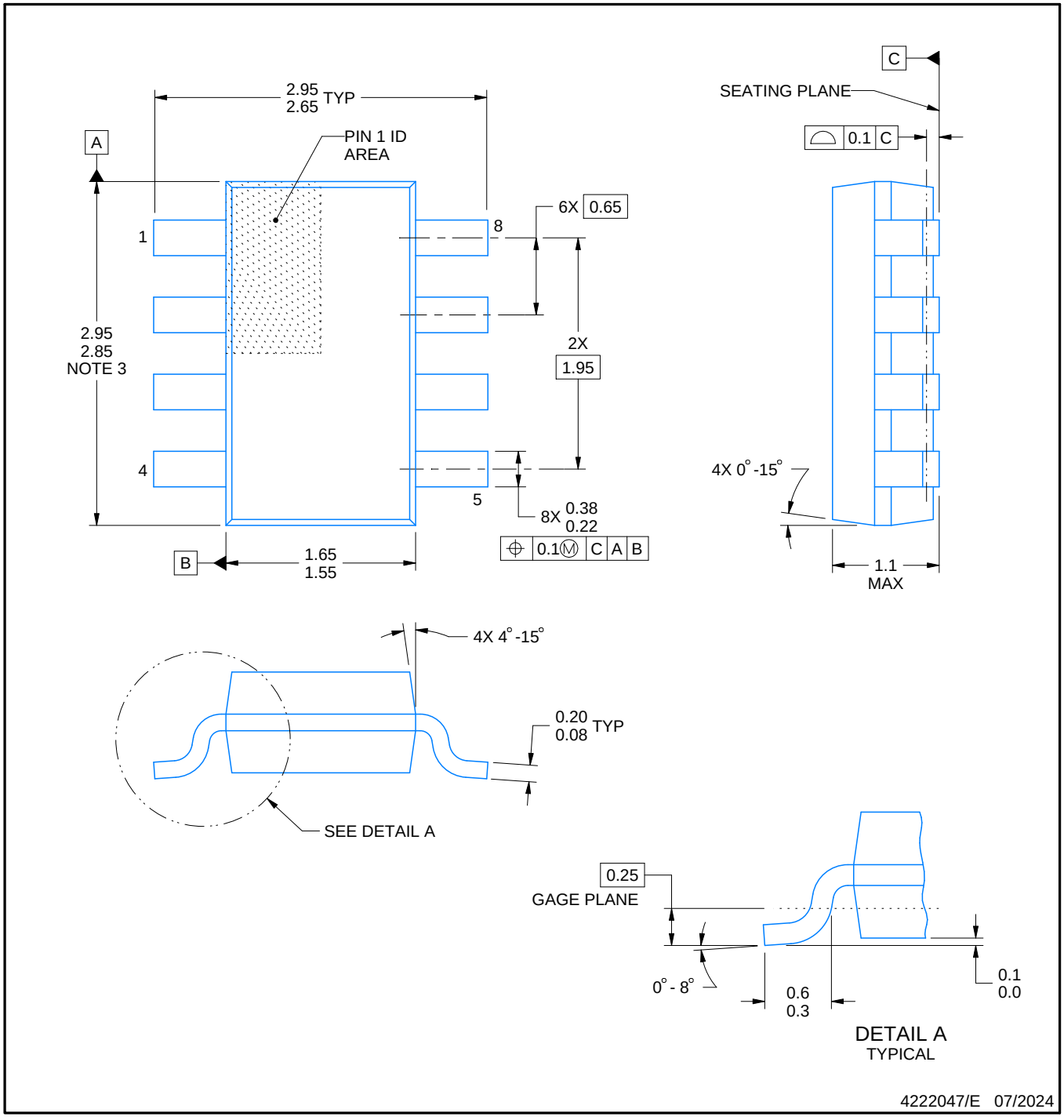
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DDF0008A

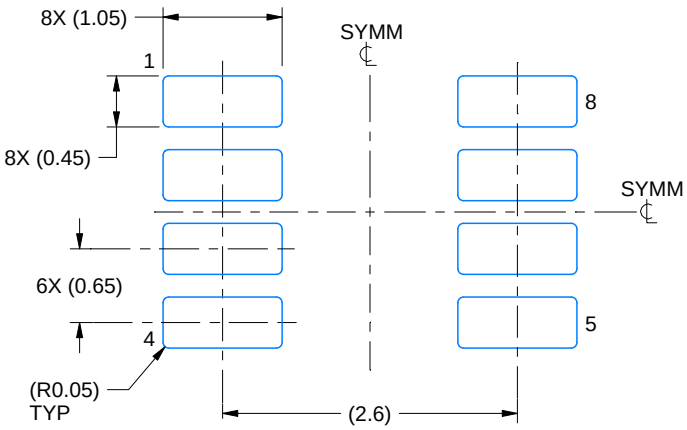
SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

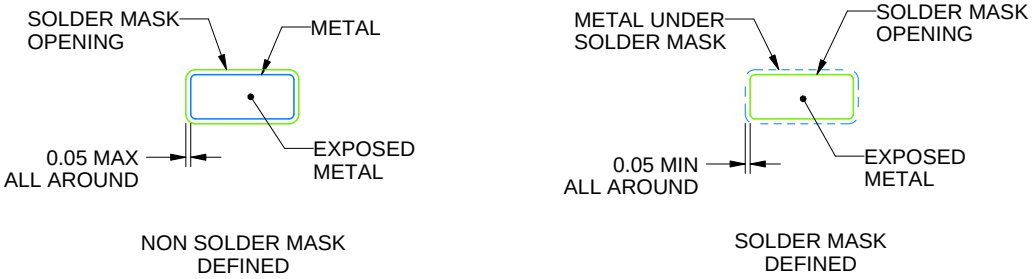


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

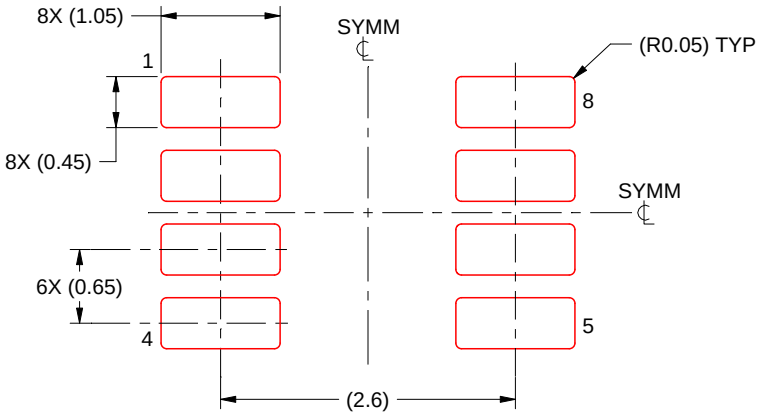
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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