参考資料

ADC08DJ5200RF
JAJSKZ0A – AUGUST 2021 – REVISED MAY 2022

ADC08DJ5200RF 10.4GSPS シングル・チャネルまたは 5.2GSPS デュアル・チャネル、8 ビット、RF サンプリング A/D コンバータ (ADC)

1 特長

- ADC コア：
  - 8 ビット分解能
  - シングル・チャネル・モードで最大 10.4GSPS
  - デュアル・チャネル・モードで最大 5.2GSPS
- 性能仕様
  - ノイズ・フロア (-20dBFS、$V_{FS} = 1V_{PP-DIFF}$)：
    - デュアル・チャネルモード：-143.4dBFS/Hz
    - シングル・チャネルモード：-146.2dBFS/Hz
  - ENOB (デュアル・チャネル、F_{IN} = 2.4GHz、標準値)：7.8 ビット
- バッファ付きアナログ入力、V_{CMI} = 0V：
  - アナログ入力帯域幅 (-3dB)：8.1GHz
  - 使用可能な入力周波数範囲：> 10GHz
  - フルスケール入力電圧 (V_{FS}、デフォルト)：0.8V_{pp}
- ノイズなしのアパーチャ遅延 (t_{AD}) 調整：
  - 高精度サンプリング制御：19fs ステップ
  - 同期およびインターリーブ動作を簡素化
  - 遅延は温度および電圧に対して不変
- 使いやすい同期機能：
  - SYSREF タイミングの自動較正
  - サンプル・マーキング用のタイムスタンプ
- JESD204C シリアル・データ・インターフェイス：
  - 最大レーン速度：17.16Gbps
  - 64b/66b および 8b/10b エンコードのサポート
  - 8b/10b モードは JESD204B 互換
- ピーク RF 入力電力 (差動)：+26.5dBm (+27.5dBFS、560x フルスケール電力)
- イコライゼーション用のプログラム可能な FIR フィルタ
- 消費電力：3.8W
- 電源：1.1V、1.9V

2 アプリケーション

- オシロスコープおよび広帯域デジタイザ
- 通信機器試験装置 (802.11ad、5G)
- 電子諜報活動 (SIGINT、ELINT)
- 衛星通信 (SATCOM)
- RF サンプリングのソフトウェア無線 (SDR)
- 分光測定

3 概要

ADC08DJ5200RF デバイスは、RF サンプリング、ギガ・サンプルの A/D コンバータ (ADC) で、DC から 10GHz 超までの入力周波数を直接サンプリングします。ADC08DJ5200RF はデュアル・チャネル 5.2GSPS の ADC、またはシングル・チャネル 10.4GSPS の ADC として構成できます。使用可能な入力周波数帯域が最高 10GHz であるため、L バンド、S バンド、C バンド、X バンドを直接 RF サンプリングでき、多様な周波数に対応したシステムを実現できます。

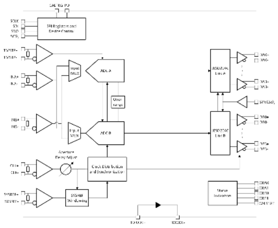
ADC08DJ5200RF は、最大 17.16Gbps のライン速度をサポートする最大 16 個のシリアル化されたレーンを備えた、高速な JESD204C 出力インターフェイスを使っています。JESD204C subclass-1 により、決定論的レイテンシおよびマルチデバイス同期をサポートしています。JESD204C インターフェイスは、ライン速度とレーン数との間でトレードオフのバランスを取るように構成できます。8b/10b と 64b/66b の両方のデータ・エンコードをサポートしています。64b/66b エンコードでは、前方誤り訂正 (FEC) によるビット・エラー率の改善をサポートしています。このインターフェイスは、JESD204B レシーバと下位互換性があります。

ノイズなしのアパーチャ遅延調整や、SYSREF ウィンドウ処理などの革新的な同期機能により、マルチ・チャネル・アプリケーションのシステム設計を簡素化できます。プログラム可能な FIR フィルタにより、オンチップのイコライゼーションが可能です。

製品情報

部品番号	パッケージ[1]	本体サイズ (公称)
ADC08DJ5200RF	FCBGA (144)	10.00mm × 10.00mm

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



ADC08DJ5200RF ブロック図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (August 2021) to Revision A (May 2022)	Page
• Added plots 図 6-123 through 図 6-126 to show overdrive recovery	28
• Change four TAD_COARSE LSBs per 256 t_{CLK} cycles to *384 t_{CLK} cycles* in Aperture Delay Ramp Control (TAD_RAMP)	57
• Changed TAD Register to properly show TAD_FINE register bits	90
• Changed PFIR_AB2 to PFIR_B2 in PFIR_B2	90
• Added the JMODE register table information	90
• Removed registers 0x102-0x152 as these should be reserved	90
• Added note 1 to 表 7-130	90

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5 Pin Configuration and Functions

	1	2	3	4	5	6	7	8	9	10	11	12
A	AGND	AGND	AGND	INA+	INA–	AGND	AGND	DA3+	DA3–	DA2+	DA2–	DGND
B	TMSTP+	AGND	AGND	AGND	AGND	AGND	AGND	DA7+	DA7–	DA6+	DA6–	DGND
C	TMSTP–	$\overline{\text{SYNCSE}}$	BG	VA19	VA11	AGND	NCOA0	ORA0	VD11	VD11	DA5+	DA1+
D	AGND	VA11	VA11	VA19	VA11	AGND	NCOA1	ORA1	DGND	DGND	DA5–	DA1–
E	AGND	VA19	VA19	VA19	VA11	AGND	CALTRIG	$\overline{\text{SCS}}$	VD11	VD11	DA4+	DA0+
F	CLK+	AGND	AGND	VA19	VA11	AGND	CALSTAT	SCLK	DGND	DGND	DA4–	DA0–
G	CLK–	AGND	AGND	VA19	VA11	AGND	VD11	SDI	DGND	DGND	DB4–	DB0–
H	AGND	VA19	VA19	VA19	VA11	AGND	VD11	SDO	VD11	VD11	DB4+	DB0+
J	AGND	VA11	VA11	VA19	VA11	AGND	NCOB1	ORB1	DGND	DGND	DB5–	DB1–
K	SYSREF+	TDIODE+	TDIODE–	VA19	VA11	PD	NCOB0	ORB0	VD11	VD11	DB5+	DB1+
L	SYSREF–	AGND	AGND	AGND	AGND	AGND	AGND	DB7+	DB7–	DB6+	DB6–	DGND
M	AGND	AGND	AGND	INB+	INB–	AGND	AGND	DB3+	DB3–	DB2+	DB2–	DGND

Not to scale

図 5-1. AAV Package, 144-Ball Flip Chip BGA, Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	A1, A2, A3, A6, A7, B2, B3, B4, B5, B6, B7, C6, D1, D6, E1, E6, F2, F3, F6, G2, G3, G6, H1, H6, J1, J6, L2, L3, L4, L5, L6, L7, M1, M2, M3, M6, M7	—	Analog supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
BG	C3	O	Band-gap voltage output. This pin is capable of sourcing only small currents and driving limited capacitive loads, as specified in the *Recommended Operating Conditions* table. This pin can be left disconnected if not used.
CALSTAT	F7	O	Foreground calibration status output or device alarm output. Functionality is programmed through CAL_STATUS_SEL. This pin can be left disconnected if not used.
CALTRIG	E7	I	Foreground calibration trigger input. This pin is only used if hardware calibration triggering is selected in CAL_TRIG_EN, otherwise software triggering is performed using CAL_SOFT_TRIG. Tie this pin to GND if not used.
CLK+	F1	I	Device (sampling) clock positive input. The clock signal is strongly recommended to be AC-coupled to this input for best performance. In single-channel mode, the analog input signal is sampled on both the rising and falling edges. In dual-channel mode, the analog signal is sampled on the rising edge. This differential input has an internal untrimmed 100-Ω differential termination and is self-biased to the optimal input common-mode voltage as long as DEVCLK_LVPECL_EN is set to 0.
CLK–	G1	I	Device (sampling) clock negative input. TI strongly recommends using AC-coupling for best performance.
DA0+	E12	O	High-speed serialized data output for channel A, lane 0, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DA0–	F12	O	High-speed serialized data output for channel A, lane 0, negative connection. This pin can be left disconnected if not used.
DA1+	C12	O	High-speed serialized data output for channel A, lane 1, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DA1–	D12	O	High-speed serialized data output for channel A, lane 1, negative connection. This pin can be left disconnected if not used.
DA2+	A10	O	High-speed serialized-data output for channel A, lane 2, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DA2–	A11	O	High-speed serialized-data output for channel A, lane 2, negative connection. This pin can be left disconnected if not used.
DA3+	A8	O	High-speed serialized-data output for channel A, lane 3, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DA3–	A9	O	High-speed serialized-data output for channel A, lane 3, negative connection. This pin can be left disconnected if not used.
DA4+	E11	O	High-speed serialized data output for channel A, lane 4, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DA4–	F11	O	High-speed serialized data output for channel A, lane 4, negative connection. This pin can be left disconnected if not used.
DA5+	C11	O	High-speed serialized data output for channel A, lane 5, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.

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表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DA5–	D11	O	High-speed serialized data output for channel A, lane 5, negative connection. This pin can be left disconnected if not used.
DA6+	B10	O	High-speed serialized data output for channel A, lane 6, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DA6–	B11	O	High-speed serialized data output for channel A, lane 6, negative connection. This pin can be left disconnected if not used.
DA7+	B8	O	High-speed serialized data output for channel A, lane 7, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DA7–	B9	O	High-speed serialized data output for channel A, lane 7, negative connection. This pin can be left disconnected if not used.
DB0+	H12	O	High-speed serialized data output for channel B, lane 0, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DB0–	G12	O	High-speed serialized data output for channel B, lane 0, negative connection. This pin can be left disconnected if not used.
DB1+	K12	O	High-speed serialized data output for channel B, lane 1, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DB1–	J12	O	High-speed serialized data output for channel B, lane 1, negative connection. This pin can be left disconnected if not used.
DB2+	M10	O	High-speed serialized data output for channel B, lane 2, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DB2–	M11	O	High-speed serialized data output for channel B, lane 2, negative connection. This pin can be left disconnected if not used.
DB3+	M8	O	High-speed serialized data output for channel B, lane 3, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DB3–	M9	O	High-speed serialized data output for channel B, lane 3, negative connection. This pin can be left disconnected if not used.
DB4+	H11	O	High-speed serialized data output for channel B, lane 4, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DB4–	G11	O	High-speed serialized data output for channel B, lane 4, negative connection. This pin can be left disconnected if not used.
DB5+	K11	O	High-speed serialized data output for channel B, lane 5, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DB5–	J11	O	High-speed serialized data output for channel B, lane 5, negative connection. This pin can be left disconnected if not used.
DB6+	L10	O	High-speed serialized data output for channel B, lane 6, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DB6–	L11	O	High-speed serialized data output for channel B, lane 6, negative connection. This pin can be left disconnected if not used.
DB7+	L8	O	High-speed serialized data output for channel B, lane 7, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DB7–	L9	O	High-speed serialized data output for channel B, lane 7, negative connection. This pin can be left disconnected if not used.

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表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DGND	A12, B12, D9, D10, F9, F10, G9, G10, J9, J10, L12, M12	—	Digital supply ground. Tie AGND and DGND to a common ground plane (GND) on the circuit board.
INA+	A4	I	Channel A analog input positive connection. INA± is recommended for use in single channel mode for optimal performance. The differential full-scale input voltage is determined by the FS_RANGE_A register (see the *Full-Scale Voltage (V_{FS}) Adjustment* section). This input is terminated to ground through a 50-Ω termination resistor. The input common-mode voltage is typically be set to 0 V (GND) and must follow the recommendations in the *Recommended Operating Conditions* table. This pin can be left disconnected if not used.
INA–	A5	I	Channel A analog input negative connection. INA± is recommended for use in single channel mode for optimal performance. See INA+ (pin A4) for detailed description. This input is terminated to ground through a 50-Ω termination resistor. This pin can be left disconnected if not used.
INB+	M4	I	Channel B analog input positive connection. INA± is recommended for use in single channel mode for optimal performance. The differential full-scale input voltage is determined by the FS_RANGE_B register (see the *Full-Scale Voltage (V_{FS}) Adjustment* section). This input is terminated to ground through a 50-Ω termination resistor. The input common-mode voltage must typically be set to 0 V (GND) and must follow the recommendations in the *Recommended Operating Conditions* table. This pin can be left disconnected if not used.
INB–	M5	I	Channel B analog input negative connection. INA± is recommended for use in single channel mode for optimal performance. See INB+ for detailed description. This input is terminated to ground through a 50-Ω termination resistor. This pin can be left disconnected if not used.
NCOA0	C7	I	Not used. Tie this pin to GND.
NCOA1	D7	I	Not used. Tie this pin to GND.
NCOB0	K7	I	Not used. Tie this pin to GND.
NCOB1	J7	I	Not used. Tie this pin to GND.
ORA0	C8	O	Fast overrange detection status for channel A for the OVR_T0 threshold. When the analog input exceeds the threshold programmed into OVR_T0, this status indicator goes high. The minimum pulse duration is set by OVR_N. See the *ADC Overrange Detection* section for more information. This pin can be left disconnected if not used.
ORA1	D8	O	Fast overrange detection status for channel A for the OVR_T1 threshold. When the analog input exceeds the threshold programmed into OVR_T1, this status indicator goes high. The minimum pulse duration is set by OVR_N. See the *ADC Overrange Detection* section for more information. This pin can be left disconnected if not used.
ORB0	K8	O	Fast overrange detection status for channel B for the OVR_T0 threshold. When the analog input exceeds the threshold programmed into OVR_T0, this status indicator goes high. The minimum pulse duration is set by OVR_N. See the *ADC Overrange Detection* section for more information. This pin can be left disconnected if not used.
ORB1	J8	O	Fast overrange detection status for channel B for the OVR_T1 threshold. When the analog input exceeds the threshold programmed into OVR_T1, this status indicator goes high. The minimum pulse duration is set by OVR_N. See the *ADC Overrange Detection* section for more information. This pin can be left disconnected if not used.
PD	K6	I	This pin disables all analog circuits and serializer outputs when set high for temperature diode calibration or to reduce power consumption when the device is not being used. Tie this pin to GND if not used.
SCLK	F8	I	Serial interface clock. This pin functions as the serial-interface clock input that clocks the serial programming data in and out. The *Using the Serial Interface* section describes the serial interface in more detail. Supports 1.1-V and 1.8-V CMOS levels.
$\overline{\text{SCS}}$	E8	I	Serial interface chip select active low input. The *Using the Serial Interface* section describes the serial interface in more detail. Supports 1.1-V and 1.8-V CMOS levels. This pin has a 82-kΩ pullup resistor to VD11.
SDI	G8	I	Serial interface data input. The *Using the Serial Interface* section describes the serial interface in more detail. Supports 1.1-V and 1.8-V CMOS levels.
SDO	H8	O	Serial interface data output. The *Using the Serial Interface* section describes the serial interface in more detail. This pin is high impedance during normal device operation. This pin outputs 1.9-V CMOS levels during serial interface read operations. This pin can be left disconnected if not used.

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表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{SYNCSE}}$	C2	I	Single-ended JESD204C SYNC signal. This input is an active low input that is used to initialize the JESD204C serial link in 8B/10B modes when SYNC_SEL is set to 0. The 64B/66B modes do not use the SYNC signal for initialization, however it may be used for NCO synchronization. When toggled low in 8B/10B modes this input initiates code group synchronization (see the *Code Group Synchronization (CGS)* section). After code group synchronization, this input must be toggled high to start the initial lane alignment sequence (see the *Initial Lane Alignment Sequence (ILAS)* section). A differential SYNC signal can be used instead by setting SYNC_SEL to 1 and using TMSTP± as a differential $\overline{\text{SYNC}}$ input. Tie this pin to GND if differential $\overline{\text{SYNC}}$ (TMSTP±) is used as the JESD204C SYNC signal.
SYSREF+	K1	I	The SYSREF positive input is used to achieve synchronization and deterministic latency across the JESD204C interface. This differential input (SYSREF+ to SYSREF–) has an internal untrimmed 100-Ω differential termination and can be AC-coupled when SYSREF_LVPECL_EN is set to 0. This input is self-biased when SYSREF_LVPECL_EN is set to 0. The termination changes to 50 Ω to ground on each input pin (SYSREF+ and SYSREF–) and can be DC-coupled when SYSREF_LVPECL_EN is set to 1. This input is not self-biased when SYSREF_LVPECL_EN is set to 1 and must be biased externally to the input common-mode voltage range provided in the *Recommended Operating Conditions* table.
SYSREF–	L1	I	SYSREF negative input
TDIODE+	K2	I	Temperature diode positive (anode) connection. An external temperature sensor can be connected to TDIODE+ and TDIODE– to monitor the junction temperature of the device. This pin can be left disconnected if not used.
TDIODE–	K3	I	Temperature diode negative (cathode) connection. This pin can be left disconnected if not used.
TMSTP+	B1	I	Timestamp input positive connection or differential JESD204C $\overline{\text{SYNC}}$ positive connection. This input is a timestamp input, used to mark a specific sample, when TIMESTAMP_EN is set to 1. This differential input is used as the JESD204C SYNC signal input when SYNC_SEL is set 1. This input can be used as both a timestamp and differential SYNC input at the same time, allowing feedback of the SYNC signal using the timestamp mechanism. TMSTP± uses active low signaling when used as a JESD204C SYNC. For additional usage information, see the *Timestamp* section. TMSTP_RECV_EN must be set to 1 to use this input. This differential input (TMSTP+ to TMSTP–) has an internal untrimmed 100-Ω differential termination and can be AC-coupled when TMSTP_LVPECL_EN is set to 0. The termination changes to 50 Ω to ground on each input pin (TMSTP+ and TMSTP–) and can be DC coupled when TMSTP_LVPECL_EN is set to 1. This pin is not self-biased and therefore must be externally biased for both AC- and DC-coupled configurations. The common-mode voltage must be within the range provided in the *Recommended Operating Conditions* table when both AC and DC coupled. This pin can be left disconnected and disabled (TMSTP_RECV_EN = 0) if $\overline{\text{SYNCSE}}$ is used for JESD204C SYNC and timestamp is not required.
TMSTP–	C1	I	Timestamp input positive connection or differential JESD204C $\overline{\text{SYNC}}$ negative connection. This pin can be left disconnected and disabled (TMSTP_RECV_EN = 0) if $\overline{\text{SYNCSE}}$ is used for JESD204C SYNC and timestamp is not required.
VA11	C5, D2, D3, D5, E5, F5, G5, H5, J2, J3, J5, K5	I	1.1-V analog supply
VA19	C4, D4, E2, E3, E4, F4, G4, H2, H3, H4, J4, K4	I	1.9-V analog supply
VD11	C9, C10, E9, E10, G7, H7, H9, H10, K9, K10	I	1.1-V digital supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{DD}	Supply voltage range	VA19[2]	–0.3	2.35	V
		VA11[2]	–0.3	1.32	
		VD11[3]	–0.3	1.32	
		Voltage between VD11 and VA11	–1.32	1.32	
V_{GND}	Voltage between AGND and DGND		–0.1	0.1	V
V_{PIN}	Pin voltage range	DA[7:0]+, DA[7:0]–, DB[7:0]+, DB[7:0]–, TMSTP+, TMSTP–[3]	–0.5	VD11 + 0.5[5]	V
		CLK+, CLK–, SYSREF+, SYSREF–[2]	–0.5	VA11 + 0.5[4]	
		BG, TDIODE+, TDIODE–[2]	–0.5	VA19 + 0.5[6]	
		INA+, INA–, INB+, INB–[2]	–1	1	
		CALSTAT, CALTRIG, NCOA0, NCOA1, NCOB0, NCOB1, ORA0, ORA1, ORB0, ORB1, PD, SCLK, $\overline{SCS}$, SDI, SDO, $\overline{SYNCSE}$ [2]	–0.5	VA19 + 0.5[6]	
$I_{MAX(ANY)}$	Peak input current (any input except INA+, INA–, INB+, INB–)		–25	25	mA
$I_{MAX(INx)}$	Peak input current (INA+, INA–, INB+, INB–)		–50	50	mA
$P_{MAX(INx)}$	Peak RF input power (INA+, INA–, INB+, INB–)	differential with $Z_{S\text{-}DIFF}$ = 100 Ω, up to 21 days[7]		26.5	dBm
		Single-ended with $Z_{S\text{-}SE}$ = 50 Ω		16.4	dBm
$I_{MAX(ALL)}$	Peak total input current (sum of absolute value of all currents forced in or out, not including power-supply current)			100	mA
T_j	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured to AGND.
(3) Measured to DGND.
(4) Maximum voltage not to exceed VA11 absolute maximum rating.
(5) Maximum voltage not to exceed VD11 absolute maximum rating.
(6) Maximum voltage not to exceed VA19 absolute maximum rating.
(7) Tested continuously for 21 days with F_{IN} = 1.2 GHz on a typical device. At the end of testing, the device was not damaged. During the overdrive, the ADC is still properly converting the input signal, although it will be saturated for voltages beyond the input fullscale.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage range	VA19, analog 1.9-V supply[2]	1.8	1.9	2.0	V
		VA11, analog 1.1-V supply[2]	1.05	1.1	1.15	
		VD11, digital 1.1-V supply[3]	1.05	1.1	1.15	
V_{CMI}	Input common-mode voltage	INA+, INA–, INB+, INB–[2]	–50	0	100	mV
		CLK+, CLK–, SYSREF+, SYSREF–[2] [4]	0	0.3	0.55	V
		TMSTP+, TMSTP–[3] [5]	0	0.3	0.55	
V_{ID}	Input voltage, peak-to-peak differential	CLK+ to CLK–, SYSREF+ to SYSREF–, TMSTP+ to TMSTP–	0.4	1.0	2.0	$V_{PP\text{-}DIFF}$
		INA+ to INA–, INB+ to INB–			0.8[6]	
I_{C_TD}	Temperature diode input current	TDIODE+ to TDIODE–		100		µA
C_L	BG maximum load capacitance				50	pF
I_O	BG maximum output current				100	µA
DC	Input clock duty cycle		30	50	70	%
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature				125[1]	°C

(1) Prolonged use above junction temperature of 105°C may increase the device failure-in-time (FIT) rate.
(2) Measured to AGND.
(3) Measured to DGND.
(4) TI strongly recommends that CLK± be AC-coupled with DEVCLK_LVPECL_EN set to 0 to allow CLK± to self-bias to the optimal input common-mode voltage for best performance. TI recommends AC-coupling for SYSREF± unless DC-coupling is required, in which case, the LVPECL input mode must be used (SYSREF_LVPECL_EN = 1).
(5) TMSTP± does not have internal biasing that requires TMSTP± to be biased externally whether AC-coupled with TMSTP_LVPECL_EN = 0 or DC-coupled with TMSTP_LVPECL_EN= 1.
(6) The ADC output code saturates when V_{ID} for INA± or INB± exceeds the programmed full-scale voltage(V_{FS}) set by FS_RANGE_A for INA± or FS_RANGE_B for INB±.

6.4 Thermal Information

THERMAL METRIC[1]		ADC08DJ5200RF AAV or ZEG (FCBGA) 144 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	23.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.23	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	8.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

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6.5 Electrical Characteristics: DC Specifications

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2 GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 6, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
	Resolution	Resolution with no missing codes		8		Bits
DNL	Differential nonlinearity	Maximum positive excursion from ideal step size		0.08		LSB
		Maximum negative excursion from ideal step size		–0.08		
INL	Integral nonlinearity	Maximum positive excursion from ideal transfer function		0.1		LSB
		Maximum negative excursion from ideal transfer function		–0.15		LSB
ANALOG INPUTS (INA+, INA–, INB+, INB–)						
V_{OFF}	Offset error	CAL_OS = 0		±0.50		mV
		CAL_OS = 1		±0.15		mV
V_{OFF_ADJ}	Input offset voltage adjustment range	Available offset correction range (see OS_CAL or OADJ_x_INx)		±50		mV
V_{OFF_DRIFT}	Offset drift	Foreground calibration at nominal temperature only		11		µV/°C
		Foreground calibration at each temperature		-2.7		
		Foreground and FGOS calibration at each temperature		0		
V_{FS}	Analog differential input full-scale range	Default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000)	775	825	875	mV_{PPDIFF}
		Maximum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xFFFF)	1000	1060		
		Minimum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0x2000)		500	550	
V_{FS_DRIFT}	Analog differential input full-scale range drift	Default FS_RANGE_A and FS_RANGE_B setting, foreground calibration at each temperature, inputs driven by a 50-Ω source, includes effect of R_{IN} drift		0.055		%/°C
V_{FS_MATCH}	Analog differential input full-scale range matching	Matching between INA± and INB±, default setting, dual-channel mode		0.4%		
R_{IN}	Single-ended input resistance to AGND	Each input pin is terminated to AGND, measured at T_A = 25°C	48	50	52	Ω
R_{IN_TEMPCO}	Input termination linear temperature coefficient			14.7		mΩ/°C
C_{IN}	Single-ended input capacitance	Single-channel mode measured at DC		0.4		pF
		Dual-channel mode measured at DC		0.4		
TEMPERATURE DIODE CHARACTERISTICS (TDIODE+, TDIODE–)						
ΔV_{BE}	Temperature diode voltage slope	Forced forward current of 100 µA. Offset voltage (approximately 0.792 V at 0°C) varies with process and must be measured for each part. Offset measurement must be done with the device unpowered or with the PD pin asserted to minimize device self-heating.		–1.65		mV/°C

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6.5 Electrical Characteristics: DC Specifications (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2 GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 6, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BAND-GAP VOLTAGE OUTPUT (BG)						
V_{BG}	Reference output voltage	I_L ≤ 100 µA		1.1		V
V_{BG_DRIFT}	Reference output temperature drift	I_L ≤ 100 µA		–123		µV/°C
CLOCK INPUTS (CLK+, CLK–, SYSREF+, SYSREF–, TMSTP+, TMSTP–)						
Z_T	Internal termination	Differential termination with DEVCLK_LVPECL_EN = 0, SYSREF_LVPECL_EN = 0, and TMSTP_LVPECL_EN = 0		100		Ω
		Single-ended termination to GND (per pin) with DEVCLK_LVPECL_EN = 0, SYSREF_LVPECL_EN = 0, and TMSTP_LVPECL_EN = 0		50		
V_{CM}	Input common-mode voltage, self-biased	Self-biasing common-mode voltage for CLK± when AC-coupled (DEVCLK_LVPECL_EN must be set to 0)		0.3		V
		Self-biasing common-mode voltage for SYSREF± when AC-coupled (SYSREF_LVPECL_EN must be set to 0) and with receiver enabled (SYSREF_RECV_EN = 1)		0.28		
		Self-biasing common-mode voltage for SYSREF± when AC-coupled (SYSREF_LVPECL_EN must be set to 0) and with receiver disabled (SYSREF_RECV_EN = 0)		0.28		
C_{L_DIFF}	Differential input capacitance	Between positive and negative differential input pins		0.04		pF
C_{L_SE}	Single-ended input capacitance	Each input to ground		0.5		pF
SERDES OUTPUTS (DA[7:0]+, DA[7:0]–, DB[7:0]+, DB[7:0]–)						
V_{OD}	Differential output voltage, peak-to-peak	100-Ω load	550	600	650	$mV_{PP\text{-}DIFF}$
V_{CM}	Output common-mode voltage	AC coupled		VD11 / 2		V
Z_{DIFF}	Differential output impedance			100		Ω
CMOS INTERFACE: SCLK, SDI, SDO, $\overline{\text{SCS}}$, PD, NCOA0, NCOA1, NCOB0, NCOB1, CALSTAT, CALTRIG, ORA0, ORA1, ORB0, ORB1, $\overline{\text{SYNCSE}}$						
V_{IH}	High-level input voltage	required input voltage	0.7			V
V_{IL}	Low-level input voltage	required input voltage			0.45	V
I_{IH}	High-level input current				40	µA
I_{IL}	Low-level input current		–40			µA
C_I	Input capacitance			3.4		pF
V_{OH}	High-level output voltage	I_{LOAD} = –400 µA	1.65			V
V_{OL}	Low-level output voltage	I_{LOAD} = 400 µA			150	mV

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6.6 Electrical Characteristics: Power Consumption

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2 GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 6, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VA19}	1.9-V analog supply current	Power mode 1: JMODE 6 (single-channel mode, 16 lanes, 8B/10B encoding), foreground calibration		950		mA
I_{VA11}	1.1-V analog supply current			870		mA
I_{VD11}	1.1-V digital supply current			1010		mA
P_{DIS}	Power dissipation			3.8		W
I_{VA19}	1.9-V analog supply current	Power mode 2: JMODE 44 (single-channel mode, 8 lanes, 64B/66B encoding), foreground calibration		925	1050	mA
I_{VA11}	1.1-V analog supply current			870	1000	mA
I_{VD11}	1.1-V digital supply current			960	1150	mA
P_{DIS}	Power dissipation			3.7	4.2	W
I_{VA19}	1.9-V analog supply current	Power mode 3: JMODE 6 (single-channel mode, 16 lanes, 8B/10B encoding), background calibration		1255		mA
I_{VA11}	1.1-V analog supply current			1050		mA
I_{VD11}	1.1-V digital supply current			1160		mA
P_{DIS}	Power dissipation			4.65		W
I_{VA19}	1.9-V analog supply current	Power mode 7: PD pin held high, clock disabled		44		mA
I_{VA11}	1.1-V analog supply current			27		mA
I_{VD11}	1.1-V digital supply current			33		mA
P_{DIS}	Power dissipation			0.15		W

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6.7 Electrical Characteristics: AC Specifications (Dual-Channel Mode)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 8, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FPBW	Full-power input bandwidth (–3 dB)(1)	Foreground calibration			8.1		GHz
		Background calibration			8.1		
XTALK	Channel-to-channel crosstalk	Aggressor = 1 GHz, –1 dBFS			–81		dB
		Aggressor = 3 GHz, –1 dBFS			–76		
		Aggressor = 6 GHz, –1 dBFS			–69		
CER	Code error rate	Maximum CER, does not include JESD204C interface BER			10^{-18}		Errors/ sample
$NOISE_{DC}$	DC input noise standard deviation	No input, foreground calibration, excludes DC offset, includes fixed interleaving spur (f_S / 2 spur)			0.26		LSB
NSD	Noise spectral density, excludes fixed interleaving spur (f_S / 2 spur)	Maximum full-scale voltage (V_{FS} = 1.0 V_{PP}), A_{IN} = –20 dBFS			–143.4		dBFS/ Hz
		Default full-scale voltage (V_{FS} = 0.8 V_{PP}), A_{IN} = –20 dBFS			–143.2		
NF	Noise figure, Z_S = 100 Ω	Maximum full-scale voltage (V_{FS} = 1.0 V_{PP}), A_{IN} = –20 dBFS			31.6		dB
		Default full-scale voltage (V_{FS} = 0.8 V_{PP}), A_{IN} = –20 dBFS			29.9		
SNR	Signal-to-noise ratio, excluding DC, HD2 to HD9, f_S / 2, f_S / 2 – f_{IN},	f_{IN} = 347 MHz	A_{IN} = –1 dBFS		48.8		dBFS
			A_{IN} = –3 dBFS		49		
			A_{IN} = –12 dBFS		49.0		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		49.1		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		48.7		
			A_{IN} = –3 dBFS		48.9		
			A_{IN} = –12 dBFS		49.0		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS	46.5	48.6		
			A_{IN} = –3 dBFS		48.8		
			A_{IN} = –12 dBFS		49.0		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		49.0		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		48.1		
			A_{IN} = –3 dBFS		48.5		
			A_{IN} = –12 dBFS		49.0		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		47.7		
			A_{IN} = –3 dBFS		48.2		
			A_{IN} = –12 dBFS		48.9		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		47.1		
			A_{IN} = –3 dBFS		47.8		
			A_{IN} = –12 dBFS		48.9		

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6.7 Electrical Characteristics: AC Specifications (Dual-Channel Mode) (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 8, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise and distortion ratio, excluding DC and f_S / 2 fixed spurs	f_{IN} = 347 MHz	A_{IN} = –1 dBFS		48.5		dBFS
			A_{IN} = –3 dBFS		48.8		
			A_{IN} = –12 dBFS		48.9		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		48.9		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		48.4		
			A_{IN} = –3 dBFS		48.8		
			A_{IN} = –12 dBFS		48.9		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS	45.5	48.4		
			A_{IN} = –3 dBFS		48.7		
			A_{IN} = –12 dBFS		48.9		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		48.9		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		47.6		
			A_{IN} = –3 dBFS		48.2		
			A_{IN} = –12 dBFS		48.8		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		45.5		
			A_{IN} = –3 dBFS		47.4		
			A_{IN} = –12 dBFS		48.8		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		45.8		
			A_{IN} = –3 dBFS		47.4		
			A_{IN} = –12 dBFS		48.7		
ENOB	Effective number of bits, excluding DC and f_S / 2 fixed spurs	f_{IN} = 347 MHz	A_{IN} = –1 dBFS		7.8		bits
			A_{IN} = –3 dBFS		7.8		
			A_{IN} = –12 dBFS		7.8		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		7.8		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		7.7		
			A_{IN} = –3 dBFS		7.8		
			A_{IN} = -12 dBFS		7.9		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS	7.27	7.8		
			A_{IN} = –3 dBFS		7.8		
			A_{IN} = –12 dBFS		7.8		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		7.8		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		7.6		
			A_{IN} = –3 dBFS		7.7		
			A_{IN} = –12 dBFS		7.8		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		7.3		
			A_{IN} = –3 dBFS		7.6		
			A_{IN} = –12 dBFS		7.8		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		7.3		
			A_{IN} = –3 dBFS		7.6		
			A_{IN} = –12 dBFS		7.8		

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6.7 Electrical Characteristics: AC Specifications (Dual-Channel Mode) (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 8, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SFDR	Spurious-free dynamic range, excluding DC and f_S / 2 fixed spurs	f_{IN} = 347 MHz	A_{IN} = –1 dBFS		65		dBFS
			A_{IN} = –3 dBFS		68		
			A_{IN} = –12 dBFS		68		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		67		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		63		
			A_{IN} = –3 dBFS		69		
			A_{IN} = –12 dBFS		68		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS	52	67		
			A_{IN} = –3 dBFS		69		
			A_{IN} = –12 dBFS		69		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		69		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		59		
			A_{IN} = –3 dBFS		63		
			A_{IN} = –12 dBFS		68		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		52		
			A_{IN} = –3 dBFS		58		
			A_{IN} = –12 dBFS		68		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		53		
			A_{IN} = –3 dBFS		61		
			A_{IN} = –12 dBFS		69		
HD2	2nd-order harmonic distortion	f_{IN} = 347 MHz	AIN = –1 dBFS		–74		dBFS
			A_{IN} = –3 dBFS		–76		
			A_{IN} = –12 dBFS		–78		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–75		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		–74		
			A_{IN} = –3 dBFS		–76		
			A_{IN} = –12 dBFS		–75		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS		–74	-55	
			A_{IN} = –3 dBFS		–74		
			A_{IN} = –12 dBFS		–78		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–75		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		–61		
			A_{IN} = –3 dBFS		–65		
			A_{IN} = –12 dBFS		–77		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		–55		
			A_{IN} = –3 dBFS		–60		
			A_{IN} = –12 dBFS		–73		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		–64		
			A_{IN} = –3 dBFS		–69		
			A_{IN} = –12 dBFS		–75		

6.7 Electrical Characteristics: AC Specifications (Dual-Channel Mode) (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 8, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HD3	3rd-order harmonic distortion	f_{IN} = 347 MHz	AIN = –1 dBFS		–66		dBFS
			A_{IN} = –3 dBFS		–72		
			A_{IN} = –12 dBFS		–73		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–70		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		–63		
			A_{IN} = –3 dBFS		–79		
			A_{IN} = –12 dBFS		–75		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS		–71	-55	
			A_{IN} = –3 dBFS		–72		
			A_{IN} = –12 dBFS		–80		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–73		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		–65		
			A_{IN} = –3 dBFS		–65		
			A_{IN} = –12 dBFS		–75		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		–53		
			A_{IN} = –3 dBFS		–61		
			A_{IN} = –12 dBFS		–71		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		–53		
			A_{IN} = –3 dBFS		–62		
			A_{IN} = –12 dBFS		–87		
f_S / 2 – f_{IN}	f_S / 2 – f_{IN} input signal dependent interleaving spur	f_{IN} = 347 MHz	AIN = –1 dBFS		–73		dBFS
			A_{IN} = –3 dBFS		–73		
			A_{IN} = –12 dBFS		–78		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–73		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		–69		
			A_{IN} = –3 dBFS		–71		
			A_{IN} = –12 dBFS		–79		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS		–70	-52	
			A_{IN} = –3 dBFS		–74		
			A_{IN} = –12 dBFS		–75		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–74		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		–67		
			A_{IN} = –3 dBFS		–68		
			A_{IN} = –12 dBFS		–74		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		–67		
			A_{IN} = –3 dBFS		–69		
			A_{IN} = –12 dBFS		–74		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		–62		
			A_{IN} = –3 dBFS		–64		
			A_{IN} = –12 dBFS		–72		
f_S / 2	f_S / 2 fixed interleaving spur, independent of input signal	A_{IN} = –20 dBFS			–76	-52	dBFS

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6.7 Electrical Characteristics: AC Specifications (Dual-Channel Mode) (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 8, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SPUR	Worst spur, excluding DC, HD2, HD3, f_S / 2 and f_S / 2 - f_{IN} spurs	f_{IN} = 347 MHz	AIN = –1 dBFS		–70		dBFS
			A_{IN} = –3 dBFS		–70		
			A_{IN} = –12 dBFS		–70		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–70		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		–68		
			A_{IN} = –3 dBFS		–71		
			A_{IN} = –12 dBFS		–68		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS		–72	-60	
			A_{IN} = –3 dBFS		–72		
			A_{IN} = –12 dBFS		–70		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–71		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		–69		
			A_{IN} = –3 dBFS		–71		
			A_{IN} = –12 dBFS		–69		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		–65		
			A_{IN} = –3 dBFS		–70		
			A_{IN} = –12 dBFS		–70		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		–69		
			A_{IN} = –3 dBFS		–71		
			A_{IN} = –12 dBFS		–70		
IMD3	3rd-order intermodulation distortion	f_1 = 343 MHz, f_2 = 353 MHz	A_{IN} = –7 dBFS per tone		–80		dBFS
			A_{IN} = –9 dBFS per tone		–77		
			A_{IN} = –18 dBFS per tone		–77		
			A_{IN} = –9 dBFS per tone, V_{FS} = 1.0 V_{PP}		–79		
		f_1 = 993 MHz, f_2 = 1003 MHz	A_{IN} = –7 dBFS per tone		–80		
			A_{IN} = –9 dBFS per tone		–82		
			A_{IN} = –18 dBFS per tone		–73		
		f_1 = 2393 MHz, f_2 = 2403 MHz	A_{IN} = –7 dBFS per tone		–69		
			A_{IN} = –9 dBFS per tone		–70		
			A_{IN} = –18 dBFS per tone		–83		
			A_{IN} = –9 dBFS per tone, V_{FS} = 1.0 V_{PP}		–69		
		f_1 = 4193 MHz, f_2 = 4203 MHz	A_{IN} = –7 dBFS per tone		–67		
			A_{IN} = –9 dBFS per tone		–74		
			A_{IN} = –18 dBFS per tone		–73		
		f_1 = 5993 MHz, f_2 = 6003 MHz	A_{IN} = –7 dBFS per tone		–59		
			A_{IN} = –9 dBFS per tone		–66		
			A_{IN} = –18 dBFS per tone		–72		
		f_1 = 7593 MHz, f_2 = 7603 MHz	A_{IN} = –7 dBFS per tone		–46		
			A_{IN} = –9 dBFS per tone		–53		
			A_{IN} = –18 dBFS per tone		–79		

(1) Full-power input bandwidth (FPBW) is defined as the input frequency where the reconstructed output of the ADC has dropped 3 dB below the power of a full-scale input signal at a low input frequency. Useable bandwidth may exceed the –3-dB, full-power input bandwidth.

6.8 Electrical Characteristics: AC Specifications (Single-Channel Mode)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, input signal applied to INA±, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2 GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 6, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FPBW	Full-power input bandwidth (–3 dB)(1)	Foreground calibration			7.9		GHz
		Background calibration			7.9		
CER	Code error rate	Maximum CER, does not include JESD204C interface BER			10^{-18}		Errors/ sample
$NOISE_{DC}$	DC input noise standard deviation	No input, foreground calibration, excludes DC offset, includes fixed interleaving spurs (f_S / 2 and f_S / 4 spurs), OS_CAL enabled			0.15		LSB
NSD	Noise spectral density, excludes fixed interleaving spurs (f_S / 2 and f_S / 4 spur)	Maximum full-scale voltage (V_{FS} = 1.0 V_{PP}), A_{IN} = –20 dBFS			–146.2		dBFS/ Hz
		Default full-scale voltage (V_{FS} = 0.8 V_{PP}), A_{IN} = –20 dBFS			–146.0		
NF	Noise figure, Z_S = 100 Ω	Maximum full-scale voltage (V_{FS} = 1.0 V_{PP}), A_{IN} = –20 dBFS			28.7		dB
		Default full-scale voltage (V_{FS} = 0.8 V_{PP}), A_{IN} = –20 dBFS			27.1		
SNR	Signal-to-noise ratio, excluding DC, HD2 to HD9, f_S / 2, f_S / 4, f_S / 2 – f_{IN}, f_S / 4 ± f_{IN}	f_{IN} = 347 MHz	A_{IN} = –1 dBFS		48.7		dBFS
			A_{IN} = –3 dBFS		48.9		
			A_{IN} = –12 dBFS		49.0		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		49.0		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		48.7		
			A_{IN} = –3 dBFS		48.8		
			A_{IN} = –12 dBFS		49.0		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS	46.8	48.6		
			A_{IN} = –3 dBFS		48.7		
			A_{IN} = –12 dBFS		49.0		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		48.9		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		48.2		
			A_{IN} = –3 dBFS		48.5		
			A_{IN} = –12 dBFS		48.9		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		47.7		
			A_{IN} = –3 dBFS		48.1		
			A_{IN} = –12 dBFS		49.0		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		47.1		
			A_{IN} = –3 dBFS		47.7		
			A_{IN} = –12 dBFS		48.9		

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6.8 Electrical Characteristics: AC Specifications (Single-Channel Mode) (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, input signal applied to INA±, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2 GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 6, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise and distortion ratio, excluding DC and f_S / 2 fixed spurs	f_{IN} = 347 MHz	A_{IN} = –1 dBFS		48.2		dBFS
			A_{IN} = –3 dBFS		48.5		
			A_{IN} = –12 dBFS		48.8		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		48.7		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		47.9		
			A_{IN} = –3 dBFS		48.4		
			A_{IN} = –12 dBFS		48.8		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS	44.5	47.3		
			A_{IN} = –3 dBFS		47.8		
			A_{IN} = –12 dBFS		48.7		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		48.0		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		46.5		
			A_{IN} = –3 dBFS		47.3		
			A_{IN} = –12 dBFS		48.6		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		45.5		
			A_{IN} = –3 dBFS		46.9		
			A_{IN} = –12 dBFS		48.7		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		44.9		
			A_{IN} = –3 dBFS		46.3		
			A_{IN} = –12 dBFS		48.6		
ENOB	Effective number of bits, excluding DC and f_S / 2 fixed spurs	f_{IN} = 347 MHz	A_{IN} = –1 dBFS		7.7		bits
			A_{IN} = –3 dBFS		7.7		
			A_{IN} = –12 dBFS		7.8		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		7.8		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		7.7		
			A_{IN} = –3 dBFS		7.7		
			A_{IN} = –12 dBFS		7.8		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS	7.1	7.6		
			A_{IN} = –3 dBFS		7.7		
			A_{IN} = –12 dBFS		7.8		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		7.7		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		7.4		
			A_{IN} = –3 dBFS		7.6		
			A_{IN} = –12 dBFS		7.8		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		7.3		
			A_{IN} = –3 dBFS		7.5		
			A_{IN} = –12 dBFS		7.8		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		7.2		
			A_{IN} = –3 dBFS		7.4		
			A_{IN} = –12 dBFS		7.8		

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6.8 Electrical Characteristics: AC Specifications (Single-Channel Mode) (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, input signal applied to INA±, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2 GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 6, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SFDR	Spurious free dynamic range, excluding DC, f_S / 4 and f_S / 2 fixed spurs	f_{IN} = 347 MHz	A_{IN} = –1 dBFS		63		dBFS
			A_{IN} = –3 dBFS		66		
			A_{IN} = –12 dBFS		70		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		65		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		60		
			A_{IN} = –3 dBFS		63		
			A_{IN} = –12 dBFS		69		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS	46	56		
			A_{IN} = –3 dBFS		59		
			A_{IN} = –12 dBFS		67		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		58		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		55		
			A_{IN} = –3 dBFS		57		
			A_{IN} = –12 dBFS		65		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		53		
			A_{IN} = –3 dBFS		56		
			A_{IN} = –12 dBFS		65		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		51		
			A_{IN} = –3 dBFS		54		
			A_{IN} = –12 dBFS		63		
HD2	2nd-order harmonic distortion	f_{IN} = 347 MHz	A_{IN} = –1 dBFS		–74		dBFS
			A_{IN} = –3 dBFS		–75		
			A_{IN} = –12 dBFS		–82		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–77		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		–77		
			A_{IN} = –3 dBFS		–77		
			A_{IN} = –12 dBFS		–82		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS		–71	-55	
			A_{IN} = –3 dBFS		–76		
			A_{IN} = –12 dBFS		–85		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–75		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		–63		
			A_{IN} = –3 dBFS		–64		
			A_{IN} = –12 dBFS		–80		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		–62		
			A_{IN} = –3 dBFS		–65		
			A_{IN} = –12 dBFS		–80		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		–68		
			A_{IN} = –3 dBFS		–72		
			A_{IN} = –12 dBFS		–83		

6.8 Electrical Characteristics: AC Specifications (Single-Channel Mode) (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, input signal applied to INA±, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2 GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 6, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HD3	3rd-order harmonic distortion	f_{IN} = 347 MHz	A_{IN} = –1 dBFS		–65		dBFS
			A_{IN} = –3 dBFS		–71		
			A_{IN} = –12 dBFS		–76		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–68		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		–63		
			A_{IN} = –3 dBFS		–78		
			A_{IN} = –12 dBFS		–76		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS		–70	-55	
			A_{IN} = –3 dBFS		–73		
			A_{IN} = –12 dBFS		–83		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–74		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		–70		
			A_{IN} = –3 dBFS		–66		
			A_{IN} = –12 dBFS		–75		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		–55		
			A_{IN} = –3 dBFS		–62		
			A_{IN} = –12 dBFS		–71		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		–53		
			A_{IN} = –3 dBFS		–64		
			A_{IN} = –12 dBFS		–86		
f_S / 2 – f_{IN}	f_S / 2 – f_{IN} input signal dependent interleaving spur	f_{IN} = 347 MHz	A_{IN} = –1 dBFS		–68		dBFS
			A_{IN} = –3 dBFS		–68		
			A_{IN} = –12 dBFS		–73		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–67		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		–62		
			A_{IN} = –3 dBFS		–63		
			A_{IN} = –12 dBFS		–75		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS		–56	-46	
			A_{IN} = –3 dBFS		–60		
			A_{IN} = –12 dBFS		–68		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–59		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		–56		
			A_{IN} = –3 dBFS		–58		
			A_{IN} = –12 dBFS		–67		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		–54		
			A_{IN} = –3 dBFS		–56		
			A_{IN} = –12 dBFS		–68		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		–52		
			A_{IN} = –3 dBFS		–55		
			A_{IN} = –12 dBFS		–64		

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6.8 Electrical Characteristics: AC Specifications (Single-Channel Mode) (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, input signal applied to INA±, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2 GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 6, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_S / 4 ± f_{IN}	f_S / 4 ± f_{IN} input signal dependent interleaving spur	f_{IN} = 347 MHz	A_{IN} = –1 dBFS		–74		dBFS
			A_{IN} = –3 dBFS		–74		
			A_{IN} = –12 dBFS		–80		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–74		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		–71		
			A_{IN} = –3 dBFS		–70		
			A_{IN} = –12 dBFS		–77		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS		–69	-50	
			A_{IN} = –3 dBFS		–74		
			A_{IN} = –12 dBFS		–79		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–75		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		–69		
			A_{IN} = –3 dBFS		–69		
			A_{IN} = –12 dBFS		–77		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		–70		
			A_{IN} = –3 dBFS		–69		
			A_{IN} = –12 dBFS		–78		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		–67		
			A_{IN} = –3 dBFS		–68		
			A_{IN} = –12 dBFS		–77		
f_S / 2	f_S / 2 fixed interleaving spur, independent of input signal	A_{IN} = –20 dBFS, OS_CAL disabled			–64		dBFS
		A_{IN} = –20 dBFS, OS_CAL enabled			–73		
f_S / 4	f_S / 4 fixed interleaving spur, independent of input signal	A_{IN} = –20 dBFS			–66	-50	dBFS
SPUR	Worst spur, excluding DC, HD2, HD3, f_S / 2, f_S / 4, f_S / 2 - f_{IN}, and f_S / 4 ± f_{IN}	f_{IN} = 347 MHz	A_{IN} = –1 dBFS		–70		dBFS
			A_{IN} = –3 dBFS		–71		
			A_{IN} = –12 dBFS		–71		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–70		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		–68		
			A_{IN} = –3 dBFS		–72		
			A_{IN} = –12 dBFS		–68		
		f_{IN} = 2397 MHz	A_{IN} = –1 dBFS		–73	-58	
			A_{IN} = –3 dBFS		–73		
			A_{IN} = –12 dBFS		–71		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–72		
		f_{IN} = 4197 MHz	A_{IN} = –1 dBFS		–68		
			A_{IN} = –3 dBFS		–71		
			A_{IN} = –12 dBFS		–68		
		f_{IN} = 5997 MHz	A_{IN} = –1 dBFS		–65		
			A_{IN} = –3 dBFS		–70		
			A_{IN} = –12 dBFS		–71		
		f_{IN} = 7597 MHz	A_{IN} = –1 dBFS		–67		
			A_{IN} = –3 dBFS		–71		
			A_{IN} = –12 dBFS		–72		

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6.8 Electrical Characteristics: AC Specifications (Single-Channel Mode) (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, input signal applied to INA±, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2 GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 6, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
IMD3	3rd-order intermodulation distortion	f_1 = 343 MHz, f_2 = 353 MHz	A_{IN} = –7 dBFS per tone		–77		dBFS
			A_{IN} = –9 dBFS per tone		–81		
			A_{IN} = –18 dBFS per tone		–77		
			A_{IN} = –9 dBFS per tone, V_{FS} = 1.0 V_{PP}		–82		
		f_1 = 993 MHz, f_2 = 1003 MHz	A_{IN} = –7 dBFS per tone		–80		
			A_{IN} = –9 dBFS per tone		–82		
			A_{IN} = –18 dBFS per tone		–73		
		f_1 = 2393 MHz, f_2 = 2403 MHz	A_{IN} = –7 dBFS per tone		–69		
			A_{IN} = –9 dBFS per tone		–70		
			A_{IN} = –18 dBFS per tone		–84		
			A_{IN} = –9 dBFS per tone, V_{FS} = 1.0 V_{PP}		–69		
		f_1 = 4193 MHz, f_2 = 4203 MHz	A_{IN} = –7 dBFS per tone		–68		
			A_{IN} = –9 dBFS per tone		–75		
			A_{IN} = –18 dBFS per tone		–73		
		f_1 = 5993 MHz, f_2 = 6003 MHz	A_{IN} = –7 dBFS per tone		-60		
			A_{IN} = –9 dBFS per tone		–67		
			A_{IN} = –18 dBFS per tone		–72		
		f_1 = 7593 MHz, f_2 = 7603 MHz	A_{IN} = –7 dBFS per tone		–49		
			A_{IN} = –9 dBFS per tone		–55		
			A_{IN} = –18 dBFS per tone		–81		

(1) Full-power input bandwidth (FPBW) is defined as the input frequency where the reconstructed output of the ADC has dropped 3 dB below the power of a full-scale input signal at a low input frequency. Useable bandwidth may exceed the –3-dB, full-power input bandwidth.

6.9 Timing Requirements

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2 GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 6, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the Recommended Operating Conditions table

			MIN	NOM	MAX	UNIT
DEVICE (SAMPLING) CLOCK (CLK+, CLK–)						
f_{CLK}	Input clock frequency (CLK±), both single-channel and dual-channel modes(1)		800		5200	MHz
t_{CLK}	Input clock period (CLK±), both single-channel and dual-channel modes(1)		192		1250	ps
SYSREF (SYSREF+, SYSREF–)						
$t_{INV(SYSREF)}$	Width of invalid SYSREF capture region of CLK± period, indicating setup or hold time violation, as measured by SYSREF_POS status register, SYSREF_ZOOM = 1(2)			48		ps
$t_{INV(TEMP)}$	Drift of invalid SYSREF capture region over temperature, positive number indicates a shift toward MSB of SYSREF_POS register, SYSREF_ZOOM = 1			0.02		ps/°C
$t_{INV(VA11)}$	Drift of invalid SYSREF capture region over VA11 supply voltage, positive number indicates a shift toward MSB of SYSREF_POS register, SYSREF_ZOOM = 1			-0.03		ps/mV
$t_{STEP(SP)}$	Delay of SYSREF_POS LSB(3)	SYSREF_ZOOM = 0		39		ps
		SYSREF_ZOOM = 1		24		
$t_{(PH\_SYS)}$	Minimum SYSREF± assertion duration with SYSREF Windowing after SYSREF± rising edge event			$5*T_{CLK}$ +4.5		ns
$t_{(PL\_SYS)}$	Minimum SYSREF± de-assertion duration with SYSREF Windowing after SYSREF± falling edge event			$5*T_{CLK}$ +4.5		ns
JESD204B SYNC TIMING ($\overline{SYNCSE}$ OR TMSTP±)						
$t_{(\overline{SYNCSE})}$	$\overline{SYNCSE}$ minimum assertion time to trigger link resynchronization			4		Frames
SERIAL PROGRAMMING INTERFACE (SCLK, SDI, $\overline{SCS}$)						
$f_{CLK(SCLK)}$	Serial clock frequency				15.625	MHz
$t_{(PH)}$	Serial clock high value pulse duration		32			ns
$t_{(PL)}$	Serial clock low value pulse duration		32			ns
$t_{SU(\overline{SCS})}$	Setup time from $\overline{SCS}$ to rising edge of SCLK		30			ns
$t_{H(\overline{SCS})}$	Hold time from rising edge of SCLK to $\overline{SCS}$		30			ns
$t_{SU(SDI)}$	Setup time from SDI to rising edge of SCLK		25			ns
$t_{H(SDI)}$	Hold time from rising edge of SCLK to SDI		3			ns

(1) Unless functionally limited to a smaller range in the Operating Modes table based on programmed JMODE.

(2) Use SYSREF_POS to select an optimal SYSREF_SEL value for the SYSREF capture, see the *SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing)* section for more information on SYSREF windowing. The invalid region, specified by $t_{INV(SYSREF)}$, indicates the portion of the CLK± period(t_{CLK}), as measured by SYSREF_SEL, that may result in a setup and hold violation. Verify that the timing skew between SYSREF± and CLK± over system operating conditions from the nominal conditions (that used to find optimal SYSREF_SEL) does not result in the invalid region occurring at the selected SYSREF_SEL position in SYSREF_POS, otherwise a temperature dependent SYSREF_SEL selection may be needed to track the skew between CLK± and SYSREF±.

(3) It is recommended to use SYSREF_ZOOM = 0 below f_{CLK} = 3GHz and SYSREF_ZOOM = 1 above f_{CLK} = 3GHz

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6.10 Switching Characteristics

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2 GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 6, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE (SAMPLING) CLOCK (CLK+, CLK–)						
t_{AD}	Sampling (aperture) delay from the CLK± rising edge (dual-channel mode) or rising and falling edge (single-channel mode) to sampling instant	TAD_COARSE = 0x00, TAD_FINE = 0x00, and TAD_INV = 0		360		ps
$t_{TAD(MAX)}$	Maximum t_{AD} adjust programmable delay, not including clock inversion (TAD_INV = 0)	Coarse adjustment (TAD_COARSE = 0xFF)		289		ps
		Fine adjustment (TAD_FINE = 0xFF)		4.9		ps
$t_{TAD(STEP)}$	t_{AD} adjust programmable delay step size	Coarse adjustment (TAD_COARSE)		1.13		ps
		Fine adjustment (TAD_FINE)		19		fs
t_{AJ}	Aperture jitter, rms	Minimum t_{AD} adjust coarse setting (TAD_COARSE = 0x00, TAD_INV = 0), dither disabled (ADC_DITH_EN = 0)		50		fs
t_{AJ}	Aperture jitter, rms	Minimum t_{AD} adjust coarse setting (TAD_COARSE = 0x00, TAD_INV = 0), dither enabled (ADC_DITH_EN = 1)		60		fs
t_{AJ}	Aperture jitter, rms	Maximum t_{AD} adjust coarse setting (TAD_COARSE = 0xFF) excluding TAD_INV (TAD_INV = 0), dither disabled (ADC_DITH_EN = 0)		65[3]		fs
t_{AJ}	Aperture jitter, rms	Maximum t_{AD} adjust coarse setting (TAD_COARSE = 0xFF) excluding TAD_INV (TAD_INV = 0), dither enabled (ADC_DITH_EN = 1)		74[3]		fs
SERIAL DATA OUTPUTS (DA[7:0]+, DA[7:0]–, DB[7:0]+, DB[7:0]–)						
f_{SERDES}	Serialized output bit rate		1		17.16	Gbps
UI	Serialized output unit interval		58.2		1000	ps
t_{TLH}	Low-to-high transition time (differential)	20% to 80%, 8H8L test pattern, 13.0 Gbps		18.6		ps
t_{THL}	High-to-low transition time (differential)	20% to 80%, 8H8L test pattern, 13.0 Gbps		18.4		ps
DDJ	Data dependent jitter, peak-to-peak	PRBS-7 test pattern, JMODE = 5, 13.0 Gbps		7.1		ps
DDJ	Data dependent jitter, peak-to-peak	PRBS-9 test pattern, JMODE = 44, 10.725 Gbps		7.1		ps
DCD	Even-odd jitter, peak-to-peak	PRBS-7 test pattern, JMODE = 5, 13.0 Gbps		0.22		ps
DCD	Even-odd jitter, peak-to-peak	PRBS-9 test pattern, JMODE = 44, 10.725 Gbps		0.06		ps
EBUJ	Effective bounded uncorrelated jitter, peak-to-peak	PRBS-7 test pattern, JMODE = 5, 13.0 Gbps		1.7		ps
EBUJ	Effective bounded uncorrelated jitter, peak-to-peak	PRBS-9 test pattern, JMODE = 44, 10.725 Gbps		0.30		ps
RJ	Unbounded random jitter, RMS	8H8L test pattern, JMODE = 5, 13.0 Gbps		0.75		ps
RJ	Unbounded random jitter, RMS	8H8L test pattern, JMODE = 44, 10.725 Gbps		1.1		ps
TJ	Total jitter, peak-to-peak, with unbounded random jitter portion defined with respect to a BER = 1e-15 (Q = 7.94)	PRBS-7 test pattern, JMODE = 5, 13.0 Gbps		18.5		ps
TJ	Total jitter, peak-to-peak, with unbounded random jitter portion defined with respect to a BER = 1e-15 (Q = 7.94)	PRBS-9 test pattern, JMODE = 44, 10.725 Gbps		25.4		ps

6.10 Switching Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2 GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 6, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC CORE LATENCY						
t_{ADC}	Deterministic delay from the CLK± edge that samples the reference sample to the CLK± edge that samples SYSREF going high[1]	JMODE = 5, 44		-9.5		t_{CLK} cycles
		JMODE = 7		-10		t_{CLK} cycles
		JMODE = 6, 50		-13.5		t_{CLK} cycles
		JMODE = 8, 51		-14		t_{CLK} cycles
		JMODE = 34		6.5		t_{CLK} cycles
		JMODE = 35		6		t_{CLK} cycles
		JMODE = 45		-10.0		t_{CLK} cycles

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6.10 Switching Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2 GHz, filtered 1-V_{PP} sine-wave clock, JMODE = 6, Dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
JESD204C AND SERIALIZER LATENCY						
t_{TX}	Delay from the CLK± rising edge that samples SYSREF high to the first bit of the multiframe (8B/10B encoding) or extended multiblock (64B/66B encoding) on the JESD204C serial output lane corresponding to the reference sample of t_{ADC} (2)	JMODE = 5	143		168	t_{CLK} cycles
		JMODE = 6, 8	191		215	
		JMODE = 7	143		168	
		JMODE = 34	102		119	
		JMODE = 35	103		119	
		JMODE = 44, 45	179		202	
		JMODE = 50	267		291	
		JMODE = 51	268		291	
SERIAL PROGRAMMING INTERFACE (SDO)						
$t_{(OZD)}$	Delay from the falling edge of the 16th SCLK cycle during read operation for SDO transition from tri-state to valid data		1			ns
$t_{(ODZ)}$	Delay from the $\overline{SCS}$ rising edge for SDO transition from valid data to tri-state				10	ns
$t_{(OD)}$	Delay from the falling edge of SCLK during read operation to SDO valid		1		12	ns

(1) t_{ADC} is an exact, unrounded, deterministic delay. The delay can be negative if the reference sample is sampled after the SYSREF high capture point, in which case the total latency is smaller than the delay given by t_{TX}.

(2) The values given for t_{TX} include deterministic and non-deterministic delays. Over process, temperature, and voltage, the delay will vary. JESD204B accounts for these variations when operating in subclass-1 mode in order to achieve deterministic latency. Proper receiver RBD values must be chosen such that the elastic buffer release point does not occur within the invalid region of the local multiframe clock (LMFC) cycle.

(3) t_{AJ} increases because of additional attenuation on the internal clock path.

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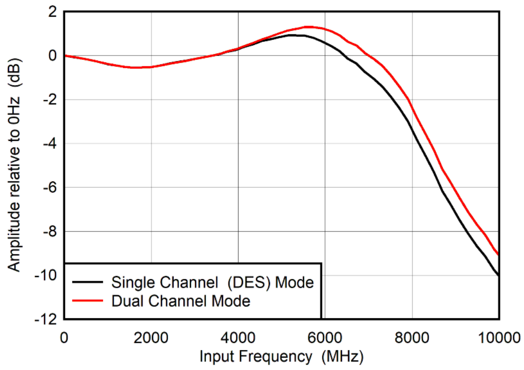
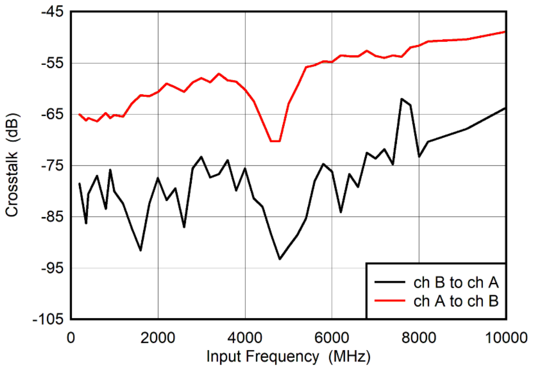
6.11 Typical Characteristics

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs



Relative to 0 Hz, FG calibration

図 6-1. Input Amplitude vs Input Frequency



Dual channel mode, JMODE 8

図 6-2. Crosstalk vs Input Frequency

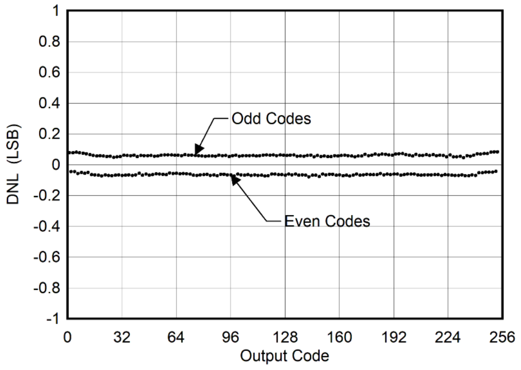


図 6-3. DNL vs ADC Code

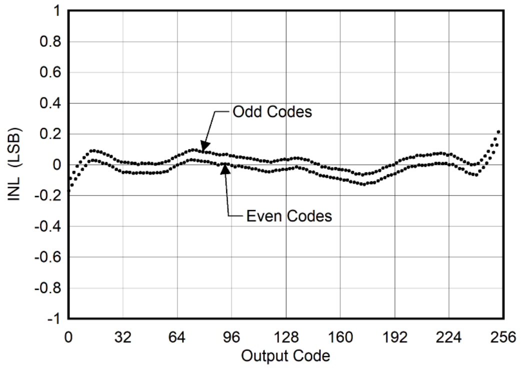


図 6-4. INL vs ADC Code

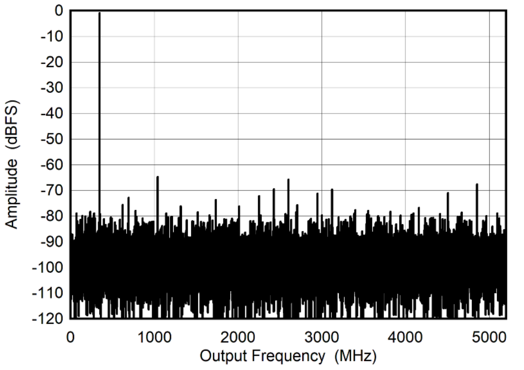


図 6-5. DES Mode: Single Tone FFT at 347 MHz

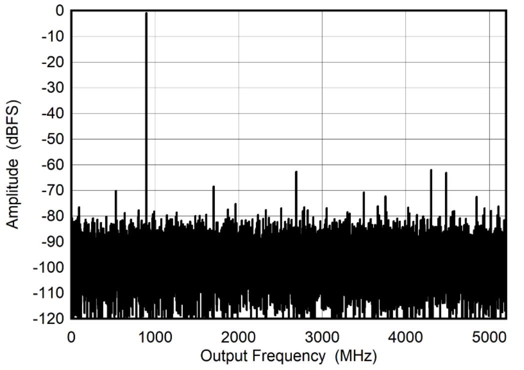


図 6-6. DES Mode: Single Tone FFT at 897 MHz

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6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs

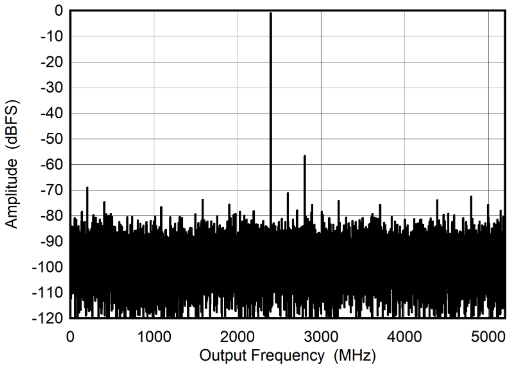


図 6-7. DES Mode: Single Tone FFT at 2397 MHz

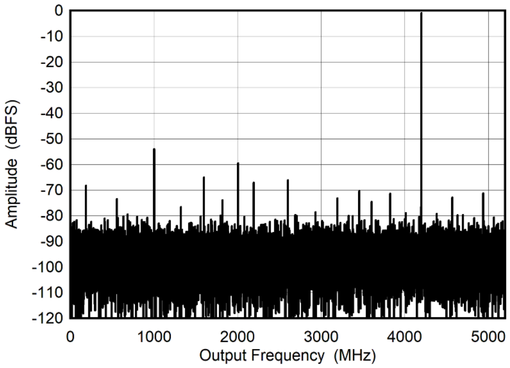


図 6-8. DES Mode: Single Tone FFT at 4197 MHz

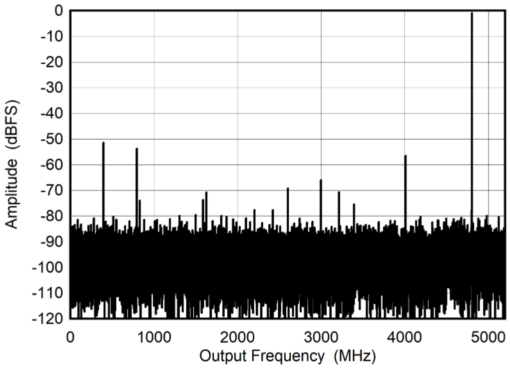


図 6-9. DES Mode: Single Tone FFT at 5597 MHz

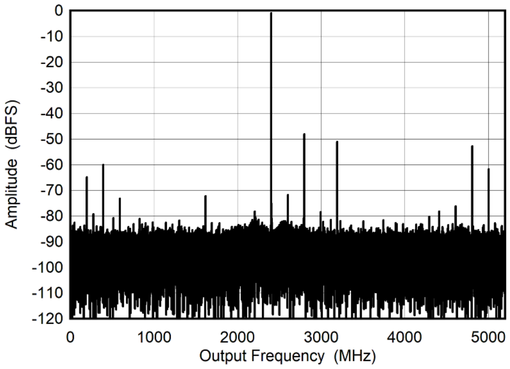
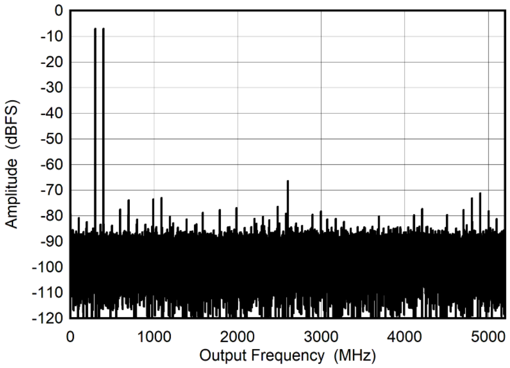
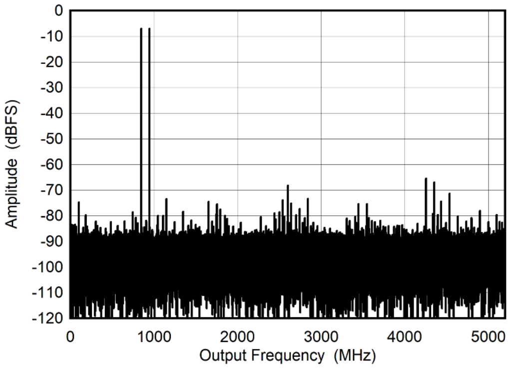


図 6-10. DES Mode: Single Tone FFT at 7997 MHz



each tone at -7 dBFS, 100 MHz Tone Spacing

図 6-11. DES Mode: Two Tone FFT at 347 MHz



each tone at -7 dBFS, 100 MHz Tone Spacing

図 6-12. DES Mode: Two Tone FFT at 897 MHz

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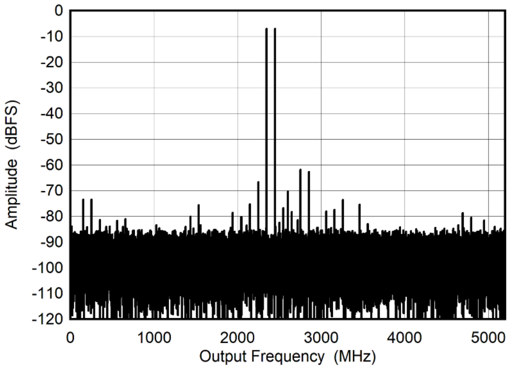
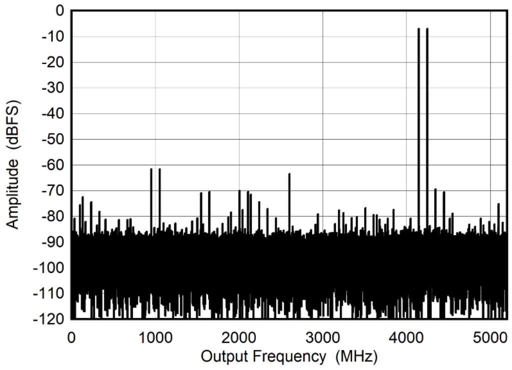
6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs



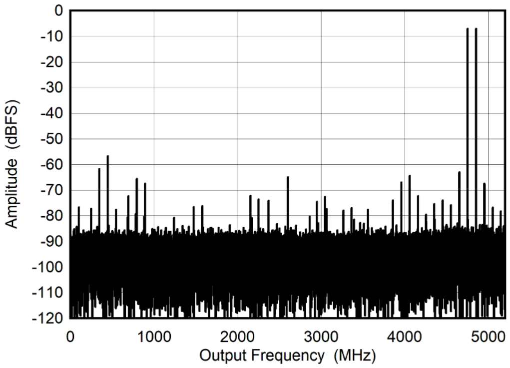
each tone at -7 dBFS, 100 MHz Tone Spacing

図 6-13. DES Mode: Two Tone FFT at 2397 MHz



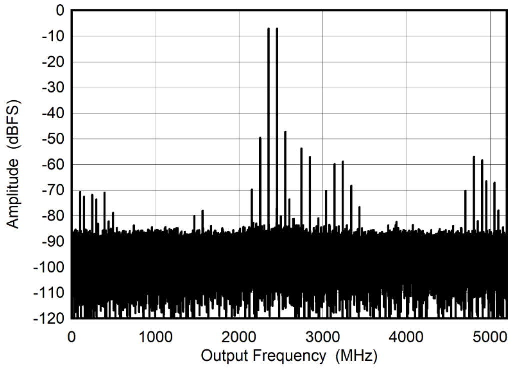
each tone at -7dBFS, 100MHz Tone Spacing

図 6-14. DES Mode: Two Tone FFT at 4197 MHz



each tone at -7 dBFS, 100 MHz Tone Spacing

図 6-15. DES Mode: Two Tone FFT at 5597 MHz



each tone at -7 dBFS, 100 MHz Tone Spacing

図 6-16. DES Mode: Two Tone FFT at 7997 MHz

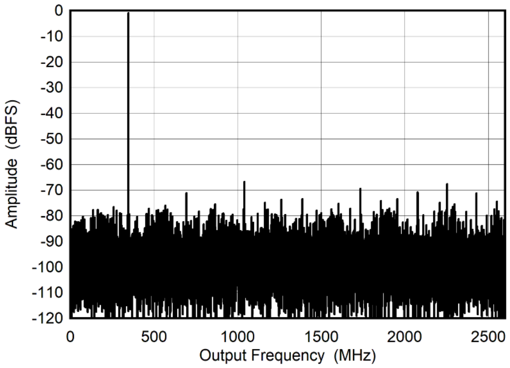


図 6-17. Dual Channel Mode: Single Tone FFT at 347 MHz

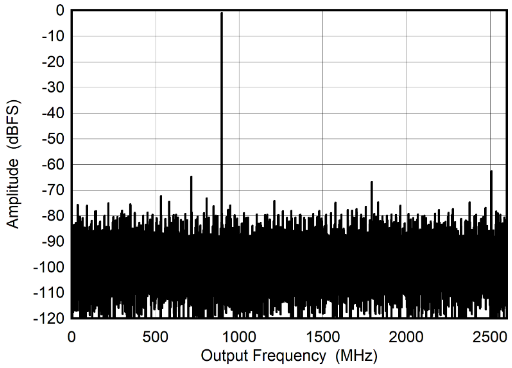


図 6-18. Dual Channel Mode: Single Tone FFT at 897 MHz

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6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs

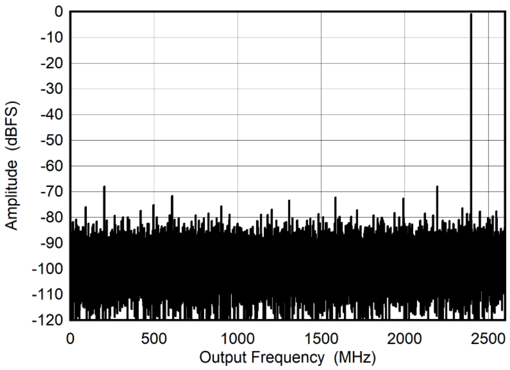


図 6-19. Dual Channel Mode: Single Tone FFT at 2397 MHz

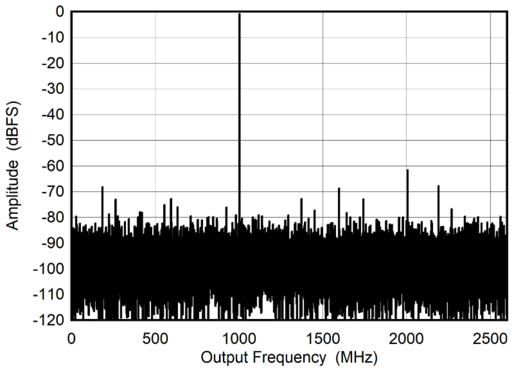


図 6-20. Dual Channel Mode: Single Tone FFT at 4197 MHz

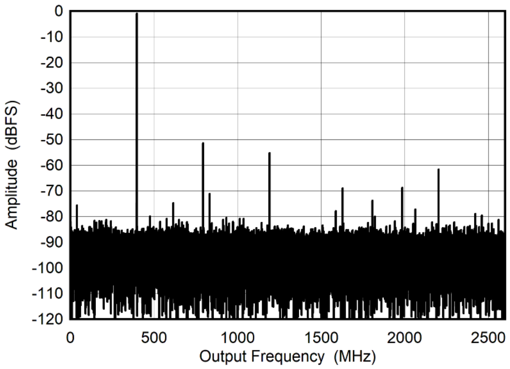


図 6-21. Dual Channel Mode: Single Tone FFT at 5597 MHz

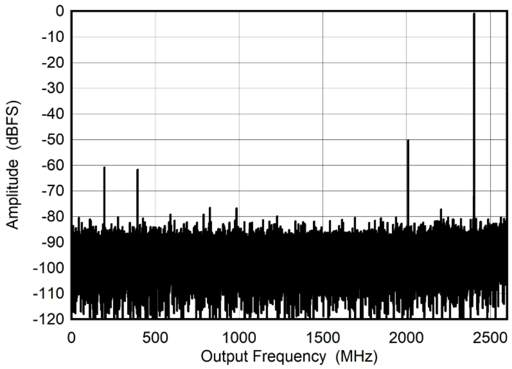
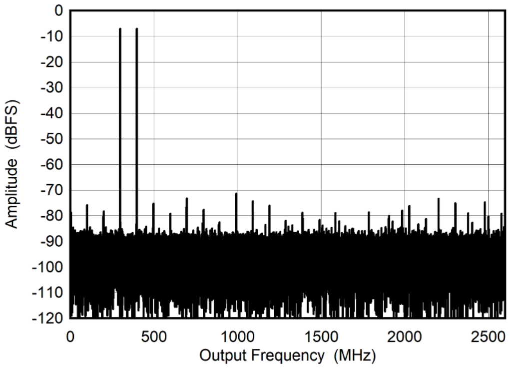
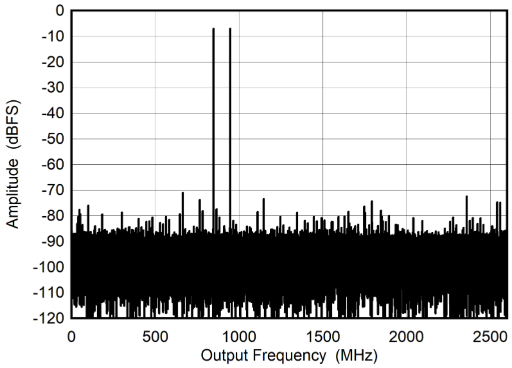


図 6-22. Dual Channel Mode: Single Tone FFT at 7997 MHz



each tone at -7 dBFS, 100 MHz Tone Spacing

図 6-23. Dual Channel Mode: Two Tone FFT at 347 MHz



each tone at -7 dBFS, 100 MHz Tone Spacing

図 6-24. Dual Channel Mode: Two Tone FFT at 897 MHz

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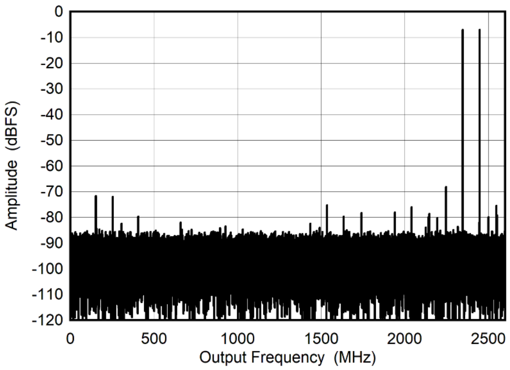
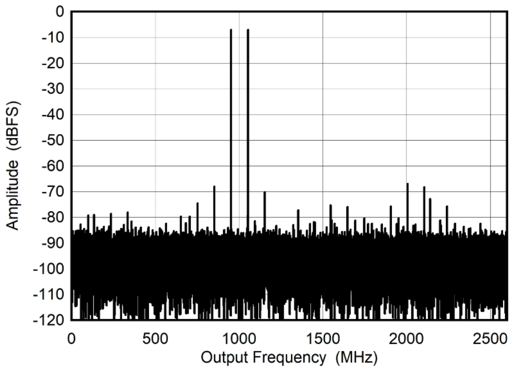
6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs



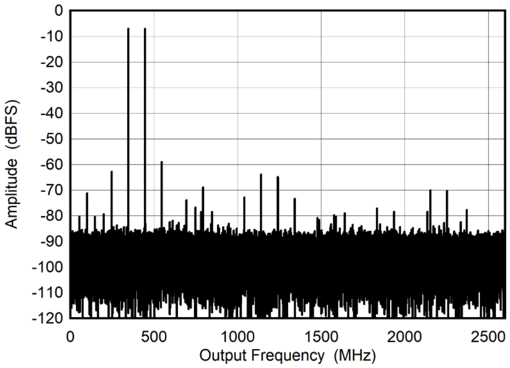
each tone at -7 dBFS, 100 MHz Tone Spacing

図 6-25. Dual Channel Mode: Two Tone FFT at 897 MHz



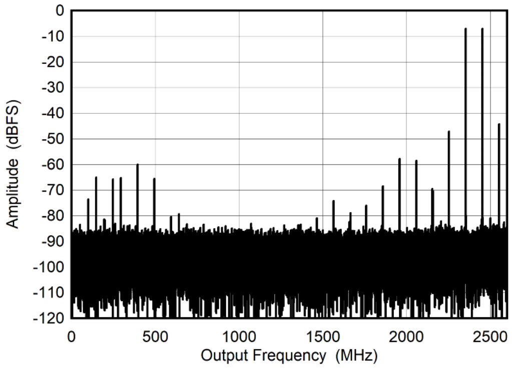
each tone at -7 dBFS, 100 MHz Tone Spacing

図 6-26. Dual Channel Mode: Two Tone FFT at 4197 MHz



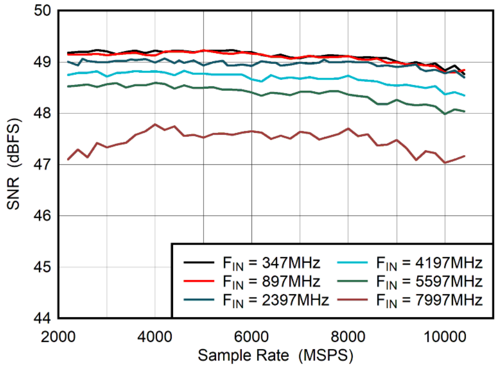
each tone at -7 dBFS, 100 MHz Tone Spacing

図 6-27. Dual Channel Mode: Two Tone FFT at 5597 MHz



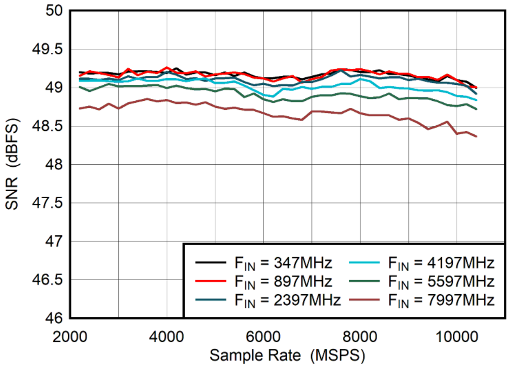
each tone at -7 dBFS, 100 MHz Tone Spacing

図 6-28. Dual Channel Mode: Two Tone FFT at 7997 MHz



A_{IN} = -1 dBFS

図 6-29. DES Mode: SNR vs Sample Rate



A_{IN} = -6 dBFS

図 6-30. DES Mode: SNR vs Sample Rate

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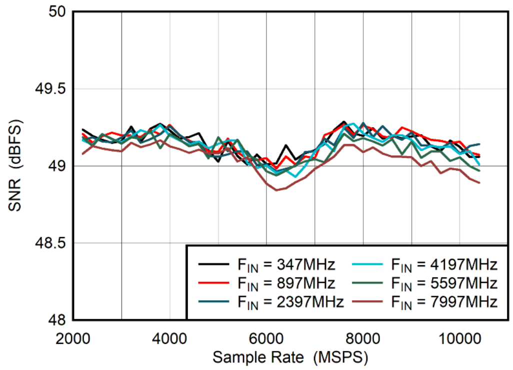
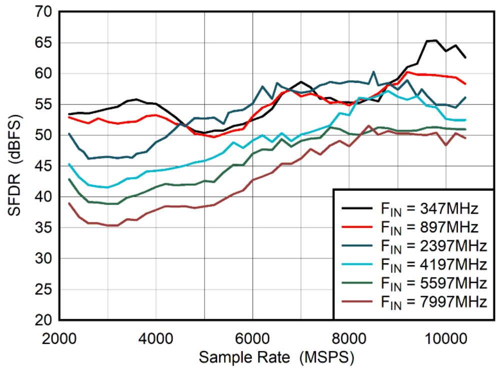
6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs



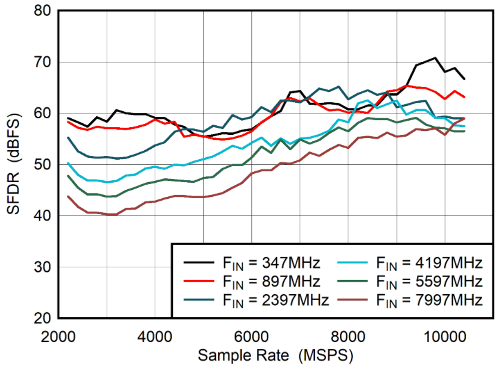
A_{IN} = -12 dBFS

図 6-31. DES Mode: SNR vs Sample Rate



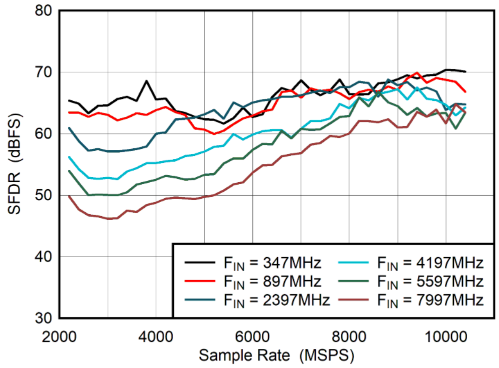
A_{IN} = -1 dBFS

図 6-32. DES Mode: SFDR vs Sample Rate



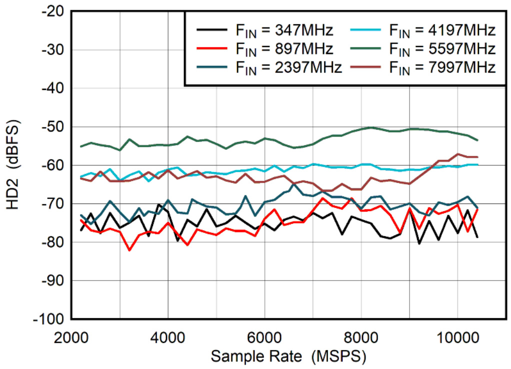
A_{IN} = -6 dBFS

図 6-33. DES Mode: SFDR vs Sample Rate



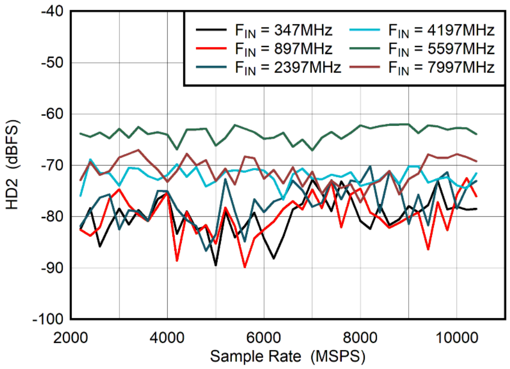
A_{IN} = -12 dBFS

図 6-34. DES Mode: SFDR vs Sample Rate



A_{IN} = -1 dBFS

図 6-35. DES Mode: HD2 vs Sample Rate

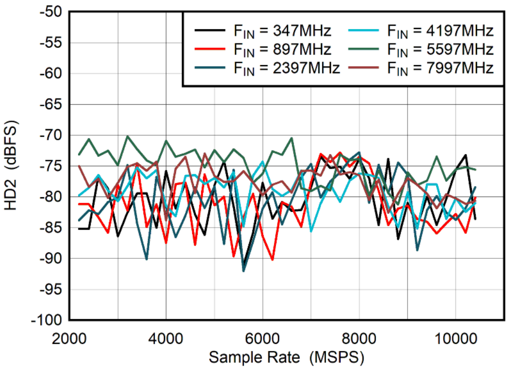


A_{IN} = -6 dBFS

図 6-36. DES Mode: HD2 vs Sample Rate

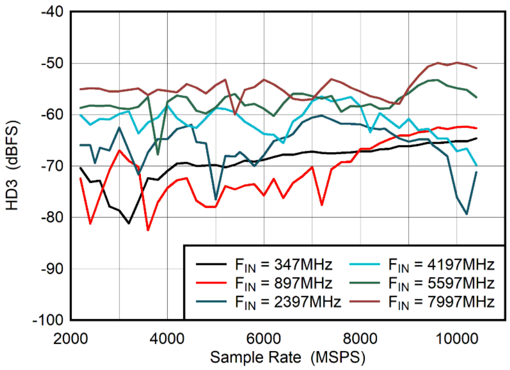
6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs



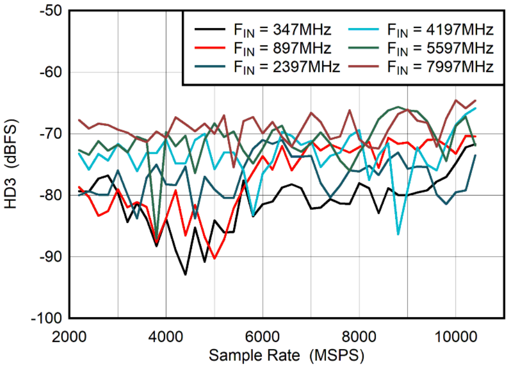
A_{IN} = -12 dBFS

図 6-37. DES Mode: HD2 vs Sample Rate



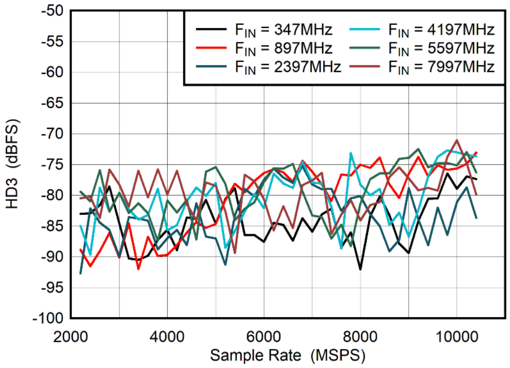
A_{IN} = -1 dBFS

図 6-38. DES Mode: HD3 vs Sample Rate



A_{IN} = -6 dBFS

図 6-39. DES Mode: HD3 vs Sample Rate



A_{IN} = -12 dBFS

図 6-40. DES Mode: HD3 vs Sample Rate

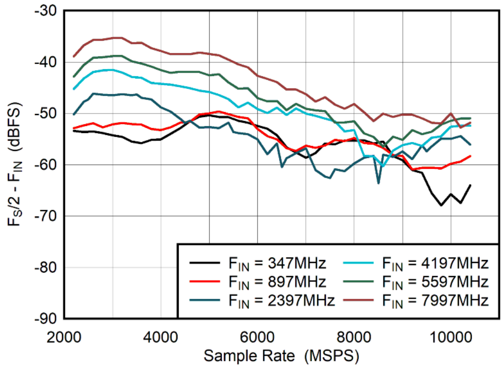


図 6-41. DES Mode: $F_S/2$ - F_{IN} vs Sample Rate

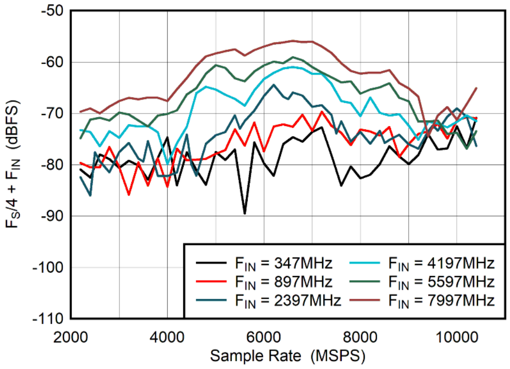


図 6-42. DES Mode: $F_S/4$ + F_{IN} vs Sample Rate

6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs

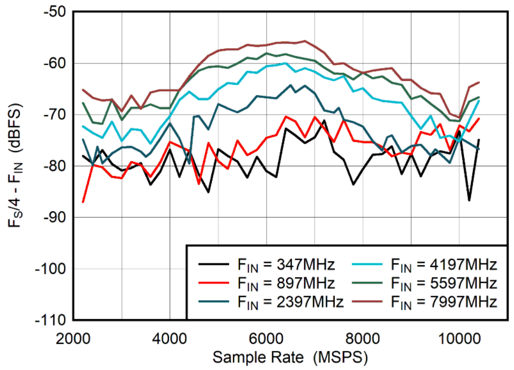
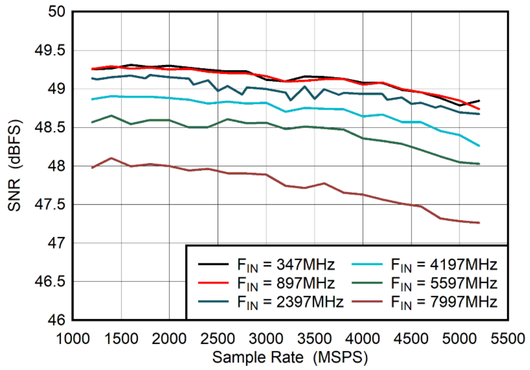
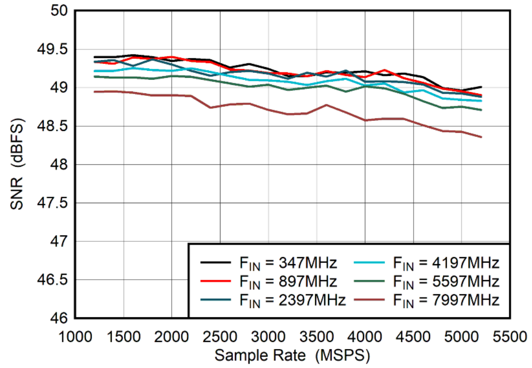


図 6-43. DES Mode: $F_S/4$ - F_{IN} vs Sample Rate



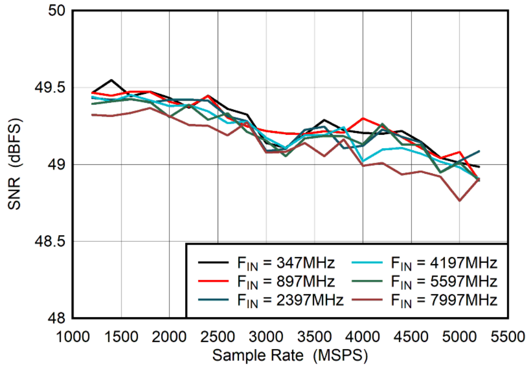
A_{IN} = -1 dBFS

図 6-44. Dual Channel Mode: SNR vs Sample Rate



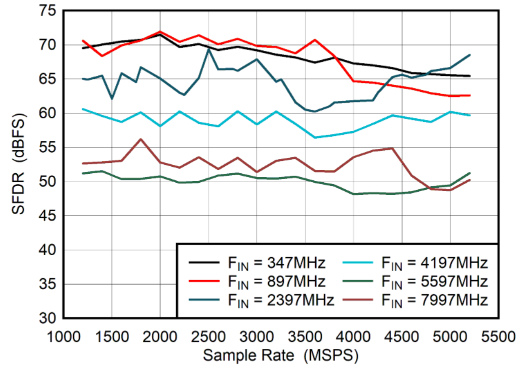
A_{IN} = -6 dBFS

図 6-45. Dual Channel Mode: SNR vs Sample Rate



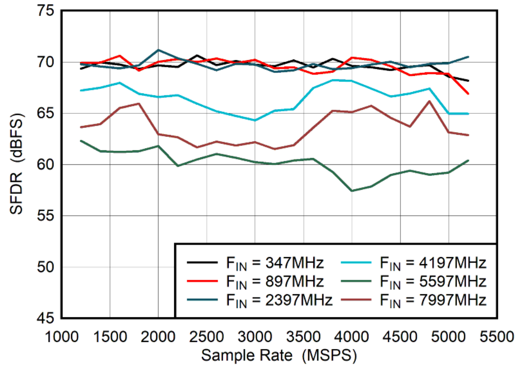
A_{IN} = -12 dBFS

図 6-46. Dual Channel Mode: SNR vs Sample Rate



A_{IN} = -1 dBFS

図 6-47. Dual Channel Mode: SFDR vs Sample Rate



A_{IN} = -6 dBFS

図 6-48. Dual Channel Mode: SFDR vs Sample Rate

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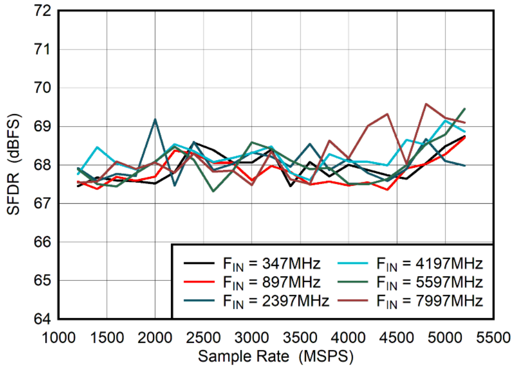
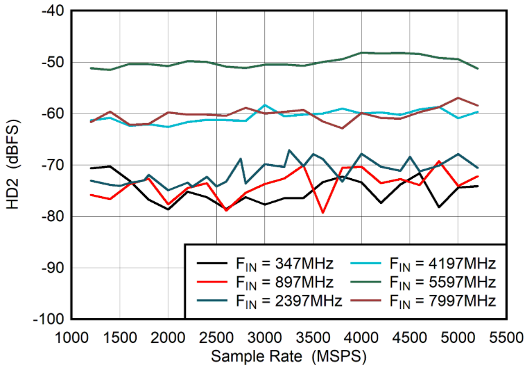
6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs



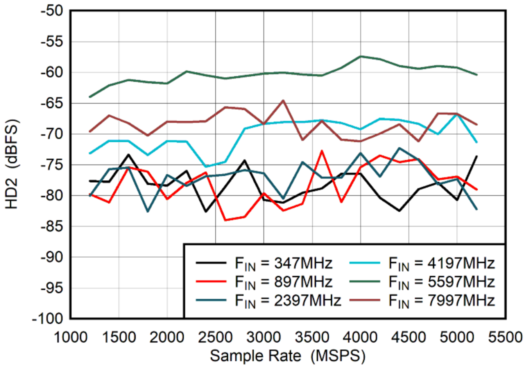
A_{IN} = -12 dBFS

図 6-49. Dual Channel Mode: SFDR vs Sample Rate



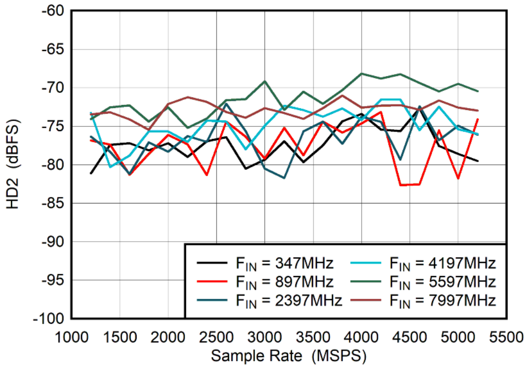
A_{IN} = -1 dBFS

図 6-50. Dual Channel Mode: HD2 vs Sample Rate



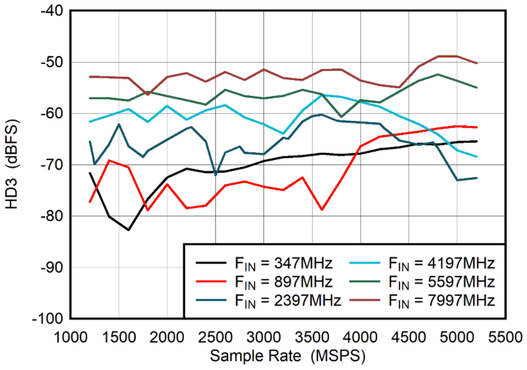
A_{IN} = -6 dBFS

図 6-51. Dual Channel Mode: HD2 vs Sample Rate



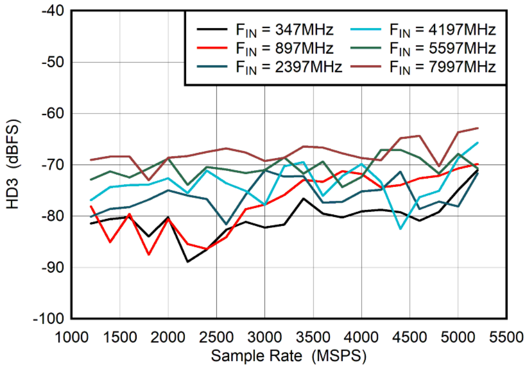
A_{IN} = -12 dBFS

図 6-52. Dual Channel Mode: HD2 vs Sample Rate



A_{IN} = -1 dBFS

図 6-53. Dual Channel Mode: HD3 vs Sample Rate



A_{IN} = -6 dBFS

図 6-54. Dual Channel Mode: HD3 vs Sample Rate

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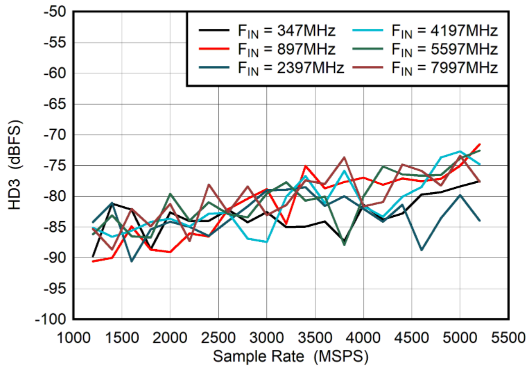
6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs



A_{IN} = -12 dBFS

図 6-55. Dual Channel Mode: HD3 vs Sample Rate

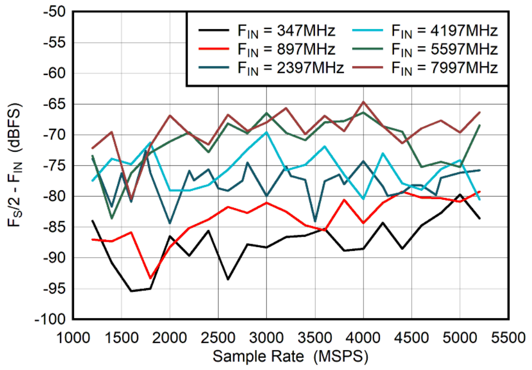


図 6-56. Dual Channel Mode: $F_S/2$ - F_{IN} vs Sample Rate

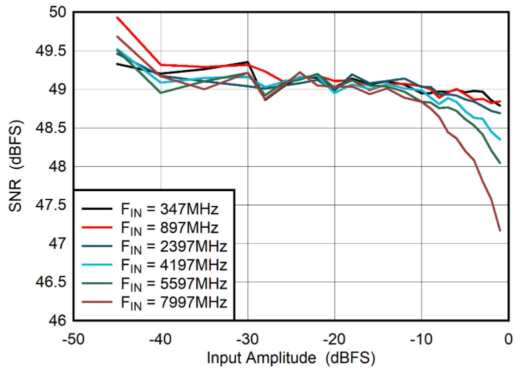


図 6-57. DES Mode: SNR vs Input Amplitude

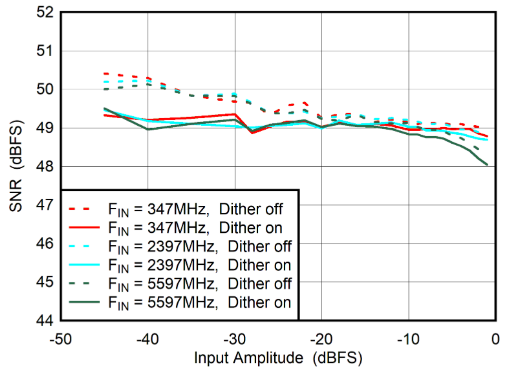


図 6-58. DES Mode: SNR vs Input Amplitude and Dither

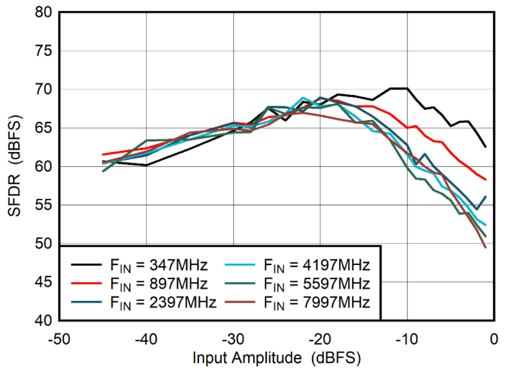


図 6-59. DES Mode: SFDR vs Input Amplitude

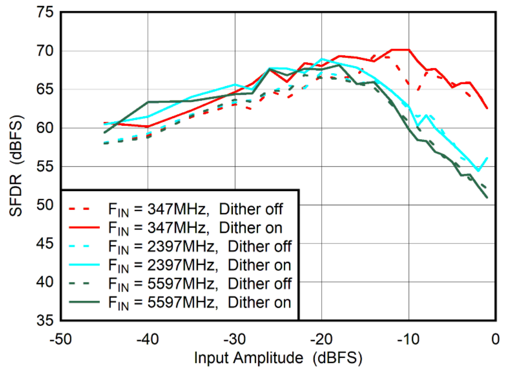


図 6-60. DES Mode: SFDR vs Input Amplitude and Dither

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6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs

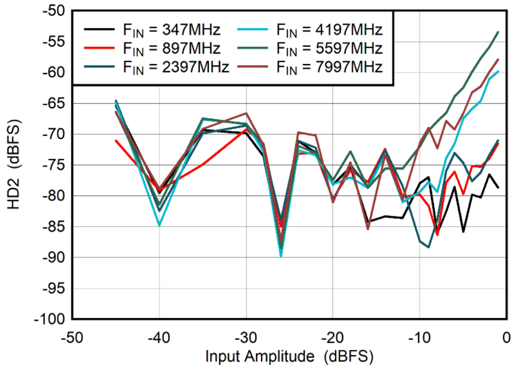

図 6-61. DES Mode: HD2 vs Input Amplitude

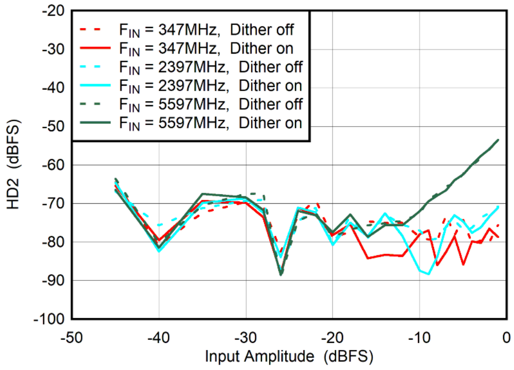

図 6-62. DES Mode: HD2 vs Input Amplitude and Dither

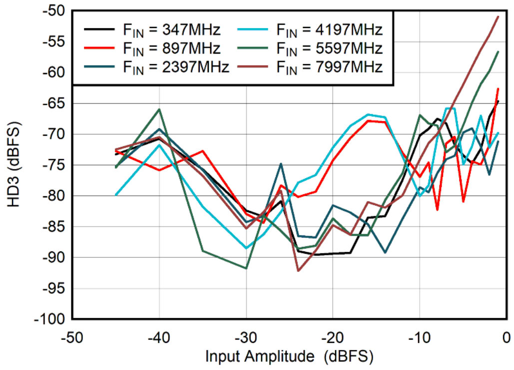

図 6-63. DES Mode: HD3 vs Input Amplitude

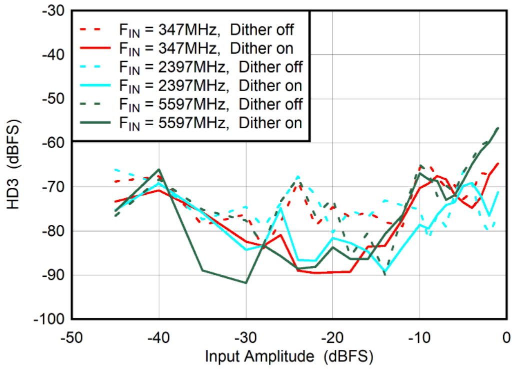

図 6-64. DES Mode: HD3 vs Input Amplitude and Dither

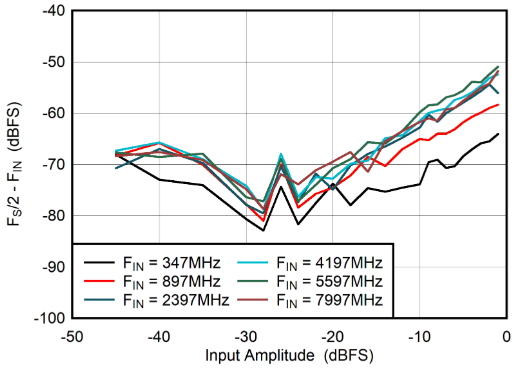

図 6-65. DES Mode: $F_S/2$ - F_{IN} vs Input Amplitude

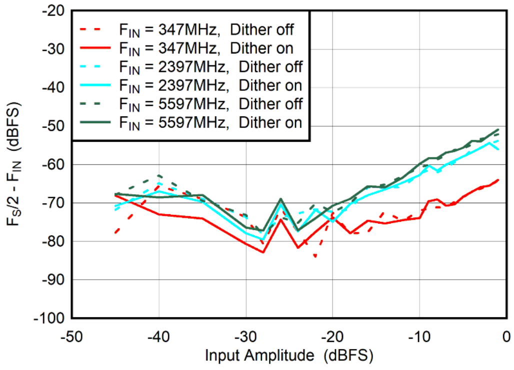

図 6-66. DES Mode: $F_S/2$ - F_{IN} vs Input Amplitude and Dither

6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs

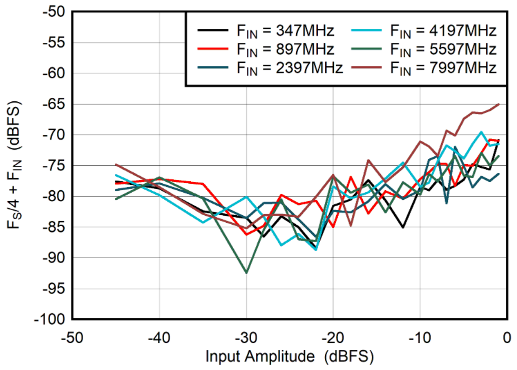

図 6-67. DES Mode: $F_S/4 + F_{IN}$ vs Input Amplitude

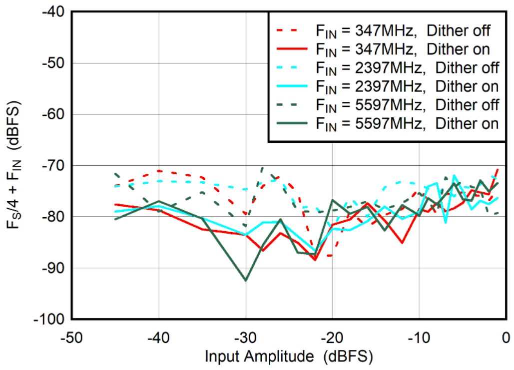

図 6-68. DES Mode: $F_S/4 + F_{IN}$ vs Input Amplitude and Dither

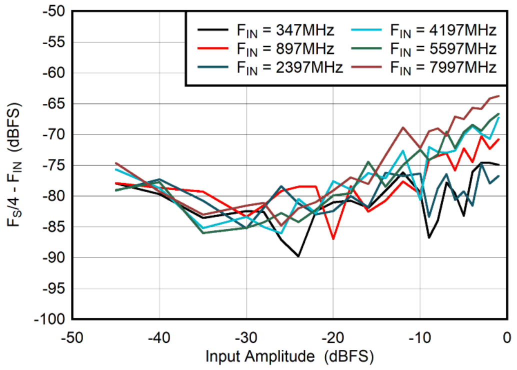

図 6-69. DES Mode: $F_S/4 - F_{IN}$ vs Input Amplitude

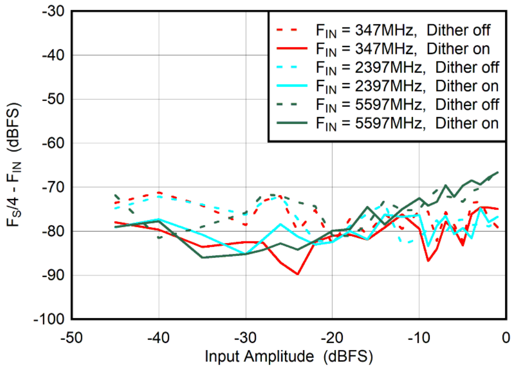

図 6-70. DES Mode: $F_S/4 - F_{IN}$ vs Input Amplitude and Dither

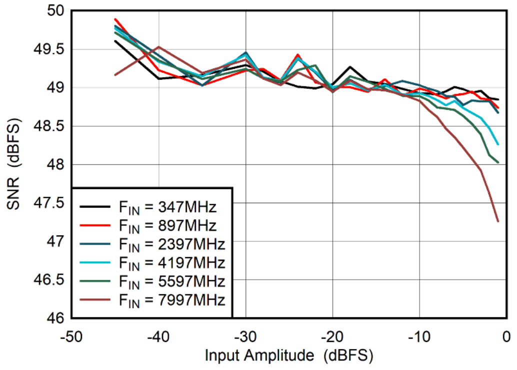

図 6-71. Dual Channel Mode: SNR vs Input Amplitude

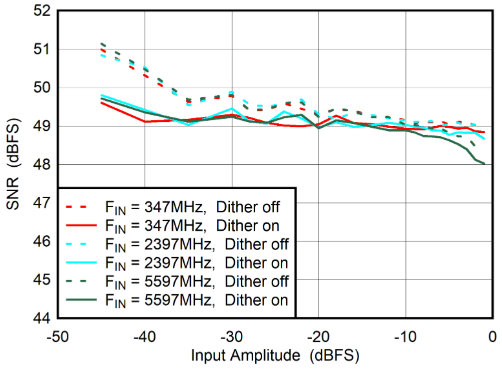

図 6-72. Dual Channel Mode: SNR vs Input Amplitude and Dither

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6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs

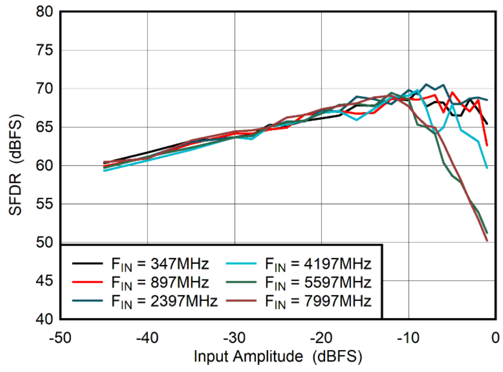

図 6-73. Dual Channel Mode: SFDR vs Input Amplitude

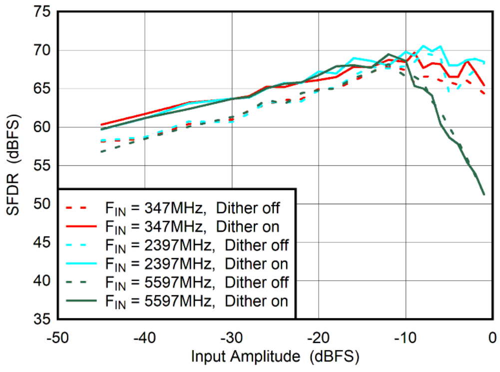

図 6-74. Dual Channel Mode: SFDR vs Input Amplitude and Dither

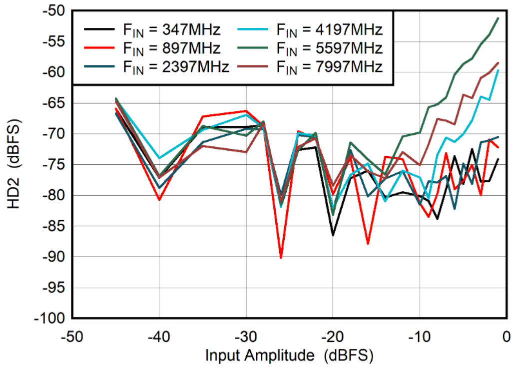

図 6-75. Dual Channel Mode: HD2 vs Input Amplitude

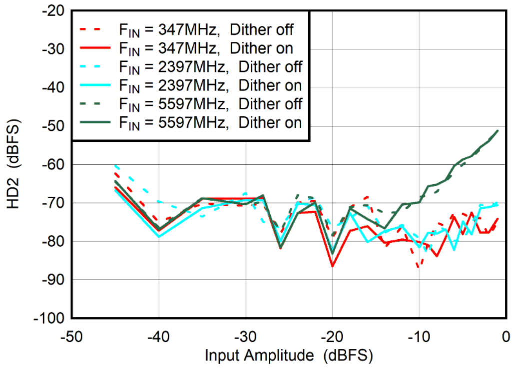

図 6-76. Dual Channel Mode: HD2 vs Input Amplitude and Dither

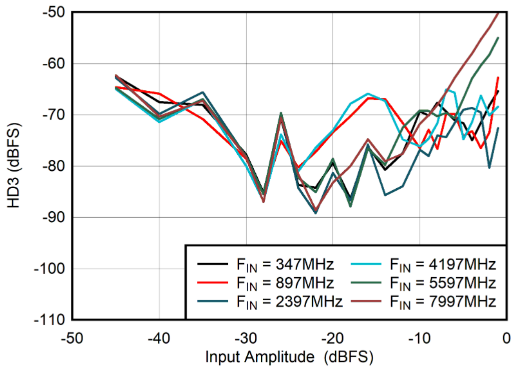

図 6-77. Dual Channel Mode: HD3 vs Input Amplitude

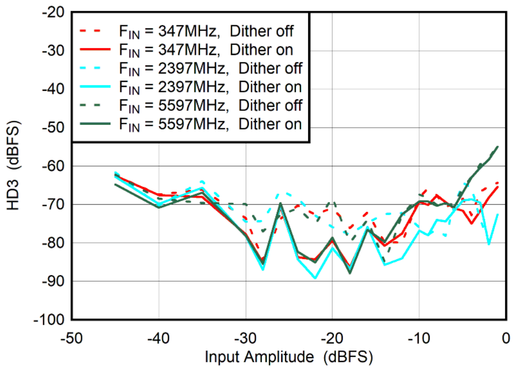

図 6-78. Dual Channel Mode: HD3 vs Input Amplitude and Dither

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6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs

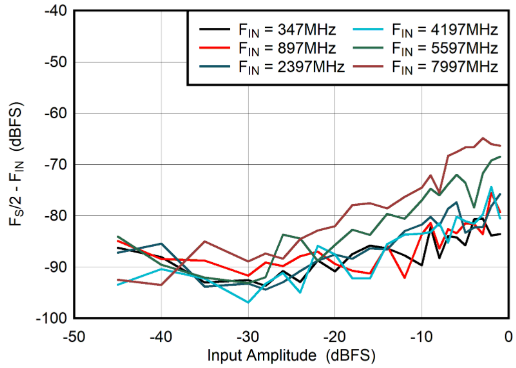

図 6-79. Dual Channel Mode: $F_S/2 - F_{IN}$ vs Input Amplitude

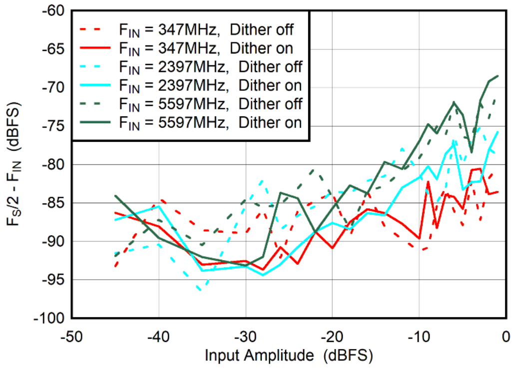

図 6-80. Dual Channel Mode: $F_S/2 - F_{IN}$ vs Input Amplitude and Dither

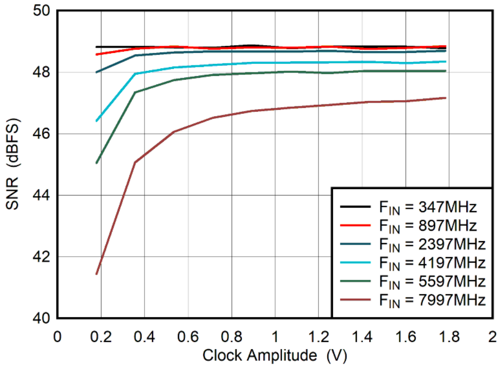

図 6-81. DES Mode: SNR vs Clock Amplitude

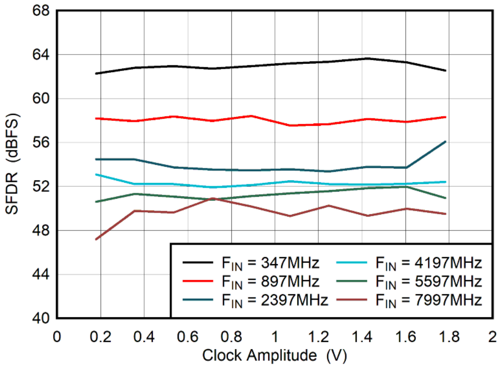

図 6-82. DES Mode: SFDR vs Clock Amplitude

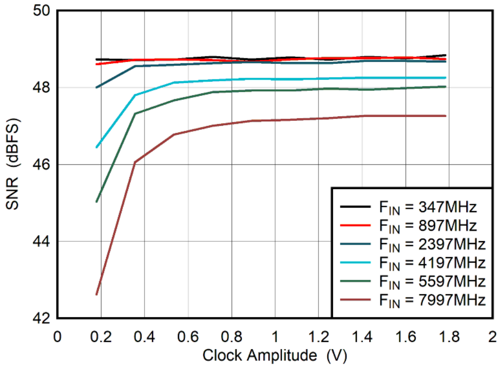

図 6-83. Dual Channel Mode: SNR vs Clock Amplitude

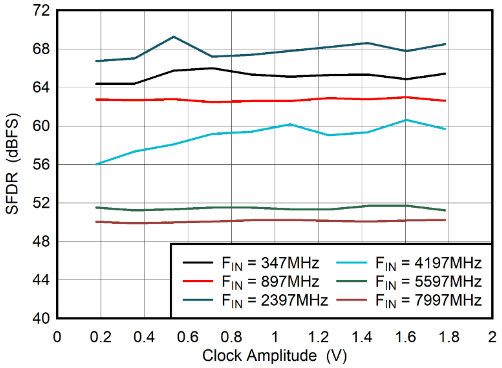

図 6-84. Dual Channel Mode: SFDR vs Clock Amplitude

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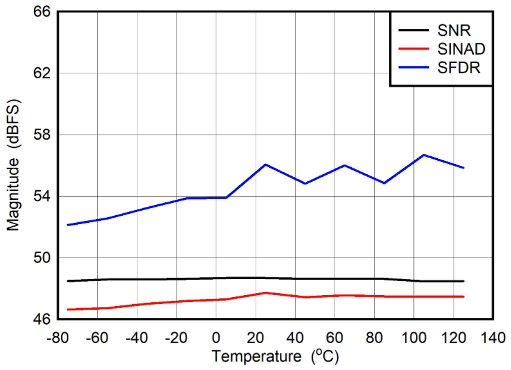
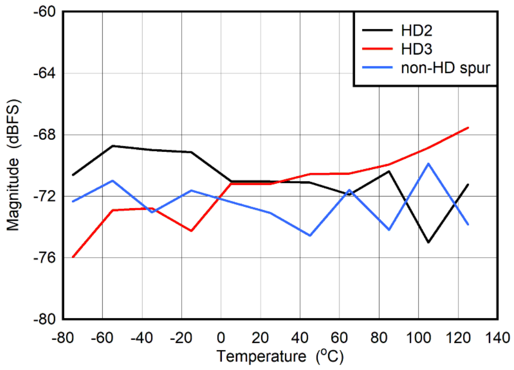
6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs



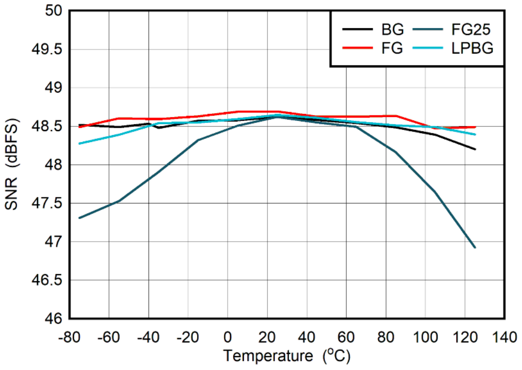
FG calibration at each temperature

図 6-85. DES Mode: SNR, SINAD and SFDR vs Temperature



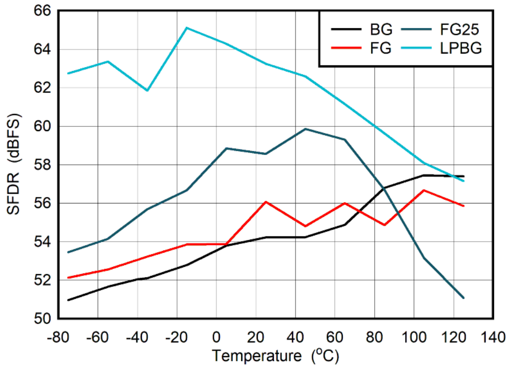
FG calibration at each temperature

図 6-86. DES Mode: HD2, HD3 and Worst Spur vs Temperature



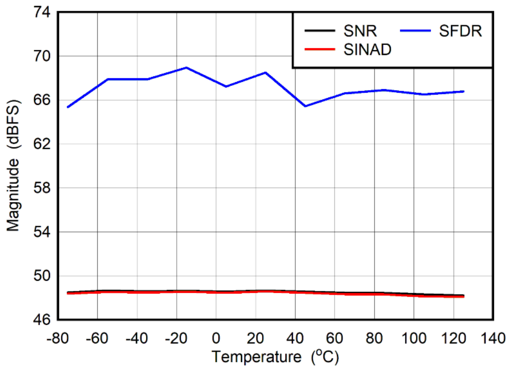
FG25 is calibrated at 25°C and held at other temperatures, other modes recalibrated at each temperature

図 6-87. DES Mode: SNR vs Temperature and Calibration



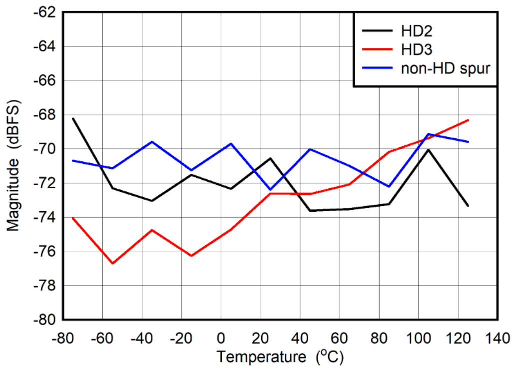
FG25 is calibrated at 25°C and held at other temperatures, other modes recalibrated at each temperature

図 6-88. DES Mode: SFDR vs Temperature and Calibration



FG calibration at each temperature

図 6-89. Dual Channel Mode: SNR, SINAD and SFDR vs Temperature



FG calibration at each temperature

図 6-90. Dual Channel Mode: HD2, HD3 and Worst Spur vs Temperature

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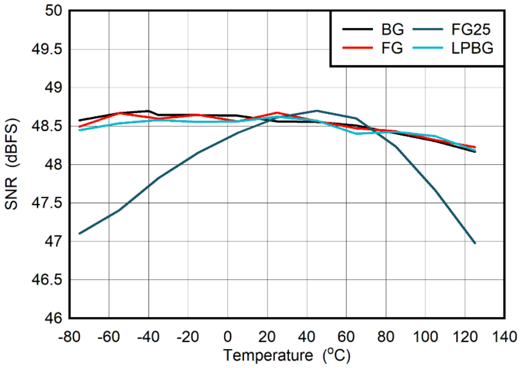
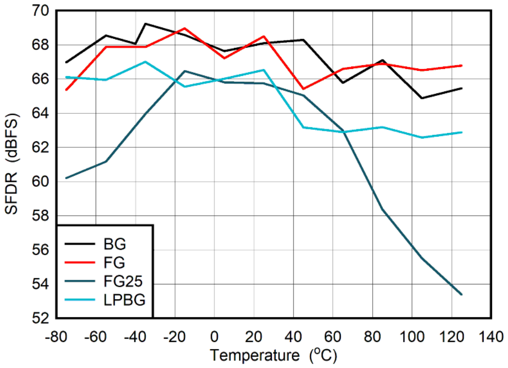
6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs



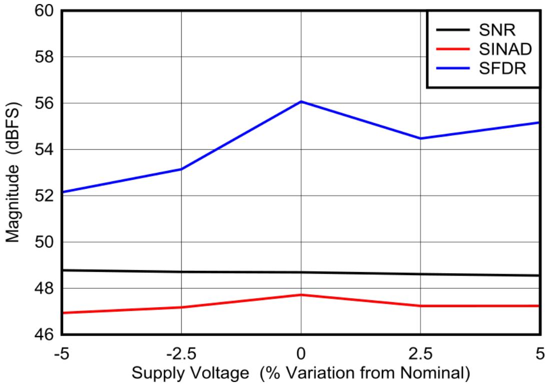
FG25 is calibrated at 25°C and held at other temperatures, other modes recalibrated at each temperature

図 6-91. Dual Channel Mode: SNR vs Temperature and Calibration



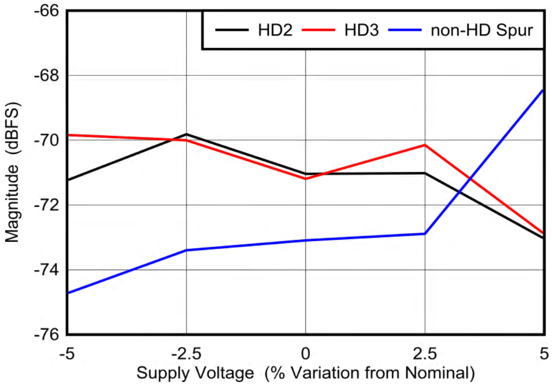
FG25 is calibrated at 25°C and held at other temperatures, other modes recalibrated at each temperature

図 6-92. Dual Channel Mode: SFDR vs Temperature and Calibration



All supplies varied together

図 6-93. DES Mode: SNR, SINAD and SFDR vs Supply Voltage

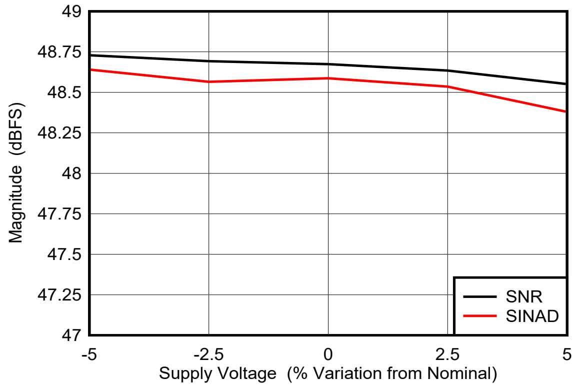


All supplies varied together

図 6-94. DES Mode: HD2, HD3 and Worst Spur vs Supply Voltage

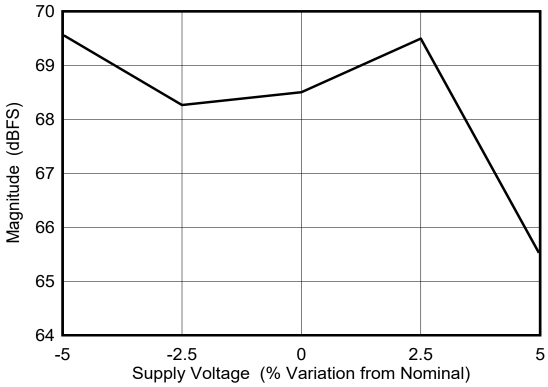
6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs



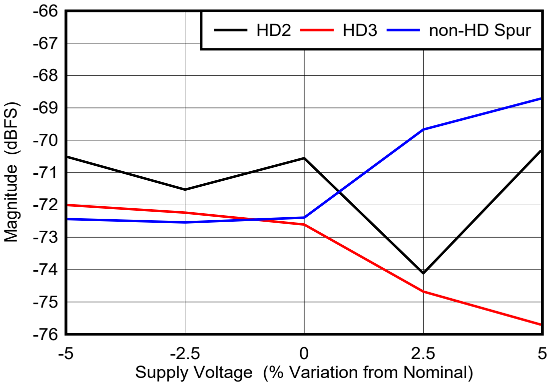
All supplies varied together

図 6-95. Dual Channel Mode: SNR and SINAD vs Supply Voltage



All supplies varied together

図 6-96. Dual Channel Mode: SFDR vs Supply Voltage



All supplies varied together

図 6-97. Dual Channel Mode: HD2, HD3 and Worst Spur vs Supply Voltage

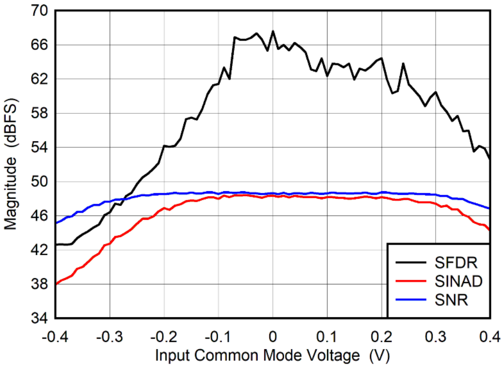


図 6-98. DES Mode: SNR, SFDR and SINAD vs Input Common Mode Voltage

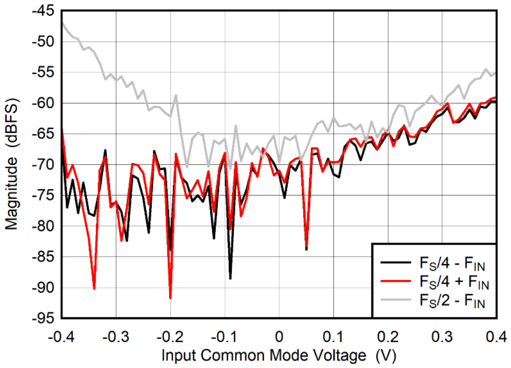
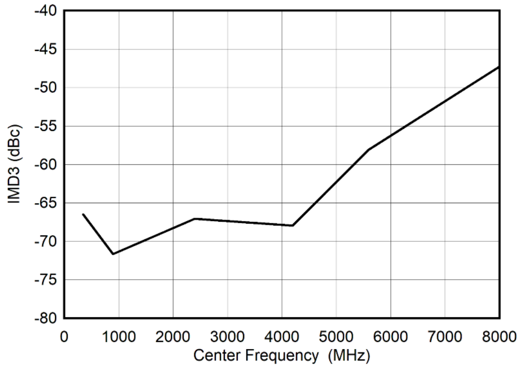


図 6-99. DES Mode: $F_S/2-F_{IN}$, $F_S/4$ +/-F_{IN} vs Input Common Mode Voltage

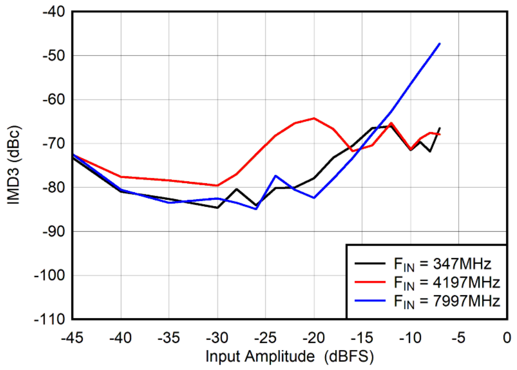


each tone -7dBFS, 100MHz tone spacing

図 6-100. DES Mode: IMD3 vs Input Frequency

6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs



100MHz tone spacing

図 6-101. DES Mode: IMD3 vs Input Amplitude

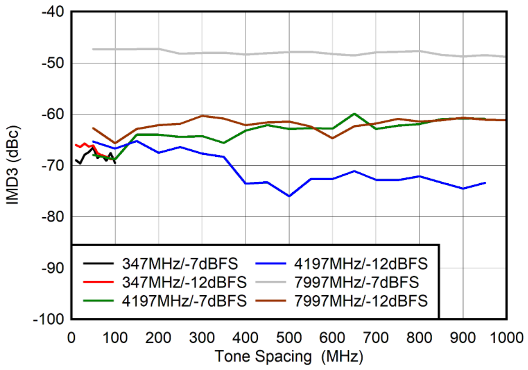
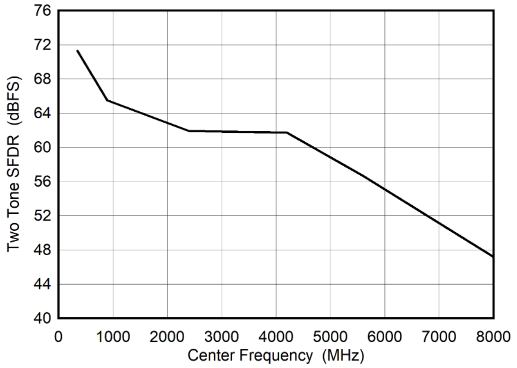
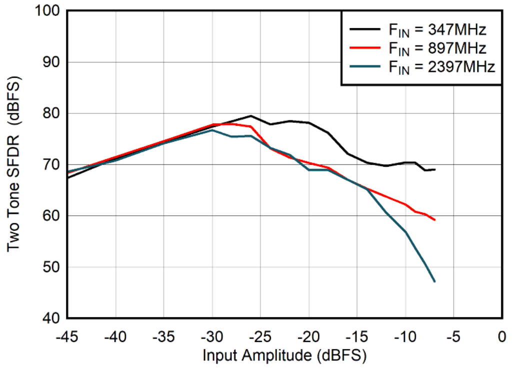


図 6-102. DES Mode: IMD3 vs Tone Spacing



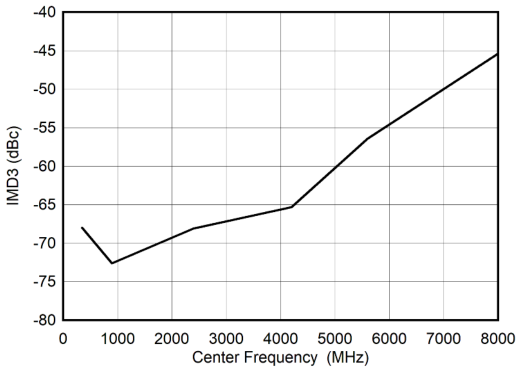
each tone -7 dBFS, 100MHz tone spacing, not including IMD3 spurs

図 6-103. DES Mode: Two Tone SFDR vs Input Frequency



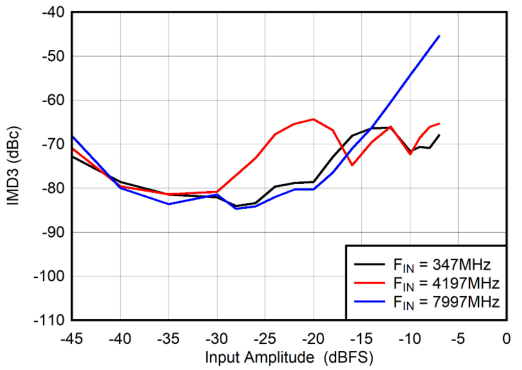
not including IMD3 spurs, 100MHz tone spacing

図 6-104. DES Mode: Two Tone SFDR vs Input Amplitude



each tone -7 dBFS, 100MHz tone spacing

図 6-105. Dual Channel Mode: IMD3 vs Input Frequency



each tone -7 dBFS, 100MHz tone spacing

図 6-106. Dual Channel Mode: IMD3 vs Input Amplitude

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6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs

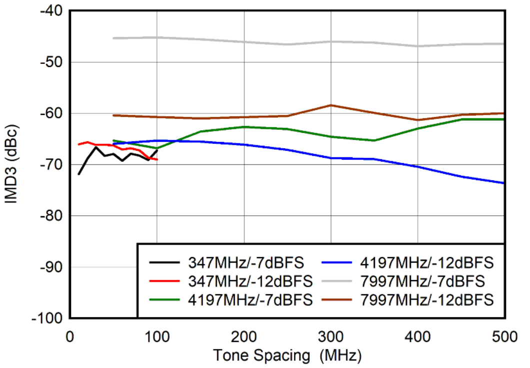
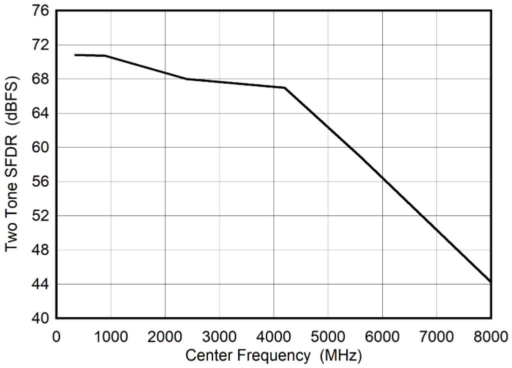
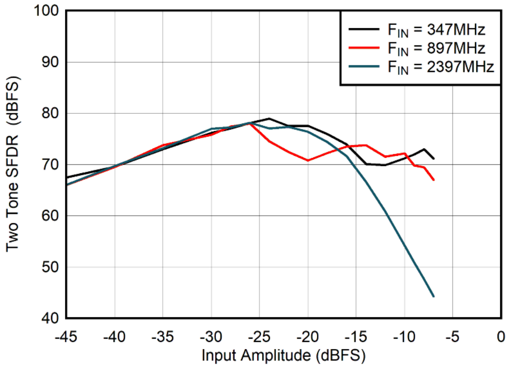


図 6-107. Dual Channel Mode: IMD3 vs Tone Spacing



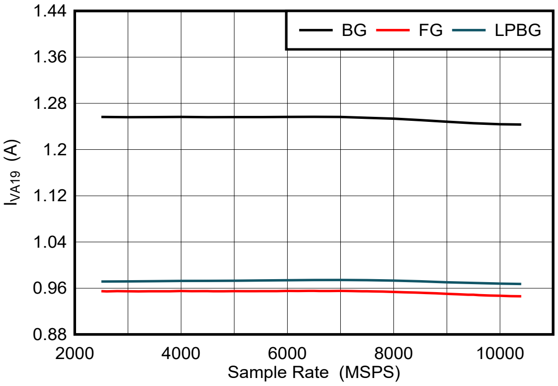
each tone -7 dBFS, 100MHz tone spacing, not including IMD3 spurs

図 6-108. Dual Channel Mode: Two Tone SFDR vs Input Frequency



not including IMD3 spurs, 100MHz tone spacing

図 6-109. Dual Channel Mode: Two Tone SFDR vs Input Amplitude

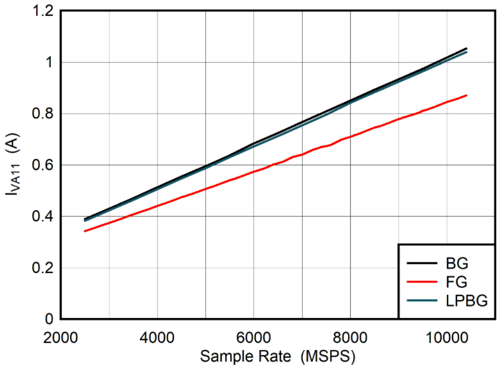


Independent of JMODE

図 6-110. DES Mode: I_{VA19} vs Sample Rate

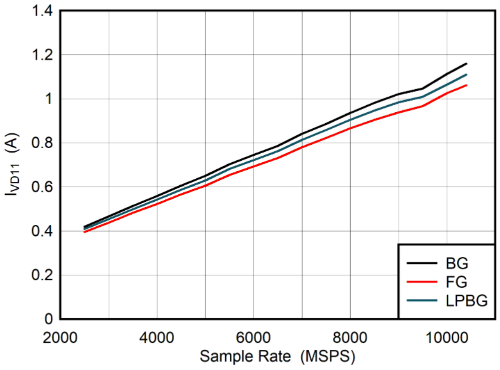
6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs



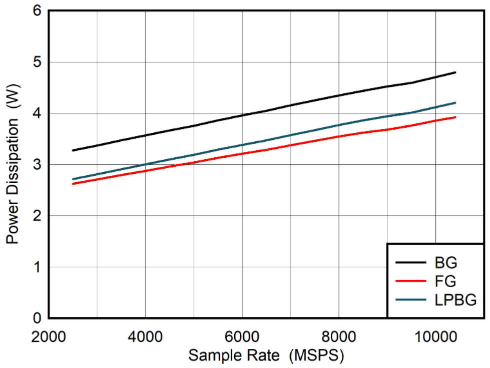
Independent of JMODE

図 6-111. DES Mode: I_{VA11} vs Sample Rate



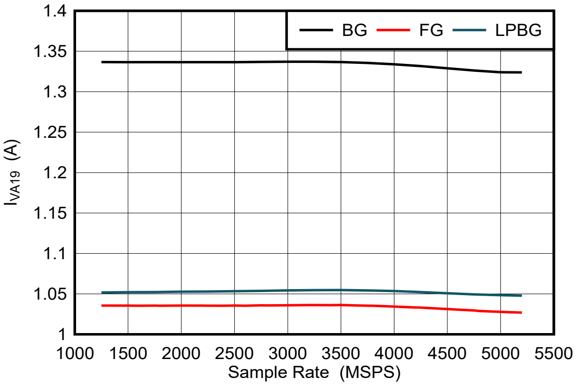
JMODE 7

図 6-112. DES Mode: I_{VD11} vs Sample Rate



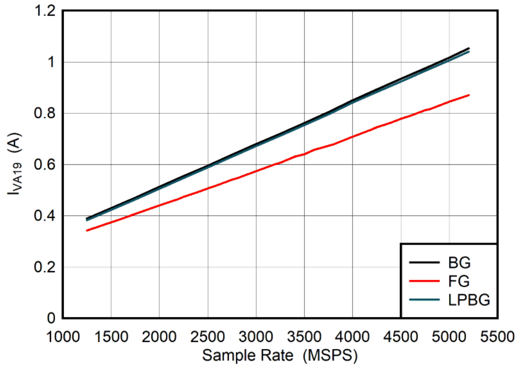
JMODE 7

図 6-113. DES Mode: Power Dissipation vs Sample Rate



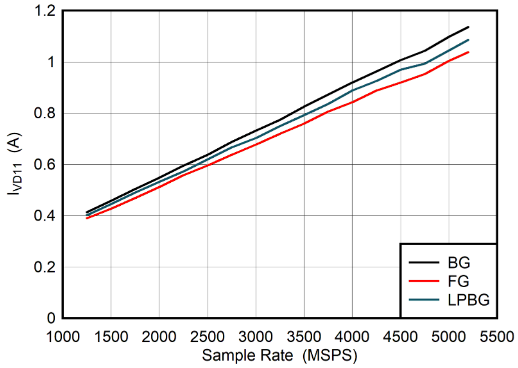
Independent of JMODE

図 6-114. Dual Channel Mode: I_{VA19} vs Sample Rate



Independent of JMODE

図 6-115. Dual Channel Mode: I_{VA11} vs Sample Rate

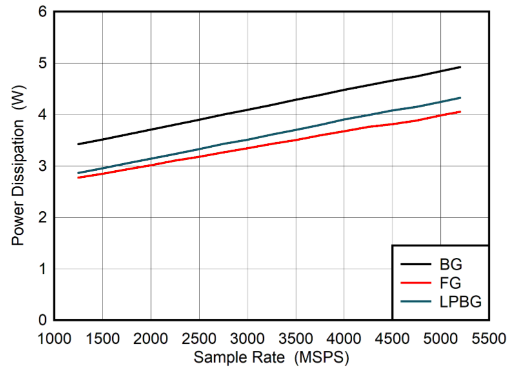


JMODE 8

図 6-116. Dual Channel Mode: I_{VD11} vs Sample Rate

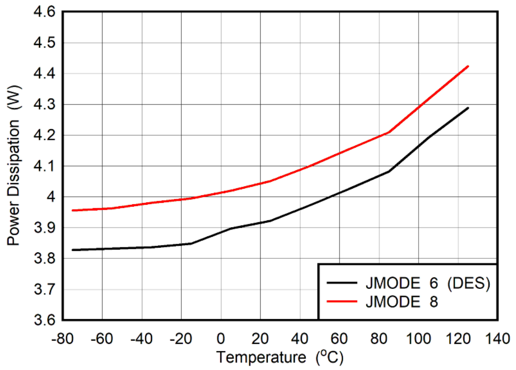
6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs



JMODE 8

図 6-117. Dual Chanel Mode: Power Dissipation vs Sample Rate



JMODES 7 (DES) and 8 (Dual Channel)

図 6-118. Power Dissipation vs Temperature

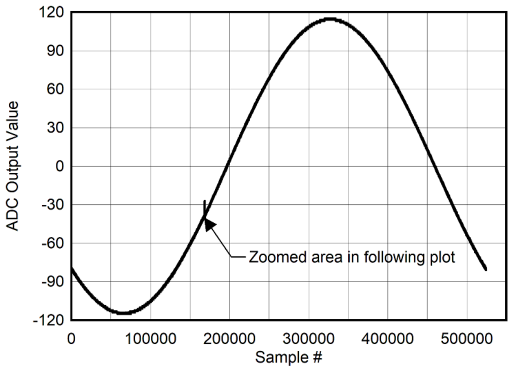


図 6-119. Background Calibration Core Transition (AC Signal)

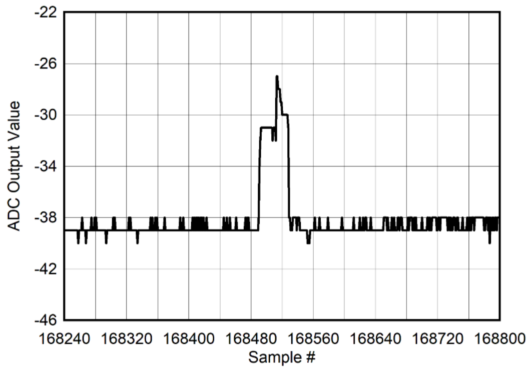


図 6-120. Background Calibration Core Transition (AC Signal Zoomed)

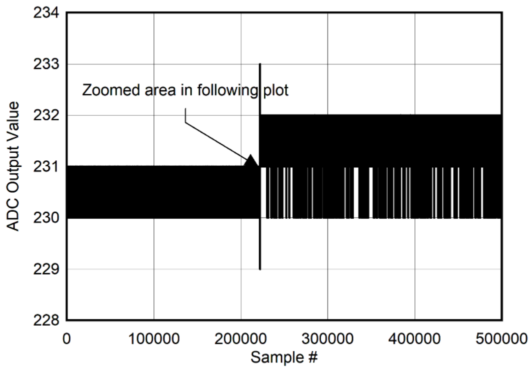


図 6-121. Background Calibration Core Transition (DC Signal)

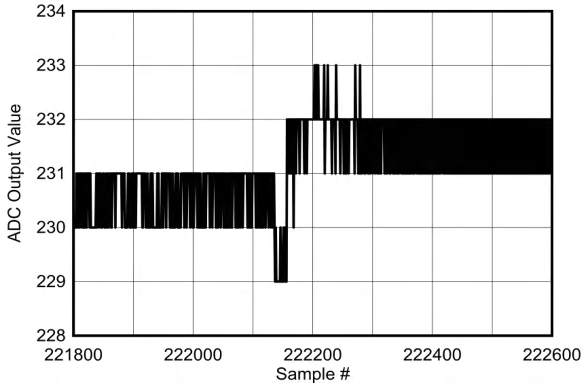


図 6-122. Background Calibration Core Transition (DC Signal Zoomed)

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6.11 Typical Characteristics (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = VD11 = 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = 5.2GHz, filtered, 1-V_{PP} sine-wave clock, JMODE = 7, dither enabled with default settings, VA11, VD11 and VS11 noise suppression ON (EN_VA11_NOISE_SUPPR = EN_VD11_NOISE_SUPPR = EN_VS11_NOISE_SUPPR = 1), and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD, ENOB, and SFDR results exclude DC and fixed-frequency interleaving spurs

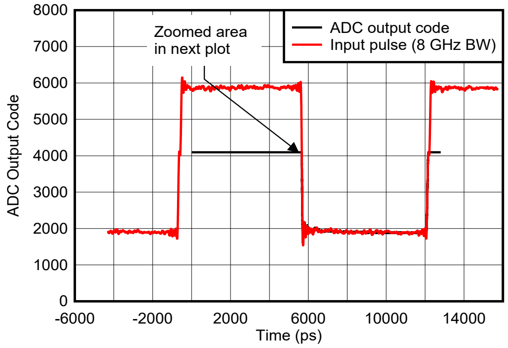

図 6-123. Pulse Overdrive Recovery

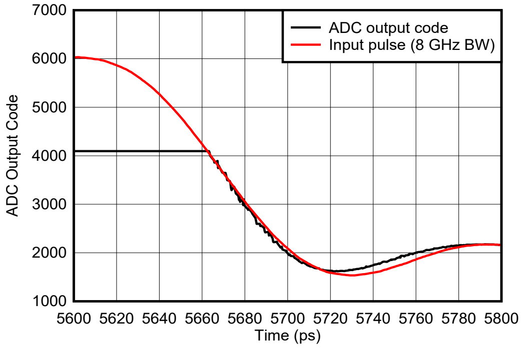

図 6-124. Pulse Overdrive Recovery Zoomed

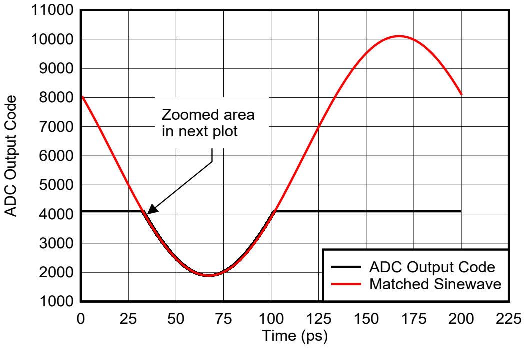

図 6-125. Sinewave Overdrive Recovery

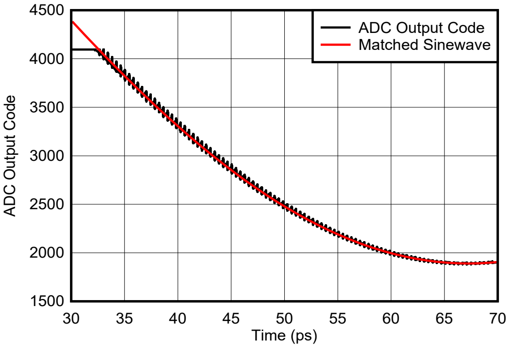

図 6-126. Sinewave Overdrive Recovery

7 Detailed Description

7.1 Overview

ADC08DJ5200RF device is an RF-sampling, giga-sample, analog-to-digital converter (ADC) that can directly sample input frequencies from DC to above 10 GHz. In dual-channel mode, the device can sample up to 5.2 GSPS and up to 10.4 GSPS in single-channel mode. Programmable tradeoffs in channel count (dual-channel mode) and Nyquist bandwidth (single-channel mode) allow development of flexible hardware that meets the needs of both high channel count or wide instantaneous signal bandwidth applications. Full-power input bandwidth (–3 dB) of 8.0 GHz, with usable frequencies exceeding the –3-dB point in both dual- and single-channel modes, allows direct RF sampling of L-band, S-band, C-band, and X-band for frequency agile systems.

The device uses a high-speed JESD204C output interface with up to 16 serialized lanes and subclass-1 compliance for deterministic latency and multi-device synchronization. The serial output lanes support up to 17.16 Gbps and can be configured to trade-off bit rate and number of lanes. Both 8B/10B and 64B/66B data encoding schemes are supported. The 64B/66B encoding schemes support forward error correction (FEC) for improved bit error rates. The JESD204C interface is backwards compatible with JESD204B receivers when using 8B/10B encoding modes.

A number of synchronization features, including noiseless aperture delay (t_{AD}) adjustment and SYSREF windowing, simplify system design for multi-channel systems. Aperture delay adjustment can be used to simplify SYSREF capture, to align the sampling instance between multiple ADCs or to sample an ideal location of a front-end track and hold (T&H) amplifier output. SYSREF windowing offers a simplistic way to measure invalid timing regions of SYSREF relative to the device clock and then choose an optimal sampling location. Dual-edge sampling (DES) is implemented in single-channel mode to reduce the maximum clock rate applied to the ADC to support a wide range of clock sources and relax setup and hold timing for SYSREF capture.

The device provides foreground and background calibration options for gain, offset and static linearity errors. Foreground calibration is run at system startup or at specified times during which the ADC is offline and not sending data to the logic device. Background calibration allows the ADC to run continually while the cores are calibrated in the background so that the system does not experience downtime. The calibration routine is also used to match the gain and offset between sub-ADC cores to minimize spurious artifacts from time interleaving.

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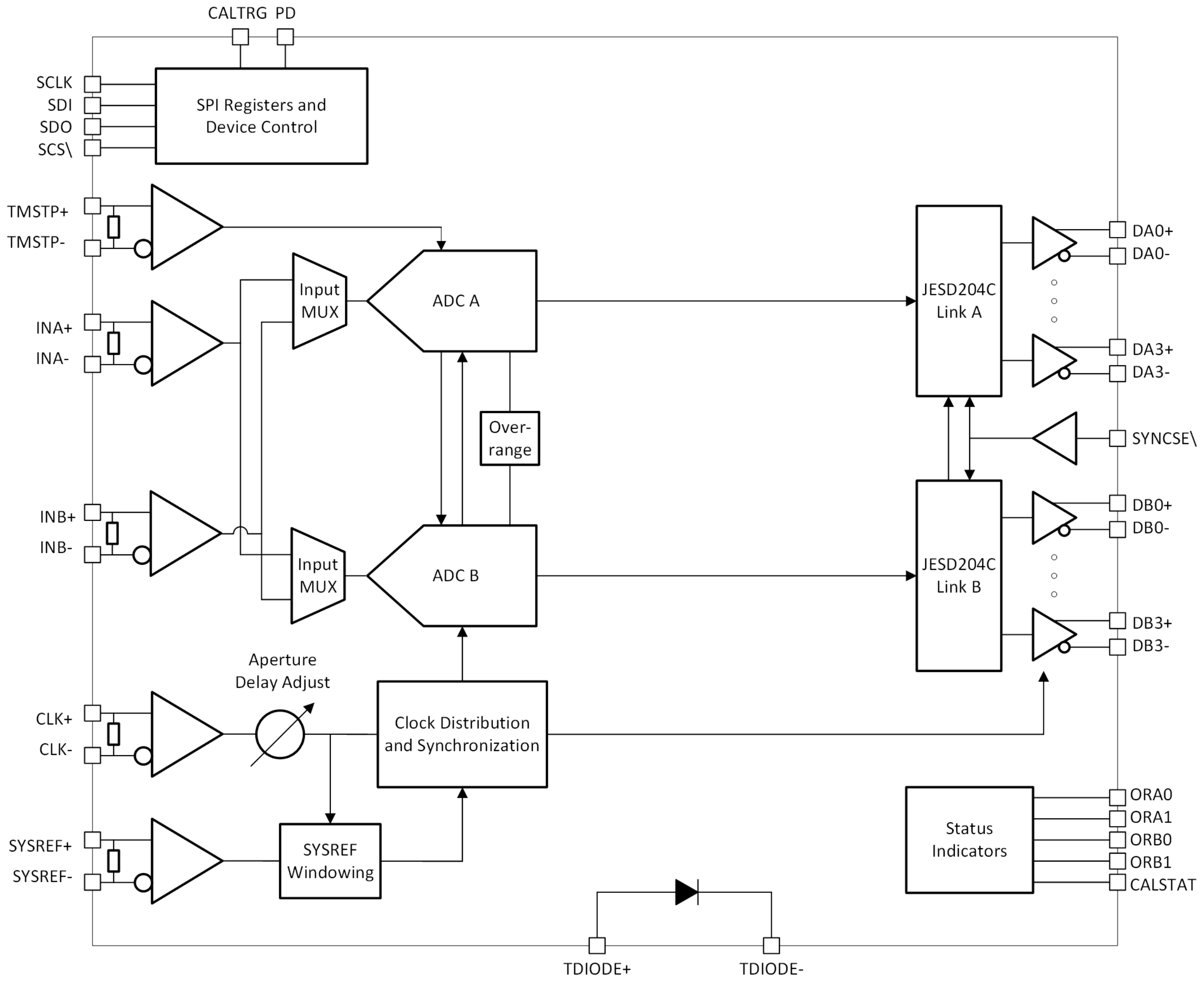
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Comparison

The devices listed in 表 7-1 are part of a pin-to-pin compatible, high-speed, wide-bandwidth ADC family. The family is offered to provide a scalable family of devices for varying resolution, sampling rate and signal bandwidth.

表 7-1. Device Family Comparison

PART NUMBER	MAXIMUM SAMPLING RATE	RESOLUTION	DUAL CHANNEL DECIMATION	SINGLE CHANNEL DECIMATION	INTERFACE (MAX LINERATE)
ADC12DJ5200RF	Single 10.4 GSPS Dual 5.2 GSPS	12-bit	Complex: 4x, 8x, 16x, 32x	Complex: 4x, 8x, 16x, 32x	JESD204B / JESD204C (17.16 Gbps)
ADC08DJ5200RF	Single 10.4 GSPS Dual 5.2 GSPS	8-bit	None	None	JESD204B / JESD204C (17.16 Gbps)
ADC12DJ4000RF	Single 8 GSPS Dual 4 GSPS	12-bit	Complex: 4x, 8x	Complex: 4x, 8x	JESD204B / JESD204C (17.16 Gbps)
ADC12DJ3200	Single 6.4 GSPS Dual 3.2 GSPS	12-bit	Real: 2x Complex: 4x, 8x, 16x	None	JESD204B (12.8 Gbps)
ADC08DJ3200	Single 6.4 GSPS Dual 3.2 GSPS	8-bit	None	None	JESD204B (12.8 Gbps)
ADC12DJ2700	Single 5.4 GSPS Dual 2.7 GSPS	12-bit	Real: 2x Complex: 4x, 8x, 16x	None	JESD204B (12.8 Gbps)

7.3.2 Analog Inputs

The analog inputs of the device have internal buffers to enable high input bandwidth and to isolate sampling capacitor glitch noise from the input circuit. Analog inputs must be driven differentially because operation with a single-ended signal results in degraded performance. Both AC-coupling and DC-coupling of the analog inputs is supported. The analog inputs are designed for an input common-mode voltage (V_{CMI}) of 0 V, which is terminated internally through single-ended, 50-Ω resistors to ground (GND) on each input pin. DC-coupled input signals must have a common-mode voltage that meets the device input common-mode requirements specified as V_{CMI} in the *Recommended Operating Conditions* table. The 0-V input common-mode voltage simplifies the interface to split-supply, fully-differential amplifiers and to a variety of transformers and baluns. The device includes internal analog input protection to protect the ADC inputs during overranged input conditions; see the *Analog Input Protection* section. 図 7-1 provides a simplified analog input model.

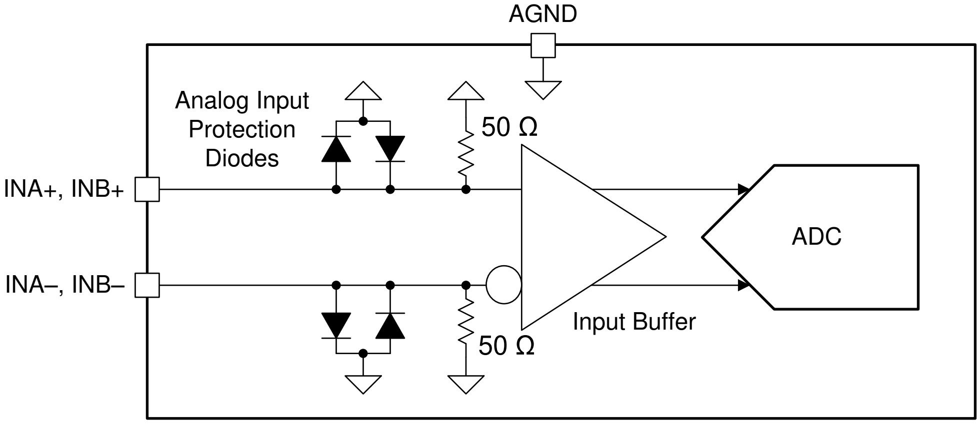


図 7-1. ADC08DJ5200RF Analog Input Internal Termination and Protection Diagram

There is minimal degradation in analog input bandwidth when using single-channel mode versus dual-channel mode. Either analog input (INA+ and INA– or INB+ and INB–) can be used in single-channel mode. The desired

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input can be chosen using SINGLE_INPUT in the input mux control register. A calibration needs to be performed after switching the input mux for the changes to take effect. Further, two inputs can be used in single-channel mode to drive the interleaved ADCs separately using the SINGLE_INPUT register setting. This mode is called dual-input single-channel mode. Dual-input single-channel mode is equivalent to dual channel mode, except ADC B samples out-of-phase with ADC A (single-channel mode sample timing). This mode is available when a single-channel mode JMODE setting is chosen.

7.3.2.1 Analog Input Protection

The analog inputs are protected against overdrive conditions by internal clamping diodes that are capable of sourcing or sinking input currents during overrange conditions, see the voltage and current limits in the *Absolute Maximum Ratings* table. The overrange protection is also defined for a peak RF input power in the *Absolute Maximum Ratings* table, which is frequency independent. Operation above the maximum conditions listed in the *Recommended Operating Conditions* table results in an increase in failure-in-time (FIT) rate, so the system must correct the overdrive condition as quickly as possible. 図 7-1 shows the analog input protection diodes.

7.3.2.2 Full-Scale Voltage (V_{FS}) Adjustment

Input full-scale voltage (V_{FS}) adjustment is available, in fine increments, for each analog input through the FS_RANGE_A register setting (see the INA full-scale range adjust register) and FS_RANGE_B register setting (see the INB full-scale range adjust register) for INA± and INB±, respectively. The available adjustment range is specified in the *Electrical Characterization: DC Specifications* table. Larger full-scale voltages improve SNR and noise floor (in dBFS/Hz) performance, but can degrade harmonic distortion. The full-scale voltage adjustment is useful for matching the full-scale range of multiple ADCs when developing a multi-converter system or for external interleaving of multiple ADC08DJ5200RF's to achieve higher sampling rates.

7.3.2.3 Analog Input Offset Adjust

In foreground calibration mode, the input offset voltage for each input and for each ADC core can be adjusted through SPI registers. The OADJ_A_FG0_VINx and OADJ_A_FG90_VINx registers (registers 0x344 to 0x34A) are used to adjust ADC core A's offset voltage when sampling analog input x (where x is A for INA± or B for INB±) where the FG0 register is used for dual channel mode and FG90 is used for single channel mode. OADJ_B_FG0_VINx is used to adjust ADC core B's offset voltage when sampling input x. OADJ_B_FG0_VINx applies to both single channel mode and dual channel mode. To adjust the offset voltage in dual channel mode simply adjust the offset for the ADC core sampling the desired input. In single channel mode, both ADC core A's offset and ADC core B's offset must be adjusted together. The difference in the two core's offsets in single channel mode will result in a spur at $f_S/2$ that is independent of the input. These registers can be used to compensate the $f_S/2$ spur in single channel mode. See the *Calibration Modes and Trimming* section for more information.

7.3.3 ADC Core

The ADC08DJ5200RF consists of a total of six ADC cores. The cores are interleaved for higher sampling rates and swapped on-the-fly for calibration as required by the operating mode. This section highlights the theory and key features of the ADC cores.

7.3.3.1 ADC Theory of Operation

The differential voltages at the analog inputs are captured by the rising edge of CLK± in dual-channel mode or by the rising and falling edges of CLK± in single-channel mode. After capturing the input signal, the ADC converts the analog voltage to a digital value by comparing the voltage to the internal reference voltage. If the voltage on INA– or INB– is higher than the voltage on INA+ or INB+, respectively, then the digital output is a negative 2's complement value. If the voltage on INA+ or INB+ is higher than the voltage on INA– or INB–, respectively, then the digital output is a positive 2's complement value. 式 1 can calculate the differential voltage at the input pins from the digital output.

$$V_{IN} = \frac{\text{Code}}{2^N} V_{FS} \tag{1}$$

where

- Code is the signed decimal output code (for example, –2048 to +2047)
- N is the ADC resolution
- and V_{FS} is the full-scale input voltage of the ADC as specified in the *Recommended Operating Conditions* table, including any adjustment performed by programming FS_RANGE_A or FS_RANGE_B

7.3.3.2 ADC Core Calibration

ADC core calibration is required to optimize the analog performance of the ADC cores. Calibration must be repeated when operating conditions change significantly, namely temperature, in order to maintain optimal performance. The device has a built-in calibration routine that can be run as a foreground operation or a background operation. Foreground operation requires ADC downtime, where the ADC is no longer sampling the input signal, to complete the process. Background calibration can be used to overcome this limitation and allow constant operation of the ADC. See the *Calibration Modes and Trimming* section for detailed information on each mode.

7.3.3.3 Analog Reference Voltage

The reference voltage for the ADC08DJ5200RF is derived from an internal band-gap reference. A buffered version of the reference voltage is available at the BG pin for user convenience. This output has an output-current capability of ±100 µA. The BG output must be buffered if more current is required. No provision exists for the use of an external reference voltage, but the full-scale input voltage can be adjusted through the full-scale-range register settings.

7.3.3.4 ADC Overrange Detection

To make sure that system gain management has the quickest possible response time, a low-latency configurable overrange function is included. The overrange function works by monitoring the converted samples at the ADC to quickly detect if the ADC is near saturation or already in an overrange condition. The absolute value of the ADC data are checked against two programmable thresholds, OVR_T0 and OVR_T1. These thresholds apply to both channel A and channel B in dual-channel mode. 表 7-2 lists how an ADC sample is converted to an absolute value for a comparison of the thresholds.

表 7-2. Conversion of ADC Sample for Overrange Comparison

ADC SAMPLE (Offset Binary)	ADC SAMPLE (2's Complement)	ABSOLUTE VALUE
1111 1111 (255)	0111 1111(+127)	111 1111 (127)
1111 0000 (240)	0111 0000 (+112)	111 0000 (112)
1000 0000 (128)	0000 0000 (0)	0000 0000(0)
0001 0000 (16)	1000 0001 0000 (–112)	111 0000 (112)
0000 0000 (0)	1000 0000 0000 (–128)	111 1111 (127)

If the absolute value equal or exceed the OVR_T0 or OVR_T1 thresholds during the monitoring period, then the overrange bit associated with the threshold is set to 1, otherwise the overrange bit is 0. In dual-channel mode, the overrange status can be monitored on the ORA0 and ORA1 pins for channel A and the ORB0 and ORB1 pins for channel B, where ORx0 corresponds to the OVR_T0 threshold and ORx1 corresponds to the OVR_T1 threshold. In single-channel mode, the overrange status for the OVR_T0 threshold is determined by monitoring both the ORA0 and ORB0 outputs and the OVR_T1 threshold is determined by monitoring both ORA1 and ORB1 outputs. In single-channel mode, the two outputs for each threshold must be OR'd together to determine whether an overrange condition occurred. OVR_N can be used to set the output pulse duration from the last overrange event. 表 7-3 lists the overrange pulse lengths for the various OVR_N settings.

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表 7-3. Overrange Monitoring Period for the ORA0, ORA1, ORB0, and ORB1 Outputs

OVR_N	OVERRANGE PULSE LENGTH SINCE LAST OVERRANGE EVENT (DEVCLK Cycles)
0	8
1	16
2	32
3	64
4	128
5	256
6	512
7	1024

Typically, the OVR_T0 threshold can be set near the full-scale value (228 for example). When the threshold is triggered, a typical system can turn down the system gain to avoid clipping. The OVR_T1 threshold can be set much lower. For example, the OVR_T1 threshold can be set to 64 (peak input voltage of −12 dBFS). If the input signal is strong, the OVR_T1 threshold is tripped occasionally. If the input is quite weak, the threshold is never tripped. The downstream logic device monitors the OVR_T1 bit. If OVR_T1 stays low for an extended period of time, then the system gain can be increased until the threshold is occasionally tripped (meaning the peak level of the signal is above −12 dBFS).

7.3.3.5 Code Error Rate (CER)

ADC cores can generate bit errors within a sample, often called *code errors (CER)* or referred to as *sparkle codes*, resulting from metastability caused by non-ideal comparator limitations. The device uses a unique ADC architecture that inherently allows significant code error rate improvements from traditional pipelined flash or successive approximation register (SAR) ADCs. The code error rate of the device is multiple orders of magnitude better than what can be achieved in alternative architectures at equivalent sampling rates providing significant signal reliability improvements.

7.3.4 Temperature Monitoring Diode

A built-in thermal monitoring diode is made available on the TDIODE+ and TDIODE– pins. This diode facilitates temperature monitoring and characterization of the device in higher ambient temperature environments. Although the on-chip diode is not highly characterized, the diode can be used effectively by performing a baseline measurement (offset) at a known ambient or board temperature and creating a linear equation with the diode voltage slope provided in the *Electrical Characteristics: DC Specifications* table. Perform offset measurement with the device unpowered or with the PD pin asserted to minimize device self-heating. Recommended monitoring devices include the LM95233 device and similar remote-diode temperature monitoring products from Texas Instruments.

7.3.5 Timestamp

The TMSTP+ and TMSTP– differential input can be used as a time-stamp input to mark a specific sample based on the timing of an external trigger event relative to the sampled signal. TIMESTAMP_EN (see the LSB control bit output register) must be set in order to use the timestamp feature and output the timestamp data. When enabled, the LSB of the 8-bit output sample is used to output the timestamp status. The trigger must be applied to the differential TMSTP+ and TMSTP– inputs. The trigger can be asynchronous to the ADC sampling clock and is sampled at approximately the same time as the analog input.

7.3.6 Clocking

The clocking subsystem of the device has two input signals, device clock (CLK+, CLK−) and SYSREF (SYSREF+, SYSREF−). Within the clocking subsystem there is a noiseless aperture delay adjustment (t_{AD} adjust), a clock duty cycle corrector and a SYSREF capture block. 図 7-2 describes the clocking subsystem.

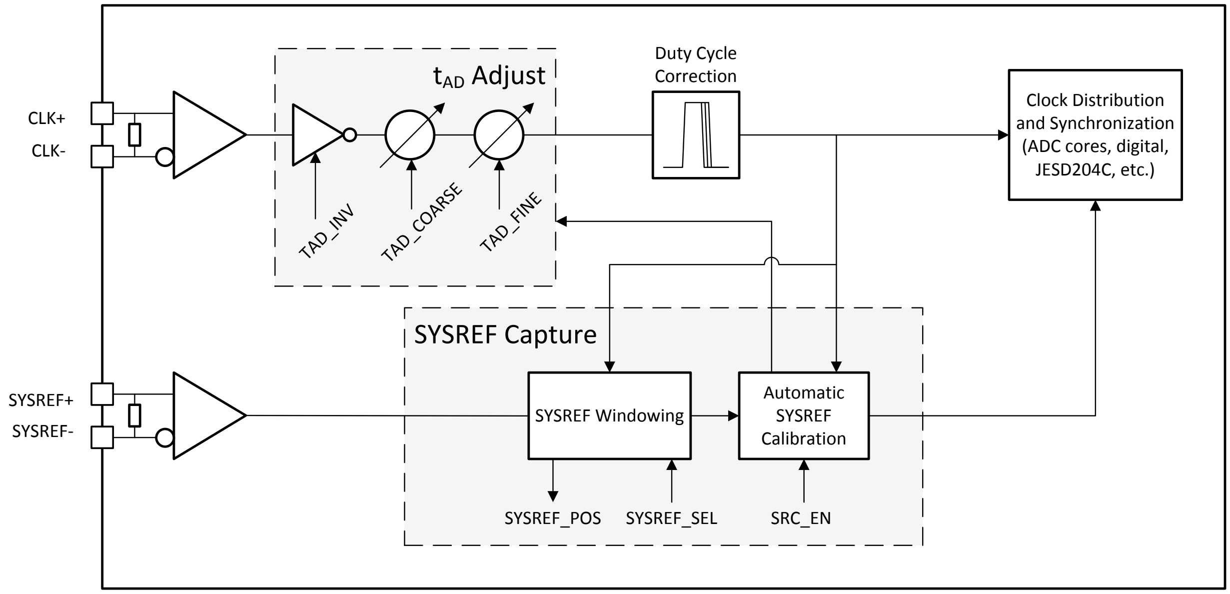

図 7-2. Clocking Subsystem

The device clock is used as the sampling clock for the ADC core as well as the clocking for the digital processing and serializer outputs. Use a low-noise (low jitter) device clock to maintain high signal-to-noise ratio (SNR) within the ADC. In dual-channel mode, the analog input signal for each input is sampled on the rising edge of the device clock. In single-channel mode, both the rising and falling edges of the device clock are used to capture the analog signal to reduce the maximum clock rate required by the ADC. A noiseless aperture delay adjustment (t_{AD} adjust) allows the user to shift the sampling instance of the ADC in fine steps in order to synchronize multiple ADC08DJ5200RFs or to fine-tune system latency. Duty cycle correction is implemented in the device to ease the requirements on the external device clock while maintaining high performance. 表 7-4 summarizes the device clock interface in dual-channel mode and single-channel mode.

表 7-4. Device Clock vs Mode of Operation

MODE OF OPERATION	SAMPLING RATE VS f_{CLK}	SAMPLING INSTANT
Dual-channel mode	1 × f_{CLK}	Rising edge
Single-channel mode	2 × f_{CLK}	Rising and falling edge

SYSREF is a system timing reference used for JESD204C subclass-1 implementations of deterministic latency. SYSREF is used to achieve deterministic latency and for multi-device synchronization. SYSREF must be captured by the correct device clock edge in order to achieve repeatable latency and synchronization. The ADC08DJ5200RF includes SYSREF windowing and automatic SYSREF calibration to ease the requirements on the external clocking circuits and to simplify the synchronization process. SYSREF can be implemented as a single pulse or as a periodic clock. In periodic implementations, SYSREF must be equal to, or an integer division of, the local multiframe clock frequency in 8B/10B encoding modes or the local extended multiblock clock frequency in 64B/66B encoding modes. 式 2 is used to calculate valid SYSREF frequencies in 8B/10B encoding modes and 式 3 in 64B/66B encoding modes.

$$f_{SYSREF} = \frac{R \times f_{CLK}}{10 \times F \times K \times n} \tag{2}$$

$$f_{SYSREF} = \frac{R \times f_{CLK}}{66 \times 32 \times E \times n} \tag{3}$$

where

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- R and F are set by the JMODE setting (see)
- f_{CLK} is the device clock frequency (CLK±)
- K is the programmed multiframe length (see for valid K settings)
- E is the number of multiblocks in an extended multiblock.
- n is any positive integer

7.3.6.1 Noiseless Aperture Delay Adjustment (t_{AD} Adjust)

The device contains a delay adjustment on the device clock (sampling clock) input path, called t_{AD} adjust, that can be used to shift the sampling instance within the device in order to align sampling instances among multiple devices or for external interleaving of multiple devices. Further, t_{AD} adjust can be used for automatic SYSREF calibration to simplify synchronization; see the *Automatic SYSREF Calibration* section. Aperture delay adjustment is implemented in a way that adds no additional noise to the clock path; however, a slight degradation in aperture jitter (t_{AJ}) is possible at large values of TAD_COARSE because of internal clock path attenuation. The degradation in aperture jitter can result in minor SNR degradations at high input frequencies (see t_{AJ} in the *Switching Characteristics* table). This feature is programmed using TAD_INV, TAD_COARSE, and TAD_FINE in the DEVCLK timing adjust ramp control register. Setting TAD_INV inverts the input clock resulting in a delay equal to half the clock period. 表 7-5 summarizes the step sizes and ranges of the TAD_COARSE and TAD_FINE variable analog delays. All three delay options are independent and can be used in conjunction. All clocks within the device are shifted by the programmed t_{AD} adjust amount, which results in a shift of the timing of the JESD204C serialized outputs and affects the capture of SYSREF.

表 7-5. t_{AD} Adjust Adjustment Ranges

ADJUSTMENT PARAMETER	ADJUSTMENT STEP	DELAY SETTINGS	MAXIMUM DELAY
TAD_INV	$1 / (f_{CLK} \times 2)$	1	$1 / (f_{CLK} \times 2)$
TAD_COARSE	See $t_{TAD(STEP)}$ in the *Switching Characteristics* table	256	See $t_{TAD(MAX)}$ in the *Switching Characteristics* table
TAD_FINE	See $t_{TAD(STEP)}$ in the *Switching Characteristics* table	256	See $t_{TAD(MAX)}$ in the *Switching Characteristics* table

In order to maintain timing alignment between converters, stable and matched power-supply voltages and device temperatures must be provided.

Aperture delay adjustment can be changed on-the-fly during normal operation but may result in brief upsets to the JESD204C data link. Use TAD_RAMP to reduce the probability of the JESD204C link losing synchronization; see the *Aperture Delay Ramp Control* section.

7.3.6.2 Aperture Delay Ramp Control (TAD_RAMP)

The ADC08DJ5200RF contains a function to gradually adjust the t_{AD} adjust setting towards the newly written TAD_COARSE value. This functionality allows the t_{AD} adjust setting to be adjusted with minimal internal clock circuitry glitches. The TAD_RAMP_RATE parameter allows either a slower (one TAD_COARSE LSB per 384 t_{CLK} cycles) or faster ramp (four TAD_COARSE LSBs per 384 t_{CLK} cycles) to be selected. The TAD_RAMP_EN parameter enables the ramp feature and any subsequent writes to TAD_COARSE initiate a new cramp.

7.3.6.3 SYSREF Capture for Multi-Device Synchronization and Deterministic Latency

The clocking subsystem is largely responsible for achieving multi-device synchronization and deterministic latency. The ADC08DJ5200RF uses the JESD204C subclass-1 method to achieve deterministic latency and synchronization. Subclass 1 requires that the SYSREF signal be captured by a deterministic device clock (CLK±) edge at each system power-on and at each device in the system. This requirement imposes setup and hold constraints on SYSREF relative to CLK±, which can be difficult to meet at giga-sample clock rates over all system operating conditions. The device includes a number of features to simplify this synchronization process and to relax system timing constraints:

- The device uses dual-edge sampling (DES) in single-channel mode to reduce the CLK± input frequency by half and double the timing window for SYSREF (see 表 7-4)
- A SYSREF position detector (relative to CLK±) and selectable SYSREF sampling position aid the user in meeting setup and hold times over all conditions; see the *SYSREF Position Detector* section

- Easy-to-use automatic SYSREF calibration uses the aperture timing adjust block (t_{AD} adjust) to shift the ADC sampling instance based on the phase of SYSREF (rather than adjusting SYSREF based on the phase of the ADC sampling instance); see the *Automatic SYSREF Calibration* section

7.3.6.3.1 SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing)

The SYSREF windowing block is used to first detect the position of SYSREF relative to the CLK± rising edge and then to select a desired SYSREF sampling instance, which is a delay version of CLK±, to maximize setup and hold timing margins. In many cases a single SYSREF sampling position (SYSREF_SEL) is sufficient to meet timing for all systems (device-to-device variation) and conditions (temperature and voltage variations). However, this feature can also be used by the system to expand the timing window by tracking the movement of SYSREF as operating conditions change or to remove system-to-system variation at production test by finding a unique optimal value at nominal conditions for each system.

This section describes proper usage of the SYSREF windowing block. First, apply the device clock and SYSREF to the device. The location of SYSREF relative to the device clock cycle is determined and stored in the SYSREF_POS bits of the SYSREF capture position register. ADC08DJ5200RF must see at least 3 rising edges of SYSREF before the SYSREF_POS output is valid. Each bit of SYSREF_POS represents a potential SYSREF sampling position. If a bit in SYSREF_POS is set to 1, then the corresponding SYSREF sampling position has a potential setup or hold violation. Upon determining the valid SYSREF sampling positions (the positions of SYSREF_POS that are set to 0) the desired sampling position can be chosen by setting SYSREF_SEL in the clock control register 0 to the value corresponding to that SYSREF_POS position. In general, the middle sampling position between two setup and hold instances is chosen. Ideally, SYSREF_POS and SYSREF_SEL are performed at the nominal operating conditions of the system (temperature and supply voltage) to provide maximum margin for operating condition variations. This process can be performed at final test and the optimal SYSREF_SEL setting can be stored for use at every system power up. Further, SYSREF_POS can be used to characterize the skew between CLK± and SYSREF± over operating conditions for a system by sweeping the system temperature and supply voltages. For systems that have large variations in CLK± to SYSREF± skew, this characterization can be used to track the optimal SYSREF sampling position as system operating conditions change. In general, a single value can be found that meets timing over all conditions for well-matched systems, such as those where CLK± and SYSREF± come from a single clocking device.

Note

SYSREF_SEL must be set to 0 when using automatic SYSREF calibration; see the *Automatic SYSREF Calibration* section.

The step size between each SYSREF_POS sampling position can be adjusted using SYSREF_ZOOM. When SYSREF_ZOOM is set to 0, the delay steps are coarser. When SYSREF_ZOOM is set to 1, the delay steps are finer. See the *Switching Characteristiccs* table for delay step sizes when SYSREF_ZOOM is enabled and disabled. In general, SYSREF_ZOOM = 1 is recommended to be used above f_{CLK} = 3GHz and SYSREF_ZOOM = 0 below f_{CLK} = 3GHz. Bits 0 and 23 of SYSREF_POS are always be set to 1 because there is insufficient information to determine if these settings are close to a timing violation, although the actual valid window can extend beyond these sampling positions. The value programmed into SYSREF_SEL is the decimal number representing the desired bit location in SYSREF_POS. 表 7-6 lists some example SYSREF_POS readings and the optimal SYSREF_SEL settings. Although 24 sampling positions are provided by the SYSREF_POS status register, SYSREF_SEL only allows selection of the first 16 sampling positions, corresponding to SYSREF_POS bits 0 to 15. The additional SYSREF_POS status bits are intended only to provide additional knowledge of the SYSREF valid window. In general, lower values of SYSREF_SEL are selected because of delay variation over supply voltage, however in the fourth example a value of 15 provides additional margin and can be selected instead.

表 7-6. Examples of SYSREF_POS Readings and SYSREF_SEL Selections

SYSREF_POS[23:0]			OPTIMAL SYSREF_SEL SETTING
0x02E[7:0] (Largest Delay)	0x02D[7:0][1]	0x02C[7:0][1] (Smallest Delay)	
b10000000	b0110000 0	b00011001	8 or 9

表 7-6. Examples of SYSREF_POS Readings and SYSREF_SEL Selections (continued)

SYSREF_POS[23:0]			OPTIMAL SYSREF_SEL SETTING
0x02E[7:0] (Largest Delay)	0x02D[7:0][1]	0x02C[7:0][1] (Smallest Delay)	
b10011000	b00000000	b00110001	12
b10000000	b01100000	b0 0000001	6 or 7
b10000000	b00000011	b00000001	4 or 15
b10001100	b01100011	b00011001	6

(1) Red coloration indicates the bits that are selected, as given in the last column of this table.

7.3.6.3.2 Automatic SYSREF Calibration

The ADC08DJ5200RF has an automatic SYSREF calibration feature to alleviate the often challenging setup and hold times associated with capturing SYSREF for giga-sample data converters. Automatic SYSREF calibration uses the t_{AD} adjust feature to shift the device clock to maximize the SYSREF setup and hold times or to align the sampling instance based on the SYSREF rising edge.

The device must have a proper device clock applied and be programmed for normal operation before starting the automatic SYSREF calibration. When ready to initiate automatic SYSREF calibration, a continuous SYSREF signal must be applied. SYSREF must be a continuous (periodic) signal when using the automatic SYSREF calibration. Start the calibration process by setting SRC_EN high in the SYSREF calibration enable register after configuring the automatic SYSREF calibration using the SRC_CFG register. Upon setting SRC_EN high, the device searches for the optimal t_{AD} adjust setting until the device clock falling edge is internally aligned to the SYSREF rising edge. TAD_DONE in the SYSREF calibration status register can be monitored tomake sure the SYSREF calibration has finished. By aligning the device clock falling edge with the SYSREF rising edge, automatic SYSREF calibration maximizes the internal SYSREF setup and hold times relative to the device clock and also sets the sampling instant based on the SYSREF rising edge. After the automatic SYSREF calibration finishes, the rest of the startup procedure can be performed to finish bringing up the system.

For multi-device synchronization, the SYSREF rising edge timing must be matched at all devices and therefore trace lengths must be matched from a common SYSREF source to each device. Any skew between the SYSREF rising edge at each device results in additional error in the sampling instance between devices, however repeatable deterministic latency from system startup to startup through each device must still be achieved. No other design requirements are needed in order to achieve multi-device synchronization as long as a proper elastic buffer release point is chosen in the JESD204C receiver.

図 7-3 provides a timing diagram of the SYSREF calibration procedure. The optimized setup and hold times are shown as $t_{SU(OPT)}$ and $t_{H(OPT)}$, respectively. Device clock and SYSREF are referred to as *internal* in this diagram because the phase of the internal signals are aligned within the device and not to the external (applied) phase of the device clock or SYSREF.

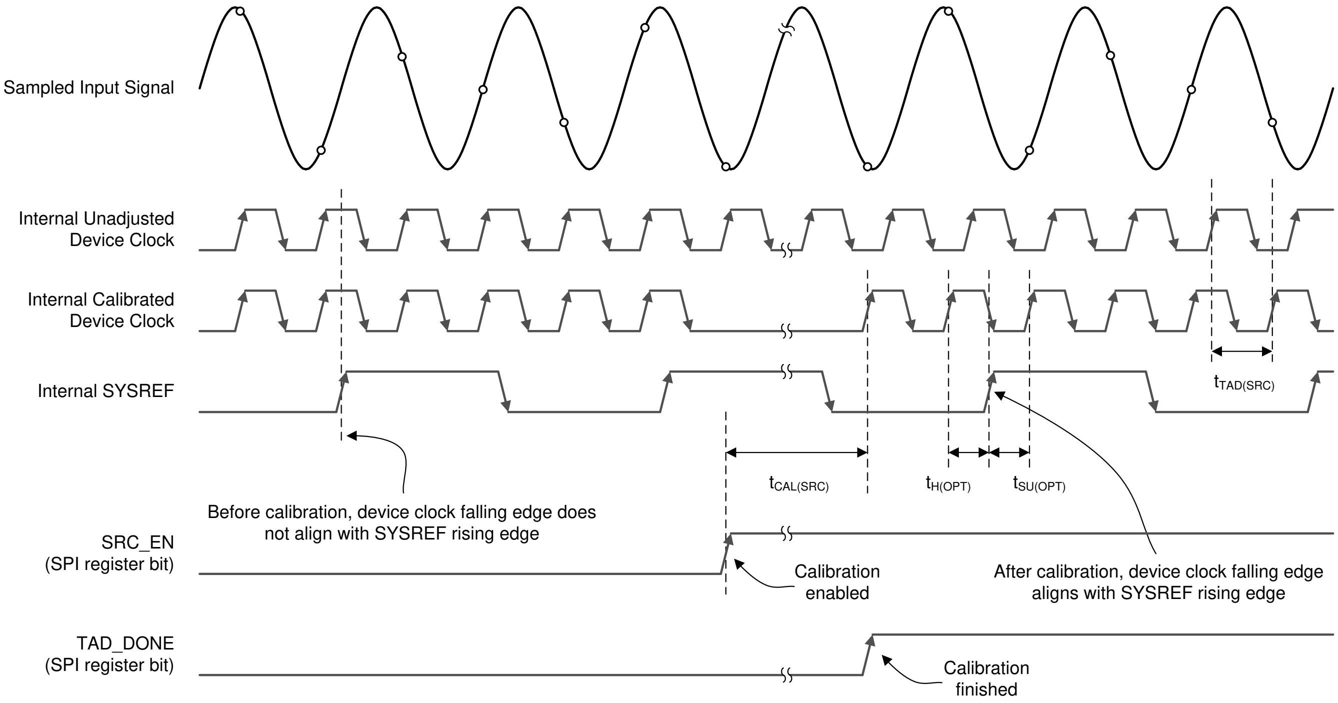

図 7-3. SYSREF Calibration Timing Diagram

When finished, the t_{AD} adjust setting found by the automatic SYSREF calibration can be read from SRC_TAD in the SYSREF calibration status register. After calibration, the system continues to use the calibrated t_{AD} adjust setting for operation until the system is powered down. However, if desired, the user can then disable the SYSREF calibration and fine-tune the t_{AD} adjust setting according to the systems needs. Alternatively, the use of the automatic SYSREF calibration can be done at product test (or periodic recalibration) of the optimal t_{AD} adjust setting for each system. This value can be stored and written to the TAD register (TAD_INV, TAD_COARSE, and TAD_FINE) upon system startup.

Do not run the SYSREF calibration when the ADC calibration (foreground or background) is running. If background calibration is the desired use case, disable the background calibration when the SYSREF calibration is used, then reenable the background calibration after TAD_DONE goes high. SYSREF_SEL in the clock control register 0 must be set to 0 when using SYSREF calibration.

SYSREF calibration searches the TAD_COARSE delays using both noninverted (TAD_INV = 0) and inverted clock polarity (TAD_INV = 1) to minimize the required TAD_COARSE setting in order to minimize loss on the clock path to reduce aperture jitter (t_{AJ}).

7.3.7 Programmable FIR Filter (PFIR)

The output of the ADCs can be sent through programmable finite-impulse-response (PFIR) digital filter for equalization of the frequency response. The filter can be setup in a few modes of operation to allow independent equalization of each channel in dual channel mode, equalization in single channel mode or as a time-varying filter in dual channel mode (such as for I/Q correction). The various PFIR operating modes are given in 表 7-7.

表 7-7. PFIR Operating Modes

PFIR Mode	Center Tap Resolution	Center Tap LSB Weight	Non-Center Tap Resolution	Non-Center Tap LSB Weight	Filter Coefficients
Dual Channel Equalization	18 bits	2^{-16}	12 bits	$2^{-10}, 2^{-11}...2^{-16}$	9 per channel
Single Channel Equalization	18 bits	2^{-16}	12 bits	$2^{-10}, 2^{-11}...2^{-16}$	9

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表 7-7. PFIR Operating Modes (continued)

PFIR Mode	Center Tap Resolution	Center Tap LSB Weight	Non-Center Tap Resolution	Non-Center Tap LSB Weight	Filter Coefficients
Time Varying Filter	18 bits	2^{-16}	12 bits	2^{-10}, 2^{-11}...2^{-16}	9 per coefficient set, 2 coefficient sets

Programming information for the various PFIR modes is given in 表 7-8. The coefficients are programmed into the PFIR_Ax and PFIR_Bx registers.

表 7-8. Programmable FIR Filter Mode Programming

PFIR Mode	PFIR_MODE	PFIR_SHARE	PFIR_MERGE
PFIR Disabled	0	X	X
Dual Channel Equalization	2	0	0
Single Channel Equalization	2	1	1
Time Varying Filter	2	0	1

7.3.7.1 Dual Channel Equalization

When the ADC is operating in *dual channel mode* (based on the JMODE setting) then the PFIR filter can be set in *dual channel equalization* mode. This mode allows independent frequency equalization of the two ADC channels. The filter for each channel consists of 9 coefficients that can be independently set. The center tap for each filter has a resolution of 18 bits and the LSB has a weight of 2^{-16}. The non-center taps have a resolution of 12-bits with programmable LSB weight of 2^{-10}, 2^{-11}, 2^{-12}, 2^{-13}, 2^{-14}, 2^{-15} or 2^{-16}. All non-center taps have the same LSB weight. The block diagram for *dual channel equalization* is shown in 図 7-4.

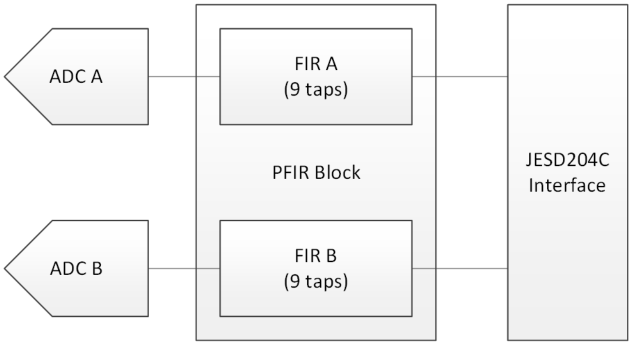

図 7-4. Dual Channel Equalization PFIR Block Diagram

7.3.7.2 Single Channel Equalization

When the ADC is operating in *single channel mode* (based on the JMODE setting) then the PFIR filter can be set in *single channel equalization* mode. This mode allows frequency equalization of the ADC. The filter consists of 9 coefficients that can be independently set. The center tap of the filter has a resolution of 18 bits and the LSB has a weight of 2^{-16}. The non-center taps have a resolution of 12-bits with programmable LSB weight of 2^{-10}, 2^{-11}, 2^{-12}, 2^{-13}, 2^{-14}, 2^{-15} or 2^{-16}. All non-center taps have the same LSB weight. The block diagram for *single channel equalization* is shown in 図 7-5.

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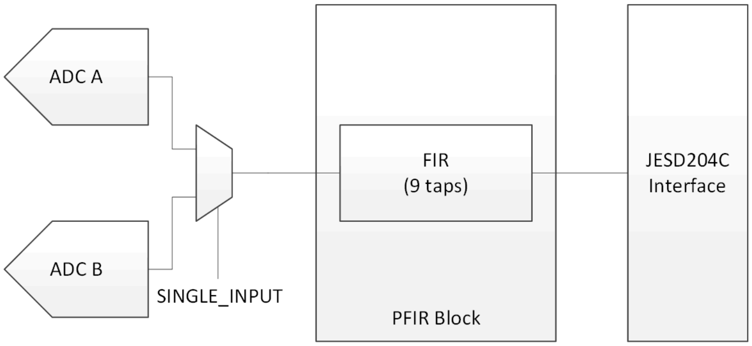

図 7-5. Single Channel Equalization PFIR Block Diagram

7.3.7.3 Time Varying Filter

When the ADC is operating in *dual-input single channel mode* (based on the JMODE setting and SINGLE_INPUT setting) then the PFIR filter can be set in *time varying filter* mode. This mode enables a time varying filter with two coefficient sets that are alternated between on a per sample basis. Each coefficient set consists of 9 coefficients that can be independently set. The center tap of the filter has a resolution of 18 bits and the LSB has a weight of 2^{-16}. The non-center taps have a resolution of 12-bits with programmable LSB weight of 2^{-10}, 2^{-11}, 2^{-12}, 2^{-13}, 2^{-14}, 2^{-15} or 2^{-16}. All non-center taps have the same LSB weight. The block diagram for *time varying filter* mode is shown in 図 7-6 and an alternate block diagram is given in 図 7-7 which shows the equivalent filter in an I/Q correction-type topology.

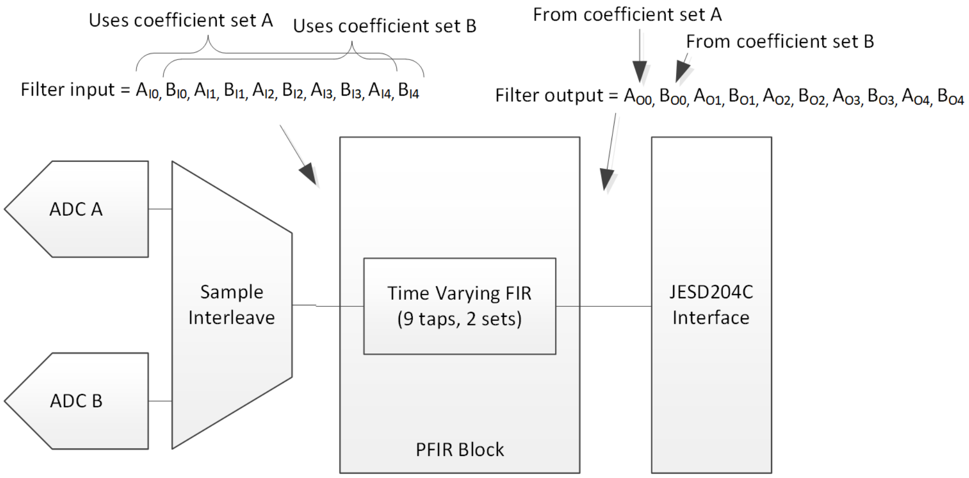

図 7-6. Time Varying Filter PFIR Block Diagram

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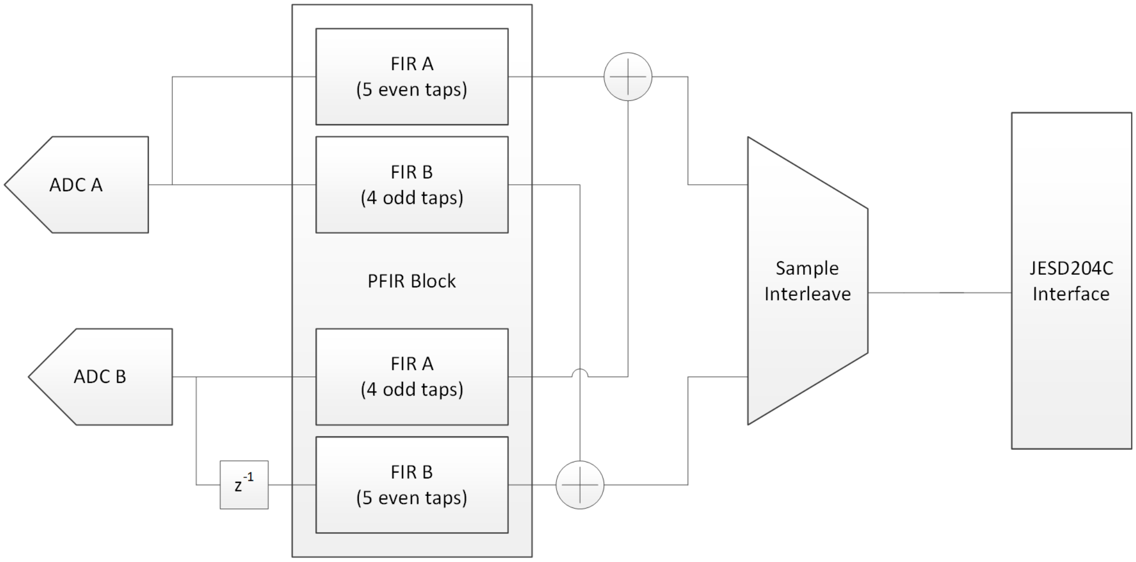

図 7-7. Alternate I/Q Correction-Type Filter Block Diagram

7.3.8 JESD204C Interface

The ADC08DJ5200RF uses a JESD204C high-speed serial interface for data converters to transfer data from the ADC to the receiving logic device. Many of the available JESD204C output formats are backwards compatible with existing JESD204B receivers, including many of the JESD204B modes in the ADC12DJ2700 and ADC12DJ3200. The device serialized lanes are capable of operating with both 8B/10B encoding and 64B/66B encoding. A maximum of 16 lanes can be used to lower lane rates for interfacing with speed-limited logic devices. There are a few differences between 8B/10B and 64B/66B encoded JESD204C, which will be described throughout this section. 図 7-8 shows a simplified block diagram of the 8B/10B encoded JESD204C interface and 図 7-9 shows a simplified block diagram of the 64B/66B encoded JESD204C interface.

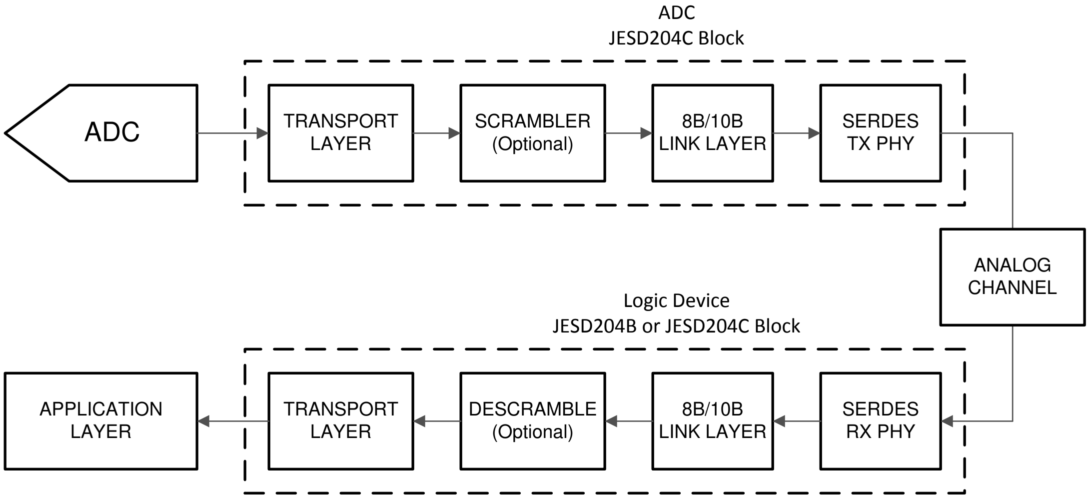

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図 7-8. Simplified 8B/10B Encoded JESD204C Interface Diagram

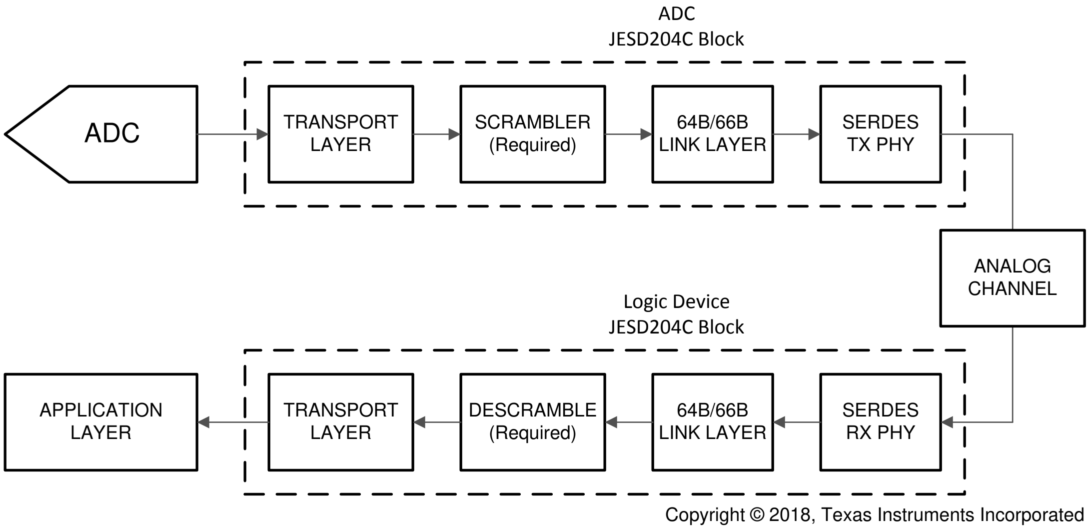

図 7-9. Simplified 64B/66B Encoded JESD204C Interface Diagram

The various signals used in the JESD204C interface and the associated the device pin names are summarized briefly in 表 7-9 for reference. Most of the signals are common between 8B/10B and 64B/66B encoded JESD204C, except for $\overline{\text{SYNC}}$ which is not needed to achieve block synchronization for 64B/66B encoding. The sync header encoded into the data stream is used for block synchronization instead of the $\overline{\text{SYNC}}$ signal.

表 7-9. Summary of JESD204C Signals

SIGNAL NAME	PIN NAMES	8B/10B	64B/66B	DESCRIPTION
Data	DA[7:0]+, DA[7:0]–, DB[7:0]+, DB[7:0]–)	Yes	Yes	High-speed serialized data after 8B/10B or 64B/66B encoding
$\overline{\text{SYNC}}$	$\overline{\text{SYNCSE}}$, TMSTP+, TMSTP–	Yes	No	Link initialization signal (handshake), toggles low to start code group synchronization (CGS) process. Not used for 64B/66B encoding modes, unless it is used for NCO synchronization purposes.
Device clock	CLK+, CLK–	Yes	Yes	ADC sampling clock, also used for clocking digital logic and output serializers
SYSREF	SYSREF+, SYSREF–	Yes	Yes	System timing reference used to deterministically reset the internal local multiframe clock (LMFC) or local extended multiblock clock (LEMC) counters in each JESD204C device

Not all optional features of JESD204C are supported by the device. The list of features that are supported and the features that are not supported is provided in 表 7-10.

表 7-10. Declaration of Supported JESD204C Features

LETTER IDENTIFIER	REFERENCE CLAUSE	FEATURE	SUPPORT IN ADC08DJ5200RF
a	clause 8	8B/10B link layer	Supported
b	clause 7	64B/66B link layer	Supported
c	clause 7	64B/80B link layer	Not supported

表 7-10. Declaration of Supported JESD204C Features (continued)

LETTER IDENTIFIER	REFERENCE CLAUSE	FEATURE	SUPPORT IN ADC08DJ5200RF
d	clause 7	The command channel when using the 64B/66B or 64B/80B link layer	Not supported
e	clause 7	Forward error correction (FEC) when using the 64B/66B or 64B/80B link layer	Supported
f	clause 7	CRC3 when using the 64B/66B or 64B/80B link layer	Not supported
g	clause 8	A physical $\overline{\text{SYNC}}$ pin when using the 8B/10B link layer	Supported
h	clause 7, clause 8	Subclass 0	Not supported, but subclass 1 transmitter is compatible with subclass 0 receiver
i	clause 7, clause 8	Subclass 1	Supported
j	clause 8	Subclass 2	Not supported
k	clause 7, clause 8	Lane alignment within a single link	Supported
l	clause 7, clause 8	Subclass 1 with support for a lane alignment on a multipoint link by means of the MULTIREF signal	Not supported
m	clause 8	$\overline{\text{SYNC}}$ interface timing is compatible with JESD204A	Supported
n	clause 8	$\overline{\text{SYNC}}$ interface timing is compatible with JESD204B	Supported

7.3.8.1 Transport Layer

The transport layer takes samples from the ADC output and maps the samples into octets inside of frames. The transport layer is common to both 8B/10B and 64B/66B encoding modes. These frames are then mapped onto the available lanes. The mapping of octets into frames and frames onto lanes is defined by the transport layer settings such as L, M, F, S, N and N'. An octet is 8 bits (before 8B/10B or 64B/66B encoding), a frame consists of F octets and the frames are mapped onto L lanes. Samples are N bits, but sent as N' bits across the link. The samples come from M converters and there are S samples per converter per frame cycle. M is sometimes artificially increased in order to obtain a more desirable mapping, for instance lower latency may be achieved with a larger M value for long frames.

There are a number of predefined transport layer modes in the device that are defined in . The high level configuration parameters for the transport layer in the device are described in 表 7-14. The transport layer mode is chosen by simply setting the JMODE register setting. For reference, the various configuration parameters for JESD204C are defined in 表 7-15.

The link layer further maps the frames into multiframes when using 8B/10B encoding or blocks, multiblocks and extended multiblocks when using 64B/66B encoding.

7.3.8.2 Scrambler

A data scrambler is available to scramble the data before transmission across the channel. Scrambling is used to remove the possibility of spectral peaks in the transmitted data due to repetitive data streams. The scrambler is optional for 8B/10B encoded modes, however it is mandatory for 64B/66B encoded modes in order to have sufficient spectral content for clock recovery and adaptive equalization and to maintain DC balance to allow AC coupling of the transmitter to the receiver. The scrambler operates on the data before encoding, such that the 8B/10B scrambler scrambles the 8-bit octets before 10-bit encoding and the 64B/66B scrambler scrambles the 64-bit block before the sync header insertion (66-bit encoding). The JESD204C receiver automatically synchronizes its descrambler to the incoming scrambled data stream. For 8B/10B encoding, the initial lane alignment sequence (ILA) is never scrambled. Scrambling can be enabled by setting SCR (in the JESD204C control register) for 8B/10B encoding modes, but it is automatically enabled in 64B/66B modes. The scrambling polynomial is different for 8B/10B encoding and 64B/66B encoding schemes as defined by the JESD204C standard.

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7.3.8.3 Link Layer

The link layer serves multiple purposes in JESD204C for both 8B/10B and 64B/66B encoding schemes, however there are some differences in implementation for each encoding scheme. In general, the link layer's responsibilities include scrambling of the data (see Scrambler), establishing the code (8B/10B) or block (64B/66B) boundaries and the multiframe (8B/10B) or multiblock (64B/66B) boundaries, initializing the link, encoding the data, and monitoring the health of the link. This section is split into an 8B/10B section (8B/10B Link Layer) and a 64B/66B section (64B/66B Link Layer) in order to cover the specific implementation for each encoding scheme.

7.3.8.4 8B/10B Link Layer

This section covers the link layer for the 8B/10B encoding operating modes including initialization of the character, frame and multiframe boundaries, alignment of the lanes, 8B/10B encoding and monitoring of the frame and multiframe alignment during operation.

7.3.8.4.1 Data Encoding (8B/10B)

The data link layer converts the 8-bit octets from the transport layer into 10-bit characters for transmission across the link using 8B/10B encoding. 8B/10B encoding specifies DC balance to allow use of AC-coupling between the SerDes transmitter and receiver, and maintains a sufficient number of edge transitions for the receiver to reliably recover the data clock. 8B/10B encoding also provides some error detection since a single bit error in a character likely results in either not being able to find the 10-bit character in the 8B/10B decoder lookup table or an incorrect character disparity.

7.3.8.4.2 Multiframes and the Local Multiframe Clock (LMFC)

The frames from the transport layer are combined into multiframes which are used in the process of achieving deterministic latency in subclass 1 implementations. The length of a multiframe is set by the K parameter which defines the number of frames in a multiframe. JESD204C increases the maximum allowed number of frames per multiframe (K) from 32 in JESD204B to 256 in JESD204C to allow a longer multi-frame to ease deterministic latency requirements. The total allowed range of K is defined by the inequality ceil(17/F) ≤ K ≤ min(256, floor(1024/F)) where ceil() and floor() are the ceiling and floor function, respectively. The local multiframe clock (LMFC) keeps track of the start and end of a multiframe for deterministic latency and data synchronization purposes. The LMFC is reset by the SYSREF signal to a deterministic phase in both the transmitter and receiver in order to act as a timing reference for deterministic latency. The LMFC clock frequency is given in 式 4 where f_{BIT} is the serialized bit rate (line rate) of the SerDes interface and F and K are as defined above. The frequency of SYSREF must equal to or an integer division of f_{LMFC} when using 8B/10B encoding modes if SYSREF is a continuous signal.

$$f_{LMFC} = f_{BIT} / (10 \times F \times K) \qquad (4)$$

7.3.8.4.3 Code Group Synchronization (CGS)

The first step in initializing the JESD204C link, after the LMFC is deterministically reset by SYSREF, is for the receiver to find the boundaries of the encoded 10-bit characters sent across each SerDes lane. This process is called code group synchronization (CGS). The receiver first asserts the $\overline{\text{SYNC}}$ signal (set to logic '0') when ready to initialize the link. The transmitter responds to the request by sending a stream of K28.5 comma characters. The receiver aligns its character clock to the K28.5 character sequence and CGS is achieved after successfully receiving four consecutive K28.5 characters. The receiver deasserts $\overline{\text{SYNC}}$ (set to logic '1') on the next LMFC edge after CGS is achieved and waits for the transmitter to start the initial lane alignment sequence (ILAS).

7.3.8.4.4 Initial Lane Alignment Sequence (ILAS)

After the transmitter detects the $\overline{\text{SYNC}}$ signal deassert (logic '0' to logic '1' transition), the transmitter waits until its next LMFC edge to start sending the initial lane alignment sequence (ILAS). The ILAS consists of four multiframes each containing a predetermined sequence. The receiver searches for the start of the ILAS to determine the frame and multiframe boundaries. Each multiframe of the ILAS starts with a /R/ character (K28.0) and ends with a /A/ character (K28.3) and either can be used to detect the boundary of a multiframe. Each lane starts buffering its data in the elastic buffer once the ILAS reaches the receiver, starting with the /R/ character, until all receivers have received the ILAS and subsequently release the ILAS from all lanes at the same time in

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order to align the lanes. The elastic buffer release point is chosen to avoid ambiguity in the release of the data caused by variation in the data delay (arrival of the ILAS at the receiver for each lane). The second multiframe of the ILAS contains configuration parameters for the JESD204C link configuration that can be used by the receiver to verify that the transmitter and receiver configurations match.

7.3.8.4.5 Frame and Multiframe Monitoring

The ADC08DJ5200RF supports frame and multiframe monitoring for verifying the health of the JESD204C link when using 8B/10B encoding. The scheme changes depending on the use of scrambling. The implementation when scrambling is disabled is covered first. If the last octet of the current frame matches the last octet of the previous frame, then the last octet of the current frame is encoded as an /F/ (K28.7) character. If the current frame is also the last frame of a multiframe, then an /A/ (K28.3) character is used instead. Neither an /F/ or /A/ character should occur in a normal data stream, except when replaced by the transmitter for alignment monitoring. When the receiver detects an /F/ or /A/ character in the normal data stream the receiver checks to see if the character occurs at the location expected to be the end of a frame or multiframe. If the character occurs at a location other than the end of a frame or multiframe then either the transmitter or receiver has become misaligned. The receiver replaces the alignment character with the appropriate data character upon reception of a properly aligned /F/ or /A/ character. The appropriate data character is the last octet of the previously received frame. This scheme increases the probability of an alignment character for non-scrambled data streams.

The implementation when scrambling is enabled is slightly different since the octets will be randomized. If the last octet of a frame is 0xFC (before 8B/10B encoding) then the transmitter encodes the octet as an /F/ (/K28.7/) character. If the last octet of a multiframe is 0x7C (before 8B/10B encoding) then the transmitter encodes the octet as an /A/ (/K28.3/) character. The location of the /A/ and /F/ characters is monitored to verify proper frame and multiframe alignment. The receiver replaces the alignment characters by simply replacing an /F/ character with the 0xFC octet and an /A/ character with the 0x7C octet.

The receiver can report an error if multiple alignment characters occur in the incorrect location or do not occur when expected. Upon detection of a frame or multiframe misalignment, the receiver should trigger a link realignment by asserting $\overline{\text{SYNC}}$. SYSREF should also be reissued to verify that the LMFC in the transmitter and receiver have proper alignment before restarting the link.

7.3.8.5 64B/66B Link Layer

This section covers the link layer for the 64B/66B encoding operating modes which includes scrambling of the data, addition of the sync headers (64B/66B encoding), the structure of the block and multiblock, the sync header, cyclic redundancy checking (CRC), forward error correction (FEC) and link alignment.

7.3.8.5.1 64B/66B Encoding

The frames formed by the transport layer are packed into 8-octet long blocks (64 bits). This 64-bit block is scrambled and then a 2-bit sync header (SH) is appended to form a 66-bit transmission block. The sync header is used for block synchronization by marking the end of a block as well as allowing for cyclic redundancy checking (CRC), forward error correction (FEC) or a command channel. The structure of a block is given in 表 7-11 where SH represents the appended 2-bit sync header.

表 7-11. Structure of 64B/66B Block with Sync Header

SH	OCTET0	OCTET1	OCTET2	OCTET3	OCTET4	OCTET5	OCTET6	OCTET7
[0:1]	[2:9]	[10:17]	[18:25]	[26:33]	[34:41]	[42:49]	[50:57]	[58:65]

7.3.8.5.2 Multiblocks, Extended Multiblocks and the Local Extended Multiblock Clock (LEMC)

A multiblock is a 32 block container which consists of a concatenation of 32 blocks. An extended multiblock is a concatenation of multiple multiblocks, where E defines the number of multiblocks in an extended multiblock. A frame can be split between blocks and multiblocks, but there must be an integer number of frames in an extended multiblock. An extended multiblock is only necessary when a multiblock does not have an integer number of frames. If an extended multiblock is not used, because a multiblock contains an integer number of frames, then the E parameter is equal to 1 to indicate that there is one multiblock in an extended multiblock. Values of E greater than 1 are not supported in ADC08DJ5200RF.

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An extended multiblock is analogous to a multiframe in the 8B/10B transport layer. The local extended mutiblock clock (LEMC) keeps track of the start and end of a multiblock for deterministic latency and data synchronization purposes in the same way the LMFC tracks the start and end of a multiframe in 8B/10B encoding. The LEMC is reset by the SYSREF signal to a deterministic phase in both the transmitter and receiver in order to act as a timing reference for deterministic latency. The LEMC clock frequency is defined by 式 5 where f_{BIT} is the serialized bit rate (line rate) of the SerDes interface. The frequency of SYSREF must equal to or an integer division of f_{LMFC} when using 64B/66B encoding modes if SYSREF is a continuous signal.

$$f_{LEMC} = f_{BIT} / (66 \times 32 \times E) \quad (5)$$

7.3.8.5.3 Block, Multiblock and Extended Multiblock Alignment using Sync Header

The sync header contains two bits that are always opposite of each other (either 01 or 10). The JESD204C receiver can find the block boundaries by looking for a 66-bit boundary that always contains a 0 to 1 or 1 to 0 transition. Although 0 to 1 and 1 to 0 transitions will occur at other locations in a block, it is impossible for the sequence to appear at a fixed location, other than the proper sync header location, in successive blocks for a long period of time. The sync header indicates the start of a block and can be used for block alignment monitoring. If a 00 or a 11 bit sequence is seen at the assumed sync header location of a block, then block alignment may have been lost. Multiple occurrences of incorrect sync header bits should trigger a search for the sync header after sending SYSREF to all devices to reset LEMC alignment.

A sync header ([0:1]) of 01 corresponds to transmission of a 1 while a sync header of 10 corresponds to a transmission of a 0. The transmitted bit from the sync header of each block of a multiblock are combined into a 32-bit word called the sync header stream. The sync header stream is used to transmit data in parallel with the user data in order to synchronize the link by marking the borders of multiblocks and extended multiblocks. In addition, the sync header stream provides one of either CRC, FEC or a command channel. The device supports CRC-12 and FEC and does not support CRC-3 or the command channel.

The 32-bit sync header stream always ends with a 00001 bit sequence, called the end-of-multiblock (EoMB) signal, that indicates the end of a multiblock. For CRC and command channel modes, a 00001 sequence will never occur in any other location in the sync header stream. For FEC mode, it is possible for a 00001 sequence to appear in another location within the sync header stream, however it is improbable to see the 00001 sequence in the same location within a sequence of multiple multiblocks. Therefore, in FEC mode it may take more than one multiblock to find the end of a multiblock. The end of an extended multiblock is found for all modes by monitoring bit 22 of the sync header stream, the EoEMB bit, which indicates the end of an extended multiblock when set to a 1. The EoMB (00001) and EoEMB signals, as well as fixed 1s in the sync header stream for CRC and command channel modes, form the pilot signal of the sync header stream.

The defined format for each form of the sync header stream are defined in the following sections.

7.3.8.5.3.1 Cyclic Redundancy Check (CRC) Mode

The cyclic redundancy check (CRC) mode is available to allow detection of potential bit errors during transmission. Support for the 12-bit word CRC-12 mode is required by JESD204C, while a 3-bit word CRC-3 mode is optional. The device does not support the CRC-3 mode and therefore this section is specific to the CRC-12 mode only. The transmitter computes the CRC-12 parity bits from the scrambled data bits of the 32 blocks of a multiblock. The 12-bit CRC parity word is then transmitted in the sync header stream of the next multiblock. The receiver computes the 12-bit parity word of the received multiblock and compares it against the received 12-bit parity word of the next multiblock. A difference indicates that there is at least one error in the received data bits or in the received 12-bit parity word. The minimum latency to the detection of a bit error in the first data bit of a multiblock is 46 blocks.

The mapping of the sync header stream when using the CRC-12 mode is shown in 表 7-12. CRC[x] corresponds to bit x of the 12-bit CRC word. Cmd[x] corresponds to bit x of the 7 bit command word, which are always set to 0's in the device. The 00001 bit sequence at the end of the sync header stream is the pilot signal that is used to identify the end of a multiblock. The 1s that occur throughout the sync header makes suer the pilot signal is only seen at the end of the sync header, allowing multiblock alignment after only a single multiblock has been received. EoEMB is the end-of-extended-multiblock bit, which is set to 1 for the last multiblock of an extended multiblock.

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表 7-12. Sync Header Stream Bit Mapping for CRC-12 Mode

Bit	Function	Bit	Function	Bit	Function	Bit	Function
0	CRC[11]	8	CRC[5]	16	Cmd[6]	24	Cmd[2]
1	CRC[10]	9	CRC[4]	17	Cmd[5]	25	Cmd[1]
2	CRC[9]	10	CRC[3]	18	Cmd[4]	26	Cmd[0]
3	1	11	1	19	1	27	0
4	CRC[8]	12	CRC[2]	20	Cmd[3]	28	0
5	CRC[7]	13	CRC[1]	21	1	29	0
6	CRC[6]	14	CRC[0]	22	EoEMB	30	0
7	1	15	1	23	1	31	1

The CRC-12 encoder takes in a multiblock of 32 scrambled blocks (2048 bits) and computes the 12-bit parity word using the generator polynomial given by 式 6. The polynomial is sufficient to detect all 2-bit errors in a multiblock, spanning any distance, and burst error sequences of up to 12-bits in length. The probability of not detecting a 3-bit error spanning any distance in a multiblock is approximately 0.004%.

$$0x987 == x^{12}+x^9+x^8+x^3+x^2+x+1 \tag{6}$$

The full parity bit generation for CRC-12 is shown in 図 7-10. The input is a 2048 bit sequence, built from the 32 scrambled blocks of a multiblock (sync header is not included). The 12-bit parity word, CRC[11:0], is taken from the S_X blocks after the full 2048 bit sequence is processed. The S_X blocks are initialized with 0's before processing each multiblock. For more information on the CRC-12 parity word generation, refer to the JESD204C standard.

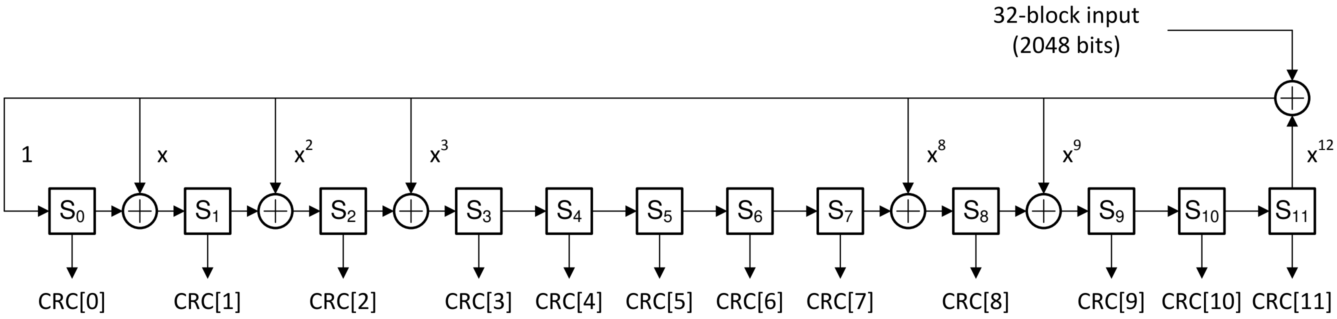

図 7-10. CRC-12 Parity Bit Generator

7.3.8.5.3.2 Forward Error Correction (FEC) Mode

Forward error correction (FEC) is an optional feature in JESD204C and is supported by the device. Whereas CRC-12 mode can only detect errors on the link, FEC is able to detect and correct errors in order to improve the bit error rate (BER) for error-sensitive applications. Many applications can tolerate random bit errors, however some applications, such as an oscilloscope, rely on long error-free measurements in order to detect a certain response from the device under test (DUT). An error in these applications may result in a false-positive detection of the response.

A scrambled multiblock of 32 blocks (2048 bits) is input into the FEC parity bit generator to generate the 26-bit parity word. The parity word is sent in the sync header stream of the next multiblock. The receiver then calculates its own 26-bit parity word and calculates the difference between the locally generated and received parity word, called the syndrome of the received bits. If the syndrome is 0, then all bits are assumed to have been received correctly, while any value other than 0 indicates at least one error in either the data bits or the parity word. If the syndrome is non-zero, then it can be used to determine the most likely error and then correct the error. The minimum latency from a bit error to detection and correct of a bit error in the first bit of a multiblock is 58 blocks.

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The mapping of the sync header stream when using FEC mode is shown in 表 7-13. FEC[x] corresponds to bit x of the 26-bit FEC word. The 00001 bit sequence at the end of the sync header stream is the pilot signal that is used to identify the end of a multiblock. It is possible for a 00001 sequence to appear in another location within the sync header stream in FEC mode, however it is improbable to see the 00001 sequence in the same location within a sequence of multiple multiblocks. Therefore, in FEC mode it may take more than one multiblock to find the end of a multiblock. EoEMB is the end-of-extended-multiblock bit, which is set to 1 for the last multiblock of an extended multiblock.

表 7-13. Sync Header Stream Bit Mapping for FEC Mode

Bit	Function	Bit	Function	Bit	Function	Bit	Function
0	FEC[25]	8	FEC[17]	16	FEC[9]	24	FEC[2]
1	FEC[24]	9	FEC[16]	17	FEC[8]	25	FEC[1]
2	FEC[23]	10	FEC[15]	18	FEC[7]	26	FEC[0]
3	FEC[22]	11	FEC[14]	19	FEC[6]	27	0
4	FEC[21]	12	FEC[13]	20	FEC[5]	28	0
5	FEC[20]	13	FEC[12]	21	FEC[4]	29	0
6	FEC[19]	14	FEC[11]	22	EoEMB	30	0
7	FEC[18]	15	FEC[10]	23	FEC[3]	31	1

The FEC encoder takes in a multiblock of 32 scrambled blocks (2048 bits) and computes the 26-bit parity word using the generator polynomial given by 式 7. The 2048 scrambled input bits plus 26 parity bits forms a shortened (2074, 2048) binary cyclic code. The (2074, 2048) binary cyclic code is shortened from the cyclic Fire code (8687, 8661). This polynomial can correct up to a 9-bit burst error per multiblock.

$$g(x) = (x^{17}+1)(x^{9}+x^{4}+1) == x^{26}+x^{21}+x^{17}+x^{9}+x^{4}+1 \tag{7}$$

The full 26-bit FEC parity word generation is shown in 図 7-11. The input is a 2048 bit sequence, built from the 32 scrambled blocks of a multiblock (sync header is not included). The 26-bit parity word, FEC[25:0], is taken from the S_x blocks after the full 2048 bit sequence is processed. The S_x blocks are initialized with 0's before processing each multiblock. For more information on the FEC parity word generation, refer to the JESD204C standard.

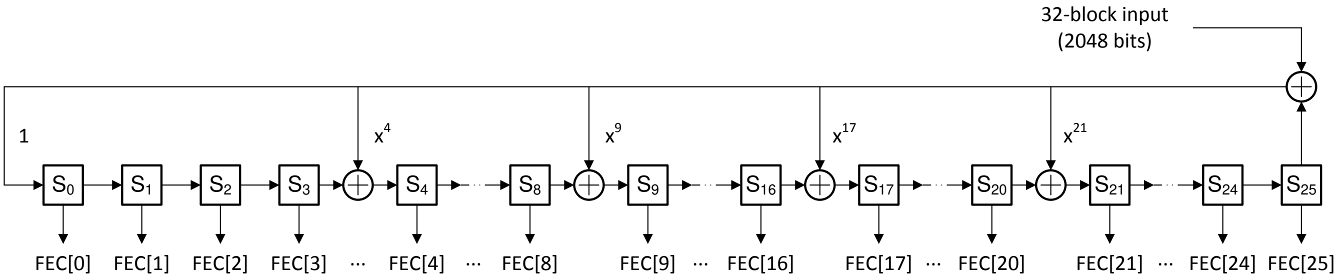

図 7-11. FEC Parity Bit Generator

FEC decoding and error correction are not covered here. For full details on FEC decoding and error correction, refer to the JESD204C standard.

7.3.8.5.4 Initial Lane Alignment

The 64B/66B link layer does not use an initial lane alignment sequence (ILAS) like the 8B/10B link layer. Therefore, the receiver must use a different scheme to align lanes using the elastic buffer. In 8B/10B mode, the ILAS triggers the elastic buffer to start buffering the data for each lane. After all lanes have started buffering the data, the elastic buffers for each lane are released at a release point determined by the release buffer delay (RBD) parameter and the phase of the LMFC. In 64B/66B mode, the process starts by having all lanes achieve block, multiblock and extended multiblock alignment. Once all lanes have achieved alignment, the receiver can begin buffering data in the elastic buffers at the start of the next extended multiblock on each lane. The data is released at the next release point after all lanes have seen the start of an extended multiblock and have started buffering the data. The release point is defined relative to the LEMC edge and the programmed RBD value, the most intuitive of which is to release on the LEMC edge itself. The release point must be chosen to avoid the region of the LEMC containing variation in the data delay on each lane from startup to startup.

7.3.8.5.5 Block, Multiblock and Extended Multiblock Alignment Monitoring

Synchronization of blocks, multiblocks and extended multiblocks by monitoring the sync header of each block and EoMB and EoEMB bit of the sync header stream. A block will always begin with a 0 to 1 or 1 to 0 transition (sync header). A single missed sync header can occur due to a bit error, however it there are a number of sync header errors within a set number of blocks, then block synchronization has been lost and block synchronization should be reinitialized. It is possible to still have block synchronization, but to lose multiblock or extended multiblock synchronization. Multiblock synchronization is monitored by looking for the EoMB signal, 00001, at the end of the sync header stream for each multiblock. If multiple EoMB signals are erroneous within a number of blocks, multiblock synchronization has been lost and multiblock synchronization should be reinitialized. If an erroneous EoEMB bit is received for multiple extended multiblocks within a number of extended multiblocks, such as a 1 for a multiblock that is not the end of an extended multiblock or a 0 for a multiblock that is the end of an extended multiblock, then multiblock synchronization is lost and extended multiblock synchronization should be reinitialized. If multiblock or extended multiblock synchronizaton is lost, SYSREF should be applied to the erroneous devices in order to reestablish the LEMC before the synchronization process begins.

7.3.8.6 Physical Layer

The JESD204C physical layer consists of a current mode logic (CML) output driver and receiver. The receiver consists of a clock detection and recovery (CDR) unit to extract the data clock from the serialized data stream and can contain a continuous time linear equalizer (CTLE) and/or discrete feedback equalizer (DFE) to correct for the low-pass response of the physical transmission channel. Likewise, the transmitter can contain pre-equalization to account for frequency dependent losses across the channel. The total reach of the SerDes links depends on the data rate, board material, connectors, equalization, noise and jitter, and required bit-error performance. The SerDes lanes do not have to be matched in length because the receiver aligns the lanes during the initial lane alignment sequence.

7.3.8.6.1 SerDes Pre-Emphasis

The device high-speed output drivers can pre-equalize the transmitted data stream by using pre-emphasis in order to compensate for the low-pass response of the transmission channel. Configurable pre-emphasis settings allow the output drive waveform to be optimized for different PCB materials and signal transmission distances. The pre-emphasis setting is adjusted through the serializer pre-emphasis setting SER_PE (in the serializer pre-emphasis control register). Higher values increase the pre-emphasis to compensate for more lossy PCB materials. This adjustment is best used in conjunction with an eye-diagram analysis capability in the receiver. Adjust the pre-emphasis setting to optimize the eye-opening for the specific hardware configuration and line rates needed.

7.3.8.7 JESD204C Enable

The JESD204C interface must be disabled through JESD_EN (in the JESD204C enable register) while any of the other JESD204C parameters are being changed. When JESD_EN is set to 0 the block is held in reset and the serializers are powered down. The clocks for this section are also gated off to further save power. When the parameters are set as desired, the JESD204C block can be enabled (JESD_EN is set to 1).

7.3.8.8 Multi-Device Synchronization and Deterministic Latency

JESD204C subclass 1 outlines a method to achieve deterministic latency across the serial link. If two devices achieve the same deterministic latency then they can be considered synchronized. This latency must be achieved from system startup to startup to be deterministic. There are two key requirements to achieve deterministic latency. The first is proper capture of SYSREF for which the device provides a number of features to simplify this requirement at giga-sample clock rates (see the *SYSREF Capture* section for more information). SYSREF resets either the LMFC in 8B/10B encoding mode or the LEMC is 64B/66B encoding mode. The LMFC and LEMC are analogous between the two modes and are now referred to as LMFC/LEMC.

The second requirement is to choose a proper elastic buffer release point in the receiver. Because the device is an ADC, the device is the transmitter (TX) in the JESD204C link and the logic device is the receiver (RX). The elastic buffer is the key block for achieving deterministic latency, and does so by absorbing variations in the propagation delays of the serialized data as the data travels from the transmitter to the receiver. A proper release point is one that provides sufficient margin against delay variations. An incorrect release point results in a latency variation of one LMFC/LEMC period. Choosing a proper release point requires knowing the average arrival time of data at the elastic buffer, referenced to an LMFC/LEMC edge, and the total expected delay variation for all devices. With this information the region of invalid release points within the LMFC/LEMC period can be defined, which stretches from the minimum to maximum delay for all lanes. Essentially, the designer must make sure the data for all lanes arrives at all devices after the previous release point occurs, and before the next release point occurs.

図 7-12 provides a timing diagram that demonstrates this requirement. In this figure, the data for two ADCs is shown. The second ADC has a longer routing distance (t_{PCB}) and results in a longer link delay. First, the invalid region of the LMFC/LEMC period is marked off as determined by the data arrival times for all devices. Then, the release point is set by using the release buffer delay (RBD) parameter to shift the release point an appropriate number of frame clocks from the LMFC/LEMC edge so that the release point occurs within the valid region of the LMFC/LEMC cycle. In the case of 図 7-12, the LMFC/LEMC edge (RBD = 0) is a good choice for the release point because there is sufficient margin on each side of the valid region.

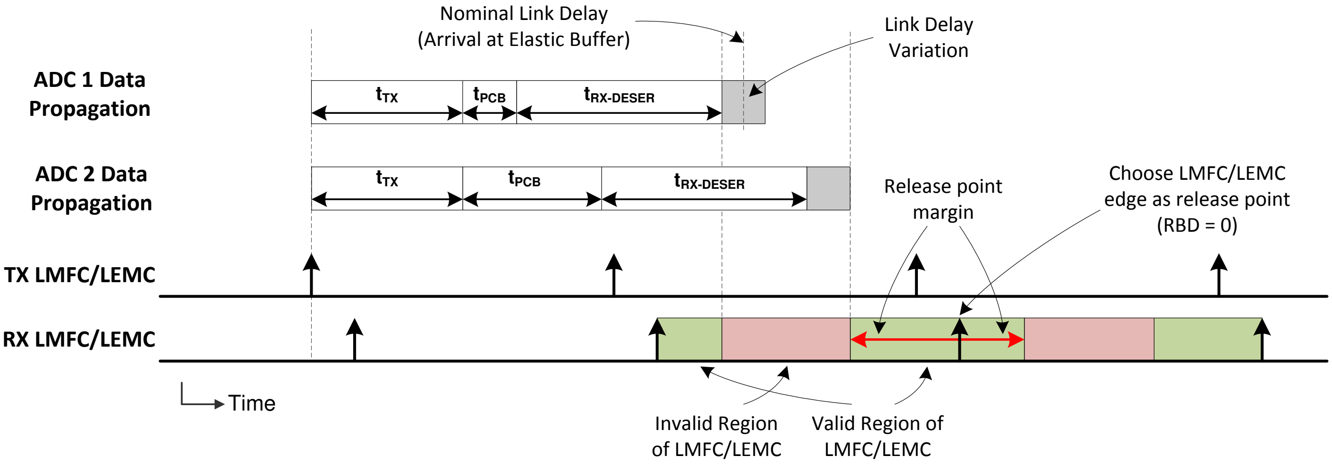

図 7-12. LMFC/LEMC Valid Region Definition for Elastic Buffer Release Point Selection

The TX and RX LMFC/LEMCs do not necessarily need to be phase aligned, but knowledge of their phase is important for proper elastic buffer release point selection. Also, the elastic buffer release point occurs within every LMFC/LEMC cycle, but the buffers only release when all lanes have arrived. Therefore, the total link delay can exceed a single LMFC/LEMC period; see *JESD204B multi-device synchronization: Breaking down the requirements* for more information.

7.3.8.9 Operation in Subclass 0 Systems

ADC08DJ5200RF can operate with subclass 0 compatibility provided that multi-ADC synchronization and deterministic latency are not required. With these limitations, the device can operate without the application of SYSREF. The internal LMFC/LEMC is automatically self-generated with unknown timing. SYNC is used as normal to initiate the CGS and ILAS in 8B/10B mode.

7.3.9 Alarm Monitoring

A number of built-in alarms are available to monitor internal events. Several types of alarms and upsets are detected by this feature:

1. Serializer FIFO alarm (FIFO overflow or underflow)
2. Serializer PLL is not locked
3. JESD204C link is enabled, but not transmitting data (not in the data transmission state)

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4. SYSREF causes internal clocks to be realigned
5. An upset that impacts the NCO phase
6. An upset that impacts the JESD204C clocks

When an alarm occurs, a bit for each specific alarm is set in ALM_STATUS. Each alarm bit remains set until the host system writes a 1 to clear the alarm. If the alarm type is not masked (see the alarm mask register), then the alarm is also indicated by the ALARM register. The CALSTAT output pin can be configured as an alarm output that goes high when an alarm occurs; see the CAL_STATUS_SEL bit in the calibration pin configuration register.

7.3.9.1 Clock Upset Detection

The CLK_ALM register bit indicates if the internal clocks have been upset. The clocks in channel A are continuously compared to channel B. If the clocks differ for even one DEVCLK / 2 cycle, the CLK_ALM register bit is set and remains set until cleared by the host system by writing a 1. For the CLK_ALM register bit to function properly, follow these steps:

1. Program JESD_EN = 0
2. The part must be configured to use both channels (PD_ACH = 0, PD_BCH = 0)
3. Program JESD_EN = 1
4. Write CLK_ALM = 1 to clear CLK_ALM
5. Monitor the CLK_ALM status bit or the CALSTAT output pin if CAL_STATUS_SEL is properly configured
6. When exiting global power-down (via MODE or the PD pin), the CLK_ALM status bit may be set and must be cleared by writing a 1 to CLK_ALM

7.3.9.2 FIFO Upset Detection

The FIFO_ALM bit indicates if an underflow or overflow condition has occurred on any of the JESD204C serializer lanes within the synchronizing FIFO between the digital logic block and serializer outputs. The FIFO_LANE_ALM register bits can be used to determine which lane triggered the underflow or overflow condition alarm. If the FIFO pointers are upset due to an undesired clock shift or other single event or incorrect clocking frequencies the FIFO_LANE_ALM bit for the erroneous lane will be set to 1. If the INIT_ON_FIFO_ALM bit is set then the serializers, FIFO and JESD204C block will automatically reinitialize.

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7.4 Device Functional Modes

The ADC08DJ5200RF can be configured to operate in a number of functional modes. These modes are described in this section.

7.4.1 Dual-Channel Mode

ADC08DJ5200RF can be used as a dual-channel ADC where the sampling rate is equal to the clock frequency ($f_S = f_{CLK}$) provided at the CLK+ and CLK– pins. The two inputs, AIN± and BIN±, serve as the respective inputs for each channel in this mode. This mode is chosen simply by setting JMODE to the appropriate setting for the desired configuration as described in . The analog inputs can be swapped by setting DUAL_INPUT (see the input mux control register). One channel can be powered down to operate ADC08DJ5200RF as a single channel at the maximum sampling rate of dual channel mode to save power compared to single channel mode operating at half the rate.

7.4.2 Single-Channel Mode (DES Mode)

The ADC08DJ5200RF can also be used as a single-channel ADC where the sampling rate is equal to two times the clock frequency ($f_S = 2 \times f_{CLK}$) provided at the CLK+ and CLK– pins. This mode effectively interleaves the two ADC channels together to form a single-channel ADC at twice the sampling rate. This mode is chosen simply by setting JMODE to the appropriate setting for the desired configuration as described in . INA± or INB±, can serve as the input to the ADC, however INA± is recommended for highest performance. The analog input can be selected using SINGLE_INPUT (see the input mux control register). A calibration needs to be performance after switching the input mux for the changes to take effect.

7.4.3 Dual-Input Single-Channel Mode (DUAL DES Mode)

The ADC08DJ5200RF can also be used as a single-channel ADC where the sampling rate is equal to two times the clock frequency ($f_S = 2 \times f_{CLK}$) provided at the CLK+ and CLK– pins. This mode interleaves the two channels by sampling them out-of-phase and each channel samples separate analog inputs (INA± and INB±). The effective sampling rate is twice the device clock input (CLK±). This mode is useful for sampling the output of interleaved track-and-hold analog front-ends. This mode is chosen by setting JMODE to a *single channel mode* as described in and setting SINGLE_INPUT to use both INA± and INB± (see the input mux control register). The digital processing and JESD204C interface operate as if the device is in single-channel mode sampling only one of the inputs.

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7.4.4 JESD204C Modes

The ADC08DJ5200RF can be programmed as a single-channel or dual-channel ADC and a number JESD204C output formats. 表 7-14 summarizes the basic operating mode configuration parameters and whether they are user configured or derived.

表 7-14. ADC08DJ5200RF Operating Mode Configuration Parameters

PARAMETER	DESCRIPTION	USER CONFIGURED OR DERIVED	VALUE
JMODE	JESD204C operating mode, automatically derives the rest of the JESD204C parameters, single-channel or dual-channel mode	User configured	Set by JMODE (see the JESD204C mode register)
DES	1 = single-channel mode, 0 = dual-channel mode	Derived	See *Operating Modes*
R	Number of bits transmitted per lane per CLK± cycle. The JESD204C line rate is the CLK± frequency times R. This parameter sets the SerDes PLL multiplication factor or controls bypassing of the SerDes PLL.	Derived	See *Operating Modes*
Links	Number of JESD204C links used	Derived	See *Operating Modes*
K	Number of frames per multiframe (8B/10B mode)	User configured	Set by KM1 (see the JESD204C K parameter register), see the allowed values in *Operating Modes*. This parameter is ignored in 64B/66B modes.
E	Number of multiblocks per extended multiblock (64B/66B mode)	Derived	Always set to '1' in ADC08DJ5200RF. This parameter is ignored in 8B/10B modes.

There are a number of parameters required to define the JESD204C transport layer format, all of which are sent across the link during the initial lane alignment sequence in 8B/10B mode. 64B/66B mode does not use the ILAS, however the transport layer uses the same parameters. In the ADC08DJ5200RF, most parameters are automatically derived based on the selected JMODE; however, a few are configured by the user. 表 7-15 describes these parameters.

表 7-15. JESD204C Initial Lane Alignment Sequence Parameters

PARAMETER	DESCRIPTION	USER CONFIGURED OR DERIVED	VALUE
ADJCNT	LMFC adjustment amount (not applicable)	Derived	Always 0
ADJDIR	LMFC adjustment direction (not applicable)	Derived	Always 0
BID	Bank ID	Derived	Always 0
CF	Number of control words per frame	Derived	Always 0
CS	Control bits per sample	Derived	Always set to 0 in ILAS, see *Operating Modes* for actual usage
DID	Device identifier, used to identify the link	User configured	Set by DID (see the JESD204C DID parameter register), see Lane Assignments
F	Number of octets (bytes) per frame (per lane)	Derived	See *Operating Modes*
HD	High-density format (samples split between lanes)	Derived	Always 0
JESDV	JESD204 standard revision	Derived	Always 1
K	Number of frames per multiframe	User configured	Set by the KM1 register, see the JESD204C K parameter register
L	Number of serial output lanes per link	Derived	See *Operating Modes*
LID	Lane identifier for each lane	Derived	See Lane Assignments
M	Number of converters used to determine lane bit packing; may not match number of ADC channels in the device	Derived	See *Operating Modes*
N	Sample resolution (before adding control and tail bits)	Derived	See *Operating Modes*
N'	Bits per sample after adding control and tail bits	Derived	See *Operating Modes*
S	Number of samples per converter (M) per frame	Derived	See *Operating Modes*
SCR	Scrambler enabled	User configured	Set by the JESD204C control register
SUBCLASSV	Device subclass version	Derived	Always 1
RES1	Reserved field 1	Derived	Always 0
RES2	Reserved field 2	Derived	Always 0
CHKSUM	Checksum for ILAS checking (sum of all above parameters modulo 256)	Derived	Computed based on parameters in this table

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7.4.4.1 JESD204C Operating Modes Table

表 7-16. ADC08DJ5200RF Operating Modes

ADC08DJ5200RF OPERATING MODE	USER-SPECIFIED PARAMETER		DERIVED PARAMETERS													INPUT CLOCK RANGE (MHz)
	JMODE	K [Min:Step:Max]	Encoding	DES	LINKS	N	CS	N’	L (Per Link)	M (Per Link)	F	S	HD	E	R (Fbit / Fclk)	
RESERVED	0-4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
8-bit, single channel, 8 lanes	5	32:16:256	8b/10b	1	2	8	0	8	4	1	1	4	0	—	2.5	800-5200
8-bit, single channel, 16 lanes	6	32:16:256	8b/10b	1	2	8	0	8	8	1	1	8	0	—	1.25	800-5200
8-bit, dual channel, 8 lanes	7	32:16:256	8b/10b	0	2	8	0	8	4	1	1	4	0	—	2.5	800-5200
8-bit, dual channel, 16 lanes	8	32:16:256	8b/10b	0	2	8	0	8	8	1	1	8	0	—	1.25	800-5200
RESERVED	9-33	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
8-bit, single channel, 4 lanes	34	256(1)	64b/66b	1	2	8	0	8	2	1	1	2	0	1	4.125	800-4160
8-bit, dual channel, 4 lanes	35	256(1)	64b/66b	0	2	8	0	8	2	1	1	2	0	1	4.125	800-4160
RESERVED	36-43	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
8-bit, single channel, 8 lanes	44	256(1)	64b/66b	1	2	8	0	8	4	1	1	4	0	1	2.0625	800-5200
8-bit, dual channel, 8 lanes	45	256(1)	64b/66b	0	2	8	0	8	4	1	1	4	0	1	2.0625	800-5200
RESERVED	46-49	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
8-bit, single channel, 16 lanes	50	256(1)	64b/66b	1	2	8	0	8	8	1	1	8	0	1	1.03125	800-5200
8-bit, dual channel, 16 lanes	51	256(1)	64b/66b	0	2	8	0	8	8	1	1	8	0	1	1.03125	800-5200
RESERVED	52-71	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

(1) In the 64B/66B modes, the K parameter is not directly programmable. K is related to E and F according to the equation K=8*32*E/F. K is not an actual parameter of the 64B/66B link layer.

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7.4.4.2 JESD204C Modes continued

Configuring the ADC08DJ5200RF is made easy by using a single configuration parameter called JMODE (see the JESD204C mode register). Using *Operating Modes*, the correct JMODE value can be found for the desired operating mode. The modes listed in *Operating Modes* are the only available operating modes. This table also gives a range and allowable step size for the K parameter (set by KM1, see the JESD204C K parameter register), which sets the multiframe length in number of frames.

The ADC08DJ5200RF has a total of 16 high-speed output drivers that are grouped into two 8-lane JESD204C links. All operating modes use two links with up to eight lanes per link. The lanes and their derived configuration parameters are described in the Lane Assignement and Parameters table. For a specified JMODE, the lowest indexed lanes for each link are used and the higher indexed lanes for each link are automatically powered down. Always route the lowest indexed lanes to the logic device.

表 7-17. ADC08DJ5200RF Lane Assignment and Parameters

DEVICE PIN DESIGNATION	JESD204C LINK	DID (User Configured)	LID (Derived)
DA0±	A	Set by DID (see the JESD204C DID parameter register), the effective DID is equal to the DID register setting (DID)	0
DA1±			1
DA2±			2
DA3±			3
DA4±			4
DA5±			5
DA6±			6
DA7±			7
DB0±	B	Set by DID (see the JESD204C DID parameter register), the effective DID is equal to the DID register setting plus 1 (DID+1)	0
DB1±			1
DB2±			2
DB3±			3
DB4±			4
DB5±			5
DB6±			6
DB7±			7

7.4.4.3 JESD204C Transport Layer Data Formats

Output data are formatted in a specific optimized fashion for each JMODE setting based on the transport layer settings for that JMODE. The 8-bit offset binary values are mapped into octets. The following tables show the specific mapping formats for a single frame for each JMODE. The symbol definitions used in the JMODE tables is provided in 表 7-18. In all mappings the tail bits (T) are 0 (zero). All samples are formatted as MSB first, LSB last.

表 7-18. JMODE Table Symbol Definitions

NOTATION	MODE	DESCRIPTION
S[n]	Single channel	Sample n from ADC in single channel mode
A[n]	Dual channel	Sample n from channel A in dual channel mode
B[n]	Dual channel	Sample n from channel A in dual channel mode
T	—	Tail bits, always set to 0

表 7-19. JMODE 5 (8-bit, Single Channel, 8 Lanes)

OCTET	0	
NIBBLE	0	1
DA0	S[0]	

表 7-19. JMODE 5 (8-bit, Single Channel, 8 Lanes) (continued)

OCTET	0	
NIBBLE	**0**	**1**
DA1	S[2]	
DA2	S[4]	
DA3	S[6]	
DB0	S[1]	
DB1	S[3]	
DB2	S[5]	
DB3	S[7]	

表 7-19 also applies to JMODE 44.

表 7-20. JMODE 6 (8-bit, Single Channel, 16 Lanes)

OCTET	0	
NIBBLE	**0**	**1**
DA0	S[0]	
DA1	S[2]	
DA2	S[4]	
DA3	S[6]	
DA4	S[8]	
DA5	S[10]	
DA6	S[12]	
DA7	S[14]	
DB0	S[1]	
DB1	S[3]	
DB2	S[5]	
DB3	S[7]	
DB4	S[9]	
DB5	S[11]	
DB6	S[13]	
DB7	S[15]	

表 7-20 also applies to JMODE 50.

表 7-21. JMODE 7 (8-bit, Dual Channel, 8 Lanes)

OCTET	0	
NIBBLE	**0**	**1**
DA0	A[0]	
DA1	A[1]	
DA2	A[2]	
DA3	A[3]	
DB0	B[0]	
DB1	B[1]	
DB2	B[2]	
DB3	B[3]	

表 7-21 also applies to JMODE 45.

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表 7-22. JMODE 8 (8-bit, Dual Channel, 16 Lanes)

OCTET	0	
NIBBLE	0	1
DA0	A[0]	
DA1	A[1]	
DA2	A[2]	
DA3	A[3]	
DA4	A[4]	
DA5	A[5]	
DA6	A[6]	
DA7	A[7]	
DB0	B[0]	
DB1	B[1]	
DB2	B[2]	
DB3	B[3]	
DB4	B[4]	
DB5	B[5]	
DB6	B[6]	
DB7	B[7]	

表 7-22 also applies to JMODE 51.

表 7-23. JMODE 34 (8-bit, Single Channel, 4 lanes)

OCTET	0	
NIBBLE	0	1
DA0	S[0]	
DA1	S[2]	
DB0	S[1]	
DB1	S[3]	

表 7-24. JMODE 35 (8-bit, Dual Channel, 4 lanes)

OCTET	0	
NIBBLE	0	1
DA0	A[0]	
DA1	A[1]	
DB0	B[0]	
DB1	B[1]	

7.4.4.4 64B/66B Sync Header Stream Configuration

The sync header stream can be used to identify bit errors on the link or to correct bit errors. Two modes of operation are available in the device. Cyclic redundancy checking (CRC) can be used to identify bit errors. The device only supports 12-bit CRC (CRC-12) and does not support the optional 3-bit CRC-3 described by JESD204C. Alternatively, forward error correction (FEC) can be used to identify bit errors and then correct bit errors. For information on CRC-12, see Cyclic Redundancy Check (CRC) Mode. For information on FEC, see Forward Error Correction (FEC) Mode. Set the sync header stream configuration by using the sync header mode register.

7.4.5 Power-Down Modes

The PD input pin allows the devices to be entirely powered down. Power-down can also be controlled by MODE (see the device configuration register). To power down only one channel in dual channel mode use the channel

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power down register. The serial data output drivers are disabled when PD is high. For proper operation in foreground calibration mode, ADC_OFF in the CAL_CFG register should be programmed to 0x1. When the device returns to normal operation, the JESD204 link must be re-established, and the ADC pipeline contain meaningless information so the system must wait a sufficient time for the data to be flushed.

7.4.6 Test Modes

A number of device test modes are available. These modes insert known patterns of information into the device data path for assistance with system debug, development, or characterization.

7.4.6.1 Serializer Test-Mode Details

Test modes are enabled by setting JTEST (see the JESD204C test pattern control register) to the desired test mode. Each test mode is described in detail in the following sections. Regardless of the test mode, the serializer outputs (number of lanes, rate) are powered up based on JMODE. Only enable the test modes when the JESD204C link is disabled. 図 7-13 provides a diagram showing the various test mode insertion points.

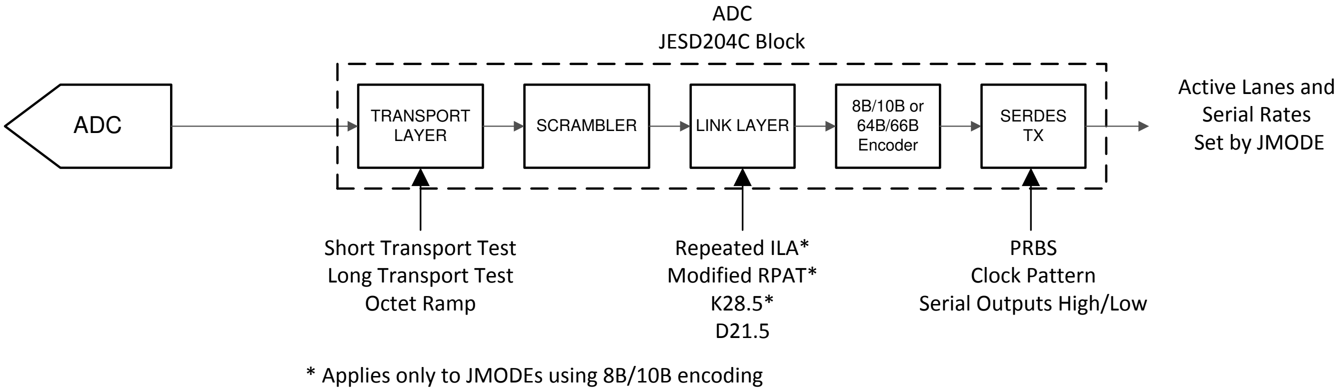

図 7-13. Test Mode Insertion Points

7.4.6.2 PRBS Test Modes

The PRBS test modes bypass the JESD204C transport layer and link layer and are therefore neither scrambled nor encoded. These test modes produce pseudo-random bit streams that comply with the ITU-T O.150 specification. These bit streams are used with lab test equipment or logic devices that can self-synchronize to the bit pattern. The initial phase of the pattern is not defined since the receiver self synchronizes.

The sequences are defined by a recursive equation. For example, 式 8 defines the PRBS7 sequence.

$$y[n] = y[n-6] \oplus y[n-7] \tag{8}$$

where

- bit n is the XOR of bit [n – 6] and bit [n – 7], which are previously transmitted bits

表 7-25 lists equations and sequence lengths for the available PRBS test modes where ⊕ is the XOR operation and y[n] represents bit n in the PRBS sequence. The initial phase of the pattern is unique for each lane.

表 7-25. PBRS Mode Equations

PRBS TEST MODE	SEQUENCE	SEQUENCE LENGTH (bits)
PRBS7	$y[n] = y[n-6] \oplus y[n-7]$	127
PRBS9	$y[n] = y[n-5] \oplus y[n-9]$	511
PRBS15	$y[n] = y[n-14] \oplus y[n-15]$	32,767
PRBS23	$y[n] = y[n-18] \oplus y[n-23]$	8,388,607
PRBS31	$y[n] = y[n-28] \oplus y[n-31]$	2,147,483,647

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7.4.6.3 Clock Pattern Mode

In the clock pattern mode, the JESD204C transport layer and link layer are bypassed, so the test sequence is neither scrambled nor encoded. The pattern consists of a 16-bit long sequence of 8 ones and 8 zeros (1111 1111 0000 0000) that repeats indefinitely.

7.4.6.4 Ramp Test Mode

In the ramp test mode, the JESD204C link layer operates normally, but the transport layer is disabled and the input from the formatter is ignored. In 8B/10B modes, the pattern begins after the ILA sequence finishes. In 64B/66B mode, the pattern begins after the serializers are initialized. Each lane transmits an identical octet stream that is encoded and scrambled by the link layer. The octet stream increments from 0x00 to 0xFF and repeats. This mode is available for both 8B/10B and 64B/66B modes.

7.4.6.5 Short and Long Transport Test Mode

JESD204C defines both short and long transport test modes to verify that the transport layers in the transmitter and receiver are operating correctly. The transport layer test modes are the same for 8B/10B mode and 64B/66B modes, since the transport layer is independent of the link layer.

7.4.6.5.1 Short Transport Test Pattern

Short transport test patterns send a predefined octet format that repeats every frame. In the ADC08DJ5200RF, all JMODE configurations use the short transport test pattern. The N' = 8 short transport test pattern is shown in 表 7-26. All applicable lanes are shown, however only the enabled lanes (lowest indexed) for the configured JMODE are used.

表 7-26. Short Transport Test Pattern for N' = 8 Modes (Length = 2 Frames)

FRAME	0	1
DA0	0x00	0xFF
DA1	0x01	0xFE
DA2	0x02	0xFD
DA3	0x03	0xFC
DB0	0x00	0xFF
DB1	0x01	0xFE
DB2	0x02	0xFD
DB3	0x03	0xFC

7.4.6.6 D21.5 Test Mode

In this test mode, the controller transmits a continuous stream of D21.5 characters (alternating 0s and 1s). This mode applies to 8B/10B and 64B/66B modes.

7.4.6.7 K28.5 Test Mode

In this test mode, the controller transmits a continuous stream of K28.5 characters. This mode only applies to 8B/10B modes.

7.4.6.8 Repeated ILA Test Mode

In this test mode, the JESD204C link layer operates normally, except that the ILA sequence (ILAS) repeats indefinitely instead of starting the data phase. Whenever the receiver issues a synchronization request, the transmitter initiates code group synchronization. Upon completion of code group synchronization, the transmitter repeatedly transmits the ILA sequence. This mode only applies to 8B/10B modes.

7.4.6.9 Modified RPAT Test Mode

A 12-octet repeating pattern is defined in INCITS TR-35-2004. The purpose of this pattern is to generate white spectral content for JESD204C compliance and jitter testing. 表 7-27 lists the pattern before and after 8B/10B encoding. This mode only applies to 8B/10B modes.

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表 7-27. Modified RPAT Pattern Values

OCTET NUMBER	Dx.y NOTATION	8-BIT INPUT TO 8B/10B ENCODER	20b OUTPUT OF 8B/10B ENCODER (Two Characters)
0	D30.5	0xBE	0x86BA6
1	D23.6	0xD7	
2	D3.1	0x23	0xC6475
3	D7.2	0x47	
4	D11.3	0x6B	0xD0E8D
5	D15.4	0x8F	
6	D19.5	0xB3	0xCA8B4
7	D20.0	0x14	
8	D30.2	0x5E	0x7949E
9	D27.7	0xFB	
10	D21.1	0x35	0xAA665
11	D25.2	0x59	

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7.4.7 Calibration Modes and Trimming

ADC08DJ5200RF has two calibration modes available: foreground calibration and background calibration. When foreground calibration is initiated the ADCs are automatically taken offline and the output data becomes mid-code (0x000 in 2's complement) while a calibration is occurring. Background calibration allows the ADC to continue normal operation while the ADC cores are calibrated in the background by swapping in a different ADC core to take its place. Additional offset calibration features are available in both foreground and background calibration modes. Further, a number of ADC parameters can be trimmed to optimize performance in a user system.

ADC08DJ5200RF consists of a total of six sub-ADCs, each referred to as a *bank*, with two banks forming an *ADC core*. The banks sample out-of-phase so that each ADC core is two-way interleaved. The six banks form three *ADC cores*, referred to as ADC A, ADC B, and ADC C. In foreground calibration mode, ADC A samples INA± and ADC B samples INB± in dual-channel mode and both ADC A and ADC B sample INA± (or INB±) in single-channel mode. In the background calibration modes, the third ADC core, ADC C, is swapped in periodically for ADC A and ADC B so that they can be calibrated without disrupting operation. 図 7-14 provides a diagram of the calibration system including labeling of the banks that make up each ADC core. When calibration is performed the linearity, gain and offset voltage for each bank are calibrated to an internally generated calibration signal. The analog inputs can be driven during calibration, in both foreground and background calibration, except that when offset calibration (OS_CAL or BGOS_CAL) is used there must be no signals (or aliased signals) near DC for proper estimation of the offset (see the *Offset Calibration* section).

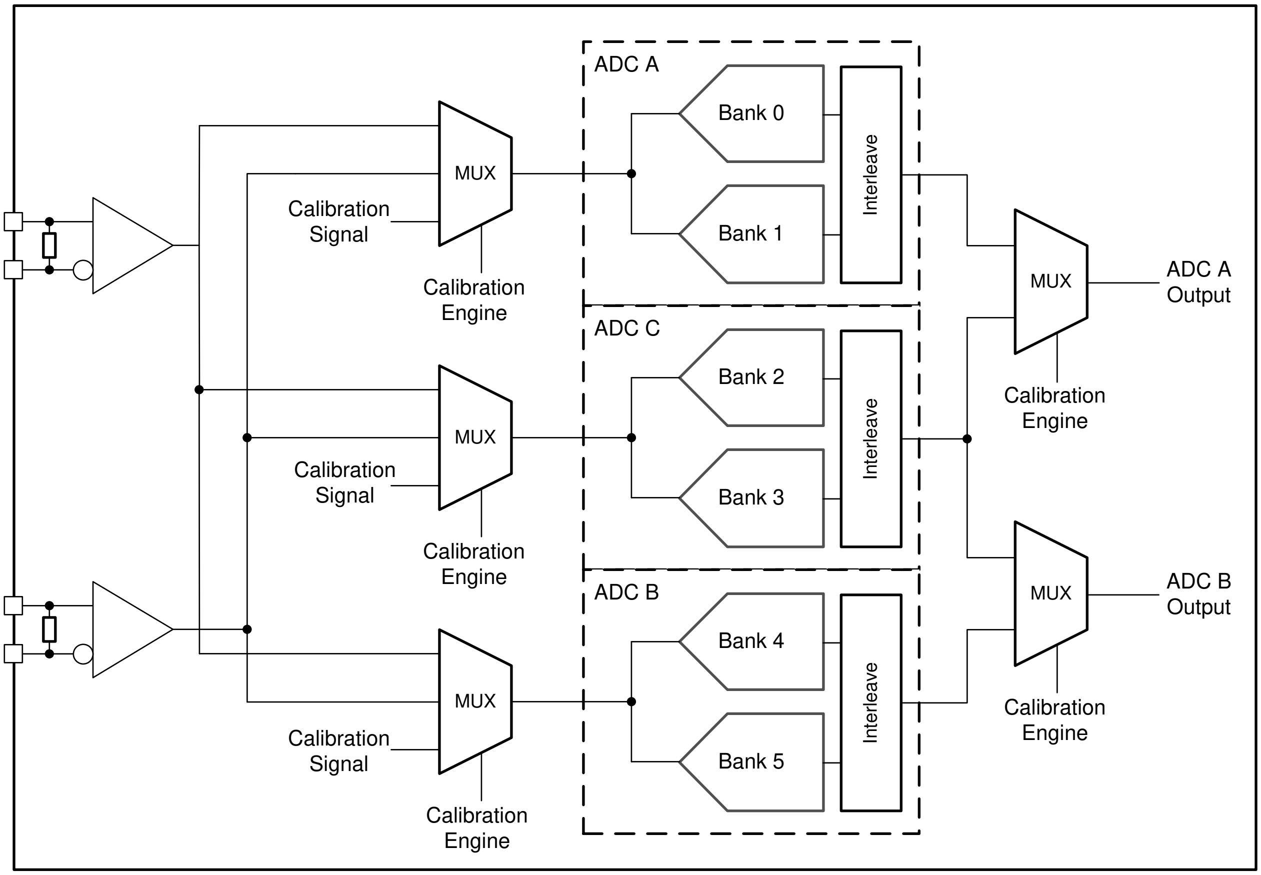

図 7-14. ADC08DJ5200RF Calibration System Block Diagram

In addition to calibration, a number of ADC parameters are user controllable to provide trimming for optimal performance. These parameters include input offset voltage, ADC gain, interleaving timing, and input termination resistance. The default trim values are programmed at the factory to unique values for each device that are determined to be optimal at the test system operating conditions. The user can read the factory-programmed values from the trim registers and adjust as desired. The register fields that control the trimming are labeled according to the input that is being sampled (INA± or INB±), the bank that is being trimmed, or the ADC core that is being trimmed. The user is not expected to change the trim values as operating conditions change, however optimal performance can be obtained by doing so. Any custom trimming must be done on a per device basis because of process variations, meaning that there is no global optimal setting for all parts. See the *Trimming* section for information about the available trim parameters and associated registers.

7.4.7.1 Foreground Calibration Mode

Foreground calibration requires the ADC to stop converting the analog input signals during the procedure. Foreground calibration always runs on power-up and the user must wait a sufficient time before programming the device to nake sure the calibration is finished. Foreground calibration can be initiated by triggering the calibration engine. The trigger source can be either the CAL_TRIG pin or CAL_SOFT_TRIG (see the calibration software trigger register) and is chosen by setting CAL_TRIG_EN (see the calibration pin configuration register).

7.4.7.2 Background Calibration Mode

Background calibration mode allows the ADC to continuously operate, with no interruption of data. This continuous operation is accomplished by activating an extra ADC core that is calibrated and then takes over operation for one of the other previously active ADC cores. When that ADC core is taken off-line, that ADC is calibrated and can in turn take over to allow the next ADC to be calibrated. This process operates continuously, ensuring the ADC cores always provide the optimum performance regardless of system operating condition changes. Because of the additional active ADC core, background calibration mode has increased power consumption in comparison to foreground calibration mode. The low-power background calibration (LPBG) mode discussed in the *Low-Power Background Calibration (LPBG) Mode* section provides reduced average power consumption in comparison with the standard background calibration mode. Background calibration can be enabled by setting CAL_BG (see the calibration configuration 0 register). CAL_TRIG_EN must be set to 0 and CAL_SOFT_TRIG must be set to 1.

Great care has been taken to minimize effects on converted data as the core switching process occurs, however, small brief glitches may still occur on the converter data as the cores are swapped.

7.4.7.3 Low-Power Background Calibration (LPBG) Mode

Low-power background calibration (LPBG) mode reduces the power-overhead of enabling additional ADC cores. Off-line cores are powered down until ready to be calibrated and put on-line. Set LP_EN = 1 to enable the low-power background calibration feature. LP_SLEEP_DLY is used to adjust the amount of time an ADC sleeps before waking up for calibration (if LP_EN = 1 and LP_TRIG = 0). LP_WAKE_DLY sets how long the core is allowed to stabilize before calibration and being put on-line. LP_TRIG is used to select between an automatic switching process or one that is controlled by the user via CAL_SOFT_TRIG or CAL_TRIG. In this mode there is an increase in power consumption during the ADC core calibration. The power consumption roughly alternates between the power consumption in foreground calibration when the spare ADC core is sleeping to the power consumption in background calibration when the spare ADC is being calibrated. Design the power-supply network to handle the transient power requirements for this mode. LPBG calibration mode is not recommended to be used in single channel operating modes.

7.4.8 Offset Calibration

Foreground calibration and background calibration modes inherently calibrate the offsets of the ADC cores; however, the input buffers sit outside of the calibration loop and therefore their offsets are not calibrated by the standard calibration process. In both dual-channel mode and single-channel mode, uncalibrated input buffer offsets result in a shift in the mid-code output (DC offset) with no input. Further, in single-channel mode uncalibrated input buffer offsets can result in a fixed spur at f_S / 2. A separate calibration is provided to correct the input buffer offsets.

There must be no signals at or near DC or aliased signals that fall at or near DC in order to properly calibration the offsets, requiring the system to specify this condition during normal operation or have the ability to mute the input signal during calibration. Foreground offset calibration is enabled via CAL_OS and only performs the calibration one time as part of the foreground calibration procedure. Background offset calibration is enabled via CAL_BGOS and continues to correct the offset as part of the background calibration routine to account for

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operating condition changes. When CAL_BGOS is set, the system must make sure there are no DC or near DC signals or aliased signals that fall at or near DC during normal operation. When background offset calibration is used the analog to digital conversion is disturbed by a bandwidth difference. The calibration time is relatively long becuase the offset calibration engine requires a lot of averaging. A preferred method for offset calibration is to use foreground calibration as a one-time operation so the timing of the disturbing glitch can be controlled. A one time foreground calibration can be performed by setting CAL_OS to 1 before setting CAL_EN. However, this will not correct for variations as operating conditions change.

The offset calibration correction uses the input offset voltage trim registers (see 表 7-28) to correct the offset and therefore must not be written by the user when offset calibration is used. The user can read the calibrated values by reading the OADJ_x_VINy registers, where x is the ADC core and y is the input (INA± or INB±), after calibration is completed. Only read the values when FG_DONE is read as 1 when using foreground offset calibration (CAL_OS = 1) and do not read the values when using background offset calibration (CAL_BGOS = 1).

7.4.9 Trimming

表 7-28 lists the parameters that can be trimmed and the associated registers. User trimming is limited to foreground (FG) calibration mode only.

表 7-28. Trim Register Descriptions

TRIM PARAMETER	TRIM REGISTER	NOTES
Band-gap reference	BG_TRIM	Measurement on BG output pin.
Input termination resistance	RTRIM_x, where x = A for INA± or B for INB±)	The device must be powered on with a clock applied.
Input offset voltage	OADJ_A_FG0_VINx, OADJ_A_FG90_VINx and OADJ_B_FG0_VINx, where OADJ_A applies to ADC core A and OADJ_B applies to ADC core B, FG0 applies to dual channel mode for ADC cores A and B and single channel mode for ADC core B, FG90 applies to ADC core A in single channel mode and x = A for INA± or B for INB±)	Input offset adjustment in dual channel mode consists of changing OADJ_A_FG0_VINA for channel A and OADJ_B_FG0_VINB for channel B. In single channel mode, OADJ_A_FG90_VINx and OADJ_B_FG0_VINx must be adjusted together to trim the input offset or adjusted separate to compensate the $f_S/2$ offset spur.
INA± and INB± gain	GAIN_xy_FGDUAL or GAIN_xy_FGDES, where x = ADC channel (A or B) and y = bank number (0 or 1)	Set FS_RANGE_A and FS_RANGE_B to default values before trimming the input. Use FS_RANGE_A and FS_RANGE_B to adjust the full-scale input voltage. The GAIN_xy_FGDUAL registers apply to Dual Channel Mode and the GAIN_xy_FGDES registers apply to the Single Channel Mode. To trim the gain of ADC core A or B, change GAIN_x0_FGDUAL and GAIN_x1_FGDUAL (or GAIN_x0_FGDES and GAIN_x1_FGDES) together in the same direction. To trim the gain of the two banks within ADC A or B, change GAIN_x0_FGDUAL and GAIN_x1_FGDUAL (or GAIN_x0_FGDES and GAIN_x1_FGDES) in opposite directions.
INA± and INB± full-scale input voltage	FS_RANGE_x, where x = A for INA± or B for INB±)	Full-scale input voltage adjustment for each input. The default value is effected by GAIN_Bx (x = 0, 1, 4 or 5). Trim GAIN_Bx with FS_RANGE_x set to the default value. FS_RANGE_x can then be used to trim the full-scale input voltage.
Intra-ADC core timing (bank timing)	Bx_TIME_y, where x = bank number (0, 1, 4 or 5) and y = 0° (0) or –90° (90) clock phase	Trims the timing between the two banks of an ADC core (ADC A or B). The 0° clock phase is used for dual channel mode and for ADC B in single channel mode. The –90° clock phase is used only for ADC A in single-channel mode. A mismatch in the timing between the two banks of an ADC core can result in an $f_S/2\text{-}f_{IN}$ spur in dual channel mode or $f_S/4 \pm f_{IN}$ spurs in single channel mode.
Inter-ADC core timing (dual-channel mode)	TADJ_A, TADJ_B	The suffix letter (A or B) indicates the ADC core that is being trimmed. Changing either TADJ_A or TADJ_B adjusts the sampling instance of ADC A relative to ADC B in dual channel mode.

表 7-28. Trim Register Descriptions (continued)

TRIM PARAMETER	TRIM REGISTER	NOTES
Inter-ADC core timing (single-channel mode)	TADJ_A_FG90_VINx, TADJ_B_FG0_VINx, where x = analog input (INA± or INB±)	These trim registers are used to adjust the timing of ADC core A relative to ADC core B in single channel mode. A mismatch in the timing will result in an $f_S/2-f_{IN}$ spur that is signal dependent. Changing either TADJ_A_FG90_VINx or TADJ_B_FG0_VINx changes the relative timing of ADC core A relative to ADC core B in single channel mode.

7.5 Programming

7.5.1 Using the Serial Interface

The serial interface is accessed using the following four pins: serial clock (SCLK), serial data in (SDI), serial data out (SDO), and serial interface chip-select ($\overline{\text{SCS}}$). Register access is enabled through the $\overline{\text{SCS}}$ pin.

7.5.1.1 $\overline{\text{SCS}}$

This signal must be asserted low to access a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

7.5.1.2 SCLK

Serial data input is accepted at the rising edge of this signal. SCLK has no minimum frequency requirement.

7.5.1.3 SDI

Each register access requires a specific 24-bit pattern at this input. This pattern consists of a read-and-write (R/W) bit, register address, and register value. The data are shifted in MSB first and multi-byte registers are always in little-endian format (least significant byte stored at the lowest address). Setup and hold times with respect to the SCLK must be observed (see the *Tining Requirements* table).

7.5.1.4 SDO

The SDO signal provides the output data requested by a read command. This output is high impedance during write bus cycles and during the read bit and register address portion of read bus cycles.

As shown in 図 7-15, each register access consists of 24 bits. The first bit is high for a read and low for a write.

The next 15 bits are the address of the register that is to be written to. During write operations, the last eight bits are the data written to the addressed register. During read operations, the last eight bits on SDI are ignored and, during this time, the SDO outputs the data from the addressed register. 図 7-15 shows the serial protocol details.

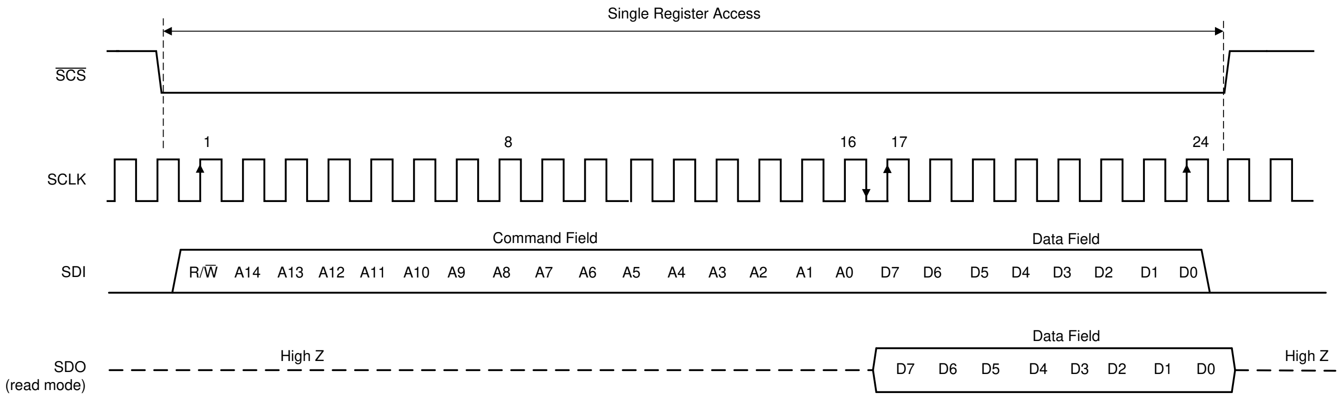

図 7-15. Serial Interface Protocol: Single Read/Write

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7.5.1.5 Streaming Mode

The serial interface supports streaming reads and writes. In this mode, the initial 24 bits of the transaction specifics the access type, register address, and data value as normal. Additional clock cycles of write or read data are immediately transferred, as long as the $\overline{\text{SCS}}$ input is maintained in the asserted (logic low) state. The register address auto increments (default) or decrements for each subsequent 8-bit transfer of the streaming transaction. The ADDR_ASC bit (register 000h, bits 5 and 2) controls whether the address value ascends (increments) or descends (decrements). Streaming mode can be disabled by setting the ADDR_HOLD bit (see the user SPI configuration register). 図 7-16 shows the streaming mode transaction details.

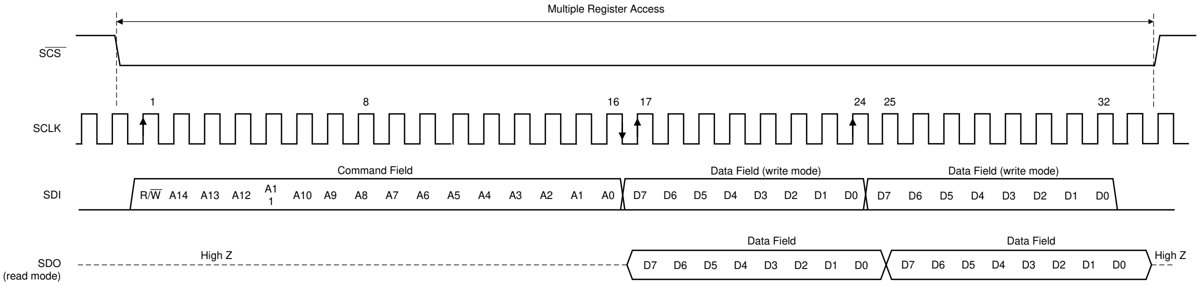

図 7-16. Serial Interface Protocol: Streaming Read/Write

See the *SPI Register Map* section for detailed information regarding the registers.

Note

The serial interface must not be accessed during ADC calibration. Accessing the serial interface during this time impairs the performance of the device until the device is calibrated correctly. Writing or reading the serial registers also reduces dynamic ADC performance for the duration of the register access time.

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7.6 SPI Register Map

表 7-29 lists the SPI_Register_Map registers. All register offset addresses not listed in 表 7-29 should be considered as reserved locations and the register contents should not be modified.

表 7-29. SPI REGISTER MAP Registers

Address	Acronym	Register Name	Section
0x0	CONFIG_A	Configuration A (default: 0x30)	Go
0x2	DEVICE_CONFIG	Device Configuration (default: 0x00)	Go
0x3	CHIP_TYPE	Chip Type (Default: 0x03)	Go
0x4	CHIP_ID	Chip Identification	Go
0xC	VENDOR_ID	Vendor Identification (Default = 0x0451)	Go
0x10	USR0	User SPI Configuration (Default: 0x00)	Go
0x29	CLK_CTRL0	Clock Control 0 (default: 0x00)	Go
0x2A	CLK_CTRL1	Clock Control 1 (default: 0x00)	Go
0x02B	CLK_CNTL2	Clock Control 2 (default: 0x11)	Go
0x2C	SYSREF_POS	SYSREF Capture Position (Read-Only, Default: undefined)	Go
0x30	FS_RANGE_A	FS_RANGE_A (default: 0xA000)	Go
0x32	FS_RANGE_B	FS_RANGE_B (default: 0xA000)	Go
0x38	BG_BYPASS	Band-Gap Bypass (default: 0x00)	Go
0x3B	TMSTP_CTRL	TMSTP Control (default: 0x00)	Go
0x48	SER_PE	Serializer Pre-Emphasis Control (default: 0x00)	Go
0x60	INPUT_MUX	Input Mux Control (default: 0x01)	Go
0x61	CAL_EN	Calibration Enable (Default: 0x01)	Go
0x62	CAL_CFG0	Calibration Configuration 0 (Default: 0x01)	Go
0x64	CAL_CFG2	Calibration Configuration 0 (Default: 0x02)	Go
0x68	CAL_AVG	Calibration Averaging (default: 0x61)	Go
0x6A	CAL_STATUS	Calibration Status (default: undefined) (read-only)	Go
0x6B	CAL_PIN_CFG	Calibration Pin Configuration (default: 0x00)	Go
0x6C	CAL_SOFT_TRIG	Calibration Software Trigger (default: 0x01)	Go
0x6E	CAL_LP	Low-Power Background Calibration (default: 0x88)	Go
0x70	CAL_DATA_EN	Calibration Data Enable (default: 0x00)	Go
0x71	CAL_DATA	Calibration Data (default: undefined)	Go
0x7A	GAIN_TRIM_A	Gain DAC Trim A (default from Fuse ROM)	Go
0x7B	GAIN_TRIM_B	Gain DAC Trim B (default from Fuse ROM)	Go
0x7C	BG_TRIM	Band-Gap Trim (default from Fuse ROM)	Go
0x7E	RTRIM_A	Resistor Trim for VinA (default from Fuse ROM)	Go
0x7F	RTRIM_B	Resistor Trim for VinB (default from Fuse ROM)	Go
0x9D	ADC_DITH	ADC Dither Control (default from Fuse ROM)	Go
0x160	LSB_CTRL	LSB Control Bit Output (default: 0x00)	Go
0x200	JESD_EN	JESD204C Subsystem Enable (default: 0x01)	Go
0x201	JMODE	JESD204C Mode (default: 0x02)	Go
0x202	KM1	JESD204C K Parameter (default: 0x1F)	Go
0x203	JSYNC_N	JESD204C Manual Sync Request (default: 0x01)	Go
0x204	JCTRL	JESD204C Control (default: 0x03)	Go
0x205	JTEST	JESD204C Test Control (default: 0x00)	Go
0x206	DID	JESD204C DID Parameter (default: 0x00)	Go
0x207	FCHAR	JESD204C Frame Character (default: 0x00)	Go

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表 7-29. SPI REGISTER MAP Registers (continued)

Address	Acronym	Register Name	Section
0x208	JESD_STATUS	JESD204C / System Status Register	Go
0x209	PD_CH	JESD204C Channel Power Down (default: 0x00)	Go
0x20A	JEXTRA_A	JESD204C Extra Lane Enable (Link A) (default: 0x00)	Go
0x20B	JEXTRA_B	JESD204C Extra Lane Enable (Link B) (default: 0x00)	Go
0x20F	SHMODE	JESD204C Sync Word Mode (default: 0x00)	Go
0x211	OVR_T0	Over-range Threshold 0 (default: 0xF2)	Go
0x212	OVR_T1	Over-range Threshold 1 (default: 0xAB)	Go
0x213	OVR_CFG	Over-range Enable / Hold Off (default: 0x07)	Go
0x270	INIT_STATUS	Initialization Status (read-only)	Go
0x297	SPIN_ID	Chip Spin Identifier (default: See description, read-only)	Go
0x2A2	TESTBUS	Analog Test Bus Control (default: 0x00)	Go
0x2B0	SRC_EN	SYSREF Calibration Enable (default: 0x00)	Go
0x2B1	SRC_CFG	SYSREF Calibration Configuration (default: 0x05)	Go
0x2B2	SRC_STATUS	SYSREF Calibration Status (read-only, default: undefined)	Go
0x2B5	TAD	DEVCLK Timing Adjust (default: 0x00)	Go
0x2B8	TAD_RAMP	DEVCLK Timing Adjust Ramp Control (default: 0x00)	Go
0x2C0	ALARM	Alarm Interrupt (read-only)	Go
0x2C1	ALM_STATUS	Alarm Status (default: 0x3F, write to clear)	Go
0x2C2	ALM_MASK	Alarm Mask Register (default: 0x3F)	Go
0x2C4	FIFO_LANE_ALM	FIFO Overflow/Underflow Alarm (default: 0xFFFF)	Go
0x310	TADJ_A	Timing Adjust for A-ADC operating in Dual Channel Mode (default from Fuse ROM)	Go
0x313	TADJ_B	Timing Adjust for B-ADC operating in Dual Channel Mode (default from Fuse ROM)	Go
0x314	TADJ_A_FG90_VINA	Timing Adjust for A-ADC operating in Single Channel Mode and sampling INA± (default from Fuse ROM)	Go
0x315	TADJ_B_FG0_VINA	Timing Adjust for B-ADC operating in Single Channel Mode and sampling INA± (default from Fuse ROM)	Go
0x31A	TADJ_A_FG90_VINB	Timing Adjust for A-ADC operating in Single Channel Mode and sampling INB± (default from Fuse ROM)	Go
0x31B	TADJ_B_FG0_VINB	Timing Adjust for B-ADC operating in Single Channel Mode and sampling INB± (default from Fuse ROM)	Go
0x344	OADJ_A_FG0_VINA	Offset Adjustment for A-ADC operating in Dual Channel Mode sampling INA± (default from Fuse ROM)	Go
0x346	OADJ_A_FG0_VINB	Offset Adjustment for A-ADC operating in Dual Channel Mode sampling INB± (default from Fuse ROM)	Go
0x348	OADJ_A_FG90_VINA	Offset Adjustment for A-ADC operating in Single Channel Mode sampling INA± (default from Fuse ROM)	Go
0x34A	OADJ_A_FG90_VINB	Offset Adjustment for A-ADC operating in Single Channel Mode sampling INB± (default from Fuse ROM)	Go
0x34C	OADJ_B_FG0_VINA	Offset Adjustment for B-ADC sampling INA± (default from Fuse ROM)	Go
0x34E	OADJ_B_FG0_VINB	Offset Adjustment for B-ADC sampling INB± (default from Fuse ROM)	Go
0x350	GAIN_A0_FGDUAL	Fine Gain Adjust for ADC A Bank 0 in Dual Channel Mode (default from Fuse ROM)	Go
0x351	GAIN_A1_FGDUAL	Fine Gain Adjust for ADC A Bank 1 in Dual Channel Mode (default from Fuse ROM)	Go
0x352	GAIN_B0_FGDUAL	Fine Gain Adjust for ADC B Bank 0 in Dual Channel Mode (default from Fuse ROM)	Go
0x353	GAIN_B1_FGDUAL	Fine Gain Adjust for ADC B Bank 1 in Dual Channel Mode (default from Fuse ROM)	Go
0x354	GAIN_A0_FGDES	Fine Gain Adjust for ADC A Bank 0 in Single Channel Mode (default from Fuse ROM)	Go
0x355	GAIN_A1_FGDES	Fine Gain Adjust for ADC A Bank 1 in Single Channel Mode (default from Fuse ROM)	Go

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表 7-29. SPI REGISTER MAP Registers (continued)

Address	Acronym	Register Name	Section
0x356	GAIN_B0_FGDES	Fine Gain Adjust for ADC B Bank 0 in Single Channel Mode (default from Fuse ROM)	Go
0x357	GAIN_B1_FGDES	Fine Gain Adjust for ADC B Bank 1 in Single Channel Mode (default from Fuse ROM)	Go
0x400	PFIR_CFG	Programmable FIR Mode (default: 0x00)	Go
0x418	PFIR_A0	PFIR Coefficient A0	Go
0x41A	PFIR_A1	PFIR Coefficient A1	Go
0x41C	PFIR_A2	PFIR Coefficient A2	Go
0x41E	PFIR_A3	PFIR Coefficient A3	Go
0x420	PFIR_A4	PFIR Coefficient A4	Go
0x423	PFIR_A5	PFIR Coefficient A5	Go
0x425	PFIR_A6	PFIR Coefficient A6	Go
0x427	PFIR_A7	PFIR Coefficient A7	Go
0x429	PFIR_A8	PFIR Coefficient A8	Go
0x448	PFIR_B0	PFIR Coefficient B0	Go
0x44A	PFIR_B1	PFIR Coefficient B1	Go
0x44C	PFIR_B2	PFIR Coefficient B2	Go
0x44E	PFIR_B3	PFIR Coefficient B3	Go
0x450	PFIR_B4	PFIR Coefficient B4	Go
0x453	PFIR_B5	PFIR Coefficient B5	Go
0x455	PFIR_B6	PFIR Coefficient B6	Go
0x457	PFIR_B7	PFIR Coefficient B7	Go
0x459	PFIR_B8	PFIR Coefficient B8	Go

Complex bit access types are encoded to fit into small table cells. 表 7-30 shows the codes that are used for access types in this section.

表 7-30. SPI_Register_Map Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

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7.6.1 CONFIG_A Register (Address = 0x0) [reset = 0x30]

CONFIG_A is shown in 図 7-17 and described in 表 7-31.

Return to the Summary Table.

Configuration A (default: 0x30)

図 7-17. CONFIG_A Register

7	6	5	4	3	2	1	0
SOFT_RESET	RESERVED	ASCEND	SDO_ACTIVE	RESERVED			
R/W-0x0	R/W-0x0	R/W-0x1	R-0x1	R/W-0x0			

表 7-31. CONFIG_A Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SOFT_RESET	R/W	0x0	Setting this bit causes a full reset of the chip and all SPI registers (including CONFIG_A). This bit is self-clearing. After writing this bit, the part may take up to 750ns to reset. During this time, do not perform any SPI transactions.
6	RESERVED	R/W	0x0	
5	ASCEND	R/W	0x1	0 : Address is decremented during streaming reads/writes 1 : Address is incremented during streaming reads/writes (default)
4	SDO_ACTIVE	R	0x1	Always returns 1. Always use SDO for SPI reads. No SDIO mode supported.
3:0	RESERVED	R/W	0x0	

7.6.2 DEVICE_CONFIG Register (Address = 0x2) [reset = 0x00]

DEVICE_CONFIG is shown in 図 7-18 and described in 表 7-32.

Return to the Summary Table.

Device Configuration (default: 0x00)

図 7-18. DEVICE_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED						MODE	
R/W-0x0						R/W-0x0	

表 7-32. DEVICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0x0	
1:0	MODE	R/W	0x0	0 : Normal operation (default) 1 : Reserved 2 : Reserved 3 : Power down (lowest power, slower resume)

7.6.3 CHIP_TYPE Register (Address = 0x3) [reset = 0x03]

CHIP_TYPE is shown in 図 7-19 and described in 表 7-33.

Return to the Summary Table.

Chip Type (Default: 0x03)

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図 7-19. CHIP_TYPE Register

7	6	5	4	3	2	1	0
RESERVED				CHIP_TYPE			
R/W-0x0				R-0x3			

表 7-33. CHIP_TYPE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	
3:0	CHIP_TYPE	R	0x3	Always returns 0x3, indicating that the part is a high speed ADC.

7.6.4 CHIP_ID Register (Address = 0x4) [reset = 0x0]

CHIP_ID is shown in 図 7-20 and described in 表 7-34.

Return to the Summary Table.

Chip Identification

図 7-20. CHIP_ID Register

15	14	13	12	11	10	9	8
CHIP_ID							
R-0x0							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CHIP_ID							
R-0x0							

表 7-34. CHIP_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	CHIP_ID	R	0x0	Returns 0x0021 indicating the device is in the ADCrrDJssssRF family.

7.6.5 VENDOR_ID Register (Address = 0xC) [reset = 0x0]

VENDOR_ID is shown in 図 7-21 and described in 表 7-35.

Return to the Summary Table.

Vendor Identification (Default = 0x0451)

図 7-21. VENDOR_ID Register

15	14	13	12	11	10	9	8
VENDOR_ID							
R-0x0							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
VENDOR_ID							
R-0x0							

表 7-35. VENDOR_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	VENDOR_ID	R	0x0	Always returns 0x0451 (Vendor ID for Texas Instruments)

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7.6.6 USR0 Register (Address = 0x10) [reset = 0x00]

USR0 is shown in 図 7-22 and described in 表 7-36.

Return to the Summary Table.

User SPI Configuration (Default: 0x00)

図 7-22. USR0 Register

7	6	5	4	3	2	1	0
RESERVED							ADDR_HOLD
R/W-0x0							R/W-0x0

表 7-36. USR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	
0	ADDR_HOLD	R/W	0x0	0 : Use ASCEND register to select address ascend/descend mode (default) 1 : Address stays constant throughout streaming operation; useful for reading and writing calibration vector information at the CAL_DATA register

7.6.7 CLK_CTRL0 Register (Address = 0x29) [reset = 0x00]

CLK_CTRL0 is shown in 図 7-23 and described in 表 7-37.

Return to the Summary Table.

Clock Control 0 (default: 0x00)

図 7-23. CLK_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED	SYSREF_PROC_EN	SYSREF_RECV_EN	SYSREF_ZOOM	SYSREF_SEL			
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0			

表 7-37. CLK_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	
6	SYSREF_PROC_EN	R/W	0x0	This bit enables the SYSREF processor, which allows the device to process SYSREF events (default: disabled). SYSREF_RECV_EN must be set before setting SYSREF_PROC_EN.
5	SYSREF_RECV_EN	R/W	0x0	Set this bit to enable the SYSREF receiver circuit (default: disabled)
4	SYSREF_ZOOM	R/W	0x0	Set this bit to zoom in the SYSREF windowing status and delays (impacts SYSERF_POS and SYSREF_SEL). When set, the delays used in the SYSREF windowing feature (reported in the SYSREF_POS register) become smaller. Use SYSREF_ZOOM for high clock rates, specifically when multiple SYSREF valid windows are encountered in the SYSREF_POS register; see the SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing) section.

表 7-37. CLK_CTRL0 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3:0	SYSREF_SEL	R/W	0x0	Set this field to select which SYSREF delay to use. Set this field based on the results returned by SYSREF_POS; see the SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing) section. These bits must be set to 0 to use SYSREF calibration; see the Automatic SYSREF Calibration section.

7.6.8 CLK_CTRL1 Register (Address = 0x2A) [reset = 0x00]

CLK_CTRL1 is shown in 図 7-24 and described in 表 7-38.

Return to the Summary Table.

Clock Control 1 (default: 0x00)

図 7-24. CLK_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED				SYSREF_TIME_STAMP_EN	DEVCLK_LVPECL_EN	SYSREF_LVPECL_EN	SYSREF_INVERTED
R/W-0x0				R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

表 7-38. CLK_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	
3	SYSREF_TIME_STAMP_EN	R/W	0x0	The SYSREF signal can be observed on the LSB of the JESD204C output samples when SYSREF_TIMESTAMP_EN and TIME_STAMP_EN are both set. This bit allows SYSREF± to be used as the timestamp input.
2	DEVCLK_LVPECL_EN	R/W	0x0	Activate DC-coupled, low-voltage PECL mode for CLK±; see the Pin Functions table.
1	SYSREF_LVPECL_EN	R/W	0x0	Activate DC-coupled, low-voltage PECL mode for SYSREF±; see the Pin Functions table.
0	SYSREF_INVERTED	R/W	0x0	This bit inverts the SYSREF signal used for alignment.

7.6.9 CLK_CTRL2 Register (Address = 0x02B) [reset = 0x11]

CLK_CTRL2 is shown in and described in 図 7-25 and described in 表 7-39.

Return to the Summary Table.

Clock Control 2 (default: 0x11)

図 7-25. CLK_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED			C_CLK_FEEDBACK_GAIN	Reserved	EN_VA11_NOISE_SUPPR	CLKSAMP_DEL	
R/W-0x0			R/W-0x1	R/W-0x0	R/W-0x0	R/W-0x1	

表 7-39. CLK_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	

表 7-39. CLK_CTRL2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	C_CLK_FEEDBACK_GAIN	R/W	0x1	Adjustable feedback gain for CMLtoCMOS converter (high gain:1)
3	Reserved	R/W	0x0	Reserved
2	EN_VA11_NOISE_SUPPR	R/W	0x0	When set, noise on VA11 is suppressed. It is recommended to have this set, as it reduces noise coupling from the digital circuits to analog clock, at the expense of a small increase in power.
1:0	CLKSAMP_DEL	R/W	0x1	Adjustable delay for the sampling clock (one hot encoded)

7.6.10 SYSREF_POS Register (Address = 0x2C) [reset = 0x0]

SYSREF_POS is shown in 図 7-26 and described in 表 7-40.

Return to the Summary Table.

SYSREF Capture Position (Read-Only, Default: undefined)

図 7-26. SYSREF_POS Register

23	22	21	20	19	18	17	16
SYSREF_POS							
R/W-0x0							
15	14	13	12	11	10	9	8
SYSREF_POS							
R/W-0x0							
7	6	5	4	3	2	1	0
SYSREF_POS							
R/W-0x0							

表 7-40. SYSREF_POS Register Field Descriptions

Bit	Field	Type	Reset	Description
23:0	SYSREF_POS	R/W	0x0	Returns a 24-bit status value that indicates the position of the SYSREF edge with respect to CLK±. Use this to program SYSREF_SEL.

7.6.11 FS_RANGE_A Register (Address = 0x30) [reset = 0xA000]

FS_RANGE_A is shown in 図 7-27 and described in 表 7-41.

Return to the Summary Table.

FS_RANGE_A (default: 0xA000)

図 7-27. FS_RANGE_A Register

15	14	13	12	11	10	9	8
FS_RANGE_A							
R/W-0xA000							
7	6	5	4	3	2	1	0
FS_RANGE_A							
R/W-0xA000							

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表 7-41. FS_RANGE_A Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FS_RANGE_A	R/W	0xA000	These bits enable adjustment of the analog full-scale range for INA±. 0x0000: Settings below 0x2000 result in degraded performance 0x2000: 500 mVPP - Recommended minimum setting 0xA000: 800 mVPP (default) 0xFFFF: 1000 mVPP - Maximum setting

7.6.12 FS_RANGE_B Register (Address = 0x32) [reset = 0xA000]

FS_RANGE_B is shown in 図 7-28 and described in 表 7-42.

Return to the Summary Table.

FS_RANGE_B (default: 0xA000)

図 7-28. FS_RANGE_B Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="8">FS_RANGE_B</td></tr>
<tr><td colspan="8">R/W-0xA000</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">FS_RANGE_B</td></tr>
<tr><td colspan="8">R/W-0xA000</td></tr>
</table>

表 7-42. FS_RANGE_B Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FS_RANGE_B	R/W	0xA000	These bits enable adjustment of the analog full-scale range for INB±. 0x0000: Settings below 0x2000 result in degraded performance 0x2000: 500 mVPP - Recommended minimum setting 0xA000: 800 mVPP (default) 0xFFFF: 1000 mVPP - Maximum setting

7.6.13 BG_BYPASS Register (Address = 0x38) [reset = 0x00]

BG_BYPASS is shown in 図 7-29 and described in 表 7-43.

Return to the Summary Table.

Band-Gap Bypass (default: 0x00)

図 7-29. BG_BYPASS Register

<table>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="7">RESERVED</td><td>BG_BYPASS</td></tr>
<tr><td colspan="7">R/W-0x0</td><td>R/W-0x0</td></tr>
</table>

表 7-43. BG_BYPASS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	
0	BG_BYPASS	R/W	0x0	When set, VA11 is used as the voltage reference instead of the band-gap voltage.

7.6.14 TMSTP_CTRL Register (Address = 0x3B) [reset = 0x00]

TMSTP_CTRL is shown in 図 7-30 and described in 表 7-44.

Return to the Summary Table.

TMSTP Control (default: 0x00)

図 7-30. TMSTP_CTRL Register

7	6	5	4	3	2	1	0
RESERVED						TMSTP_LVPECL_EN	TMSTP_RECV_EN
R/W-0x0						R/W-0x0	R/W-0x0

表 7-44. TMSTP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0x0	
1	TMSTP_LVPECL_EN	R/W	0x0	When set, activates the low voltage PECL mode for the differential TMSTP± input.
0	TMSTP_RECV_EN	R/W	0x0	Enables the differential differential TMSTP± input.

7.6.15 SER_PE Register (Address = 0x48) [reset = 0x00]

SER_PE is shown in 図 7-31 and described in 表 7-45.

Return to the Summary Table.

Serializer Pre-Emphasis Control (default: 0x00)

図 7-31. SER_PE Register

7	6	5	4	3	2	1	0
RESERVED				SER_PE_BOOST	SER_PE		
R/W-0x0				R/W-0x0	R/W-0x0		

表 7-45. SER_PE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	
3	SER_PE_BOOST	R/W	0x0	Additional pre-emphasis boost that increases the pre-emphasis slightly and extends it in time.
2:0	SER_PE	R/W	0x0	Sets the pre-emphasis for the SerDes output lanes. Pre-emphasis can be used to compensate for the high-frequency loss of the PCB trace. This is a global setting that affects all 16 lanes (DA[7:0]±, DB[7:0]±).

7.6.16 INPUT_MUX Register (Address = 0x60) [reset = 0x01]

INPUT_MUX is shown in 図 7-32 and described in 表 7-46.

Return to the Summary Table.

Input Mux Control (default: 0x01)

図 7-32. INPUT_MUX Register

7	6	5	4	3	2	1	0

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図 7-32. INPUT_MUX Register (continued)

RESERVED	DUAL_INPUT	RESERVED	SINGLE_INPUT
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x1

表 7-46. INPUT_MUX Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	
4	DUAL_INPUT	R/W	0x0	Select inputs for dual channel modes. If JMODE is selecting a single channel mode, this register has no effect. 0: A channel samples INA±, B channel samples INB± (no swap) (default) 1: A channel samples INB±, B channel samples INA± (swap)
3:2	RESERVED	R/W	0x0	
1:0	SINGLE_INPUT	R/W	0x1	Defines which input is sampled in single channel mode. If JMODE is not selecting a single channel mode, this register has no effect. 0: RESERVED 1: INA± is used (default) 2: INB± is used 3: ADC channel A samples INA± and ADC channel B samples INB± (DUAL DES mode). A calibration needs to be performance after switching the input mux for the changes to take effect.

7.6.17 CAL_EN Register (Address = 0x61) [reset = 0x01]

CAL_EN is shown in 図 7-33 and described in 表 7-47.

Return to the Summary Table.

Calibration Enable (Default: 0x01)

図 7-33. CAL_EN Register

7	6	5	4	3	2	1	0
RESERVED							CAL_EN
R/W-0x0							R/W-0x1

表 7-47. CAL_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	
0	CAL_EN	R/W	0x1	Calibration Enable. Set high to run calibration. Set low to hold calibration in reset to program new calibration settings. Clearing CAL_EN also resets the clock dividers that clock the digital block and JESD204C interface. Some calibration registers require clearing CAL_EN before making any changes. All registers with this requirement contain a note in their descriptions. After changing the registers, set CAL_EN to re-run calibration with the new settings. Always set CAL_EN before setting JESD_EN. Always clear JESD_EN before clearing CAL_EN.

7.6.18 CAL_CFG0 Register (Address = 0x62) [reset = 0x01]

CAL_CFG0 is shown in 図 7-34 and described in 表 7-48.

Return to the Summary Table.

Calibration Configuration 0 (Default: 0x01)

図 7-34. CAL_CFG0 Register

7	6	5	4	3	2	1	0
RESERVED				CAL_BGOS	CAL_OS	CAL_BG	CAL_FG
R/W-0x0				R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x1

表 7-48. CAL_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	
3	CAL_BGOS	R/W	0x0	0 : Disable background offset calibration (default) 1 : Enable background offset calibration (requires CAL_BG to be set).
2	CAL_OS	R/W	0x0	0 : Disable foreground offset calibration (default) 1 : Enable foreground offset calibration (requires CAL_FG to be set).
1	CAL_BG	R/W	0x0	0 : Disable background calibration (default) 1 : Enable background calibration
0	CAL_FG	R/W	0x1	0 : Reset calibration values, skip foreground calibration. 1 : Reset calibration values, then run foreground calibration (default).

7.6.19 CAL_CFG2 Register (Address = 0x64) [reset = 0x02]

CAL_CFG2 is shown in 図 7-35and described in 表 7-49.

Return to the Summary Table.

Calibration Configuration 2 (Default: 0x02)

図 7-35. CAL_CFG2 Register

7	6	5	4	3	2	1	0
RESERVED						ADC_OFF	
R/W-0x00						R/W-0x10	

表 7-49. CAL_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0x00	Reserved
1:0	ADC_OFF	R/W	0x1	If background calibration is disabled, this selects which ADC will be disabled and never calibrated. Only change ADC_OFF while JESD_EN is 0. 0 : ADC0 (ADC1 will stand in for ADC0) 1 : ADC1 2 : ADC2 (ADC1 will stand in for ADC2) 3 : Reserved

7.6.20 CAL_AVG Register (Address = 0x68) [reset = 0x61]

CAL_AVG is shown in 図 7-36 and described in 表 7-50.

Return to the Summary Table.

Calibration Averaging (default: 0x61)

図 7-36. CAL_AVG Register

7	6	5	4	3	2	1	0

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図 7-36. CAL_AVG Register (continued)

RESERVED	OS_AVG	RESERVED	CAL_AVG
R/W-0x0	R/W-0x6	R/W-0x0	R/W-0x1

表 7-50. CAL_AVG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	
6:4	OS_AVG	R/W	0x6	Select the amount of averaging used for the offset correction routine. A larger number corresponds to more averaging.
3	RESERVED	R/W	0x0	
2:0	CAL_AVG	R/W	0x1	Select the amount of averaging used for the linearity calibration routine. A larger number corresponds to more averaging.

7.6.21 CAL_STATUS Register (Address = 0x6A) [reset = 0x0]

CAL_STATUS is shown in 図 7-37 and described in 表 7-51.

Return to the Summary Table.

Calibration Status (default: undefined) (read-only)

図 7-37. CAL_STATUS Register

7	6	5	4	3	2	1	0
RESERVED			CAL_STAT			CAL_STOPPED	FG_DONE
R-0x0			R-0x0			R-0x0	R-0x0

表 7-51. CAL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	
4:2	CAL_STAT	R	0x0	Calibration status code
1	CAL_STOPPED	R	0x0	This bit returns a 1 when background calibration is successfully stopped at the requested phase. This bit returns a 0 when calibration starts operating again. If background calibration is disabled, this bit is set when foreground calibration is completed or skipped.
0	FG_DONE	R	0x0	This bit is high to indicate that foreground calibration has completed (or was skipped).

7.6.22 CAL_PIN_CFG Register (Address = 0x6B) [reset = 0x00]

CAL_PIN_CFG is shown in 図 7-38 and described in 表 7-52.

Return to the Summary Table.

Calibration Pin Configuration (default: 0x00)

図 7-38. CAL_PIN_CFG Register

7	6	5	4	3	2	1	0
RESERVED					CAL_STATUS_SEL		CAL_TRIG_EN
R/W-0x0					R/W-0x0		R/W-0x0

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表 7-52. CAL_PIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0x0	
2:1	CAL_STATUS_SEL	R/W	0x0	0 : CALSTAT output matches FG_DONE. 1 : CALSTAT output matches CAL_STOPPED. 2 : CALSTAT output matches ALARM. 3 : CALSTAT output is always low.
0	CAL_TRIG_EN	R/W	0x0	This bit selects the hardware or software trigger source. 0 : Use the CAL_SOFT_TRIG register for the calibration trigger. The CALTRIG input is disabled (ignored). 1 : Use the CALTRIG input for the calibration trigger. The CAL_SOFT_TRIG register is ignored.

7.6.23 CAL_SOFT_TRIG Register (Address = 0x6C) [reset = 0x01]

CAL_SOFT_TRIG is shown in 図 7-39 and described in 表 7-53.

Return to the Summary Table.

Calibration Software Trigger (default: 0x01)

図 7-39. CAL_SOFT_TRIG Register

7	6	5	4	3	2	1	0
RESERVED							CAL_SOFT_TRIG
R/W-0x0							R/W-0x1

表 7-53. CAL_SOFT_TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	
0	CAL_SOFT_TRIG	R/W	0x1	CAL_SOFT_TRIG is a software bit to provide the functionality of the CALTRIG input pin when there are no hardware resources to drive CALTRIG. Program CAL_TRIG_EN=0 to use CAL_SOFT_TRIG for the calibration trigger. Note: If no calibration trigger is needed, leave CAL_TRIG_EN=0 and CAL_SOFT_TRIG=1 (trigger set high).

7.6.24 CAL_LP Register (Address = 0x6E) [reset = 0x88]

CAL_LP is shown in 図 7-40 and described in 表 7-54.

Return to the Summary Table.

Low-Power Background Calibration (default: 0x88)

図 7-40. CAL_LP Register

7	6	5	4	3	2	1	0
LP_SLEEP_DLY			LP_WAKE_DLY		RESERVED	LP_TRIG	LP_EN
R/W-0x4			R/W-0x1		R/W-0x0	R/W-0x0	R/W-0x0

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表 7-54. CAL_LP Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	LP_SLEEP_DLY	R/W	0x4	These bits adjust how long an ADC sleeps before waking for calibration (only applies when LP_EN = 1 and LP_TRIG = 0). Values below 4 are not recommended because of limited overall power reduction benefits. 0: Sleep delay = (23 + 1) × 256 × tCLK 1: Sleep delay = (215 + 1) × 256 × tCLK 2: Sleep delay = (218 + 1) × 256 × tCLK 3: Sleep delay = (221 + 1) × 256 × tCLK 4: Sleep delay = (224 + 1) × 256 × tCLK (default, approximately 1.338 seconds with a 3.2-GHz clock) 5: Sleep delay = (227 + 1) × 256 × tCLK 6: Sleep delay = (230 + 1) × 256 × tCLK 7: Sleep delay = (233 + 1) × 256 × tCLK
4:3	LP_WAKE_DLY	R/W	0x1	These bits adjust how much time is provided for settling before calibrating an ADC after the ADC wakes up (only applies when LP_EN = 1). Values lower than 1 are not recommended because there is insufficient time for the core to stabilize before calibration begins. 0: Wake delay = (23 + 1) × 256 × tCLK 1: Wake delay = (218 + 1) × 256 × tCLK (default, approximately 21 ms with a 3.2-GHz clock) 2: Wake delay = (221 + 1) × 256 × tCLK 3: Wake delay = (224 + 1) × 256 × tCLK
2	RESERVED	R/W	0x0	
1	LP_TRIG	R/W	0x0	0 : ADC sleep duration is set by LP_SLEEP_DLY (autonomous mode). 1 : ADCs sleep until awoken by a trigger. An ADC is awoken when the calibration trigger is low.
0	LP_EN	R/W	0x0	0 : Disable low-power background calibration (default) 1 : Enable low-power background calibration (only applies when CAL_BG=1).

7.6.25 CAL_DATA_EN Register (Address = 0x70) [reset = 0x00]

CAL_DATA_EN is shown in 図 7-41 and described in 表 7-55.

Return to the Summary Table.

Calibration Data Enable (default: 0x00)

図 7-41. CAL_DATA_EN Register

7	6	5	4	3	2	1	0
RESERVED							CAL_DATA_EN
R/W-0x0							R/W-0x0

表 7-55. CAL_DATA_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	

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表 7-55. CAL_DATA_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	CAL_DATA_EN	R/W	0x0	Set this bit to enable the CAL_DATA register to enable reading and writing of calibration data; see the CAL_DATA register for more information.

7.6.26 CAL_DATA Register (Address = 0x71) [reset = 0x0]

CAL_DATA is shown in 図 7-42 and described in 表 7-56.

Return to the Summary Table.

Calibration Data (default: undefined)

図 7-42. CAL_DATA Register

7	6	5	4	3	2	1	0
CAL_DATA							
R/W-0x0							

表 7-56. CAL_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	CAL_DATA	R/W	0x0	After setting CAL_DATA_EN, repeated reads of this register return all calibration values for the ADCs. Repeated writes of this register input all calibration values for the ADCs. To read the calibration data, read the register 673 times. To write the vector, write the register 673 times with previously stored calibration data. To speed up the read or write operation, set ADDR_HOLD = 1 and use streaming read or write process. IMPORTANT: Accessing the CAL_DATA register when CAL_STOPPED = 0 corrupts the calibration. Also, stopping the process before reading or writing 673 times leaves the calibration data in an invalid state.

7.6.27 GAIN_TRIM_A Register (Address = 0x7A) [reset = 0x0]

GAIN_TRIM_A is shown in 図 7-43 and described in 表 7-57.

Return to the Summary Table.

Gain DAC Trim A (default from Fuse ROM)

図 7-43. GAIN_TRIM_A Register

7	6	5	4	3	2	1	0
GAIN_TRIM_A							
R/W-0x0							

表 7-57. GAIN_TRIM_A Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	GAIN_TRIM_A	R/W	0x0	This register enables gain trim of INA±. After reset, the factory trimmed value can be read and adjusted as required. Use FS_RANGE_A to adjust the analog full-scale voltage (Vfs) of INA±.

7.6.28 GAIN_TRIM_B Register (Address = 0x7B) [reset = 0x0]

GAIN_TRIM_B is shown in 図 7-44 and described in 表 7-58.

Return to the Summary Table.

Gain DAC Trim B (default from Fuse ROM)

図 7-44. GAIN_TRIM_B Register

7	6	5	4	3	2	1	0
GAIN_TRIM_B							
R/W-0x0							

表 7-58. GAIN_TRIM_B Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	GAIN_TRIM_B	R/W	0x0	This register enables gain trim of INB±. After reset, the factory trimmed value can be read and adjusted as required. Use FS_RANGE_B to adjust the analog full-scale voltage (Vfs) of INB±.

7.6.29 BG_TRIM Register (Address = 0x7C) [reset = 0x0]

BG_TRIM is shown in 図 7-45 and described in 表 7-59.

Return to the Summary Table.

Band-Gap Trim (default from Fuse ROM)

図 7-45. BG_TRIM Register

7	6	5	4	3	2	1	0
RESERVED				BG_TRIM			
R/W-0x0				R/W-0x0			

表 7-59. BG_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	
3:0	BG_TRIM	R/W	0x0	This register enables trimming of the internal band-gap reference. After reset, the factory trimmed value can be read and adjusted as required.

7.6.30 RTRIM_A Register (Address = 0x7E) [reset = 0x0]

RTRIM_A is shown in 図 7-46 and described in 表 7-60.

Return to the Summary Table.

Resistor Trim for VinA (default from Fuse ROM)

図 7-46. RTRIM_A Register

7	6	5	4	3	2	1	0
RTRIM_A							
R/W-0x0							

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表 7-60. RTRIM_A Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RTRIM_A	R/W	0x0	This register controls the INA± ADC input termination trim. After reset, the factory trimmed value can be read and adjusted as required.

7.6.31 RTRIM_B Register (Address = 0x7F) [reset = 0x0]

RTRIM_B is shown in 図 7-47 and described in 表 7-61.

Return to the Summary Table.

Resistor Trim for VinB (default from Fuse ROM)

図 7-47. RTRIM_B Register

7	6	5	4	3	2	1	0
RTRIM_B							
R/W-0x0							

表 7-61. RTRIM_B Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RTRIM_B	R/W	0x0	This register controls the INB± ADC input termination trim. After reset, the factory trimmed value can be read and adjusted as required.

7.6.32 ADC_DITH Register (Address = 0x9D) [reset = 0x01]

ADC_DITH is shown in 図 7-48 and described in 表 7-62.

Return to the Summary Table.

ADC Dither Control (default from Fuse ROM)

図 7-48. ADC_DITH Register

7	6	5	4	3	2	1	0
RESERVED					ADC_DITH_ERR	ADC_DITH_AMP	ADC_DITH_EN
R/W-0x0					R/W-0x0	R/W-0x0	R/W-0x1

表 7-62. ADC_DITH Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0x0	
2	ADC_DITH_ERR	R/W	0x0	Small rounding errors may occur when subtracting the dither signal. The error can be chosen to either slightly degrade SNR or to slightly increase the DC offset and FS/2 spur. In addition, the FS/4 spur will also be increased slightly while in single channel mode. 0 : Rounding error degrades SNR 1 : Rounding error degrades DC offset, FS/2 spur and FS/4 spur
1	ADC_DITH_AMP	R/W	0x0	0 : Small dither for better SNR (default) 1 : Large dither for better spurious performance

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表 7-62. ADC_DITH Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	ADC_DITH_EN	R/W	0x1	Set this bit to enable ADC dither. Dither can improve spurious performance at the expense of slightly degraded SNR. The dither amplitude (ADC_DITH_AMP) can be used to further tradeoff SNR and spurious performance.

7.6.33 LSB_CTRL Register (Address = 0x160) [reset = 0x00]

LSB_CTRL is shown in 図 7-49 and described in 表 7-63.

Return to the Summary Table.

LSB Control Bit Output (default: 0x00)

図 7-49. LSB_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							TIME_STAMP_EN
R/W-0x0							R/W-0x0

表 7-63. LSB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	
0	TIME_STAMP_EN	R/W	0x0	When set, the timestamp signal is transmitted on the LSB of the output samples. The latency of the timestamp signal (through the entire chip) matches the latency of the analog ADC inputs. Also set SYNC_RECV_EN when using TIME_STAMP_EN. Note 1: The control bit is placed on the LSB of the 8-bit samples (leaving 7-bits of sample data). Note 2: The control bit that is enabled by this register is never advertised in the ILA (CS is 0 in the ILA).

7.6.34 JESD_EN Register (Address = 0x200) [reset = 0x01]

JESD_EN is shown in 図 7-50 and described in 表 7-64.

Return to the Summary Table.

JESD204C Subsystem Enable (default: 0x01)

図 7-50. JESD_EN Register

7	6	5	4	3	2	1	0
RESERVED							JESD_EN
R/W-0x0							R/W-0x1

表 7-64. JESD_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	

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表 7-64. JESD_EN Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	JESD_EN	R/W	0x1	0 : Disable JESD204C interface 1 : Enable JESD204C interface Note: Before altering other JESD204C registers, you must clear JESD_EN. When JESD_EN is 0, the block is held in reset and the serializers are powered down. The clocks are gated off to save power. The LMFC/LEMC counter is also held in reset, so SYSREF will not align the LMFC/LEMC. Note 2: Always set CAL_EN before setting JESD_EN. Note 3: Always clear JESD_EN before clearing CAL_EN.

7.6.35 JMODE Register (Address = 0x201) [reset = 0x02]

JMODE is shown in 図 7-51 and described in 表 7-65.

Return to the Summary Table.

JESD204C Mode (default: 0x02)

図 7-51. JMODE Register

7	6	5	4	3	2	1	0
RW							

表 7-65. JMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	JMODE	RW	0x02	Specify the JESD204C Modes (including DDC decimation factor) Note 1: This register should only be changed when JESD_EN=0 and CAL_EN=0. Note 2: The MODE_LOCK register determines which modes are allowed.

7.6.36 KM1 Register (Address = 0x202) [reset = 0x1F]

KM1 is shown in 図 7-52 and described in 表 7-66.

Return to the Summary Table.

JESD204C K Parameter (default: 0x1F)

図 7-52. KM1 Register

7	6	5	4	3	2	1	0
KM1							
R/W-0x1F							

表 7-66. KM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	KM1	R/W	0x1F	K is the number of frames per multiframe and this register must be programmed as K-1. Depending on the JMODE setting, there are constraints on the legal values of K (see KR). The default values is KM1=31, which corresponds to K=32. Note: For modes using the 64b/66b link layer, the KM1 register is ignored and the value of K is determined from JMODE. The effective value of K is 256*E/F. Note: This register should only be changed when JESD_EN is 0.

7.6.37 JSYNC_N Register (Address = 0x203) [reset = 0x01]

JSYNC_N is shown in 図 7-53 and described in 表 7-67.

Return to the Summary Table.

JESD204C Manual Sync Request (default: 0x01)

図 7-53. JSYNC_N Register

7	6	5	4	3	2	1	0
RESERVED							JSYNC_N
R/W-0x0							R/W-0x1

表 7-67. JSYNC_N Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	
0	JSYNC_N	R/W	0x1	Set this bit to 0 to request JESD204C synchronization (equivalent to the SYNC~ signal being asserted). For normal operation, leave this bit set to 1. Note: The JSYNC_N register can always generate a synchronization request, regardless of the SYNC_SEL register. However, if the selected sync pin is stuck low, you cannot de-assert the synchronization request unless you program SYNC_SEL=2.

7.6.38 JCTRL Register (Address = 0x204) [reset = 0x03]

JCTRL is shown in 図 7-54 and described in 表 7-68.

Return to the Summary Table.

JESD204C Control (default: 0x03)

図 7-54. JCTRL Register

7	6	5	4	3	2	1	0
RESERVED			ALT_LANES	SYNC_SEL		SFORMAT	SCR
R/W-0x0			R/W-0x0	R/W-0x0		R/W-0x1	R/W-0x1

表 7-68. JCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	

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表 7-68. JCTRL Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	ALT_LANES	R/W	0x0	0 : Normal lane mapping (default). Link A uses lanes DA0 to DA3 and link B uses lanes DB0 to DB3. Other lanes are powered down. 1 : Alternate lane mapping (use upper lanes). Link A uses lanes DA4 to DA7 and link B uses lanes DB4 to DB7. Lanes DA0 to DA3 and DB0 to DB3 are powered down. Note: This option is only supported when JMODE selects a mode that uses 8 or less lanes. The behavior is undefined for modes that do not meet this requirement.
3:2	SYNC_SEL	R/W	0x0	0 : Use the SYNCSE input for SYNC~ function (default) 1 : Use the TMSTP input for SYNC~ function. TMSTP_RECV_EN must also be set. 2 : Do not use any sync input pin (use software SYNC~ through JSYNC_N)
1	SFORMAT	R/W	0x1	Output sample format for JESD204C samples 0 : Offset binary 1 : Signed 2’s complement (default)
0	SCR	R/W	0x1	0 : 8B/10B Scrambler disabled (applies only to 8B/10B modes) 1 : 8b/10b Scrambler enabled (default) Note 1: 64B/66B modes always use scrambling. This register does not apply to 64B/66B modes. Note 2: This register should only be changed when JESD_EN is 0.

7.6.39 JTEST Register (Address = 0x205) [reset = 0x00]

JTEST is shown in 図 7-55 and described in 表 7-69.

Return to the Summary Table.

JESD204C Test Control (default: 0x00)

図 7-55. JTEST Register

7	6	5	4	3	2	1	0
RESERVED			JTEST				
R/W-0x0			R/W-0x0				

表 7-69. JTEST Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	

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表 7-69. JTEST Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4:0	JTEST	R/W	0x0	0 : Test mode disabled. Normal operation (default) 1 : PRBS7 test mode 2 : PRBS15 test mode 3 : PRBS23 test mode 4 : Ramp test mode 5 : Transport Layer test mode 6 : D21.5 test mode 7 : K28.5 test mode* 8 : Repeated ILA test mode* 9 : Modified RPAT test mode* 10: Serial outputs held low 11: Serial outputs held high 12: RESERVED 13: PRBS9 test mode 14: PRBS31 test mode 15: Clock test pattern (0x00FF) 16: K28.7 test mode* 17-31: RESERVED * These test modes are only supported when JMODE is selecting a mode that uses 8b/10b encoding. Note: This register should only be changed when JESD_EN is 0.

7.6.40 DID Register (Address = 0x206) [reset = 0x00]

DID is shown in 図 7-56 and described in 表 7-70.

Return to the Summary Table.

JESD204C DID Parameter (default: 0x00)

図 7-56. DID Register

7	6	5	4	3	2	1	0
DID							
R/W-0x0							

表 7-70. DID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DID	R/W	0x0	Specifies the DID (Device ID) value that is transmitted during the second multiframe of the JESD204B ILA. Link A will transmit DID, and link B will transmit DID+1. Bit 0 is ignored and always returns 0 (if you program an odd number, it will be decremented to an even number). Note: This register should only be changed when JESD_EN is 0.

7.6.41 FCHAR Register (Address = 0x207) [reset = 0x00]

FCHAR is shown in 図 7-57 and described in 表 7-71.

Return to the Summary Table.

JESD204C Frame Character (default: 0x00)

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図 7-57. FCHAR Register

7	6	5	4	3	2	1	0
RESERVED						FCHAR	
R/W-0x0						R/W-0x0	

表 7-71. FCHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0x0	
1:0	FCHAR	R/W	0x0	Specify which comma character is used to denote end-of-frame. This character is transmitted opportunistically. This only applies to modes that use 8B/10B encoding. 0 : Use K28.7 (default) (JESD204C compliant) 1 : Use K28.1 (not JESD204C compliant) 2 : Use K28.5 (not JESD204C compliant) 3 : Reserved When using a JESD204C receiver, always use FCHAR=0. When using a general purpose 8B/10B receiver, the K28.7 character may cause issues. When K28.7 is combined with certain data characters, a false, misaligned comma character can result, and some receivers will re-align to the false comma. To avoid this, program FCHAR to 1 or 2. Note: This register should only be changed when JESD_EN is 0.

7.6.42 JESD_STATUS Register (Address = 0x208) [reset = 0x0]

JESD_STATUS is shown in 図 7-58 and described in 表 7-72.

Return to the Summary Table.

JESD204C / System Status Register

図 7-58. JESD_STATUS Register

7	6	5	4	3	2	1	0
RESERVED	LINK_UP	SYNC_STATUS	REALIGNED	ALIGNED	PLL_LOCKED	RESERVED	
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	

表 7-72. JESD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	
6	LINK_UP	R/W	0x0	When set, indicates that the JESD204C link is up.
5	SYNC_STATUS	R/W	0x0	Returns the state of the JESD204C SYNC~ signal. 0 : SYNC~ asserted 1 : SYNC~ de-asserted
4	REALIGNED	R/W	0x0	When high, indicates that the digital block clock, frame clock, or multiframe (LMFC) clock phase was realigned by SYSREF. Writing a 1 to this bit will clear it.
3	ALIGNED	R/W	0x0	When high, indicates that the multiframe (LMFC) clock phase has been established by SYSREF. The first SYSREF event after enabling the JESD204B encoder will set this bit. Writing a 1 to this bit will clear it.
2	PLL_LOCKED	R/W	0x0	When high, indicates that the serializer PLL is locked.

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表 7-72. JESD_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1:0	RESERVED	R/W	0x0	

7.6.43 PD_CH Register (Address = 0x209) [reset = 0x00]

PD_CH is shown in 図 7-59 and described in 表 7-73.

Return to the Summary Table.

JESD204C Channel Power Down (default: 0x00)

図 7-59. PD_CH Register

7	6	5	4	3	2	1	0
RESERVED						PD_BCH	PD_ACH
R/W-0x0						R/W-0x0	R/W-0x0

表 7-73. PD_CH Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0x0	
1	PD_BCH	R/W	0x0	When set, the “B” ADC channel is powered down. The digital channels that are bound to the “B” ADC channel are also powered down (see DIG_BIND). Important notes: 1. You must set JESD_EN=0 before changing PD_CH. 2. To power down both ADC channels, use the MODE register. 3. If both channels are powered down, then the entire JESD204C subsystem is powered down, including serializer PLL and LMFC. 4. If the selected JESD204C mode transmits A and B data on link A, and the B digital channel is disabled, link A remains operational, but the B-channel samples are undefined. For proper operation in foreground calibration mode, ADC_OFF in the CAL_CFG register should be programmed to 0x1.
0	PD_ACH	R/W	0x0	When set, the “A” ADC channel is powered down. The digital channels that are bound to the “A” ADC channel are also powered down (see DIG_BIND). Important notes: 1. You must set JESD_EN=0 before changing PD_CH. 2. To power down both ADC channels, use the MODE register. 3. If both channels are powered down, then the entire JESD204C subsystem is powered down, including serializer PLL and LMFC. 4. If the selected JESD204C mode transmits A and B data on link A, and the B digital channel is disabled, link A remains operational, but the B-channel samples are undefined. For proper operation in foreground calibration mode, ADC_OFF in the CAL_CFG register should be programmed to 0x1.

7.6.44 JEXTRA_A Register (Address = 0x20A) [reset = 0x00]

JEXTRA_A is shown in 図 7-60 and described in 表 7-74.

Return to the Summary Table.

JESD204C Extra Lane Enable (Link A) (default: 0x00)

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図 7-60. JEXTRA_A Register

7	6	5	4	3	2	1	0
EXTRA_LANE_A							EXTRA_SER_A
R/W-0x0							R/W-0x0

表 7-74. JEXTRA_A Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	EXTRA_LANE_A	R/W	0x0	Program these register bits to enable extra lanes (even if the selected JMODE does not require the lanes to be enabled). EXTRA_LANE_A(n) enables An (n=1 to 7). This register enables the link layer clocks for the affected lanes. To also enable the extra serializes set EXTRA_SER_A=1.
0	EXTRA_SER_A	R/W	0x0	0 : Only the link layer clocks for extra lanes are enabled. 1 : Serializers for extra lanes are enabled (as well as link layer clocks). Use this mode to transmit data from the extra lanes. Important Notes: 1. This register should only be changed when JESD_EN is 0. 2. The bit-rate and mode of the extra lanes are set by JMODE and JTEST (see exception below). 3. If a lane is enabled by this register (and was not enabled by JMODE), and JTEST is 0 or 5, the extra lanes will use an octet ramp (same as JTEST=4). 4. This register does not override the PD_CH register, so make sure the link is enabled to use this feature. 5. To enable serializer 'n', the lower number lanes 0 to n-1 must also be enabled, otherwise serializer 'n' will not receive a clock.

7.6.45 JEXTRA_B Register (Address = 0x20B) [reset = 0x00]

JEXTRA_B is shown in 図 7-61 and described in 表 7-75.

Return to the Summary Table.

JESD204C Extra Lane Enable (Link B) (default: 0x00)

図 7-61. JEXTRA_B Register

7	6	5	4	3	2	1	0
EXTRA_LANE_B							EXTRA_SER_B
R/W-0x0							R/W-0x0

表 7-75. JEXTRA_B Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	EXTRA_LANE_B	R/W	0x0	Program these register bits to enable extra lanes (even if the selected JMODE does not require the lanes to be enabled). EXTRA_LANE_B(n) enables Bn (n=1 to 7). This register enables the link layer clocks for the affected lanes. To also enable the extra serializes set EXTRA_SER_B=1.

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表 7-75. JEXTRA_B Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0	EXTRA_SER_B	R/W	0x0	0 : Only the link layer clocks for extra lanes are enabled. 1 : Serializers for extra lanes are enabled (as well as link layer clocks). Use this mode to transmit data from the extra lanes. Important Notes: 1. This register should only be changed when JESD_EN is 0. 2. The bit-rate and mode of the extra lanes are set by JMODE and JTEST (see exception below). 3. If a lane is enabled by this register (and was not enabled by JMODE), and JTEST is 0 or 5, the extra lanes will use an octet ramp (same as JTEST=4). 4. This register does not override the PD_CH register, so make sure that the link is enabled to use this feature. 5. To enable serializer 'n', the lower number lanes 0 to n-1 must also be enabled, otherwise serializer 'n' will not receive a clock.

7.6.46 SHMODE Register (Address = 0x20F) [reset = 0x00]

SHMODE is shown in 図 7-62 and described in 表 7-76.

Return to the Summary Table.

JESD204C Sync Word Mode (default: 0x00)

図 7-62. SHMODE Register

7	6	5	4	3	2	1	0
RESERVED						SHMODE	
R/W-0x0						R/W-0x0	

表 7-76. SHMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0x0	
1:0	SHMODE	R/W	0x0	Select the mode for the 64b/66b sync word (32 bits of data per multi-block). This only applies when JMODE is selecting a 64b/66b mode. 0 : Transmit CRC-12 signal (default setting) 1 : RESERVED 2 : Transmit FEC signal 3 : RESERVED Note: This device does not support any JESD204C command features. All command fields will be set to zero (idle headers). Note: This register should only be changed when JESD_EN is 0.

7.6.47 OVR_T0 Register (Address = 0x211) [reset = 0xF2]

OVR_T0 is shown in 図 7-63 and described in 表 7-77.

Return to the Summary Table.

Over-range Threshold 0 (default: 0xF2)

図 7-63. OVR_T0 Register

7	6	5	4	3	2	1	0
OVR_T0							

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図 7-63. OVR_T0 Register (continued)

R/W-0xF2

表 7-77. OVR_T0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OVR_T0	R/W	0xF2	This parameter defines the absolute sample level that causes control bit 0 to be set. The detection level in dBFS (peak) is 20log10(OVR_T0/256) (Default: 0xF2 = 242-> -0.5dBFS)

7.6.48 OVR_T1 Register (Address = 0x212) [reset = 0xAB]

OVR_T1 is shown in 図 7-64 and described in 表 7-78.

Return to the Summary Table.

Over-range Threshold 1 (default: 0xAB)

図 7-64. OVR_T1 Register

7	6	5	4	3	2	1	0
OVR_T1							
R/W-0xAB							

表 7-78. OVR_T1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OVR_T1	R/W	0xAB	This parameter defines the absolute sample level that causes control bit 1 to be set. The detection level in dBFS (peak) is 20log10(OVR_T1/256) (Default: 0xAB = 171 -> -3.5dBFS)

7.6.49 OVR_CFG Register (Address = 0x213) [reset = 0x07]

OVR_CFG is shown in 図 7-65 and described in 表 7-79.

Return to the Summary Table.

Over-range Enable / Hold Off (default: 0x07)

図 7-65. OVR_CFG Register

7	6	5	4	3	2	1	0
RESERVED				OVR_EN	OVR_N		
R/W-0x0				R/W-0x0	R/W-0x7		

表 7-79. OVR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	
3	OVR_EN	R/W	0x0	Enables over-range status output pins when set high. The ORA0, ORA1, ORB0 and ORB1 outputs are held low when OVR_EN is set low. This register only affects the over-range output pins (ORxx). JESD204C modes that transmit over-range bits are not affected by this register.

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表 7-79. OVR_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2:0	OVR_N	R/W	0x7	Program this register to adjust the pulse extension for the ORA0/1 and ORB0/1 outputs. The minimum pulse duration of the over-range outputs is 8 * 2^{OVR_N} DEVCLK cycles. Incrementing this field doubles the monitoring period.

7.6.50 INIT_STATUS Register (Address = 0x270) [reset = undefined]

INIT_STATUS is shown in 図 7-66 and described in 表 7-80.

Return to the Summary Table.

Chip Spin Identifier (default: See description, read-only)

図 7-66. INIT_STATUS Register

7	6	5	4	3	2	1	0
RESERVED							INIT_STATUS
R-undefined							R-undefined

表 7-80. INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	undefined	RESERVED
0	INIT_DONE	R	undefined	Returns 1 when the initialization logic has finished initializing the device. This indicates that it is now safe to proceed with startup. No SPI transactions should be performed before INIT_DONE returns 1(except SOFT_RESET).

7.6.51 SPIN_ID Register (Address = 0x297) [reset = 0x0A]

SPIN_ID is shown in 図 7-67 and described in 表 7-81.

Return to the Summary Table.

Chip Spin Identifier (default: See description, read-only)

図 7-67. SPIN_ID Register

7	6	5	4	3	2	1	0
RESERVED			SPIN_ID				
R/W-0x0			R/W-0x0A				

表 7-81. SPIN_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	
4:0	SPIN_ID	R/W	0xA	Spin identification value: 0: ADC12DJ5200RF 2 : ADC12DJ4000RF 10: ADC08DJ5200RF

7.6.52 TESTBUS Register (Address = 0x2A2) [reset = 0x0]

TESTBUS is shown in 図 7-68 and described in 表 7-82.

Return to the Summary Table.

TESTBUS Register (default: 0x0)

図 7-68. TESTBUS Register

7	6	5	4	3	2	1	0
RESERVED		EN_VD11_NOISE_SUPPR	EN_VS11_NOISE_SUPPR	RESERVED			
R/W-0x0		R/W-0x0	R/W-0x0	R/W-0x0			

表 7-82. TESTBUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	RESERVED
5	EN_VD11_NOISE_SUPPR	R/W	0x0	When set, noise on VD11 is suppressed. It is recommended to have this set, as it reduces noise coupling from the digital circuits to analog clock, at the expense of a small increase in power.
4	EN_VS11_NOISE_SUPPR	R/W		When set, noise on VS11 is suppressed. It is recommended to have this set, as it reduces noise coupling from the digital circuits to analog clock, at the expense of a small increase in power.
3:0	RESERVED	R/W	R/W	RESERVED

7.6.53 SRC_EN Register (Address = 0x2B0) [reset = 0x00]

SRC_EN is shown in 図 7-69 and described in 表 7-83.

Return to the Summary Table.

SYSREF Calibration Enable (default: 0x00)

図 7-69. SRC_EN Register

7	6	5	4	3	2	1	0
RESERVED							SRC_EN
R/W-0x0							R/W-0x0

表 7-83. SRC_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	
0	SRC_EN	R/W	0x0	0: SYSREF Calibration Disabled. Use the TAD register to manually control the tad[16:0] output and adjust the DEVCLK delay. (default) 1: SYSREF Calibration Enabled. The DEVCLK delay is automatically calibrated. The TAD register is ignored. A 0-to-1 transition on SRC_EN starts the SYSREF calibration sequence. Program SRC_CFG before setting SRC_EN. Make sure that ADC calibration is not currently running before setting SRC_EN.

7.6.54 SRC_CFG Register (Address = 0x2B1) [reset = 0x05]

SRC_CFG is shown in 図 7-70 and described in 表 7-84.

Return to the Summary Table.

SYSREF Calibration Configuration (default: 0x05)

図 7-70. SRC_CFG Register

7	6	5	4	3	2	1	0
RESERVED				SRC_AVG		SRC_HDUR	

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図 7-70. SRC_CFG Register (continued)

R/W-0x0	R/W-0x1	R/W-0x1

表 7-84. SRC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	
3:2	SRC_AVG	R/W	0x1	Specifies the amount of averaging used for SYSREF Calibration. Larger values will increase calibration time and reduce the variance of the calibrated value. 0: 4 averages 1: 16 averages 2: 64 averages 3: 256 averages
1:0	SRC_HDUR	R/W	0x1	Specifies the duration of each high-speed accumulation for SYSREF Calibration. If the SYSREF period exceeds the supported value, calibration will fail. Larger values will increase calibration time and support longer SYSREF periods. For a given SYSREF period, larger values will also reduce the variance of the calibrated value. 0: 4 cycles per accumulation, max SYSREF period of 128 DEVCLK cycles 1: 16 cycles per accumulation, max SYSREF period of 1664 DEVCLK cycles 2: 64 cycles per accumulation, max SYSREF period of 7808 DEVCLK cycles 3: 256 cycles per accumulation, max SYSREF period of 32384 DEVCLK cycles Max duration of SYSREF calibration is bounded by: TSYSREFCAL (in DEVCLK cycles) = 384 * 19 * 4^(SRC_AVG + SRC_HDUR + 2)

7.6.55 SRC_STATUS Register (Address = 0x2B2) [reset = 0x0]

SRC_STATUS is shown in 図 7-71 and described in 表 7-85.

Return to the Summary Table.

SYSREF Calibration Status (read-only, default: undefined)

図 7-71. SRC_STATUS Register

23	22	21	20	19	18	17	16
RESERVED						SRC_DONE	SRC_TAD
R/W-0x0						R/W-0x0	R/W-0x0
15	14	13	12	11	10	9	8
SRC_TAD							
R/W-0x0							
7	6	5	4	3	2	1	0
SRC_TAD							
R/W-0x0							

表 7-85. SRC_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
23:18	RESERVED	R/W	0x0	

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表 7-85. SRC_STATUS Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	SRC_DONE	R/W	0x0	This bit returns ‘1’ when SRC_EN=1 and SYSREF Calibration has been completed.
16:0	SRC_TAD	R/W	0x0	This field returns the value for TAD[16:0] computed by SYSREF Calibration. It is only valid if SRC_DONE=1. SRC_TAD[16] indicates if DEVCLK has been inverted. SRC_TAD[15:8] indicates the coarse delay adjustment. SRC_TAD[7:0] indicates the fine delay adjustment.

7.6.56 TAD Register (Address = 0x2B5) [reset = 0x00]

TAD is shown in 図 7-72 and described in 表 7-86.

Return to the Summary Table.

DEVCLK Timing Adjust (default: 0x00)

図 7-72. TAD Register

23	22	21	20	19	18	17	16
RESERVED							TAD_INV
R/W-0x0							R/W-0x0
15	14	13	12	11	10	9	8
TAD_COARSE							
R/W-0x0							
7	6	5	4	3	2	1	0
TAD_FINE							
R-0x0							

表 7-86. TAD Register Field Descriptions

Bit	Field	Type	Reset	Description
23:17	RESERVED	R/W	0x0	
16	TAD_INV	R/W	0x0	Inverts the sampling clock when set.
15:8	TAD_COARSE	R/W	0x0	This register controls the coarse resolution of the sampling aperture delay adjustment when SRC_EN=0. Use this register to manually control the DEVCLK aperture delay when SYSREF Calibration is disabled. If ADC calibration or JESD204B is running, it is recommended that you gradually increase or decrease this value (1 code at a time) to avoid clock glitches. Refer to Switching Characteristics for TAD_COARSE resolution. If ADC calibration is enabled (CAL_EN=1), or the JESD204C link is enabled (JESD_EN=1), the following rules must be obeyed to avoid clock glitches and unpredictable behavior: 1. Do not change TAD_INV. You must program CAL_EN=0 and JESD_EN=0 before changing TAD_INV. 2. TAD_COARSE must be increased or decreased gradually (no more than 4 codes at a time). This rule can be obeyed manually via SPI writes, or by setting TAD_RAMP_EN.

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表 7-86. TAD Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7:0	TAD_FINE	R/W	0x0	This register controls the fine resolution of the sampling aperture delay adjustment when SRC_EN=0. Use this register to manually control the DEVCLK aperture delay when SYSREF Calibration is disabled. Refer to Switching Characteristics for TAD_FINE resolution. TAD_FINE may be changed to any value at any time (its adjustment is too fine to cause clock glitches).

7.6.57 TAD_RAMP Register (Address = 0x2B8) [reset = 0x00]

TAD_RAMP is shown in 図 7-73 and described in 表 7-87.

Return to the Summary Table.

DEVCLK Timing Adjust Ramp Control (default: 0x00)

図 7-73. TAD_RAMP Register

7	6	5	4	3	2	1	0
RESERVED						TAD_RAMP_RATE	TAD_RAMP_EN
R/W-0x0						R/W-0x0	R/W-0x0

表 7-87. TAD_RAMP Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0x0	
1	TAD_RAMP_RATE	R/W	0x0	Specifies the ramp rate for TAD_COARSE when the TAD_COARSE register is written while TAD_RAMP_EN=1. 0: TAD_COARSE ramps up or down one code per 384 sampling clock cycles. 1: TAD_COARSE ramps up or down 4 codes per 384 sampling clock cycles.
0	TAD_RAMP_EN	R/W	0x0	TAD ramp enable. Set this bit if you want the coarse TAD adjustment (TAD_COARSE) to ramp up or down instead of changing abruptly. 0 : After writing the TAD_COARSE register, the applied TAD_COARSE setting is updated within 1536 CLK cycles (ramp feature disabled). 1 : After writing the TAD_COARSE register, the applied TAD_COARSE setting ramps up or down gradually until it matches the TAD_COARSE register.

7.6.58 ALARM Register (Address = 0x2C0) [reset = 0x0]

ALARM is shown in 図 7-74 and described in 表 7-88.

Return to the Summary Table.

Alarm Interrupt (read-only)

図 7-74. ALARM Register

7	6	5	4	3	2	1	0
RESERVED							ALARM
R-0x0							R-0x0

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表 7-88. ALARM Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	
0	ALARM	R	0x0	This bit returns a ‘1’ whenever any alarm occurs that is unmasked in the ALM_STATUS register. Use ALM_MASK to mask (disable) individual alarms. CAL_STATUS_SEL can be used to drive the ALARM bit onto the CALSTAT output pin to provide a hardware alarm interrupt signal.

7.6.59 ALM_STATUS Register (Address = 0x2C1) [reset = 0x3F]

ALM_STATUS is shown in 図 7-75 and described in 表 7-89.

Return to the Summary Table.

Alarm Status (default: 0x3F, write to clear)

図 7-75. ALM_STATUS Register

7	6	5	4	3	2	1	0
RESERVED		FIFO_ALM	PLL_ALM	LINK_ALM	REALIGNED_ALM	NCO_ALM	CLK_ALM
R/W-0x0		R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1

表 7-89. ALM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	
5	FIFO_ALM	R/W	0x1	FIFO overflow/underflow alarm: This bit is set whenever an active JESD204C lane FIFO experiences an underflow or overflow condition. Write a ‘1’ to clear this bit. To inspect which lane generated the alarm, read FIFO_LANE_ALM.
4	PLL_ALM	R/W	0x1	PLL Lock Lost Alarm: This bit is set whenever the PLL is not locked. Write a ‘1’ to clear this bit.
3	LINK_ALM	R/W	0x1	Link Alarm: This bit is set whenever the JESD204C link is enabled, but is not in the data encoder state (for 8B/10B modes). In 64B/66B modes, there is no data encoder state, so this alarm will be set when the link first starts up, and will also be set if any event causes a FIFO/serializer realignment. Write a ‘1’ to clear this bit.
2	REALIGNED_ALM	R/W	0x1	Realigned Alarm: This bit is set whenever SYSREF causes the internal clocks (including the LMFC/LEMC) to be realigned. Write a ‘1’ to clear this bit.
1	NCO_ALM	R/W	0x1	Not used for ADC08DJ5200RF.
0	CLK_ALM	R/W	0x1	Clock Alarm: This bit can be used to detect an upset to the internal JESD204C clocks. This bit is set whenever the internal clock dividers for the A and B channels do not match. Write a ‘1’ to clear this bit. Refer to the alarm section for the proper usage of this register. Note: After power-on reset or soft-reset, all alarm bits are set to ‘1.’ Note: When JESD_EN=0, all alarms (except CLK_ALM) are undefined. It is recommended that the user clears the alarms after setting JESD_EN=1.

7.6.60 ALM_MASK Register (Address = 0x2C2) [reset = 0x3F]

ALM_MASK is shown in 図 7-76 and described in 表 7-90.

Return to the Summary Table.

Alarm Mask Register (default: 0x3F)

図 7-76. ALM_MASK Register

7	6	5	4	3	2	1	0
RESERVED		MASK_FIFO_ALM	MASK_PLL_ALM	MASK_LINK_ALM	MASK_REALIGNED_ALM	MASK_NCO_ALM	MASK_CLK_ALM
R/W-0x0		R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1

表 7-90. ALM_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	
5	MASK_FIFO_ALM	R/W	0x1	When set, FIFO_ALM is masked and will not impact the ALARM register bit.
4	MASK_PLL_ALM	R/W	0x1	When set, PLL_ALM is masked and will not impact the ALARM register bit.
3	MASK_LINK_ALM	R/W	0x1	When set, LINK_ALM is masked and will not impact the ALARM register bit.
2	MASK_REALIGNED_ALM	R/W	0x1	When set, REALIGNED_ALM is masked and will not impact the ALARM register bit.
1	MASK_NCO_ALM	R/W	0x1	Not used for ADC08DJ5200RF.
0	MASK_CLK_ALM	R/W	0x1	When set, CLK_ALM is masked and will not impact the ALARM register bit.

7.6.61 FIFO_LANE_ALM Register (Address = 0x2C4) [reset = 0xFFFF]

FIFO_LANE_ALM is shown in 図 7-77 and described in 表 7-91.

Return to the Summary Table.

FIFO Overflow/Underflow Alarm (default: 0xFFFF)

図 7-77. FIFO_LANE_ALM Register

15	14	13	12	11	10	9	8
FIFO_LANE_ALM							
R/W-0xFFFF							
7	6	5	4	3	2	1	0
FIFO_LANE_ALM							
R/W-0xFFFF							

表 7-91. FIFO_LANE_ALM Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FIFO_LANE_ALM	R/W	0xFFFF	FIFO_LANE_ALM[i] is set if the FIFO for lane i experiences overflow or underflow. Use this register to determine which lane(s) generated an alarm. Writing a ‘1’ to any bit in this register will clear the alarm (the alarm may immediately trip again if the overflow/underflow condition persists). Writing a ‘1’ to the FIFO_ALM bit in the ALM_STATUS register will clear all bits of this register.

7.6.62 TADJ_A Register (Address = 0x310) [reset = 0x0]

TADJ_A is shown in 図 7-78 and described in 表 7-92.

Return to the Summary Table.

Timing Adjust for A-ADC operating in Dual Channel Mode (default from Fuse ROM)

図 7-78. TADJ_A Register

7	6	5	4	3	2	1	0
TADJ_A							
R/W-0x0							

表 7-92. TADJ_A Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TADJ_A	R/W	0x0	This register (and other TADJ* registers that follow it) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes. The default values for all TADJ* registers are factory programmed values. The factory trimmed values can be read out and adjusted as required.

7.6.63 TADJ_B Register (Address = 0x313) [reset = 0x0]

TADJ_B is shown in 図 7-79 and described in 表 7-93.

Return to the Summary Table.

Timing Adjust for B-ADC operating in Dual Channel Mode (default from Fuse ROM)

図 7-79. TADJ_B Register

7	6	5	4	3	2	1	0
TADJ_B							
R/W-0x0							

表 7-93. TADJ_B Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TADJ_B	R/W	0x0	See TADJ_A register for description. Adjusts timing of B-ADC in dual channel mode with foreground calibration enabled.

7.6.64 TADJ_A_FG90_VINA Register (Address = 0x314) [reset = 0x0]

TADJ_A_FG90_VINA is shown in 図 7-80 and described in 表 7-94.

Return to the Summary Table.

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Timing Adjust for A-ADC operating in Single Channel Mode and sampling INA± (default from Fuse ROM)

図 7-80. TADJ_A_FG90_VINA Register

7	6	5	4	3	2	1	0
TADJ_A_FG90_VINA							
R/W-0x0							

表 7-94. TADJ_A_FG90_VINA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TADJ_A_FG90_VINA	R/W	0x0	See TADJ_A register for description. Adjusts timing of A-ADC in single channel mode with foreground calibration enabled and sampling INA±.

7.6.65 TADJ_B_FG0_VINA Register (Address = 0x315) [reset = 0x0]

TADJ_B_FG0_VINA is shown in 図 7-81 and described in 表 7-95.

Return to the Summary Table.

Timing Adjust for B-ADC operating in Single Channel Mode and sampling INA± (default from Fuse ROM)

図 7-81. TADJ_B_FG0_VINA Register

7	6	5	4	3	2	1	0
TADJ_B_FG0_VINA							
R/W-0x0							

表 7-95. TADJ_B_FG0_VINA Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TADJ_B_FG0_VINA	R/W	0x0	See TADJ_A register for description. Adjusts timing of B-ADC in single channel mode with foreground calibration enabled and sampling INA±.

7.6.66 TADJ_A_FG90_VINB Register (Address = 0x31A) [reset = 0x0]

TADJ_A_FG90_VINB is shown in 図 7-82 and described in 表 7-96.

Return to the Summary Table.

Timing Adjust for A-ADC operating in Single Channel Mode and sampling INB± (default from Fuse ROM)

図 7-82. TADJ_A_FG90_VINB Register

7	6	5	4	3	2	1	0
TADJ_A_FG90_VINB							
R/W-0x0							

表 7-96. TADJ_A_FG90_VINB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TADJ_A_FG90_VINB	R/W	0x0	See TADJ_A register for description. Adjusts timing of A-ADC in single channel mode with foreground calibration enabled and sampling INB±.

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7.6.67 TADJ_B_FG0_VINB Register (Address = 0x31B) [reset = 0x0]

TADJ_B_FG0_VINB is shown in 図 7-83 and described in 表 7-97.

Return to the Summary Table.

Timing Adjust for B-ADC operating in Single Channel Mode and sampling INB± (default from Fuse ROM)

図 7-83. TADJ_B_FG0_VINB Register

7	6	5	4	3	2	1	0
TADJ_B_FG0_VINB							
R/W-0x0							

表 7-97. TADJ_B_FG0_VINB Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	TADJ_B_FG0_VINB	R/W	0x0	See TADJ_A register for description. Adjusts timing of B-ADC in single channel mode with foreground calibration enabled and sampling INB±.

7.6.68 OADJ_A_FG0_VINA Register (Address = 0x344) [reset = 0x0]

OADJ_A_FG0_VINA is shown in 図 7-84 and described in 表 7-98.

Return to the Summary Table.

Offset Adjustment for A-ADC operating in Dual Channel Mode sampling INA± (default from Fuse ROM)

図 7-84. OADJ_A_FG0_VINA Register

15	14	13	12	11	10	9	8
RESERVED				OADJ_A_FG0_VINA			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OADJ_A_FG0_VINA							
R/W-0x0							

表 7-98. OADJ_A_FG0_VINA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	OADJ_A_FG0_VINA	R/W	0x0	Offset adjustment value applied to A-ADC when it samples INA± in dual channel mode and foreground calibration is enabled.

7.6.69 OADJ_A_FG0_VINB Register (Address = 0x346) [reset = 0x0]

OADJ_A_FG0_VINB is shown in 図 7-85 and described in 表 7-99.

Return to the Summary Table.

Offset Adjustment for A-ADC operating in Dual Channel Mode sampling INB± (default from Fuse ROM)

図 7-85. OADJ_A_FG0_VINB Register

15	14	13	12	11	10	9	8
RESERVED				OADJ_A_FG_VINB			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

図 7-85. OADJ_A_FG0_VINB Register (continued)

OADJ_A_FG_VINB
R/W-0x0

表 7-99. OADJ_A_FG0_VINB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	OADJ_A_FG_VINB	R/W	0x0	Offset adjustment value applied to A-ADC when it samples INB± in dual channel mode and foreground calibration is enabled.

7.6.70 OADJ_A_FG90_VINA Register (Address = 0x348) [reset = 0x0]

OADJ_A_FG90_VINA is shown in 図 7-86 and described in 表 7-100.

Return to the Summary Table.

Offset Adjustment for A-ADC operating in Single Channel Mode sampling INA± (default from Fuse ROM)

図 7-86. OADJ_A_FG90_VINA Register

15	14	13	12	11	10	9	8
RESERVED				OADJ_A_FG90_VINA			
R/W-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
OADJ_A_FG90_VINA							
R/W-0x0							

表 7-100. OADJ_A_FG90_VINA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	OADJ_A_FG90_VINA	R/W	0x0	Offset adjustment value applied to A-ADC when it samples INA± in single channel mode and foreground calibration is enabled.

7.6.71 OADJ_A_FG90_VINB Register (Address = 0x34A) [reset = 0x0]

OADJ_A_FG90_VINB is shown in 図 7-87 and described in 表 7-101.

Return to the Summary Table.

Offset Adjustment for A-ADC operating in Single Channel Mode sampling INB± (default from Fuse ROM)

図 7-87. OADJ_A_FG90_VINB Register

15	14	13	12	11	10	9	8
RESERVED				OADJ_A_FG90_VINB			
R/W-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
OADJ_A_FG90_VINB							
R/W-0x0							

表 7-101. OADJ_A_FG90_VINB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	

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表 7-101. OADJ_A_FG90_VINB Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	OADJ_A_FG90_VINB	R/W	0x0	Offset adjustment value applied to A-ADC when it samples INB± using 90° clock phase and foreground calibration is enabled.

7.6.72 OADJ_B_FG0_VINA Register (Address = 0x34C) [reset = 0x0]

OADJ_B_FG0_VINA is shown in 図 7-88 and described in 表 7-102.

Return to the Summary Table.

Offset Adjustment for B-ADC sampling INA± (default from Fuse ROM)

図 7-88. OADJ_B_FG0_VINA Register

15	14	13	12	11	10	9	8
RESERVED				OADJ_B_FG0_VINA			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OADJ_B_FG0_VINA							
R/W-0x0							

表 7-102. OADJ_B_FG0_VINA Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	OADJ_B_FG0_VINA	R/W	0x0	Offset adjustment value applied to B-ADC when it samples INA± and foreground calibration is enabled. Applies to both dual channel mode and single channel mode.

7.6.73 OADJ_B_FG0_VINB Register (Address = 0x34E) [reset = 0x0]

OADJ_B_FG0_VINB is shown in 図 7-89 and described in 表 7-103.

Return to the Summary Table.

Offset Adjustment for B-ADC sampling INB± (default from Fuse ROM)

図 7-89. OADJ_B_FG0_VINB Register

15	14	13	12	11	10	9	8
RESERVED				OADJ_B_FG0_VINB			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OADJ_B_FG0_VINB							
R/W-0x0							

表 7-103. OADJ_B_FG0_VINB Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	OADJ_B_FG0_VINB	R/W	0x0	Offset adjustment value applied to B-ADC when it samples INB± and foreground calibration is enabled. Applies to both dual channel mode and single channel mode.

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7.6.74 GAIN_A0_FGDUAL Register (Address = 0x350) [reset = 0x0]

GAIN_A0_FGDUAL is shown in 図 7-90 and described in 表 7-104.

Return to the Summary Table.

Fine Gain Adjust for ADC A Bank 0 in Dual Channel Mode (default from Fuse ROM)

図 7-90. GAIN_A0_FGDUAL Register

7	6	5	4	3	2	1	0
RESERVED			GAIN_A0_FGDUAL				
R/W-0x0			R/W-0x0				

表 7-104. GAIN_A0_FGDUAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	
4:0	GAIN_A0_FGDUAL	R/W	0x0	Fine gain adjustment for ADC A bank 0.

7.6.75 GAIN_A1_FGDUAL Register (Address = 0x351) [reset = 0x0]

GAIN_A1_FGDUAL is shown in 図 7-91 and described in 表 7-105.

Return to the Summary Table.

Fine Gain Adjust for ADC A Bank 1 in Dual Channel Mode (default from Fuse ROM)

図 7-91. GAIN_A1_FGDUAL Register

7	6	5	4	3	2	1	0
RESERVED			GAIN_A1_FGDUAL				
R/W-0x0			R/W-0x0				

表 7-105. GAIN_A1_FGDUAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	
4:0	GAIN_A1_FGDUAL	R/W	0x0	Fine gain adjustment for ADC A bank 1.

7.6.76 GAIN_B0_FGDUAL Register (Address = 0x352) [reset = 0x0]

GAIN_B0_FGDUAL is shown in 図 7-92 and described in 表 7-106.

Return to the Summary Table.

Fine Gain Adjust for ADC B Bank 0 in Dual Channel Mode (default from Fuse ROM)

図 7-92. GAIN_B0_FGDUAL Register

7	6	5	4	3	2	1	0
RESERVED			GAIN_A0_FGDUAL				
R/W-0x0			R/W-0x0				

表 7-106. GAIN_B0_FGDUAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	
4:0	GAIN_A0_FGDUAL	R/W	0x0	Fine gain adjustment for ADC B bank 0.

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7.6.77 GAIN_B1_FGDUAL Register (Address = 0x353) [reset = 0x0]

GAIN_B1_FGDUAL is shown in 図 7-93 and described in 表 7-107.

Return to the Summary Table.

Fine Gain Adjust for ADC B Bank 1 in Dual Channel Mode (default from Fuse ROM)

図 7-93. GAIN_B1_FGDUAL Register

7	6	5	4	3	2	1	0
RESERVED			GAIN_B1_FGDUAL				
R/W-0x0			R/W-0x0				

表 7-107. GAIN_B1_FGDUAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	
4:0	GAIN_B1_FGDUAL	R/W	0x0	Fine gain adjustment for ADC B bank 1.

7.6.78 GAIN_A0_FGDES Register (Address = 0x354) [reset = 0x0]

GAIN_A0_FGDES is shown in 図 7-94 and described in 表 7-108.

Return to the Summary Table.

Fine Gain Adjust for ADC A Bank 0 in Single Channel Mode (default from Fuse ROM)

図 7-94. GAIN_A0_FGDES Register

7	6	5	4	3	2	1	0
RESERVED			GAIN_A0_FGDUAL				
R/W-0x0			R/W-0x0				

表 7-108. GAIN_A0_FGDES Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	
4:0	GAIN_A0_FGDUAL	R/W	0x0	Fine gain adjustment for ADC A bank 0.

7.6.79 GAIN_A1_FGDES Register (Address = 0x355) [reset = 0x0]

GAIN_A1_FGDES is shown in 図 7-95 and described in 表 7-109.

Return to the Summary Table.

Fine Gain Adjust for ADC A Bank 1 in Single Channel Mode (default from Fuse ROM)

図 7-95. GAIN_A1_FGDES Register

7	6	5	4	3	2	1	0
RESERVED			GAIN_A1_FGDUAL				
R/W-0x0			R/W-0x0				

表 7-109. GAIN_A1_FGDES Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	
4:0	GAIN_A1_FGDUAL	R/W	0x0	Fine gain adjustment for ADC A bank 1.

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7.6.80 GAIN_B0_FGDES Register (Address = 0x356) [reset = 0x0]

GAIN_B0_FGDES is shown in 図 7-96 and described in 表 7-110.

Return to the Summary Table.

Fine Gain Adjust for ADC B Bank 0 in Single Channel Mode (default from Fuse ROM)

図 7-96. GAIN_B0_FGDES Register

7	6	5	4	3	2	1	0
RESERVED			GAIN_A0_FGDUAL				
R/W-0x0			R/W-0x0				

表 7-110. GAIN_B0_FGDES Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	
4:0	GAIN_A0_FGDUAL	R/W	0x0	Fine gain adjustment for ADC B bank 0.

7.6.81 GAIN_B1_FGDES Register (Address = 0x357) [reset = 0x0]

GAIN_B1_FGDES is shown in 図 7-97 and described in 表 7-111.

Return to the Summary Table.

Fine Gain Adjust for ADC B Bank 1 in Single Channel Mode (default from Fuse ROM)

図 7-97. GAIN_B1_FGDES Register

7	6	5	4	3	2	1	0
RESERVED			GAIN_B1_FGDUAL				
R/W-0x0			R/W-0x0				

表 7-111. GAIN_B1_FGDES Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	
4:0	GAIN_B1_FGDUAL	R/W	0x0	Fine gain adjustment for ADC B bank 1.

7.6.82 PFIR_CFG Register (Address = 0x400) [reset = 0x00]

PFIR_CFG is shown in 図 7-98 and described in 表 7-112.

Return to the Summary Table.

Programmable FIR Mode (default: 0x00)

図 7-98. PFIR_CFG Register

7	6	5	4	3	2	1	0
RESERVED	PFIR_SHARE	PFIR_MERGE	PFIR_SCW			PFIR_MODE	
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0			R/W-0x0	

表 7-112. PFIR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	

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表 7-112. PFIR_CFG Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
6	PFIR_SHARE	R/W	0x0	When set, the PFIR on the B channel uses the same coefficients as the PFIR on the A channel. When PFIR_SHARE=0, the B channel filter uses its own set of coefficients (unique from channel A). See Programmable FIR Filter (PFIR) section for usage details.
5	PFIR_MERGE	R/W	0x0	When set, the PFIR filters are merged into a single logical filter. This mode processes ADC data samples as if they belong to a single sample stream. Set PFIR_MERGE=1 whenever the ADC is setup in Single Channel Mode.
4:2	PFIR_SCW	R/W	0x0	Side coefficient weight for PFIR. This field determines the weight of the coefficients (except for the center coefficient). Increasing the coefficient weight increases the range of the coefficients at the expense of reduced precision. The LSB weight is 2^{PFIR_SCW-16}, where PFIR_SCW weight can be programmed from 0 to 6. The default is 0 which provides an LSB weight of 2^{-16}.
1:0	PFIR_MODE	R/W	0x0	0 : PFIR block is disabled (default) 1 : RESERVED 2 : Enable PFIR block 3 : RESERVED Note: When using the PFIR, you must also program the filter coefficients. Note: All PFIR_* register should only be changed when JESD_EN=0.

7.6.83 PFIR_A0 Register (Address = 0x418) [reset = 0x0]

PFIR_A0 is shown in 図 7-99 and described in 表 7-113.

Return to the Summary Table.

PFIR Coefficient A0

図 7-99. PFIR_A0 Register

15	14	13	12	11	10	9	8
RESERVED				PFIR_A0			
R/W-0x0				R/W-0x0			

7	6	5	4	3	2	1	0
PFIR_A0							
R/W-0x0							

表 7-113. PFIR_A0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	PFIR_A0	R/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the first tap for the ADC A programmable FIR filter in Dual Channel Mode or the first tap for the programmable FIR filter in Single Channel Mode.

7.6.84 PFIR_A1 Register (Address = 0x41A) [reset = 0x0]

PFIR_A1 is shown in 図 7-100 and described in 表 7-114.

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PFIR Coefficient A1

図 7-100. PFIR_A1 Register

15	14	13	12	11	10	9	8
RESERVED				PFIR_A1			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PFIR_A1							
R/W-0x0							

表 7-114. PFIR_A1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	PFIR_A1	R/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the second tap for the ADC A programmable FIR filter in Dual Channel Mode or the second tap for the programmable FIR filter in Single Channel Mode.

7.6.85 PFIR_A2 Register (Address = 0x41C) [reset = 0x0]

PFIR_A2 is shown in 図 7-101 and described in 表 7-115.

Return to the Summary Table.

PFIR Coefficient A2

図 7-101. PFIR_A2 Register

15	14	13	12	11	10	9	8
RESERVED				PFIR_A2			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PFIR_A2							
R/W-0x0							

表 7-115. PFIR_A2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	PFIR_A2	R/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the third tap for the ADC A programmable FIR filter in Dual Channel Mode or the third tap for the programmable FIR filter in Single Channel Mode.

7.6.86 PFIR_A3 Register (Address = 0x41E) [reset = 0x0]

PFIR_A3 is shown in 図 7-102 and described in 表 7-116.

Return to the Summary Table.

PFIR Coefficient A3

図 7-102. PFIR_A3 Register

15	14	13	12	11	10	9	8
RESERVED				PFIR_A3			

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図 7-102. PFIR_A3 Register (continued)

R/W-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
PFIR_A3							
R/W-0x0							

表 7-116. PFIR_A3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	PFIR_A3	R/W	0x0	Signed, 2’s complement coefficient for the PFIR filter. This is the fourth tap for the ADC A programmable FIR filter in Dual Channel Mode or the fourth tap for the programmable FIR filter in Single Channel Mode.

7.6.87 PFIR_A4 Register (Address = 0x420) [reset = 0x0]

PFIR_A4 is shown in 図 7-103 and described in 表 7-117.

Return to the Summary Table.

PFIR Coefficient A4

図 7-103. PFIR_A4 Register

23	22	21	20	19	18	17	16
RESERVED						PFIR_A4	
R/W-0x0						R/W-0x0	
15	14	13	12	11	10	9	8
PFIR_A4							
R/W-0x0							
7	6	5	4	3	2	1	0
PFIR_A4							
R/W-0x0							

表 7-117. PFIR_A4 Register Field Descriptions

Bit	Field	Type	Reset	Description
23:18	RESERVED	R/W	0x0	
17:0	PFIR_A4	R/W	0x0	Signed, 2’s complement coefficient for the PFIR filter. This is the fifth tap for the ADC A programmable FIR filter in Dual Channel Mode or the fifth tap for the programmable FIR filter in Single Channel Mode. This is the center tap of the 9-tap filter and therefore has a resolution of 18-bits.

7.6.88 PFIR_A5 Register (Address = 0x423) [reset = 0x0]

PFIR_A5 is shown in 図 7-104 and described in 表 7-118.

Return to the Summary Table.

PFIR Coefficient A5

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図 7-104. PFIR_A5 Register

15	14	13	12	11	10	9	8
RESERVED				PFIR_A5			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PFIR_A5							
R/W-0x0							

表 7-118. PFIR_A5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	PFIR_A5	R/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the sixth tap for the ADC A programmable FIR filter in Dual Channel Mode or the sixth tap for the programmable FIR filter in Single Channel Mode.

7.6.89 PFIR_A6 Register (Address = 0x425) [reset = 0x0]

PFIR_A6 is shown in 図 7-105 and described in 表 7-119.

Return to the Summary Table.

PFIR Coefficient A6

図 7-105. PFIR_A6 Register

15	14	13	12	11	10	9	8
RESERVED				PFIR_A6			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PFIR_A6							
R/W-0x0							

表 7-119. PFIR_A6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	PFIR_A6	R/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the seventh tap for the ADC A programmable FIR filter in Dual Channel Mode or the seventh tap for the programmable FIR filter in Single Channel Mode.

7.6.90 PFIR_A7 Register (Address = 0x427) [reset = 0x0]

PFIR_A7 is shown in 図 7-106 and described in 表 7-120.

Return to the Summary Table.

PFIR Coefficient A7

図 7-106. PFIR_A7 Register

15	14	13	12	11	10	9	8
RESERVED				PFIR_A7			
R/W-0x0				R/W-0x0			

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図 7-106. PFIR_A7 Register (continued)

7	6	5	4	3	2	1	0
PFIR_A7							
R/W-0x0							

表 7-120. PFIR_A7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	PFIR_A7	R/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the eighth tap for the ADC A programmable FIR filter in Dual Channel Mode or the eighth tap for the programmable FIR filter in Single Channel Mode.

7.6.91 PFIR_A8 Register (Address = 0x429) [reset = 0x0]

PFIR_A8 is shown in 図 7-107 and described in 表 7-121.

Return to the Summary Table.

PFIR Coefficient A8

図 7-107. PFIR_A8 Register

15	14	13	12	11	10	9	8
RESERVED				PFIR_A8			
R/W-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
PFIR_A8							
R/W-0x0							

表 7-121. PFIR_A8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	PFIR_A8	R/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the ninth tap for the ADC A programmable FIR filter in Dual Channel Mode or the ninth tap for the programmable FIR filter in Single Channel Mode.

7.6.92 PFIR_B0 Register (Address = 0x448) [reset = 0x0]

PFIR_B0 is shown in 図 7-108 and described in 表 7-122.

Return to the Summary Table.

PFIR Coefficient B0

図 7-108. PFIR_B0 Register

15	14	13	12	11	10	9	8
RESERVED				PFIR_B0			
R/W-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
PFIR_B0							

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図 7-108. PFIR_B0 Register (continued)

R/W-0x0

表 7-122. PFIR_B0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	PFIR_B0	R/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the first tap for the ADC B programmable FIR filter in Dual Channel Mode.

7.6.93 PFIR_B1 Register (Address = 0x44A) [reset = 0x0]

PFIR_B1 is shown in 図 7-109 and described in 表 7-123.

Return to the Summary Table.

PFIR Coefficient B1

図 7-109. PFIR_B1 Register

15	14	13	12	11	10	9	8
RESERVED				PFIR_B1			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PFIR_B1							
R/W-0x0							

表 7-123. PFIR_B1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	PFIR_B1	R/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the second tap for the ADC B programmable FIR filter in Dual Channel Mode.

7.6.94 PFIR_B2 Register (Address = 0x44C) [reset = 0x0]

PFIR_B2 is shown in 図 7-110 and described in 表 7-124.

Return to the Summary Table.

PFIR Coefficient B2

図 7-110. PFIR_B2 Register

15	14	13	12	11	10	9	8
RESERVED				PFIR_B2			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PFIR_B2							
R/W-0x0							

表 7-124. PFIR_B2 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	

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表 7-124. PFIR_B2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	PFIR_B2	R/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the third tap for the ADC B programmable FIR filter in Dual Channel Mode.

7.6.95 PFIR_B3 Register (Address = 0x44E) [reset = 0x0]

PFIR_B3 is shown in 図 7-111 and described in 表 7-125.

Return to the Summary Table.

PFIR Coefficient B3

図 7-111. PFIR_B3 Register

15	14	13	12	11	10	9	8
RESERVED				PFIR_B3			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PFIR_B3							
R/W-0x0							

表 7-125. PFIR_B3 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	PFIR_B3	R/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the fourth tap for the ADC B programmable FIR filter in Dual Channel Mode.

7.6.96 PFIR_B4 Register (Address = 0x450) [reset = 0x0]

PFIR_B4 is shown in 図 7-112 and described in 表 7-126.

Return to the Summary Table.

PFIR Coefficient B4

図 7-112. PFIR_B4 Register

23	22	21	20	19	18	17	16
RESERVED						PFIR_B4	
R/W-0x0						R/W-0x0	
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PFIR_B4							
R/W-0x0							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PFIR_B4							
R/W-0x0							

表 7-126. PFIR_B4 Register Field Descriptions

Bit	Field	Type	Reset	Description
23:18	RESERVED	R/W	0x0	

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表 7-126. PFIR_B4 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17:0	PFIR_B4	R/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the fifth tap for the ADC B programmable FIR filter in Dual Channel Mode. This is the center tap of the 9-tap filter and therefore has a resolution of 18-bits.

7.6.97 PFIR_B5 Register (Address = 0x453) [reset = 0x0]

PFIR_B5 is shown in 図 7-113 and described in 表 7-127.

Return to the Summary Table.

PFIR Coefficient B5

図 7-113. PFIR_B5 Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PFIR_B5</td></tr>
<tr><td colspan="4">R/W-0x0</td><td colspan="4">R/W-0x0</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PFIR_B5</td></tr>
<tr><td colspan="8">R/W-0x0</td></tr>
</table>

表 7-127. PFIR_B5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	PFIR_B5	R/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the sixth tap for the ADC B programmable FIR filter in Dual Channel Mode.

7.6.98 PFIR_B6 Register (Address = 0x455) [reset = 0x0]

PFIR_B6 is shown in 図 7-114 and described in 表 7-128.

Return to the Summary Table.

PFIR Coefficient B6

図 7-114. PFIR_B6 Register

<table>
<tr><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">PFIR_B6</td></tr>
<tr><td colspan="4">R/W-0x0</td><td colspan="4">R/W-0x0</td></tr>
<tr><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="8">PFIR_B6</td></tr>
<tr><td colspan="8">R/W-0x0</td></tr>
</table>

表 7-128. PFIR_B6 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	

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表 7-128. PFIR_B6 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11:0	PFIR_B6	R/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the seventh tap for the ADC B programmable FIR filter in Dual Channel Mode.

7.6.99 PFIR_B7 Register (Address = 0x457) [reset = 0x0]

PFIR_B7 is shown in 図 7-115 and described in 表 7-129.

Return to the Summary Table.

PFIR Coefficient B7

図 7-115. PFIR_B7 Register

15	14	13	12	11	10	9	8
RESERVED				PFIR_B7			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PFIR_B7							
R/W-0x0							

表 7-129. PFIR_B7 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	PFIR_B7	R/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the eighth tap for the ADC B programmable FIR filter in Dual Channel Mode.

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7.6.100 PFIR_B8 Register (Address = 0x459) [reset = 0x0]

PFIR_B8 is shown in 図 7-116 and described in 表 7-130.

Return to the Summary Table.

PFIR Coefficient B8

図 7-116. PFIR_B8 Register

15	14	13	12	11	10	9	8
RESERVED				PFIR_B8			
R/W-0x0				R/W-0x0			
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PFIR_B8							
R/W-0x0							

表 7-130. PFIR_B8 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	
11:0	PFIR_B8	R(1)/W	0x0	Signed, 2's complement coefficient for the PFIR filter. This is the ninth tap for the ADC B programmable FIR filter in Dual Channel Mode.

(1) Read function does not properly return MSB value - the MSB value in readback is always 0.

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8 Application Information Disclaimer

Note

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8.1 Application Information

ADC08DJ5200RF can be used in a wide range of applications including radar, satellite communications, test equipment (communications testers and oscilloscopes), and software-defined radios (SDRs). The wide input bandwidth enables direct RF sampling to at least 10 GHz and the high sampling rate allows signal bandwidths of greater than 5 GHz. ADC08DJ5200RF can also be DC-coupled to meet the needs of oscilloscopes or wideband digitizers. The *Typical Applications* section describes two configurations that meet the needs of a number of these applications.

8.2 Typical Applications

8.2.1 Reconfigurable Dual-Channel 5-GSPS or Single-Channel 10-Gsps Oscilloscope

This section demonstrates the use of the device in a reconfigurable oscilloscope. The device is ideally suited for oscilloscope applications. The ability to tradeoff channel count and sampling speed allows designers to build flexible hardware to meet multiple needs. This flexibility saves development time and cost, allows hardware reuse for various projects and enables software upgrade paths for additional functionality. This section describes an oscilloscope that can operate as a dual-channel oscilloscope running at 5 GSPS or can be reconfigured through SPI programming as a single-channel, 10-GSPS oscilloscope. A reconfigurable setup allows users to trade off the number of channels and the sampling rate of the oscilloscope as needed without changing the hardware. Set the input bandwidth to the desired maximum signal bandwidth through the use of an antialiasing, low-pass filter. Digital filtering can then be used to reconfigure the analog bandwidth as required. For instance, the maximum bandwidth can be set to 2 GHz for use during pulsed transient detection and then reconfigured to 100 MHz through digital filtering for low-noise, power-supply ripple observation. 図 8-1 shows the application block diagram.

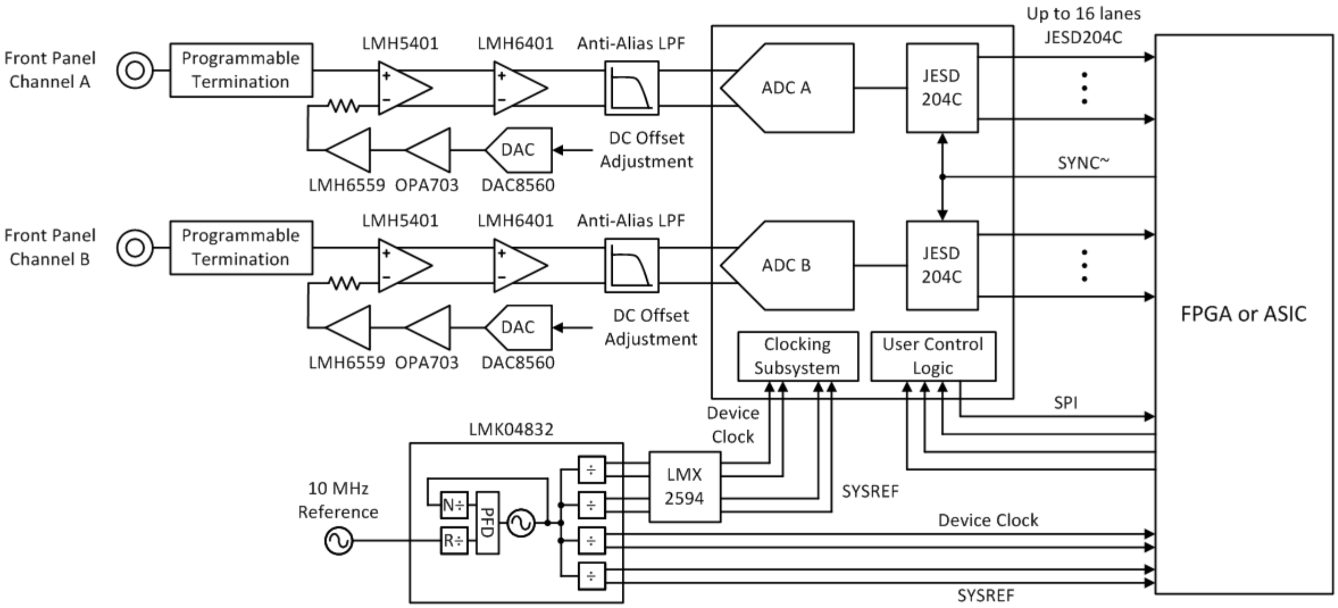

図 8-1. Typical Configuration for Reconfigurable Oscilloscope

8.2.1.1 Design Requirements

8.2.1.1.1 Input Signal Path

Most oscilloscopes are required to be DC-coupled in order to monitor DC or low-frequency signals. This requirement forces the design to use DC-coupled, fully differential amplifiers to convert from single-ended signaling at the front panel to differential signaling at the ADC. This design uses two differential amplifiers. The first amplifier shown in 図 8-1 is the LMH5401 that converts from single-ended to differential signaling. The LMH5401 interfaces with the front panel through a programmable termination network and has an offset adjustment input. The amplifier has an 8-GHz, gain-bandwidth product that is sufficient to support a 1-GHz bandwidth oscilloscope. A second amplifier, the LMH6401, comes after the LMH5401 to provide a digitally programmable gain control for the oscilloscope. The LMH6401 supports a gain range from –6 dB to 26 dB in 1-dB steps. If gain control is not necessary or is performed in a different location in the signal chain, then this amplifier can be replaced with a second LMH5401 for additional fixed gain or omitted altogether.

The input of the oscilloscope contains a programmable termination block that is not covered in detail here. This block enables the front-panel input termination to be programmed. For instance, many oscilloscopes allow the termination to be programmed as either 50-Ω or 1-MΩ to meet the needs of various applications. A 75-Ω termination can also be desired to support cable infrastructure use cases. This block can also contain an option for DC blocking to remove the DC component of the external signal and therefore pass only AC signals.

A precision DAC is used to configure the offset of the oscilloscope front-end to prevent saturation of the analog signal chain for input signals containing large DC offsets. The DAC8560 is shown in 図 8-1 along with signal-conditioning amplifiers OPA703 and LMH6559. The first differential amplifier, LMH5401, is driven by the front panel input circuitry on one input, and the DC offset bias on the second input. The impedance of these driving signals must be matched at DC and over frequency to ensure good even-order harmonic performance in the single-ended to differential conversion operation. The high bandwidth of the LMH6559 allows the device to maintain low impedance over a wide frequency range.

An antialiasing, low-pass filter is positioned at the input of the ADC to limit the bandwidth of the input signal into the ADC. This amplifier also band-limits the front-end noise to prevent aliased noise from degrading the signal-to-noise ratio of the overall system. Design this filter for the maximum input signal bandwidth specified by the oscilloscope. The input bandwidth can then be reconfigured through the use of digital filters in the FPGA or ASIC to limit the oscilloscope input bandwidth to a bandwidth less than the maximum.

8.2.1.1.2 Clocking

The ADC08DJ5200RF clock inputs must be AC-coupled to the device to ensure rated performance. The clock source must have extremely low jitter (integrated phase noise) to enable rated performance. Recommended clock synthesizers include LMX2594 and LMX2572.

The JESD204C data converter system (ADC plus logic device) requires additional SYSREF and device clocks. LMK04832, LMK04828, LMK04826, and LMK04821 devices are suitable to generate these clocks. Depending on the ADC clock frequency and jitter requirements, this device can also be used as the system clock synthesizer or as a device clock and SYSREF distribution device when multiple ADC08DJ5200RF devices are used in a system. For clock frequencies higher than 3.2 GHz, LMX2594 and LMX2572 can supply both the device clock and SYSREF from a single device.

8.2.1.1.3 ADC08DJ5200RF

ADC08DJ5200RF has a number of features that make it a great fit for oscilloscope applications. The low code-error rate (CER) eliminates concerns about undesired time domain glitches or sparkle codes. The low CER makes the device a perfect fit for long-duration transient detection measurements and reduces the probability of false triggers. The input common-mode voltage of 0 V allows the driving amplifiers to use equal split power supplies that center the amplifier output common-mode voltage at 0 V and eliminates the need for common-mode voltage shifting before the ADC inputs. The high input bandwidth of the device simplifies the design of the driving amplifier circuit and antialiasing, low-pass filter. The use of dual-edge sampling (DES) in single-channel mode eliminates the need to change the clock frequency when switching between dual- and single-channel modes and simplifies synchronization by relaxing the setup and hold timing requirements of SYSREF. The t_{AD}

adjust circuit allows the user to time-align the sampling instances of multiple ADC08DJ5200RF devices or to set the ideal sampling point of a front-end track and hold (T&H) amplifier.

8.3 Initialization Set Up

The device and JESD204C interface require a specific startup and alignment sequence. The order of that sequence is listed in the following steps.

1. Power-up or reset the device.
2. Apply a stable device CLK signal at the desired frequency.
3. Perform a software reset by toggling SOFT_RESET to 1. Wait at least 1 µs before continuing.
4. Program JESD_EN = 0 to stop the JESD204C state machine and allow setting changes.
5. Program CAL_EN = 0 to stop the calibration state machine and allow setting changes.
6. Program the desired JMODE.
7. Program the desired KM1 value. KM1 = K–1.
8. Program SYNC_SEL as needed. Choose SYNCSE or timestamp differential inputs.
9. Configure device calibration settings as desired. Select foreground or background calibration modes and offset calibration as needed.
10. Program CAL_EN = 1 to enable the calibration state machine.
11. Enable overrange via OVR_EN and adjust settings if desired.
12. Program JESD_EN = 1 to re-start the JESD204C state machine and allow the link to restart.
13. The JESD204C interface operates in response to the applied SYNC signal from the receiver.
14. Program CAL_SOFT_TRIG = 0.
15. Program CAL_SOFT_TRIG = 1 to initiate a calibration.

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9 Power Supply Recommendations

The device requires two different power-supply voltages. 1.9-V DC is required for the VA19 power bus and 1.1-V DC is required for the VA11 and VD11 power buses.

The power-supply voltages must be low noise and provide the needed current to achieve rated device performance.

There are two recommended power supply architectures:

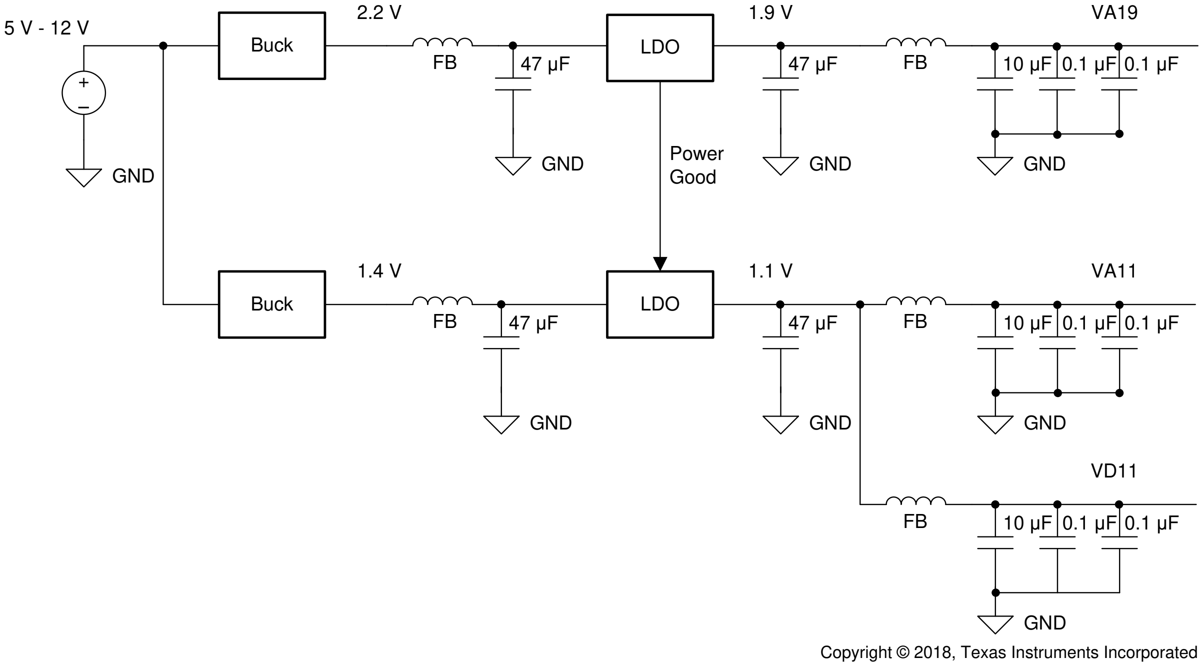
1. Step down using high-efficiency switching converters, followed by a second stage of regulation to provide switching noise reduction and improved voltage accuracy.
2. Directly step down the final ADC supply voltage using high-efficiency switching converters. This approach provides the best efficiency, but care must be taken for switching noise to be minimized to prevent degraded ADC performance.

TI WEBENCH® Power Designer can be used to select and design the individual power supply elements needed: see the WEBENCH® Power Designer

Recommended switching regulators for the first stage include LMS3635-Q1, LMS3655-Q1, TPSM84424 and similar devices.

Recommended low drop-out (LDO), low-noise linear regulators include the TPS7A84, TPS7A83A, TPS7A47 and similar devices.

For the switcher only approach, the ripple filter must be designed to provide sufficient filtering at the switching frequency of the DC-DC converter and harmonics of the switching frequency. Make a note of the switching frequency reported from WEBENCH® and design the EMI filter and capacitor combination to have the notch frequency centered as needed. Each application will have different tolerances for noise on the supply voltage so strict ripple requirements are not provided. 図 9-1 and 図 9-2 illustrate the two approaches.



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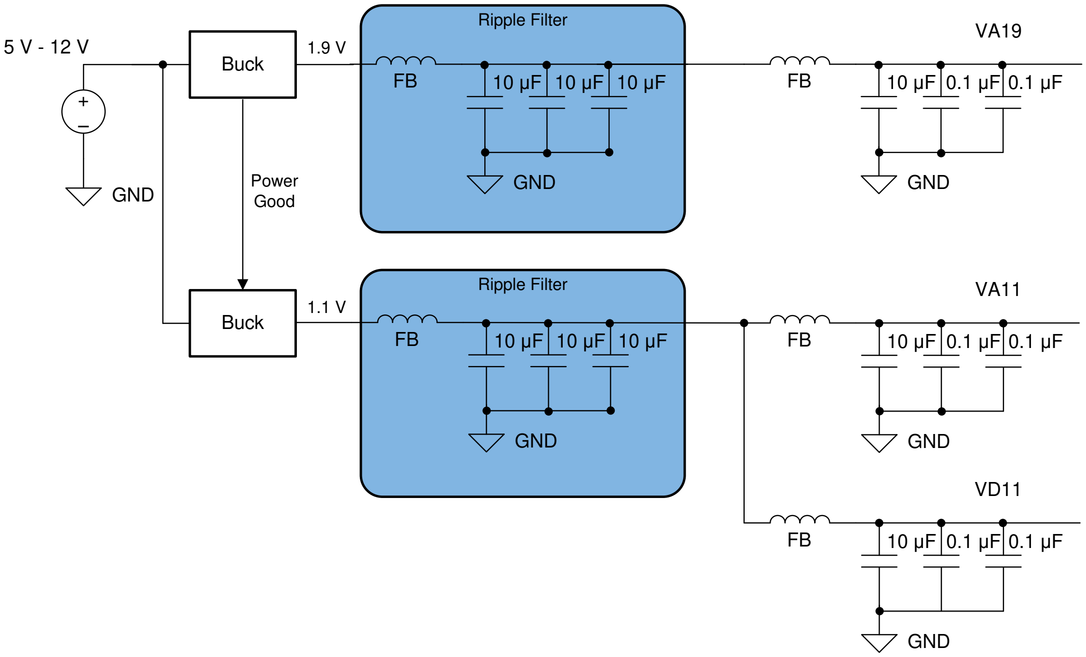
FB = ferrite bead filter.

図 9-1. LDO Linear Regulator Approach Example



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Ripple filter notch frequency to match the fs of the buck converter.

FB = ferrite bead filter.

図 9-2. Switcher-Only Approach Example

9.1 Power Sequencing

The voltage regulators must be sequenced using the power-good outputs and enable inputs to make sure the Vx11 regulator is enabled after the VA19 supply is good. Similarly, as soon as the VA19 supply drops out of regulation on power-down, the Vx11 regulator is disabled.

The general requirement for the ADC is that VA19 ≥ Vx11 during power-up, operation, and power-down.

TI also recommends that VA11 and VD11 are derived from a common 1.1-V regulator. This recommendation makes sure that all 1.1-V blocks are at the same voltage, and no sequencing problems exist between these supplies. Also use ferrite bead filters to isolate any noise on the VA11 and VD11 buses from affecting each other.

10 Layout

10.1 Layout Guidelines

There are many critical signals that require specific care during board design:

1. Analog input signals
2. CLK and SYSREF
3. JESD204C data outputs
4. Power connections
5. Ground connections

The analog input signals, clock signals and JESD204C data outputs must be routed for excellent signal quality at high frequencies, but should also be routed for maximum isolation from each other. Use the following general practices:

1. Route using loosely coupled 100-Ω differential traces when possible. This routing minimizes impact of corners and length-matching serpentines on pair impedance.
2. Provide adequate pair-to-pair spacing to minimize crosstalk, especially with loosely coupled differential traces. Tightly coupled differential traces may be used to reduce self-radiated noise or to improve neighboring trace noise immunity when adequate spacing cannot be provided.
3. Provide adequate ground plane pour spacing to minimize coupling with the high-speed traces. Any ground plane pour must have sufficient via connections to the main ground plane of the board. Do not use floating or poorly connected ground pours.
4. Use smoothly radiused corners. Avoid 45- or 90-degree bends to reduce impedance mismatches.
5. Incorporate ground plane cutouts at component landing pads to avoid impedance discontinuities at these locations. Cut-out below the landing pads on one or multiple ground planes to achieve a pad size or stackup height that achieves the needed 50-Ω, single-ended impedance.
6. Avoid routing traces near irregularities in the reference ground planes. Irregularities include cuts in the ground plane or ground plane clearances associated with power and signal vias and through-hole component leads.
7. Provide symmetrically located ground tie vias adjacent to any high-speed signal vias at an appropriate spacing as determined by the maximum frequency the trace will transport ($\ll \lambda_{MIN}/8$).
8. When high-speed signals must transition to another layer using vias, transition as far through the board as possible (top to bottom is best case) to minimize via stubs on top or bottom of the vias. If layer selection is not flexible, use back-drilled or buried, blind vias to eliminate stubs. Always place ground vias close to the signal vias when transitioning between layers to provide a nearby ground return path.

Pay particular attention to potential coupling between JESD204C data output routing and the analog input routing. Switching noise from the JESD204C outputs can couple into the analog input traces and show up as wideband noise due to the high input bandwidth fo the ADC. Ideally, route the JESD204C data outputs on a separate layer from the ADC input traces to avoid noise coupling (not shown in the *Layout Example* section). Tightly coupled traces can also be used to reduce noise coupling.

Impedance mismatch between the CLK± input pins and the clock source can result in reduced amplitude of the clock signal at the ADC CLK± pins due to signal reflections or standing waves. A reduction in the clock amplitude may degrade ADC noise performance, especially at high input frequencies. To avoid this, keep the clock source close to the ADC (as shown in the *Layout Example* section) or implement impedance matching at the ADC CLK± input pins.

In addition, TI recommends performing signal quality simulations of the critical signal traces before committing to fabrication. Insertion loss, return loss, and time domain reflectometry (TDR) evaluations should be done.

The power and ground connections for the device are also very important. These rules must be followed:

1. Provide low-resistance connection paths to all power and ground pins.
2. Use multiple power layers if necessary to access all pins.
3. Avoid narrow isolated paths that increase connection resistance.
4. Use a signal, ground, or power circuit board stackup to maximum coupling between the ground and power planes.

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10.2 Layout Example

図 10-1 to 図 10-3 provide examples of the critical traces routed on the device evaluation module (EVM).

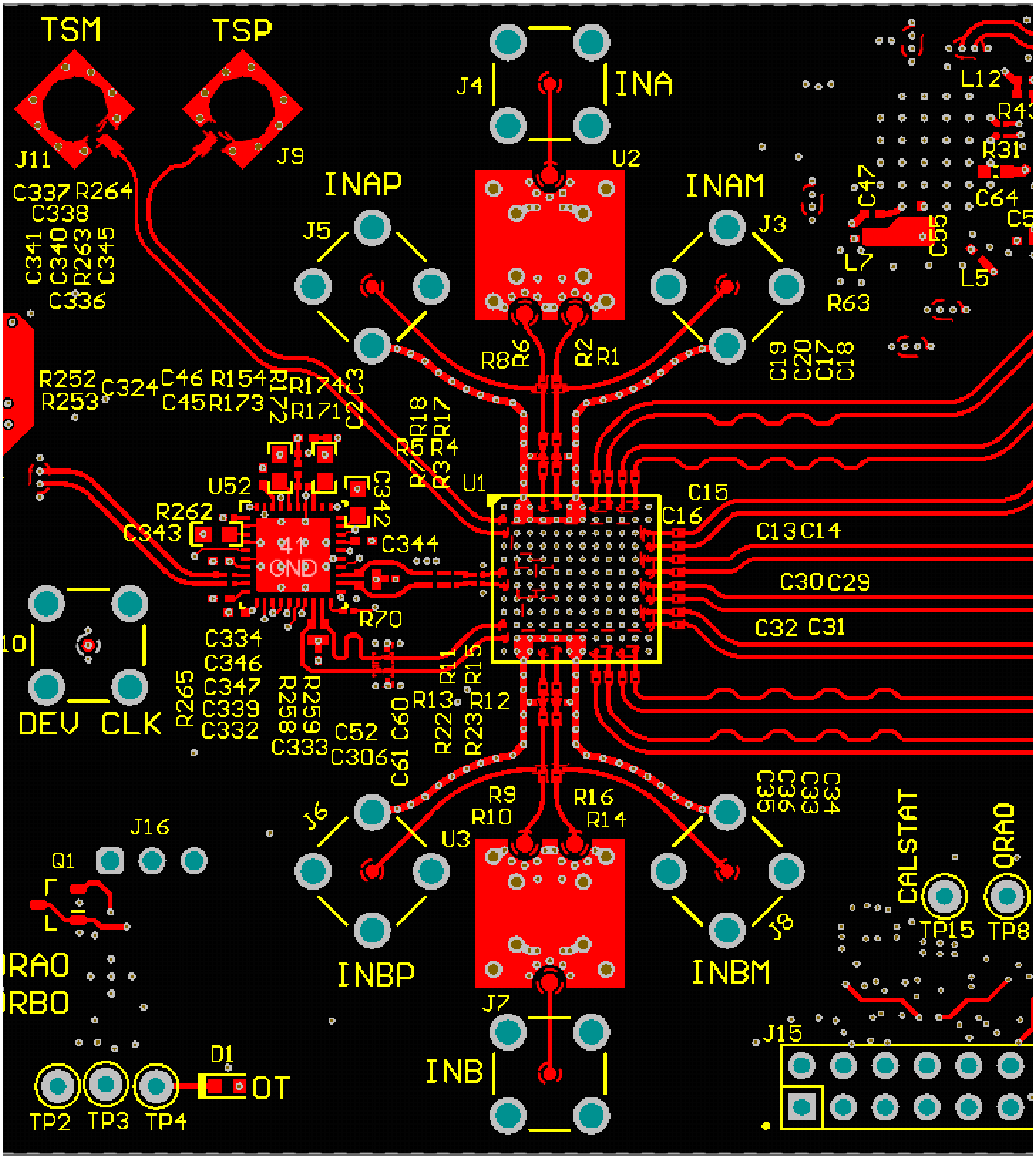

図 10-1. Top Layer Routing: Analog Inputs, CLK and SYSREF, DA0-3, DB0-3

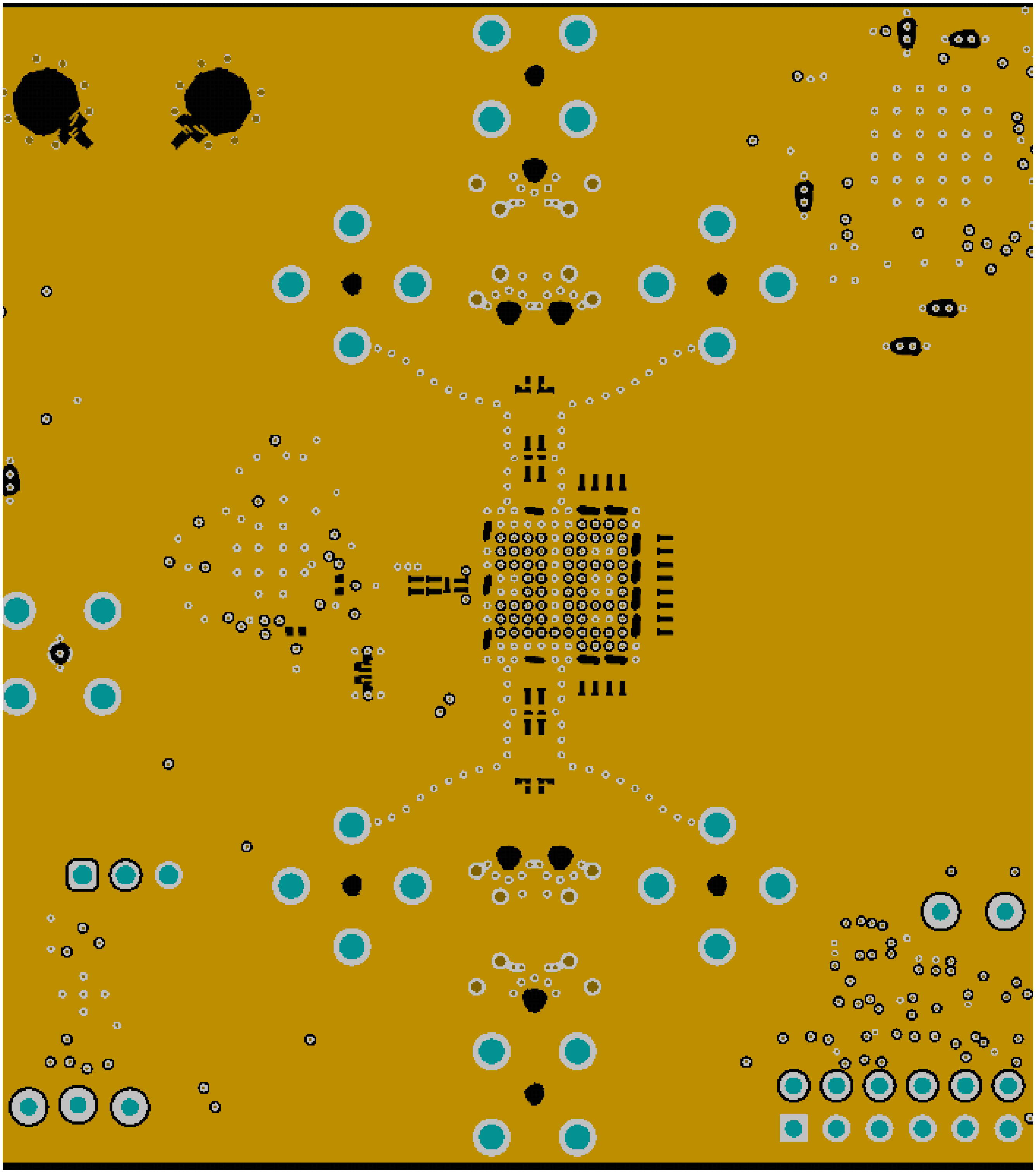

図 10-2. GND1 Cutouts to Optimize Impedance of Component Pads

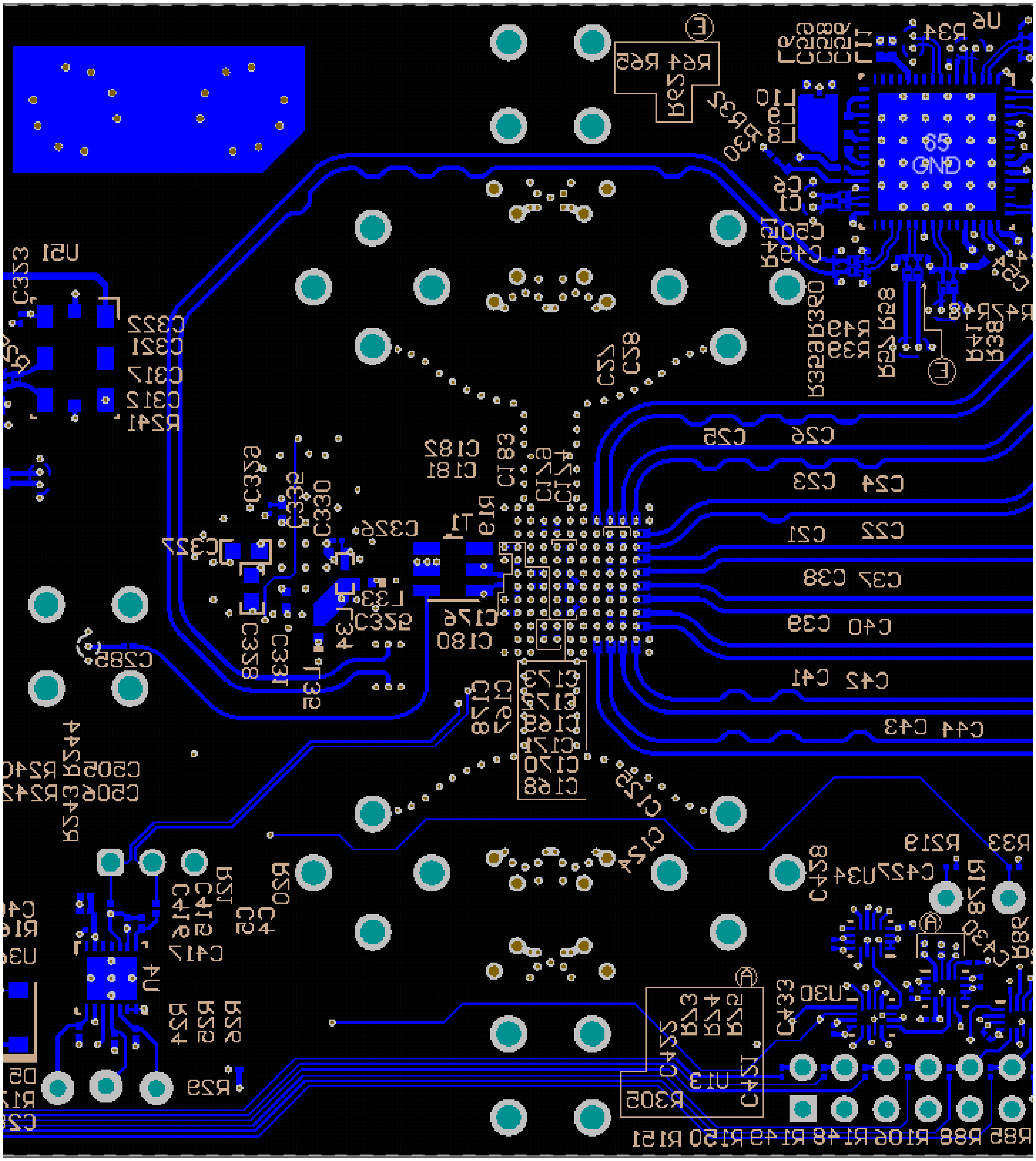

図 10-3. Bottom Layer Routing: Additional CLK Routing, DA4-7, DB4-7

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1

WEBENCH® Power Designer

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *ADC12DJ5200RF Evaluation Module User's Guide*
- *JESD204B multi-device synchronization: Breaking down the requirements*
- *Scalable 20.8 GSPS reference design for high speed 12 bit digitizers*
- *Synchronizing multi-channel data converter DDC and NCO features for RF systems reference design*
- *Multi-Channel JESD204B 15 GHz Clocking Reference Design for DSO, Radar and 5G Wireless Testers*
- *Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems*
- *Low noise power-supply reference design maximizing performance in 12.8 GSPS data acquisition systems*
- *12.8-GSPS analog front end reference design for high-speed oscilloscope and wide-band digitizer*
- *Direct RF-Sampling Radar Receiver for L-, S-, C-, and X-Band Using ADC12DJ3200 Reference Design*
- *LMX2594 Multiple PLL Reference Design*
- *LMX2594 15-GHz Wideband PLLatinum™ RF Synthesizer With Phase Synchronization and JESD204B*
- *LMX2572 6.4-GHz Low Power Wideband RF Synthesizer With Phase Synchronization and JESD204B*
- *LMK04832 Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner With Dual Loop PLLs*
- *LMK0482x Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs*
- *LMK61E2 Ultra-Low Jitter Programmable Oscillator With Internal EEPROM*
- *LMH5401 8-GHz, Low-Noise, Low-Power, Fully-Differential Amplifier*
- *LMH6401 DC to 4.5 GHz, Fully-Differential, Digital Variable-Gain Amplifier*
- *TPSM84424 4.5-V to 17-V Input, 0.6-V to 10-V Output, 4-A Power Module*
- *TPS7A470x 36-V, 1-A, 4-µVRMS, RF LDO Voltage Regulator*
- *TPS7A83A 2-A, High-Accuracy (0.75%), Low-Noise (4.4 µVRMS) LDO Regulator*
- *TPS7A84 High-Current (3 A), High-Accuracy (1%), Low-Noise (4.4 µVRMS), LDO Voltage Regulator*
- *DAC8560 16-Bit, Ultra-Low Glitch, Voltage Output Digital-to-Analog Converter With 2.5-V, 2-ppm/°C Reference*
- *LM95233 Dual Remote Diode and Local Temperature Sensor with SMBus Interface and TruTherm™*
- *TMP461 High-Accuracy Remote and Local Temperature Sensor with Pin-Programmable Bus Address*

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11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

11.5 Trademarks

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11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC08DJ5200RFAAV	ACTIVE	FCCSP	AAV	144	168	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADC08DJ52 RF	Samples
ADC08DJ5200RFAAVT	ACTIVE	FCCSP	AAV	144	250	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	ADC08DJ52 RF	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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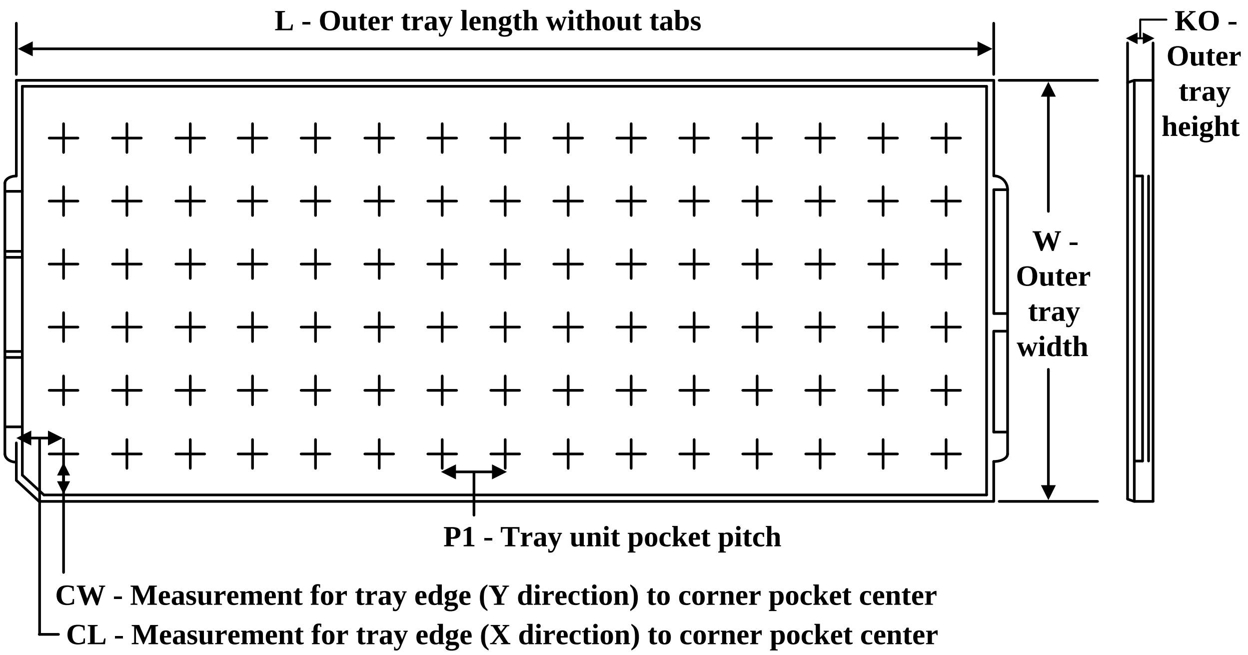
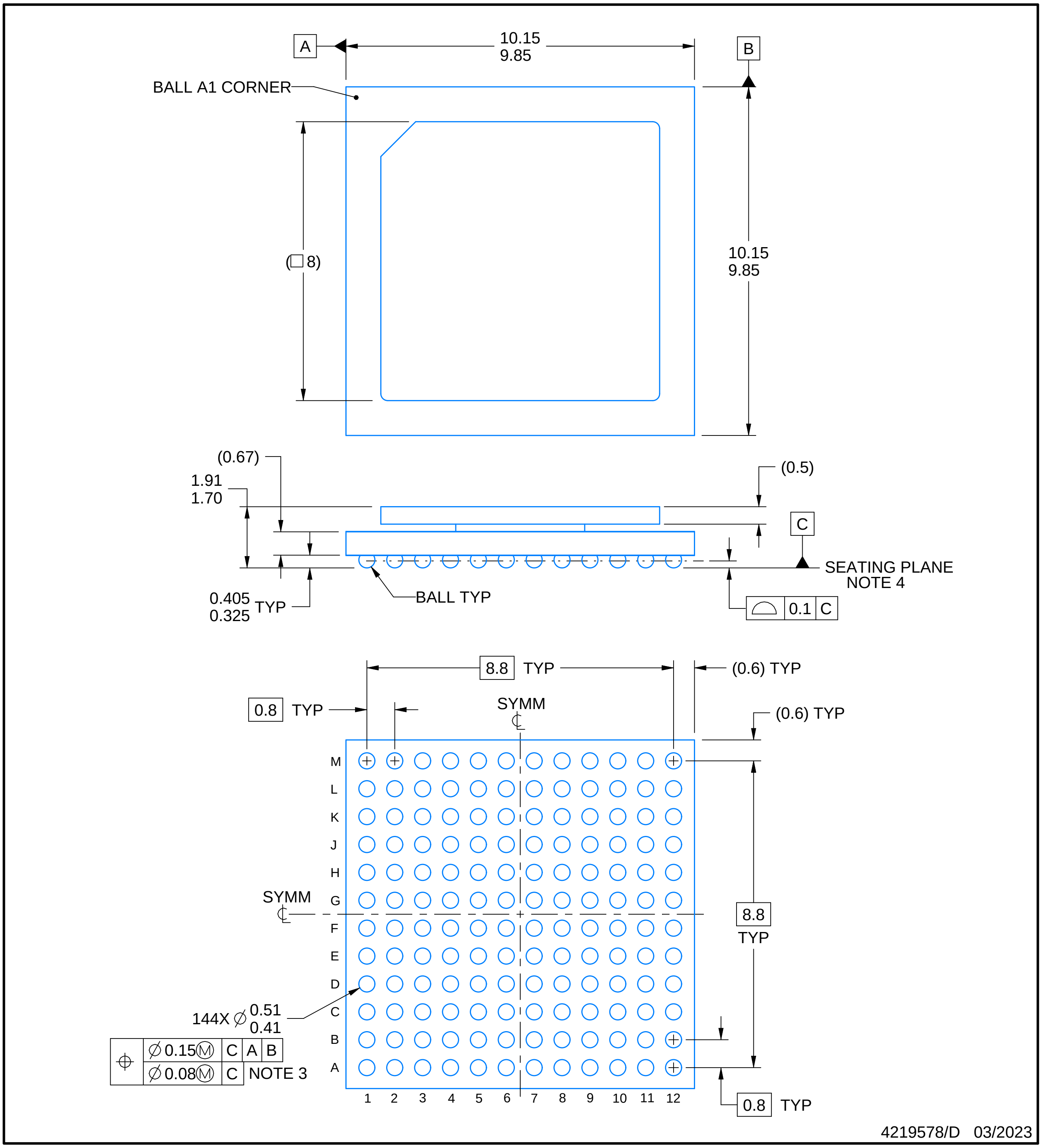
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADC08DJ5200RFAAV	AAV	FCCSP	144	168	8 X 21	150	315	135.9	7620	14.65	11	11.95



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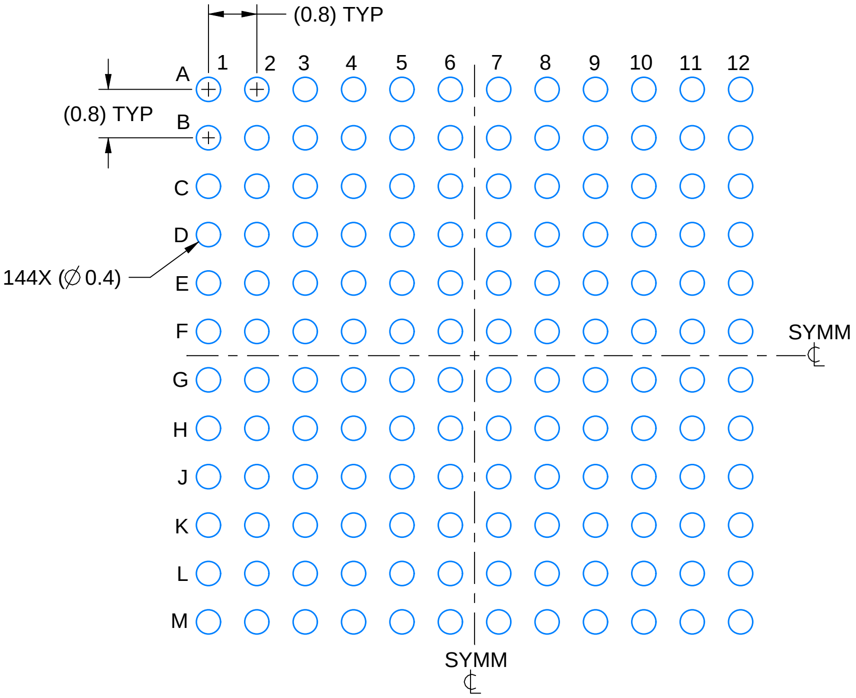
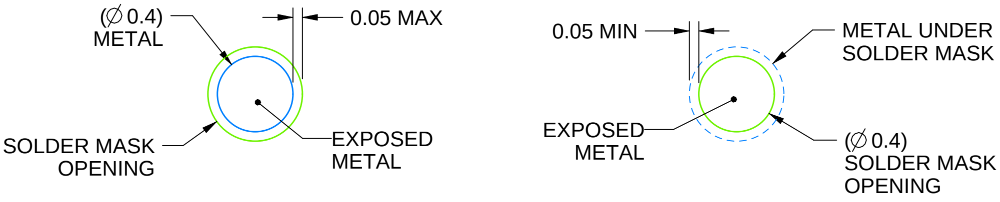
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



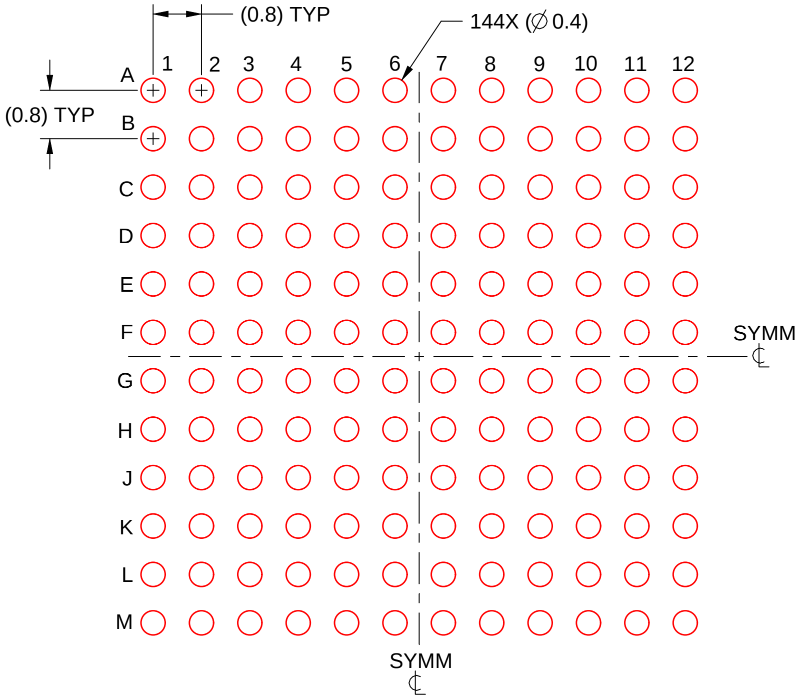
NON-SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

6. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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