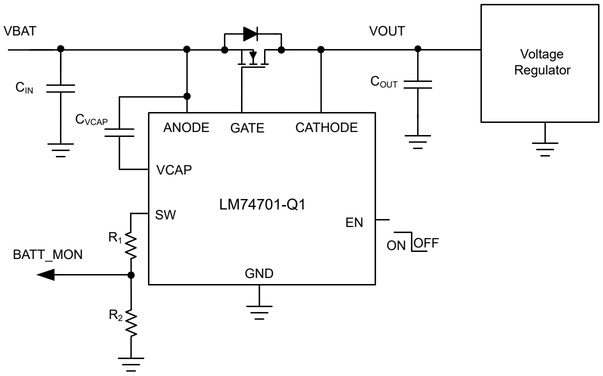
LM74701-Q1 車載用 TVS レスのバッテリ逆接続保護の理想ダイオード・コントローラ

1 特長

- 下記内容で AEC-Q100 認定済み
  - デバイス温度グレード 1: -40℃～+125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C4B
- 3.2V～65V の入力範囲 (スタートアップ時 3.9V)
- 逆電圧定格：–33V
- 外部の N チャネル MOSFET 用のチャージ・ポンプ
- アノードからカソードへの順方向電圧降下レギュレーション：20mV
- シャットダウン時電流 (EN = LOW)：1μA
- 動作時静止電流 (EN = HIGH)：80μA
- ピーク・ゲート・ターンオフ電流：2A
- 逆電流阻止に対する高速応答：0.75μs 未満
- バッテリ電圧監視スイッチ (SW) を内蔵
- 入力 TVS ダイオードを追加せずに車載 ISO7637 過渡要件に適合 (TVS レス)
- 8 ピンの SOT-23 パッケージ (2.90mm × 1.60mm)

2 アプリケーション

- 車載用 ADAS システム – カメラ
- 車載用インフォテインメント・システム – ヘッド・ユニット、テレマティクス制御ユニット
- 車載用 USB ハブ
- 冗長化電源用のアクティブ OR



代表的なアプリケーション回路図

3 概要

LM74701-Q1 は、外部の N チャネル MOSFET と組み合わせることで理想ダイオードとして動作し、20mV の順方向電圧降下で低損失逆極性保護を実現する車載用 AEC Q100 認定済み理想ダイオード・コントローラです。LM74701-Q1 は、12V 車載用システムの入力保護に適しています。3.2V の入力電圧をサポートしているため、車載用システムの厳しいコールド・クランク要件に特に適しています。

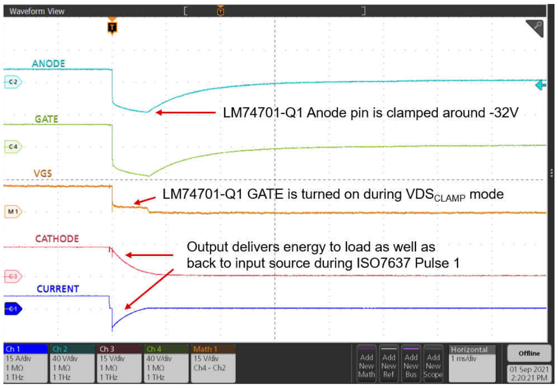
このデバイスは、MOSFET のゲートを制御し、順方向電圧降下を 20mV にレギュレートします。このレギュレーション方式により、逆電流発生時に MOSFET を穏やかにオフにでき、DC 逆電流を確実にゼロにします。このデバイスは、逆電流阻止への応答が高速 (0.75μs 未満) なため、ISO7637 のパルス・テスト時や電源障害および入力マイクロ短絡状況で出力電圧のホールドアップ要件を持つシステムに適しています。LM74701-Q1 は独自の VDS クランプ機能を内蔵しています。この機能を使うと、TVS を使わない入力極性保護ソリューションを実現でき、制約の厳しい車載システムの PCB 面積を平均で 60% 節約できます。

LM74701-Q1 コントローラは、外部の N チャネル MOSFET に対してチャージ・ポンプによるゲート駆動を行います。イネーブル・ピンが LOW のとき、コントローラはオフで、消費電流は約 1μA です。

製品情報[1]

部品番号	パッケージ	本体サイズ (公称)
LM74701-Q1	SOT-23 (8)	2.90mm × 1.60mm

(1)　利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



TVS レスの ISO7637-2 パルス 1 性能

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (June 2021) to Revision A (December 2021)	Page
• ステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

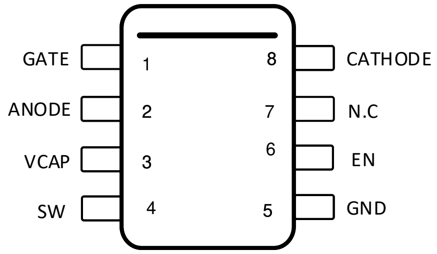


図 5-1. DDF Package 8-Pin SOT-23 Top View

表 5-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
1	GATE	O	Gate drive output. Connect to gate of the external N-channel MOSFET.
2	ANODE	I	Anode of the ideal diode and input power. Connect to the source of the external N-channel MOSFET.
3	VCAP	O	Charge pump output. Connect to external charge pump capacitor.
4	SW	O	Voltage sensing disconnect switch terminal. ANODE and SW are internally connected through a switch when EN is high. A resistor ladder from this pin to GND can be used to monitor battery voltage. When EN is pulled low, the switch is OFF disconnecting the resistor ladder from the battery line thereby cutting off the leakage current.
5	GND	G	Ground pin
6	EN	I	Enable pin. Can be connected to ANODE for always ON operation.
7	N.C	—	No connect. Keep this pin floating.
8	CATHODE	I	Cathode of the ideal diode. Connect to the drain of the external N-channel MOSFET.

(1) I = Input, O = Output, G = GND

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Pins	ANODE to GND	$-(V_{CLAMP}-1)$	65	V
	SW, EN to GND, $V_{(ANODE)} > 0$ V	–0.3	65	V
	EN to GND, $V_{(ANODE)} \leq 0$ V	$V_{(ANODE)}$	$(65 + V_{(ANODE)})$	V
	SW to GND, $V_{(ANODE)} \leq 0$ V	$V_{(ANODE)}$	$(0.3 + V_{(ANODE)})$	V
	I_{SW}	–1	10	mA
Output Pins	GATE to ANODE	–0.3	15	V
	VCAP to ANODE	–0.3	15	V
Output to Input Pins	CATHODE to ANODE	–5	V_{CLAMP}	V
Operating junction temperature(2)		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (GATE ,SW, GND, CATHODE)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
Input Pins	ANODE to GND	–33		60	V
	CATHODE to GND			60	
	EN to GND	–33		60	
Input to Output pins	ANODE to CATHODE	$-V_{CLAMP}$		5	V
External capacitance	ANODE	0.1		1	µF
	VCAP to ANODE	0.1			µF
External MOSFET max V_{GS} rating	GATE to ANODE	15			V
T_J	Operating junction temperature range(2)	–40		150	°C

(1) Recommended Operating Conditions are conditions under which the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.

(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC[1]		LM74701-Q1	UNIT
		DDF (SOT)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	133.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	54.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(ANODE)}$ = 12 V, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ANODE} SUPPLY VOLTAGE						
V_{CLAMP}	V(CATHODE–ANODE) clamp voltage		34		43	V
$V_{(ANODE)}$	Operating input voltage		4		60	V
$V_{(ANODE\ POR)}$	VANODE POR Rising threshold				3.9	V
	VANODE POR Falling threshold		2.2	2.8	3.1	V
$V_{(ANODE\ POR(Hys))}$	VANODE POR Hysteresis		0.44		0.67	V
$I_{(SHDN)}$	Shutdown Supply Current	$V_{(EN)}$ = 0 V		0.9	1.5	µA
$I_{(Q)}$	Operating Quiescent Current			80	130	µA
ENABLE INPUT						
$V_{(EN\_IL)}$	Enable input low threshold		0.5	0.9	1.22	V
$V_{(EN\_IH)}$	Enable input high threshold		1.06	2	2.6	V
$V_{(EN\_Hys)}$	Enable Hysteresis		0.52		1.35	V
$I_{(EN)}$	Enable sink current	$V_{(EN)}$ = 12 V		3	5	µA
V_{ANODE} to $V_{CATHODE}$						
$V_{(AK\ REG)}$	Regulated Forward $V_{(AK)}$ Threshold		13	20	29	mV
$V_{(AK)}$	$V_{(AK)}$ threshold for full conduction mode		34	54	59	mV
$V_{(AK\ REV)}$	$V_{(AK)}$ threshold for reverse current blocking		–17	–11	–2	mV
Gm	Regulation Error AMP Transconductance [1]		1200	1800	3100	µA/V
SWITCH						
$R_{(SW)}$	Battery sensing disconnect switch resistance	4 V < $V_{(ANODE)}$ ≤ 60 V	10	19.5	46	Ω
GATE DRIVE						
$I_{(GATE)}$	Peak source current	$V_{(ANODE)} – V_{(CATHODE)}$ = 100 mV, $V_{(GATE)} – V_{(ANODE)}$ = 5 V	3	11		mA
	Peak sink current	$V_{(ANODE)} – V_{(CATHODE)}$ = –20 mV, $V_{(GATE)} – V_{(ANODE)}$ = 5 V		2000		mA
	Regulation max sink current	$V_{(ANODE)} – V_{(CATHODE)}$ = 0 V, $V_{(GATE)} – V_{(ANODE)}$ = 5 V	6	26		µA
RDS_{ON}	discharge switch RDS_{ON}	$V_{(ANODE)} – V_{(CATHODE)}$ = –20 mV, $V_{(GATE)} – V_{(ANODE)}$ = 100 mV	0.4		2	Ω
CHARGE PUMP						

6.5 Electrical Characteristics (continued)

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(ANODE)}$ = 12 V, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(VCAP)}$	Charge Pump source current (Charge pump on)	$V_{(VCAP)} – V_{(ANODE)}$ = 7 V	162	300	600	µA
	Charge Pump sink current (Charge pump off)	$V_{(VCAP)} – V_{(ANODE)}$ = 14 V		5	10	µA
$V_{(VCAP)} – V_{(ANODE)}$	Charge pump voltage at $V_{(ANODE)}$ = 3.2 V	$I_{(VCAP)} \le 30$ µA	8			V
	Charge pump turn on voltage		10.3	11.6	13	V
	Charge pump turn off voltage		11	12.4	13.9	V
	Charge Pump Enable comparator Hysteresis		0.4	0.8	1.2	V
$V_{(VCAP\ UVLO)}$	$V_{(VCAP)} – V_{(ANODE)}$ UV release at rising edge	$V_{(ANODE)} – V_{(CATHODE)}$ = 100 mV	5.7	6.5	7.5	V
	$V_{(VCAP)} – V_{(ANODE)}$ UV threshold at falling edge	$V_{(ANODE)} – V_{(CATHODE)}$ = 100 mV	5.05	5.4	6.2	V
CATHODE						
$I_{(CATHODE)}$	CATHODE sink current	$V_{(ANODE)}$ = 12 V, $V_{(ANODE)} – V_{(CATHODE)}$ = –100 mV		1.7	2	µA
$I_{(CATHODE)}$	CATHODE sink current	$V_{(ANODE)} – V_{(CATHODE)}$ = –100 mV		1.2	2.5	µA
$I_{(CATHODE)}$	CATHODE sink current	$V_{(ANODE)}$ = –14 V, $V_{(DRAIN)}$ = 0 V			2	µA
$I_{(CATHODE)}$	CATHODE sink current	$V_{(ANODE)}$ = –16 V, $V_{(CATHODE)}$ = 16 V			24	µA

(1) Parameter assured by design and characterization

6.6 Switching Characteristics

T_J = –40°C to +125°C; typical values at T_J = 25°C, $V_{(ANODE)}$ = 12 V, $C_{(VCAP)}$ = 0.1 µF, $V_{(EN)}$ = 3.3 V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EN_{TDLY}	Enable (low to high) to Gate Turn On delay	$V_{(VCAP)} > V_{(VCAP\ UVLOR)}$		75	110	µs
$t_{Reverse\ delay}$	Reverse voltage detection to Gate Turn Off delay	$V_{(ANODE)} – V_{(CATHODE)}$ = 100 mV to –100 mV		0.45	0.75	µs
$t_{Forward\ recovery}$	Forward voltage detection to Gate Turn On delay	$V_{(ANODE)} – V_{(CATHODE)}$ = –100 mV to 700 mV		1.4	2.6	µs

6.7 Typical Characteristics

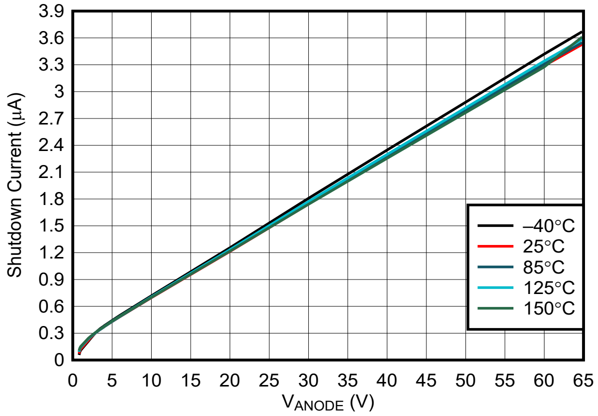


図 6-1. Shutdown Supply Current vs Supply Voltage

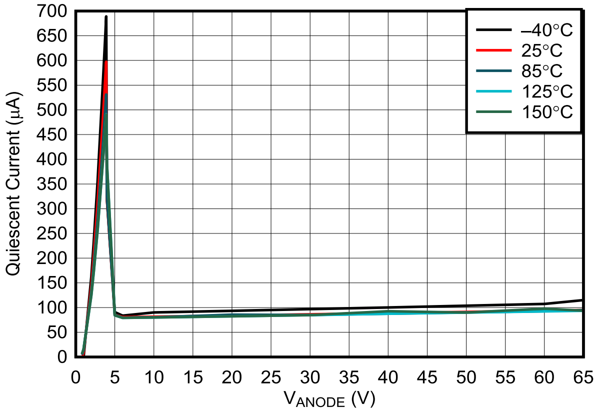


図 6-2. Operating Quiescent Current vs Supply Voltage

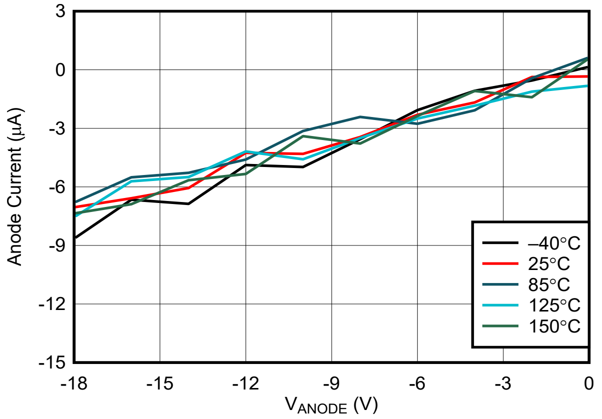


図 6-3. Anode Current vs Negative Supply Voltage

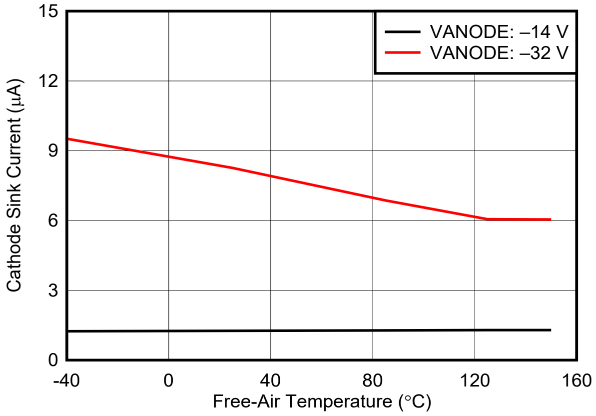


図 6-4. CATHODE Sink Current vs Supply Voltage

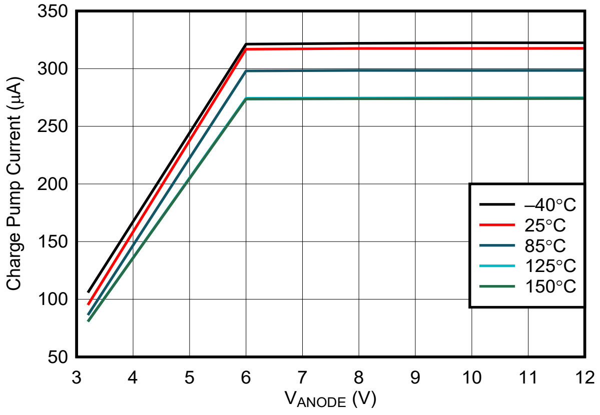


図 6-5. Charge Pump Current vs Supply Voltage at V_{CAP} = 6 V

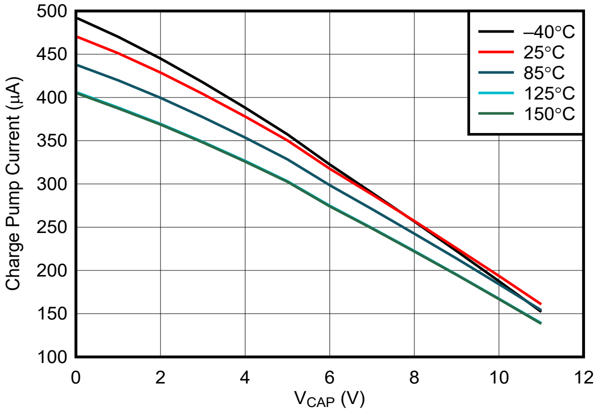


図 6-6. Charge Pump V-I Characteristics at V_{ANODE} > = 12 V

6.7 Typical Characteristics (continued)

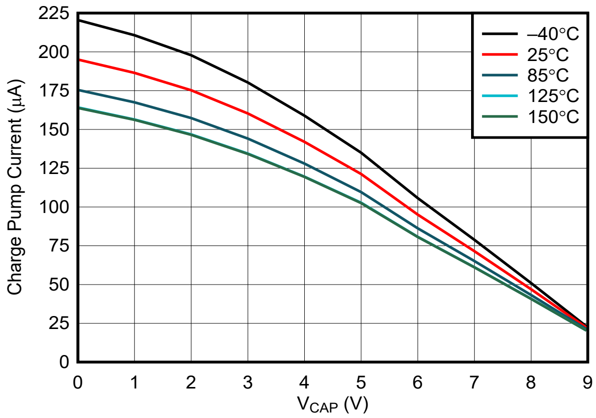


図 6-7. Charge Pump V-I Characteristics at V_{ANODE} = 3.2 V

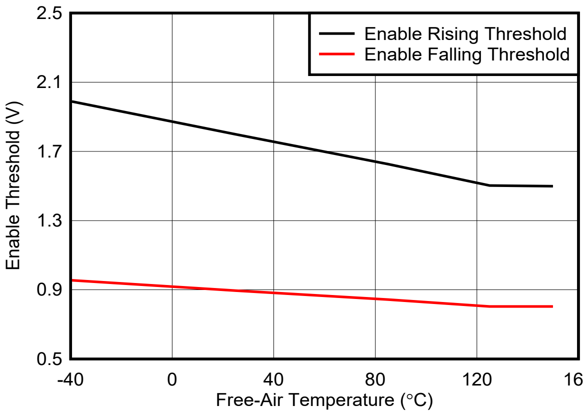


図 6-8. Enable Falling threshold vs Temperature

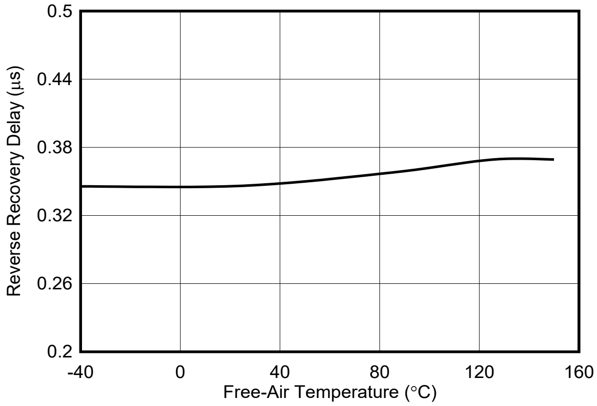


図 6-9. Reverse Current Blocking Delay vs Temperature

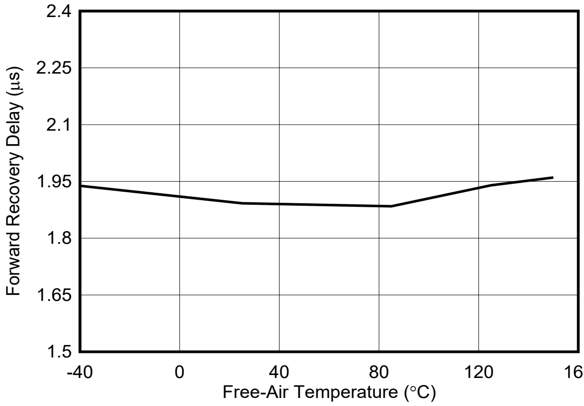


図 6-10. Forward Recovery Delay vs Temperature

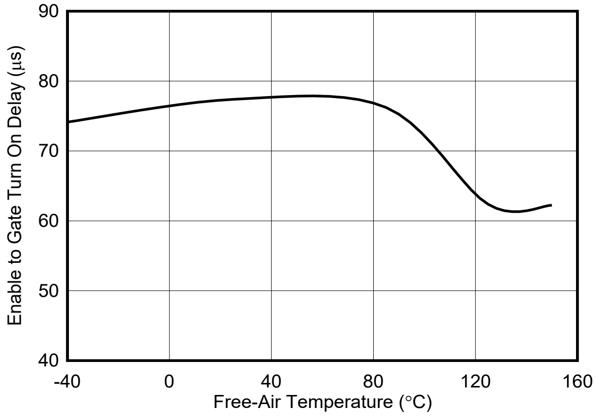


図 6-11. Enable to Gate Delay vs Temperature

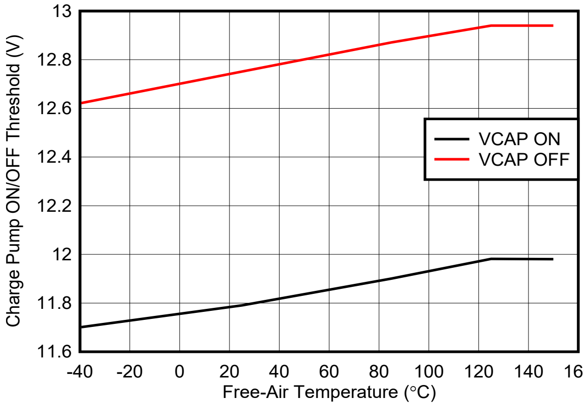


図 6-12. Charge Pump ON and OFF Threshold vs Temperature

6.7 Typical Characteristics (continued)

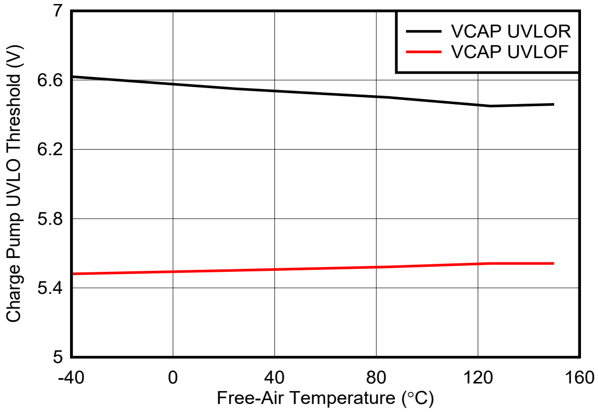


図 6-13. Charge Pump UVLO Threshold vs Temperature

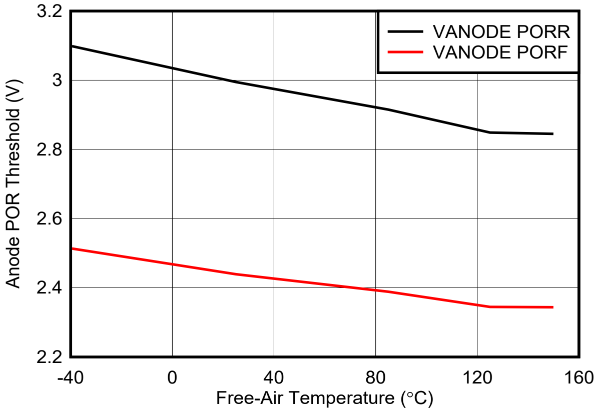


図 6-14. V_{ANODE} POR Threshold vs Temperature

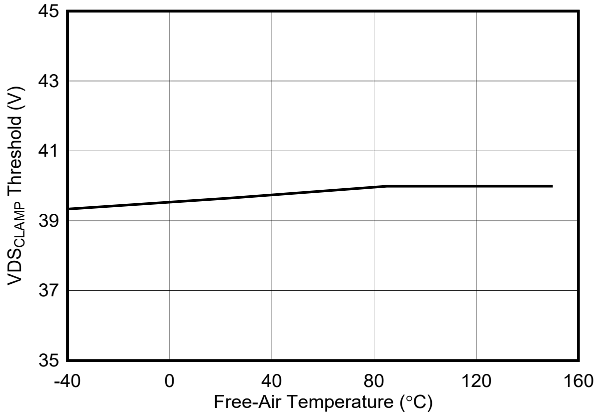


図 6-15. VDS_{CLAMP} Threshold vs Temperature

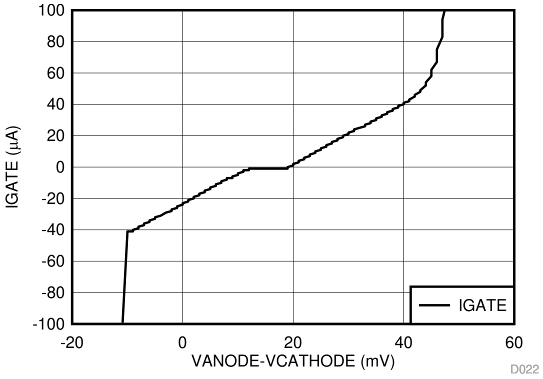


図 6-16. Gate Current vs Forward Voltage Drop

7 Parameter Measurement Information

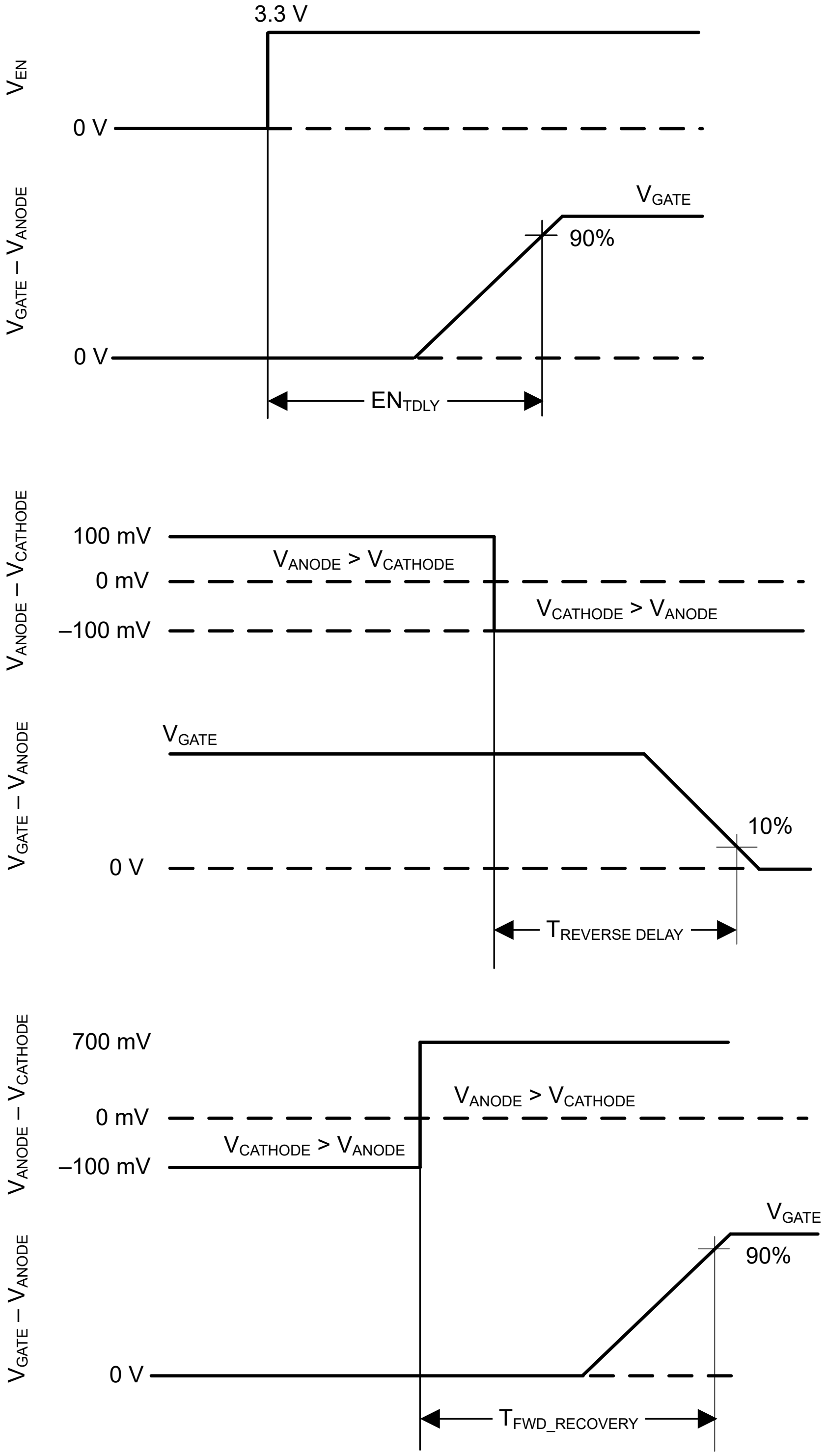


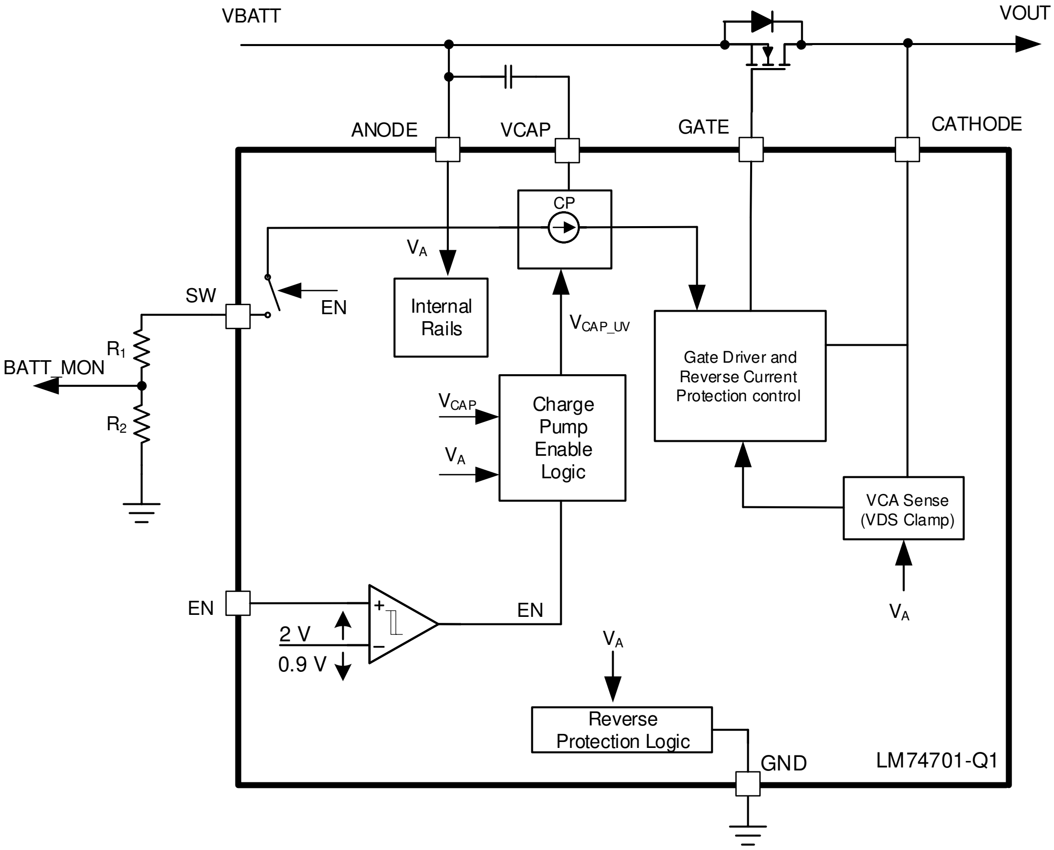
図 7-1. Timing Waveforms

8 Detailed Description

8.1 Overview

The LM74701-Q1 ideal diode controller has all the features necessary to implement an efficient and fast reverse polarity protection circuit while minimizing the number of external components. This easy to use ideal diode controller is paired with an external N-channel MOSFET to replace other reverse polarity schemes such as a P-channel MOSFET or a Schottky diode. An internal charge pump is used to drive the external N-Channel MOSFET to a maximum gate drive voltage of approximately 12 V. The voltage drop across the MOSFET is continuously monitored between the ANODE and CATHODE pins, and the GATE to ANODE voltage is adjusted as needed to regulate the forward voltage drop at 20 mV. This closed loop regulation scheme enables graceful turn off of the MOSFET during a reverse current event and ensures zero DC reverse current flow. A fast reverse current condition is detected when the voltage across ANODE and CATHODE pins reduces below −11 mV, resulting in the GATE pin being internally connected to the ANODE pin turning off the external N-channel MOSFET, and using the body diode to block any of the reverse current. An enable pin, EN is available to place the LM74701-Q1 in shutdown mode disabling the N-Channel MOSFET and minimizing the quiescent current. When device is enabled, an internal switch between SW and ANODE pin enables input voltage monitoring using an external resistor divider connected to SW pin. The device integrates VDS clamp feature which enables input TVS less reverse polarity protection. For additional details on achieving input TVS less reverse polarity protection solution, refer to the *Device Functional Modes* and *Application Information* section.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage

The ANODE pin is used to power the LM74701-Q1's internal circuitry, typically drawing 80 µA when enabled and 1 µA when disabled. If the ANODE pin voltage is greater than the POR rising threshold, then LM74701-Q1 operates in either shutdown mode or conduction mode in accordance with the EN pin voltage. The voltage from ANODE to GND is designed to vary from 65 V to –33 V, allowing the LM74701-Q1 to withstand negative voltage input.

8.3.2 Charge Pump

The charge pump supplies the voltage necessary to drive the external N-channel MOSFET. An external charge pump capacitor is placed between VCAP and ANODE pins to provide energy to turn on the external MOSFET. In order for the charge pump to supply current to the external capacitor the EN pin voltage must be above the specified input high threshold, $V_{(EN\_IH)}$. When enabled, the charge pump sources a charging current of 300 µA typical. If EN pins is pulled low, then the charge pump remains disabled. To ensure that the external MOSFET can be driven above its specified threshold voltage, the VCAP to ANODE voltage must be above the undervoltage lockout threshold, typically 6.5 V, before the internal gate driver is enabled. Use 式 1 to calculate the initial gate driver enable delay.

$$T_{(DRV\_EN)} = 75\ \mu s + C_{(VCAP)} \times \frac{V_{(VCAP\_UVLOR)}}{300\ \mu A} \tag{1}$$

where

- $C_{(VCAP)}$ is the charge pump capacitance connected across ANODE and VCAP pins
- $V_{(VCAP\_UVLOR)}$ = 6.5 V (typical)

To remove any chatter on the gate drive, approximately 800 mV of hysteresis is added to the VCAP undervoltage lockout. The charge pump remains enabled until the VCAP to ANODE voltage reaches 12.4 V, typically, at which point the charge pump is disabled decreasing the current draw on the ANODE pin. The charge pump remains disabled until the VCAP to ANODE voltage is below to 11.6 V typically at which point the charge pump is enabled. The voltage between VCAP and ANODE continue to charge and discharge between 11.6 V and 12.4 V as shown in 図 8-1. By enabling and disabling the charge pump, the operating quiescent current of the LM74701-Q1 is reduced. When the charge pump is disabled it sinks 5 µA typically.

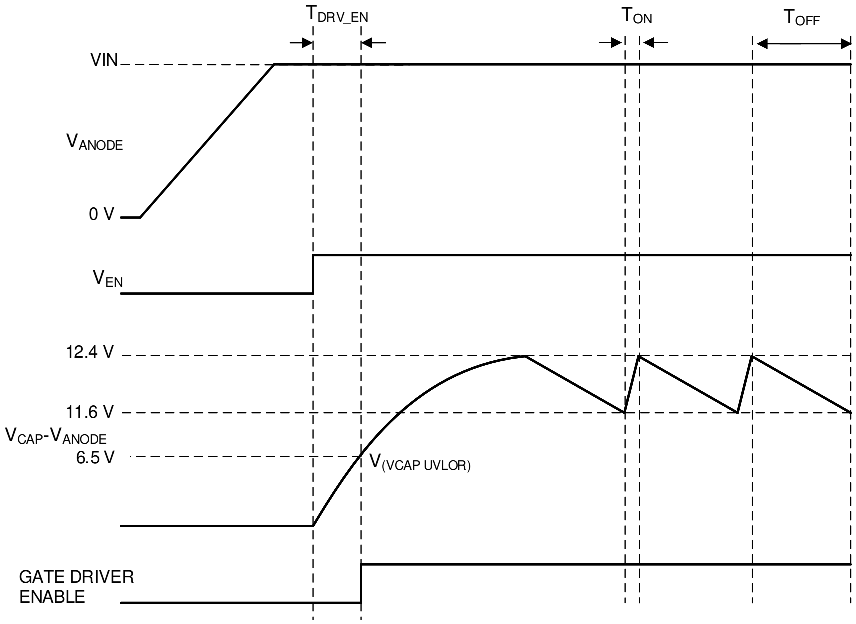


図 8-1. Charge Pump Operation

8.3.3 Gate Driver

The gate driver is used to control the external N-Channel MOSFET by setting the GATE to ANODE voltage to the corresponding mode of operation. There are four defined modes of operation that the gate driver operates under forward regulation, full conduction mode, reverse current protection and VDS clamp mode according to the ANODE to CATHODE voltage. These modes of operation are described in more detail in the *Regulated Conduction Mode*, *Full Conduction Mode* , Reverse Current Protection Mode and *VDS Clamp Mode* sections. 図 8-2 depicts how the modes of operation vary according to the ANODE to CATHODE voltage of the LM74701-Q1. The threshold between forward regulation mode and conduction mode is when the ANODE to CATHODE voltage is 50 mV. The threshold between forward regulation mode and reverse current protection mode is when the ANODE to CATHODE voltage is –11 mV. The threshold between reverse current protection mode and VDS clamp mode is when the ANODE to CATHODE voltage is –39-V typical.

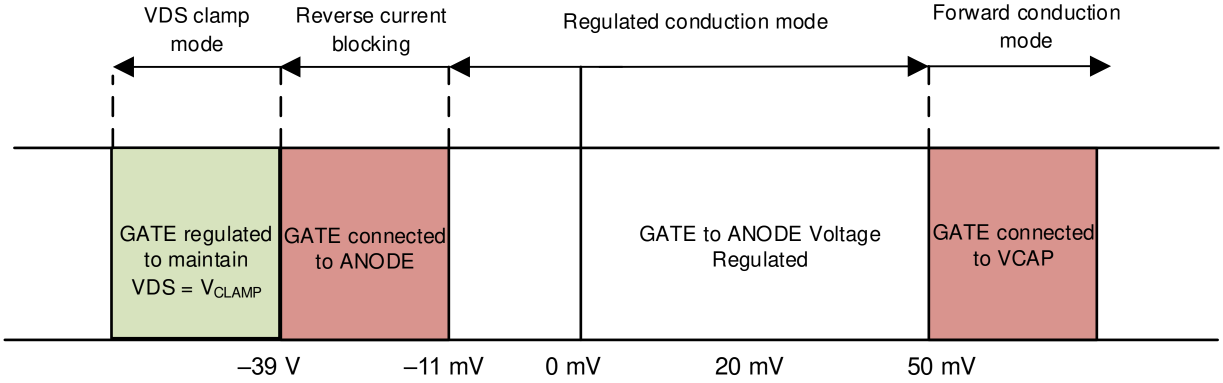


図 8-2. Gate Driver Mode Transitions

Before the gate driver is enabled following three conditions must be achieved:

- The EN pin voltage must be greater than the specified input high voltage.
- The VCAP to ANODE voltage must be greater than the undervoltage lockout voltage.
- The ANODE voltage must be greater than VANODE POR Rising threshold.

If the above conditions are not achieved, then the GATE pin is internally connected to the ANODE pin, assuring that the external MOSFET is disabled. After these conditions are achieved, the gate driver operates in the correct mode depending on the ANODE to CATHODE voltage.

8.3.4 Enable

The LM74701-Q1 has an enable pin, EN. The enable pin allows for the gate driver to be either enabled or disabled by an external signal. If the EN pin voltage is greater than the rising threshold, the gate driver and charge pump operates as described in *Gate Driver* and *Charge Pump* sections. If the enable pin voltage is less than the input low threshold, the charge pump and gate driver are disabled placing the LM74701-Q1 in shutdown mode. The EN pin can withstand a voltage as large as 65 V and as low as –33 V. This feature allows for the EN pin to be connected directly to the ANODE pin if enable functionality is not needed. In conditions where EN is left floating, the internal sink current of 1 uA pulls EN pin low and disables the device.

8.3.5 Battery Voltage Monitoring (SW)

The LM74701-Q1 has SW pin to enable battery voltage monitoring in automotive systems. When the device is enabled, an internal switch connects SW pin to ANODE. This feature enables monitoring battery voltage using an external resistor divider connected from SW pin to GND. When LM74701-Q1 is put in shutdown mode by pulling down the EN pin low, an internal switch between SW and ANODE pin is disconnected. This action ensures there is no quiescent current drawn by the resistor ladder when system is put into low power shutdown mode. When not used, SW pin must be left floating.

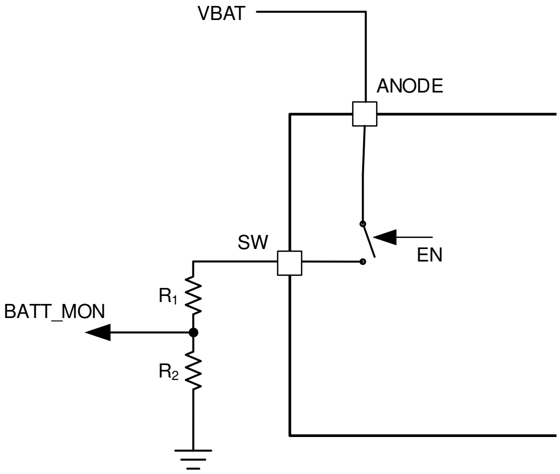


図 8-3. LM74701-Q1 SW Pin Functionality

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The LM74701-Q1 enters shutdown mode when the EN pin voltage is below the specified input low threshold $V_{(EN\_IL)}$. Both the gate driver and the charge pump are disabled in shutdown mode. During shutdown mode, the LM74701-Q1 enters low I_Q operation with the ANODE pin only sinking 1 µA. When the LM74701-Q1 is in shutdown mode, forward current flow through the external MOSFET is not interrupted but is conducted through the MOSFET's body diode.

8.4.2 Conduction Mode

Conduction mode occurs when the gate driver is enabled. There are three regions of operating during conduction mode based on the ANODE to CATHODE voltage of the LM74701-Q1. Each of the three modes is described in the *Regulated Conduction Mode*, *Full Conduction Mode* and *VDS Clamp Mode* sections.

8.4.2.1 Regulated Conduction Mode

For the LM74701-Q1 to operate in regulated conduction mode, the gate driver must be enabled as described in the *Gate Driver* section and the current from source to drain of the external MOSFET must be within the range to result in an ANODE to CATHODE voltage drop of –11 mV to 50 mV. During forward regulation mode the ANODE to CATHODE voltage is regulated to 20 mV by adjusting the GATE to ANODE voltage. This closed loop regulation scheme enables graceful turn off of the MOSFET at very light loads and ensures zero DC reverse current flow.

8.4.2.2 Full Conduction Mode

For the LM74701-Q1 to operate in full conduction mode, the gate driver must be enabled as described in the *Gate Driver* section, and the current from source to drain of the external MOSFET must be large enough to result in an ANODE to CATHODE voltage drop of greater than 50-mV typical. If these conditions are achieved, the GATE pin is internally connected to the VCAP pin resulting in the GATE to ANODE voltage being approximately the same as the VCAP to ANODE voltage. By connecting VCAP to GATE the external MOSFET's $R_{DS(ON)}$ is minimized reducing the power loss of the external MOSFET when forward currents are large.

8.4.2.3 VDS Clamp Mode

The LM74701-Q1 features an integrated VDS clamp that operates the external MOSFET as an active clamp element to dissipate transient energy of automotive EMC transients such as ISO7637-2 pulse 1 where there is no output voltage hold up requirement and system is allowed to turn off during such EMC transients. VDS clamp threshold is selected such that LM74701-Q1 does not engage into VDS clamp operation thereby ensuring the FET remains OFF during the RCB state for the system level EMC tests where output voltage hold up is required such as input short interruptions and micro cuts (LV124 E-10, ISO16750-2).

When the ISO7637 pulse 1 is applied at the input of LM74701-Q1:

1. After the voltage drop across ANODE to CATHODE reaches V(AK_REV) threshold, the device GATE goes low and turns OFF the MOSFET.
2. After the voltage across the drain and source of the MOSFET reaches VCLAMP level (34-V minimum), GATE is turned ON back in the saturation region, operating external MOSFET as an active clamp and dissipates the ISO7637 pulse 1 energy. The typical circuit operation of LM74701-Q1 during ISO7637 pulse 1 is shown in 図 8-4.

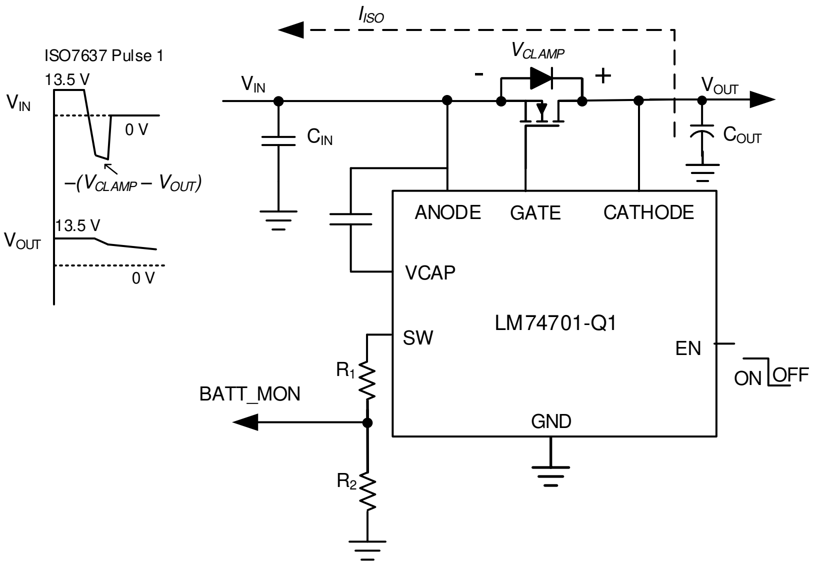


図 8-4. LM74701-Q1 Operation During VDS Clamp Mode

Note that the reverse current flows from VOUT back to input during the ISO7637 pulse 1 transient event, thus discharging VOUT capacitor. LM74701-Q1 CATHODE pin can handle negative voltage, however, if loads connected to the output of LM74701-Q1 can not handle negative voltage then the output hold up capacitor must be selected to ensure that VOUT does not go negative during ISO7637 pulse 1 test. For all the other ISO7637 pulses (that is, pulse 2a, 2b, 3a, 3b), which are short duration transient events, the input and output capacitors filtering effect suppresses these pulses.

For additional details on system level EMC performance of LM74701-Q1, refer to *Application Information.*

8.4.3 Reverse Current Protection Mode

For the LM74701-Q1 to operate in reverse current protection mode, the gate driver must be enabled as described in the *Gate Driver* section and the current of the external MOSFET must be flowing from the drain to the source. When the ANODE to CATHODE voltage is typically less than –11 mV, reverse current protection mode is entered and the GATE pin is internally connected to the ANODE pin. The connection of the GATE to ANODE pin disables the external MOSFET. The body diode of the MOSFET blocks any reverse current from flowing from the drain to source.

9 Application and Implementation

Note

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9.1 Application Information

The LM74701-Q1 is used with N-Channel MOSFET to achieve a typical reverse polarity protection solution. The schematic for the 12-V battery protection application is shown in 図 9-1 where the LM74701-Q1 is used to drive N-Channel MOSFET Q1 in series with a battery. The VDS clamp feature integrated into LM74701-Q1 enables input TVS less operation. TI recommends the output capacitor C_{OUT} to protect the immediate output voltage collapse as a result of line disturbance and to make sure output remains positive during all system EMC transient tests.

9.2 Typical Application

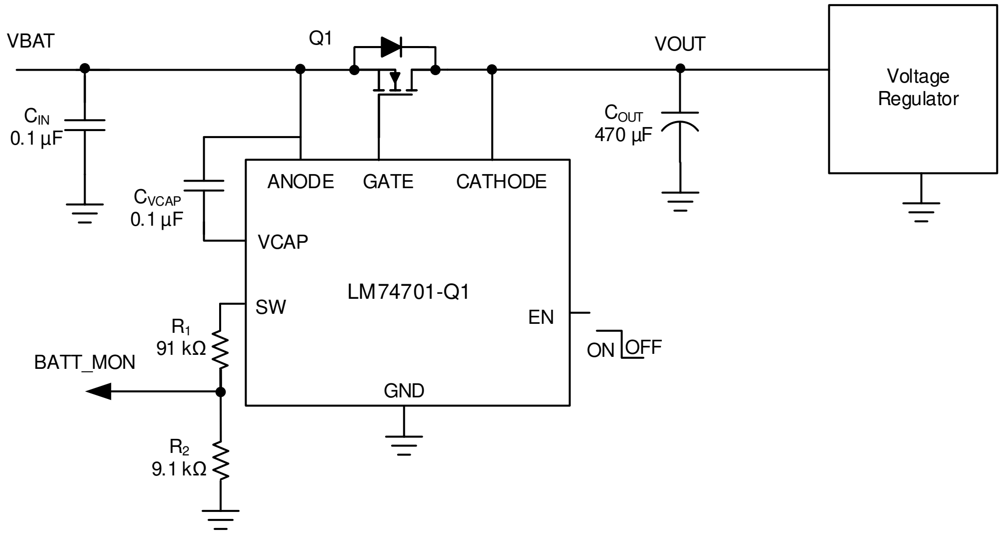


図 9-1. Typical Application Circuit

9.2.1 Design Requirements

A design example, with system design parameters listed in 表 9-1, is presented.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	12 - battery, 13.5-V nominal with 3.2-V cold crank and 35-V load dump
Output voltage	3.2 V during cold crank to 35-V load dump
Output current range	3-A nominal, 6-A maximum
Output capacitance	470-µF typical hold-up capacitance
Key automotive EMC tests	ISO 7637-2 (–100 V, pulse 1, pulse 2a, pulse 2b), ISO 16750-2 (Suppressed load dump 35 V), LV124, E-10 (input micro short)

9.2.2 Detailed Design Procedure

9.2.2.1 Design Considerations

- Input operating voltage range, including cold crank and load dump conditions
- Nominal load current and maximum load current
- Robust EMC performance during key automotive EMC transient tests

9.2.2.2 MOSFET Selection

For selecting the blocking MOSFET Q1, important electrical parameters are the maximum continuous drain current ID, the maximum drain-to-source voltage VDS(MAX), the maximum drain-to-source voltage VGS(MAX), Safe Operating Area (SOA), the maximum source current through body diode, and the drain-to-source ON resistance RDSON.

The maximum continuous drain current (ID) rating must exceed the maximum continuous load current.

To reduce the MOSFET conduction losses, MOSFET with the lowest possible $R_{DS(ON)}$ is preferred, but selecting a MOSFET based on low $R_{DS(ON)}$ can not be beneficial always. Higher $R_{DS(ON)}$ provides increased voltage information to LM74701-Q1's reverse current comparator at a lower reverse current. Reverse current detection is better with increased $R_{DS(ON)}$. Choosing a MOSFET with forward voltage drop of less than 50 mV at maximum current is a good starting point.

The maximum drain-to-source voltage, $VDS_{(MAX)}$, must be high enough to withstand the highest differential voltage seen in the application. With LM74701-Q1, the maximum differential voltage across the MOSFET is V_{CLAMP} (max) of 43 V. TI recommends a minimum of 60-V VDS rated. This recommendation includes all the automotive transient events and any anticipated fault conditions.

During the ISO7637 Pulse 1, the maximum VDS seen by the external MOSFET Q1 is $VDS_{CLAMP\ (max)}$ that is 43 V. The peak current during ISO7637-2 pulse 1 can be calculated by 式 2.

$$I_{ISO\_PEAK} = (V_{ISO} + V_{OUT} - VDS_{CLAMP(max)}) / R_S \tag{2}$$

Where

- V_{ISO} is the negative peak of the ISO7637-2 pulse 1
- V_{OUT} is the initial level of the VBATT before ISO pulse is applied
- VDS_{CLAMP} is maximum VCLAMP threshold of LM74701-Q1
- R_S is the ISO7637 pulse generator input impedance (10 Ω)

For ISO7637-2 pulse 1 with amplitude of –100 V, V_{OUT} nominal voltage of 13.5 V the peak reverse current flowing from the MOSFET Q1 comes around 7 A.

The current profile tapers down from 7 A to 0 A from the peak of 7 A as shown in 図 9-5. The resulting average current (I_{ISO_AVG}) can be approximated as one third of the peak current that is around 2.4 A. The VDS clamp operation lasts for about 1 ms. Selecting a MOSFET with SOA characteristics covering the load line of 43 V which can support drain current greater than ($I_{ISO\_PEAK}/2$) for 1 msec is a good starting point. For this particular design example, MOSFET which can support greater than 3.5 A of drain current at 43-V V_{DS} on SoA curve is suitable.

図 9-2 shows typical SoA characteristics plot highlighting maximum drain current supported by the MOSFET for the duration of 1 ms. MOSFET data sheet SoA curves are typically plotted at ambient temperature, so consider sufficient margin over MOSFET parameters calculated values to ensure safe operation over desired operating temperature range.

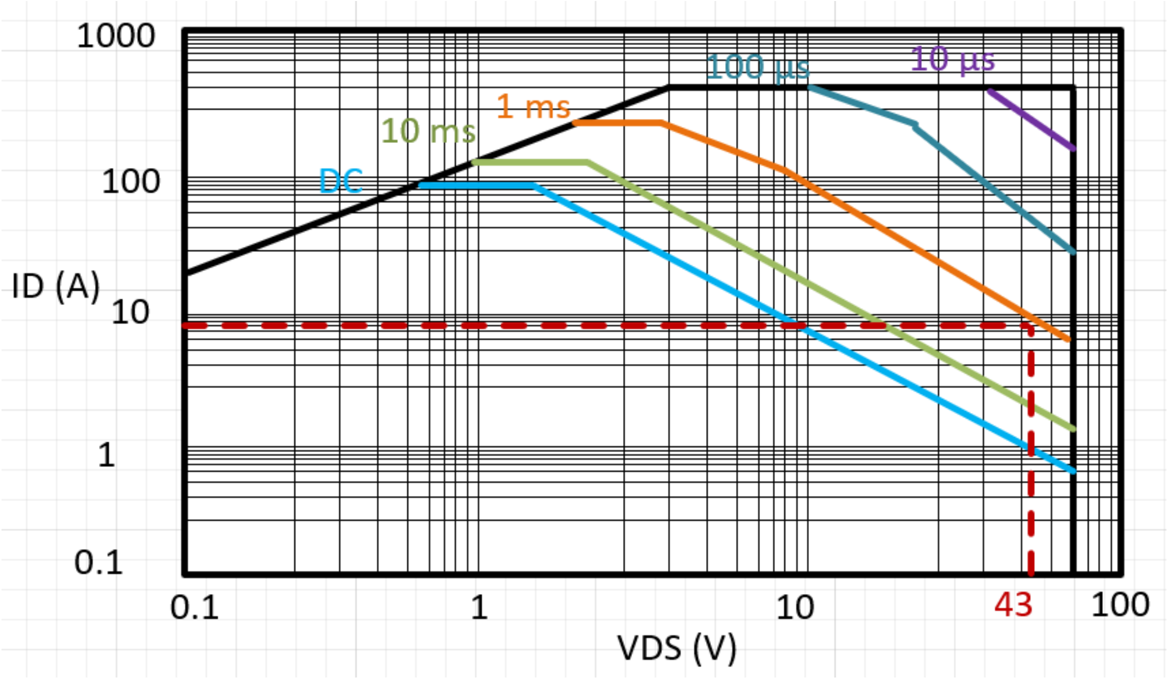


図 9-2. Typical MOSFET SoA Characteristics

As external MOSFET dissipates ISO7637-2 Pulse 1 energy, a special attention must be given while calculating maximum power dissipation and effective temperature rise. An average power dissipation across the MOSFET can be calculated by 式 3.

$$P_{D\_AVG} = VDS_{CLAMP(max)} \times I_{ISO\_AVG} \quad (3)$$

For given design example, average power dissipation comes around.

$$P_{D\_AVG} = 43\text{ V} \times 2.4\text{ A} = 103.2\text{ W} \quad (4)$$

Typical ISO7637-2 pulse 1 transient lasts for 2 ms with total time period of 200 ms between two consecutive pulses (duty cycle of 1%). The effective temperature rise due to power dissipation across MOSFET during ISO7637-2 pulse 1 event can be calculated by looking at transient thermal impedance curve in a MOSFET data sheet. Figure 9-3 shows an example of how to estimate transient thermal impedance of a MOSFET for ISO7637-2 pulse 1 event.

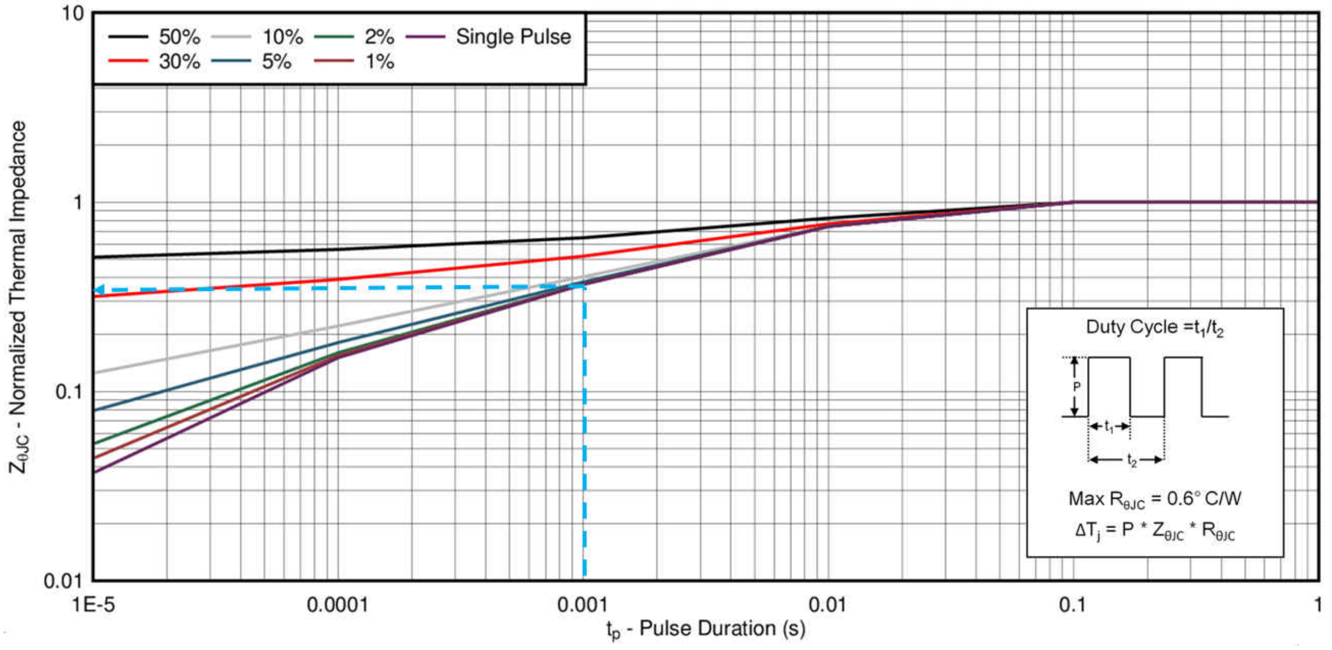


図 9-3. Typical MOSFET Transient Thermal Impedance

The maximum V_{GS} LM74701-Q1 can drive is 13.9 V, so a MOSFET with 15-V minimum V_{GS} rating must be selected.

Based on the design requirements and MOSFET selection criteria BUK7Y4R8-60E, SQJ460AEP, STL130N6F7 are some of the 60-V MOSFET options that can be selected.

9.2.2.3 Charge Pump VCAP (C_{VCAP}) and Input Capacitance (C_{IN})

Minimum required capacitance for charge pump VCAP and ANODE (input) is:

- VCAP: Minimum 0.1 µF is required; recommended value of VCAP (µF) ≥ 10 × $C_{ISS(MOSFET)}$ (µF)
- C_{IN}: Minimum 0.1 µF of input capacitance placed closed to ANODE pin to GND

9.2.2.4 Output Capacitance (C_{OUT})

LM74701-Q1 CATHODE pin is capable of handling negative voltage. However, if loads connected to LM74701-Q1 output are not capable of handling negative voltage, then sufficient output capacitor is required to ensure output does not swing negative during ISO7637-2 pulse 1 operation.

The required output capacitor during ISO7637-2 pulse 1 to ensure output does not swing negative can be calculated using 式 5.

$$C_{OUT} = (I_{LOAD} + I_{ISO\_AVG}) \times 1\ ms / \Delta V_{OUT} \quad (5)$$

Where ΔV_{OUT} is difference between output voltage at the start and the end of ISO7637-2 pulse 1.

9.2.3 Application Curves

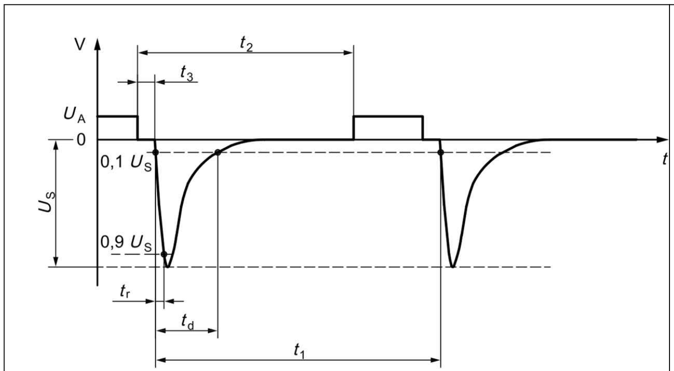
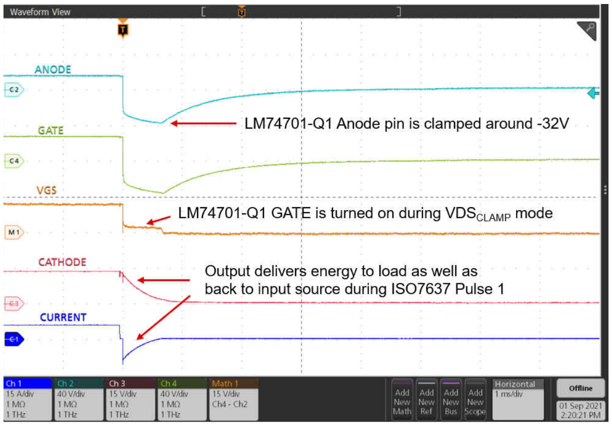


図 9-4. ISO 7637-2 Pulse 1



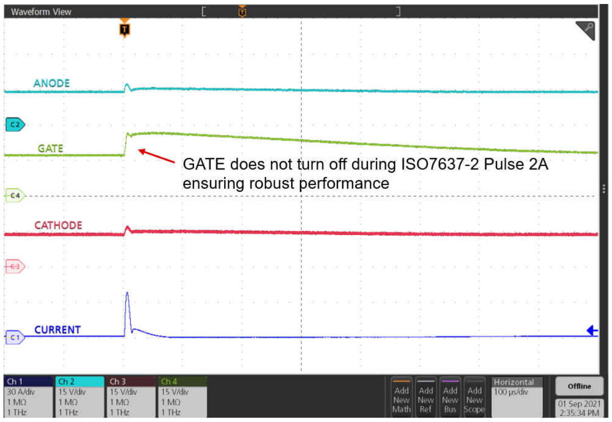
LM74701-Q1 Anode pin is clamped around -32V

LM74701-Q1 GATE is turned on during VDS_{CLAMP} mode

Output delivers energy to load as well as back to input source during ISO7637 Pulse 1

Time (1 ms/DIV)

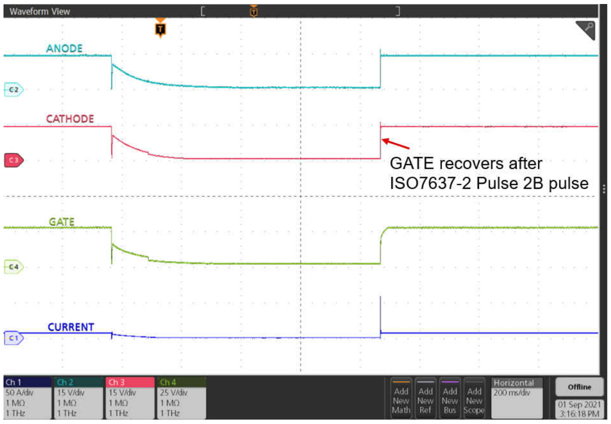
図 9-5. Response to ISO 7637-2 Pulse 1 (–100 V)



GATE does not turn off during ISO7637-2 Pulse 2A ensuring robust performance

Time (100 µs/DIV)

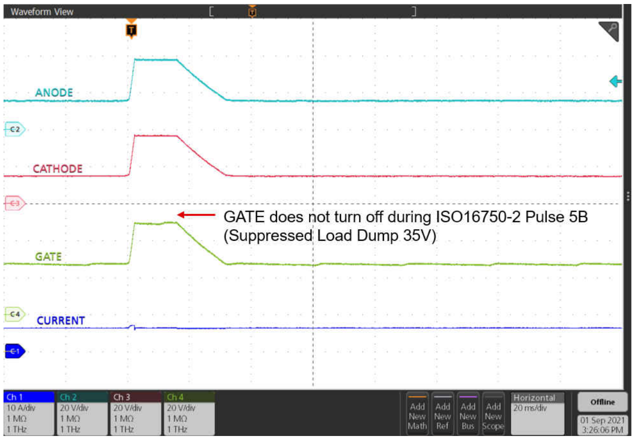
図 9-6. Response to ISO 7637-2 Pulse 2A (+112 V)



GATE recovers after ISO7637-2 Pulse 2B pulse

Time (200 ms/DIV)

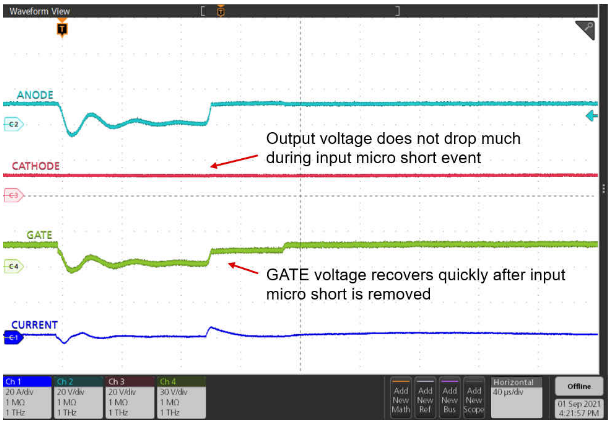
図 9-7. Response to ISO 7637-2 Pulse 2B



GATE does not turn off during ISO16750-2 Pulse 5B (Suppressed Load Dump 35V)

Time (20 ms/DIV)

図 9-8. Response to ISO 16750 Pulse 5B (35-V Suppressed Load Dump)

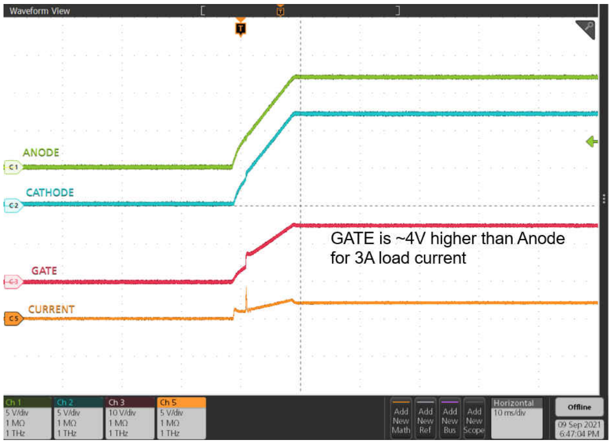


Output voltage does not drop much during input micro short event

GATE voltage recovers quickly after input micro short is removed

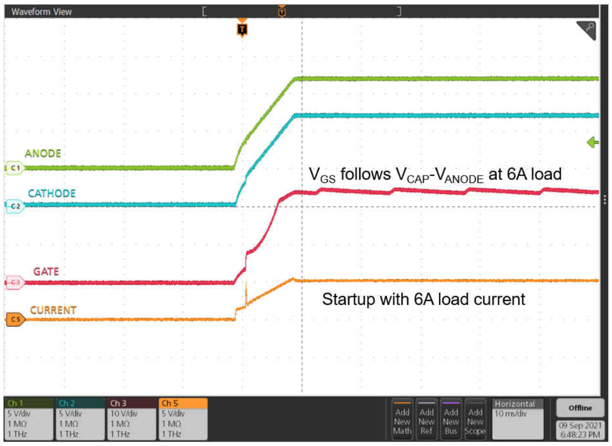
Time (40 µs/DIV)

図 9-9. Response to LV124 E-10 (Input Micro Short, 100 µs)



GATE is ~4V higher than Anode for 3A load current

図 9-10. Startup With 3-A Load



V_{GS} follows V_{CAP}-V_{ANODE} at 6A load

Startup with 6A load current

図 9-11. Startup With 6-A Load

9.3 What to Do and What Not to Do

- Place input decoupling capacitor (C_{IN}) close to ANODE pin.
- External MOSFET is used to dissipate transient energy in ISO7637-2 pulse 1 event. For the MOSFET with exposed thermal pad, make sure exposed thermal pad is in firm contact with PCB copper plane for efficient thermal transfer. Follow PCB layout and soldering guidelines mentioned in the MOSFET data sheet.

9.4 OR-ing Application Configuration

Basic redundant power architecture comprises of two or more voltage or power supply sources driving a single load. In its simplest form, the OR-ing solution for redundant power supplies consists of Schottky OR-ing diodes that protect the system against an input power supply fault condition. A diode OR-ing device provides effective and low cost solution with few components. However, the diodes forward voltage drops affects the efficiency of the system permanently, because each diode in an OR-ing application spends most of its time in forward conduction mode. These power losses increase the requirements for thermal management and allocated board space.

The LM74701-Q1 ICs combined with external N-Channel MOSFETs can be used in OR-ing Solution as shown in 図 9-12. The forward diode drop is reduced as the external N-Channel MOSFET is turned ON during normal operation. LM74701-Q1 quickly detects the reverse current, pulls down the MOSFET gate fast, leaving the body diode of the MOSFET to block the reverse current flow. An effective OR-ing solution must be extremely fast to limit the reverse current amount and duration. The LM74701-Q1 devices in OR-ing configuration constantly sense the voltage difference between Anode and Cathode pins, which are the voltage levels at the power sources (V_{IN1}, V_{IN2}) and the common load point respectively. The source to drain voltage VDS for each MOSFET is monitored by the Anode and Cathode pins of the LM74701-Q1. A fast comparator shuts down the gate drive through a fast pulldown within 0.45 µs (typical) as soon as $V_{(IN)} – V_{(OUT)}$ falls below –11 mV. The fast comparator turns on the Gate with 11 mA gate charge current after the differential forward voltage $V_{(IN)} – V_{(OUT)}$ exceeds 50 mV.

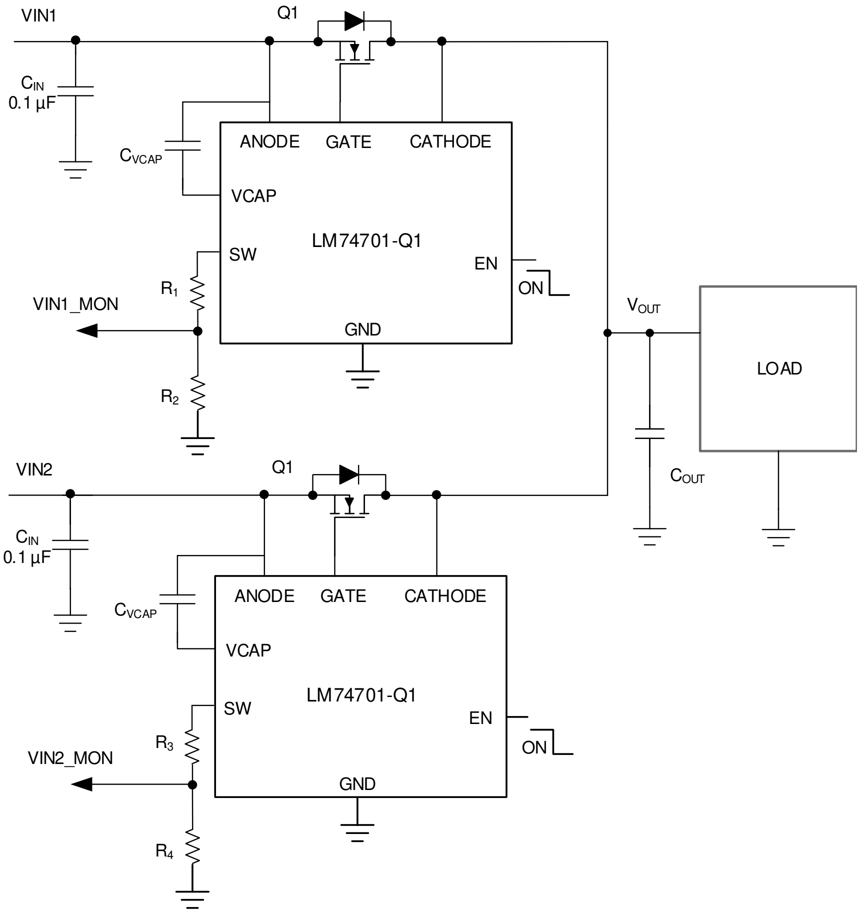


図 9-12. Typical OR-ing Application

図 9-13 to 図 9-16 show the smooth switch over between two power supply rails V_{IN1} at 12 V and V_{IN2} at 15 V. 図 9-17 and 図 9-18 illustrate the performance when V_{IN2} fails. LM74701-Q1 controlling V_{IN2} power rail turns off quickly, so that the output remains uninterrupted and V_{IN1} is protected from V_{IN2} failure.

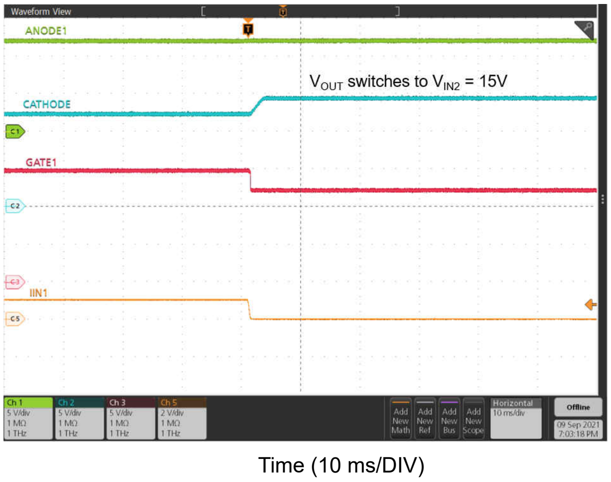


図 9-13. ORing V_{IN1} to V_{IN2} Switch Over

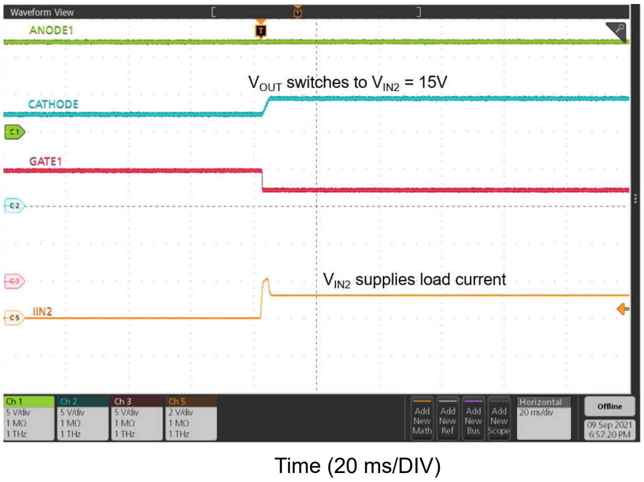


図 9-14. ORing V_{IN1} to V_{IN2} Switch Over

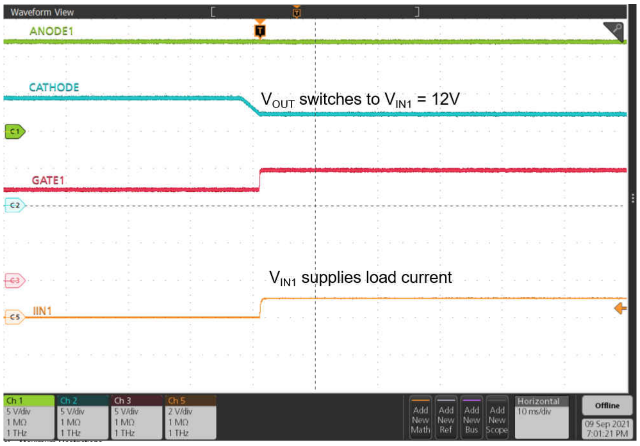


図 9-15. ORing V_{IN2} to V_{IN1} Switch Over

図 9-16. ORing V_{IN2} to V_{IN1} Switch Over

図 9-17. ORing - V_{IN2} Failure and Switch Over to V_{IN1}

図 9-18. ORing - V_{IN2} Failure and Switch Over to V_{IN1}

LM74701-Q1 has VDS clamp mode of operation where device detects the voltage difference between CATHODE and ANODE and turns on the external FET in active clamp region when the $V_{(OUT)} – V_{(IN)}$ *crosses the* VDS_{CLAMP} *threshold. So LM74701-Q1 can be used in ORing applications where worst case* $V_{(OUT)} – V_{(IN)}$ *is less than device* VDS_{CLAMP} *minimum specification as mentioned in the Electrical Characteristics table.*

10 Power Supply Recommendations

The LM74701-Q1 Ideal Diode Controller is designed for the supply voltage range of 3.2 V ≤ V_{ANODE} ≤ 65 V. If the input supply is located more than a few inches from the device, TI recommends an input ceramic bypass capacitor higher than 100 nF placed close to ANODE pin to GND. To prevent LM74701-Q1 and surrounding components from damage under the conditions of a direct output short circuit, use a power supply having over load and short circuit protection.

11 Layout

11.1 Layout Guidelines

- Place the input capacitor close to the ANODE pin to GND. Having smaller ground return path helps with better EMI performance.
- Connect ANODE, GATE and CATHODE pins of LM74701-Q1 close to the MOSFET's SOURCE, GATE and DRAIN pins.
- Use thick traces for source and drain of the MOSFET to minimize resistive losses. The high current path for this solution is through the MOSFET.
- Keep the charge pump capacitor across VCAP and ANODE pins away from the MOSFET to lower the thermal effects on the capacitance value.
- Connect the GATE pin of the LM74701-Q1 to the MOSFET gate with short trace. Avoid excessively thin and long trace to the Gate Drive.
- Keep the GATE pin close to the MOSFET to avoid increase in MOSFET turn-off delay due to trace resistance.

11.2 Layout Example

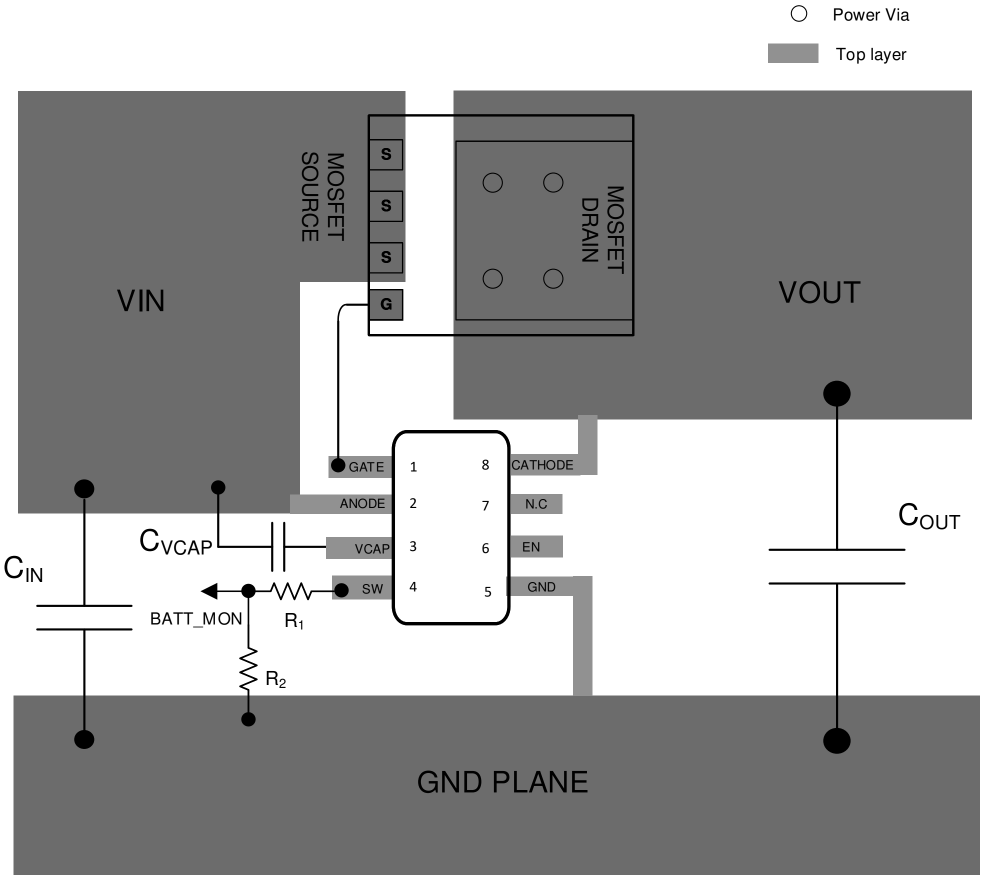


図 11-1. LM74701-Q1 Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 サポート・リソース

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM74701QDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LM701	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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