参考資料

TI Designs リファレンス・デザイン
ソリッド・ステート・リレー24V ACスイッチ、ガルバニック絶縁付

TI Designs リファレンス・デザイン

ソリッド・ステート・リレー24V ACスイッチのリファレンス・デザインは、単一リレーの代替として、標準的な電気機械式リレーに代わり、低消費電力で効率的な電力管理を可能にします。OFFモードではシステム・コントローラに電力を供給し、ONモードでは電気機械式リレーでは不可能な高速スイッチングを行い、バックアップ・バッテリの充電を可能にします。変圧器によって絶縁が可能になり、電圧マルチプライヤによりMOSFETを安全にオンにできる電圧が保証されます。

設計リソース

TIDA-00751	デザイン・フォルダ
CSD19537Q3	プロダクト・フォルダ
SN74LVC1G19	プロダクト・フォルダ
SN74AUP1G74	プロダクト・フォルダ
SN74AUP3G14	プロダクト・フォルダ
LMC555	プロダクト・フォルダ

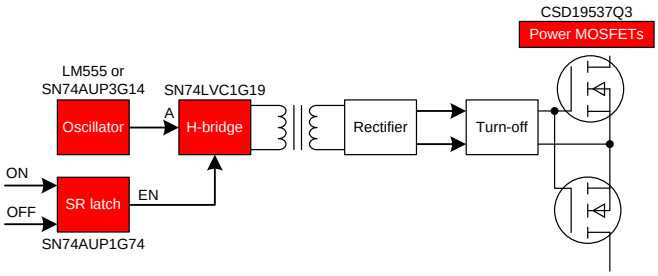
TI E2E™ Community　E2Eエキスパートに質問

デザインの特長

- 単一電気機械式リレーの代替
- 静音で低消費電力のソリッド・ステート・リレー
- クリック・ノイズなし
- オンおよびオフのスイッチング時間が1µs未満
- OFFモードでは、24V AC電源からシステムに電力を供給
- OFFモードでの消費電流が200µA未満
- 低いBOMコスト

主なアプリケーション

- ビルディング・オートメーション
- HVACシステム
- サーモスタット



1 主なシステム仕様

表 1. 主なシステム仕様

パラメータ	仕様	詳細
ロジック入力レベル範囲	3.3V	2.4
最大電源入力電圧	80V	2.1
電流範囲	2～6A_{RMS}	6.2
絶縁	変圧器(2500V AC)	3
オンおよびオフ時間	1µs未満	7.2
ON状態の消費電流	1.2mA	7.1
OFF状態の消費電流	200µA未満	4.4.1
動作温度範囲	-40℃～85℃	
動作環境	屋内設備用ビルディング・オートメーション	

2 システム概要

ソリッド・ステート・リレー(SSR)は電子的なスイッチング機器で、制御端子にわずかな外部電圧を印加することによってオン/オフを切り替えます。SSRは、機械部品を使用せず、適切な入力(制御信号)に応答する入力ロジック、負荷回路への電力を切り替えるソリッド・ステート・スイッチング・デバイス、制御信号によりこのスイッチを起動できるようにするカップリング機構で構成されます。SSRは、AC負荷とDC負荷のどちらの制御にも対応できます。電気機械式リレーと同じ機能を果たしますが、可動部品はありません。

SSRは、サイリスタやトランジスタなどの半導体パワー・デバイスを使用して、100アンペアまでの電流を切り替えることができます。SSRのスイッチング速度は電気機械式リレーよりも高速で、物理的な接点が存在しないため摩耗しません。SSRを適用する場合、瞬間的な過負荷への耐性が電気機械式の接点よりも低く、ON状態での抵抗が高いことを考慮する必要があります。電気機械式リレーとは異なり、SSRではスイッチングの配列が制限されています(単極単投のスイッチング)。

制御信号は、制御対象の回路に対して、2つの回路間でガルバニック絶縁を提供するような方法でカップリングする必要があります。SSRは、リード・リレー、変圧器、フォトカプラを使用してカップリング可能です。このデザインでは変圧器カップリングされたSSRを使用しており、絶縁バリアを超えて信号と電力を転送できるとともに、部品数、占有面積、コストを低く抑えることができます。

2.1 Nチャネル・パワーMOSFET

住居用や商業用のビルディング・オートメーションでは、標準の電源電圧として24V ACが使用されます。SSRをサーモスタット用途で機械式リレーの代替として使用する場合、電源スイッチの最大動作電圧は公称電圧の2倍になる可能性があります。入力電圧の変動と一時的な過電圧を考慮すると、公称24V AC電源のピーク電圧は42Vまで上昇する可能性があります。ワーストケースでは、電源スイッチが最高84Vで動作する可能性もあります。この理由から、この設計ではブレークダウン電圧が100VのパワーMOSFETを使用します。

2.2 入力制御ロジック

サーモスタット用途では、消費電力が主要な懸念事項の1つになります。長いバッテリ寿命を保証するため、制御ロジック(多くの場合、専用のマイクロコントローラを使用)は、低電力またはスリープモードに移行する前の短時間に制御信号を供給します。オン信号とオフ信号は2つの別個の信号で、短時間のみアクティブになります。この理由から、入力制御ロジックではテキサス・インスツルメンツ製の低消費電力AUPシングルゲートSRラッチであるSN74AUP1G74を使用します。この回路は、短いONパルスで出力ENABLE信号(アクティブLOW)をセットし、短いOFF信号により信号をリセットします。

2.3 発振器

このTI Designでは、2つの発振器回路を使用します。コストを重視する用途では、シュミットトリガ・インバータ・ゲートを使用して回路を設計します。2番目の回路はLM555を使用し、消費電力を重視する用途向けに設計されています。どちらの回路も、パワーMOSFETをオンにするために使用する300kHz信号を生成します。サーモスタットの中には、複数の機械式リレーが使用されているものがあります。これらの用途では、信号形式の単一の発振器回路を複数のSSRに対して使用できるため、この置き換えによってコストと消費電力が削減できます。

2.4 デコーダとデマルチプレクサ

デコーダおよびデマルチプレクサ・デバイスとして、SN74LVC1G19を選択しました。このリファレンス・デザインでは、デマルチプレクサにより、変圧器の一次側で高周波の方形波が必要ない場合、発振器の出力信号をオフにできます。デマルチプレクサはHブリッジとしても機能し、3.3V電源からAC方形波信号を生成します。SN74LVC1G19を選択したのは、入力電圧範囲が最高5Vと広く、3.3Vで±24mAの出力を駆動できるためです。このリファレンス・デザインのドライバでは、Hブリッジから変圧器を駆動するために4mAの最大出力が必要です。この部品は長期間の稼動に耐えられる十分な堅牢性を備えています。また、他の選択理由として、短い伝搬遅延、活線挿抜、部分パワーダウン・モード、そして最も重要な点としてバック・ドライブ保護が搭載されていることがあります。

3 Block Diagram

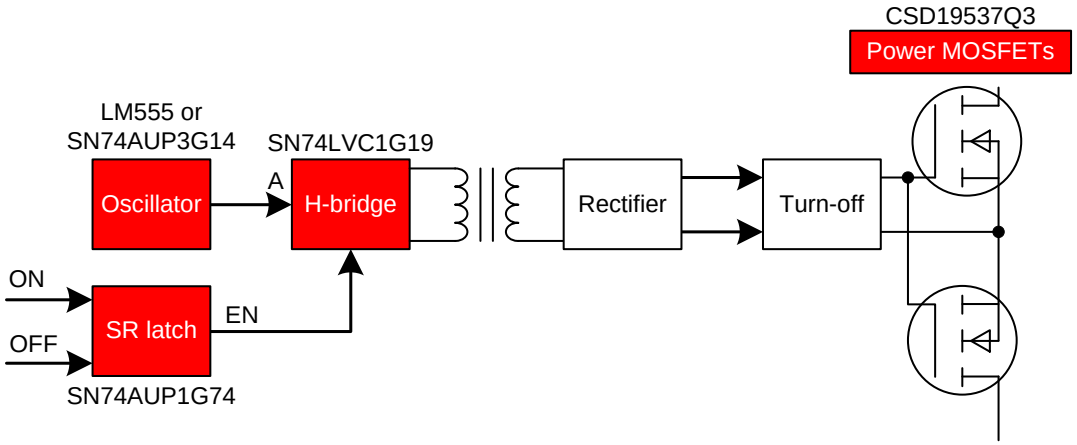


図 1. TIDA-00751 Block Diagram

3.1 Highlighted Products

The solid state relay reference design features the following devices:

- CSD19537Q3: 100-V N-channel NexFET power MOSFET
- SN74LVC1G19: 1-of-2 decoder and demultiplexer
- SN74AUP3G14: Schmitt-trigger inverter gate
- LM555: Low-power CMOS timer
- SN74AUP1G74: Single positive-edge-triggered D flip-flop

3.1.1 CSD19537Q3

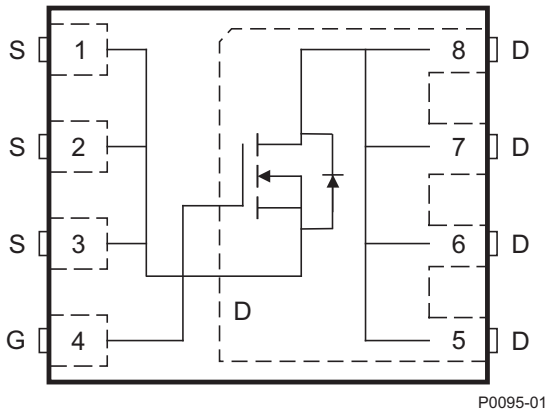


図 2. CSD19537Q3 Block Diagram (Top View)

Features:

- Ultra-low Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Pb-free terminal plating
- RoHS compliant
- Halogen free
- SON 3.3×3.3-mm plastic package

3.1.2 SN74LVC1G19

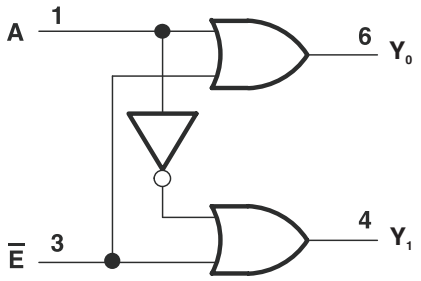


図 3. SN74LVC1G19 Functional Block Diagram

Features:

- Available in the Texas Instruments NanoFree™ package
- Supports 5-V V_{CC} operation
- Inputs accept voltages to 5.5 V
- Supports down translation to V_{CC}
- Maximum t_{pd} of 4 ns at 3.3 V
- Low power consumption, 10-µA maximum I_{CC}
- ±24-mA output drive at 3.3 V
- V_{OLP} (output ground bounce) < 0.8 V typical at V_{CC} = 3.3 V, T_A = 25°C
- V_{OHV} (output V_{OH} undershoot) >2 V typical at V_{CC} = 3.3 V, T_A = 25°C
- I_{OFF} supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000-V human-body model (A114-A)
  - 200-V machine model (A115-A)
  - 1000-V charged-device model (C101)

3.1.3 SN74AUP3G14

表 2. Function Table

INPUT	OUTPUT
A	Y
High	Low
Low	High

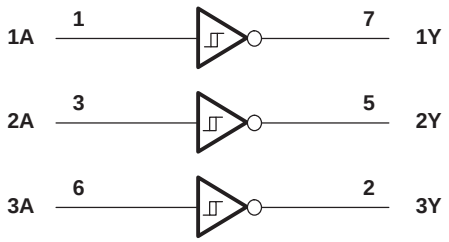


図 4. SN74AUP3G14 Logic Diagram (Positive Logic)

Features:

- Available in the Texas Instruments NanoStar™ package
- Low static-power consumption (I_{CC} = 0.9 μA maximum)
- Low dynamic-power consumption (C_{PD} = 4.3 pF typical at 3.3 V)
- Low input capacitance (C_I = 1.5 pF typical)
- Low noise: overshoot and undershoot <10% of V_{CC}
- I_{OFF} supports partial-power-down mode operation
- Wide operating V_{CC} range of 0.8 to 3.6 V
- Optimized for 3.3-V operation
- 3.6-V I/O tolerant to support mixed-mode signal operation
- t_{PD} = 4.3 ns maximum at 3.3 V
- Suitable for point-to-point applications
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance tested per JESD 22:
  - 2000-V human-body model (A114-B, Class II)
  - 1000-V charged-device model (C101)

3.1.4 LMC555

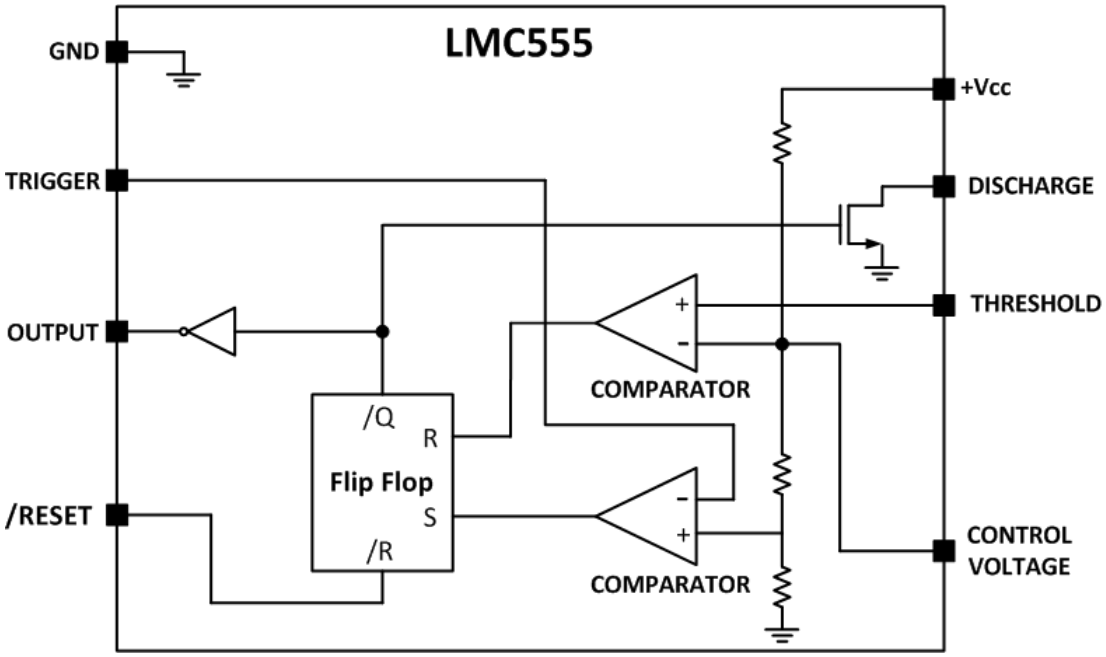


図 5. LMC555 Functional Block Diagram

Features:

- Less than 1-mW typical power dissipation at 5-V supply
- 3-MHz astable frequency capability
- 1.5-V supply operating voltage ensured
- Output fully compatible with TTL and CMOS logic at 5-V supply
- Tested to −10-mA, 50-mA output current levels
- Reduced supply current spikes during output transitions
- Extremely low reset, trigger, and threshold currents
- Excellent temperature stability
- Pin-for-pin compatible with 555 series of timers
- Available in 8-pin VSSOP package and 8-bump DSBGA package

3.1.5 SN74AUP1G74

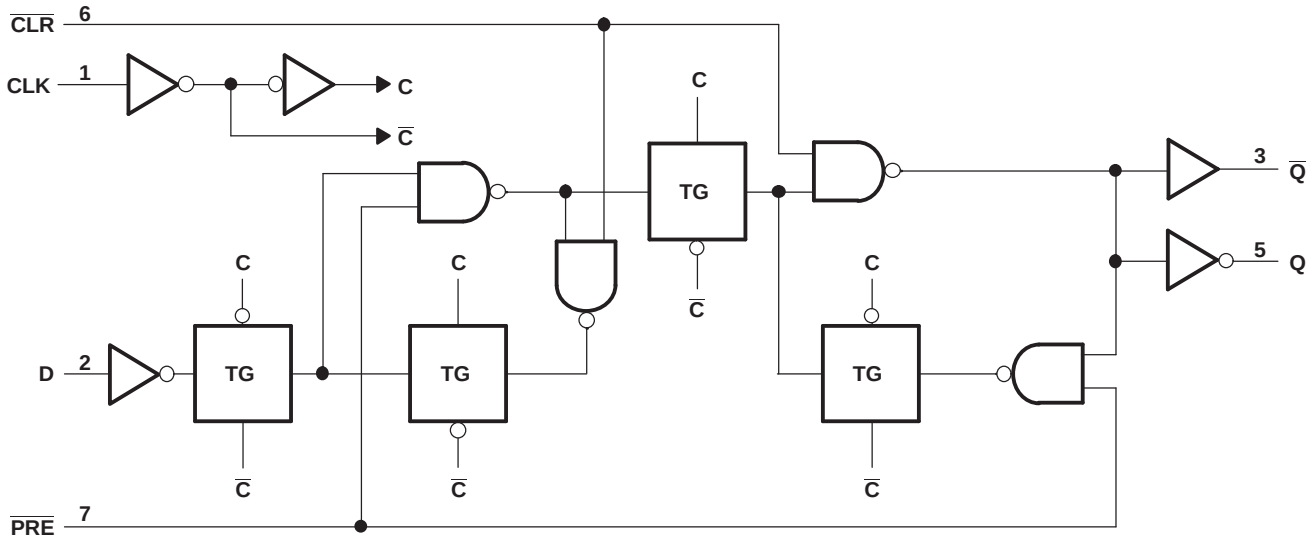


図 6. SN74AUP1G74 Functional Block Diagram

Features:

- Available in the Texas Instruments NanoStar package
- Low static-power consumption: I_{CC} = 0.9 μA maximum
- Low dynamic-power consumption: C_{pd} = 5.5 pF typical at 3.3 V
- Low input capacitance: C_i = 1.5 pF typical
- Low noise: overshoot and undershoot < 10% of V_{CC}
- I_{OFF} supports partial-power-down mode operation
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the input (V_{HYS} = 250 mV typical at 3.3 V)
- Wide operating V_{CC} range of 0.8 to 3.6 V
- Optimized for 3.3-V operation
- 3.6-V I/O tolerant to support mixed-mode signal operation
- t_{PD} = 5 ns maximum at 3.3 V
- Suitable for point-to-point applications
- Latch-up performance exceeds 100 mA per JESD 78, Class II
- ESD performance tested per JESD 22
  - 2000-V human-body model (A114-B, Class II)
  - 1000-V charged-device model (C101)

4 System Design Theory

4.1 Basic SSR Theory

SSRs are integrated electrical circuits that act as a mechanical switch. SSRs have no moving parts, hence the device name. The relays can be switched much faster and are not prone to wear because of the absence of moving parts. Another advantage is that less current and voltage is needed for SSRs to control high-voltage AC loads.

Electric isolation is still achieved in SSRs as with other electromechanical relays. Both SSRs and electromechanical relays use two different circuits: a control circuit and a separate circuit for switching the load. Transformers or optocouplers are used to isolate the control side from the high-voltage switching side of the relay. This reference design implements isolation with a transformer.

4.2 Power Management Theory

The solid state relay 24-V AC switch reference design power is used to charge either the battery or capacitor the thermostat runs off of. A normal wiring of such a system in shown in 図 7. In order to charge the battery or capacitor from the 24-V AC line, a bridge rectifier turns the AC signal into a DC voltage.

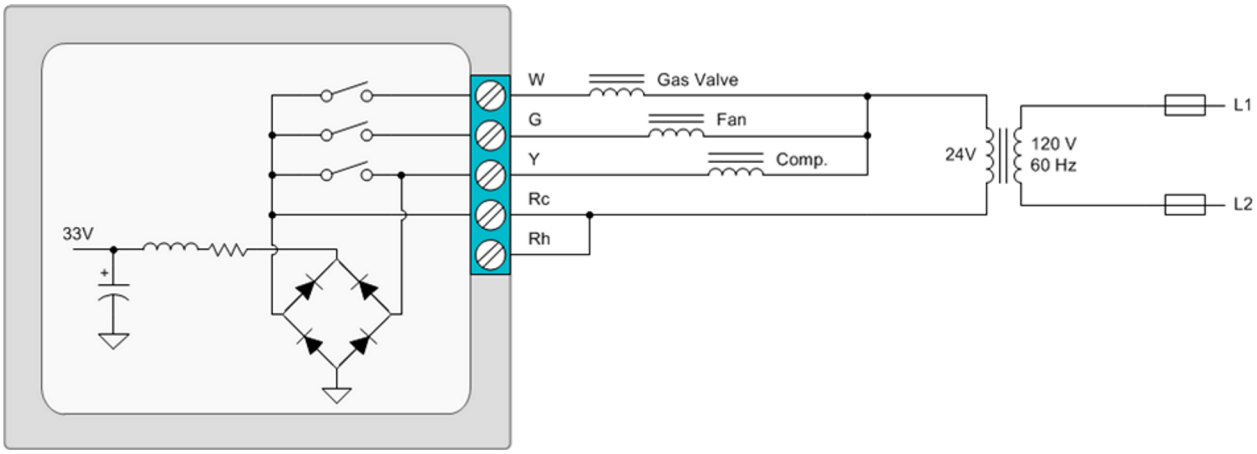


図 7. Standard Wiring of Thermostat

The rectifier allows charging of the battery or capacitor when the low-voltage relay is open, or when the HVAC system is not powering the gas valve, fan, or compressor. The high-voltage electromechanical relay that switches on each of the main high-voltage systems is controlled by the low-voltage relay. 図 8 shows the charging of the battery during HVAC inactive mode.

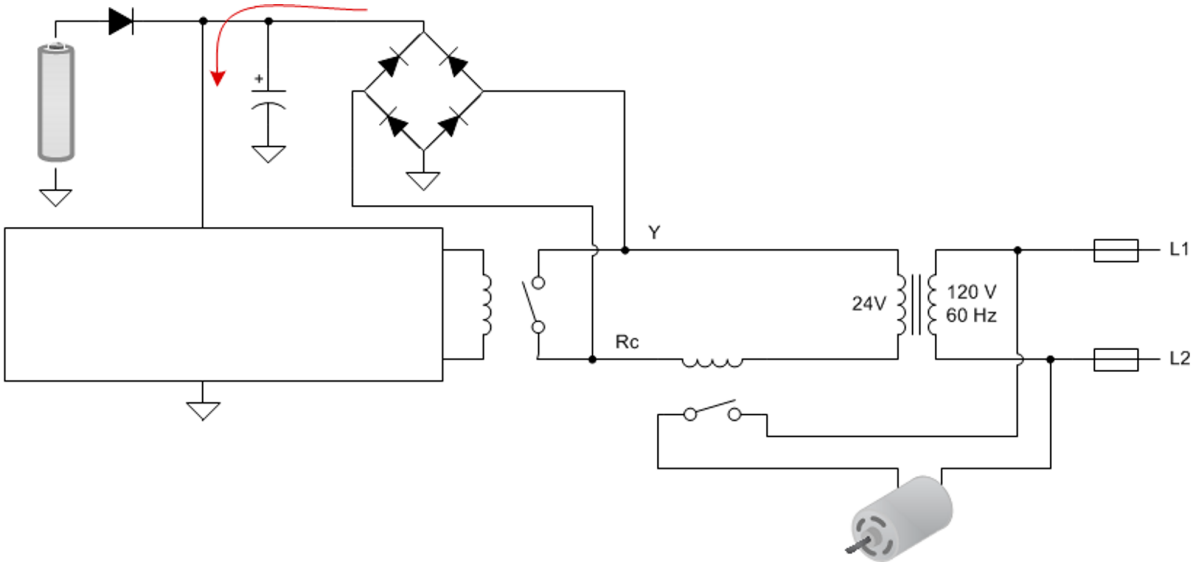


図 8. Battery Charging During HVAC Inactive Mode

During active heating and cooling the thermostat must be powered off of the battery. The circuit configuration during active mode is shown in 図 9.

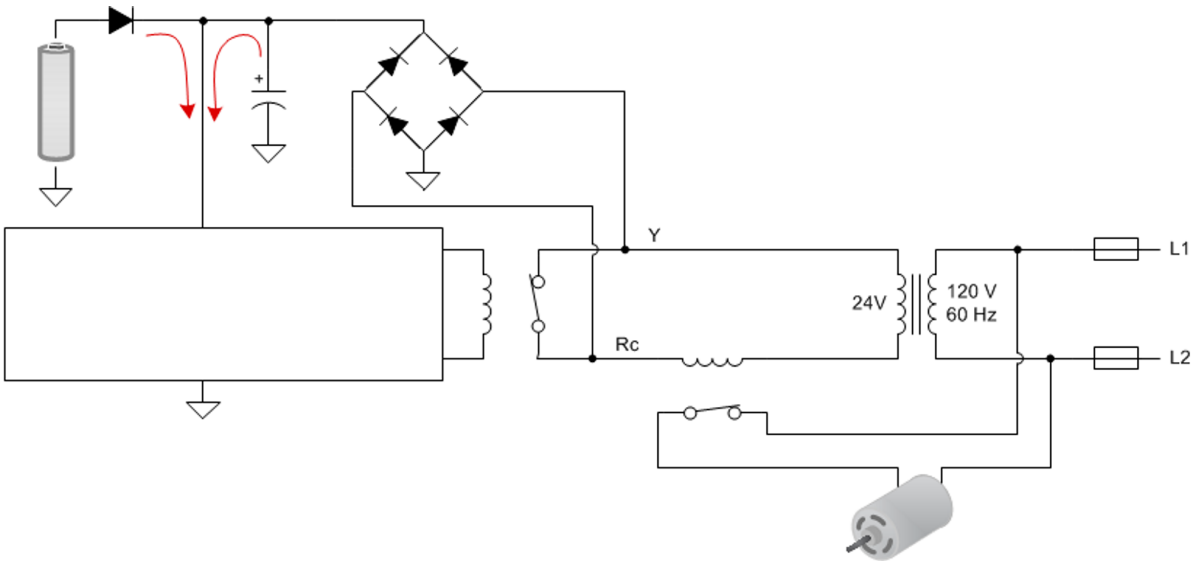


図 9. HVAC Active Mode, Thermostat Running off Battery

An adjustment to the power implementation must be made if the battery or capacitor is not large enough to power the control board during a long active mode heating or cooling. By quickly turning off and on the low-voltage relay, a charge can be added to the battery while in "active" mode. Using an SSR in place of the low-voltage electromechanical switch is one way to accomplish the active mode power management. The SSR switch much faster than the electromechanical relays. The switching frequency of the SSR must be high enough to not interrupt the power to the heater, fan, or compressor.

4.3 MOSFET Selection

When SSR is used to turn on and off inductive load, take care to limit overvoltage spikes during the turn-off process. In some thermostat applications where the load power supply also provides additional power to the thermostat, a rectifier bridge and a capacitor will act as snubber circuit absorbing energy from inductive load during turn off. When this circuit is missing from the application, an additional transient voltage suppression (TVS) diode needs to be added. For the DC application unidirectional TVS is sufficient, where for AC application a bidirectional TVS is needed.

4.4 Oscillator Design Theory

The oscillator circuitry generates a 3.3-V, 50% duty cycle square wave that is fed into the H-bridge. Two astable multivibrator circuits are included in this reference design for the implementation of the oscillator function. The first circuit uses the LMC555 timer to implement a low supply current oscillator version. The second circuit uses the SN74AUP3G14 Schmitt-trigger inverter to implement a low-cost oscillator version. The design of these oscillator circuits are discussed in the following sections. The H-bridge design is discussed in the next section of this document.

4.4.1 Timer-Based Oscillator Design

The timer-based oscillator design uses a modified oscillator topology based on the 555 timer circuit. The modification compared to traditional implementations uses the output signal to charge and discharge the timing capacitor instead of using the discharge output of the timer circuit. This modification forces the charge and discharge current to flow through a single resistor, thereby producing a 50% duty cycle oscillator output. A simplified schematic of this oscillator circuit is shown in 図 10.

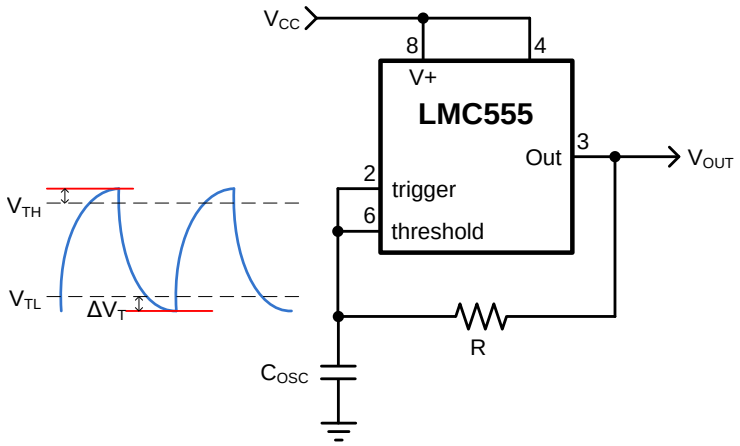


図 10. LMC555 Timer-Based Oscillator Schematic

Based on the capacitor voltage waveform shown in 図 10, the following equations can be used to describe the behavior of the circuit and to make adjustments to the component values. As shown in the waveform, the propagation delay of the timer circuit needs to be taken into account to accurately predict the output frequency and supply current. The finite propagation delay causes the capacitor voltage to be larger than what is predicted by the DC thresholds of the timing circuit. Because of this, there is additional charge that needs to be added or removed before reaching the next threshold. This additional charge or discharge time plus the finite prop delay adds to the time needed to complete each oscillator half cycle.

The excess voltage is given by the following:

$$V_{EXTRA} = V_{CC}\left(1 - e^{\frac{-t_{PD}}{RC}}\right) \cong \frac{t_{PD}}{RC} \times V_{CC}, \quad \text{since } e^{\frac{-t_{PD}}{RC}} \approx 1 - \frac{t_{PD}}{RC} \tag{1}$$

with RC >> t_{PD}

With the excess voltage defined, the charge and discharge times and therefore the output frequency is given by the following:

$$t_D = -RC\left(\ln\frac{V_{TL}}{V_{CC}} - \ln\frac{V_{INIT}}{V_{CC}}\right) + t_{PD} = -RC\left[\ln\frac{1}{3} - \ln\left(\frac{2}{3} + \frac{t_{PD}}{RC}\right)\right] + t_{PD} = RC\left[\ln\left(2 + \frac{3 \times t_{PD}}{RC}\right)\right] + t_{PD} \tag{2}$$

$$t_C = -RC\left[\ln\left(1 - \frac{V_{TH}}{V_{CC}}\right) - \ln\left(1 - \frac{V_{INIT}}{V_{CC}}\right)\right] + t_{PD} = -RC\left[\ln\left(\frac{1}{3}\right) - \ln\left(\frac{2}{3} + \frac{t_{PD}}{RC}\right)\right] + t_{PD}$$

$$= RC\left[\ln\left(2 + \frac{3 \times t_{PD}}{RC}\right)\right] + t_{PD} \tag{3}$$

$$T_{OSC} = t_C + t_D = 2\left\{R \times \left(C_{OSC} + C_{IN}\right)\left[\ln\left(2 + \frac{3 \times t_{PD}}{R\left(C_{OSC} + C_{IN}\right)}\right)\right] + t_{PD}\right\}, \quad f_{OSC} = \frac{1}{T_{OSC}} \tag{4}$$

Using typical datasheet values of 100 ns for t_{PD}, thresholds of $V_{CC}/3$ and $2V_{CC}/3$ for V_{TL} and V_{TH}, respectively, a measured nominal value of 15 pF for C_{IN}, and a nominal value of 100 pF for C_{OSC}, the value of the resistor needed to produce an output frequency of 300 kHz as an example is 17.83 kΩ, or 17.8k in a 1% standard value resistor. Because the output frequency is dependent on timer circuit parameters, which will vary from part to part, it may be necessary to adjust the resistor value slightly if the output frequency needs to have a tight tolerance across multiple boards. Also note that observing 式 4, assuming a negligible timer circuit propagation delay, will yield the more commonly quoted equation for astable operation of the timer circuit, which is:

$$f_{OSC} = \frac{1}{2 \times 0.693 \times R \times C_{OSC}} \tag{5}$$

Making use of this analysis, the equation for power supply current is derived as follows:

$$I_{CC} = I_Q + C_T \times V_{OSC} \times f_{OSC} + C_{PD} \times V_{CC} \times f_{OSC} = I_Q + \left(C_{OSC} + C_{IN}\right)\left[\frac{t_{PD}}{R\left(C_{OSC} + C_{IN}\right)} \times V_{CC} + \frac{V_{CC}}{3}\right] \times f_{OSC} + C_{PD} \times V_{CC} \times f_{OSC}$$

$$= I_Q + V_{CC} \times f_{OSC}\left[\frac{t_{PD}}{R} + \frac{\left(C_{OSC} + C_{IN}\right)}{3} + C_{PD}\right] \tag{6}$$

The variables I_Q and t_{PD} can be taken directly from the LMC555 datasheet for the timer circuit and are 80 µA and 100 ns typical, respectively. The input capacitance, C_{IN}, was measured to be ~15 pF on average for a small sample size. The internal dynamic switching current of the timer circuit power supply is not given in the datasheet but can be approximated, and represented as Cpd in equation 6, from measured supply current data over multiple frequencies with a fixed power supply voltage. The resulting value of C_{PD} is estimated to be ~55 pF. 図 11 shows the measured supply current compared to the calculated data using 式 6.

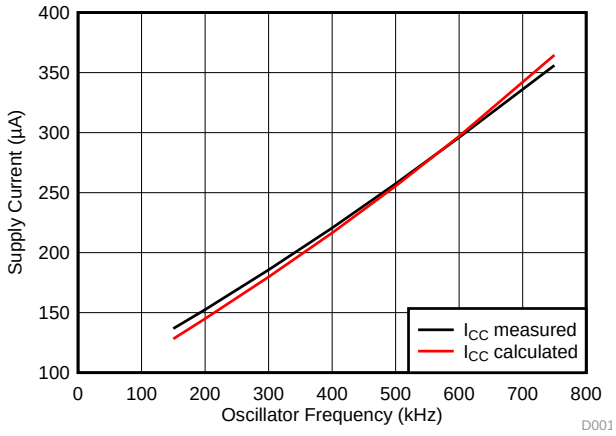


図 11. LMC555 Timer-Based Oscillator Supply Current Comparison

For more information on C_{PD} and calculating power dissipation in CMOS logic circuits, please see *CMOS Power Consumption and Cpd Calculation* (SCAA035).

4.4.2 Schmitt-Trigger Inverter-Based Oscillator Design

The inverter-based oscillator design uses a ring-of-three astable multivibrator architecture. A simplified schematic of this oscillator circuit is shown in 図 12.

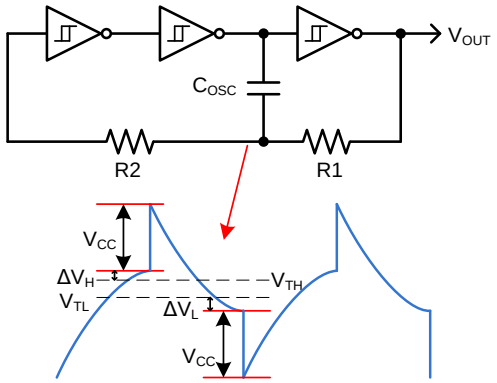


図 12. Schmitt-Trigger Inverter-Based Oscillator Schematic

There are inverter-based oscillator designs that only require two inverters; however, these architectures are known to have problems with startup when using small values of C_{OSC}. Using the smallest possible value of C_{OSC} in this circuit is important in minimizing the supply current because of the large voltage appearing across this capacitor. The lower limit for the value of C_{OSC} should be the constraint that C_{OSC} is much greater than the sum of the parasitic and stray capacitances which are present in the circuit in the absence of C_{OSC}. The resistor R2 is added to limit voltage excursions above and below the supply rails at the input of the first inverter. Depending on the oscillator frequency and stray capacitance across R2, there is still a possibility that the voltage at the input of the first inverter can exceed the supply rails, in which case R2 will also serve to limit the parasitic current to prevent damage to the inverter IC. Schmitt-trigger devices are preferred in this architecture because the input to the first inverter can have slow transitions. Use of Schmitt-trigger devices will prevent large shoot-through currents in the first stage as well as providing robustness to coupled noise by providing hysteresis in the switching threshold voltage.

Based on the capacitor voltage waveform shown in 図 12, the following equations can be used to describe the behavior of the circuit and to make adjustments to the component values. As shown in the waveform, the propagation delay of the inverters and of the R2, C_{IN} combination need to be taken into account in order to accurately predict the output frequency and supply current. The finite propagation delay causes the capacitor voltage to be larger than what is predicted by the DC thresholds of the Schmitt-trigger inverters and because of this, there is additional charge that needs to be added or removed before reaching the next threshold. This additional charge or discharge time plus the finite prop delay adds to the time needed to complete each oscillator half cycle. Further complicating the analysis of this circuit is the fact that C_{IN} is non-linear with input voltage. The non-linearity of this capacitance has been approximated for this analysis as will be described in this section. More importantly, depending on the value chosen for R2, this capacitance will cause a difference in the excess voltage on charge and discharge cycles; this ultimately leads to a duty cycle that is not the ideal 50% that is expected. The excess voltages are given by the following:

$$\Delta V_H = V_{CC}\left(1 - e^{\frac{-\left(t_{del} + 0.693 \times R2 \times C_{IN\_CH}\right)}{R1 \times C_{OSC}}}\right) \tag{7}$$

$$\Delta V_L = \left(V_{CC} + V_{TH} + \Delta V_H\right)\left(1 - e^{\frac{-\left(t_{del} + 0.693 \times R2 \times C_{IN\_CL}\right)}{R1 \times C_{OSC}}}\right) \tag{8}$$

The variable t_{del} is the sum of the propagation delays due to the first two inverter stages and was measured to be ~12 ns in this design. The variable V_{TH} is the positive going trip point taken from the datasheet for the Schmitt-trigger inverters. The input capacitance estimate based on voltage measurements in the circuit are C_{IN_CH} ~ 2.39 pF and C_{IN_CL} ~ 1.42 pF. With the excess voltage defined, the charge and discharge times, and therefore the output frequency, is given by the following:

$$t_D = -R1 \times C_{OSC} \times \ln\left(\frac{V_{TL} - \Delta V_L}{V_{CC} + V_{TH} + \Delta V_H}\right) = R1 \times C_{OSC} \times \ln\left(\frac{V_{CC} + V_{TH} + \Delta V_H}{V_{TL} - \Delta V_L}\right) \tag{9}$$

$$t_C = -R1 \times C_{OSC}\left[\ln\left(1 - \frac{V_{TH} + \Delta V_H}{V_{CC}}\right) - \ln\left(1 - \frac{V_{TL} - \Delta V_L - V_{CC}}{V_{CC}}\right)\right] = R1 \times C_{OSC}\left[\ln\left(\frac{2 \times V_{CC} - V_{TL} + \Delta V_L}{V_{CC} - V_{TH} - \Delta V_H}\right)\right] \tag{10}$$

$$T_{OSC} = t_C + t_D = R1 \times C_{OSC}\left[\ln\left(\frac{2 \times V_{CC} - V_{TL} + \Delta V_L}{V_{CC} - V_{TH} - \Delta V_H}\right) + \ln\left(\frac{V_{CC} + V_{TH} + \Delta V_H}{V_{TL} - \Delta V_L}\right)\right]$$

$$= R1 \times C_{OSC} \times \ln\left[\left(\frac{2 \times V_{CC} - V_{TL} + \Delta V_L}{V_{CC} - V_{TH} - \Delta V_H}\right)\left(\frac{V_{CC} + V_{TH} + \Delta V_H}{V_{TL} - \Delta V_L}\right)\right], \quad f_{OSC} = \frac{1}{T_{OSC}} \tag{11}$$

The variable V_{TL} is the negative going trip point taken from the datasheet for the Schmitt-trigger inverters. Observing the previous equations, there are a couple of important points to be considered. First, ΔV_L will be larger than ΔV_H. Secondly, in applying this point to equation 11, the denominator of the second term in the natural log function is at risk of going to zero for frequencies where the sum of the circuit delays and the delay due to the combination of R2, C_{IN} becomes a large percentage of the intended delay due to R1 and C_{OSC}. In reality, the oscillator capacitor will discharge to a value equal to the C_{IN} discharge current

times R2 and remain at that level until the lower threshold of the input inverter is reached. While this behavior is not comprehended by these equations, the saturation of the output frequency for a fixed value of R2 is reached at frequencies much lower than the frequency where the predicted ΔV_L approaches V_{TL}. Along this same line of reasoning, R2 will ultimately limit the upper frequency of the oscillator. This is correctly predicted by the above equations, albeit erring on the conservative side.

In order to limit the effect of the non-linear C_{IN} and to achieve a duty cycle that is as close as possible to 50% while still providing a reasonable limit to parasitic currents due to voltage excursions exceeding the supply rails at the input of the first inverter, this design chose to make R1 and R2 equal. Using 式 11, the value of R1 can be calculated for a 300-kHz operating frequency using the following values for the other variables: V_{TL} = 1 V, V_{TH} = 2 V, C_{OSC} = 100 pF, t_{del} = 12 ns, C_{IN_CH} = 2.39 pF, C_{IN_CL} = 1.42 pF, and V_{CC} = 3.3 V. This results in the following calculated values: f_{OSC} = 300.146 kHz, R1 = R2 = 9.9 kΩ.

Making use of this analysis, the equation for power supply current is derived as follows:

$$I_{CC} = I_Q + 3C_{PD} \times V_{CC} \times f_{OSC} + V_{CC} \times f_{OSC} \sum C_L + C_{OSC} \times V_{CC} \times f_{OSC} + I_{PARA}$$
$$= I_Q + f_{OSC}\left[V_{CC}\left(3C_{PD} + \sum C_L\right) + C_{OSC} \times V_{OSC}\right] + I_{PARA} \quad (12)$$

where $V_{OSC} = 2V_{CC} + [V_{TH} + \Delta V_H - (V_{TL} - \Delta V_L)]$

The variables I_Q and C_{PD} can be taken directly from the datasheet for the Schmitt-trigger inverters and are 0.9 μA and 4.5 pF typical, respectively. The ΣC_L term represents the sum of the capacitances found on the internal nodes of the oscillator circuit. For the input capacitance, an average of the C_{IN_CH} and C_{IN_CL} values is used for this calculation and is ~2 pF. The output capacitance is shown in the inverter datasheet to be 3 pF typical. In this analysis, an additional 2 pF was included to account for stray capacitances at the output nodes, with an additional 5 pF estimated for the inverter node connected to C_{OSC}. Capacitance measurements were performed on a standalone PCB to confirm these estimates. Referring to 図 12, moving from left to right through the inverter string, ΣC_L = 2 pF + 7 pF + 12 pF + 5 pF ≈ 26 pF. I_{PARA} is an error term that is independent of frequency. The exact source of I_{PARA} was not thoroughly investigated as part of this reference design, but it is suspected that this term is due to a combination of shoot-through current in the inverters along with voltage spikes appearing at the oscillator output, which exceed the supply rails at the state transitions due to coupling from the summing junction (node connecting R1, R2, and C_{OSC}) through the stray capacitance of R1. The value of this current is derived to be ~84 μA. 図 13 shows the measured supply current compared to the calculated data using 式 12.

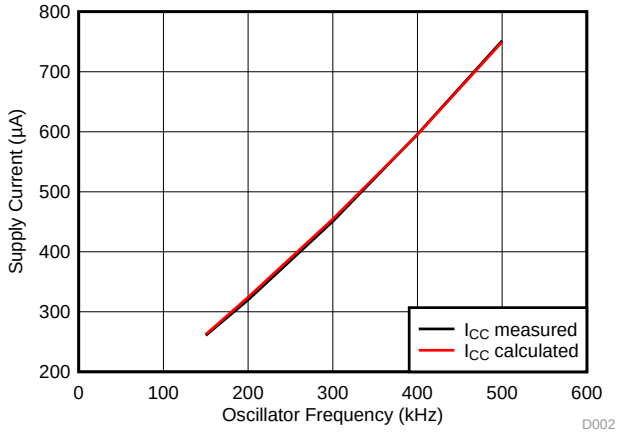


図 13. Schmitt-Trigger Inverter-Based Oscillator Supply Current Comparison

4.5 H-Bridge Design

When a 3.3-V square wave is put on the input of the H-bridge, the H-bridge outputs an AC signal. This 3.3-V AC signal drives the primary side of the transformer, enabling the transformer to operate. The SN74LVC1G19 is rated for approximately a 24-mA maximum output and gives enough robustness because the expected output peak current is 4 mA.

The SN74LVC1G19 is actually a demultiplexer, but it also works as an H-bridge. The device "decodes" the bit on input A and places a logic low on the matching address output, Y_0 or Y_1, when the enable pin ($\overline{E}$) is pulled low. The each output pin toggles (0 and 3.3 V) out of phase from each other when a square wave signal is input on the input 'A' pin of the SN74LVC part. 表 3 demonstrates what is happening at logic level.

表 3. H-Bridge Logic Table

INPUTS		OUTPUTS	
$\overline{E}$	A	Y_0	Y_1
Low	Low	Low	High
Low	High	High	Low
High	X	High	High

This part is ideal for driving the transformer because of its high-current output capability.

4.6 Choosing a Transformer

The transformer serves multiple purposes in the SSR reference design; it is used for electrical isolation and as a voltage multiplier. To ensure the power MOSFETs are in saturation at least 6.0 V is required. With only 3.3 V on the primary side of the transformer more voltage is required on the secondary side. Therefore, a higher secondary turn ratio is preferred on the transformer. This reference design’s transformer has a turns ratio of 1:3.2. With a turn ratio of 3.2, the transformer outputs approximately 10 V on the secondary side when 3.3-V AC is applied on primary. When the power MOSFETs are in saturation there will be plenty of current to turn on the high-voltage electromechanical relays.

A suitable transformer for this type of design requires the ability to operate at high frequencies with low current losses. Low losses are key to enable direct switching between older electromechanical relays and a newer SSR because the electromechanical relays do not use much current. The losses can be adjusted by trying different transformer cores and controlling leakage flux.

5 Getting Started Hardware

5.1 Board Overview

For ease of use, all of the components, jumpers, and test points are located on the top side of the board. The signal chain starts on the left side of the board and moves to the right side of the board in a linear fashion. The terminal block (J3) located on the left edge of the board has connection points for the 3.3-V supply voltage and ground. Moving right, the first jumper (J1) selects which oscillator receives the supply voltage, and the next jumper (J2) selects which oscillator output is sent to the H-bridge. Colored test points denote signal chain test points and black test points are for ground connections.

図 14. TIDA-00751 Reference Design Hardware

The control signal pins are located just below the leftmost terminal block.

A visible blank area in the ground fill can be seen in the middle of the board. The blank area is adds to the isolated properties of this design. The transformer is the only component that connects the two different ground planes or each side of the design, which are primary and secondary sides of the transformer.

5.2 Operating the Circuit

When the board is first powered on, the oscillator that is selected with the jumpers will start oscillating and the H-bridge will be enabled, allowing the power MOSFETs to turn on. To turn off MOSFETs, a short OFF pulse is sent. Since both inputs are active low and have pullup resistors, the pulse must pull down the signal to logic zero. The simplest way to do this is to short the pin to ground for a short time. The same method goes for the ON signal, shorting the #ON pin to ground will turn on the power MOSFETs.

6 Test Setup

The transformer's primary and secondary sides of the circuit are tested separately and the test setup for each are outlined in this section.

6.1 Primary Side Functional Test Setup

Two independent power supplies were needed for testing: one supply to power the 3.3-V rail and another to be a high-power load that the MOSFETs could control. A power supply that can source 3 A and drive at least 27 V at the same time was used as the load that the power MOSFETs were controlling. The secondary side of the transformer was connected to a constant 24-V, 3-A load at terminal block J5. A TVS diode was also inserted between the load connection points as a safety measure.

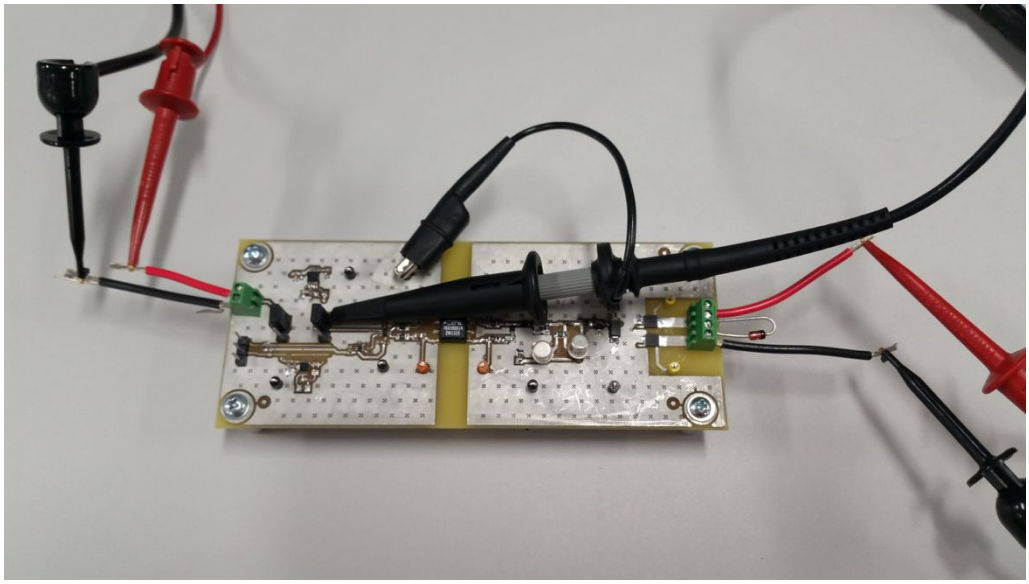


図 15. Prototype With Probes and Power Supplies Connected

In 図 15, the oscilloscope probe is set up to probe the output of Oscillator 1, and the TVS diode is connected between the load connection points. Header J2 has output pins for both oscillators, making probing easy.

To create the high-power load, a BK precision high-current DC regulated power supply is in series with a resistor decade box rated for 5 A was connected across the terminal block J5. The test setup with the power supplies, decade box, and temperature chamber is shown in 図 16. The high-current power supply has the decade box connected to the positive terminal and the output of the decade box is the new positive terminal of the high-power load, the output is seen running into the temperature chamber in 図 16.

図 16. Primary Side Functional Test Setup

Inside the temperature chamber, each power connection has its own independent positive and negative connections.

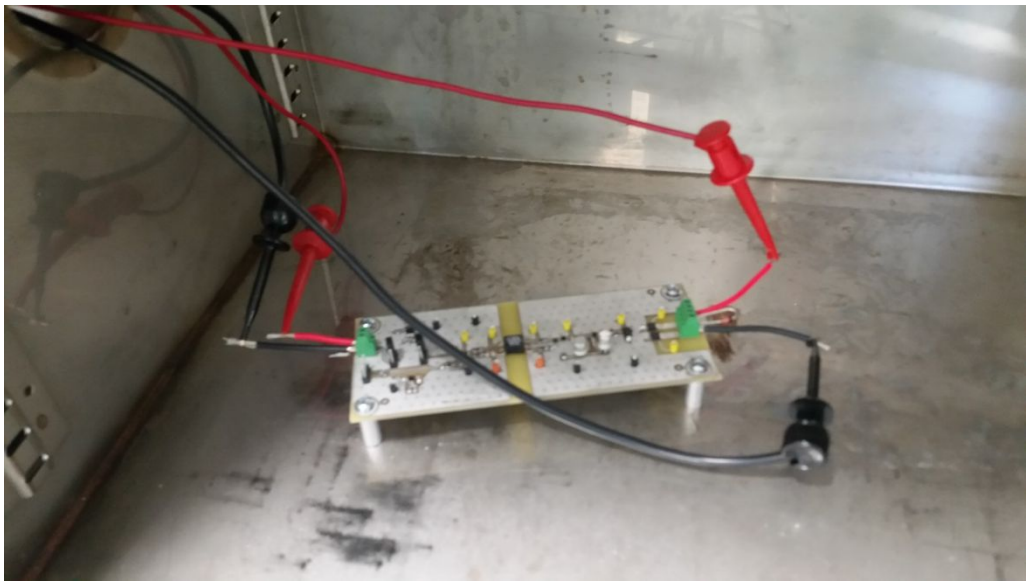


図 17. Inside Temperature Chamber

6.2 Transformer Secondary Side Test Setup

The secondary side test is to collect data of the amount of time for the turn on and off signal to propagate through the control circuit and to get waveform captures. The setup includes connecting power supplies as done in the primary side test, with one supply for the 3.3-V rail and the other high-power supply to act as the load supply. For this test, the power load was set to approximately 34 V with a current of 3.1 A. The temperature chamber was not used for this round of testing. 図 18 shows the connection points of several probe locations used to collect data.

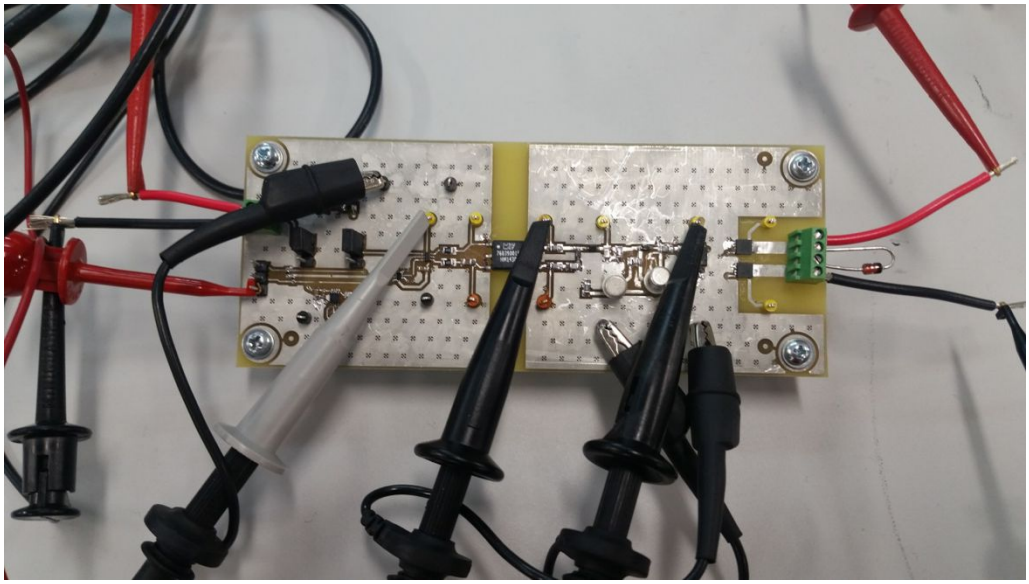


図 18. Probe Connections for Signal Chain Waveforms

To toggle the system on, the "#on" pin on jumper J4 was grounded, and grounding "#OFF" on J4 turns off the oscillator output, thus turning off the power MOSFETs.

7 Test Data

The transformer's primary and secondary sides of the circuit are tested separately, and the results are outlined in this section.

7.1 Primary Side Temperature Functional Test

This test varied temperature and supply voltage to characterize the supply current and oscillator frequency. The secondary side was connected to a constant 28-V, 3-A load.

表 4. Oscillator and H-Bridge Temperature Functional Test

PARAMETER	TEMP 1 (0°C)			TEMP 2 (25°C)			TEMP 3 (50°C)		
	3 V	3.3 V	3.6 V	3 V	3.3 V	3.6 V	3 V	3.3 V	3.6 V
I_{CC}1 (OC1) mA	1.501	1.68	1.857	1.249	1.395	1.543	1.432	1.606	1.777
Freq (OC1) kHz	305.2	308.1	310.4	300.4	303.4	305.8	296.1	299	301.6
I_{CC}2 (OC2) mA	1.666	1.871	2.089	1.422	1.588	1.768	1.576	1.774	1.969
Freq (OC2) kHz	290.6	287.3	284.5	291.7	288.6	285.6	292.7	289.3	286.3

Both oscillators operating current react in a similar way to changing temperature and supply voltage, which is to be expected. The temperature on the outer ends of the temperature spectrum does increase the operating current as seen in 図 19. This could be because the passive component values have shifted slightly due to temperature.

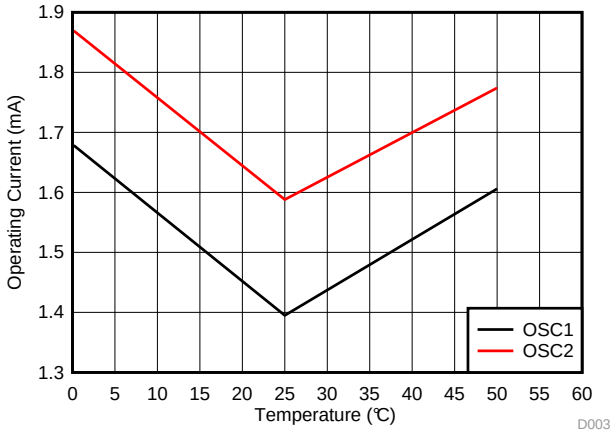


図 19. Operating Current versus Temperature

As the supply voltage increases, so does the supply current, which is to be expected. The results are shown in 図 20.

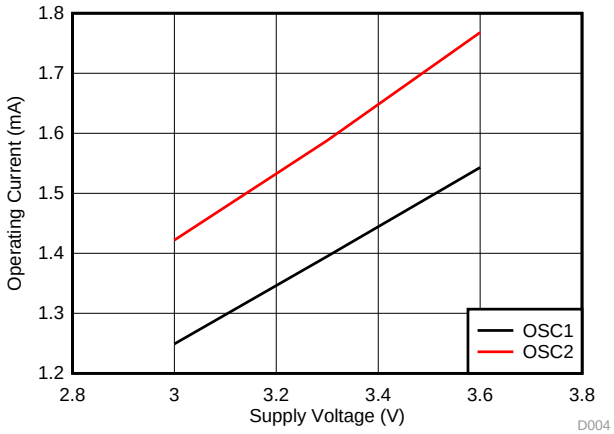


図 20. Operating Current versus Supply Voltage

The oscillator using the LM555 timer varies more over temperature than the cheaper alternative oscillator made with the triple Schmitt-trigger inverter. The following graphs show oscillator frequency in reaction to varying temperature and supply voltage.

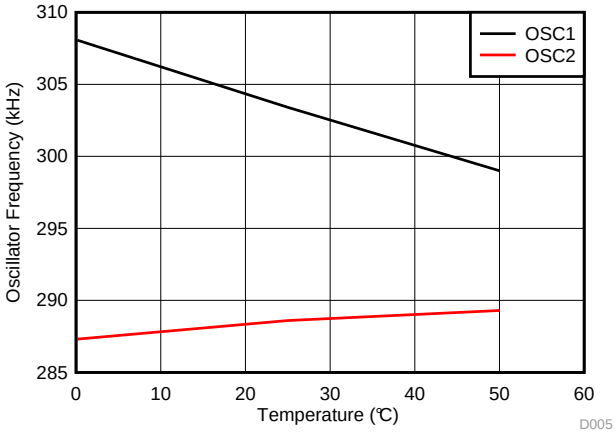


図 21. Oscillator Frequency versus Temperature

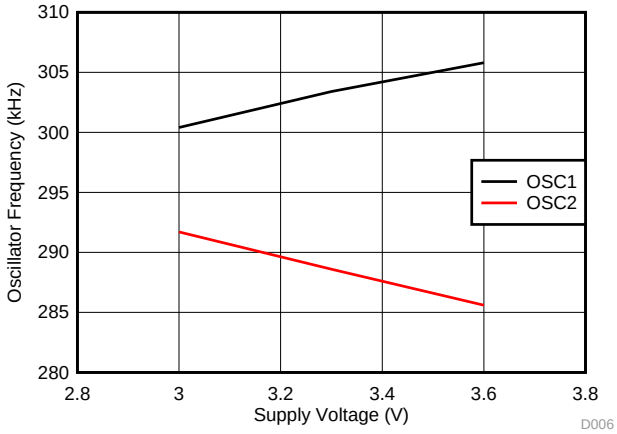


図 22. Oscillator Frequency versus Supply Voltage

7.2 Secondary Side Test

The first waveform capture is of enable signal at test point 10 (TP10), H-bridge output (TP7), and gate voltage on output (TP6). The H-bridge output is the result of the 300-kHz signal from the oscillator and the H-bridge device. The gate voltage ramps up to about 11.4 V before evening out.

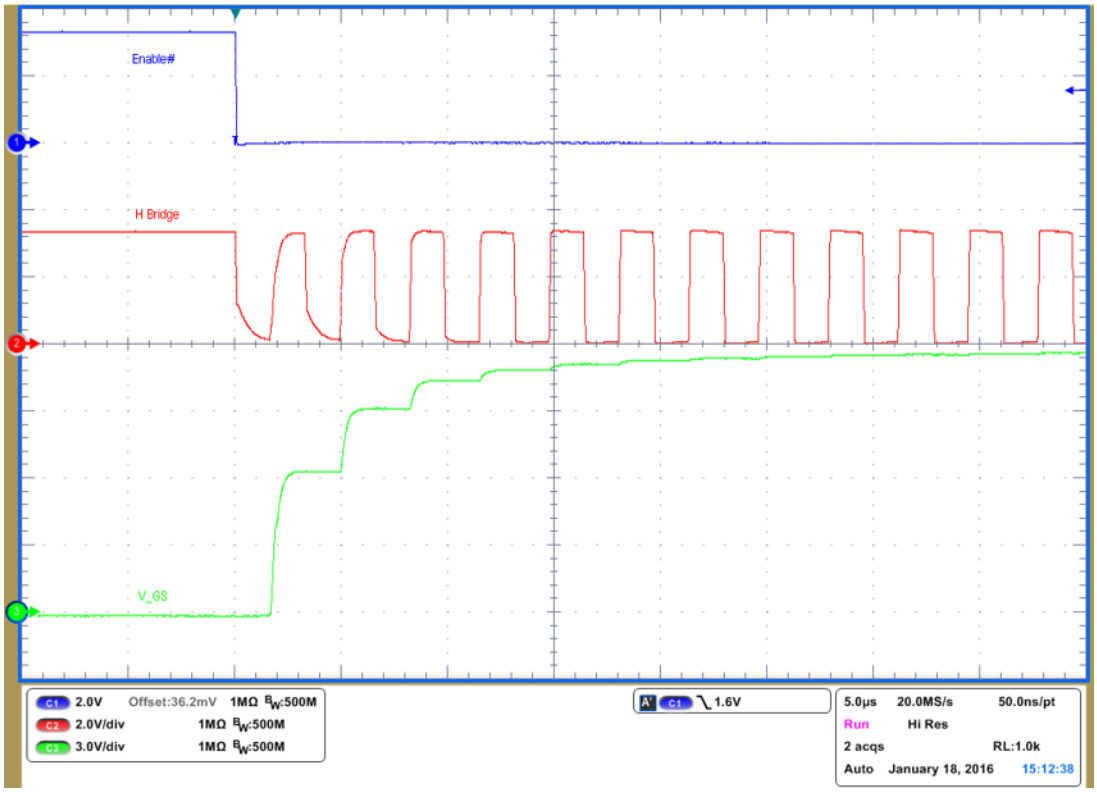


図 23. Gate Voltage Ramp-up

The next waveform collected demonstrates the propagation time of the signal (T_{delay}). The approximate time from "enable" dropping low to voltage of drain source dropping to zero. V_{DS} is the voltage difference between TP2 and TP13 (V_{GS} = TP6 – TP13). The approximate “on” delay time is ~2 µs. The actual time to turn on the MOSFET, is T_{ON} = ~100 ns as seen in 図 24. This is the time between V_{DS} starting to drop and load current, I_D, starting to ramp up. The load current waveform was also captured and can be seen in 図 24.

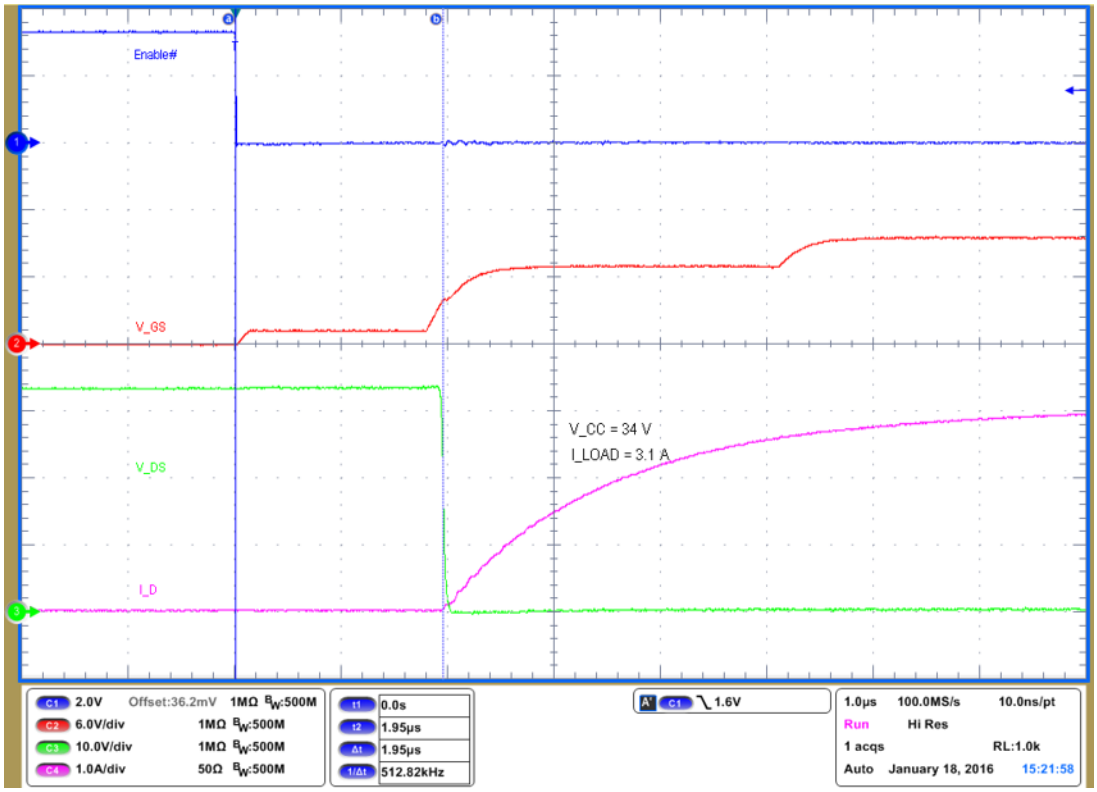


図 24. ON Delay Time Waveforms

The turn-off delay is also important in power control systems. Waveforms during turn-off were collected in the same fashion as the turn-on signals. Enable (T10), V_{GS} = TP6 – TP13, V_{DS} = TP2 – TP13. I_D was measured with a current probe on load wire connected to J5. The "off" delay time is around 5.5 µs. The time to turn off MOSFET, is T_{OFF} = 200 ns. The extra voltage spike and ripple on V_{DS} is caused by the TVS diode installed across the terminal block J5 for protection during testing. The TVS diode also makes the load current drop slower. See 図 25 for waveforms of T_{OFF} and off delay time.

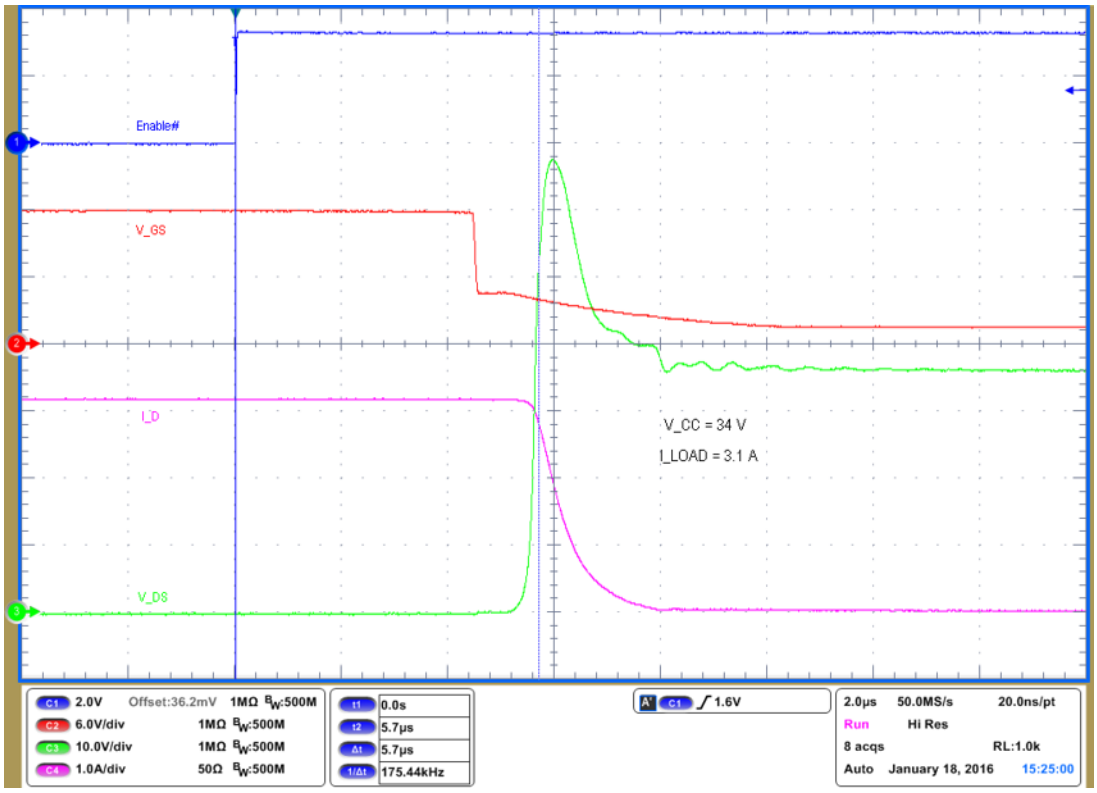


図 25. OFF Delay Time Waveforms

7.3 Summary

To sum up the results of testing, at room temperature the reference design uses approximately 1.4 mA with Oscillator 1 running at 300 kHz and a supply voltage of 3.3 V. T_{ON} is around 100 ns with a propagation delay of about 2 µs. T_{OFF} is around 200 ns with a propagation delay of about 5.5 µs.

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-00751.

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00751.

8.3 PCB Layout Recommendations

A careful PCB layout is critical and extremely important in a high-current fast-switching circuit to provide appropriate device operation and design robustness. As with all switching power supplies, pay attention to detail in the layout to save time in troubleshooting later on. Also, keep grounds separate.

8.3.1 Layout Prints

To download the layout prints, see the design files at TIDA-00751.

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00751.

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00751.

8.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00751.

9 References

1. Texas Instruments, *Noise Analysis in Operational Amplifier Circuits*, Application Report (SLVA043)
2. Texas Instruments, *CMOS Power Consumption and Cpd Calculation*, Application Report (SCAA035)
3. Texas Instruments, WEBENCH® Design Center, http://www.ti.com/webench

9.1 商標

10 About the Author

JARROD KREBS is a systems designer at Texas Instruments, where he is responsible for developing reference designs in the industrial segment. Jarrod has experience with software and embedded applications implemented on ARM-based microcontrollers and TI's MSP430 platforms. Jarrod earned his bachelor of science in computer engineering from Kansas State University in Manhattan, KS. Jarrod is also a member of the Institute of Electrical and Electronics Engineers (IEEE).

DAVID STOUT is a systems designer at Texas Instruments, where he is responsible for developing reference designs in the industrial segment. David has over 18 years of experience designing analog, mixed-signal, and RF ICs with more than 14 years focused on products for the industrial semiconductor market. David earned his bachelor of science in electrical engineering (BSEE) degree from Louisiana State University, Baton Rouge, Louisiana and a master of science in electrical engineering (MSEE) degree from the University of Texas at Dallas, Richardson, Texas.

リビジョンBの改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (February 2016) から **Revision B** に変更 **Page**

- 特長に「クリック・ノイズなし」を 追加 1
- 一般的な「高速」を具体的な「1µs未満」に 変更 1
- 「消費電力ゼロ」を「200µA未満」に 変更 1
- 表 1に詳細の列を 追加 2
- 2500V AC測定を 追加 2
- 表 1にオンおよびオフ時間の行を 追加 2
- 表 1にOFF状態の消費電流の行を 追加 2

リビジョンAの改訂履歴

2015年12月 発行のものから更新 **Page**

- プレビュー・ページから 変更 1

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お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、あるいはTIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

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お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

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