参考資料

TI Designs
3相インバータ・システム用の絶縁型IGBTゲート・ドライバの評価プラットフォーム

TEXAS INSTRUMENTS

TI Designs リファレンス・デザイン

このリファレンス・デザインは、22kWの出力段と、AC駆動などの各種アプリケーションの3相インバータを意図したTIの新しい強化絶縁型IGBTゲート・ドライバであるISO5852Sで構成されています。このデザインを使用すると、電流定格50A～200Aおよび電圧定格1200VのIGBTモジュールで構成された3相インバータ内のISO5852Sの性能を評価することができます。評価の対象として重要ないくつかの機能と性能は、DESATを使用した短絡保護、ソフト・シャットダウン、インバータのさまざまなdv/dtに対するアクティブ・ミラー・クランプの効果、調整可能な速度の電力駆動システム（IEC61800-3）から導き出したシステム・レベルにおけるIGBTゲート・ドライバのESD/EFT性能です。インバータの制御に必要なPWM信号を生成するには、Piccolo LaunchPad であるLAUNCHXL-F28027を使用します。

設計リソース

TIDA-00195	デザイン・フォルダ
ISO5852S	プロダクト・フォルダ
AMC1200	プロダクト・フォルダ
SN6501	プロダクト・フォルダ
UCC27211	プロダクト・フォルダ
CSD88537ND	プロダクト・フォルダ
TPS54286	プロダクト・フォルダ
LP38691	プロダクト・フォルダ
SN74ALVC125	プロダクト・フォルダ

TI E2E™ Community

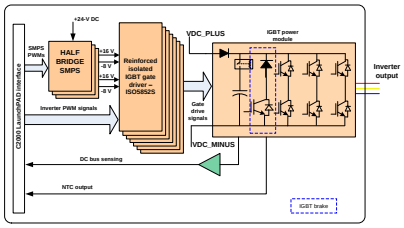
E2Eエキスパートに質問
WEBENCH®設計支援ツール

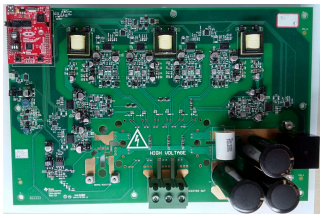
デザインの特長

- 3相インバータ・システムの特性:
  - 電圧定格が1200Vで電流定格が50A～200AのIGBTモジュール(複数ベンダをサポート)
  - 7個の強化絶縁型IGBTゲート・ドライバ: 動作時の絶縁耐圧が1.5kV$_{RMS}$で最小CMTIが50kV/µsのISO5852S
- 以下の機能を使用する、過電流と誤検出によるターンオンの保護機能を内蔵:
  - DESAT検出
  - ソフト・シャットダウン
  - アクティブ・ミラー・クランプ
- IEC61800-3のEMC耐性要件に適合:
  - ±8kV ESD CD (IEC 61000-4-2)
  - ±4kV EFT (IEC 61000-4-4)
- ゲート・ドライバ用の+16V/-8Vを生成するオンボード・ハーフ・ブリッジ絶縁型電源で、外部BJT（バイポーラ・トランジスタ）/MOSFETバッファを使用し、ユニポーラまたはバイポーラ電源をゲート・ドライバに供給
- ゲート・ドライバの入力は、反転/非反転動作用に構成することが可能
- システム評価用のオプション:
  - ゲート・ドライバ/IGBT間を接続するツイスト・ペア・ケーブル
  - ゲート/エミッタ間に接続する外部静電容量

主なアプリケーション

- 産業用可変速ドライブ
- サーボ・ドライブ
- 太陽光インバータ
- UPS





1 Introduction to IGBT Gate Drivers

Insulated gate bipolar transistors (IGBTs) are considerably used in 3-phase inverters that have numerous applications like variable-frequency drives that control the speed of AC motors, uninterruptible power supply, solar inverters, and other similar inverter applications.

IGBTs have the advantages of high input impedance as the gate is insulated, has a rapid response ability, good thermal stability, simple driving circuit, good ability to withstand high voltage, snubber-less operation, and controllability of switching behavior providing reliable short-circuit protection. The IGBT is a voltage-controlled device, which gives it the ability to turn ON/OFF very quickly.

A typical application of a three-phase inverter using six isolated gate drivers is shown in 図 1. Note that each phase uses a high-side and a low-side IGBT switch to apply positive and negative high-voltage DC pulses to the motor coils in an alternating mode.

The output voltage to the motor is controlled by pulse-width modulation (PWM). PWM is accomplished by turning the transistor on and off several times. The output voltage is an average of the peak or maximum voltage and the amount of time the transistor is turned on or off.

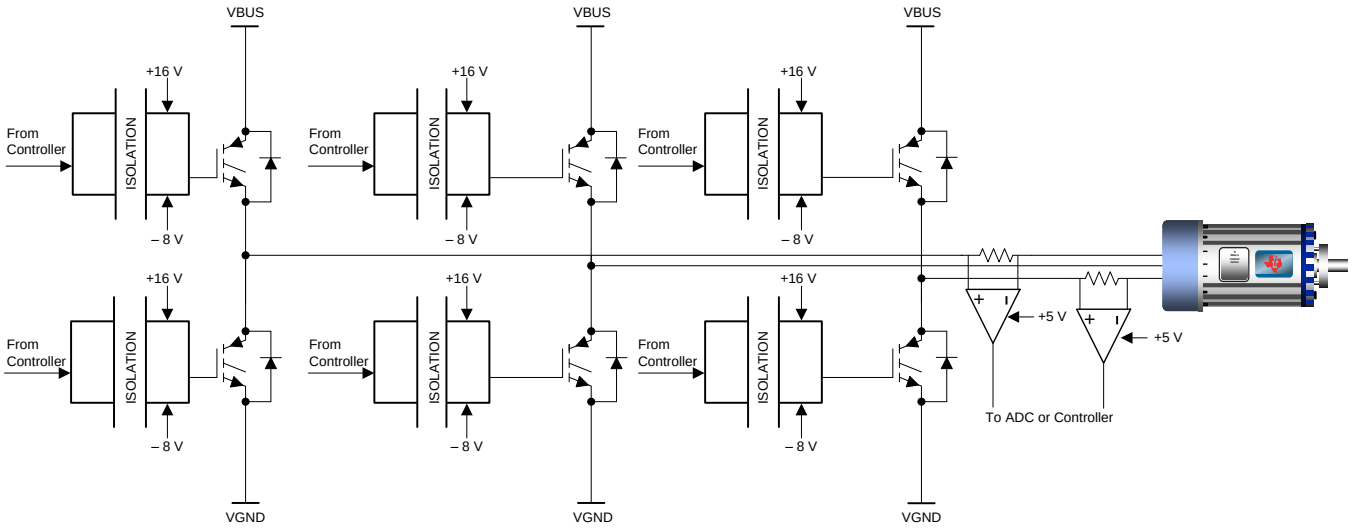


図 1. 3-Phase Inverter With Isolated Gate Drive

The ISO5852S is a reinforced isolated IGBT gate driver from TI intended for use in applications such as motor control, industrial inverters, switched-mode power supplies, and so on. In these applications, sophisticated PWM control signals are required to turn the power-devices on and off, which at the system level eventually may determine, for example, the speed, position, and torque of the motor or the output voltage, frequency, and phase of the inverter. These control signals are usually the outputs of a microcontroller (MCU), and are at low-voltage levels such as 3.3 or 5.0 V. The gate controls required by the IGBTs, on the other hand, are in the range of 15 to 20 V, and need high current capability to be able to drive the large capacitive loads offered by those power transistors. Also, the gate drive needs to be applied with reference to the emitter of the IGBT and by inverter construction, the emitter node of top IGBT swings between 0 to the DC bus voltage, which is several hundreds of volts in magnitude. As the IGBT can float with respect to ground at the power stage, both the power supply and the gate circuitry should be isolated from the inverter ground. This gives room to a limited number of gate-driver configurations:

- Gate drivers with potential separation
- Gate drivers without potential separation

The ISO5852S belongs to a family of gate drivers with potential separation and can level shift the incoming 3.3-V and 5.0-V control signals from the microcontroller to the 15-V to 20-V drive required by IGBT while ensuring high-voltage isolation between the driver side and the MCU side.

This reference design consists of a 22-kW power stage with TI's reinforced isolated gate drivers ISO5852S intended to drive AC induction motor used in various industrial applications. This reference design demonstrates the following functionality and performance of ISO5852S IGBT gate driver in the real system:

- Unipolar and bipolar IGBT gate driver supply operation
- Undervoltage shutdown
- Interface with external BJT based current buffers
- DESAT detection
- Miller clamp
- Soft turn OFF
- Propagation delay
- ESD and EFT immunity performance of IGBT gate driver at system level

IGBT power module has been chosen such that its footprint fits multiple devices so as to perform gate driver validation on IGBTs from different manufacturers. The footprint supports:

- Fuji Electric: 6MBL150VX-120-50, 6MBL100VX-120-50
- Mitsubishi: CM150TX-24S1
- Infineon: FS50R12KT4, FS200R12KT4R, FS100R17N3E4

The C2000 Piccolo LaunchPad evaluation kit, based on the F28027 MCU is been used to control the inverter.

The power stage includes protection against IGBT overcurrent, over temperature of power module, and DC bus sensing for protection against overvoltage.

2 Key System Specifications

表 1. Key System Specifications of Power Stage

PARAMETER	SPECIFICATION
DC link input voltage	400 to 1100 V
Control voltage	24-V DC
IGBT power module	1200 V/50 to 150 A
Maximum input DC current	50 A with 200 CFM Airflow
Rated power capacity	22 kW
Inverter switching frequency	16 kHz (Default); adjustable through software
Isolation	Reinforced (IEC61800-5)
Operating ambient temperature	–25°C to 65°C
Inverter efficiency	≥ 97% (Theoretical) at rated load
Controller	TMS320F28027
Motor	3-phase 400-V Induction motor
Provision for resistive braking	Yes
Power supply specification for MCU	3.3 V ±5%
Feedbacks	DC bus voltage, IGBT temperature
Protections	Short circuit, over temperature, DC bus under- or overvoltage
ESD (IEC61000-4-2)	±8-kV Contact discharge
EFT (IEC61000-4-4)	±4-kV on motor cables (shielded and unshielded)
PCB	370 × 240 mm / 4 Layer, 2Oz copper

3 System Description

The system consists of

- IGBT power module: hex bridge IGBTs to provide three phases output for variable-frequency drives to control the speed of AC motors (up to 22 kW). The PCB footprint supports mounting of different current rated modules from different manufactures
- ISO5852S reinforced isolated gate driver capable of sourcing a 2.5-A and 5-A sink current is used to drive the IGBTs. Half-bridge converter powered from 24-V with isolated 16-V/-8-V rails are used to power gate drivers. The half-bridge transformer has been designed to meet safety requirements as described in IEC61800-5
- Isolated amplifiers for measuring DC link voltage
- C2000 LaunchPad for controlling the inverter. This design uses F28027 InstaSPIN™ FOC-enabled MCU. The sinusoidal voltage waveform applied to the motor is created by using the Space Vector modulation technique implemented in the F28027 MCU
- Buck converters for powering control electronics, operated from a 24-V supply and generates multiple voltage rails like 15 V and 5 V. An LDO is used to generate 3.3 V from a 5-V supply for powering the C2000 LaunchPad
- Local DC link capacitor of ~220 μF. Relay is used to bypass NTC after power up
- Discrete brake IGBT for braking during regeneration
- Provision to measure the power module temperature using NTC
- Provision for operating the FAN

PCB is designed to fulfill the requirements of IEC61800-5. 図 2 depicts the block diagram of the power stage.

4 Block Diagram

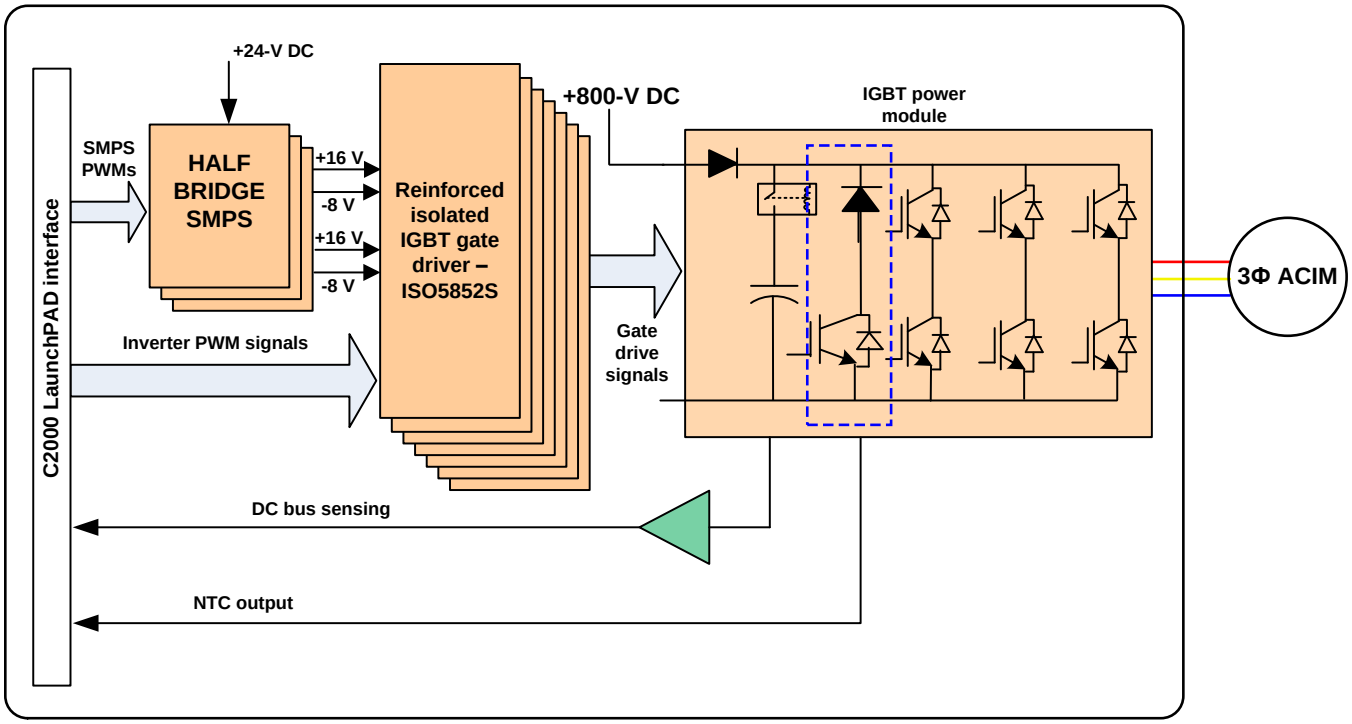


図 2. Power Stage Block Diagram

5 Highlighted Products

Key features of the highlighted devices can be taken from product datasheets. The following are the highlighted products used in the reference design.

5.1 ISO5852S

The ISO5852S is a 5.7 kV_{RMS}, reinforced isolated, IGBT gate driver with split outputs, OUTH and OUTL, providing 2.5-A source and 5-A sink currents. The primary side operates from a single 3-V or 5-V supply. The output side allows for a supply range from minimum 15 V to maximum 30 V. An internal DESAT detection recognizes when the IGBT is in an overload condition. Upon a DESAT detect, a Mute logic immediately blocks the output of the isolator and initiates a soft-turn-off procedure, which disables OUTH and reduces the voltage at OUTL over a minimum time span of 2 μs. When OUTL reaches 2 V with respect to the most negative supply potential, V_{EE2}, the output is hard-clamped to V_{EE2}.

During normal operation with bipolar output supply the output is hard clamp to V_{EE2} when the IGBT is turned OFF. If the output supply is unipolar, an active miller clamp connects the output to V_{EE2}.

5.2 CSD88537

The CSD88537 is a 60-V, dual N Channel, SO-8 NexFET™ power MOSFET with very low Drain-to-Source ON resistance of 12.5 mΩ. FET is capable of handling continuous current of 8 A. CSD88537 is designed to serve in half-bridge power supplies and motor control applications to generate gate driver supplies.

5.3 UCC27211

The UCC27211 is a MOSFET driver delivering peak source and sink current of up to 4 A. The inputs are independent of the supply voltage and have a maximum rating of 20 V. The floating high-side driver can operate with supply voltages of up to 120 V. The high-side driver is referred to the switch node (HS), which is typically the source pin of the high-side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to VSS, which is typically ground. Features of the UCC27211 include input stages UVLO protection, level shift, and built-in boot diode.

5.4 Piccolo LaunchPad

The C2000 LaunchPad is based around the C2000 Piccolo TMS320F28027 MCU, which features a 60-MIPS processing core, 64-KB integrated flash, 8 PWM channels with high resolution capability, 12-bit 4.6-MSPS ADC, capture interface, serial connectivity, and more. It is used to generate the PWM signals for the 3-phase inverter.

5.5 TPS54286

The TPS54286 is a dual output non-synchronous buck converter capable of supporting 2-A output applications that operate from a 4.5-V to 28-V input supply voltage, and provides output voltages between 0.8 V and 90% of the input voltage. The outputs can be enabled independently, or it can be configured to allow either ratio metric or sequential startup.

With an internally-determined operating frequency, soft start time, and control loop compensation, this converter provides many features with a minimum of external components. Other features include pulse-by-pulse overcurrent protection and thermal shutdown protection at 148ºC.

5.6 AMC1200

The AMC1200 is a precision isolation amplifier with an output separated from the input circuitry by a silicon dioxide (SiO_2) barrier that is highly resistant to magnetic interference. This barrier has been certified to provide galvanic isolation of up to 4000 V_{PEAK} according to UL1577 and IEC60747-5-2. The input of the AMC1200 is optimized for direct connection to shunt resistors with a voltage range of ±250 mV. The device has low offset error of 1.5 mV max, BW of 60 KHz and CMMR of 108 dB. The AMC1200 has a working voltage rating of 1200 V_{PEAK}.

The MC1200 is fully specified over the extended industrial temperature range of –40°C to 105°C and are available in a wide-body SOIC-8 package (DWV) and a gullwing 8 package (DUB).

5.7 SN6501

The SN6501 is a monolithic oscillator/power-driver, specifically designed for small form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 3.3-V or 5-V DC power supply. The secondary can be wound to provide any isolated voltage based on transformer turns ratio. The SN6501 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive the ground referenced N channel power switches. The internal logic ensures break-before-make action between the two switches. The SN6501 is available in a small SOT-23 (5) package, and is specified for operation at temperatures from –40°C to 125°C.

6 System Design Theory

6.1 Main Power Input

The main power input section is shown in 図 3. D1 is the reverse polarity protection diode and has reverse breakdown voltage of 1600 V. The input bulk aluminum electrolytic capacitors C3, C6, and C7 serve as local reservoirs for the IGBT module. These capacitors are rated to carry ripple current of 7.7 A. The rest of ripple current is expected to be sourced from external capacitors. In addition to the bulk aluminum capacitor, a polyester capacitor is used across the DC bus to suppress high frequency noises.

The startup current through the bulk capacitor is limited using thermistor, and the thermistor is bypassed after one second using a relay.

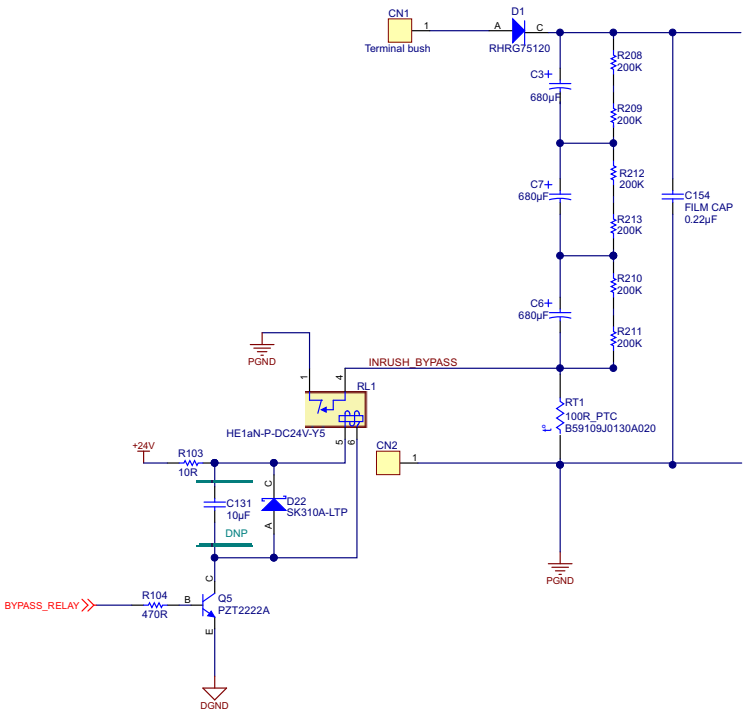


図 3. Main Power Input

6.2 Inverter Stage

The IGBT-based 3-phase hex bridge inverter is shown in 図 4. The decoupling capacitor (C154) should be placed near to DC bus entry of inverter for better filtering. An improper layout or position of the decoupling capacitors can cause undesired switching voltage spikes. IGBT (Q1) and free-wheeling diode (D2) is added externally to the hex bridge IGBT module for braking.

The brake IGBT (APT70GR120L) is rated for 70 A (at T_C = 110°C) current rating and 1200 V.

When DC bus voltage increases above the pre-defined value (this reference design uses a 1-kV threshold) brake operation is enabled through controller and the excessive energy will be dissipated through the resistive bank. The resistor bank is connected across the terminal blocks CN11 and CN12. The rating of external brake resistor is selected on the basis of the VFD rating, braking duty cycle, and magnitude of the energy to be dissipated.

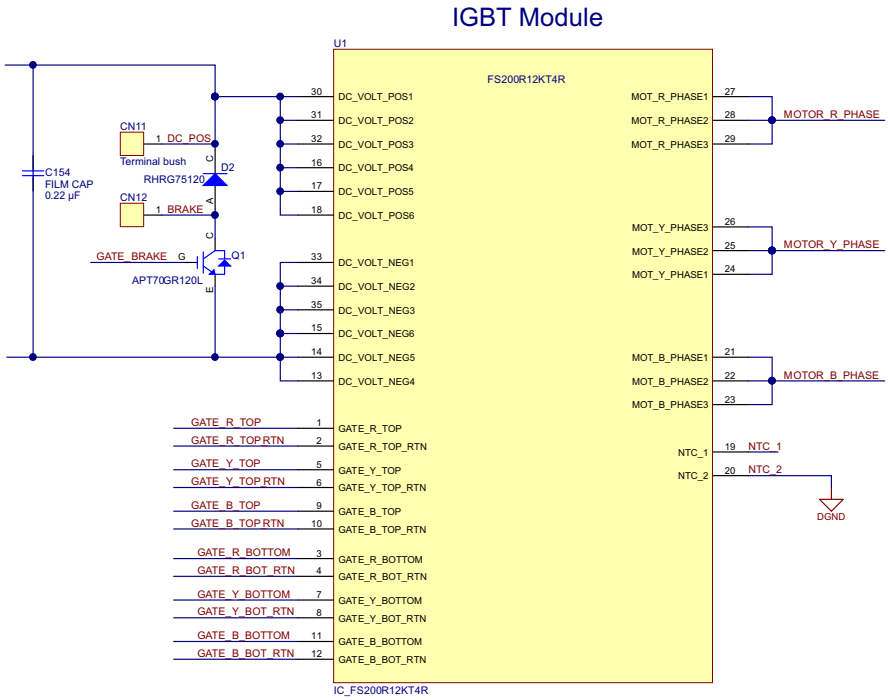


図 4. 3-Phase Inverter of Power Stage

6.2.1 IGBT module

This reference design is intended to support various makes of IGBT modules like Infineon, Fuji & Mitsubishi, and so on. The power stage is designed to deliver up to 22-kW power. The power stage was supplied with 800-V DC replicating high DC bus voltage during regeneration. Considering the safety factor and switching spikes, IGBTs were selected with the voltage rating greater than or equal to 1200 V. The current rating of the IGBT depends on the peak winding current.

The 3-phase inverter bridge is switched such that the sinusoidal current is injected into the motor windings.

- Motor rating = 22 kW
- Line-to-line voltage = 415-V AC
- Power factor considered = 0.8
- Motor efficiency = 85%

$$I_{LL} = \frac{P_{out}}{\eta_{motor} \times V_{LL} \times \sqrt{3} \times \cos\varnothing} \quad (1)$$

Current through the winding = 47 A

Therefore, the peak value of the winding current = $\sqrt{2} \times I_{RMS}$ = 66 A. (2)

Considering an overloading of 200%, the peak winding current would be 132 A.

The IGBT module used in this reference design (CM150TX-24S1) has continuous collector current carrying capacity of 150 A at T_C = 100°C and peak current capacity of 300 A.

The selection of IGBT module with inbuilt NTC Thermistor is preferred to avoid thermal breakdown of the IGBT. This IGBT temperature rise information is routed to the MCU to take necessary action.

IGBTs can be driven into saturation to provide a very low voltage drop between the emitter and collector.

6.3 DC Link Voltage Sense Circuit

The DC bus input voltage to the inverter module is scaled down and fed to the MCU using the AMC1200 isolation amplifier, which has a gain of 8. The differential output of the AMC1200 can directly drive an analog-to-digital converter (ADC) input or can be further filtered before being processed by the ADC.

The resistor divider network is chosen considering the maximum voltage for the MCU ADC input as 3.3 V and the maximum DC link voltage to be measured as 1200 V.

To achieve better linearity and the noise performance of the device, the allowable input voltage between the amplifier pin V_{INP} and V_{INN} is ±250 mV. The voltage divider resistor is selected such that input voltage to the amplifier is less than ±250 mV at maximum DC bus condition.

Resistors R76 to R81 (see 図 5) are selected as 1-M high-voltage resistors and R85 = 1K and R88 = 10K. The differential output of the AMC1200 is directly routed to ADC of MCU.

AMC Output = AMC Gain × V_{IN}

$$V_{IN} = \left(\frac{R_{85}}{R_{IN}}\right) \times V_{DC} \qquad (3)$$

$$V_{IN} = \left(\frac{1K}{6M + 11K}\right) \times V_{DC}$$

$$V_{IN} = 0.00017 \times V_{DC}$$

For 400-V DC input
V_{IN} = 0.00017 × 400 ≈ 0.0665 V and V_{OUT} = 8 × 0.0665 V ≈ 0.532 V.

For 1200-V DC
V_{IN} = 0.00017 × 1200 ≈ 0.2 V
V_{OUT} = 8 × 0.2 V ≈ 1.6 V

A decoupling capacitor of 4.7 µF and 0.1 µF is used for filtering the power-supply path of the AMC1200. A capacitor (C166 and C84 in 図 5) should be placed as close as possible to the VDD1 pin for best performance.

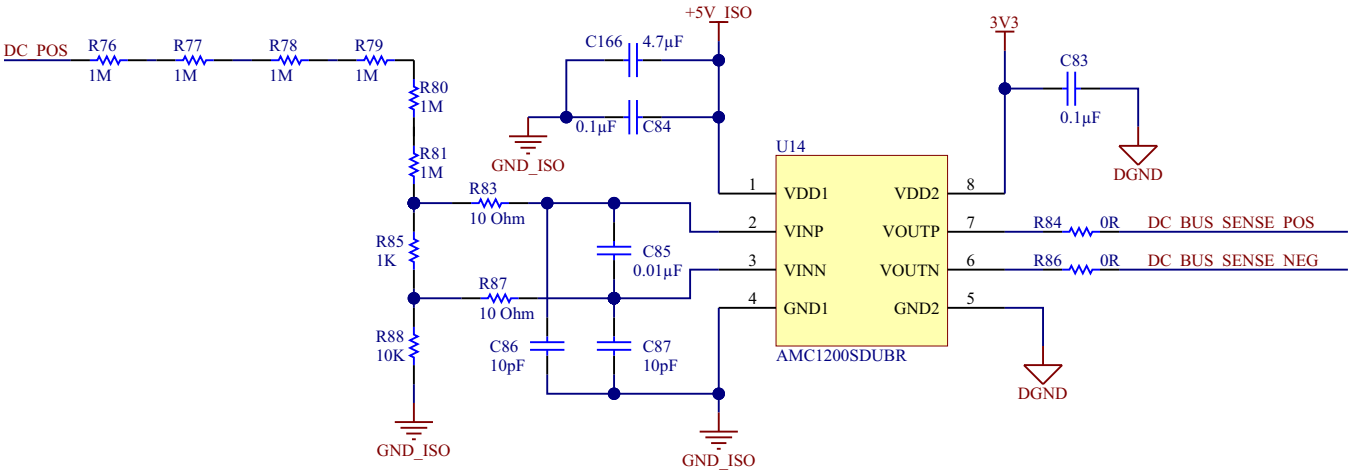


図 5. DC Voltage Sensing Module

6.4 ISO5852S: Isolated IGBT Gate Driver

The ISO5852S is a 5.7-kV_{RMS}, reinforced, isolated IGBT gate driver with split outputs OUTH and OUTL capable of providing a 2.5-A source and 5-A sink currents. The primary side operates from a single 3.3-V or 5-V supply. The output side allows for a supply range from minimum of 15 V to maximum 35 V. The ISO5852S has both inverting and non-inverting gate control inputs, an active low reset input, and an open drain fault output suitable for wired-OR applications.

図 6 shows the one section of the gate driver schematic. This IC can be powered with either a unipolar or bipolar supply. If the IC is powered by unipolar supply, the V_{EE2} PIN should be connected to GND2. The supply bypass capacitors provide the large transient currents necessary during a switching transition.

The ISO5852S has the following features:

- 5.7-kV_{RMS} reinforced isolation voltage
- 1.5-kV_{RMS} working voltage
- 12-kV surge rating
- Split outputs providing 2.5-A peak source and 5-A peak sink currents
- Short propagation delay: 76 ns typical
- Active miller and short-circuit clamp
- Soft turn-off during short circuit
- $\overline{\text{FAULT}}$ alarm and $\overline{\text{RESET}}$
- Input and output supply UVLO with ready (RDY) output
- CMOS compatible inputs

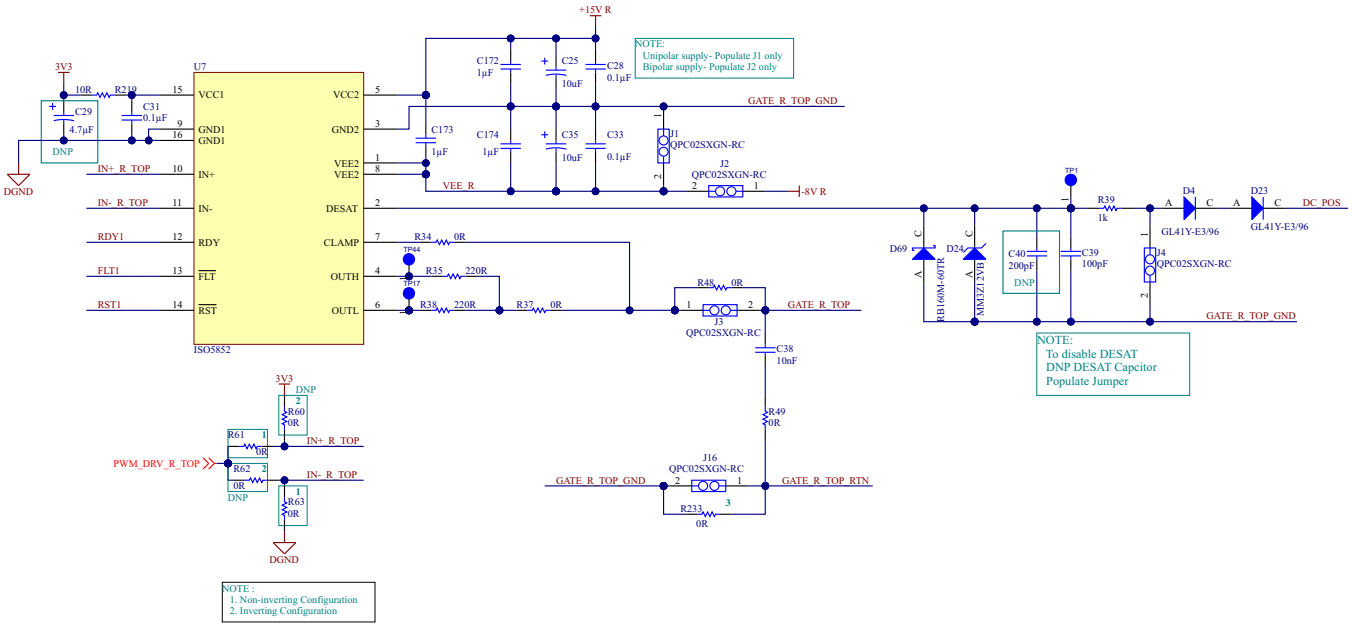


図 6. ISO5852S Application Schematic

6.4.1 Power Supply

VCC1 and GND1 are the supply pins for the input side of the ISO5852S. The supply voltage at VCC1 can range from 3 to 5.5 V with respect to GND1, thus supporting the direct interface to 3.3 V low-power controllers as well as legacy 5 V controllers.

VCC2 and GND2 are the supply pins for the output side of the ISO5852S. VEE2 is the supply return for the output driver and GND2 is the reference for the logic circuitry. The supply voltage at VCC2 can range from 15 V up to 30 V with respect to VEE2.

A positive VGE of typically 15 V is required to switch the IGBT well into saturation. In this design, VCC2 is fed with 16 V to ensure that IGBT is in full saturation.

For low power IGBTs, miller clamp functionality of the gate driver enables it to be operated with unipolar voltage (VEE2 connected to GND2). For larger IGBTs, negative values of VGE, ranging from a required minimum of –5 V up to the recommended –15 V, are necessary to keep the IGBT turned off and to prevent it from unintentional conducting due to noise transients, particularly during short circuit faults. The board has provision for connecting VEE2 to either 0 V or –8 V through jumpers.

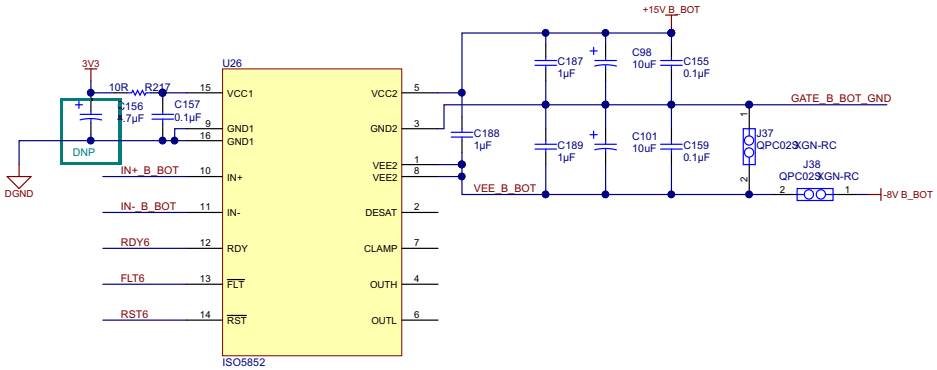


図 7. ISO5852S Supply Voltages

6.4.2 Control Signal Inputs

The two digital control inputs, IN+ and IN–, allow for inverting and non-inverting control of the gate driver output. In the non-inverting configuration, IN+ receives the control input signal and VIN– is connected to GND1. In the inverting configuration, VIN– is the control input while VIN+ is connected to VCC1.

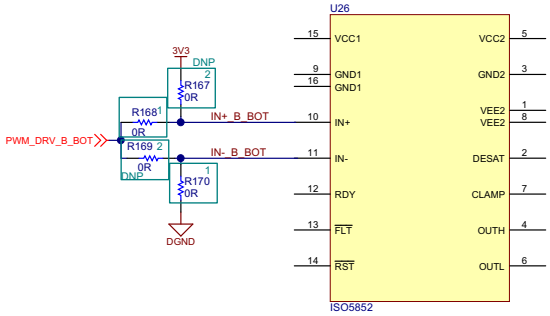


図 8. ISO5852 Non-Inverting and Inverting Input Configurations

6.4.3 Gate Resistance

The gate current and the appropriate power of the voltage supply depend on the operating frequency, bias control voltages, and total gate charge. The total gate charge is published in IGBT datasheets, depending on gate-control voltage. The gate charge necessary for switching is very important to establish the switching performance of a MOSFET or IGBT. The lower the charge, the lower is the gate-drive current needed for a given switching time. The gate current can be controlled using external gate resistor between driver output and gate of IGBT. The value of the gate resistor determines the peak charge and discharge currents.

The ISO5852S device features a split-output configuration where the gate drive current is sourced through the OUTH pin and sunk through the OUTL pin. This pin arrangement provides flexibility to apply independent turn-on and turn-off resistors to the OUTH and OUTL pins respectively and easily control the switching slew rates. The value of the gate resistor influences different aspects of the switching process like:

- IGBT switching losses
- Control di/dt
- Cross conduction
- Reverse recovery losses of the diode

The value of gate resistor is system dependent and usually chosen a value to provide optimum performance. Strong sink capability (5 A) in an asymmetrical drive also boosts immunity against parasitic Miller turn-on effect.

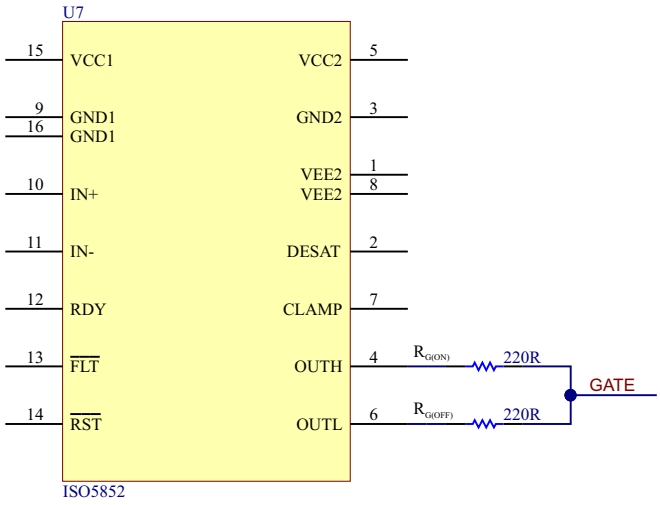


図 9. Gate Drive Split Outputs

6.4.4 Optional External Current Buffer

When driving larger IGBTs requiring gate currents more than 5 A, an external current boost circuit can be built with discrete NPN/PNP complimentary pair. One possible implementation is shown in Figure 10. The selected BJT should be of fast switching and to have sufficient current gain to deliver the desired peak output current. The circuit, in 図 10, with a MJD3055T4/MJD2955 pair can drive gate currents up to 10 A.

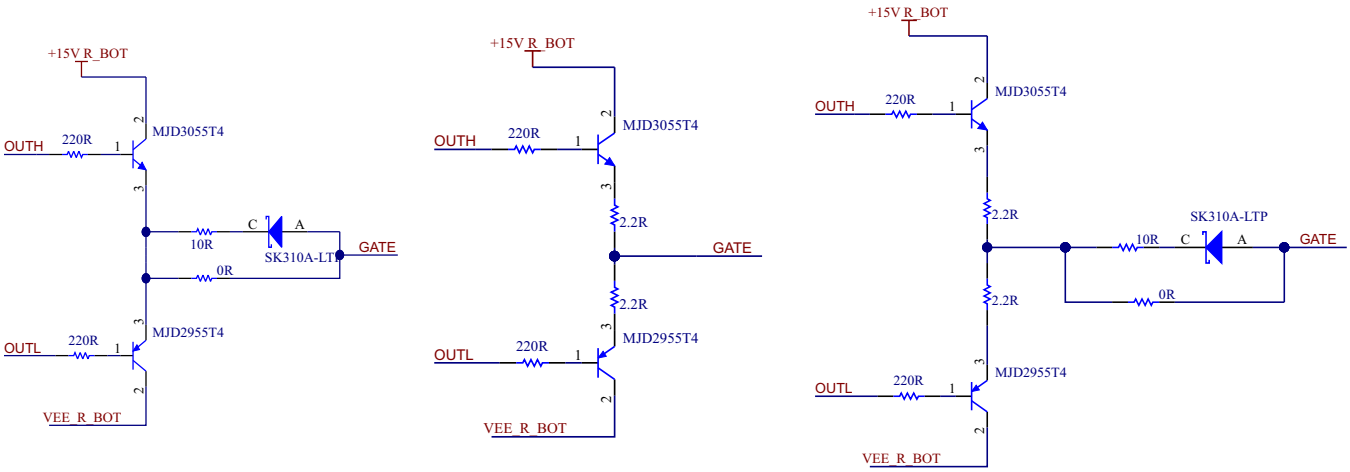


図 10. Options in Using External Current Buffer

6.4.5 Undervoltage Lockout

The undervoltage lockout feature prevents the application of insufficient gate voltage (V_{GE-ON}) to the power device by forcing OUTH/OTL low during power-up and whenever supply voltage drops below 11 V. IGBTs typically require gate voltages of V_{GE} = 15 V to achieve their rated, low saturation voltage, V_{CES}. At gate voltages below 13 V typically, their V_{CE-ON} increases drastically, especially at higher collector currents. At even lower voltages, that is V_{GE} < 10 V, an IGBT starts operating in the linear region and quickly overheats. The UVLO feature of ISO5852S avoids operating the IGBT in linear region by shutting it off during insufficient gate supply voltage.

The UVLO feature has a hysteresis of 1 V typical and the typical values for the positive and negative going input threshold voltages are V_{TH+} = 12 V and V_{TH-} = 11 V.

6.4.6 Desaturation Protection (DESAT)

The DESAT fault detection prevents IGBT destruction due to excessive collector currents during a short circuit fault. Short circuits caused by bad wiring, or overload conditions induced by the load can cause a rapid increase in IGBT current, leading to excessive power dissipation and heating. IGBTs become damaged when the current approaches the saturation current of the device and the collector-emitter voltage, V_{CE}, rises above the saturation voltage level, V_{CE-sat}. The drastically increased power dissipation overheats and destroys the IGBT.

To prevent damage to IGBT, ISO5852S slowly turns OFF the IGBT in the event of fault detection. Slow turn OFF ensures the overcurrent is reduced in a controlled manner during the fault condition. The DESAT fault detection involves a comparator that monitors the IGBT's V_{CE} and compares it to an internal 9-V reference. If voltage across the IGBT reaches the threshold, DESAT detects immediately and blocks the gate driver output and initiates a soft-turn-off procedure that disables the OUTH, and reduces the voltage at OUTL over a minimum time span of 2 µs. The output is hard clamped to VEE2 when OUTL reaches 2 V with respect to VEE2.

6.4.6.1 DESAT Pin Protection

The diodes (GL41Y in 図 11) at the DESAT signal block the high voltage during the IGBT OFF state and conduct forward current, which allows the sensing of the IGBT's saturated collector-to-emitter voltage (V_{CESAT}) when the IGBT is "ON". To avoid false DESAT triggering, fast switching diodes with low capacitance are recommended. Because the sum of the DESAT diode forward-voltage and the IGBT collector-emitter voltage make up the voltage at the DESAT-pin, $V_F + V_{CE} = V_{DESAT}$, the VCE level, which triggers a fault condition, can be modified by adding multiple DESAT diodes in series: $V_{CE\text{-}FAULT\ (TH)} = 9\ V - n \times V_F$ (where n is the number of DESAT diodes). When using two diodes instead of one, diodes with half the required maximum reverse-voltage rating may be chosen. See 図 11 where provision is provided to mount two DESAT diodes.

Switching inductive loads causes large instantaneous forward voltage transients across the freewheeling diodes of IGBTs. These transients result in large negative voltage spikes on the DESAT pin which draw substantial current out of the device. To limit this current below damaging levels, a 100-Ω to 1-kΩ resistor can be connected in series with the DESAT diode. Further protection is possible through an optional Schottky diode (MM3Z12VB), whose low forward voltage assures clamping of the DESAT input to GND potential at low voltage levels.

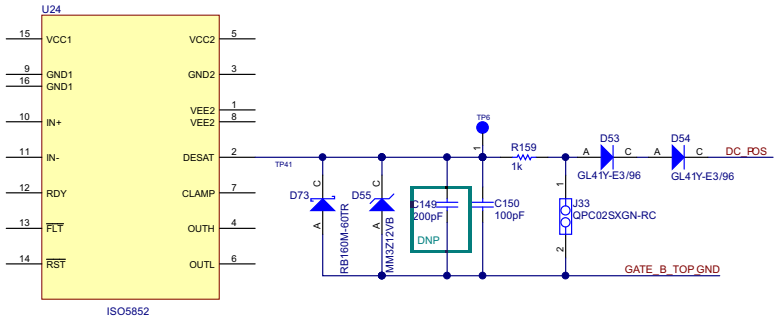


図 11. DESAT Detection

DESAT Blanking Time

The DESAT fault detection must remain disabled for a short time period following the turn-on of the IGBT to allow its collector voltage to drop below the 9-V DESAT threshold. This time period, called the DESAT blanking time, t_{BLK}, is controlled by an internal charge current of I_{CHG} = 500 μA, the 9-V DESAT threshold, V_{DSTH}, and an external blanking capacitor, C_{BLK}.

CDESAT = 100 pF (refer to C150 in 図 11).

$$t_b = \frac{9\,V \times C_{DESAT}}{500\ \mu A} \tag{4}$$

$$t_b = \frac{9\,V \times 100\ pF}{500\ \mu A}$$

$$t_b\,(\mu s) = 1.8$$

The capacitor value can be scaled slightly to adjust the blanking time. However, because the blanking capacitor and the DESAT diode capacitance build a voltage divider that attenuates large voltage transients at DESAT, C_{BLK} values smaller than 100 pF are not recommended.

If V_{CE} exceeds this reference voltage (9 V) after the blanking time, the comparator inside ISO5852S causes the gate drive and fault logic to initiate a fault shutdown sequence. This sequence starts with the immediate generation of a fault signal, which is transmitted across the isolation barrier towards the fault indicator circuit at the input side of the ISO5852S.

This board also provides feature of disabling the DESAT during testing by connecting the jumper at the DESAT pin.

6.4.7 Active Miller Clamp

During turn-on or turn-off of IGBTs, displacement current flows through the miller capacitor (gate to collector capacitor) of the IGBT, raising its gate voltage. It could lead to unintentional turn-on of the IGBT. When the high-side IGBT turns on within an inverter leg, the voltage across the low-side IGBT increases with a high dv/dt. The ratio of reverse transfer capacitance to the input capacitance is larger for IGBTs (C_{RES}/C_{IES}). This produces an increased Miller effect and a larger noise is coupled from the collector to the gate.

This induces a current in the gate of the lower IGBT that may produce turn-on of the low-side device shorting the DC bus.

However, certain low-power IGBTs have a lesser C_{RES} (reverse transfer capacitance) and do not need negative gate voltage for turn-off. Instead, the clamp functionality of the ISO5852S can be used to ensure that gate is pulled to emitter thorough a low-impedance path, preventing a false turn-on.

The CLAMP transistor is turned on when OUTL reaches 2 V with regard to VEE2 during turn-off of the IGBT. The CLAMP transistor hard clamps the OUTL pin to VEE2. The clamp transistor remains on once it is ON even if OUTL goes above 2 V. The CLAMP transistor is again turned off during IGBT turn-on process.

If the supply is unipolar, an active Miller clamp connects the output to V_{EE2} (Ground), and this condition is latched. During a bipolar supply operation, the output is hard clamped to VEE2 (-8 V) when the IGBT is turned off.

For larger IGBTs, a still negative gate voltage is required. Another reason for the negative gate voltage at IGBTs is of the operation at higher voltages with increased (dv/dt) coupling of noise.

6.4.8 Fault and Protection Handling

The $\overline{\text{FAULT}}$ pin indicates an error event (with soft shutdown) has occurred such as IGBT short circuit. Fault will be latched until the reset is applied. $\overline{\text{FAULT}}$ will go high, when the logic low pulse is applied to RESET pin. This can be accomplished with an MCU, or an additional logic gate that synchronizes the RESET signal with the appropriate input signal.

The ready pin is high during the primary and secondary side supplies are good. It is pulled LOW when the supply voltage is less than the UVLO limits.

6.4.9 External Gate Emitter Capacitor to Shunt Miller Current

An option to mount external capacitor between IGBT gate and emitter has been provided to evaluate the effectiveness of clamp functionality.

This capacitor can sink the additional charge originating from the Miller capacitance during the turn-on of top IGBT. Due to the additional capacitance, the effective input capacitance of the IGBT is $C_G||C_{GE}$, the gate charge required to reach the threshold voltage will be increased.

6.4.10 Power Dissipation

In the process of turning the IGBT ON and OFF, power is dissipated by the driver IC, IGBT gate, and by any RC circuits in the gate drive path.

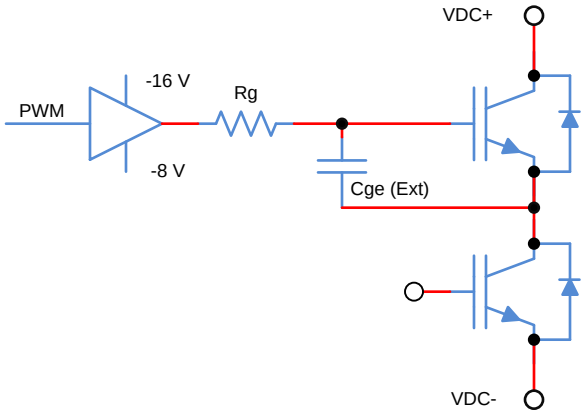


図 12. Driver Power Loss

The total gate power dissipation is calculated with 式 5:

$$P_{gate} = P_{dc} + \left(Q_{gate} \times F_{sw} \times \Delta V_{gate}\right) + \left(C_{ge} \times F_{sw} \times \Delta V^{2}_{gate}\right) \quad (5)$$

where

- Q_{gate} = total gate charge
- F_{sw} = Switching frequency
- ΔV_{gate} = Gate driver output voltage swing

For CM150TX-24S1, Qg is approximated as 450 nC for bipolar switching and 300 nC for unipolar switching with V_{ge} = 15 V.

- F_{SW} = 16 KHz
- ΔV_{gate} = 15 V and 23 V
- C_{ge} = 10 nF

The static power dissipation of ISO5852S is PDC = $I_Q \times V_{DD}$ where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and so on, and also any current associated with switching of internal devices when the driver output changes state. The ISO5852S features very low quiescent currents — 6 mA when supplied with 15 V and –8 V.

Power dissipation for bipolar switching: P_{gate} = 0.138 + 0.1656 + 0.085 = 0.4 W

Power dissipation for unipolar switching: P_{gate} = 0.2 W

6.5 Half-Bridge SMPS for Gate Driver

A half-bridge SMPS is used to generate isolated positive (16 V) and negative (–8 V) voltage rails required by IGBT gate drivers from a single 24-V DC input supply. The half-bridge driver is operated in open loop mode with 500 kHz / 50% duty cycle generated by the Piccolo controller.

This half-bridge topology allows for more efficient use of the transformer core than the flyback or forward converters. The transformer has two secondaries, each generating 8.7 V (required output = 8 V with a diode drop of 0.7 V). A voltage doubler has been used to generate 16 V from the secondary generated 8 V. Each transformer is used to power TOP and BOTTOM IGBTs of each phase.

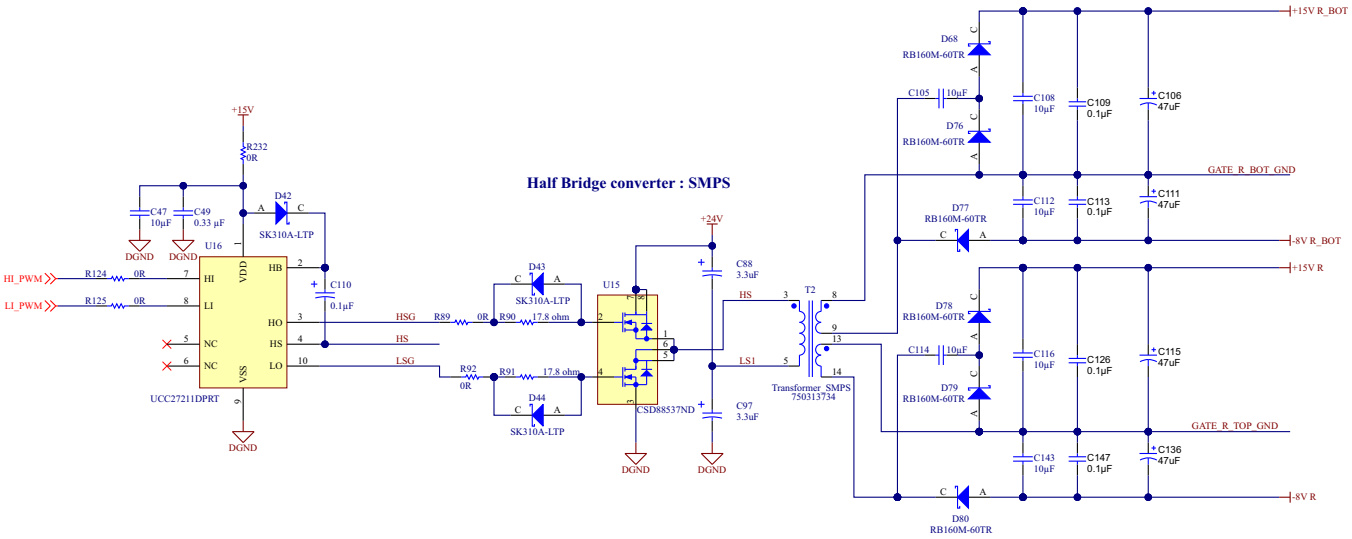


図 13. Isolated Power Supply

During the turn-on and turn-off of IGBT, gate driver requires instant peak current from its power supply for a short period of time, so it is important to use proper by-pass capacitors for the power supply. To achieve the minimum output ripple with high-current load transients, a 47-µF capacitor at each of the output on the secondary side is used.

6.5.1 Transformer Specification

- Two isolated outputs with V_{OUT1} = 8.7 V at 250 mA and V_{OUT2} = 8.7 V at 250 mA
- Switching frequency = 500 kHz
- Primary to secondary isolation = 7.4 kV for 1.2/50-µs impulse voltage
- Type test voltage:
  - Primary to Secondary = 3.6 kV_{RMS}
  - Secondary1 to Secondary2 = 1.8 kV_{RMS}
- Spacing:
  - Primary to Secondary clearance = 8 mm
  - Secondary1 to Secondary2 clearance = 5.5 mm
  - Creepage distance = 9.2 mm
- Functional Isolation Primary and secondary : 1.5-kV DC
- DC isolation between secondaries: 1.5-kV DC

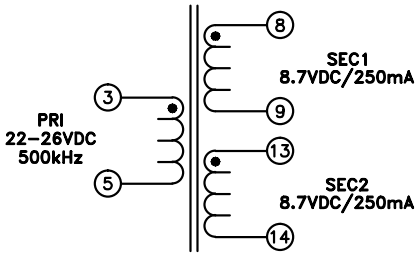


図 14. Half-Bridge Transformer Symbol

6.6 Design of 24-V to 15-V and 5-V Step-Down DC-DC Converter

The 15-V regulated power supply for the half-bridge driver and 5 V are derived using the TPS54286 switching converter. The TPS54286 device is a dual step-down (buck) regulator with an integrated high-side and low-side n-channel MOSFET. This operates in constant switching frequency, current mode control which reduces output capacitance, and also reduces the complexity of compensation design. The design specifications of the step-down converter are given 表 2. The schematic of the step-down converter is shown in 図 15.

表 2. Design Specifications of Step-Down Converter

PARAMETER	SPECIFICATION
Output voltage	15 V and 5 V
Maximum output current	150 mA and 500 mA
Input voltage	24 V pre-regulated
Output voltage ripple	0.5% of V_{OUT}

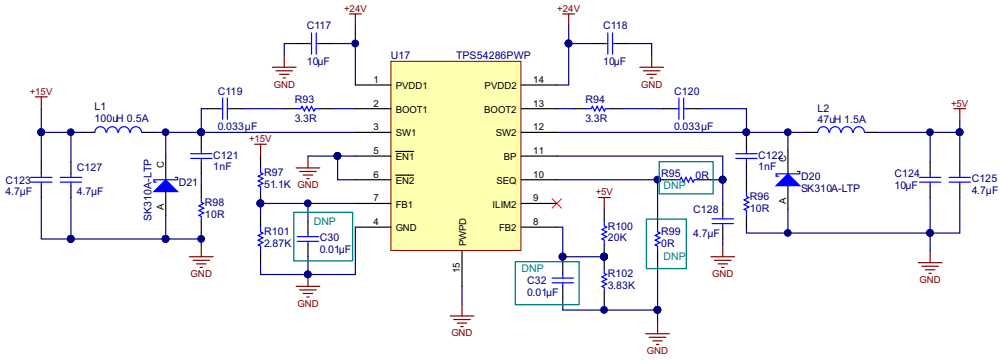


図 15. 24-V to 15-V and 5-V Step-Down Converter

6.6.1 Circuit Design

6.6.1.1 Output Inductor Selection (LO)

To calculate the minimum value of the output inductor,

For 5-V output

$$D_{min} \approx \frac{V_{OUT} + V_{FD}}{V_{IN(max)} + V_{FD}} \tag{6}$$

$$D_{min} \approx \frac{15\ V + 0.7\ V}{24\ V + 0.7\ V} \approx 0.23$$

$$L_{min} \approx \frac{V_{IN(max)} - V_{OUT}}{I_{LRIP(max)}} \times D_{min} \times \frac{1}{f_{SW}} \tag{7}$$

$$L_{min} \approx \frac{24 - 5}{0.15} \times 0.23 \times \frac{1}{600 \times 10^3} = 48.71\ \mu H \approx 47\ \mu H$$

For 15-V output

$$D_{min} \approx \frac{15\ V + 0.7\ V}{24\ V + 0.7\ V} \approx 0.635$$

$$L_{min} \approx \frac{24\ V - 15\ V}{0.1} \times 0.635 \times \frac{1}{600 \times 10^3} = 95.25\ \mu H \approx 100\ \mu H$$

Ripple current for 15 V

$$I_{RIPPLE} \approx \frac{V_{IN(max)} - V_{OUT}}{L} \times D_{min} \times \frac{1}{f_{SW}} \tag{8}$$

$$I_{RIPPLE} \approx \frac{24\,V - 15\,V}{100\ \mu H} \times 0.635 \times \frac{1}{600 \times 10^3} = 0.095\,A \approx 0.1\,A$$

$$I_{L(rms)} = \sqrt{\left(I_{L(avg)}\right)^2 + \frac{1}{12}\left(I_{RIPPLE}\right)^2} \tag{9}$$

$$I_{L(rms)} = \sqrt{(0.2)^2 + \frac{1}{12}(0.1)^2} = 0.202\ A$$

Ripple current for 5 V

$$I_{RIPPLE} \approx \frac{24\ V - 5\ V}{47\ \mu H} \times 0.230 \times \frac{1}{600 \times 10^3} = 0.154\,A \approx 0.15\ A$$

$$I_{L(rms)} = \sqrt{(0.5)^2 + \frac{1}{12}(0.15)^2} = 0.501\,A$$

6.6.1.2 Output Capacitor

The internal compensation of the TPS54286 limits the selection of the output capacitors. Internal compensation has a double zero resonance at about 6 kHz, so the output capacitor is selected by 式 10.

For 15 V

$$C_{OUT} = \frac{1}{4 \times \pi^2 \times \left(f_{RES}\right)^2 \times L} \tag{10}$$

$$C_{OUT} = \frac{1}{4 \times \pi^2 \times \left(6 \times 10^3\right)^2 \times 100\ \mu H} = 7.04\ \mu F$$

For 5 V

$$C_{OUT} = \frac{1}{4 \times \pi^2 \times \left(6 \times 10^3\right)^2 \times 47\ \mu H} = 14.97\ \mu F$$

6.6.1.3 Output Voltage Regulation

For this design feedback divider resistors (R97, R100) are 20K and 51.1K. The lower resistor R102 and R103 are found using the following equations.

$$R102 = \frac{V_{FB} \times R97}{V_{OUT1} - V_{FB}} \tag{11}$$

$$R102 = \frac{0.8 \times 51.1 \times 10^3}{15\,V - 0.8} = 2.873\ k\Omega$$

$$R103 = \frac{V_{FB} \times R97}{V_{OUT1} - V_{FB}} \tag{12}$$

$$R103 = \frac{0.8 \times 20 \times 10^3}{5 - 0.8} = 3.809\ k\Omega$$

6.6.1.4 Bootstrap circuit

A 3.3-nF ceramic capacitor must be connected between the BOOT and SW pins for proper operation. Use a ceramic capacitor with X5R or better grade dielectric. The capacitor should be rated 50 V or higher.

A small resistor with value between 1 and 3 Ω to be placed in series with the bootstrap capacitor; this reduces the rising edge ringing at the SW node.

6.6.1.5 Snubber

Fast switching and parasitic inductance and capacitance results in a voltage ringing at the SW node. If the ringing results in excessive voltage on the SW node or erratic operation of the converter, an R-C snubber (C = between 330 pF and 1 nF, R = 10 Ω) may be used to dampen the ringing at the SW node to ensure proper operation over the full load range.

6.7 Design of 5-V isolated DC-DC Converter

The AMC1200 requires isolated power supply for powering its input section. The SN6501 is used as a switching device to generate a 5-V isolated output.

表 3. Specifications for Selection of 5-V DC-DC Converter

PARAMETER	SPECIFICATION
Output voltage	5 V
Output current required	10 mA
Input voltage	5 V
Output voltage ripple	0.5% of V_{OUT}

The SN6501 is a monolithic oscillator and power-driver, specifically designed for isolated power supplies in isolated interface applications with small form factor. It drives a low-profile, center-tapped transformer primary from a 3.3-V or 5-V DC power supply. The SN6501 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive the ground referenced N-channel power switches. The internal logic ensures break-before-make action between the two switches.

Features:

- Push-pull driver for small transformers
- Single 3.3-V or 5-V supply

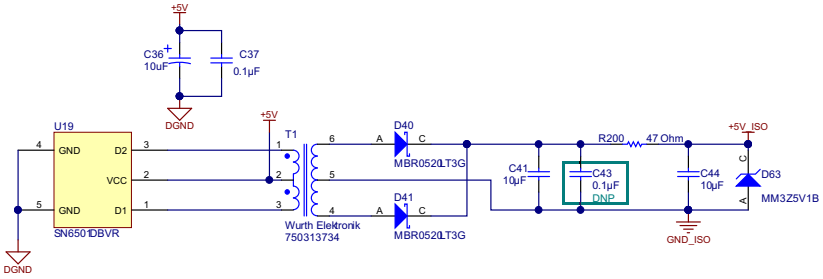


図 16. Isolated 5-V Converter

Transformer Selection

To prevent a transformer from saturation its V-t product must be greater than the maximum V-t product applied by the SN6501. The maximum voltage delivered by the SN6501 is the nominal converter input plus 10%. The maximum time voltage is applied to the primary is half the period of the lowest frequency at the specified input voltage. Therefore, the transformer's minimum V-t product is determined using 式 13.

$$Vt_{min} \geq V_{IN-max} \times \frac{T_{max}}{2} = \frac{V_{IN-max}}{2 \times f_{min}} \tag{13}$$

$$Vt_{min} \geq \frac{5.5\ V}{2 \times 300\ kHz} = 9.1\ V\mu s$$

Common V-t values for low-power center-tapped transformers range from 22 Vμs to 150 Vμs with typical footprints of 10 × 12 mm. Other important factors to be considered in transformer selection are isolation voltage, transformer wattage, and turns ratio.

Transformer Turns Ratio Estimation

$$n_{min} = 1.031 \times \frac{V_{F-max} + V_{DO-max} + V_{O-max}}{V_{IN-min} - R_{DS-max} \times I_{D-max}} \tag{14}$$

表 4. Transformer Specifications

PARAMETERS	TEST CONDITIONS	VALUE
DC resistance 1-3	@ 20°C	0.419 Ω max
DC resistance 6-4	@ 20°C	0.335 Ω max
Inductance 1-3	100 kHz,10-mV AC, L_S	340 µH min.
Dielectric 1-6	6250 V_{RMS}, 1 second	5000 V_{RMS}, 1 minute
Turns ratio	(6-4): (1-3)	1.1:1, +-2%

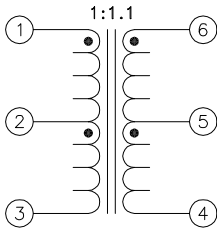


図 17. Isolated Transformer Construction

6.8 5-V To 3.3-V Regulator

表 5. Specification of 3.3-V Output LDO

PARAMETER	SPECIFICATIONS
Input voltage	5 V
Output	3.3 mA
Output current	350 mA

The LP38691 is selected is based on specifications outlined in 表 5. The LP3869x is a low-dropout CMOS linear regulator providing tight output tolerance (2% typical), extremely low-dropout voltage (250 mV at 500-mA load current V_{OUT} = 5 V), and excellent AC performance using ultra-low equivalent series resistance (ESR) ceramic output capacitors.

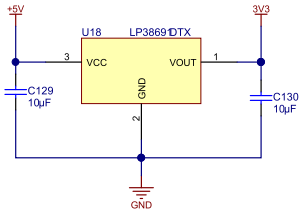


図 18. 3.3-V Circuit

6.9 Status Indications

The ISO5852S fault and ready indications are shorted and connected to two LED indications as shown in 図 19.

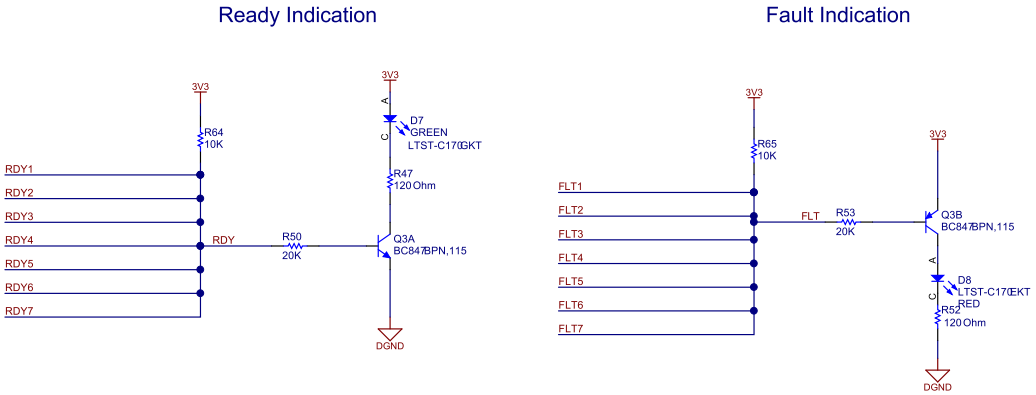


図 19. Status Indication Through LED

6.10 LaunchPad Connections

The C2000 InstaSPIN™ Piccolo LaunchPad is used for controlling the inverter.

The LaunchPad has following connections to the power stage:

- Thermistor feedback from the IGBT module
- DC bus voltage feedback
- $\overline{\text{FAULT}}$ ready
- PWM enable and RESET signals from the ISO5852S
- Relay_Enable signal
- Fan drive signals
- PWM signals for half-bridge SMPS
- PWM signals for gate driver

PWM_EN is used to control the buffer providing PWM signals to ISO5852S.

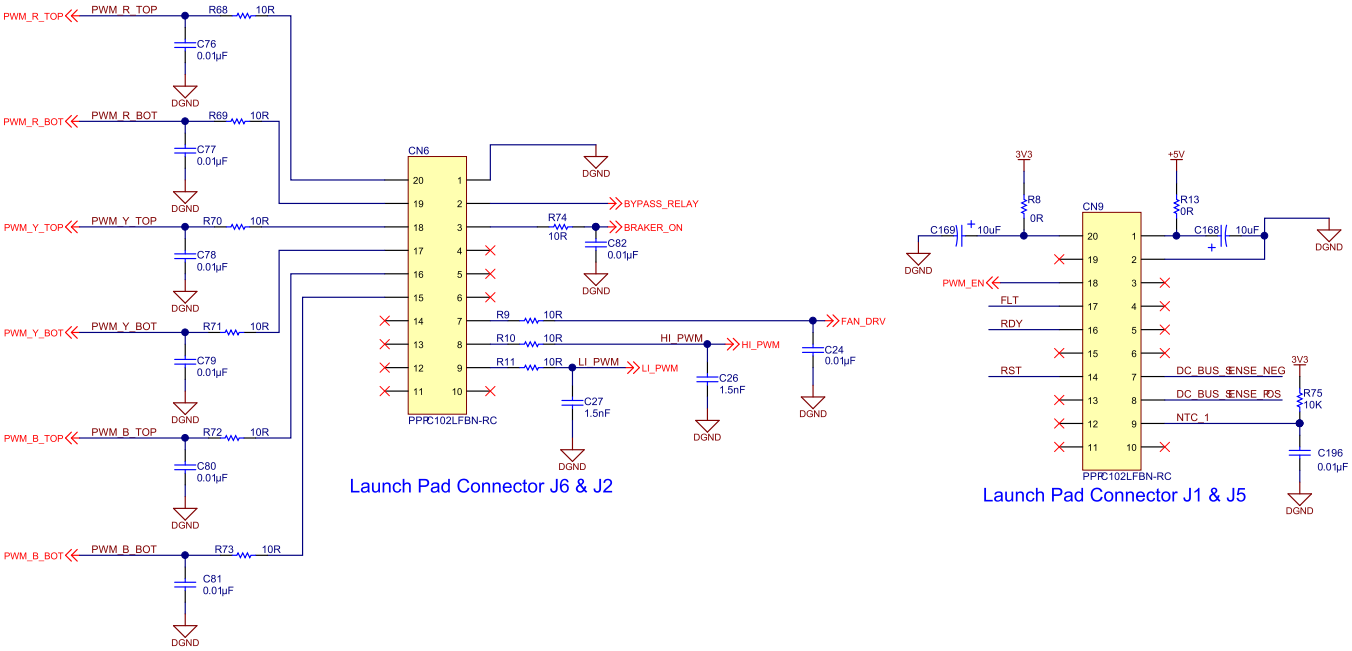


図 20. LaunchPad Connections for C2000 Piccolo LaunchPad

7 System Test Results

7.1 Power Supply

7.1.1 3.3-V LDO Output (U18)

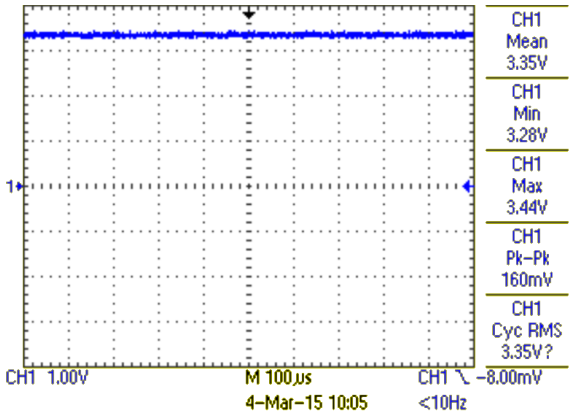


図 21. Output Voltage of 3.3-V LDO With Load of 100 mA

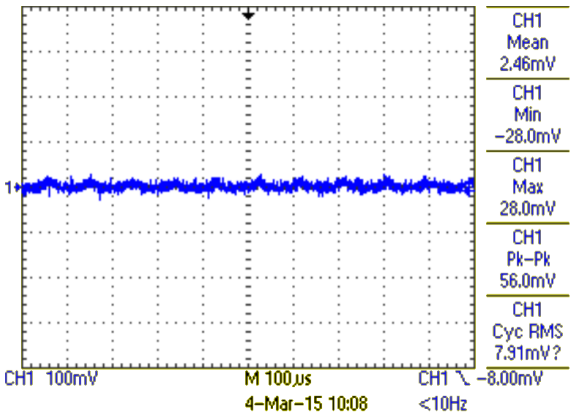


図 22. Ripples in 3.3-V LDO Output With Load of 100 mA

7.1.2 Buck Converter Outputs TPS54286PWP (U17)

7.1.2.1 15-V Output

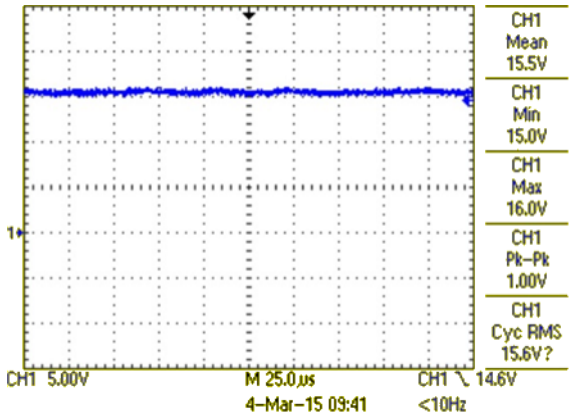


図 23. 15-V Supply With Load of 15 mA

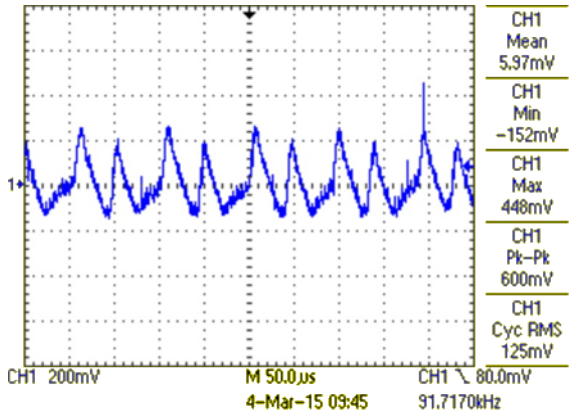


図 24. Ripples in 15-V Supply With Load of 15 mA

7.1.2.2 5-V Output

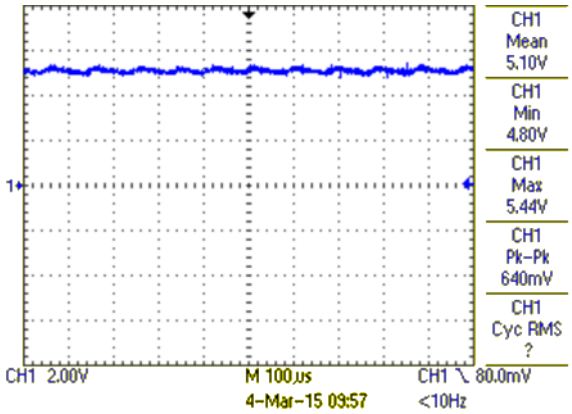


図 25. 5-V Supply With Load of 150 mA

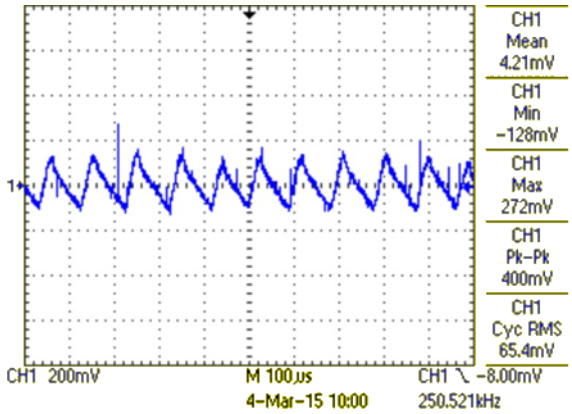


図 26. Ripples on 5 V With Load of 150 mA

7.1.3 Isolated 5-V Output SN6501DBVR (U19)

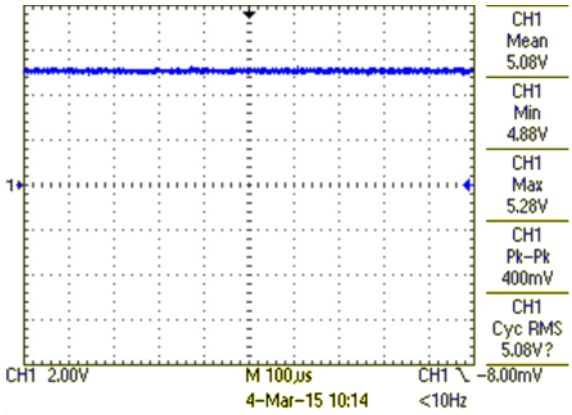


図 27. 5-V Isolated Supply Output With Load of 7 mA

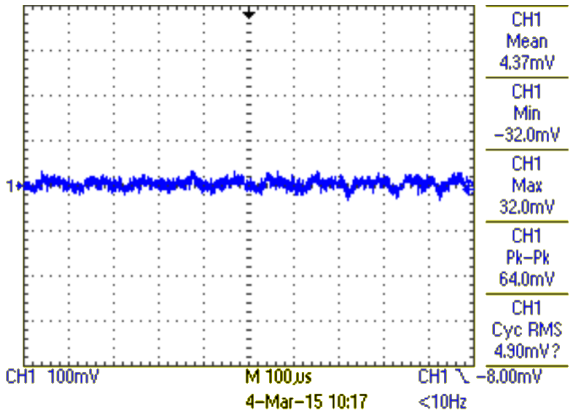


図 28. Ripple on 5-V Isolated Supply Output With Load of 7 mA

7.1.4 Half-Bridge Gate Driver supply

7.1.4.1 16-V Output From Half-Bridge SMPS

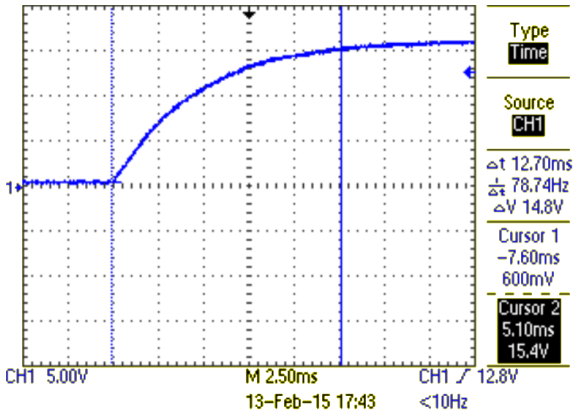


図 29. 16 V during power ON

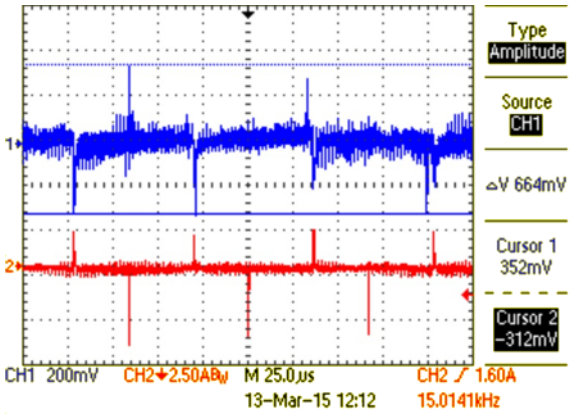


図 30. Ripples on 16 V at 2.5-A Source Current and 4.5-A Sink current

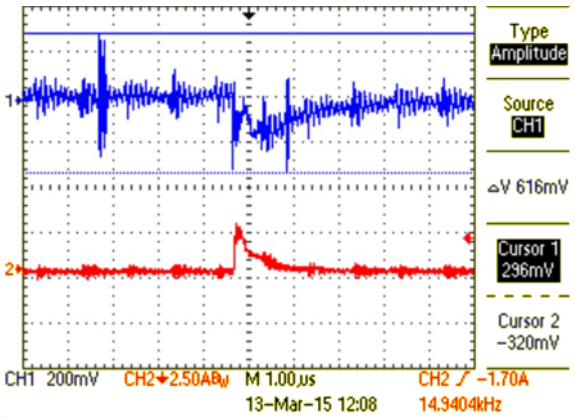


図 31. Ripples on 16 V at 2.5-A Source Current

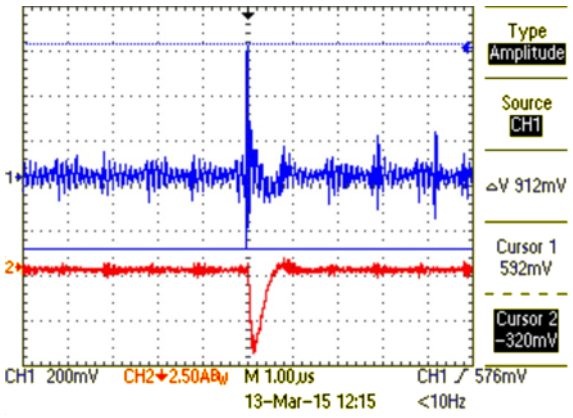


図 32. Ripples on 16 V at 4.5-A Sink Current

7.1.4.2 –8-V Output From Half-Bridge SMPS

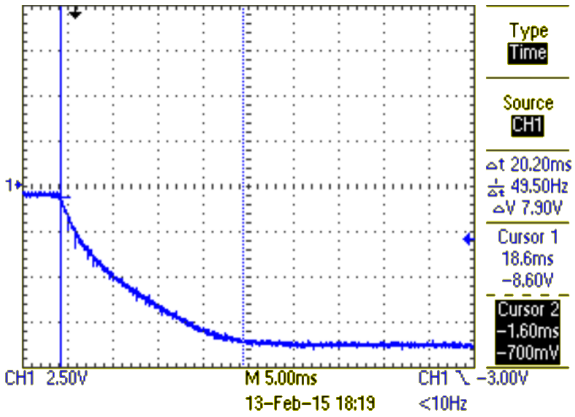


図 33. –8 V During Power ON

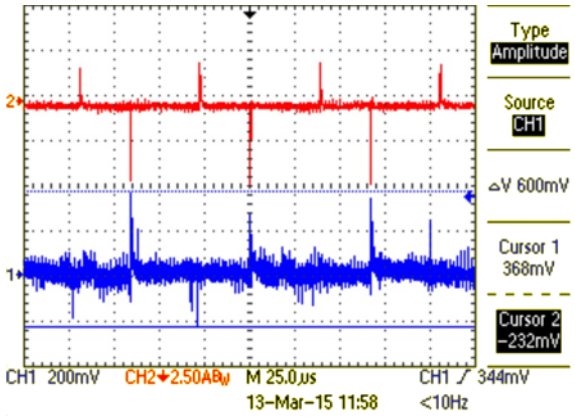


図 34. Ripple on –8 V

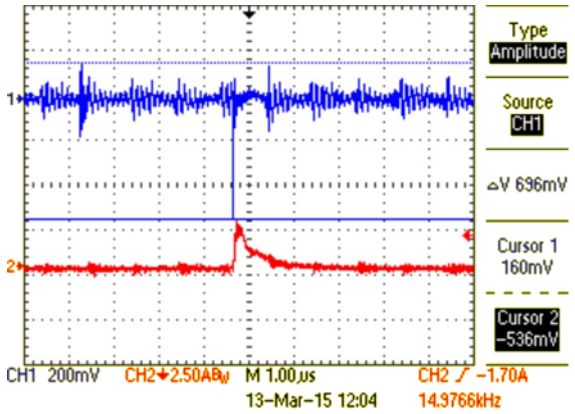


図 35. Ripple on –8 V at 2.5-A Source Current

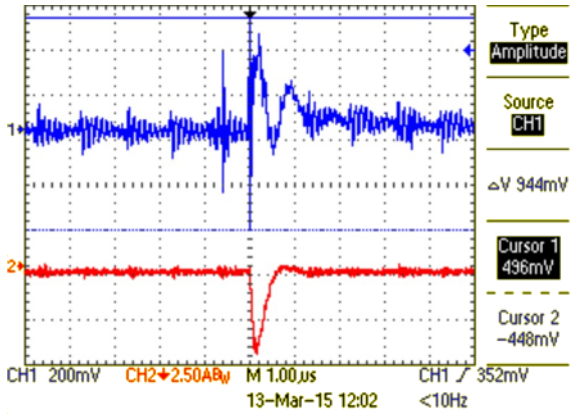


図 36. Ripple on –8 V at 4.5-A Sink Current

7.2 Power ON Test Without External BJT/MOSFET Buffer

The undervoltage lockout feature monitors the secondary voltage rail and prevents the IGBT operating with insufficient gate voltage (V_{GE-ON}) by forcing OUTH/OUTL to low (during power-up else V_{CC2} drops below 12 V). In 図 37 and 図 38, the gate driver output is held low (CH2) until VCC (CH3) exceeds 12 V. CH1 represents the PWM input of ISO5852S.

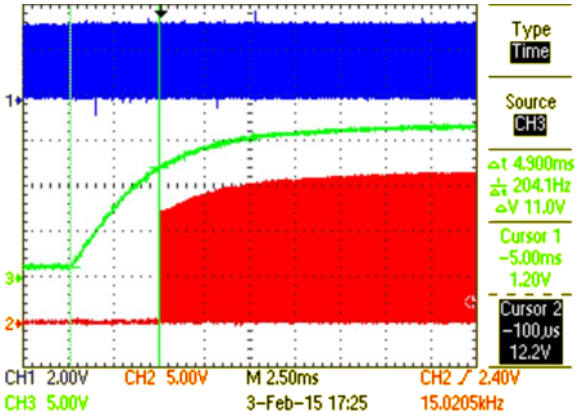


図 37. Gate Driver Output During Power ON With Unipolar Supply

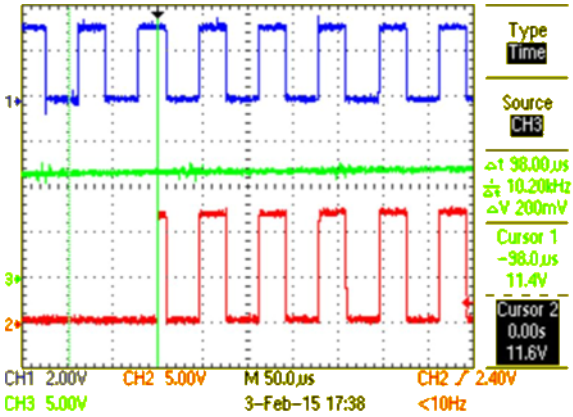


図 38. Gate Driver Output (Zoomed)

注: CH1: PWM from controller, CH2: Gate driver output, CH3: 16-V supply

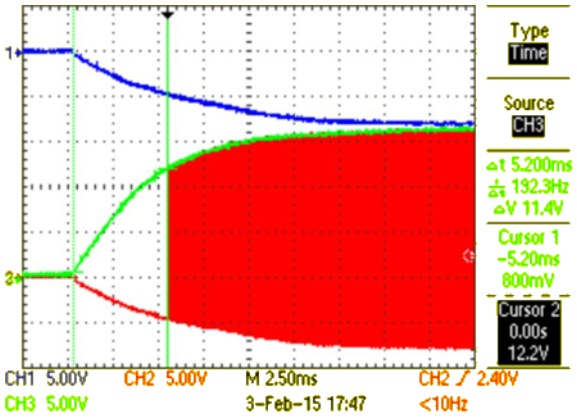


図 39. Gate Driver Output During Power ON With Bipolar Supply

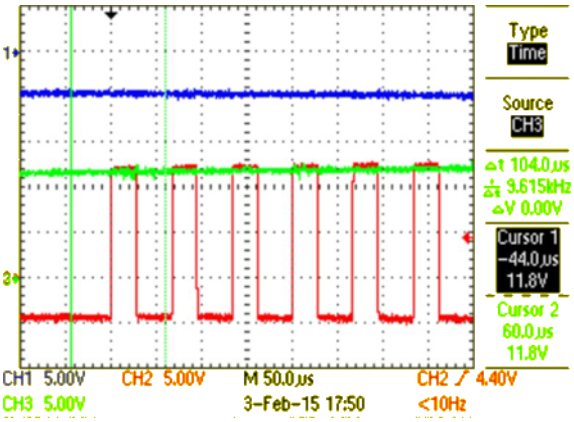


図 40. Gate Driver Output (Zoomed)

注: CH1: –8-V supply, CH2: Gate driver output, CH3: 16-V supply

7.3 Power ON Test With External BJT Buffer

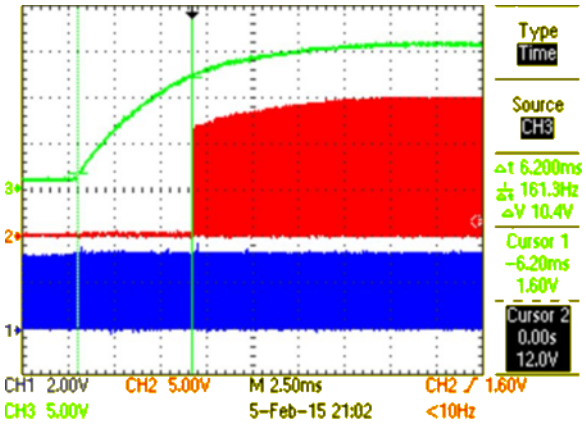


図 41. External BJT Buffer Output During Power ON With Unipolar Supply

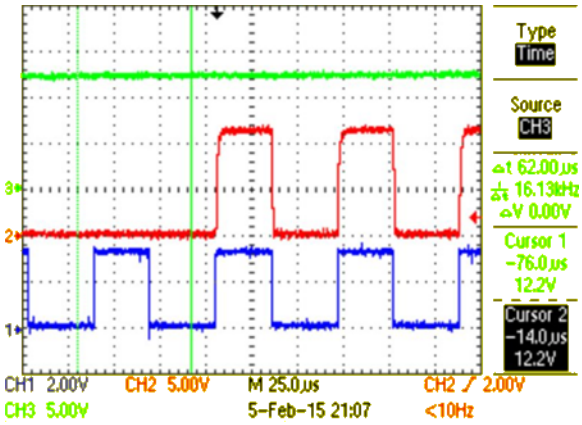


図 42. Gate Driver Output (Zoomed)

注: CH1: PWM from controller, CH2: Gate driver output, CH3: 16-V supply

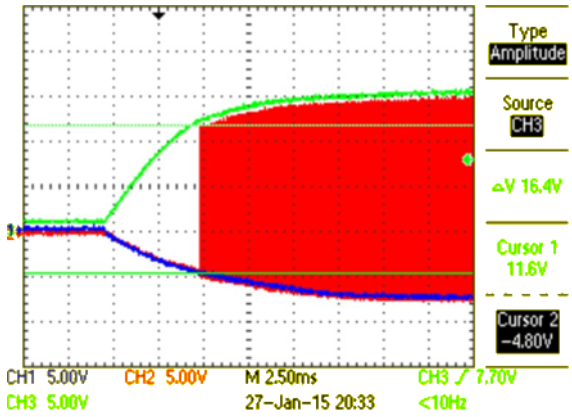


図 43. Gate Driver Output During Power ON With Bipolar Supply

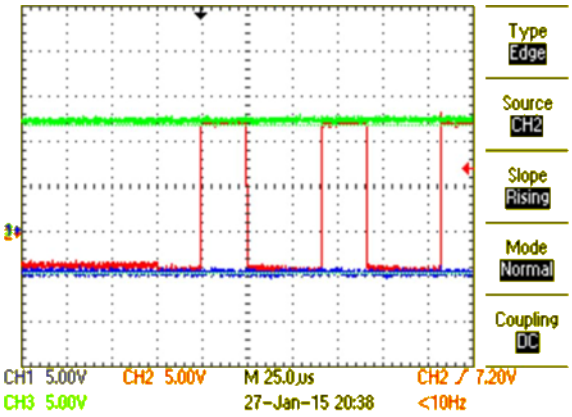


図 44. Gate Driver Output (Zoomed)

注: CH1: –8-V supply, CH2: Gate driver output, CH3: 16-V supply

7.4 2.5-A/5-A Sink and Source Current With Bipolar Supply Without BJT Buffer (Infineon Module)

図 45 through 図 47 show the sink and source currents delivered directly by ISO5852S.

Test conditions:

- $R_{G\ (ON)}$: 7.5 Ω
- $R_{G\ (OFF)}$: 0.0 Ω
- IGBT module: Infineon FS200R12KT4R_B11
- Gate charge (Q_G): 1.65 μC
- Internal resistance: 3.5 Ω
- Input capacitance Cies: 14 nF

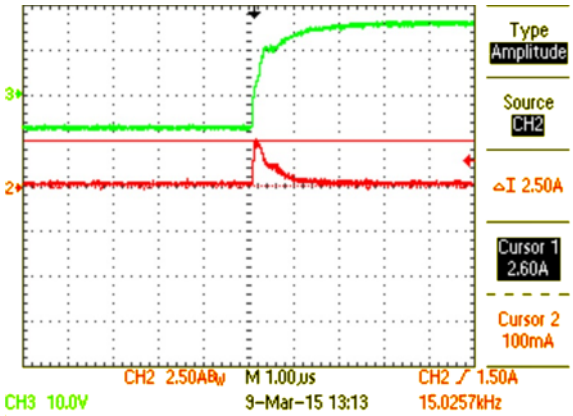


図 45. Gate Driver Output — 2.5-A Source Current

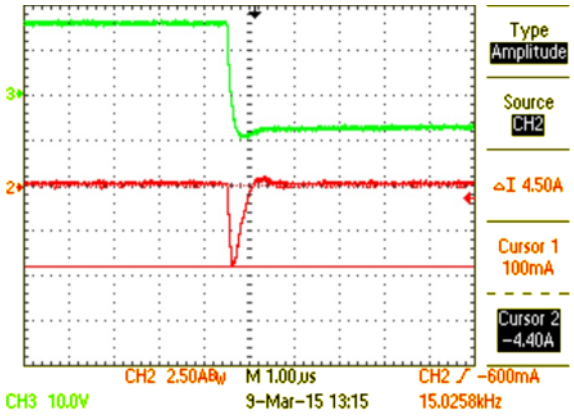


図 46. Gate Driver Output — 4.5-A Sink Current

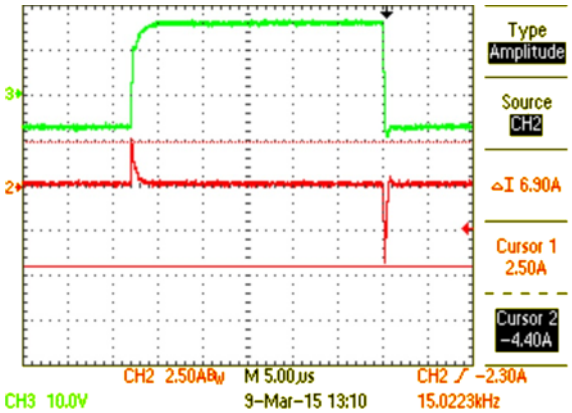


図 47. Source and Sink Current

注: CH2: Gate current, CH3: Gate driver output

7.5 PWM Signal Delay

7.5.1 and 7.5.2 show the propagation delay between the Piccolo controller and the gate driver.

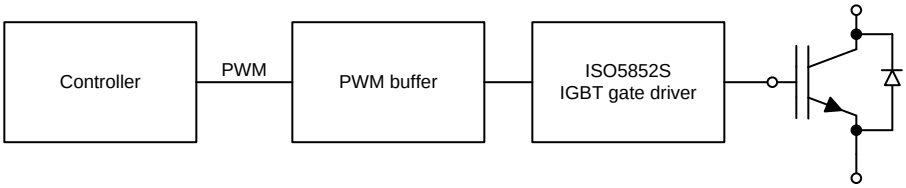


図 48. Piccolo Controller and Gate Driver Diagram

7.5.1 Delay Between PWM Buffer Input and PWM Buffer Output

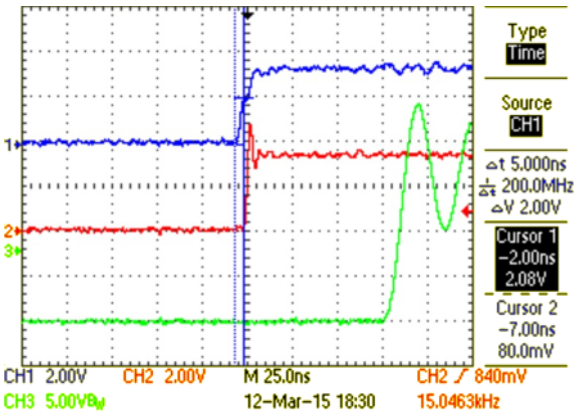


図 49. Propagation Delay of PWM Buffer (R-Top) (Rising Edge)

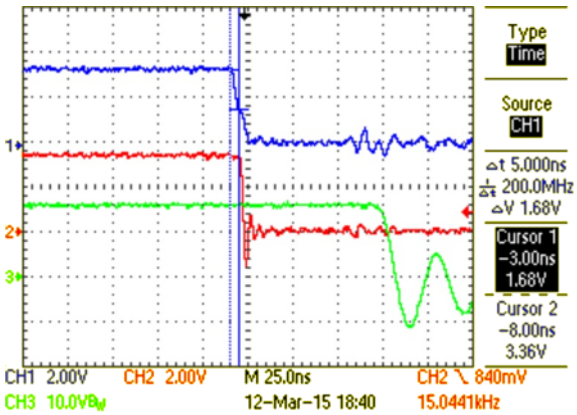


図 50. Propagation Delay of PWM Buffer (R-Top) (Falling Edge)

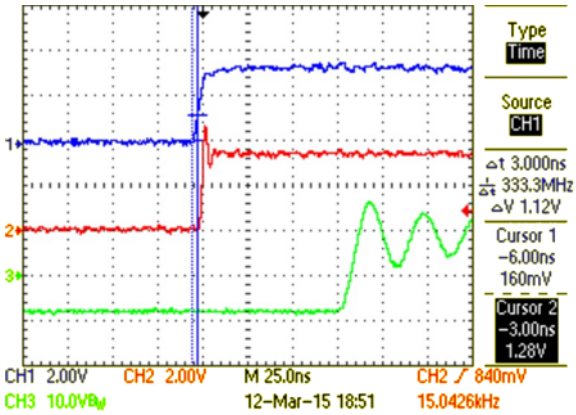


図 51. Propagation Delay of PWM Buffer (R-Bot) (Rising Edge)

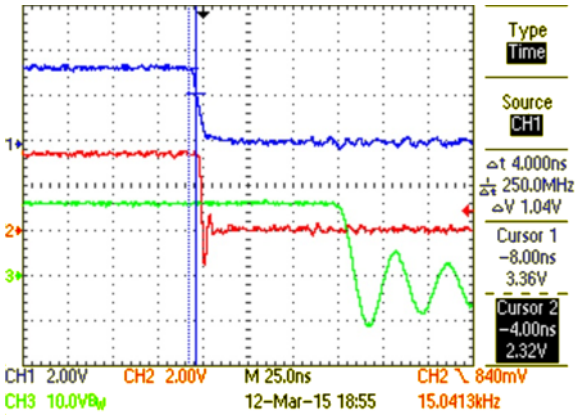


図 52. Propagation Delay of PWM Buffer (R-Bot) (Falling Edge)

注: CH1: PWM from controller, CH2: PWM buffer output, CH3: Current buffer output

表 6. Delay Between PWM Signals

PWM BUFFER INPUT AND PWM BUFFER OUTPUT	TIME (ns)
R_Top (Rising)	5.0
R_Top (Falling)	5.0
R_Bottom (Rising)	3.0
R_Bottom (Falling)	4.0

7.5.2 Delay Between PWM Buffer Input and Gate Driver Output

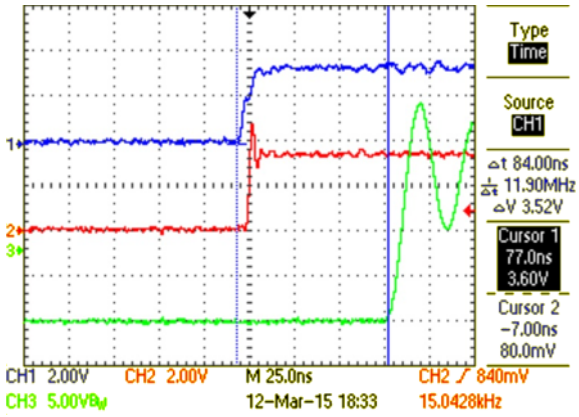


図 53. Gate Driver Propagation Delay R_Top (Rising)

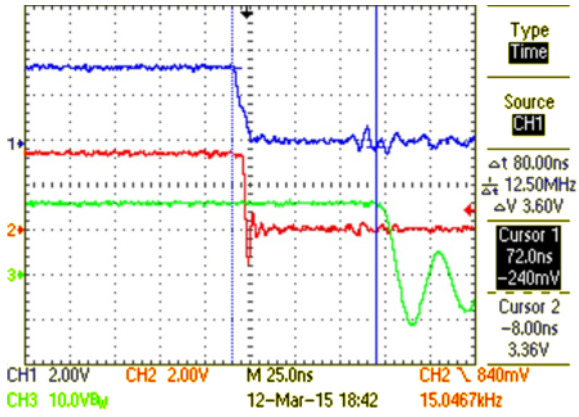


図 54. Gate Driver Propagation Delay R_Top (Falling)

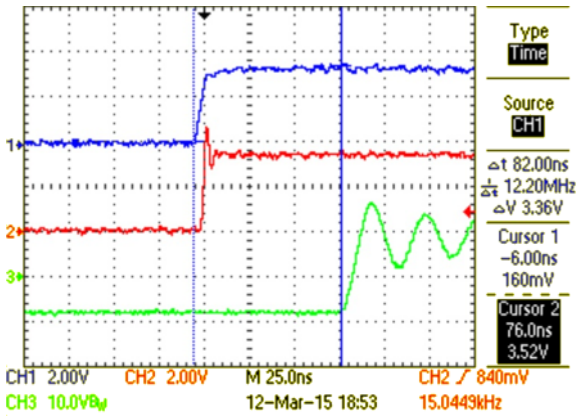


図 55. Gate Driver Propagation Delay R_Bottom (Rising)

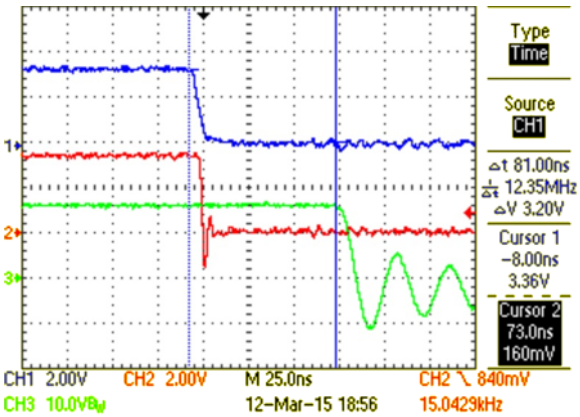


図 56. Gate Driver Propagation Delay R_Bottom (Falling)

注: CH1: PWM from controller, CH2: PWM buffer output, CH3: Current buffer output

表 7. Delay Between PWM Signals

PWM BUFFER INPUT AND GATE DRIVER OUTPUT	TIME (ns)
R_Top (Rising)	84.0
R_Top (Falling)	80.0
R_Bottom (Rising)	82.0
R_Bottom (Falling)	81.0

7.6 Induced Voltage at Gate for dV/dt of 2.5 kV/µs With 10-m Motor Cable

7.6.1 Active Miller Clamp Disabled

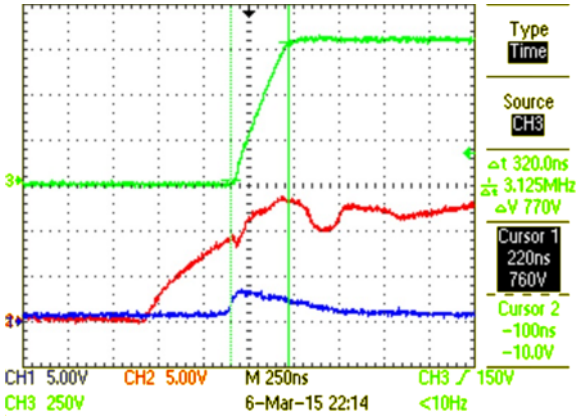


図 57. 2.5-kV/µs Inverter dV/dt

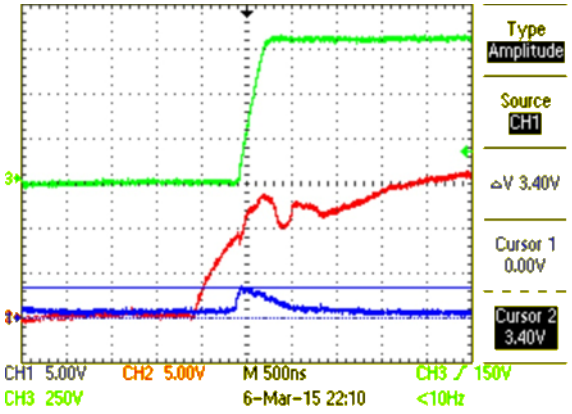


図 58. Induced Voltage at 2.5-kV/µs dV/dt

注: 2.5-kV/µs inverter output and induced voltage at the gate of bottom IGBT with active miller clamp disabled and $C_{ge(Ext)}$ **= 0 nF**

CH1: Bottom gate driver output, CH2: Top gate driver output, CH3: Vce of bottom IGBT

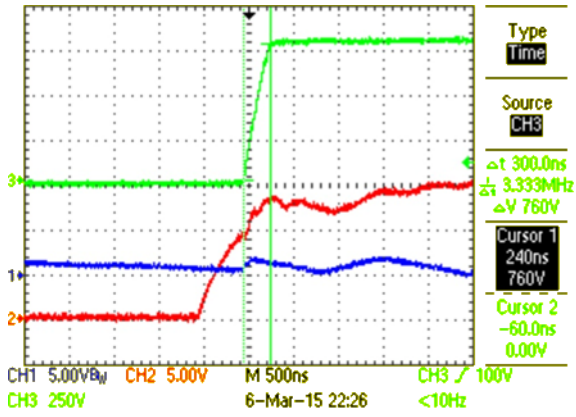


図 59. 2.5-kV/µs Inverter dV/dt

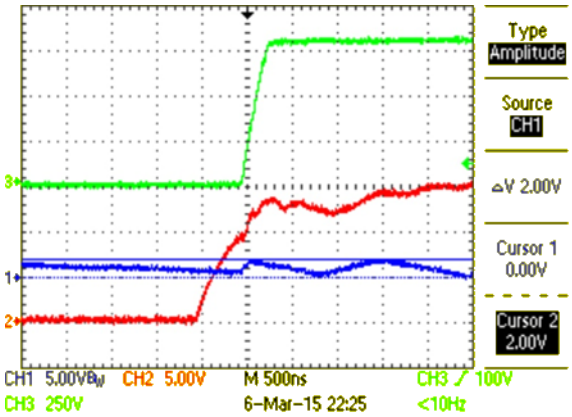


図 60. Induced Voltage at 2.5-kV/µs dV/dt

注: 2.5-kV/µs inverter output and induced voltage at gate of bottom IGBT with active miller clamp disabled and $C_{ge(Ext)}$ **= 10 nF**

CH1: Bottom gate driver output, CH2: Top gate driver output, CH3: Vce of bottom IGBT

表 8. Summary of Induced Voltage for 2.5-kV/µS dV/dt (Active Miller Clamp Disabled)

TEST CONDITIONS	INDUCED VOLTAGE AT THE BOTTOM IGBT (POSITIVE PEAK IN VOLTS)
Active Miller clamp disabled Cge(Ext)=0nF	3.4
Active Miller clamp disabled Cge(Ext)=10nF	2

7.6.2 Active Miller Clamp Enabled

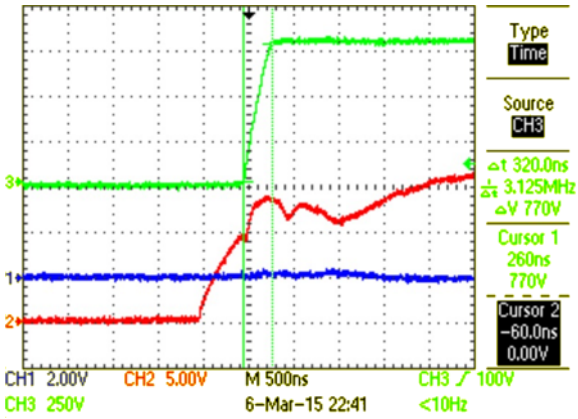


図 61. 2.5-kV/µs Inverter dV/dt

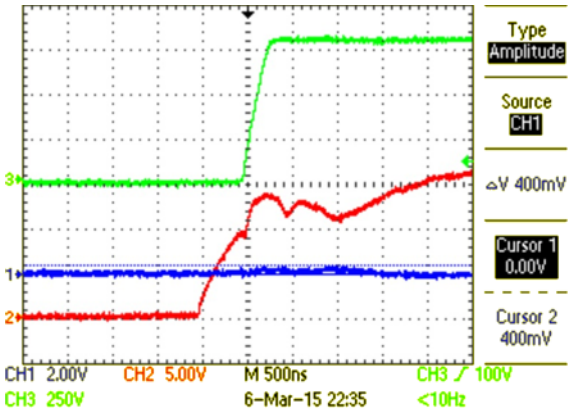


図 62. Induced Voltage at 2.5-kV/µs dV/dt

注: 2.5-kV/µs inverter output and induced voltage at the gate of bottom IGBT with active miller clamp enabled and **$C_{ge(Ext)}$ = 0 nF**

CH1: Bottom gate driver output, CH2: Top gate driver output, CH3: Vce of bottom IGBT

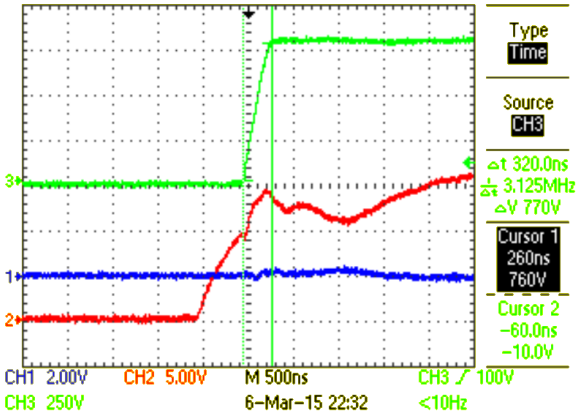


図 63. 2.5-kV/µs Inverter dV/dt

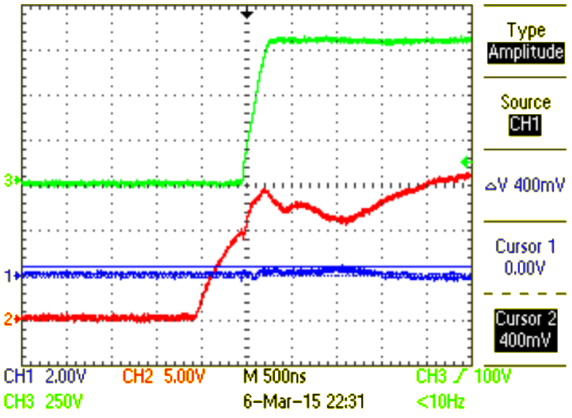


図 64. Induced Voltage at 2.5-kV/µs dV/dt

注: 2.5-kV/µs inverter output and induced voltage at gate of bottom IGBT with active miller clamp enabled and **$C_{ge(Ext)}$ = 10 nF**

CH1: Bottom gate driver output, CH2: Top gate driver output, CH3: Vce of bottom IGBT

表 9. Summary of Induced Voltage for 2.5-kV/µs dV/dt (Active Miller Clamp Enabled)

TEST CONDITIONS	INDUCED VOLTAGE AT THE BOTTOM IGBT (POSITIVE PEAK IN VOLTS)
Active Miller clamp enabled. $C_{ge(Ext)}$ = 0 nF	0.4
Active Miller clamp enabled $C_{ge(Ext)}$ = 10 nF	0.4

7.7 Induced Voltage at Gate for dV/dt of 5 kV/µs With 10-m Motor Cable

7.7.1 Active Miller Clamp Disabled

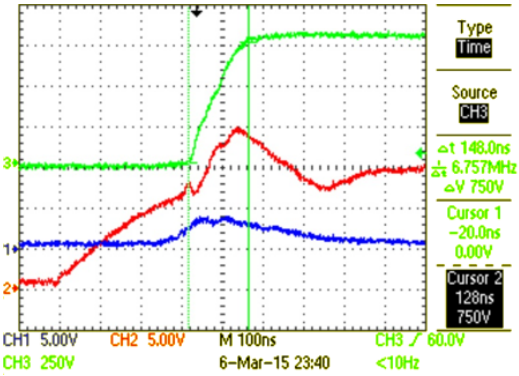


図 65. 5-kV/µs Inverter dV/dt

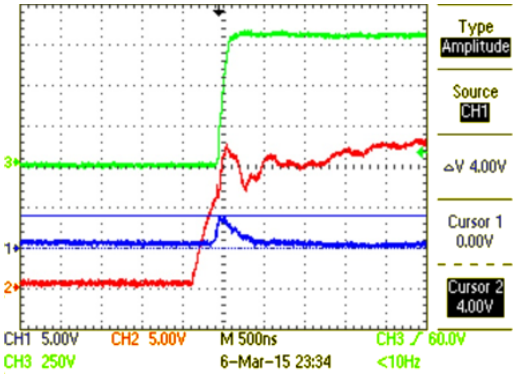


図 66. Induced Voltage at 5-kV/µs dV/dt

注: 5-kV/µs inverter output and induced voltage at the gate of bottom IGBT with active miller clamp disabled and **$C_{ge(Ext)}$ = 0 nF**

CH1: Bottom gate driver output, CH2: Top gate driver output, CH3: Vce of bottom IGBT

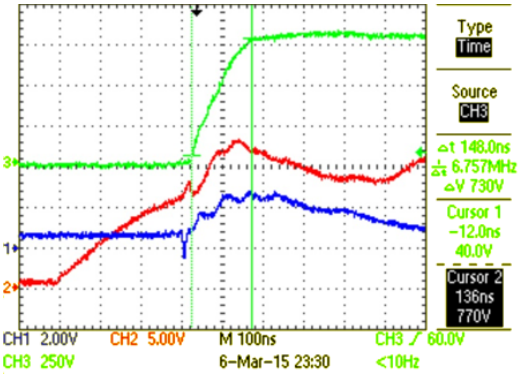


図 67. 5-kV/µs Inverter dV/dt

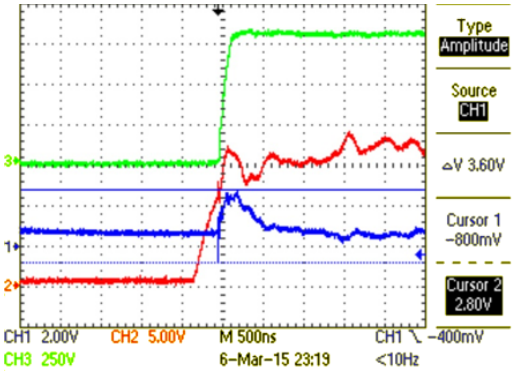


図 68. Induced Voltage at 5-kV/µs dV/dt

注: 5-kv/µs inverter output and induced voltage at the gate of bottom IGBT with active miller clamp disabled and **$C_{ge(Ext)}$ = 10 nF**

CH1: Bottom gate driver output, CH2: Top gate driver output, CH3: Vce of bottom IGBT

表 10. Summary of Induced Voltage for 5-kV/µs dV/dT (Active Miller Clamp Disabled)

TEST CONDITIONS	INDUCED VOLTAGE AT THE BOTTOM IGBT (POSITIVE PEAK IN VOLTS)
Active Miller clamp disabled Cge(Ext)=0nF	4
Active Miller clamp disabled Cge(Ext)=10nF	2.8

7.7.2 Active Miller Clamp Enabled

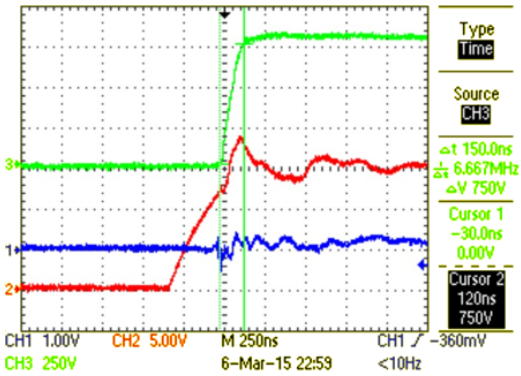


図 69. 5-kV/µs Inverter dV/dt

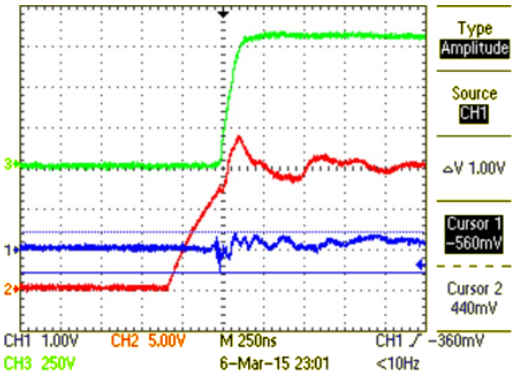


図 70. Induced Voltage at 5-kV/µs dV/dt

注: 5-kV/µs inverter output and induced voltage at the gate of bottom IGBT with active miller clamp enabled and **$C_{ge(Ext)}$ = 0 nF**

CH1: Bottom gate driver output, CH2: Top gate driver output, CH3: Vce of bottom IGBT

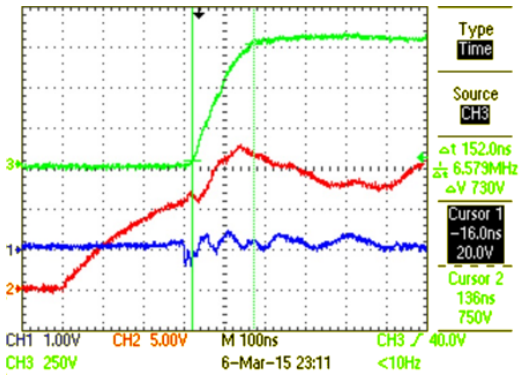


図 71. 5-kV/µs Inverter dV/dt

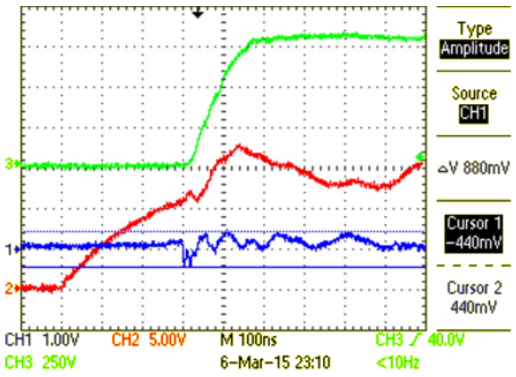


図 72. Induced Voltage at 5-kV/µs dV/dt

注: 5-kV/µs inverter output and induced voltage at the gate of bottom IGBT with active miller clamp enabled and **$C_{ge(Ext)}$ = 10 nF**

CH1: Bottom gate driver output, CH2: Top gate driver output, CH3: Vce of bottom IGBT

表 11. Summary of Induced Voltage for 5-kV/µs dV/dt (Active Miller Clamp Enabled)

TEST CONDITIONS	INDUCED VOLTAGE AT THE BOTTOM IGBT (POSITIVE PEAK IN VOLTS)
Active Miller clamp enabled $C_{ge(Ext)}$ = 0 nF	0.44
Active Miller clamp enabled $C_{ge(Ext)}$ = 10 nF	0.44

7.8 Induced Voltage at Gate for dV/dt of 7.5 kV/µs With 10-m Motor Cable

7.8.1 Active Miller Clamp Disabled

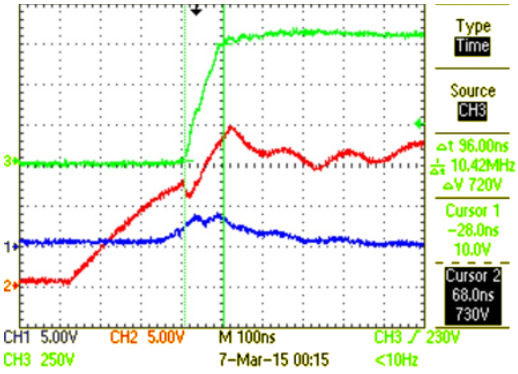


図 73. 7.5-kV/µs Inverter dV/dt

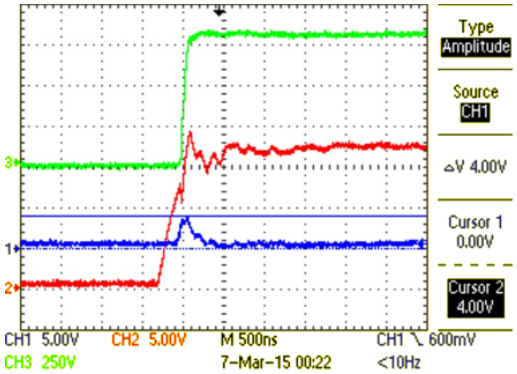


図 74. Induced Voltage at 7.5-kV/µs dV/dt

注: 7.5-kV/µs inverter output and induced voltage at the bottom IGBT - active miller clamp disabled and $C_{ge(Ext)}$ = 0 nF

CH1: Bottom gate driver output, CH2: Top gate driver output, CH3: Vce of bottom IGBT

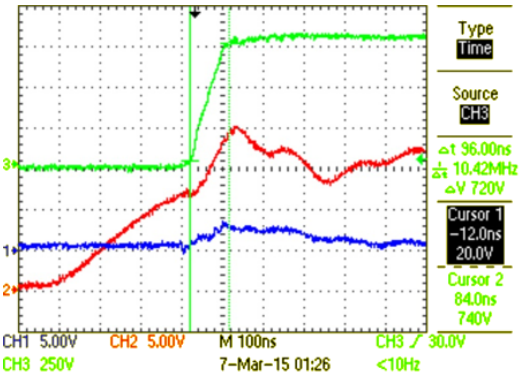


図 75. 7.5-kV/µs Inverter dV/dt

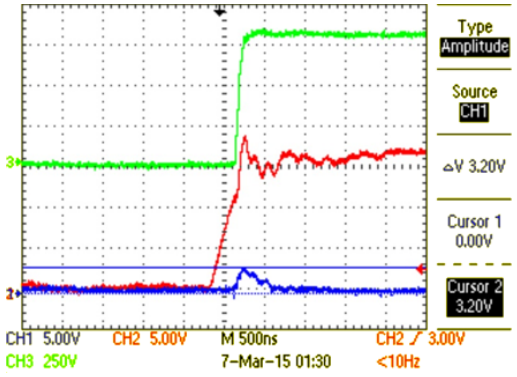


図 76. Induced Voltage at 7.5-kV/µs dV/dt

注: 7.5-kV/µs inverter output and induced voltage at the bottom IGBT with active miller clamp disabled and **$C_{ge(Ext)}$ = 10 nF**

CH1: Bottom gate driver output, CH2: Top gate driver output, CH3: Vce of bottom IGBT

表 12. Summary of Induced Voltage for 7.5-kV/µs dV/dt (Active Miller Clamp Disabled)

TEST CONDITIONS	INDUCED VOLTAGE AT THE BOTTOM IGBT (POSITIVE PEAK IN VOLTS)
Active Miller clamp disabled $C_{ge(Ext)}$ = 0 nF	4
Active Miller clamp disabled $C_{ge(Ext)}$ = 10 nF	3.2

7.8.2 Active Miller Clamp Enabled

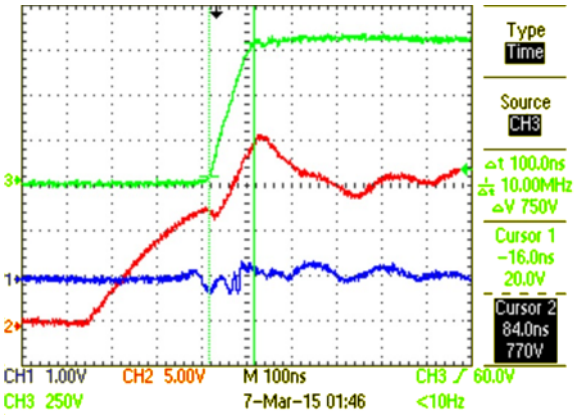


図 77. 7.5-kV/µs Inverter dV/dt

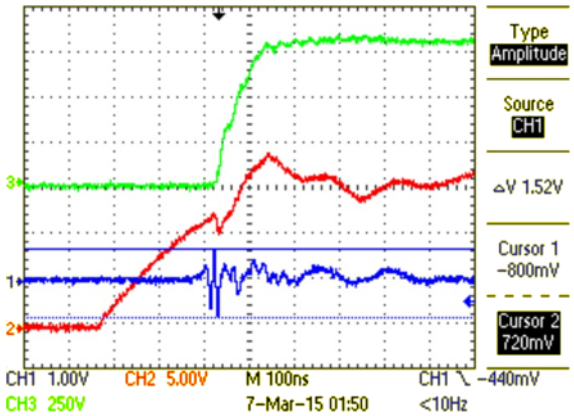


図 78. Induced Voltage at 7.5-kV/µs dV/dt

注: 7.5-kV/µs inverter output and induced voltage at the gate of bottom IGBT with active miller clamp enabled and **$C_{ge(Ext)}$ = 0 nF**

CH1: Bottom gate driver output, CH2: Top gate driver output, CH3: Vce of bottom IGBT

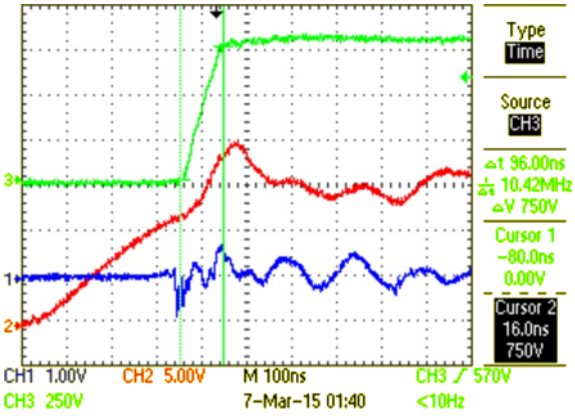


図 79. 7.5-kV/µs Inverter dV/dt

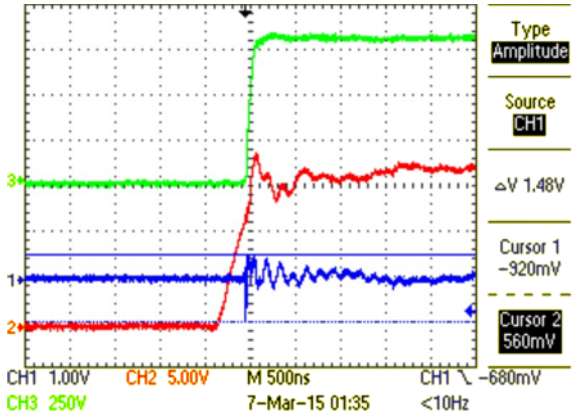


図 80. Induced Voltage at 7.5-kV/µs dV/dt

注: 7.5-kV/µs inverter output and induced voltage at the gate of bottom IGBT - active miller clamp enabled and $C_{ge(Ext)}$ = 10 nF

CH1: Bottom gate driver output, CH2: Top gate driver output, CH3: Vce of bottom IGBT

表 13. Summary of Induced Voltage for 7.5-kV/µs dV/dt (Active Miller Clamp Enabled)

TEST CONDITIONS	INDUCED VOLTAGE AT THE BOTTOM IGBT (POSITIVE PEAK IN VOLTS)
Active Miller clamp enabled $C_{ge(Ext)}$ = 0 nF	0.72
Active Miller clamp enabled $C_{ge(Ext)}$ = 10 nF	0.56

7.9 Maximum Achievable dV/dt Without External BJT Buffer

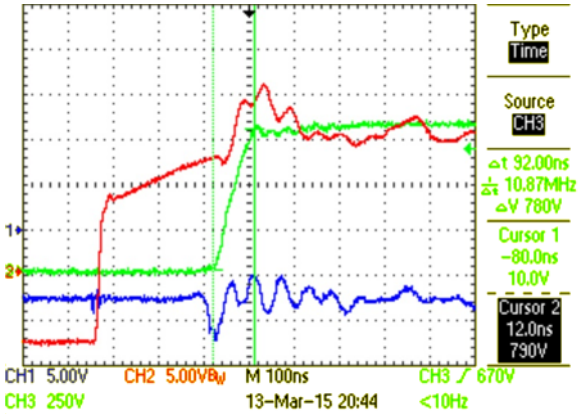


図 81. Max dV/dt and Induced Voltage Without External Buffer With 10-m Motor Cable (Bipolar)

注: CH1: Bottom gate driver output, CH2: Top gate driver output, CH3: Vce of bottom IGBT

Maximum dV/dt achieved without external BJT buffer: 8.47 kV/μs

Test conditions:

- $R_{G\ (ON)}$: 2.2 Ω
- $R_{G\ (OFF)}$: 2.2 Ω
- IGBT module: CM150TX-24S1_MITSUBISHI
- Gate charge (Q_G): 315 nC
- Internal resistance: 13 Ω
- Input capacitance C_{IES}: 15 nF

7.10 Current Through Clamp Pin

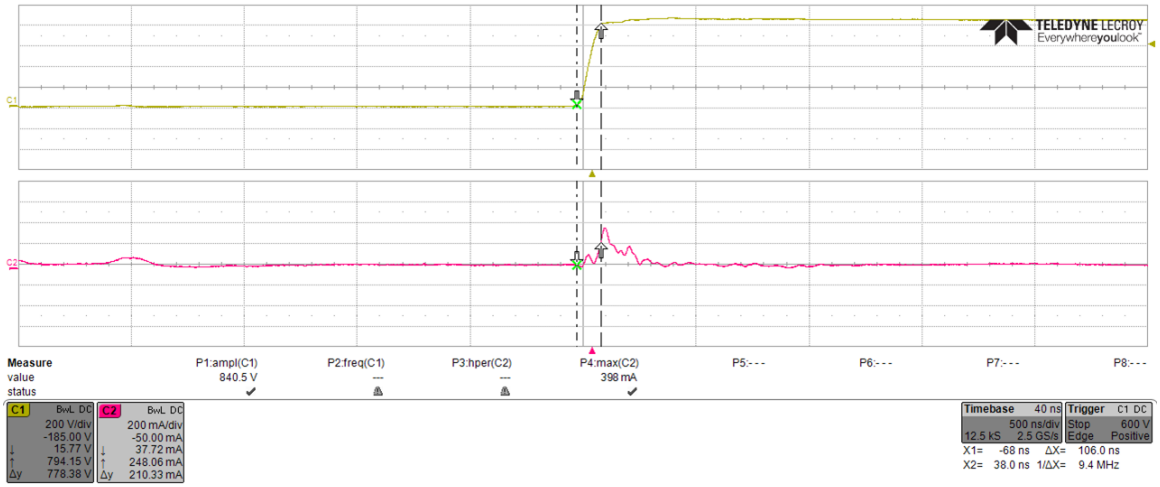


図 82. Current Through Clamp Pin

Test conditions:

- External buffer: without BJT
- Supply: Unipolar
- $R_{G\ (ON)}$: 2.2 Ω
- $R_{G\ (OFF)}$: 2.2 Ω
- IGBT module: CM150TX-24S1_MITSUBISHI
- Gate charge (Q_G): 315 nC
- Internal resistance: 13 Ω
- Input capacitance C_{IES}: 15 nF

7.11 Validation of Gate Signals With External Cable (Without BJT Buffer)

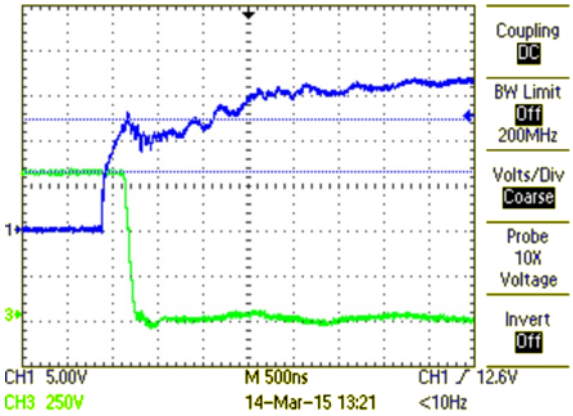


図 83. Gate signal at Gate of IGBT With 100-cm External Cable

注: CH1: Gate driver output, CH3: Vce of bottom IGBT

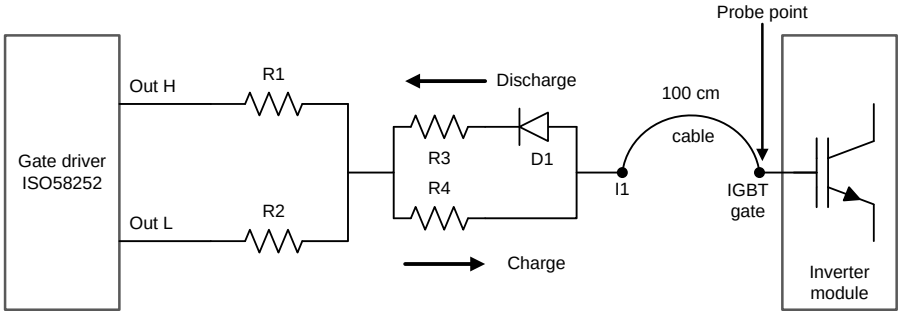


図 84. Block Diagram for Measurement of Gate Signal With External Cable

7.12 DESAT Signal During Normal Operation

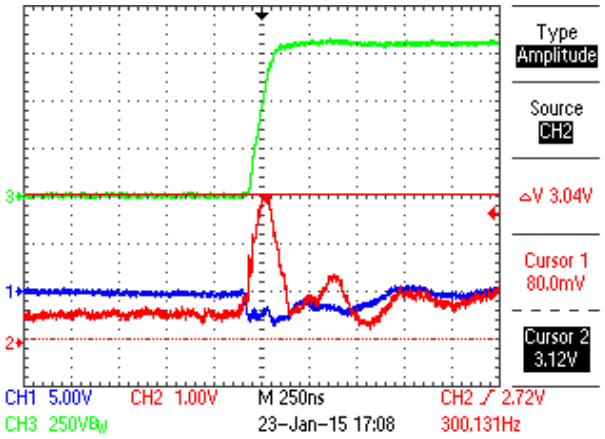


図 85. DESAT During Normal Operation (Zoomed)

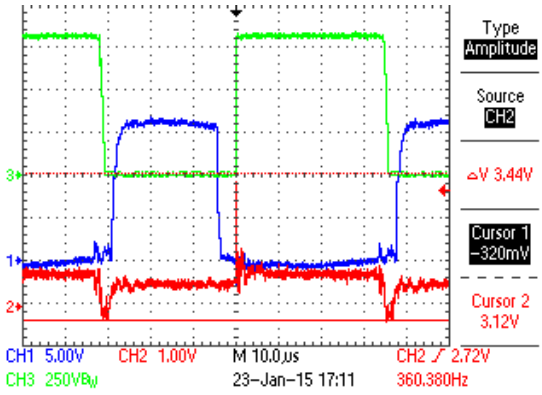


図 86. DESAT During Normal Operation

注: CH1: Bottom gate driver output, CH2: DESAT signal, CH3: Vce of bottom IGBT

7.13 Short Circuit Test — Hard Switched

注: All the tests in 7.13 and 7.14 were performed using engineering samples of ISO5852S. The final silicon has a higher pulldown drive during soft shutdown when compared to the engineering samples, resulting in lower soft shutdown time for given Qg of the IGBT die. Refer to the latest datasheet of ISO5852S on TI Website at http://www.ti.com/product/ISO5852S

図 87 shows the block diagram of hard-switched fault setup.

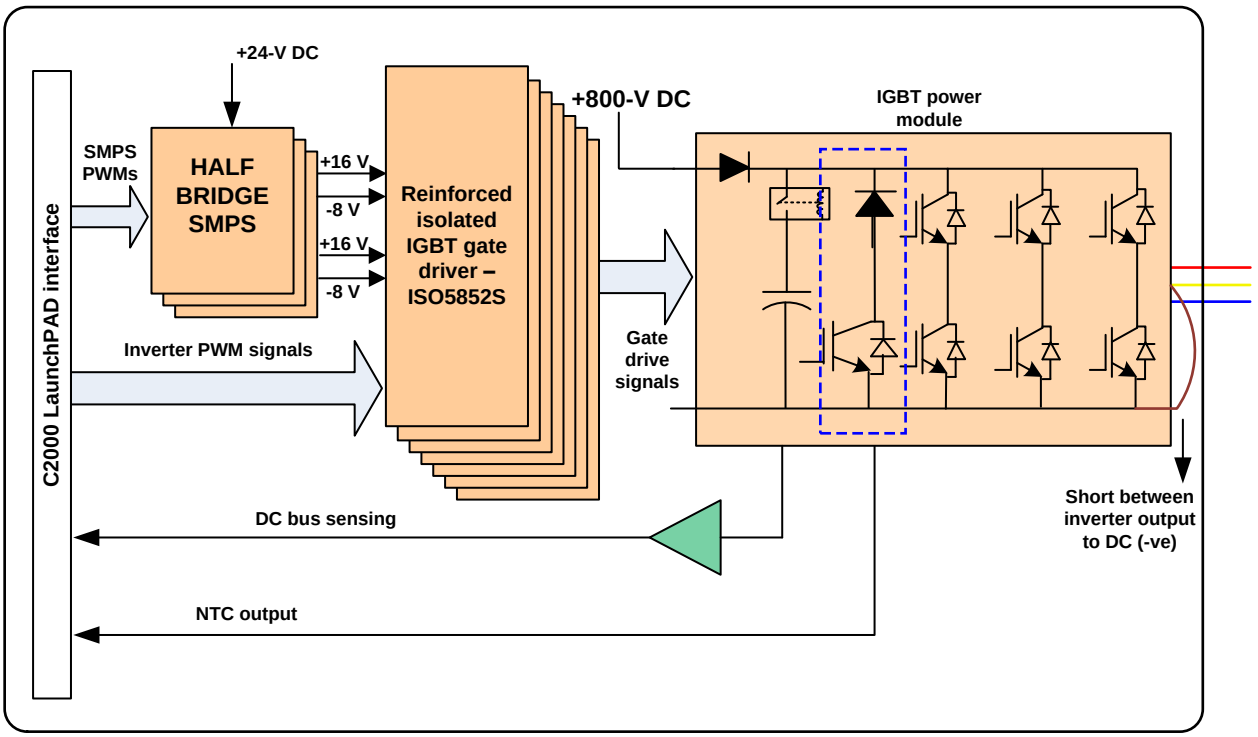


図 87. Block Diagram of Short Circuit Setup (Hard Fault Switch)

A hard fault switch short circuit test was performed using the power module CM150TX-24S1_MITSUBISHI. This test is performed such that one arm of the inverter bottom IGBT already has a short (from 図 87, Y phase output is connected to DC negative), during the same turning ON the top IGBT (Y_Top) to know the performance of DESAT detection.

Test conditions:

- Short circuit connection: Y-phase inverter output to DC negative
- Motor connected: NO
- Inverter dV/dT: 2.5 kV/µs, 5 kV/µs, 7.5 kV/µs
- IGBT module: CM150TX-24S1_MITSUBISHI
- Gate charge (Q_G): 315 nC
- Internal resistance: 13 Ω
- Input capacitance C_{IES}: 15 nF

7.13.1 Hard Switched Fault With Inverter dV/dt of 2.5kV/µs

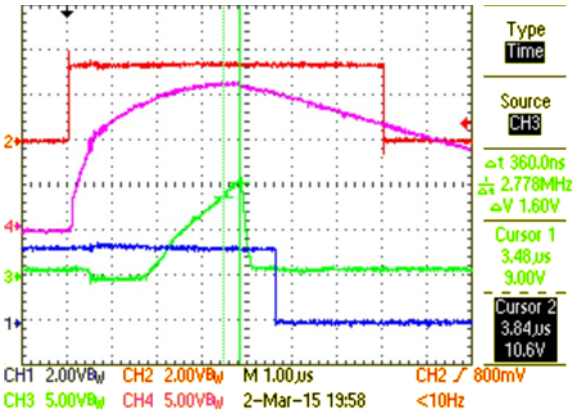


図 88. DESAT Activation to Gate Driver Turn OFF

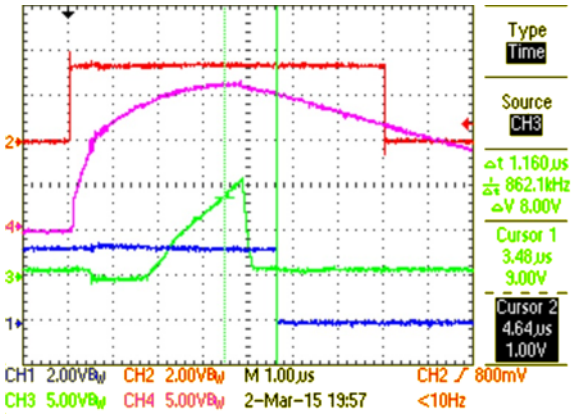


図 89. DESAT Activation to Fault Indication

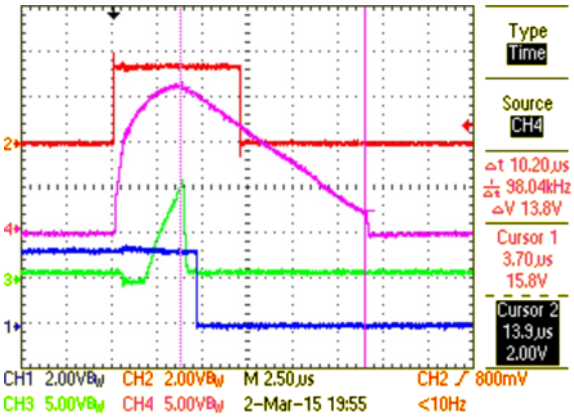


図 90. Gate Driver Output During Soft Shutdown

注: CH1: Fault signal, CH2: PWM from Controller, CH3: DESAT signal, CH4: Gate driver output

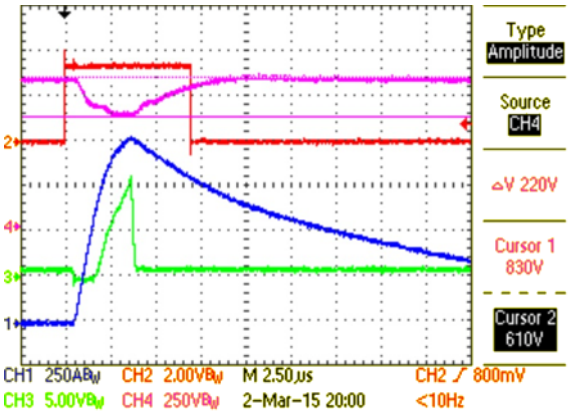


図 91. Voltage Across (Vce) Top IGBT

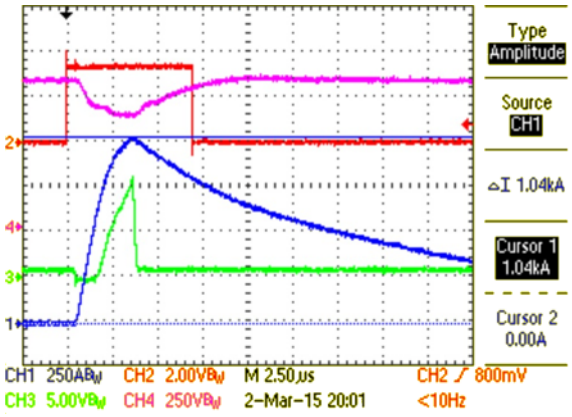


図 92. I_c — During Short circuit

注: CH1: Short circuit current, CH2: PWM from Controller, CH3: DESAT signal, CH4: Vce of top IGBT

表 14. Summary of Short Circuit Test of Hard Switched Fault with 2.5 kV/µs

PARAMETER	VALUE
DESAT activation to gate driver turn OFF	360.0 ns
DESAT activation to Fault indication	1.16 µs
Soft shutdown time	10.2 µs
Short circuit current	1.04 kA
Dip in Vce	220 V

7.13.2 Hard Switched Fault With Inverter dV/dt of 5 kV/µs

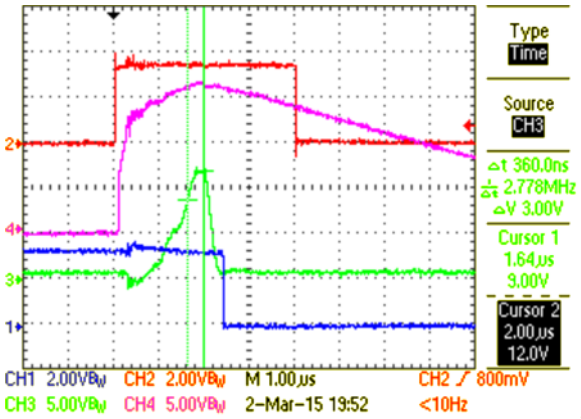


図 93. DESAT Activation to Gate Driver Turn OFF

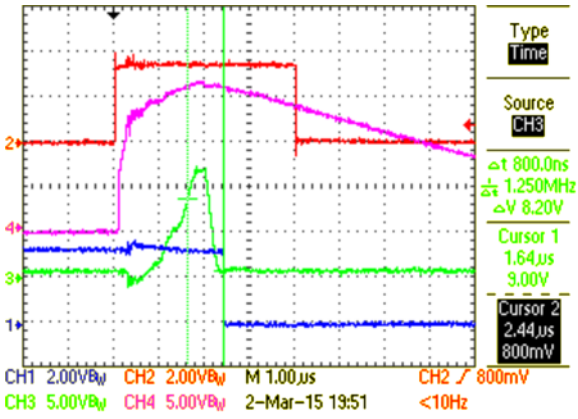


図 94. DESAT Activation to Fault Indication

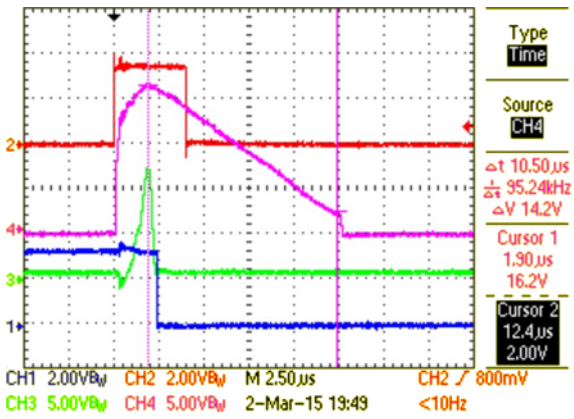


図 95. Gate Driver Output During Soft Shutdown

注: CH1: Fault signal, CH2: PWM from Controller, CH3: DESAT signal, CH4: Gate driver output

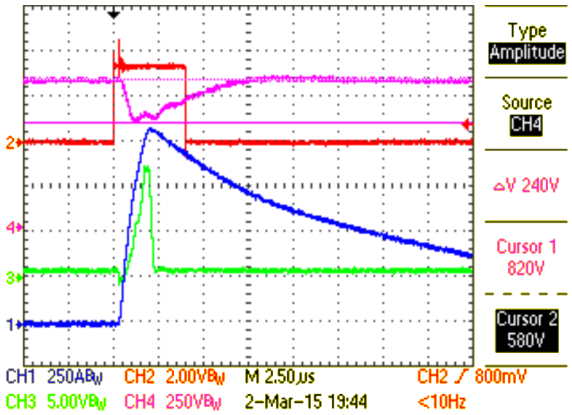


図 96. Voltage Across (Vce) Top IGBT and I_{C-} During Short Circuit

注: CH1: Short circuit current, CH2: PWM from Controller, CH3: DESAT signal, CH4: Vce of top IGBT

表 15. Summary of Short Circuit Test of Hard Switched Fault with 5 kV/µs

PARAMETER	VALUE
DESAT activation time to gate driver turn OFF	360 ns
DESAT activation to fault output	800 ns
Soft shutdown time	10.5 µs
Short circuit current	1.05 kA
Dip in Vce	240 V

7.13.3 Hard Switched Fault With Inverter dV/dt of 7.5 kV/µs

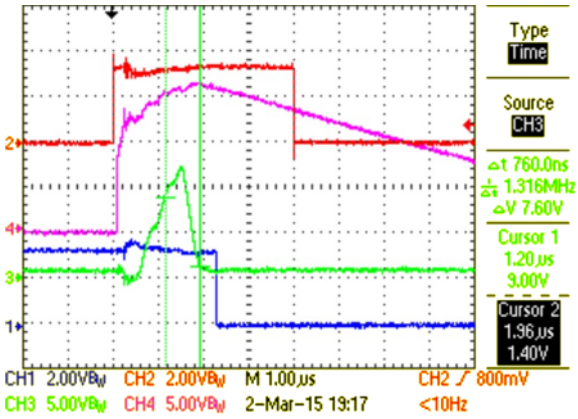


図 97. DESAT Activation to Gate Driver Turn OFF

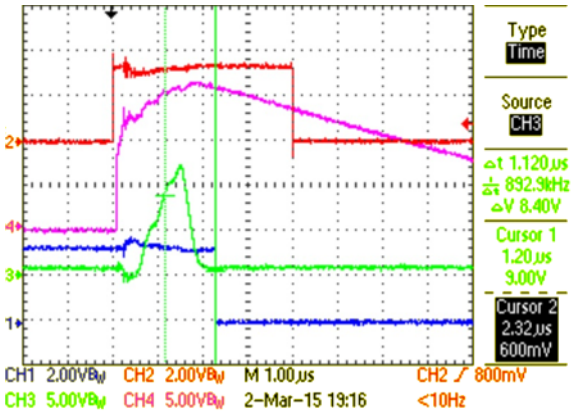


図 98. DESAT Activation to Fault Indication

注: CH1: Fault signal, CH2: PWM from Controller, CH3: DESAT signal, CH4: Gate driver output

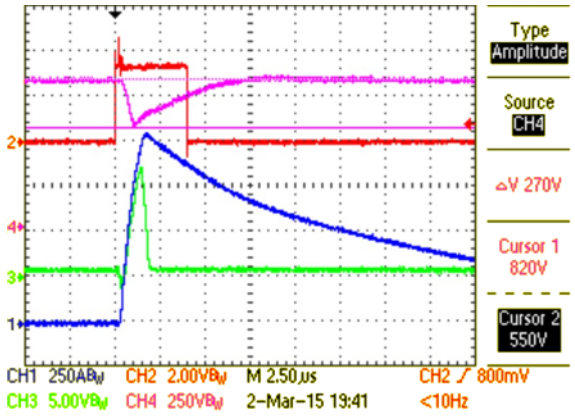


図 99. Voltage Across (Vce) Top IGBT

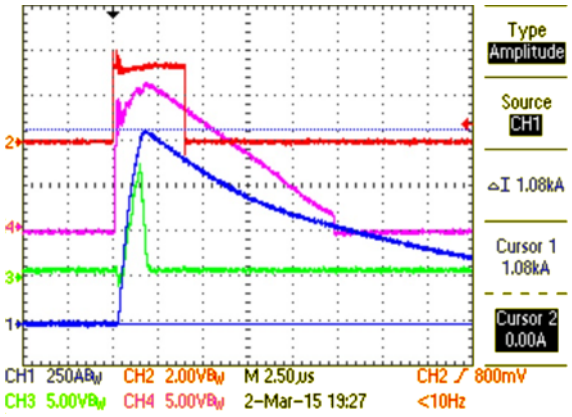


図 100. I_{C-} During Short Circuit

注: CH1: Short circuit current, CH2: PWM from Controller, CH3: DESAT signal, CH4: Vce of top IGBT

表 16. Summary of Short Circuit Test of Hard Switched Fault with 7.5 kV/µs

PARAMETER	VALUE
DESAT activation to gate driver turn OFF	760 ns
DESAT activation to fault	1.12 µs
Soft shutdown time	10 µs
Short circuit current	1.08 kA
Dip in Vce	270 V

7.14 Short Circuit Test — Fault Under Load

A fault under load short circuit test was performed using the power module CM150TX-4S1_MITSUBISHI. This test is conducted using a add on module for the short circuit consisting of high power IGBT connected between one of the phase output to DC negative. Refer 図 101 for the test setup.

図 101. Setup for Short Circuit Test — Fault Under Load

7.14.1 Fault Under Load Short Between Phase to DC –ve for 2.5-kV/µs Inverter Output

Test conditions:

- Short circuit connection: R phase inverter output to DC negative
- Motor connected: Yes
- Inverter dV/dT: 2.5 kV/µs
- IGBT module: CM150TX-24S1_MITSUBISHI
- Gate charge (Q_G): 315 nC
- Internal resistance: 13 Ω
- Input capacitance C_{IES}: 15 nF

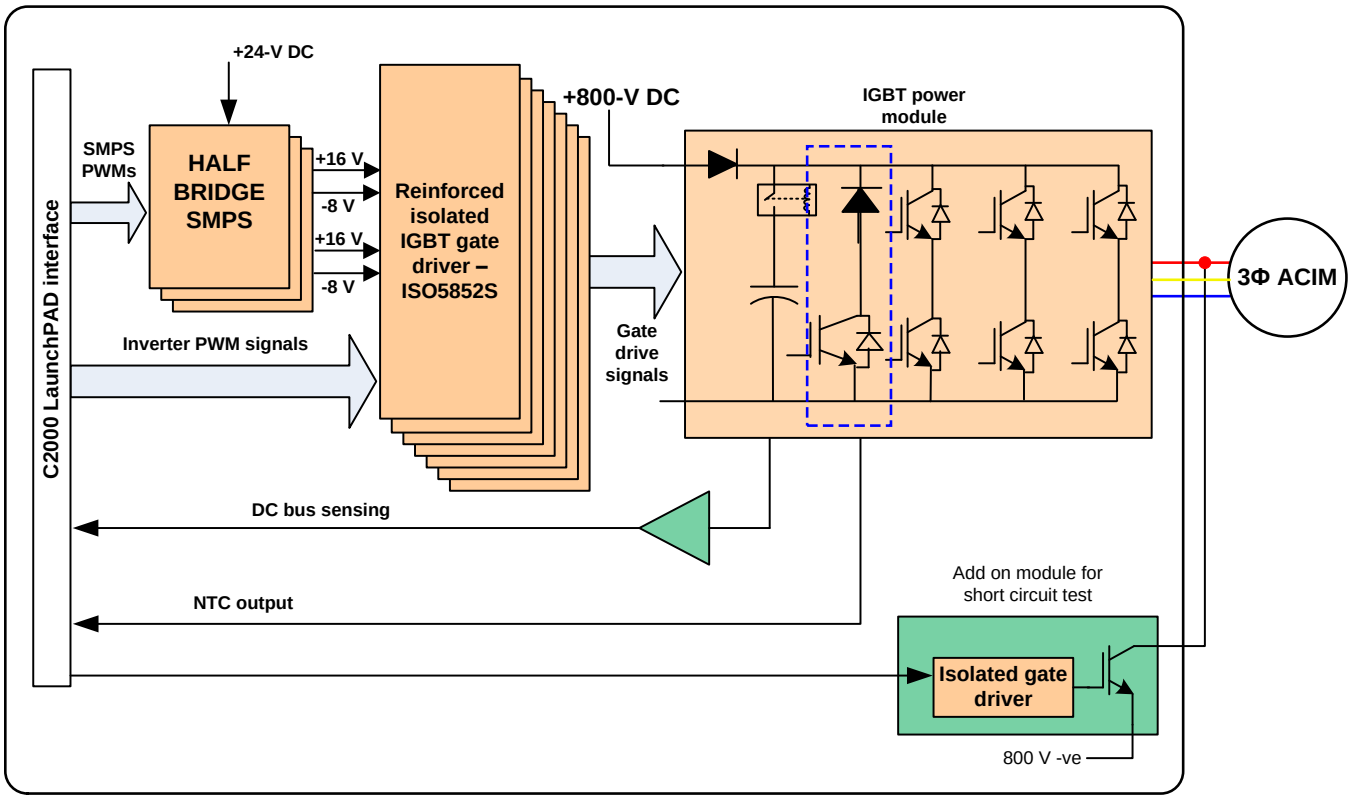


図 102. Block Diagram of Fault Under Load Test Short Between Phase to DC –ve

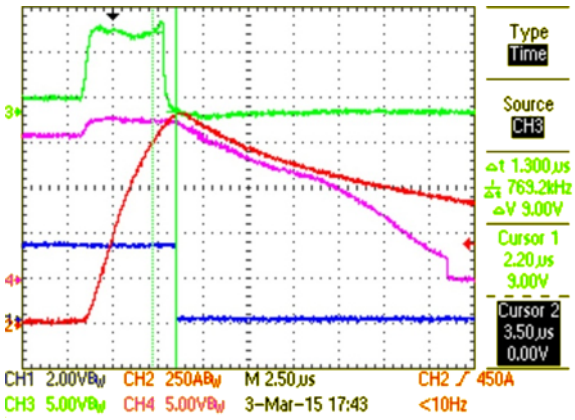


図 103. DESAT Activation to Fault Output

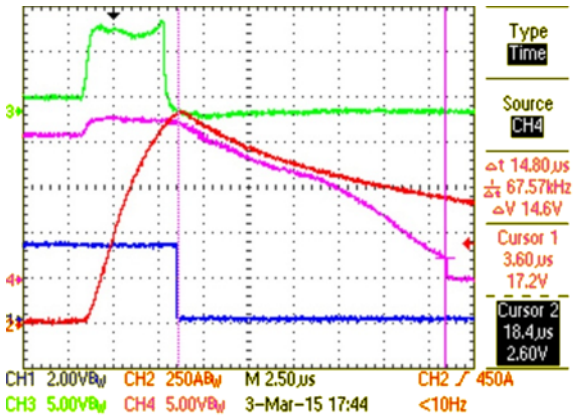


図 104. Gate Driver Output During Soft Shutdown

表 17. Summary of Short Circuit Test — Fault Under Load for 2.5 kV/µs (Phase Output to DC Negative)

PARAMETER	VALUE
DESAT activation to gate driver turn OFF	1.30 µs
Soft shutdown	14.80 µs

7.14.2 Fault Under Load — Short Circuit Between Phase to Phase

A fault under load short circuit test was performed using Mitsubishi power module CM150TX-24S1. This test is conducted using a add-on module for the short circuit consisting of high-power IGBT connected between R_phase and Y_phase of inverter output (see 図 105).

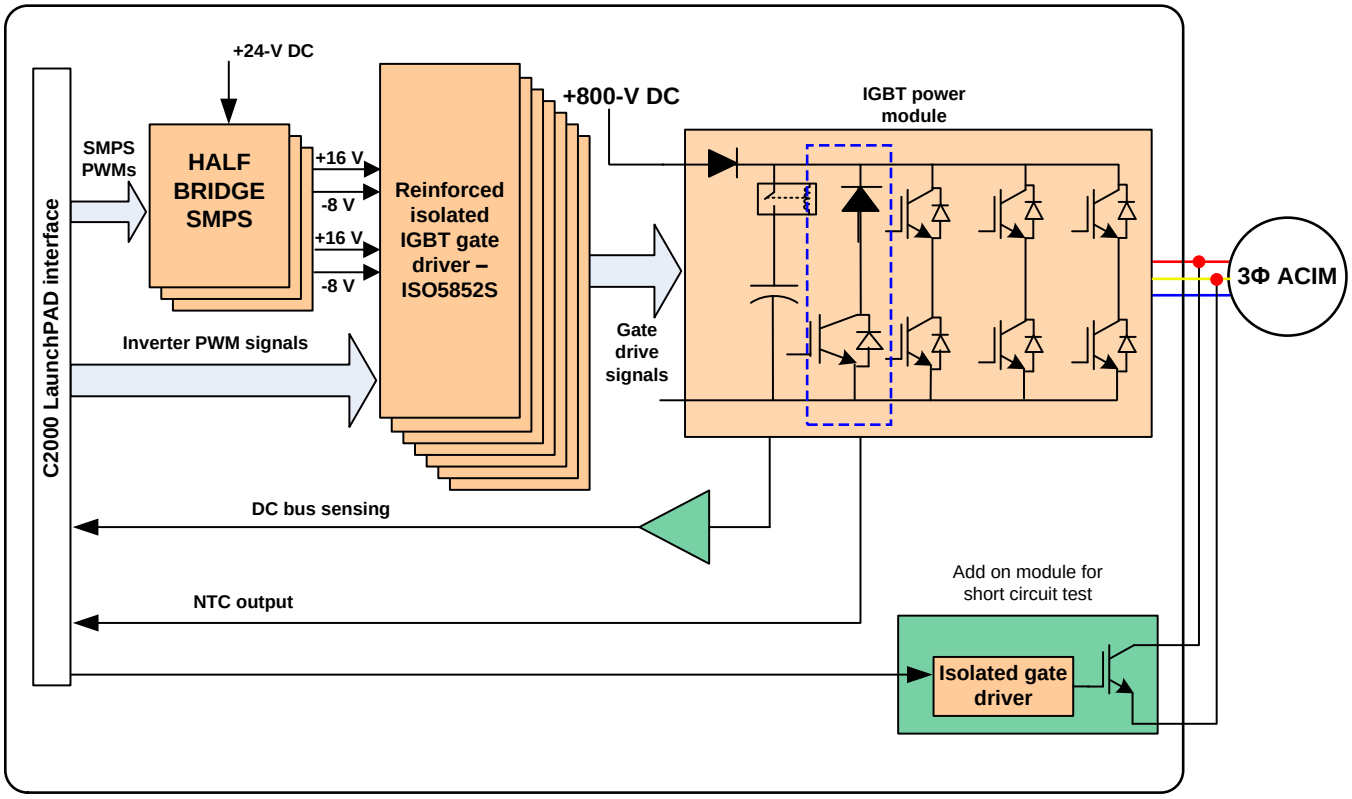


図 105. Block Diagram of Fault Under Load Test — Phase-to-Phase Short (dV/dt: 2.5 kV/µs)

Test conditions:

- Short circuit connection: Between R_phase and Y_phase
- Motor connected: Yes
- Inverter dV/dT: 2.5 kV/µs
- Cable length: 10 meters
- IGBT module: CM150TX-24S1_MITSUBISHI
- Gate charge (Q_G): 315 nC
- Internal resistance: 13 Ω
- Input capacitance C_{IES}: 15 nF

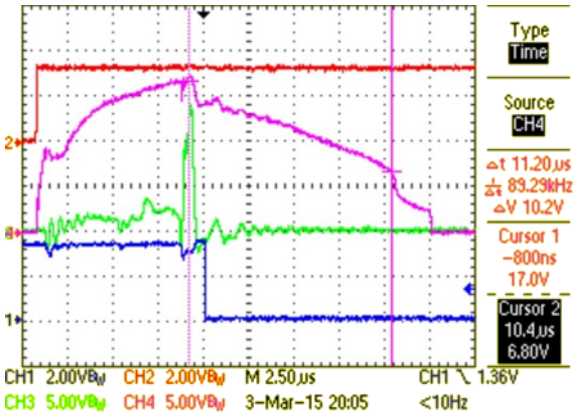


図 **106. Gate Driver Output During Soft Shutdown**

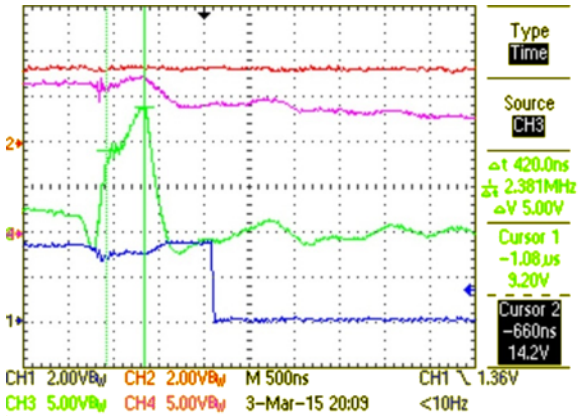


図 **107. DESAT Activation to Gate Driver Turn Off**

注: CH1: Fault signal, CH2:PWM from Controller, CH3: DESAT signal, CH4: Gate driver output

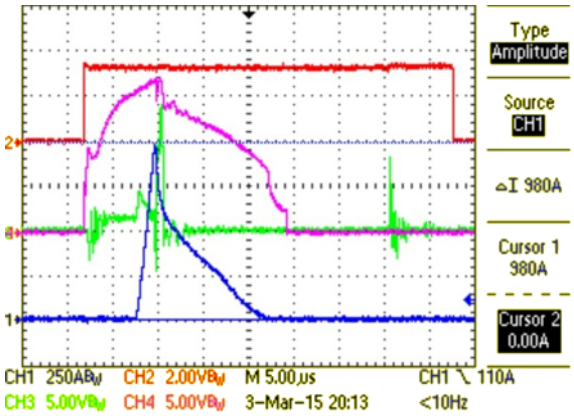


図 108. I_{C-} During Short Circuit Fault Under Load

注: CH1: Short circuit current, CH2: PWM from Controller, CH3: DESAT signal, CH4: Gate driver output

表 18. Summary of Short Circuit Test for Fault Under Load for 2.5 kV/µs (Phase-to-Phase Short)

PARAMETER	VALUE
DESAT activation to gate driver turn OFF	420.0 ns
Soft shutdown of gate driver output	11.20 µs
Peak current	980 A

7.15 EMC Test

7.15.1 Electrical Fast Transient (EFT) Test

EFT pulses were applied to motor cable using capacitive coupling clamp as per IEC 61000-4-4. This test was conducted for multiple levels of fast transient voltages (±1 kV, ±2 kV, ±3 kV, ±4 kV) at 5 kHz for duration of 60 seconds.

Different configurations used during testing are listed in 表 19:

表 19. EFT Test Configurations

TEST CONFIGURATION	MOTOR CABLE	UUT/AUX EQUIPMENT LOCATION	REFERENCE
1	Shielded	Ground plane	図 109
2	Shielded	10-cm isolated from plane	図 110
3	Unshielded	Ground plane	図 111
4	Unshielded	10-cm isolated from plane	図 112

Test setup:

- DC bus voltage: 400 V
- Auxiliary unit power rating: 2.2 kW
- Load condition: No load
- Motor rpm: 750 rpm
- Cable length: 10 meters
- EFT test equipment: emtest UCS 500N
- Capacitor coupling network

図 109. Test Configuration 1

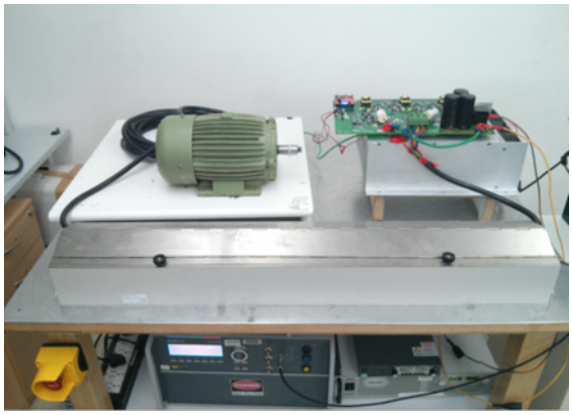


図 110. Test Configuration 2

図 111. Test Configuration 3

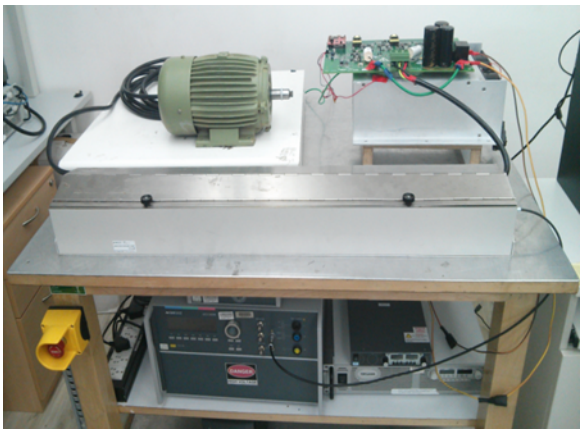


図 112. Test Configuration 4

表 20. EFT Test Results

EFT PULSES	DURATION	TEST RESULTS			
		Config:1	Config:2	Config:3	Config:4
1 kV	60 seconds	PASS	PASS	PASS	PASS
–1 kV	60 seconds	PASS	PASS	PASS	PASS
2 kV	60 seconds	PASS	PASS	PASS	PASS
–2 kV	60 seconds	PASS	PASS	PASS	PASS
3 kV	60 seconds	PASS	PASS	PASS	PASS
–3 kV	60 seconds	PASS	PASS	PASS	PASS
4 kV	60 seconds	PASS	PASS	PASS	PASS
–4 kV	60 seconds	PASS	PASS	PASS	PASS

Test pass refers to motor running continuously (without unusual sound) with no malfunctioning observed in the power stage (includes IGBT gate drivers), thereby meeting performance class B requirements as per IEC61800-3.

7.15.2 Electrostatic Discharge (ESD) Test

ESD pulses were applied (contact discharge) to the heat sink while the power stage was running the motor to check for malfunctions. CD was applied on the heat sink close to the IGBT gate drivers. ESD pulses were applied at multiple levels (±2 kV, ±4 kV, ±6 kV, ±8 kV) with 10 pulses on each polarity and level. IEC 61000-4-2 has been used as reference for the test method.

Different configurations used during testing are listed in 表 21:

表 21. ESD Test Configurations

TEST CONFIGURATION	UUT/AUX EQUIPMENT LOCATION	REFERENCE
1	Insulated sheet	図 113 and 図 114
2	Ground reference plane	図 116
3	10 cm isolated from reference	図 115

Test setup:

- DC bus voltage: 400 V
- Auxiliary unit power rating: 2.2 kW
- Load condition: No load
- Motor rpm: 750 rpm
- Cable length: 10 meters (Unshielded)
- ESD test equipment: emtest UCS 500N

表 22. ESD Test Results

ESD PULSES	DURATION	TEST RESULTS		
		Config:1	Config:2	Config:3
2 kV	10 pulses	PASS	PASS	PASS
–2 kV	10 pulses	PASS	PASS	PASS
4 kV	10 pulses	PASS	PASS	PASS
–4 kV	10 pulses	PASS	PASS	PASS
6 kV	10 pulses	PASS	PASS	PASS
–6 kV	10 pulses	PASS	PASS	PASS
8 kV	10 pulses	PASS	PASS	PASS
–8 kV	10 pulses	PASS	PASS	PASS

A test pass refers to the motor running continuously (without unusual sound) with no malfunctioning observed in the power stage (includes IGBT gate drivers), thereby meeting performance class B requirements as per IEC61800-3.

図 113. EUT/AUX Equipment on Insulated Sheet

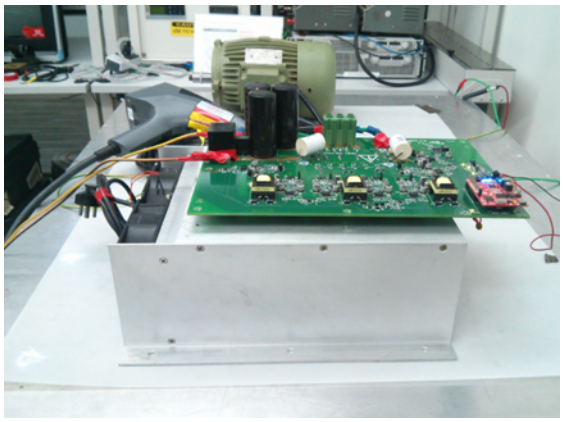


図 114. Test Configuration 1

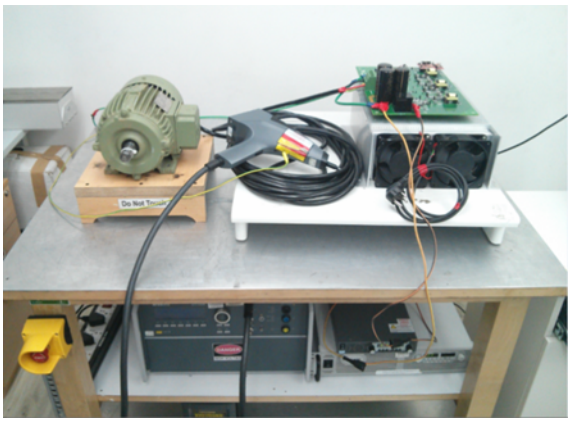


図 115. EUT/AUX Equipment Isolated From Reference Plane by 10 cm

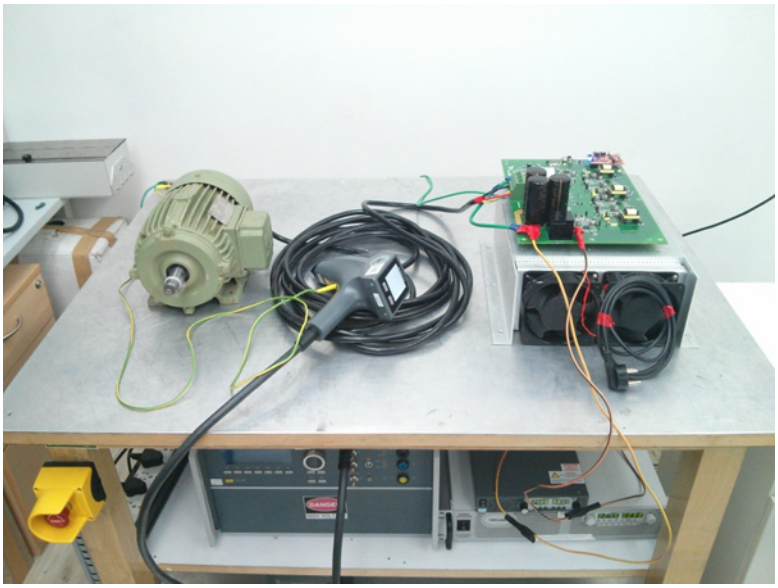


図 116. Test Configuration 2: EUT/AUX Equipment on Reference Plane

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-00195.

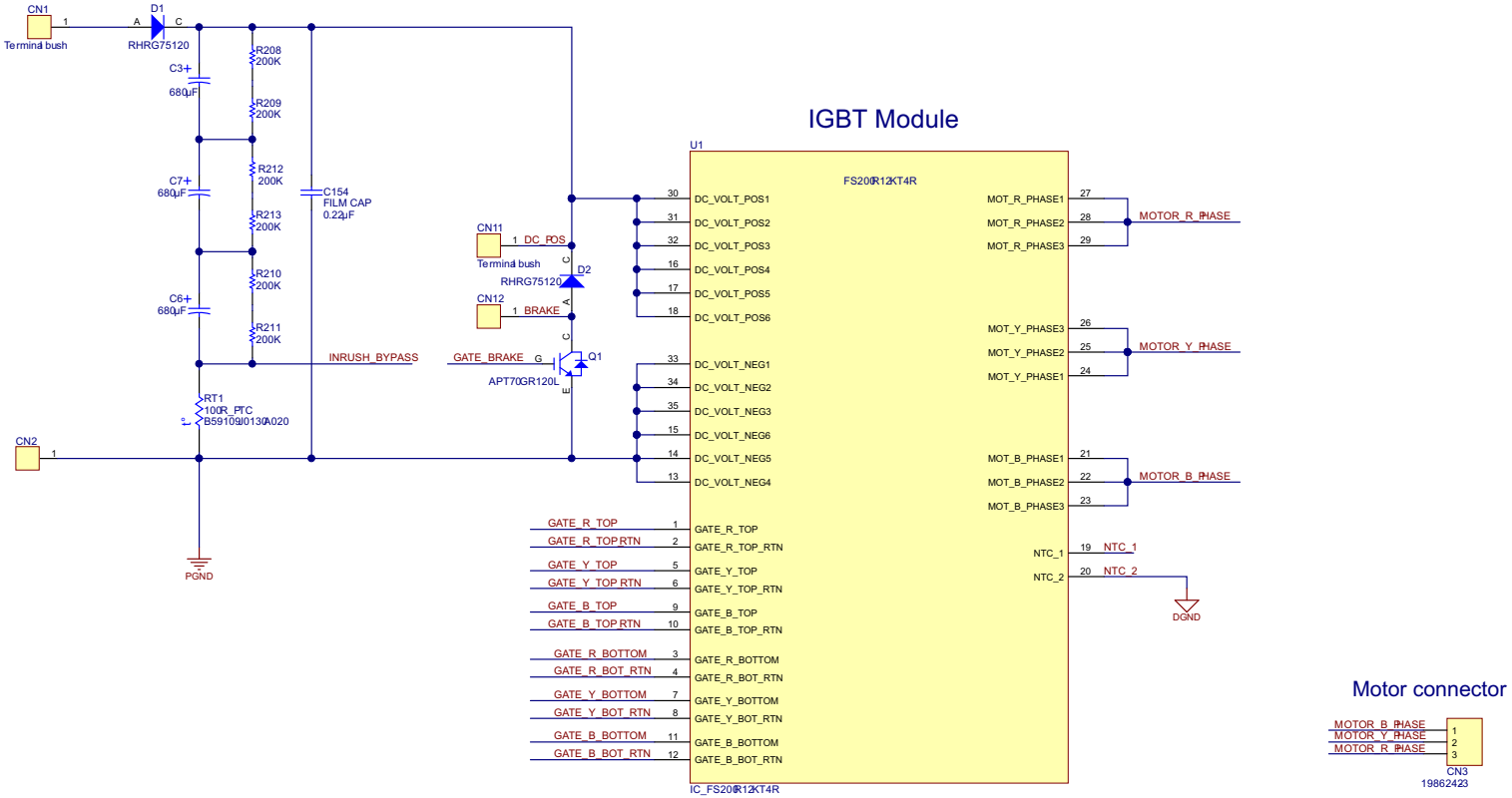


図 117. IGBT Module

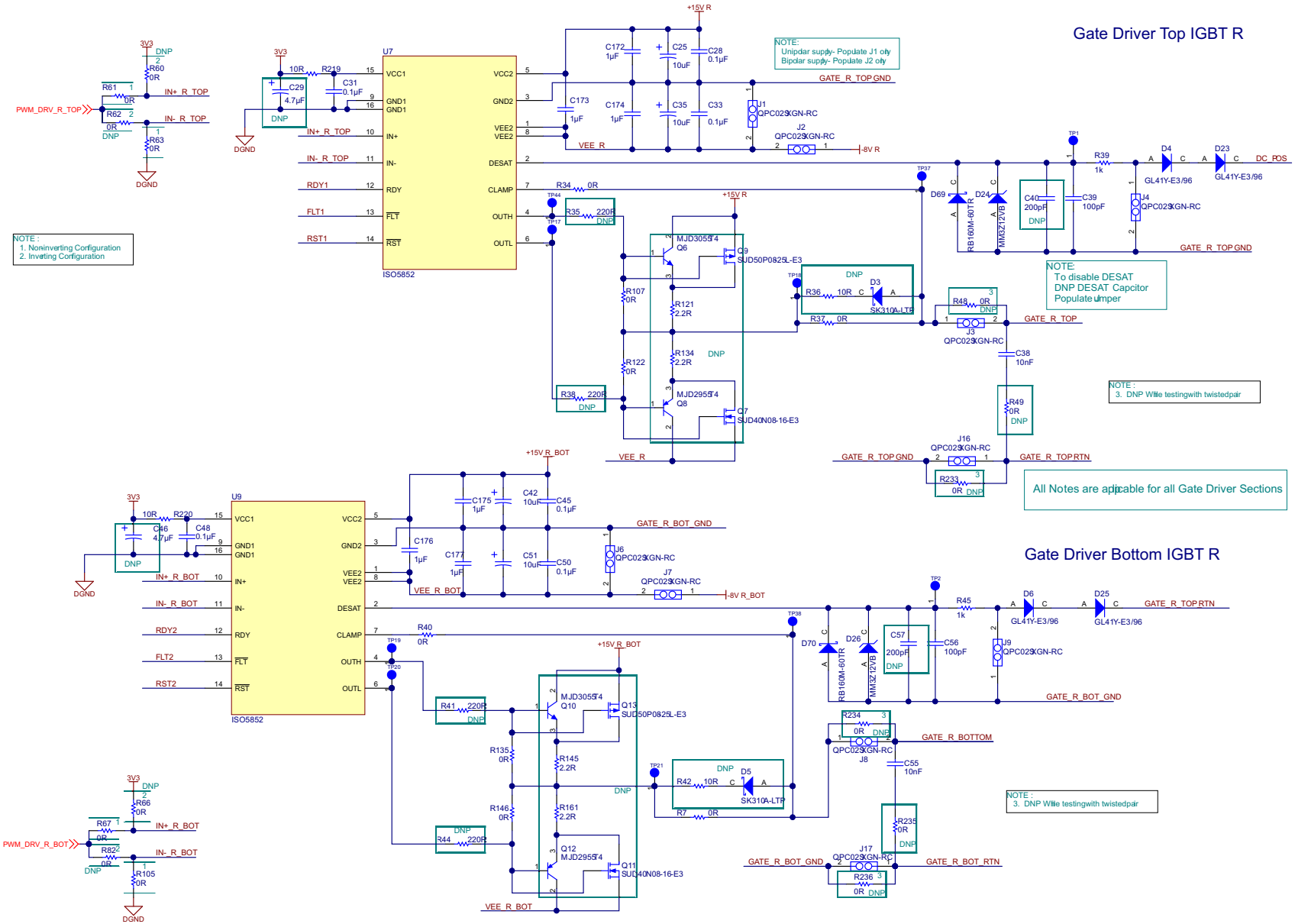


図 118. Gate Driver R

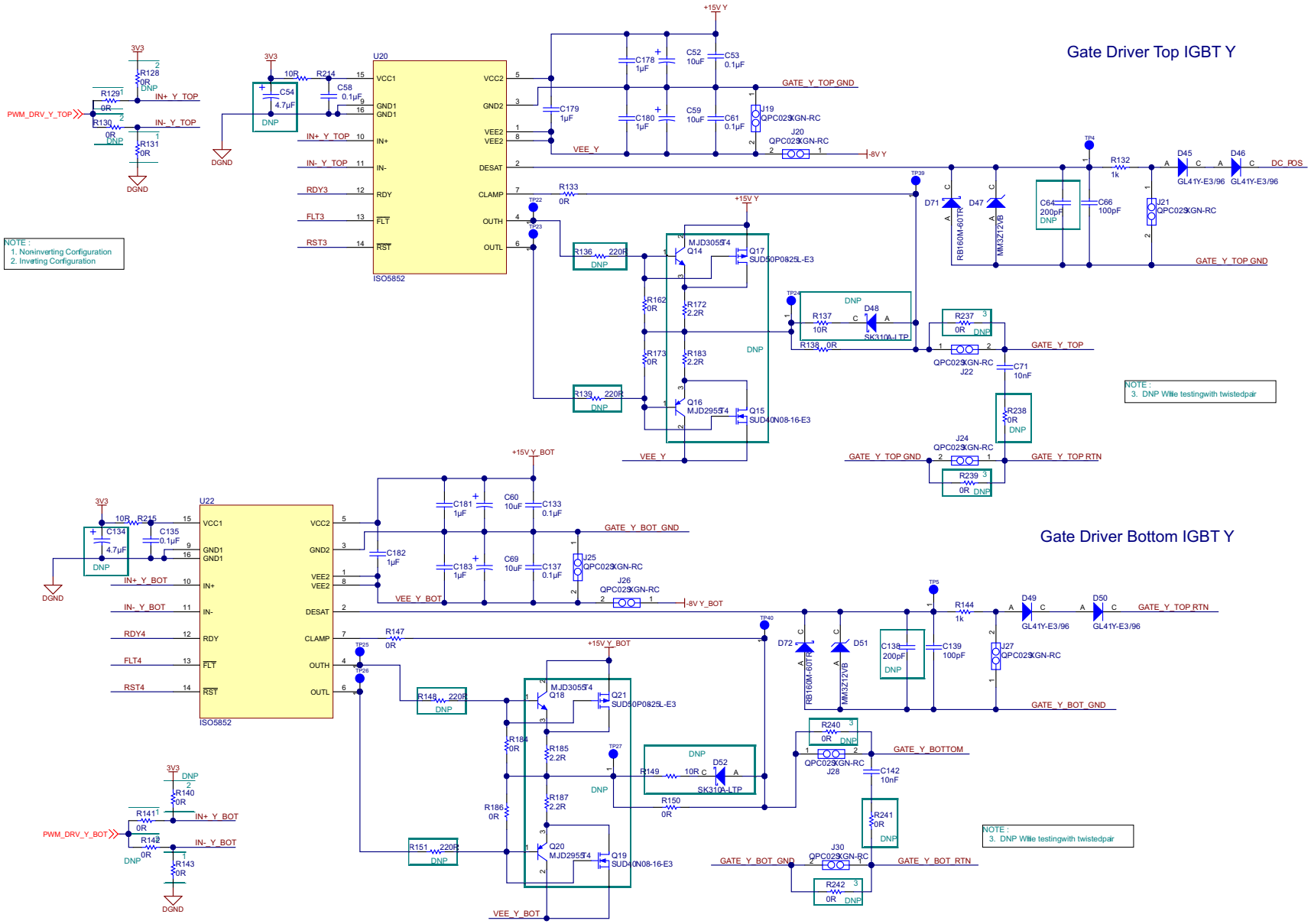


図 119. Gate Driver Y

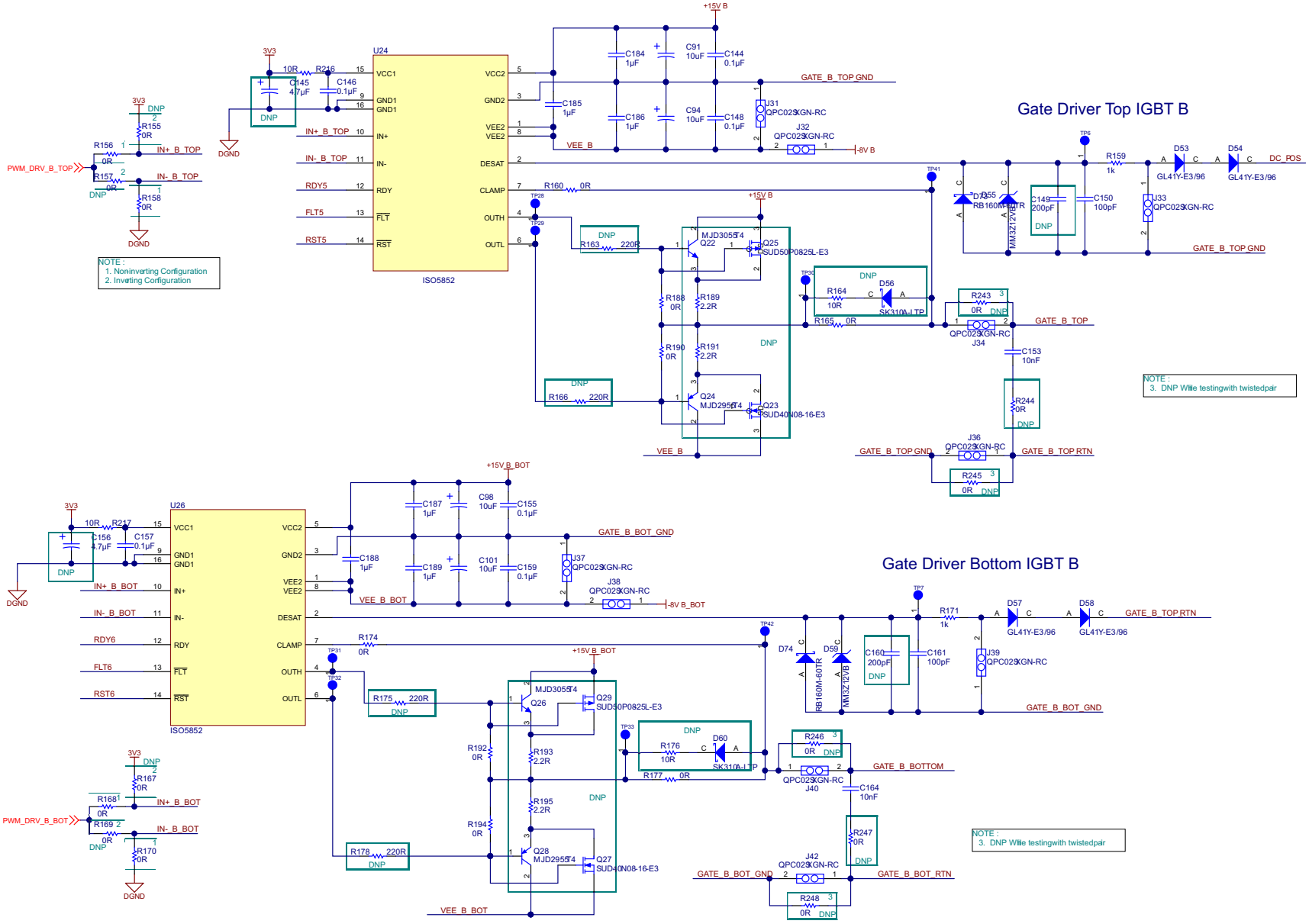


図 120. Gate Driver B

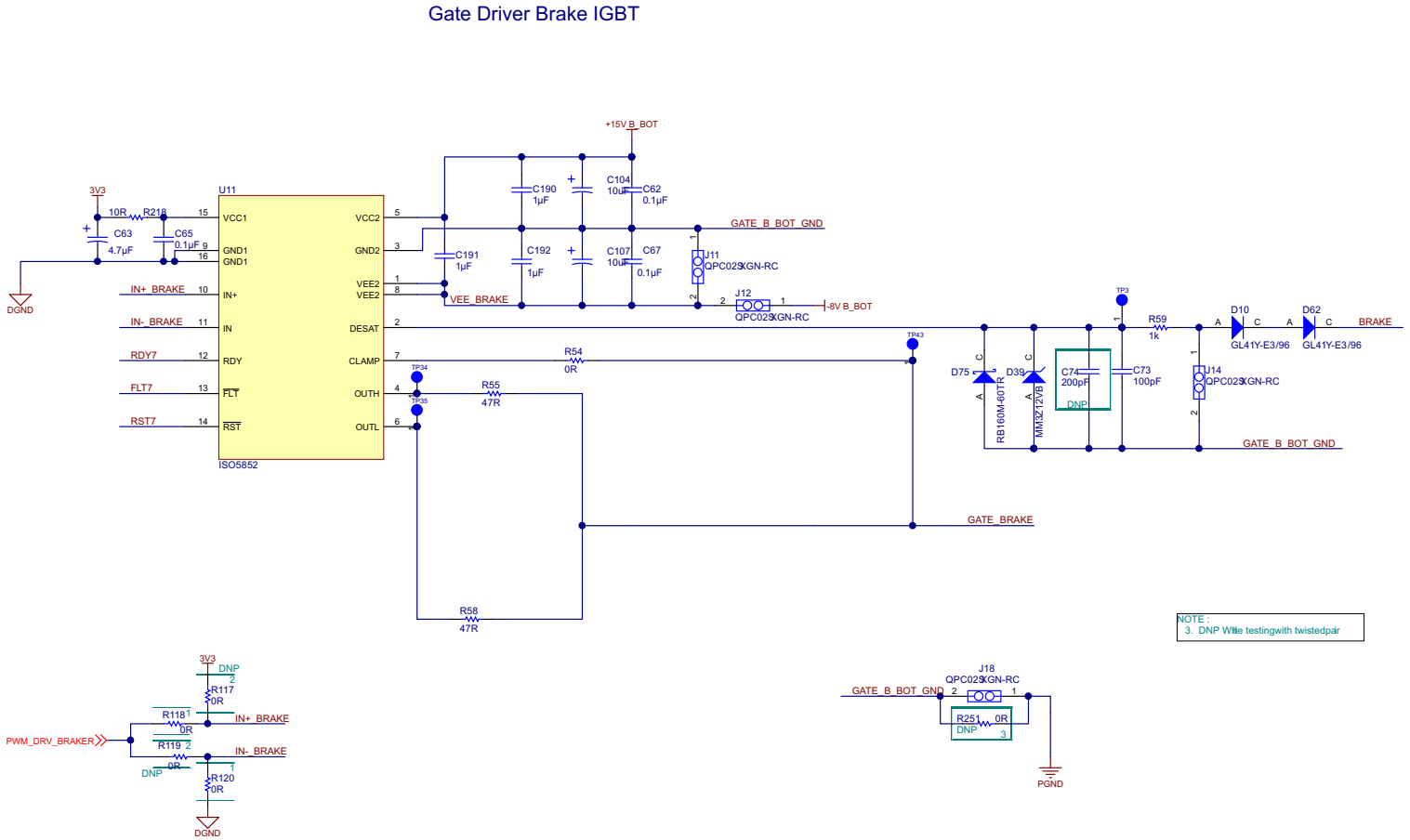


図 121. Brake Drive

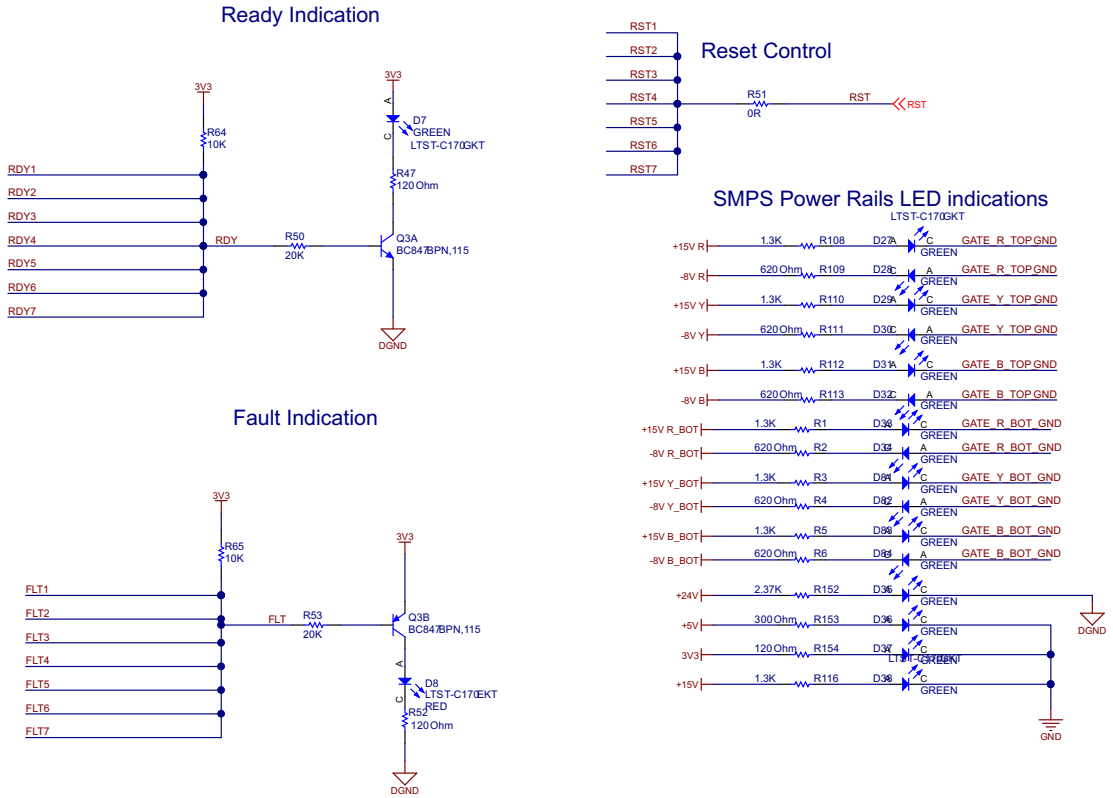


図 122. LED Indications

GATE_DRIVER_BUFFER

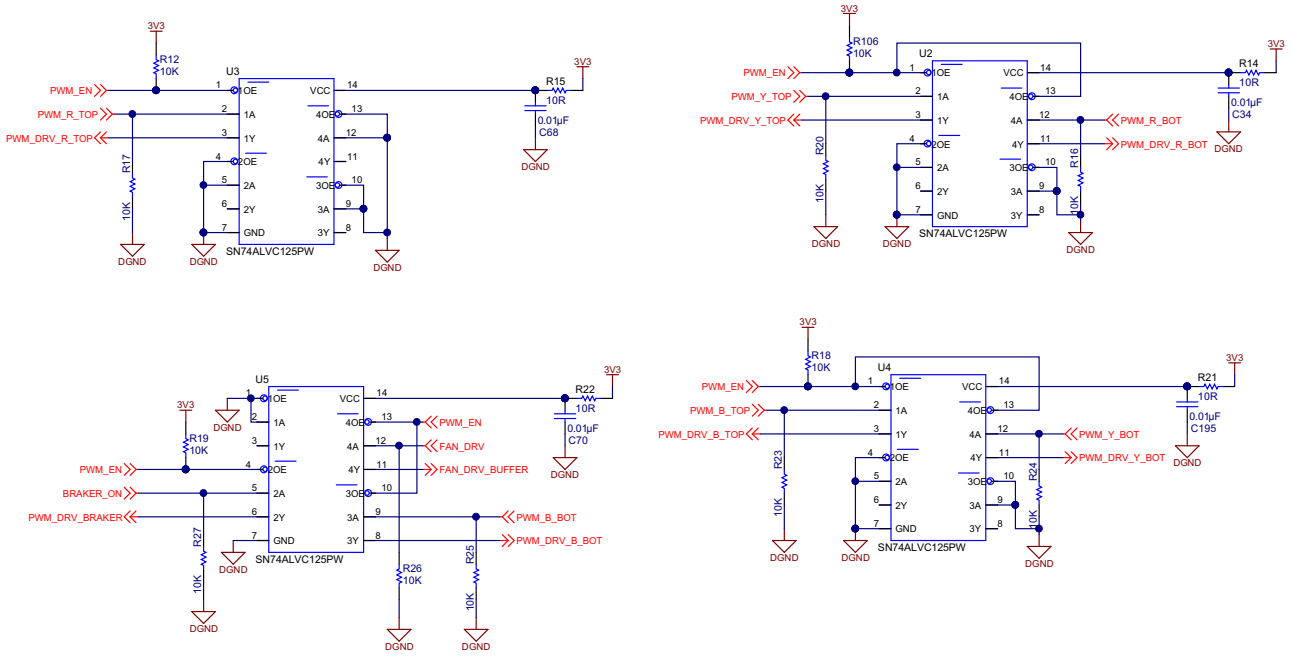


図 123. Gate Driver Buffer

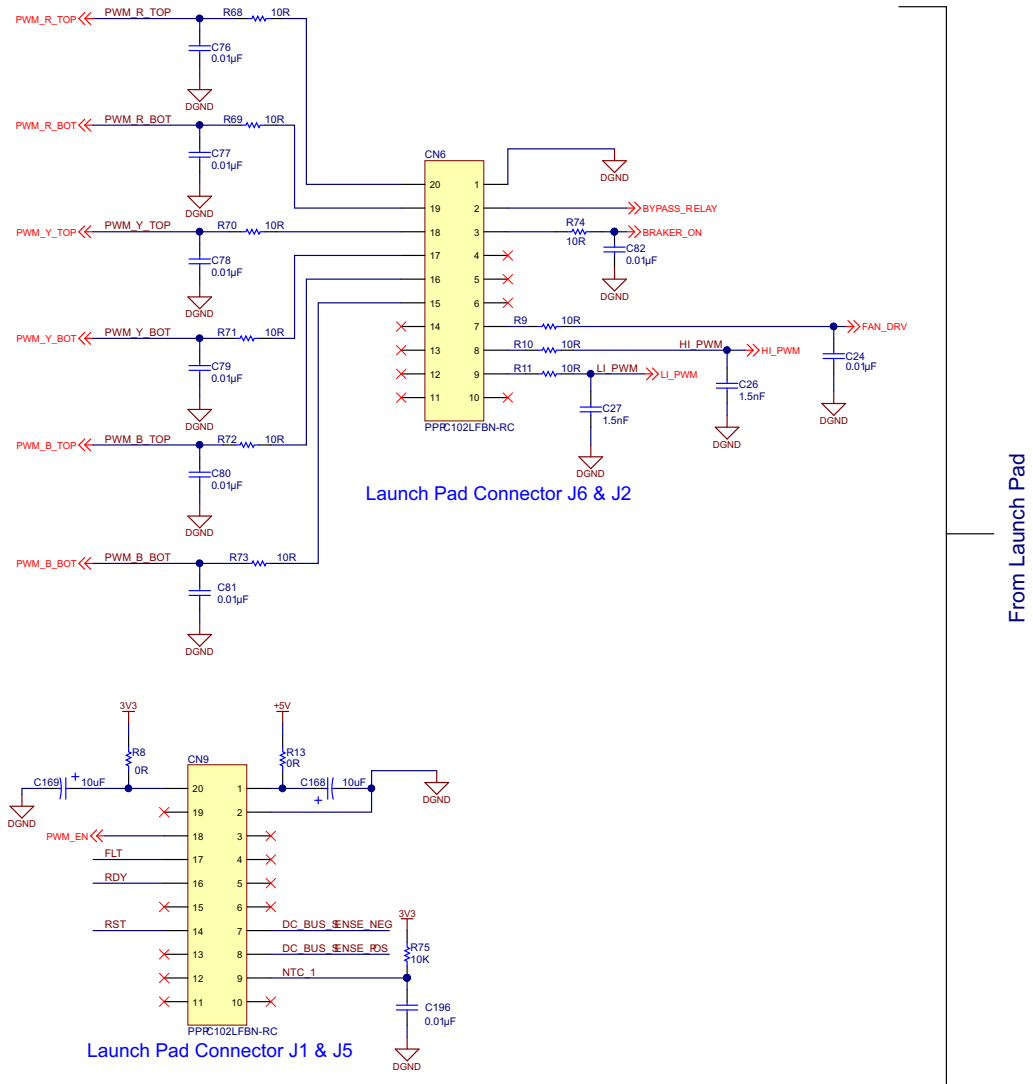


図 124. Board-to-Board Connections

DC BUS VOLTAGE SENSING

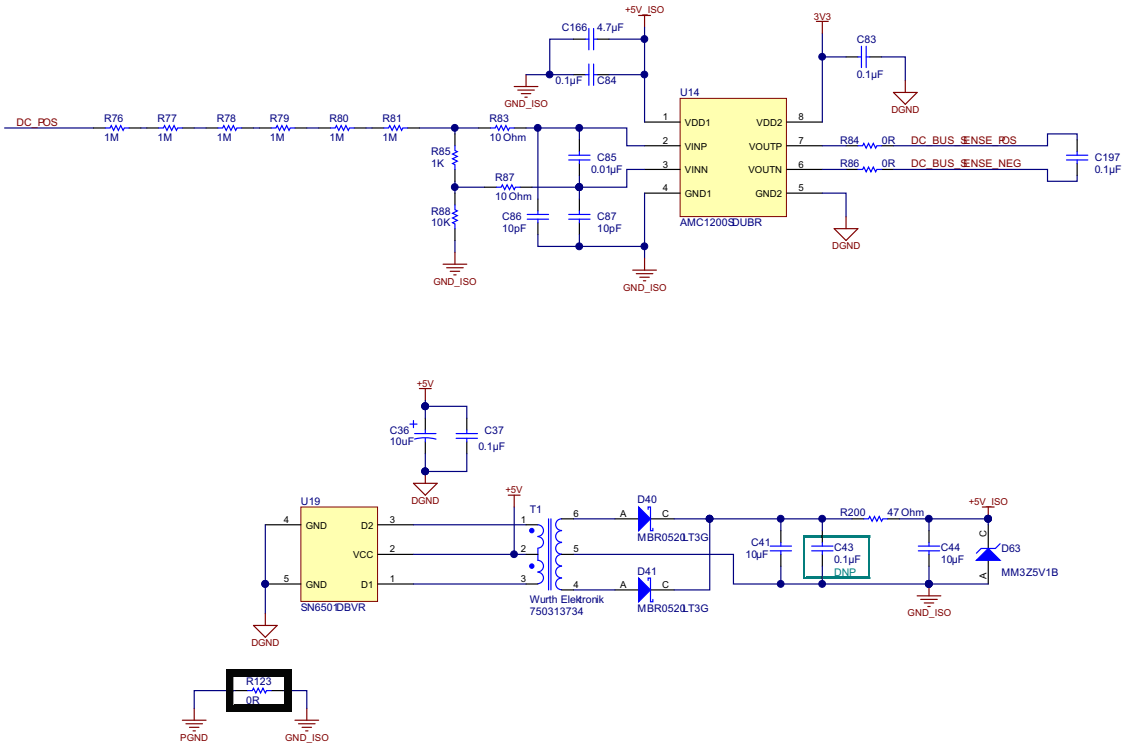


図 125. DC Bus Voltage Sensing

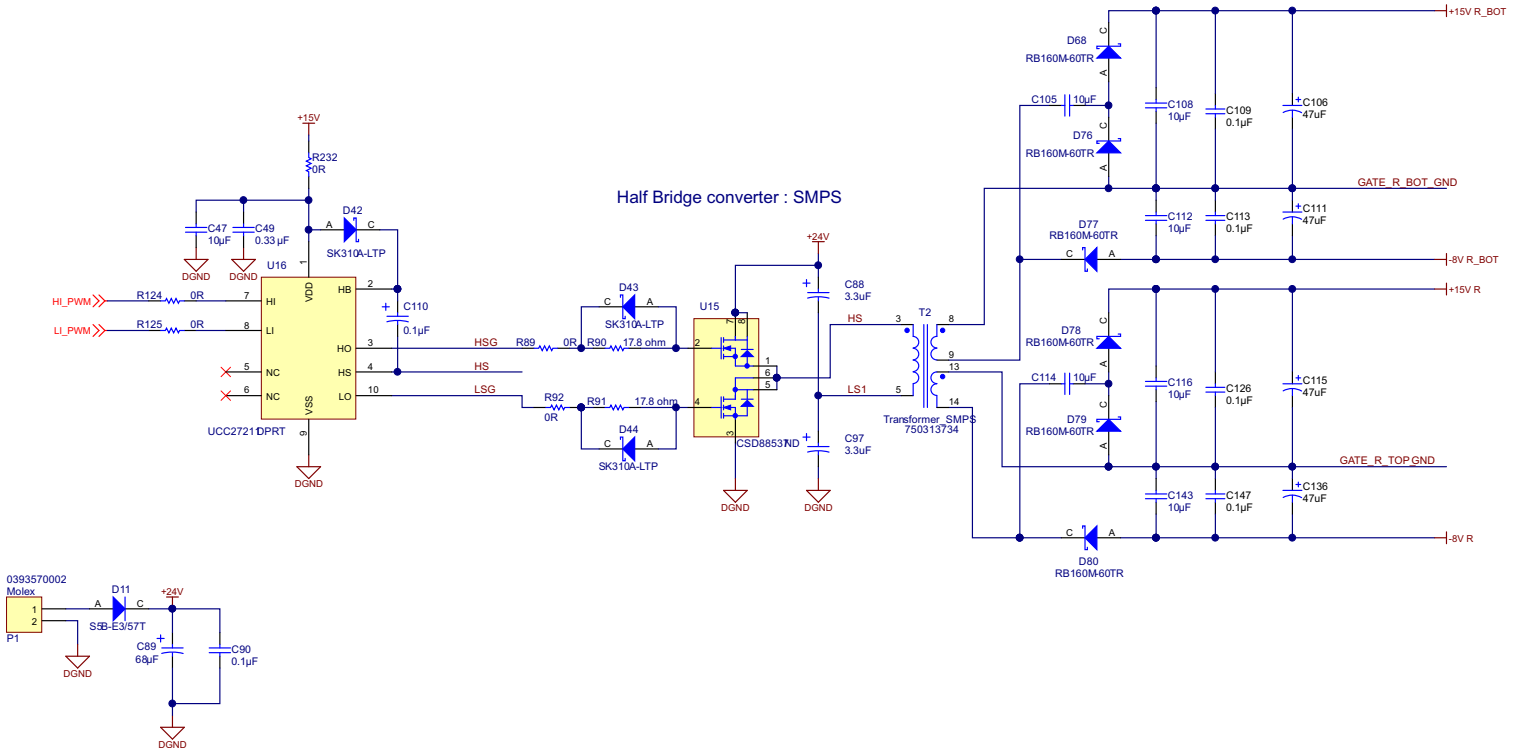


図 126. Gate Driver Power Supply (R Phase)

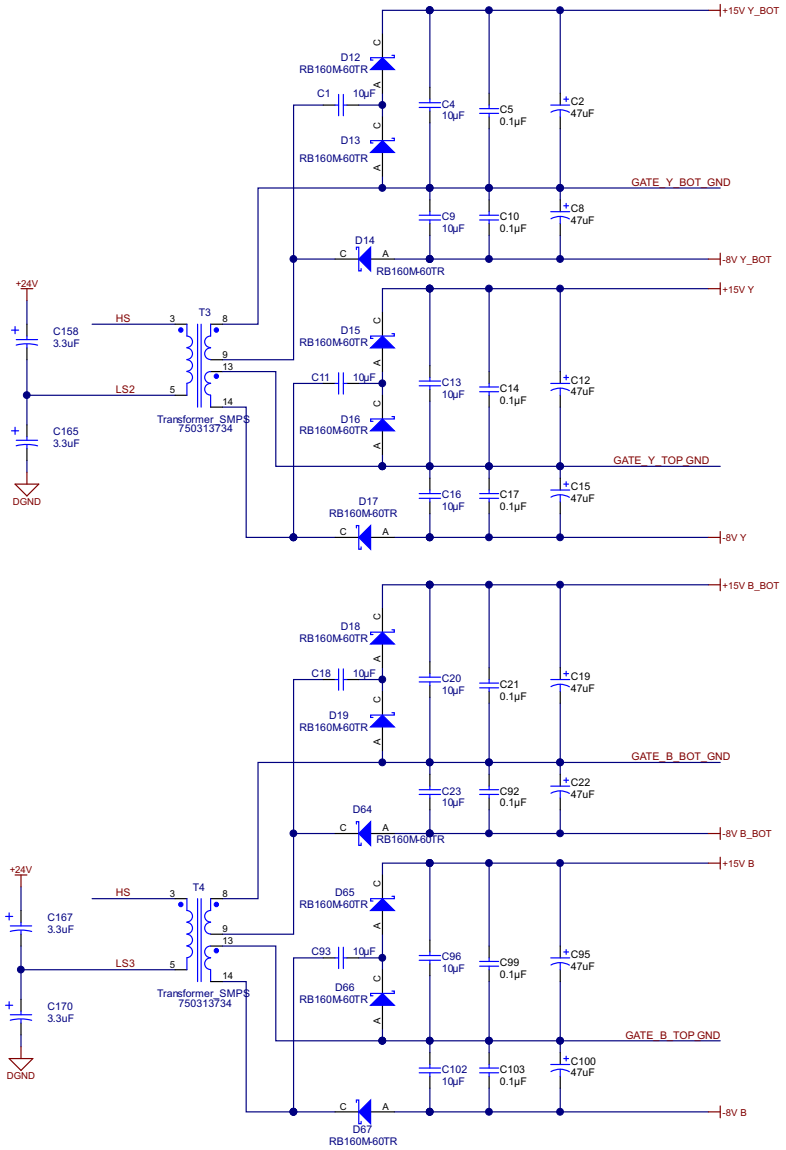


図 127. Gate Driver Power Supply (Y and B Phase)

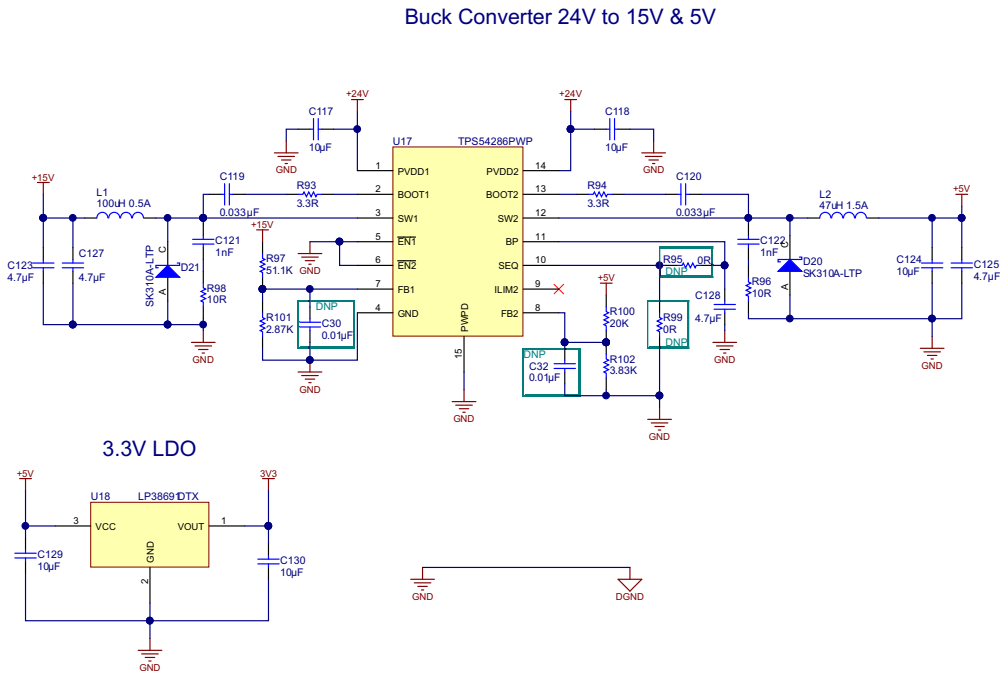


図 128. Buck Converter 24 V to 15 V and 5 V

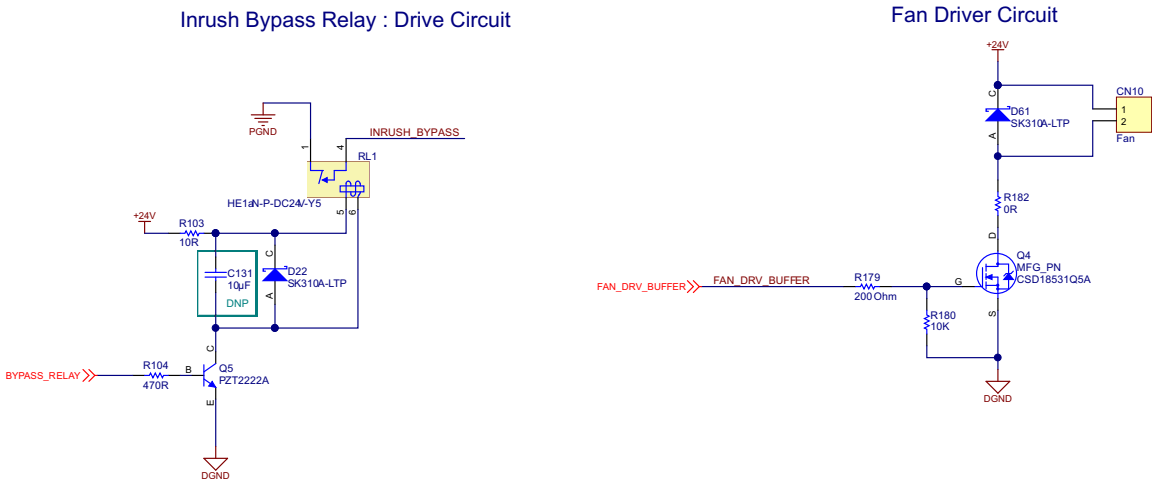


図 129. Inrush Relay

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00195.

8.3 Layer Plots

To download the layer plots, see the design files at TIDA-00195.

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00195.

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00195.

8.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00195.

9 References

1. IEEE, *Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems*, Kolar, J.W.; ETH Zurich, Power Electron. Syst. Lab., Zurich; Round, S.D., July 2006

10 Terminology

PWM— Pulse Width Modulation

LaunchPad— All reference to LaunchPad refers to InstaSPIN-FOC enabled C2000 LaunchPads

CFM— Cubic Feet per Minute

MCU— Microcontroller unit

FETs, MOSFETs—Metal–oxide–semiconductor field-effect transistor

IGBT— Insulated Bipolar Gate Transistor

ESD— Electro Static Discharge

EFT— Electrical Fast Transients

RPM— Rotation per Minute

RMS— Root Mean Square

11 Acknowledgments

The authors would like to thank Kamat Anant and Baranwal Shailendra (Industrial Interface Business unit at TI) for their technical contributions to this design.

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2015年6月発行のものから更新 **Page**

- Note under 7.13 追加 48

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