参考資料

TI Designs
気中遮断器(ACB)用の高分解能、高速スタートアップのデルタ-シグマADCベースAFEのリファレンス・デザイン

TEXAS INSTRUMENTS

デザイン概要

このデザインでは、気中遮断器(ACB)で使用するための電子トリップ・ユニット(ETU)用の信号処理フロントエンドについて紹介します。このサブシステムは、広範囲の電流および電圧入力を指定の精度で測定するために、高分解能のデルタ-シグマ(Δ∑) ADCを使用し、同時に8つまでの入力を24ビット分解能で測定できます。このADCは、MSP430 MCUと接続して入力を処理します。このデザインは、整流された電流入力、または補助DC入力電源から電力の供給を受けます。このデザインでは、正および負の電源を生成する方法を2つ選択できます。1つはLM5017を使用するもので、もう1つはFly-Buckモードに設定されているLM5160を使用するものです。ACBでETUを使用する目的は、電流と温度の広い入力範囲に対して、繰り返し可能な高速のトリップ性能を実現することです。ACBは、フォルトで駆動されたとき、ミリ秒以内にトリップを行います。

設計リソース

TIDA-00661	デザイン・ファイルを含むツール・フォルダ
ADS131E08S	プロダクト・フォルダ
MSP430F5969	プロダクト・フォルダ
LM5160	プロダクト・フォルダ
LM5017	プロダクト・フォルダ
TPS73201-Q1	プロダクト・フォルダ
TPS72301-Q1	プロダクト・フォルダ
TPS73230-EP	プロダクト・フォルダ
TPS7A6533-Q1	プロダクト・フォルダ
LMV614	プロダクト・フォルダ
LM2903	プロダクト・フォルダ
LMT87	プロダクト・フォルダ
LM4041-N	プロダクト・フォルダ
LM8364	プロダクト・フォルダ
ADS131E08	プロダクト・フォルダ

TI E2E™ Community

E2Eエキスパートに質問

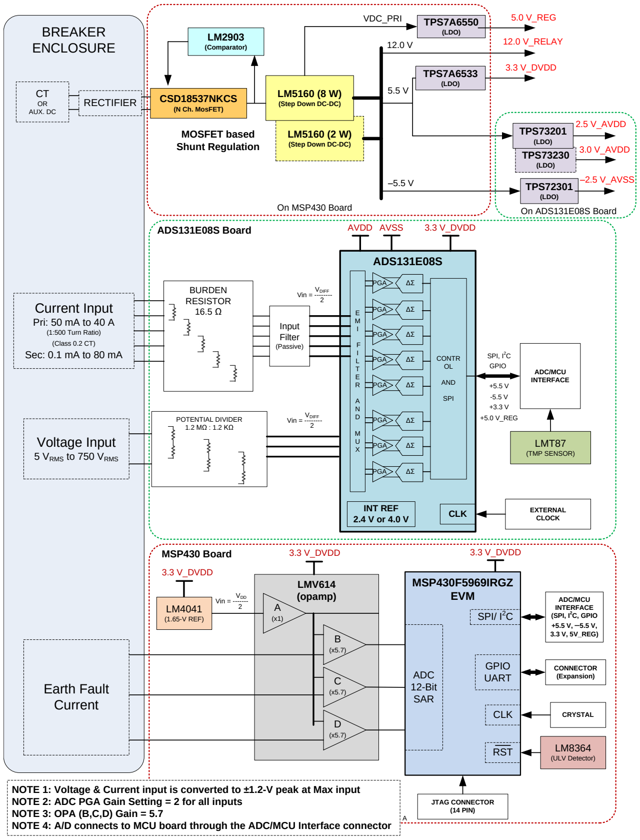
デザインの特長

- 3つの電圧と5つの電流の入力を、8チャネル同時サンプリングの24ビットΔ∑ ADC ADS131E08Sと接続し、高速なスタートアップ(3ms未満)を実現
- 固定PGAゲインで、500以下のダイナミック・レンジについて±1%の精度でAC電流入力を測定
- 固定PGAゲインで、10V～750Vの範囲について±1%の精度でAC入力を測定
- オンボードの電位分圧回路により電圧を測定し、負荷抵抗を使用して電流を測定
- Δ∑ ADC (ADS131E08S)の合計スタートアップ時間が4ms未満で、補助DC入力の印加後に±2%以内の精度で入力電圧を測定
- ADS131E08により、0.2～100AのAC入力について、±0.2%精度で電流を測定
- ADS131E08により、5～1000VのAC入力について、±0.2%精度で電圧を測定
- Fly-Buck™構成のDC/DCコンバータにより電源出力を生成
- 低消費電力電流変換器(LPCT)により、0.6mV～333V (500を超えるダイナミック・レンジ)を±0.2%の精度で測定
- 2Wまたは8Wの電力出力用にサブシステムを構成可能
- 地絡電流測定用に、MCUの内蔵12ビットADCを使用し、単一ゲインで3つの電流入力を測定する機構
- モジュール化設計により、ADCボードをADS131 EVMまたはMSP430 MCUに接続可能
- オンボードLDOにより、MCUおよびADCボード用の3.3Vおよび5Vと、ADCアナログ電源用の±2.5Vおよび3Vを生成
- ADC入力のESD保護

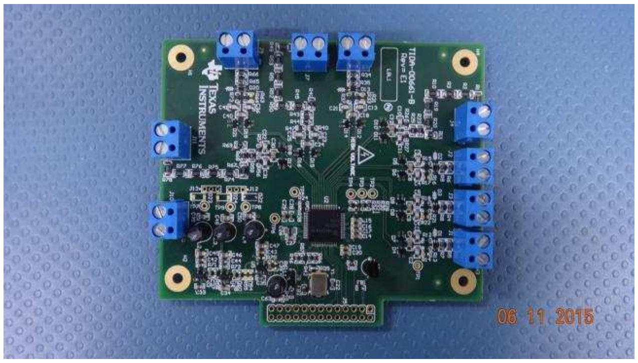
主なアプリケーション

- ACB
- MCCB
- リクローザ
- フィーダ保護リレー

TIDUB80 翻訳版 — 最新の英語版資料 http://www-s.ti.com/sc/techlit/TIDUB80



NOTE 1: Voltage & Current input is converted to ±1.2-V peak at Max input
NOTE 2: ADC PGA Gain Setting = 2 for all inputs
NOTE 3: OPA (B,C,D) Gain = 5.7
NOTE 4: A/D connects to MCU board through the ADC/MCU Interface connector



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1 Design Theory—Circuit Breaker

A circuit breaker is an automatically-operated electrical switch that has been designed to protect an electrical circuit from damage caused by overload. An overload occurs when too many devices are operating on a single circuit, or when forcing a piece of electrical equipment to work beyond its designed capabilities. A short circuit occurs when two bare conductors touch. When a short circuit occurs, resistance drops to almost zero. Short-circuit current can be thousands of times higher than a normal operating current). The basic function of a circuit breaker is to detect a fault condition and, by interrupting continuity, immediately discontinue electrical flow. Breakers are available in different types.

- Low-voltage circuit breakers: These breakers are commonly used in domestic, commercial, and industrial fields. Miniature circuit breakers (MCB), molded-case circuit breakers (MCCB), and air circuit breakers (ACB) are common examples of low-voltage circuit breakers.
- Medium-voltage circuit breakers: These breakers can be assembled into metal-enclosed switchgear lineups for indoor applications or as individual components for outdoor applications like substations. Vacuum circuit breakers, air circuit breakers, and SF6 circuit breakers are examples of medium-voltage circuit breakers.
- High-voltage circuit breakers: These breakers help to protect and control electrical power transmission networks. These breakers are use solenoids for operation and employ the use of current sensing protective relays that function through current transformers. Vacuum circuit breakers and SF6 circuit breakers are examples of high-voltage circuit breakers.

Circuit breakers perform the following functions:

- Sensing – When an overcurrent occurs
- Measuring – The amount of overcurrent
- Acting – By tripping in a timely manner to prevent damage to the circuit breaker and the conductors that the breaker protects

The current-carrying capacity (in A) of the breaker must be higher than the expected load in the circuit.

1.1 Circuit Breaker Construction

Circuit breakers are constructed from the following five major components:

- Frame (molded case)
- Contacts
- Arc chute assembly
- Operating mechanism
- Electronic trip unit (ETU)

The construction and operation of ACBs and MCCBs share common features, such as a contact system with an arc-quenching mechanism to operate the breaker and an electronic system to provide protection, control, and indication.

MCCBs are available up to 4000 A but become less cost-effective for very large ratings (2000 A and above). The advantage of MCCBs with large ratings is a compact size. In a short circuit, the contacts of MCCBs open before the first peak of the current waveform (within five ms in a 50-Hz system). The fault current flowing through an MCCB never reaches its peak and the fault energy allowed downstream is limited. This fault limitation protects sensitive equipment that is not rated to withstand faults.

An ACB is physically larger but more cost-effective for higher ratings. ACBs are selected because they have the ability to withstand fault current rather than limit it. A typical ACB opens a short circuit within 40 ms to 50 ms, allowing between one and two cycles of fault current through before opening. A load protected by an ACB (transformers or bus bars, for example) must be rated to withstand fault current for a short duration.

1.2 Circuit Breaker—Sensor Selection

Circuit breakers combine the following sensors for operation:

- Iron core sensor for the power supply to the electronics
- Air core sensor (Rogowski coils) for measurement, which guarantees high accuracy

Consider the following parameters when selecting breakers:

1. Rated current – This is the maximum value of current that a circuit breaker (fitted with a specified overcurrent tripping relay) can carry indefinitely at an ambient temperature stated by the manufacturer without exceeding the specified temperature limits of the current carrying parts.
2. Short-circuit current (fault current) – The short-circuit current-breaking rating of a circuit breaker is the highest (prospective) value of current that the circuit breaker is capable of breaking without being damaged. The value of current quoted in the standards is the root mean square (RMS) value of the AC component of the fault current, that is, the DC transient component, which is always present in the worst possible case of short circuit. When calculating the standardized value, the DC transient component is assumed to be zero.
3. Rated voltage – This is the voltage at which the circuit breaker has been designed to operate in normal or undisturbed conditions.
4. System frequency – The system frequency is normally 50 Hz or 60 Hz and can even be 400 Hz in some applications. The next subsection provides further insight on the fault current.

The system frequency is normally 50 Hz or 60 Hz and can even be 400 Hz in some applications. The next subsection provides further insight on the fault current

1.2.1 Fault Current

A circuit breaker must be capable of safely interrupting the maximum rated short-circuit current at their location in the circuit. Note that the cost of circuit breakers is lower with a lower breaking capacity.

Potential short-circuit current is determined by:

1. The available power from the transmission network
2. Transformer characteristics
3. Impedance of conductors in the distribution system

A fault level study that accounts for transformer characteristics and conductor impedance at all circuit-breaker installation points allows for a selection of breakers with an optimum breaking capacity.

1.3 Next-Generation Circuit Breakers

The previous generations of breakers have been thermal-magnetic breakers. The new generation of circuit breakers is based on the ETU. Circuit breakers based on ETU provide highly accurate protection with wide setting ranges and can integrate measurement, metering, and communication functions. Designers can combine these circuit breakers with a switchboard display unit to provide all of the functions of a power meter as well as operating assistance. Through direct access to in-depth information and networking through open protocols, these breakers allow operators to optimize the management of their electrical installations.

The new generation of circuit breakers has been specifically designed to protect electrical systems from damage caused by overloads, short circuits, and equipment ground faults. Circuit breakers are designed to open and close a circuit manually and to open the circuit automatically at a predetermined overcurrent setting. Circuit breakers can also:

- Enhance coordination because of their level of adjustability
- Provide integral ground-fault protection for equipment

- Provide high interrupting ratings and withstand ratings
- Provide communications and power monitoring
- Provide protective relaying functions
- Provide zone-selective interlocking (ZSI), which can reduce damage in the event of a fault
- Provide a means of connection to an external test device, allowing for periodical tests of the status of the ETU used in breakers
- Allow all settings to be programmed in the field, without the use of any external device
- Allow the ETU to seal upon adjustment (key lock or seal) behind a transparent door or plate, which allows the user to view the settings and protect against unauthorized tampering

1.3.1 Electronic Trip Unit (ETU)

The trip units integrated into circuit breakers are called electronic trip units (ETUs). ETUs integrate into the circuit breaker as an add-on system to maintain the compact size of a circuit breaker. ETUs are microcontroller (MCU) based and are used to meet a broad range of monitoring and protection requirements, such as curve shaping, zone selective interlocking, arc flash reduction, diagnostics, system monitoring, and system communications. True RMS sensing offers increased accuracy and reliability.

Trip units using digital electronics are faster and more accurate. Designed with signal processing capabilities, ETUs can provide measurement information and device operating assistance. Some of the functions that ETUs offer are:

- MCU and microprocessor unit (MPU) based true RMS measurement
- Four to five current sensing
- Optional voltage measurement
- Protection functions and power measurements
- Self-powered when phase current > 20% to 25% nominal current (In) or auxiliary powered (DC input)
- Making current release (MCR)
- Fault recording and event logging
- Digital outputs and inputs for coordination
- Parameterization and display
- Network communication
- Thermal memory and overtemperature protective trip
- Zone selective interlocking (ZSI) and isolated alarms provision
- Unit status light-emitting diodes (LEDs) and cause of trip LEDs
- Liquid crystal display (LCD) , reset push-button, and test push-button
- Discrete rotary or key-based programmable settings
- Auxiliary modules including
  - Analog output
  - Digital input
  - Trip circuit supervision (TCS) module
  - Power supply module

1.4 Summary of Electronic Trip Unit (ETU) Features

1.4.1 Measurements

The ETU calculates all the electrical values in real time, such as the V, A, W, VAR, VA, Wh, VARh, VAh, and Hz power factors. The ETU also calculates demand current and demand power over an adjustable time period. In the event of tripping on a fault, the interrupted current is stored. The optional external power supply enables the ETU to display the value with the circuit breaker open or not supplied.

Instantaneous values

The value displayed on the screen is refreshed at some fixed time in seconds. Minimum and maximum values of measurements are stored in memory.

Demand metering

The demand is calculated over a fixed or sliding time window, which can be programmed from 5 min to 60 min. According to the contract signed with the power supplier, an indicator associated with a load shedding function enables the ETU to avoid or minimize the costs of overrunning the subscribed power. Maximum demand values are systematically stored and time stamped.

1.4.2 Fault Recording, Event Logging, and Display

Event logs and tables are continuously activated. Providing a wealth of information, these metrics enable users to ensure that the installed equipment base operates correctly to optimize settings and maximize energy efficiency.

Local or remote displays offer easy access to operators and provide the main electrical values: I, U, V, f, energy, power, total harmonic distortion, and so forth. The user-friendly switchboard display unit with intuitive navigation is more comfortable to read and offers quick access to information.

1.4.3 Communication

Four levels of communication functionalities exist:

- Device status: on and off position, trip indication, and fault-trip indication
- Commands: open, close, and reset
- Measurements: mainly I, U, f, P, E, and THD
- Operating assistance data: settings, parameters, alarms, histograms and event tables, and maintenance indicators

Common communication interfaces include Ethernet, RS485, Profibus, and RS232.

1.4.4 I/O Modules

Input and output (I/O) modules are available to expand the capabilities of the circuit breaker. The following descriptions summarize the capabilities of these modules:

- The digital output module allows the connection of up to six binary signals to external signaling devices. The module can be alternatively utilized to control other equipment. Solid-state and relay output versions of this module are available.
- The digital input module can connect to a maximum of six digital (24-V DC) inputs. This specification enables the status of a switch or the cubicle door to be communicated to the circuit breaker.
- The analog output module can be used to output a variety of measured values (amps, volts, power, power factor, and so forth) to analog display devices on the cubicle door.
- Zone selective interlocking (ZSI) is a method that allows two or more circuit breakers to communicate with each other so that a short circuit or ground fault is cleared by the breaker closest to the fault in the minimum amount of time.

Some of the other commonly used I/O modules include:

- Communication module
- Power supply module
- Analog input module for input measurement of resistance-temperature detectors (RTDs)
- Communication module

- Display module
- Earth Leakage module

1.4.5 Time-Current Curves and Circuit Breaker Adjustments

Time-current curves show how fast a breaker trips at any magnitude of current. An ETU processes the input signals (voltage and current) and provides the trip signals to a solenoid or flux shift device (FD) based on the configured trip settings. Some of the trip curves that can be configured are:

- L = Long time
- S = Short time
- I = Instantaneous
- G = Ground fault (equipment)

1.4.6 Circuit Breaker Adjustments

表 1. Breaker Trip Parameters

FUNCTION	DESCRIPTION
Continuous ampere (Ir)	Varies the level of continuous current the circuit breaker carries without tripping. The continuous current is adjustable from 20% to 100% of the continuous ampere rating of a breaker (Ir = % of In). This is also known as long-time pickup.
Long-time delay	Referred to as the "overload" position, this function controls the "pause-in-tripping" time of a breaker to allow low level or temporary overload currents. This function allows adjustable settings from 3 s or 25 s at 6 × Ir.
Instantaneous pickup	Determines the level at which the circuit breaker trips without an intentional time delay. The instantaneous pickup function is adjustable from 2 to 40 times the continuous ampere setting (Ir) of a breaker. (Anytime an overlap exists between the instantaneous and short-time pickup settings, the instantaneous automatically takes precedence).
Short-time pickup	Controls the amount of high current the breaker remains closed against for short periods of time, which allows better coordination. This function is adjustable between 1.5 to 10 times the continuous ampere setting (Ir) of a circuit breaker.
Short-time delay	Controls the amount of time (from 0.05 to 0.2 s in fixed time, or 0.2 s at 6 × Ir in the I^2t ramp mode) a breaker remains closed against currents in the pickup range. This function is used in conjunction with the short-time pickup function to achieve selectivity and coordination. (A predetermined override automatically preempts the setting at 10.5 times the maximum continuous ampere setting In).
Ground fault pickup	Controls the level of ground fault current that causes circuit interruption to occur. This function is adjustable from 20% to 70% of the maximum continuous ampere setting (In) of a breaker.
Ground fault delay	Adds a predetermined time delay to the trip point when the ground fault pickup level has been reached. An inverse I^2t ramp is standard and provides a better tripping selectivity between the main and feeder or other downstream breakers.

1.4.7 Electric Motor Operator

The electric motor operator is designed to open, close, and remotely reset a circuit breaker. The electric motor operator is mounted on the face of a circuit breaker so that it can engage the operating handle of a breaker. The built-in motor is connected to remote pushbuttons or contacts. Pressing the “ON” pushbutton or closing the “ON” contacts causes the electric motor to move the circuit breaker to the “ON” position. Pressing the “OFF” pushbutton or closing the “OFF” contacts causes the electric motor to move the circuit breaker to the “OFF” position. To reset the circuit breaker from the tripped position, the electric motor must first move the circuit breaker handle to the “OFF” position and then to the “ON” position, just as this action is performed manually.

1.4.8 Discriminator or Making Current Release (MCR)

The discriminator (also known as a making current release (MCR)), is a setting provided with each trip unit and is based on the specific circuit breaker size and protects the circuit against closing on high magnitude faults. The MCR function immediately trips and opens the circuit breaker if high-magnitude fault current is sensed at the instant the circuit breaker closes.

The discriminator is set at ≥ ten times the rating plug ampere rating and is enabled for approximately the first ten cycles of current flow. In cases where a fault condition exists, the breaker trips with no intentional time delay on closing, which protects the user from a potentially unsafe condition.

1.4.9 Instantaneous Override

Instantaneous override is a fixed current level at which an adjustable circuit breaker overrides all settings and trips instantaneously. The instantaneous (INST) trip function trips the MCCB or ACB when the short-circuit current exceeds the pickup current setting, irrespective of the state. The instantaneous override is factory set nominally just below the breaker withstand rating.

1.4.10 Trip Unit Overtemperature

Electronic trip units can operate reliably in ambient temperatures that range from –20°C to 70°C. Breakers are derated if they are above 70°C. In the unlikely event that temperatures exceed this ambient temperature range, the trip unit has a built-in overtemperature trip to protect the trip unit.

2 ACB Ratings

A voltage rating circuit breaker has a voltage rating that designates the maximum voltage it can handle. The voltage rating of a circuit breaker can be higher than the circuit voltage, but never lower. For example, a 480-V AC circuit breaker can be used in a 240-V AC circuit, but a 240-V AC circuit breaker cannot be used in a 480-V AC circuit

表 2. Common Breaker Voltage Ratings

AC VOLTAGE RATINGS (V)	230	380	400	415	440	500	525	690

Continuous current rating

Every circuit breaker has a continuous current rating, which is the maximum continuous current a circuit breaker is designed to carry without tripping. The rated current for a circuit breaker is often represented as In. This designation is not to be confused with the current setting (Ir), which applies to those circuit breakers that have a continuous current adjustment. Ir is the maximum continuous current that a circuit breaker can carry without tripping for the given continuous current setting. Ir may be specified in amps or as a percentage of In.

表 3. Common Breaker Current Ratings

AC CURRENT RATINGS (A)	200	250	400	630	800	1000	1250	1600	2000	2500	3200	4000	5000	6300
Ir THRESHOLD SETTINGS (A)	80 to 200	100 to 250	160 to 250	250 to 630	320 to 800	400 to 1000	500 to 1250	630 to 1600	800 to 2000	1000 to 2500	1280 to 3200	1600 to 4000	2000 to 5000	2500 to 6300

Pickup (A) = Ir x … 1.5 – 10

Current setting (A) Ir = In x … 0.4 – 1.0

注: The pickup current has the option to be Ir × 15 or Ir × 20.

- ICW is the short-circuit withstand rating of a particular circuit breaker in amperes. The withstand rating is defined differently within different standards, but it is always the value of current that a circuit breaker can withstand for some period of time without interrupting.
- ICS, or the service breaking capacity per IEC 60947-2, is the breaking capacity that a breaker can safely interrupt and be operational after interrupting at least one time.
- ICU, or the ultimate breaking capacity per IEC 60947-2, is the breaking capacity that a breaker can safely interrupt, but may not remain operational after interrupting one time.

Interrupting rating

Circuit breakers are also rated according to the maximum level of current they can interrupt. This is the interrupting rating or ampere interrupting rating (AIR). The interrupting ratings for a circuit breaker are typically specified in symmetrical RMS amperes for specific rated voltages. The term symmetrical indicates that the alternating current value specified is centered around zero and has equal positive and negative half cycles.

Circuit breakers have interrupting ratings as follows:

- 25 kA – Standard, low short-circuit level applications (for example: service businesses)

- 36 kA to 50 kA – Standard applications (for example: industrial plants, buildings, and hospitals)
- 70 kA to 100 kA – High performance at controlled cost
- 150 kA – Demanding applications

2.1 Air Circuit Breaker (ACB)—Operating Time

An important specification for ACBs is the operating time. The specifications for operating time include breaking time and closing time. Breaking time includes the measurement of input current and processing of the samples to provide the solenoid trip command, which breaks the fault current.

Breaking (maximum) time (instantaneous break time at short-circuit interruption current): If the load current is greater than the set instantaneous pickup value is detected, the ACB- electronic trip unit will initiate a trip pulse within Maximum break time of having seen the current. The maximum breaking time is specified by different ACB manufacturers in the range of *30 ms to 50 ms*.

To achieve a faster breaking time, the ETU (including the power supply, MCU, and ADCs) must have a fast start-up capability.

2.2 TIDA-00661 Advantages

This TIDA-00661 design provides a solution to some of the critical requirements of an ACB, such as:

1. Fast start-up: ACBs are specified to trip within 35 ms to 40 ms when they are powered with a fault. The start-up time includes the system power up, AC input current measurement, and breaking of the fault current.
2. Wide input measurement: The fault current input range varies from 0.3 In to 12 In or more for a given current breaker rating. The circuit breakers are available in multiple current ratings. An ADC with high resolution ensures the use of the same trip unit for multiple current ratings.
3. Accurate measurement of voltage and current inputs: The accurate measurement of input current ensures a repeatable trip time performance for protection and an accurate measurement of different parameters for metering.
4. Increased reliability and temperature performance: The integration of reference and programmable gain amplifier (PGA) reduces the external components requirement, improves temperature performance, and increases reliability.

The TIDA-00661 design provides a solution for all of the above critical requirements of a circuit breaker. The design contains an AFE board and an interface board.

2.3 TIDA-00661 System Description and Functionality

2.3.1 AFE Board (With ADC and LDOs for Analog Supply)

The analog front end (AFE) board uses a fast start-up ΔΣ ADC with a start-up time of < 3 ms. The ΔΣ ADC has eight simultaneous sampling ADCs with 24-bit resolution. Additionally, the ADC has a PGA, which can be used to improve accuracy while measuring wide input currents. The AFE has a provision to measure three voltages and five currents. The AFE board uses the internal reference of the ADC. A provision for an external clock has been provided in this design to meet the measurement accuracy requirement over a wide temperature range. The ADC input has been configured for a ±2.5-V input range. The PGA has been set for a fixed gain of 2 for most measurement applications. An external, onboard temperature sensor has been provided. The digital interface is powered by 3.3-V supply. The ADC is interfaced to an MSP430F5969 based interface board or MMB0 DSP board.

The AFE board for the TIDA-00661 design features the following:

1. Fast start-up (< 3 ms) ΔΣ ADC ADS131E08S with eight simultaneous inputs for measuring up to five

currents and three voltages; onboard potential divider for measuring up to 900 V

2. LDO to generate ±2.5 V, 3 V for ADC analog input
3. Temperature sensor to measure local onboard temperature
4. Extension connectors for interfacing to MMB0 digital signal processor (DSP) board of an MSP430F5969 interface board

2.3.2 Interface Board (With MCU and DC-DC Converter)

The interface board has a provision for a self-powering regulation circuit, which generates DC voltage from a rectified current input. The user can also apply an auxiliary input if the circuit breaker has a provision for display and communication features. The DC-DC converter is used to generate multiple DC outputs such as 5.5 V, –5.5 V, and 12 V. The DC-DC converter is configured in a Texas Instruments (TI) Fly-Buck™ configuration and has a primary, non-isolated DC supply output. The primary side output voltage (V_{PRI}) is regulated to 5 V and can be used for providing additional power depending on the application. The 5 V is regulated to 3.3 V to power the MCU and the op amp. The op amp provides amplification for three current inputs, which have been configured to measure earth leakage currents. An onboard reference generates 1.65 V for level shifting the AC inputs. This design provides a provision for two DC-DC converters, one with an approximate 2-W power output and another with an approximate 8-W power output. The DC-DC converters are specified for a 60-V input operation.

The AFE board for the TIDA-00661 design features the following:

1. MSP430F5969 MCU based interface for configuring and reading samples form the ∆∑ ADC
2. Self-power supply with shunt regulator and provision for auxiliary DC input
3. Provision for two DC-DC converters (approximately 2 W and 8 W) for generating different power supplies; DC-DC converter can be selected based on the power requirement
4. Op amp to measure three earth fault current inputs
5. Extension connectors for future usage

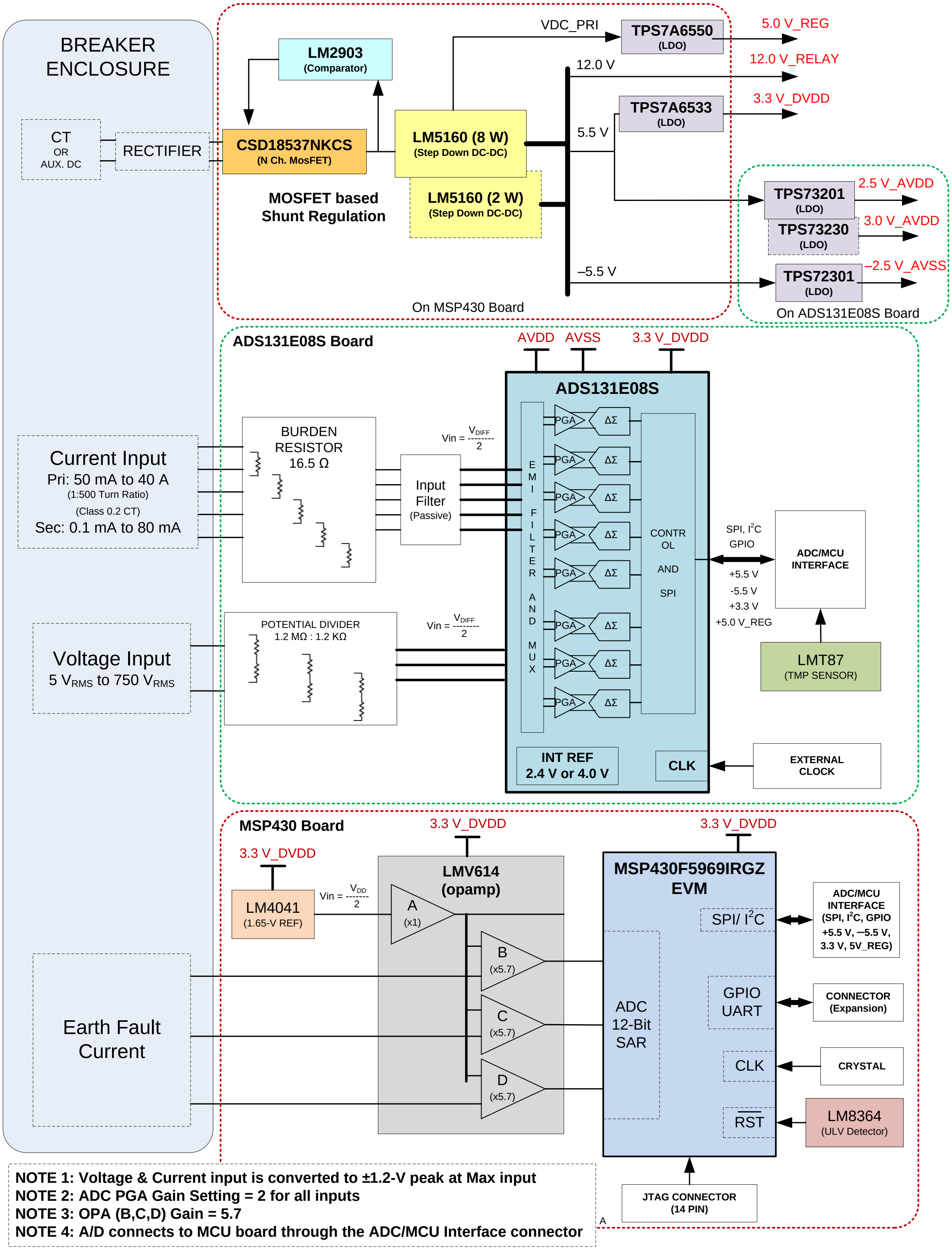
3 Key System Specifications

表 4. Key System Specifications

SERIAL NUMBER	PARAMETERS	SPECIFICATIONS
1	External ADC	ΔΣ, 24-bit resolution with internal programmable amplifier with gains (1, 2, 4, 8, and 12) and configurable sampling rate up to 64 KBPS
2	ADC start-up specification	< 5 ms after power is applied to the DC-DC converter
3	Voltage inputs and range	Three inputs, 5 V to 750 V
4	Current inputs and range	Five inputs, 50 mA to 25 A
5	DC-DC converter – Option 1	24-V input, 2-W output
6	DC-DC converter – Option 2	24-V input, 8-W output
7	ADC analog power supply configuration	±2.5 V
8	ADC digital power and MCU power supply	3.3 V
9	Power supply option for solenoid drive or FSD drive	> 12 V
10	MCU interface for processing analog input	Option 1: ADS131E08 EVM MMB0 DSP board Option 2: FRAM-based, MSP430FR5969 16-bit , 16-MHz operating frequency
11	Earth fault current measurement	Three inputs with X 5.7 gain
12	External clock input for ΔΣ ADC	2.048 MHz

4 Block Diagram

The TIDA-00661 TI Design contains two boards: An MCU board and an ADC board.



NOTE 1: Voltage & Current input is converted to ±1.2-V peak at Max input
NOTE 2: ADC PGA Gain Setting = 2 for all inputs
NOTE 3: OPA (B,C,D) Gain = 5.7
NOTE 4: A/D connects to MCU board through the ADC/MCU Interface connector

図 1. TIDA-00661 Block Diagram

The MCU board consists of:

- Fast start-up MSP430F5969 MCU for signal processing
- Fast start-up DC-DC converter for generating the supply for MCU and ADC boards
- Op amp and reference for signal conditioning the earth fault current input
- LDO to generate regulated supply for MCU and ADC board
- Undervoltage detector for MCU reset control
- Interface connector to connect to ADC

The ADC board consists of:

- Fast start-up, high-resolution ΔΣ ADC
- Current and voltage input including potential divider and protection
- Onboard temperature sensor
- Interface connector to connect to MCU board or MMB0 digital signal processing (DSP) board

4.1 ADC

The use of high-resolution ΔΣ ADCs in a circuit breaker provides the following advantages:

- Wide input current measurement
- Wide voltage measurement
- Accuracy over a wide range of inputs and temperature
- Fast start-up

The ADS131E08S device with an internal PGA meets the above performance requirements and is used as the AFE for analog input measurement. The internal PGA and reference reduces design complexity and improves reliability to save on cost and board space.

Internal reference selection:

The internal reference can be configured to either 2.4 V or 4 V. When using a 3-V analog supply, the internal reference must be set to 2.4 V. In the case of a 5-V analog supply, the internal reference can be set to 4 V by setting the VREF_4V bit in the CONFIG2 register.

For a higher dynamic range, a 5-V supply with a 4-V reference (set by the VREF_4V bit of the CONFIG3 register) can be used.

4.1.1 ADS131E08S

The ADS131E08S is a multichannel, simultaneous sampling, 24-bit ΔΣ ADC with a built-in PGA, internal reference, and onboard oscillator.

The ADS131E08S uses the core from the ADS131E08 family with an improved start-up time for line-powered applications. This device incorporates features commonly required in industrial power monitoring, control, and protection applications with the first set of data becoming available within 3 ms of applying power to the device. Interface the ADS131E08S inputs independently and directly interface with a resistor-divider network or a transformer to measure voltage. Interface the inputs to a current transformer or Rogowski coil to measure current. With high integration levels and exceptional performance, the ADS131E08S device enables the creation of scalable industrial power systems at a significantly reduced size, power, and low overall cost.

The ADS131E08S has a flexible input multiplexer per channel, which can be independently connected to internally-generated signals for test, temperature, and fault detection. Fault detection can be implemented internal to the device using the integrated comparators with digital-to-analog converter (DAC)-controlled trigger levels. The ADS131E08S can operate at data rates up to 64 kSPS.

These complete analog front-end (AFE) solutions are packaged in a TQFP-64 package and are specified over the industrial temperature range of –40°C to 105°C.

Features:

- ADS131E08 with fast power-on time
- Eight differential current and voltage inputs
- Outstanding performance:
  - Exceeds Class 0.1 performance
  - Dynamic range at 1 kSPS: 118 dB
  - Crosstalk: –118 dB
  - THD: –100 dB at 50 Hz and 60 Hz
- Supply range:
  - Analog:
    - 3 V to 5 V (unipolar)
    - ±2.5 V (bipolar)
  - Digital: 1.8 V to 3.6 V
- Low Power: 2 mW/channel
- Data Rates: 1, 2, 4, 8, 16, 32, and 64 kSPS
- Programmable gains (1, 2, 4, 8, and 12)
- Fault detection and device self-testing capability
- SPI data interface and four GPIOs

For more information, visit http://www.ti.com/product/ADS131E08 and http://www.ti.com/product/ADS131E08S.

4.2 *MCU*

An MCU is used to interface to the ΔΣ ADC for configuration and processing of samples. For the breaker to start up and measure in less than 5 ms, the MCU interfaced to the ADC must also have fast start-up. Additional internal peripherals such as universal asynchronous receivers/transmitters (UARTs) and ADCs are preferred. The internal ADCs can be used for measuring the earth fault current, which does not have a wide dynamic range. Low power consumption is another important requirement. The MCU used in this design has low power consumption, starts fast (less than 1 ms) and has a 12-bit internal ADC. A ferroelectric RAM (FRAM) based MCU provides for advanced power optimization and IP encapsulation features.

4.2.1 MSP430F5969

The TI MSP430™ ultra-low-power (ULP) FRAM platform combines uniquely embedded FRAM and a holistic ultra-low-power system architecture, allowing innovators to increase performance at lowered energy budgets. FRAM technology combines the speed, flexibility, and endurance of SRAM with the stability and reliability of flash at much lower power.

The MSP430 ULP FRAM portfolio consists of a diverse set of devices featuring FRAM, the ULP 16-bit MSP430 CPU, and intelligent peripherals targeted for various applications.

Features:

- Embedded MCU

  - 16-bit RISC architecture up to 16 MHz clock
  - Wide supply voltage range: 1.8 V to 3.6 V (minimum supply voltage is restricted by single virtual system (SVS) levels)
- Ultra-low-power FRAM
  - Up to 64KB of nonvolatile memory
  - Ultra-low-power writes
  - Fast write at 125 ns per word (64KB in 4 ms)
  - Unified memory = program + data + storage in one single space
  - 10^{15} write cycle endurance
  - Radiation resistant and nonmagnetic
- High-performance analog
  - 12-bit ADC with internal reference, sample-and-hold, and up to 16 external input channels
- Enhanced serial communication
  - eUSCI_A0 and eUSCI_A1 support
    - UART with automatic baud-rate detection
    - IrDA encode and decode
    - Serial peripheral interface (SPI) at rates up to 10 Mbps
  - eUSCI_B0 supports
    - I^2C with multiple slave addressing
    - SPI at rates up to 8 Mbps
  - Hardware UART and I2C bootstrap loader (BSL)

The features of this MCU have been further outlined in the TIDA-00498 TI Design (TIDUA09). For more information, visit http://www.ti.com/product/msp430fr5969.

4.3 DC-DC Converter

Circuit breakers can operate with the following inputs:

- Self-power (rectified current input)
- Auxiliary DC input
- AC input

In this design, functions such as display, communication, and power quality analysis have been included, along with basic trip functionality. When using these functions, the breaker operates with an auxiliary power supply with a higher power output capability. The power requirement varies depending on the application. This TIDA-00661 TI Design provides an option for two DC-DC converters:

1. LM5017 – This configuration can be used in applications requiring ≤ 2-W power output.
2. LM5160 – This configuration can be used in applications requiring > 2 W and up to an 8-W power output These DC-DC converters have been selected because they have a very fast start-up time. The DC-DC converters have been configured in Fly-Buck configuration to generate multiple outputs including negative supply for ΔΣ converters.

4.3.1 LM5017

The LM5017 is a 100-V, 600-mA synchronous step-down regulator with integrated high-side and low-side MOSFETs. The constant on-time (COT) control scheme employed in the LM5017 requires no loop compensation, provides excellent transient response, and enables very high step-down ratios. The on-time varies inversely with the input voltage resulting in nearly constant frequency over the input voltage range. A high voltage start-up regulator provides bias power for internal operation of the IC and for integrated gate drivers.

A peak current limit circuit protects against overload conditions. The undervoltage lockout (UVLO) circuit allows the input undervoltage threshold and hysteresis to be independently programmed. Other protection features include thermal shutdown and bias supply undervoltage lockout (V_{CC} UVLO).

For more information, visit http://www.ti.com/product/lm5017.

4.3.2 LM5160

The LM5160 family is a 65-V, 1.5-A synchronous step-down converter with integrated high-side and low-side MOSFETs. The constant-on-time (COT) control scheme requires no loop compensation and supports high step-down ratios with fast transient response. An internal feedback amplifier maintains a ±1% output voltage regulation over the entire operating temperature range. The on-time varies inversely with input voltage resulting in nearly constant switching frequency. Peak and valley current limit circuits protect against overload conditions. The undervoltage lockout (EN/UVLO) circuit provides independently adjustable input undervoltage threshold and hysteresis. The LM5160 is programmed through the FPWM pin to operate in continuous conduction mode (CCM) from no load to full load or to automatically switch to discontinuous conduction mode (DCM) at light load for higher efficiency. Forced CCM operation supports multiple output and isolated Fly-Buck applications using a coupled inductor.

For more information, visit http://www.ti.com/product/lm5160.

4.4 LDO

A number of power rails are required in the TIDA-00661 TI Design. The output of the DC-DC converter is regulated by the LDOs.

This design requires multiple power supplies for the following:

- MCU: 3.3 V
- ADC: 3.3 V, ±2.5 V (3 V or 5 V for unipolar configuration)
- Op amp: 3.3 V
- Relay and FSD: 12 V

DC-DC converters generate ±5.5 V and 12 V. The other supplies that the subsystem requires to operate are generated using LDOs. LDOs provide the stable and accurate power output required for ADC performance. The LDOs selected have a higher current output than required and provide options for further expansion. The LDO current output can be optimized based on the design.

4.4.1 TPS73201

For more information on this LDO regulator, visit http://www.ti.com/product/tps73201-Q1.

4.4.2 TPS72301

For more information on this LDO regulator, visit http://www.ti.com/product/tps72301-Q1.

4.4.3 TPS73230

For more information on this LDO regulator, visit http://www.ti.com/product/tps73230-EP.

4.4.4 TPS7A6533

For more information on this LDO regulator, visit http://www.ti.com/product/tps7a6533-Q1.

4.5 Op Amp and Reference

Op amps and references are used to measure earth fault current inputs using the internal ADC of an MCU. The current must be measured within the specified accuracy to ensure that the trip time is within the allowed time and repeatable. The measurement must also be accurate over a wide range of temperature inputs. The low current input must be amplified to measure the current range within the required accuracy. The op amp drift and offset performance are also important and low drift amplifiers have been selected for this application. The MCU ADC is unipolar. To measure AC input, the input must be level shifted. A LM4041, which is a programmable reference, is used in this TIDA-00661 design to provide the required level shifting. The reference is buffered to support the required current for multiple inputs.

4.5.1 LMV614

The LMV614 series of devices are single, dual, and quad low voltage, low power op amps. These devices have been specifically designed for low voltage, general purpose applications. Other important product characteristics are rail to-rail input and output, a low supply voltage of 1.8 V, and a wide temperature range. The LMV614 input common-mode extends 200 mV beyond the supplies and the output can swing rail-to-rail unloaded and within 30 mV with a 2-kΩ load on a 1.8-V supply. The LMV614 achieves a gain bandwidth of 1.4 MHz while drawing 100-µA (typical) quiescent current.

For more information on this op amp, visit http://www.ti.com/product/lmv614.

4.5.2 LM4041

For more information on this op amp, visit http://www.ti.com/product/lm4041-N.

4.6 Self-Power Regulation Using Comparators and MOSFET

Circuit breakers offer different power supply options. The following two options are commonly used. A possible third option exists that consists of using an AC-DC converter operated from a mains input.

Self-power (rectified-current transformer input)

The input to the self-power supply input is a full wave-rectified current input. This rectified input charges the capacitor to generate the output voltage. The regulated DC output voltage is set by a Zener diode and controlled by a MOSFET-based shunt regulator. The output voltage is compared against a set voltage by the comparator to regulate the output DC voltage.

Dual-power (auxiliary DC or rectified-current transformer input)

An auxiliary DC input voltage can also be applied to generate the required power supply, along with the self-powered current inputs. The shunt regulation is bypassed when the auxiliary voltage is applied. The supply range for the auxiliary input is 18- to 35-V DC. The self-powered output voltage threshold can be set based on the auxiliary input voltage range.

Comparators with a 105°C rating are preferable. The LM2903 device is rated for −40°C to 125°C, which suits this application.

A MOSFET is used as a shunt regulator to shunt the input current when the power supply voltage exceeds 24 V. The low ON resistance ensures lower power dissipation and requires a smaller heat sink. The required shunting voltage is adjustable by using Zener regulation.

4.6.1 LM2903

For more information on this comparator, visit http://www.ti.com/product/lm2903.

4.6.2 CSD18537NKCS

For more information on this MOSFET, visit http://www.ti.com/product/csd18537nq5a.

4.7 Temperature Sensor

The onboard temperature is a useful parameter in circuit breaker applications to provide overtemperature protection. Most of the breakers are specified for 105°C operation. A temperature sensor capable of measuring temperatures greater than 105°C is preferable in this application. The accuracy specified in the LMT87 device is in the operating range of −50°C to 150°C.

4.7.1 LMT87

For more information on this temperature sensor, visit http://www.ti.com/product/lmt87.

4.8 Undervoltage Sensor

For an MCU with fast start-up, a reset generator with a timing in the µs (micro seconds) is required. The MCU reset timing requirement at V_{CC} = 2 V or 3 V is 2 µs (minimum). The propagation delay of the undervoltage sensor is 60 µs to 300 µs. This configuration is one the few options that can be used as a power-on reset.

4.8.1 LM8364

For more information on this undervoltage sensing circuit, visit http://www.ti.com/product/lm8364.

5 AFE With ADC and MCU—Design Theory

5.1 ADC

5.1.1 ΔΣ ADC

The TIDA-00661 design uses an external clock input and internal reference. The schematic in the following 図 2 shows an ADS131E08S ΔΣ ADC configured for a circuit breaker application.

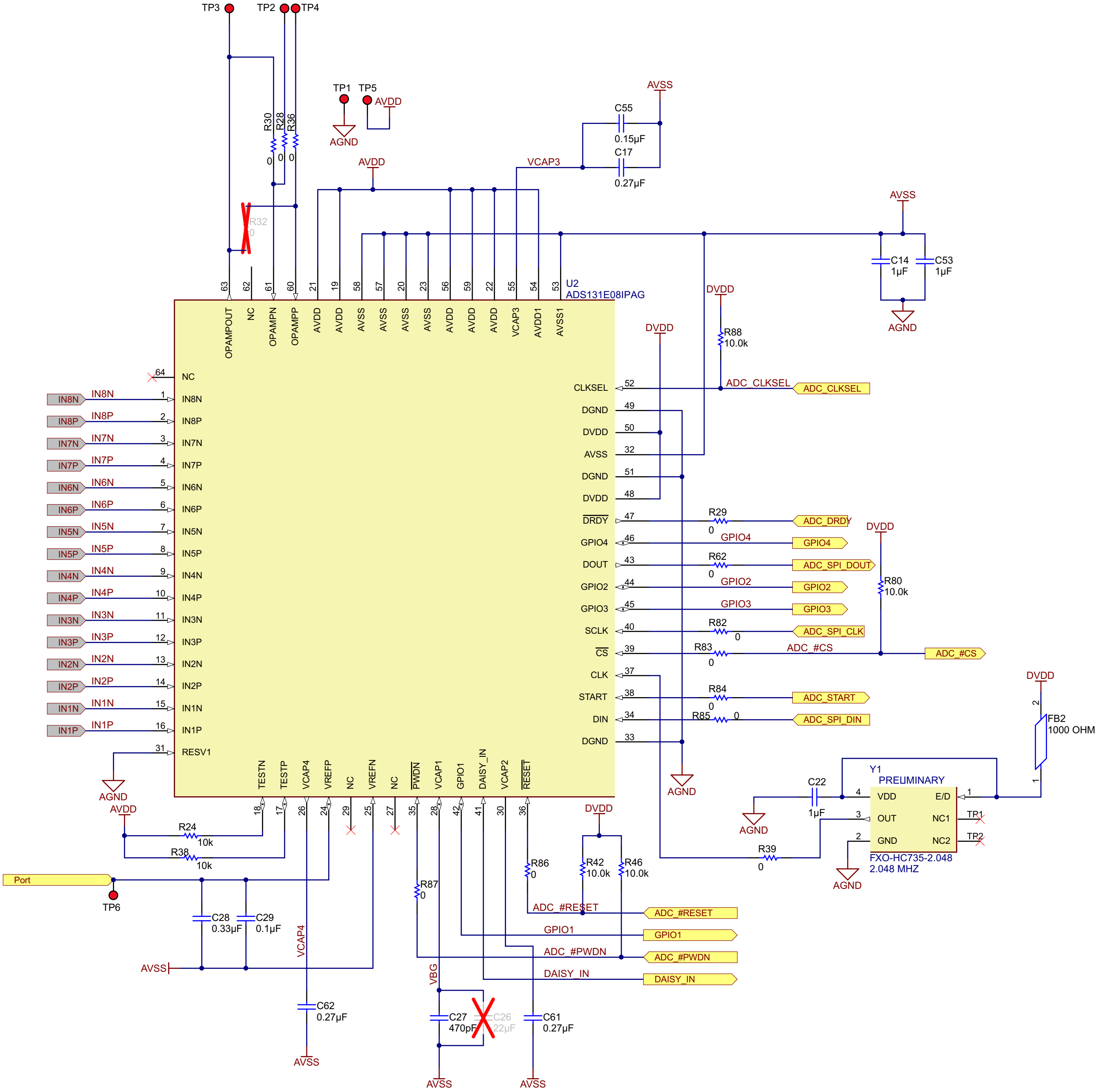


図 2. ADS131E08S Configuration

Analog supply range options:

3 V to 5 V (unipolar)

±2.5 V (bipolar, allows DC coupling)

The analog supply range has been configured for ±2.5 V in this design.

Digital supply range:

1.8 V to 3.6 V

The digital supply has been configured to 3.3 V.

Reference

The internal reference can be programmed to either 2.4 V or 4 V. Testing with this design has been performed using both reference voltages.

The reference voltage is generated with respect to AVSS. When using the internal voltage reference, connect VREFN to AVSS.

The external band-limiting capacitors determine the amount of reference noise contribution. For high-end systems, choose the capacitor values such that the bandwidth is limited to less than 10 Hz, so that the reference noise does not dominate the system noise. When using a 3-V analog supply, the internal reference must be set to 2.4 V. In the case of using a 5-V analog supply, the internal reference can be set to 4 V by setting the VREF_4V bit in the CONFIG2 register.

Gain

The ADS131E0x devices have a highly-programmable multiplexer that allows for various signal measurements including temperature, supply, and input short. The PGA gain can be chosen from one of five settings (1, 2, 4, 8, and 12), as 表 5 shows.

表 5. ADS131E08S PGA Functionality

V_{REF}	PGA GAIN	FULL-SCALE DIFFERENTIAL INPUT VOLTAGE, FSDI (V_{pp})	RMS VOLTAGE [= FSDI / ($2\sqrt{2}$)] (V_{RMS})
2.4 V	1	4.8	1.698
	2	2.4	0.849
	4	1.2	0.424
	8	0.6	0.212
	12	0.4	0.141
4.0 V	1	8	2.828
	2	4	1.141
	4	2	0.707
	8	1	0.354
	12	0.66	0.236

SPI

The SPI-compatible serial interface consists of four signals: CS, SCLK, DIN, and DOUT. The interface reads conversion data, reads and writes registers, and controls the ADS131E0x operation. The DRDY output is used as a status signal to indicate when ADC data is ready for read back. DRDY goes low when new data become available.

Chip select (CS)

Chip select (CS) selects the ADS131E0x for SPI communication. CS must remain low for the entire serial communication duration. After the serial communication is finished, four or more t_{CLK} cycles must elapse before taking CS high. When the CS has been taken high, the serial interface resets, SCLK and DIN are ignored, and DOUT enters a high-impedance state. The DRDY asserts when data conversion has completed, regardless of whether CS is high or low.

Serial clock (SCLK)

SCLK is the SPI serial clock. This signal is used to shift in commands and shift out data from the device. The serial clock (SCLK) features a Schmitt-triggered input and clocks data on the DIN and DOUT pins into and out of the ADS131E0x.

Take care to prevent glitches on the SCLK while the CS is low. Glitches as small as 1 ns wide can be interpreted as a valid serial clock. After eight serial clock events, the ADS131E0x device assumes an instruction must be interrupted and executed. If is the device suspects that instructions are being interrupted erroneously, toggle the CS high and then back low to return the chip to normal operation.

EMI filter

An RC filter at the input acts as an EMI filter on all channels. The –3-dB filter bandwidth is approximately 3 MHz.

GPIO

The ADS131E0x devices have a total of four general-purpose digital I/O (GPIO) pins available in the normal mode of operation. The digital I/O pins are individually configurable as either inputs or outputs through the GPIOC bits register. These GPIOs can be used to configure the measurement current range of the breakers for a wider dynamic range performance.

Clock

The ADS131E0x device provides two different device clocking methods, internal and external. Internal clocking is ideally suited for low-power, battery-powered systems. The internal oscillator is trimmed for accuracy at room temperature. Accuracy varies over the specified temperature range

5.1.2 AC Voltage Input

The ADC board has the following options to measure AC input voltages:

- Measure three AC voltage inputs.
- An AC input of up to 750 V can be measured with a gain (or X2) and reference of 2.4 V.
- An AC input of up to 900 V can be measured with a gain (or X2) and reference of 4 V.
- The AC input is divided using a potential divider and applied as an input of the ADC. Select the potential divider values to ensure that the ADC input saturates at approximately 750 V for a 2.4-V reference when the gain has been programmed to X2.

The schematic in the following 図 3 shows the connector and potential divider for the voltage input in this design.

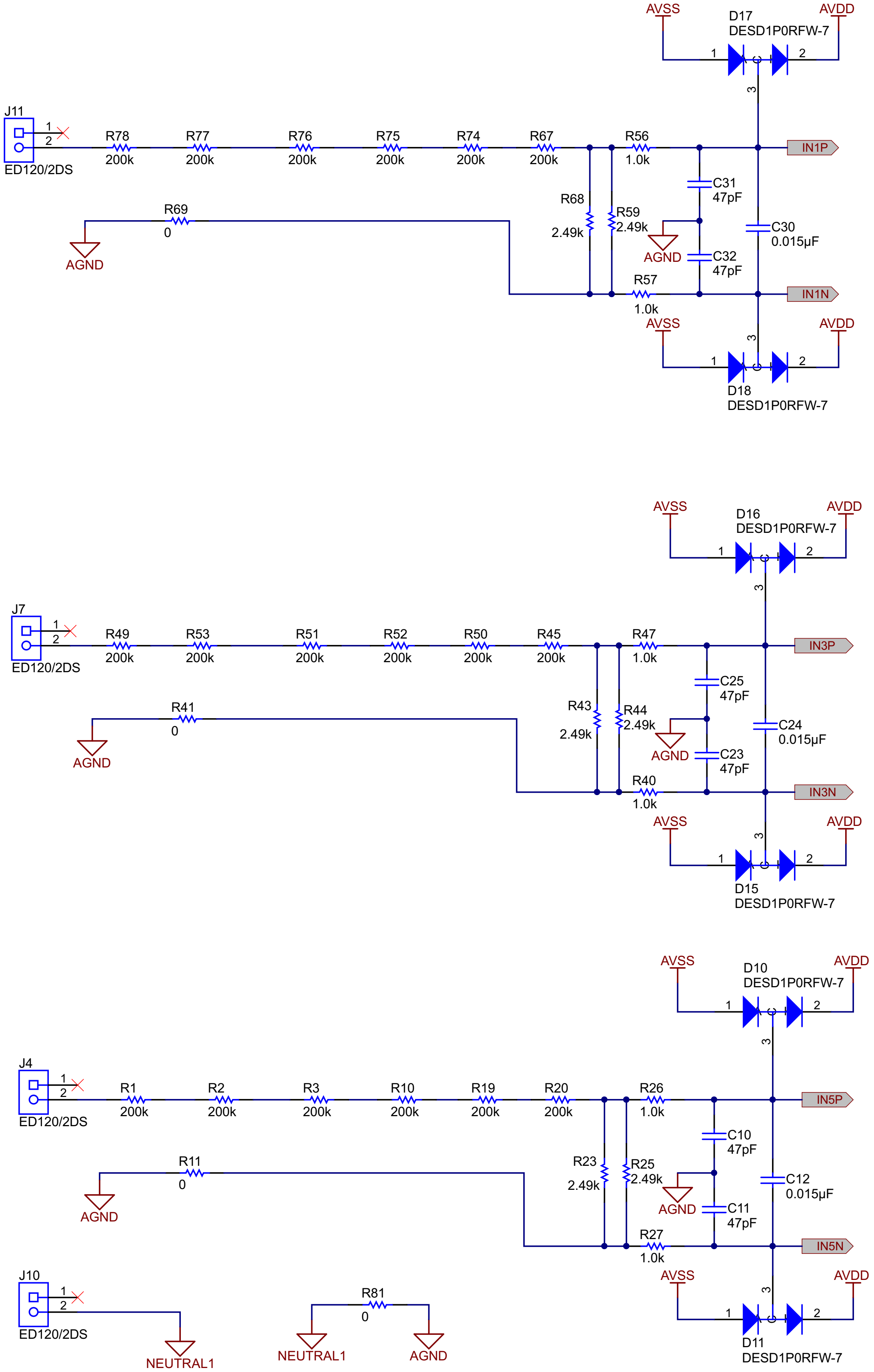


図 3. Voltage Input—Connector and Potential Divider for Three Phases

5.1.3 Current Input

This TIDA-00661 design has a provision to measure up to five inputs. The current transformer (CT) input can be single-ended or differential. CTs are external to the ADC board and the secondary of the CT can be connected to the ADC. Onboard burden resistors have been provided and the output of the burden resistors connects to the ADC.

To test the performance of the ADC, use a CT with a 1:500 ratio and select the burden to ensure that the ADC input saturates at approximately 25 A with a gain of X2.

The schematic in the following 図 4 shows the current input with connector.

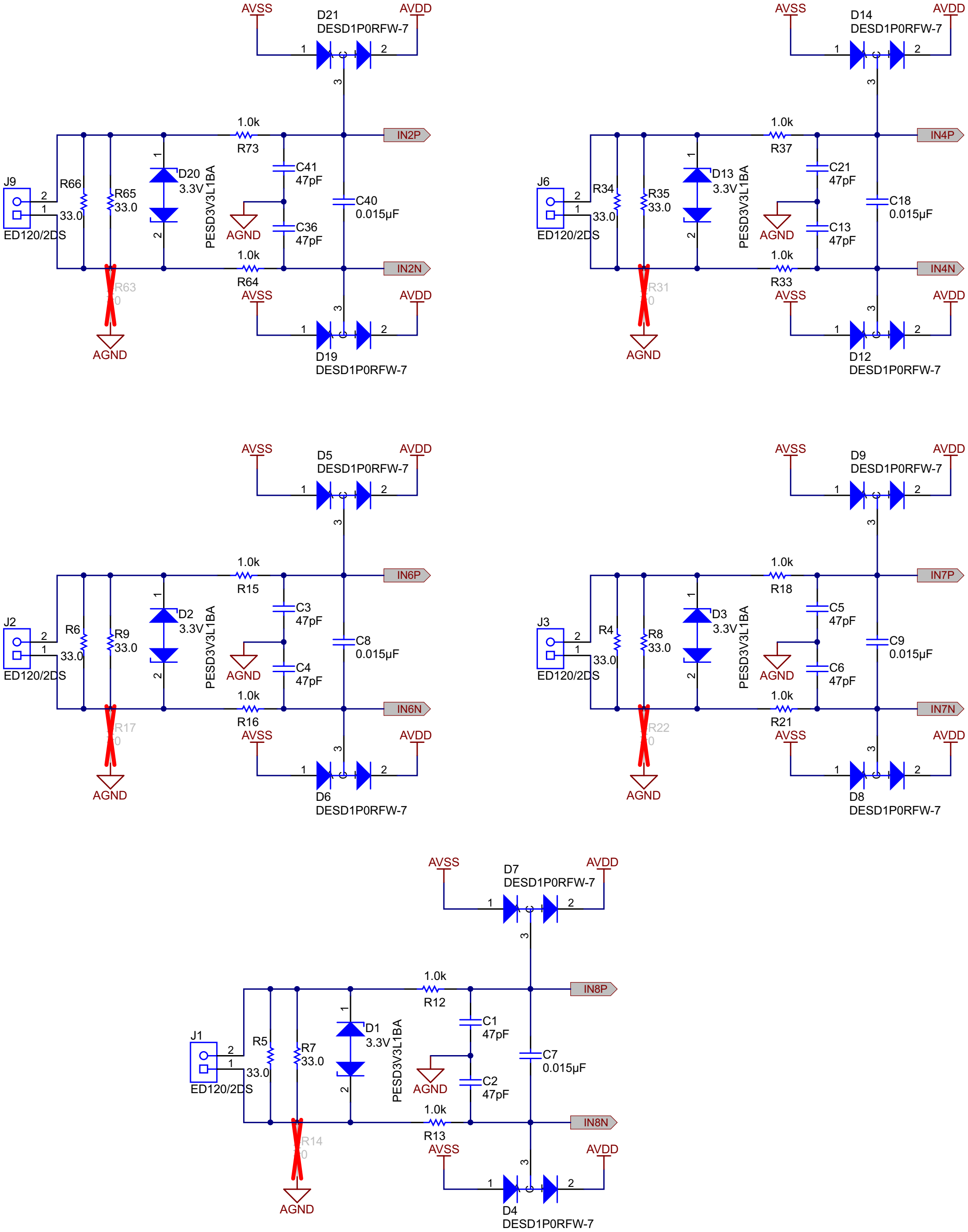


図 4. Current Input Connectors

注: **Regarding current input and burden**: Do not apply current without connecting the CT secondary to the connectors.

The burden resistor is secondary current-dependent and changes with the current transformer type. The total from the secondary current multiplied by the burden must not exceed a 1250-mV peak with the PGA gain configuration of X2 and V_{REF} of 2.4 V.

5.2 MCU

5.2.1 MSP430F5969

The MCU in this TIDA-00661 design (see 図 5) has the following interfaces:

- ADC input: A 12-bit ADC with an option to scan the current input channels
- ADC reference: The reference option selected is the external reference and 3.3 V
- Oscillator: The MCU can operate with a digitally controlled oscillator (DCO), 32 kHz or, or 8-MHz oscillator; this design uses a DCO
- GPIO for LEDs: Two onboard LEDs are available and the user can utilize these LEDs for the required system functionality
- GPIO for MOSFET control to drive FSD and relay drive: A MOSFET driver for FSD is available
- JTAG: A 14-pin JTAG interface is available for programming
- PWM control of self-power: The self-powered DC inputs are sensed and controlled using a PWM from the microcontroller, which is in addition to the hardware shunt regulation
- Interface connector: An interface connector with UART, SPI, and I^{2}C interface signals are available for future expansion
- Power on reset: A 60- to 300-µs power on reset is available

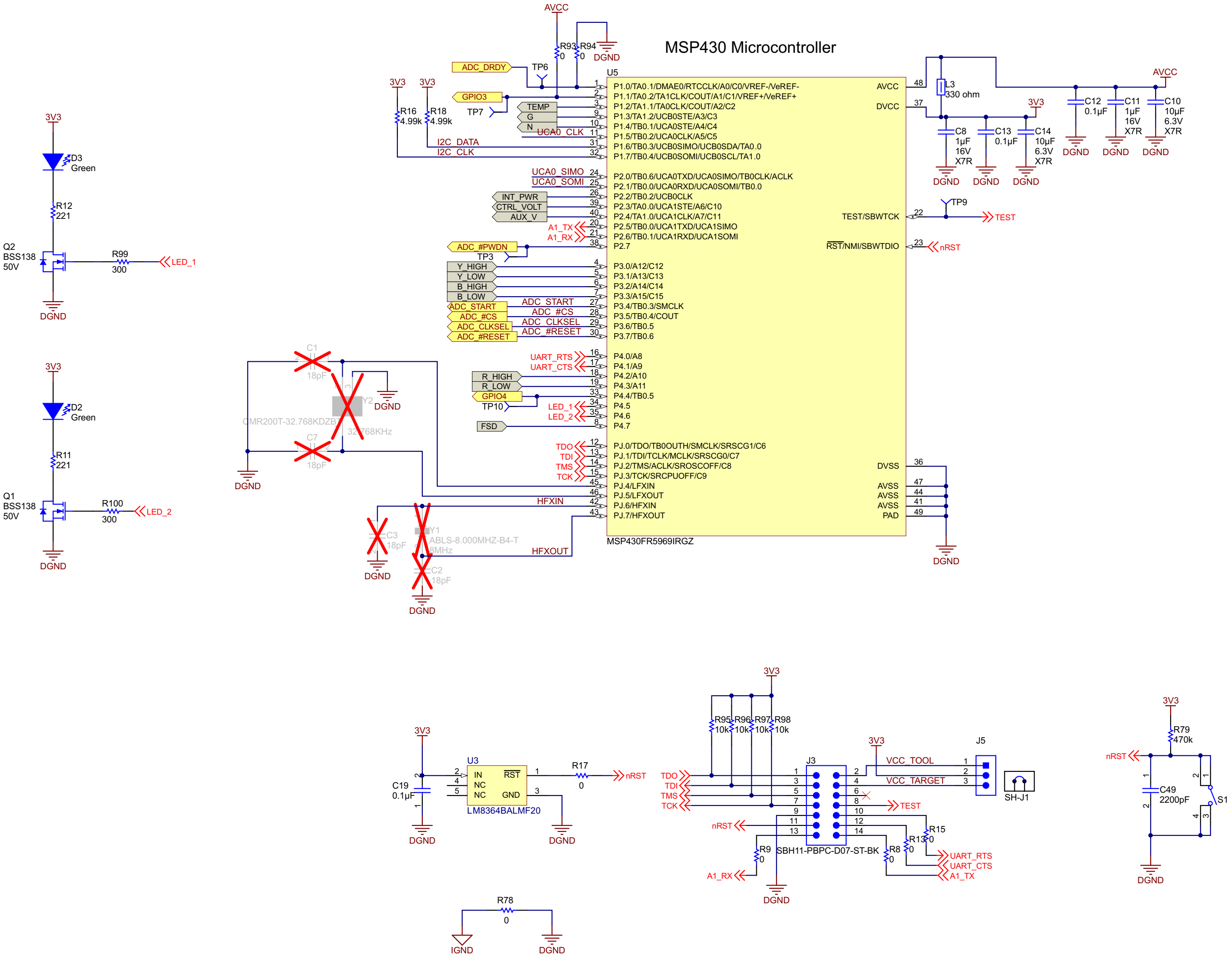


図 5. MCU Configuration

SPI to ADC

The eUSCI_A0 and eUSCI_A1 signals support an SPI at rates of up to 10 Mbps. The clock speed required for interfacing with the ADC varies with the sampling rate. For example, if the ADS131E0x device is used in an 8-kSPS mode (eight channels, 24-bit resolution), the minimum SCLK speed is 1.755 MHz. The sampling rates chosen are typically between 4 kSPS for breaker applications.

5.3 *Self-Power With Comparators and MOSFET*

Breakers have different power supply options. The following two options are common options and have been provided in this design. A possible third option exists, which consists of using an AC-DC converter.

Self-power (current sensor input based)

The input to the self-power supply input is a full wave-rectified current input. This rectified input charges the capacitor to generate the output voltage. The regulated DC output voltage is set by a Zener diode and controlled by a MOSFET-based shunt regulator. The output voltage is compared against a set voltage by the comparator to regulate the output DC voltage.

Dual-power (auxiliary DC or current transformer based)

An auxiliary DC input voltage can also be applied to generate the required power supply along with the self-powered current inputs (see 図 6). The shunt regulation is bypassed when an auxiliary voltage is applied. The supply range for the auxiliary input is 18- to 35-V DC. The self-power output voltage threshold can be set based on the auxiliary input voltage range.

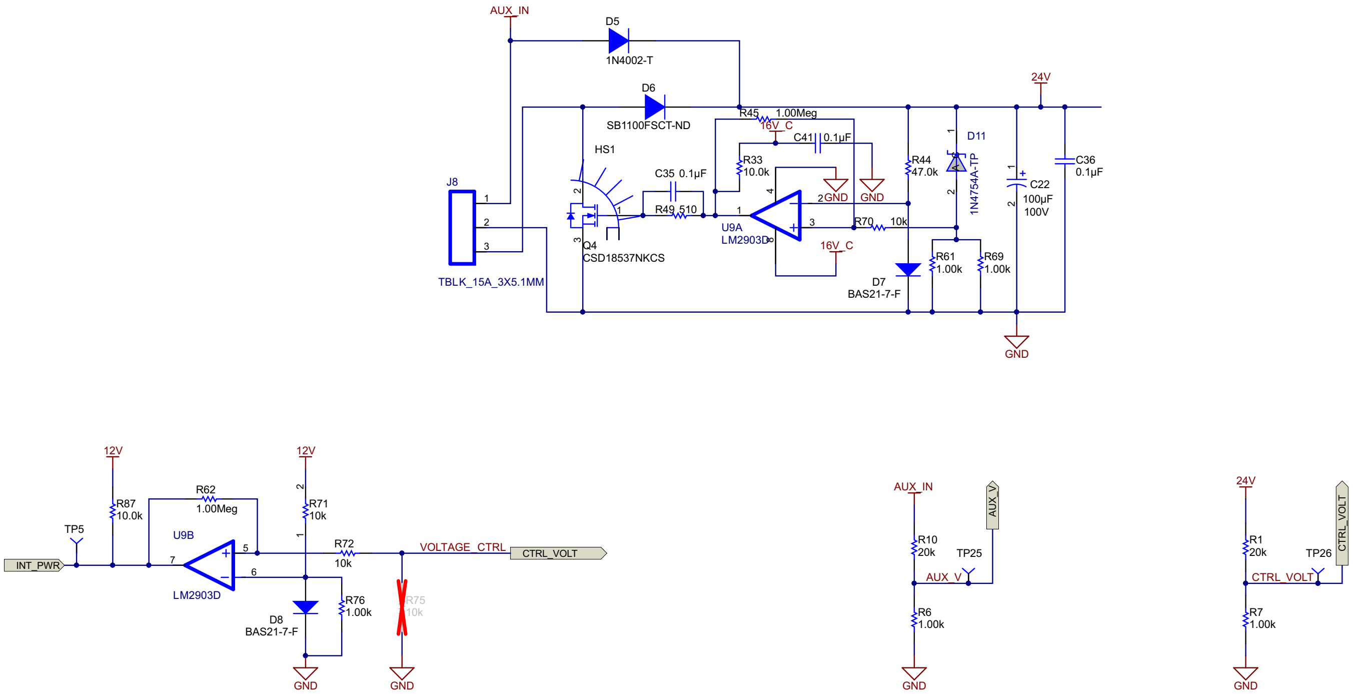


図 6. Self-Power Regulator

Rectified current inputs-based self-power supply

The rectified current input-based shunt regulator can be configured to regulate voltage ≥ 24 V. The TIDA-00661 design uses a TI MOSFET to shunt the current above the configured output voltage. Increased regulation voltage reduces power dissipation and facilitates the use of a lower VA output-rated current transformer. TI has a wide range of MOSFETs that can be selected for current shunting based on the application and the configured regulation voltage.

The self-power supply generates the output voltage from the input currents. The input to the self-power generation circuit is a rectified output from the current transformers. The rectifier diodes must be connected externally. The Zener diode reference regulates the self-power to the configured voltage. If the output voltage exceeds the configured voltage, the comparator switches the MOSFET and the MOSFET shunts the rectified input current, which limits the current input to the power supply. When the output voltage reduces, the comparator switches the MOSFET off and the input current charges the output capacitor. The advantage of this self-powering circuit is a reduced loading on the current transformer.

The critical component in the self-powering circuit is the shunt regulation MOSFET. 表 6 lists a wide range of available MOSFETs for current shunting.

表 6. TI MOSFETs With Current Shunting

PRODUCT DESCRIPTION	PRODUCT LINK
60-V, N-Channel NexFET™ Power MOSFET	CSD18537NKCS
60-V, N-Channel NexFET Power MOSFET	CSD18534KCS
80-V, N-Channel NexFET Power MOSFET	CSD19506KCS
80-V, 7.6-mΩ, N-Channel TO-220 NexFET Power MOSFET	CSD19503KCS
100-V, N-Channel NexFET Power MOSFET	CSD19535KCS
100-V, 6.4-mΩ, TO-220 NexFET Power MOSFET	CSD19531KCS

Auxiliary DC voltage inputs

Another option to power the TIDA-00661 design is to use an auxiliary 24-V input.

After the DC auxiliary voltage has been applied, the MOSFET-based shunt regulation is bypassed. A provision exists to detect whether or not the auxiliary voltage has been applied.

5.4 DC-DC Converter

The Fly-Buck converter is a versatile, isolated-power solution and offers a simple and cost-effective way to generate multiple isolated outputs. For low-power applications, a Fly-Buck converter is an excellent candidate to replace a traditional flyback converter.

A Fly-Buck regulator provides primary output voltage along with secondary outputs. The primary voltage (V_{PRI}) is V_{IN} × duty cycle. The output current along the V_{PRI} is 600 mA for the LM5017 (PMP10558) and 1.5 A for the LM5160 (PMP10532). The available current capability in V_{PRI} is equal to the total V_{PRI} current minus the secondary side currents (reflected back to the primary side).

5.4.1 LM5017

The TIDA-00661 design is based on using the PMP10558 Fly-Buck power supply. Refer to http://www.ti.com/tool/PMP10558 for more details on this device.

The PMP10558 reference design is a low-profile, triple output isolated, Fly-Buck power supply for industrial applications. The power supply has a synchronous buck regulator, LM5017, and a low profile (6-mm) transformer. This reference design generates three isolated outputs depending on the transformer selection. The LM5017 is a 100-V wide V_{IN}, 600-mA synchronous buck regulator. The input voltage range of the design is 18 V to 30 V, which make it a suitable option for 24-V input industrial applications. The Fly-Buck power supply can regulate the secondary side outputs without an optocoupler or auxiliary winding and is capable of achieving good cross regulation within ±5%. With the constant on-time control of the LM5017, no loop compensation is required, which simplifies the design and helps to reduce the external part count and bill of materials (BOM) cost.

Output voltage specifications:

- 12 V, 80 mA – Used for driving a flux shift device (solenoid drive) or relays
- 5.5 V, 150 mA – Used to generate power for MCU operation and provide an option for future expansion)
- –5.5 V, 100 mA – Used to generate negative power for ADC operation)

Input specifications:

- V_{IN} range: 18 V to 30 V
- Nominal V_{IN}: 24 V

- Switching frequency F_{SW}: 350 kHz

When using the Fly-Buck controller, the primary side can be regulated as a buck while simultaneously being used to control the secondary output; this function enables the topology to utilize primary-side regulation (PSR). By sufficiently regulating the primary side output, the user can indirectly control the isolated output without the use of any additional circuitry.

The Fly-Buck controller cannot achieve the same high level of accuracy as with the flyback using optocouplers. Through proper design, the level of accuracy of using the Fly-Buck controller falls in the range of ±5% regulation, which is well enough for many applications.

Populate R85, R86, and R91 to select the LM5017 voltage outputs and remove R52, R56, and R57 to disconnect the LM5160 voltage outputs (see 図 7).

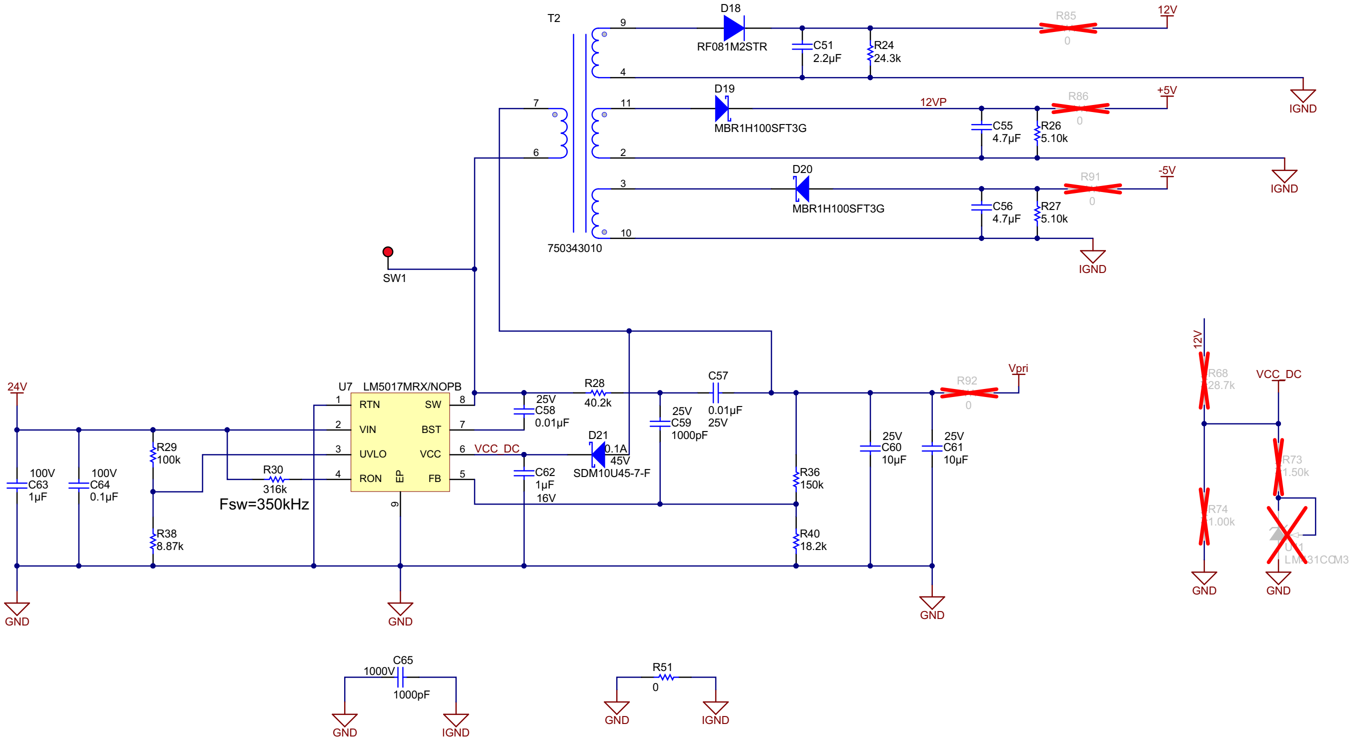


図 7. LM5017 Configured for Fly-Buck Operation

5.4.2 LM5160

The TIDA-00661 design is based on using the PMP10532 Fly-Buck power supply. Refer to http://www.ti.com/tool/PMP10532 for more details on this device.

The PMP10532 reference design is an isolated Fly-Buck power supply for industrial applications. This reference design takes a 24-V nominal input and provides three isolated outputs: 5 V, –5 V, and 12 V. The cross regulation of each output over line and load variation maintains an approximate ±5% tolerance and the input voltage range of the supply is from 19 V to 30 V. The design features the LM5160 synchronous buck converter configured as a Fly-Buck regulator. The LM5160 has a wide V_{IN} range of 4.5 V to 65 V and a 1.5-A output current capability with integrated switch FETs. This reference design employs the COT control scheme suitable for the Fly-Buck configuration. With the benefit of PSR, the Fly-Buck converter makes a compact and cost-effective solution for multiple, isolated output, power supply rails without the optocoupler feedback.

Features:

- Fly-Buck converter design, primary-side regulation
- Compact solution for multiple, isolated output supplies
- 19- to 30-V input voltage range, ±5% V_{OUT} cross regulation
- LM5160 synchronous buck regulator with up to a 65-V wide V_{IN} range (1.5-A capability)
- COT control, no loop compensation, and fast transient response

Output voltage specifications

- 12 V, 200 mA – Used for driving a flux shift device (solenoid drive) or relays
- 5.5 V, 1000 mA – Used to generate power for MCU operation and provide an option for future expansion
- –5.5 V, 50 mA – Used to generate negative power for ADC operation

Input specifications

- Nominal V_{IN}: 24 V
- V_{IN} range: 19 V to 30 V
- Switching frequency F_{SW}: 250 kHz

Remove R85, R86, and R91 to disconnect the LM5017 voltage outputs and populate R52, R56, and R57 to select the LM5160 voltage outputs (see 図 8).

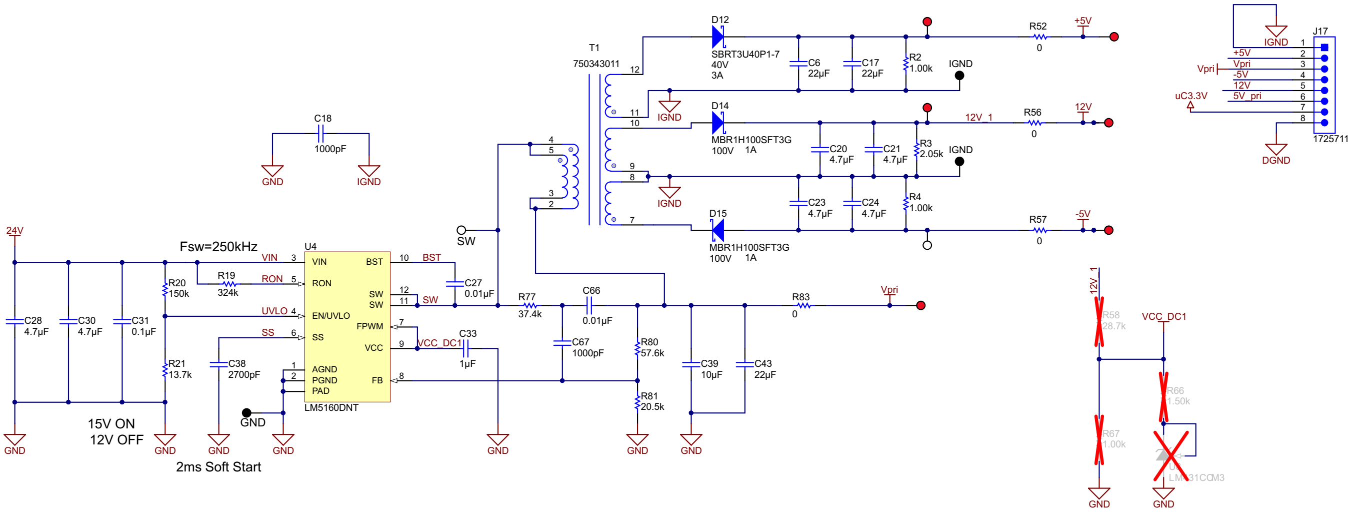


図 8. LM5160 Configured for Fly-Buck Operation

5.5 LDO

5.5.1 ADC Board

The power supply requirement for the ADC is as follows.

Analog supply: 3 V to 5 V (unipolar) and ±2.5 V (bipolar, allows DC coupling)

The following onboard regulators have been provided: 3 V, 2.5 V, and –2.5 V.

The following schematic in 図 9 shows the LDOs for an ADC analog supply as used in the TIDA-00661 design.

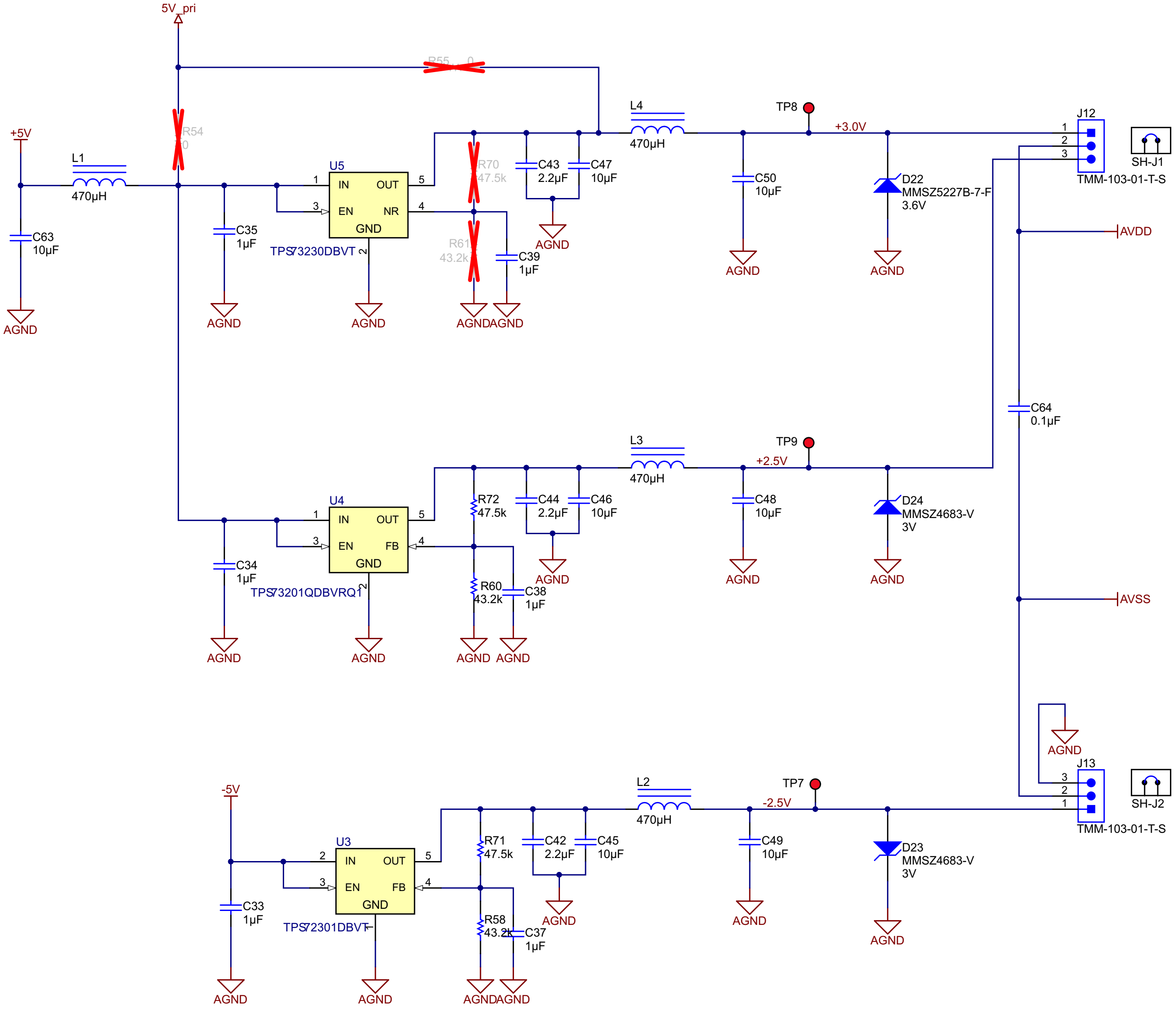


図 9. LDO for ADC Analog Supply

The ADC can work with a 5-V, 3-V, or ±2.5-V analog supply. Jumper J12 and J13 can be used to configure the analog supply range of the ADC. The analog supply range in this design has been configured for ±2.5 V. To configure for ±2.5 V, U3 and U4 are not populated and U5 is not populated. To configure the power supply to 3 V, U5 is populated and U3 and U4 are not populated. To configure the power supply to 5 V, R55 is populated and U3, U4, and U5 are not populated.

Digital Supply: The ADC can operate in the range of 1.8 V to 3.6 V. The digital supply has been configured to 3.3 V. The MCU provides the 3.3 V through the interface connector.

5.5.2 MCU Board

The following LDOs have been provided on the MCU board: 3.3 V (using a 5.5-V secondary output) and 5 V (using the V_{PRI} output, which is 8 V to 10 V).

In the TIDA-00661 design, the 5-V output is generated by using V_{PRI}. This 5 V can be used in addition to the secondary 5-V supply depending on the application requirement. 5.4 explains the current output capability of V_{PRI}.

The schematic in 図 10 shows the 3.3-V LDO for the ADC and MCU board and 図 11 shows a schematic of the primary 5-V DC output regulator.

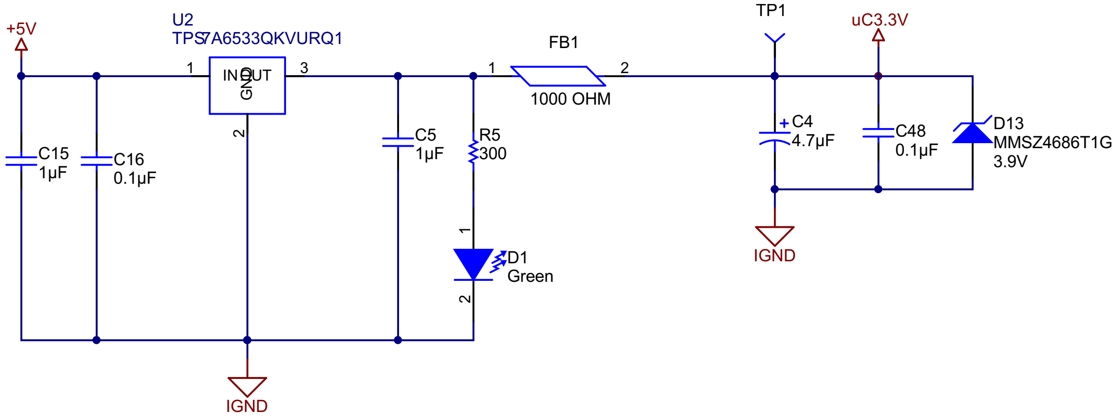


図 10. 3.3-V LDO for ADC and MCU Board

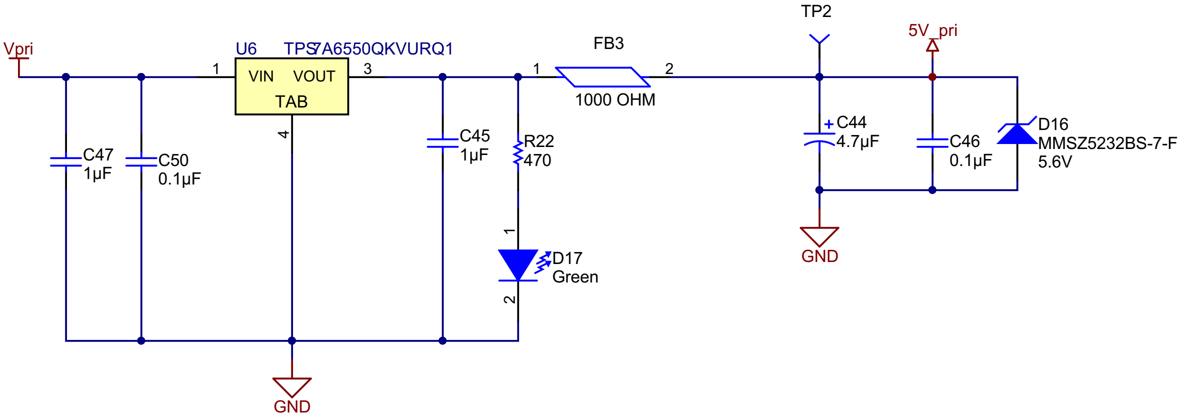


図 11. Primary-Side DC Output Regulator

5.6 Earth Fault Current Input With Op Amp and Reference

The neutral and ground amplifiers must measure between 0.05 in to 1.00 in. The TIDA-00661 design provides a single gain stage of X5.7. The gains are modifiable based on the requirement. Jumpers are provided to select the level shifting between 0 V and 1.65 V.

The LM4041 reference has been programmed to provide a level shift of V_{CC} / 2. The reference output is buffered with an op amp.

The schematic in the following 図 12 shows the signal conditioning circuit for earth fault current measurement.

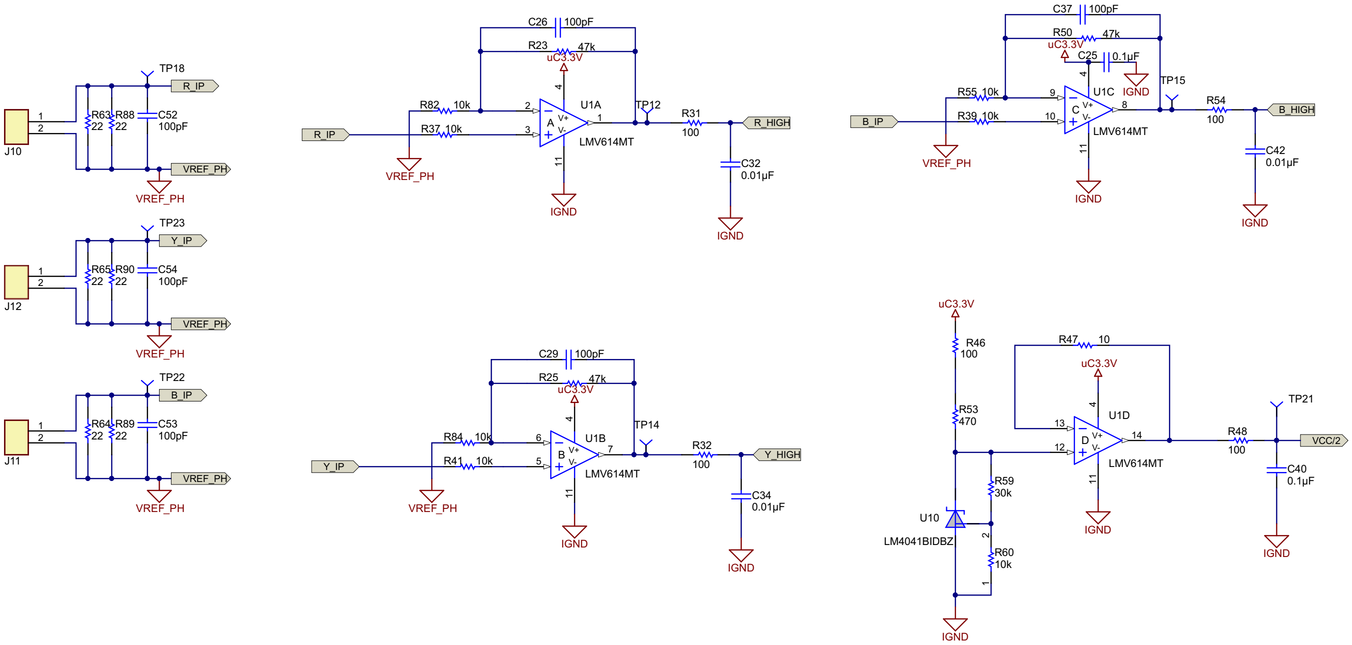


図 12. Earth Fault Current Signal Conditioning

Earth fault current input connector

The majority of breaker applications use current transformers (CT) and are part of the enclosure. The secondary output of the current sensors is connected to the MCU. Connectors with burden resistors are available to connect a total of three current inputs. The AC current input connects to the signal conditioning circuit using the above connectors. The required burden resistor and filter capacitors have been provided across the connectors.

注: Regarding current input and burden: Do not apply current without connecting the CT secondary to the connectors. The burden resistor is secondary current-dependent and changes with the current transformer type. The total from the secondary current multiplied by the burden must not exceed a 250-mV peak with the amplifier gain configuration in the current design.

5.7 MCU and ADC Boards Interface

The ADC board connects to the MCU board using the interface connector. The interface connector has the required signals for interconnecting the two boards for the purposes of communication and capturing analog input samples.

The schematics in 図 13 and 図 14 show the interface connector from the MCU board to ADC board and vice versa.

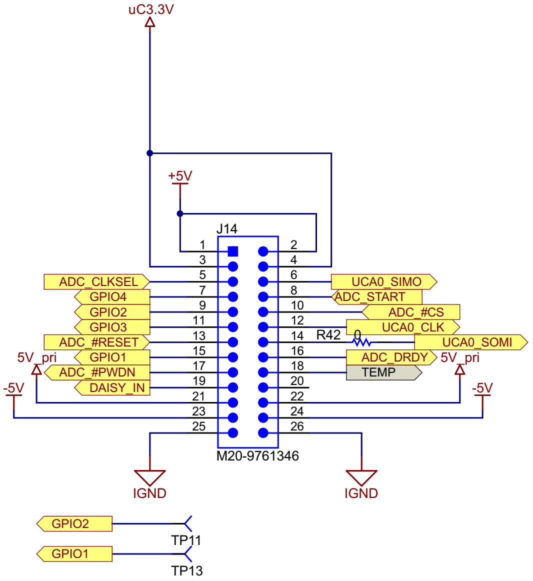


図 13. Interface Connector—From MCU Board to ADC Board

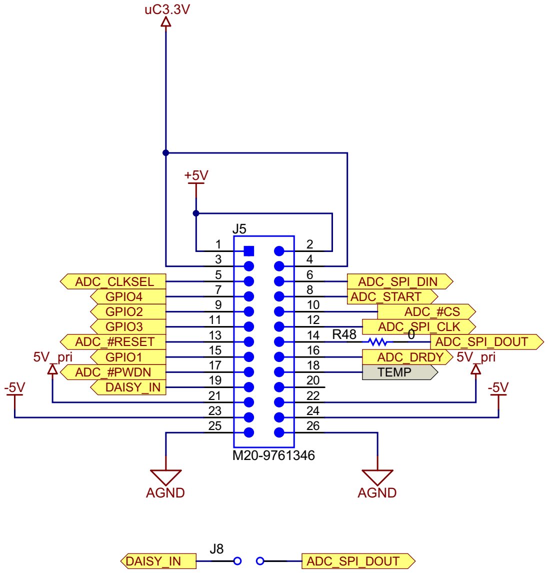


図 14. Interface Connector—From ADC Board to MCU Board

注: The user can connect the ADS131E08S ADC in daisy-chain mode. This design includes a provision to connect the ADC in daisy-chain mode; however, this configuration has not been tested.

5.8 Interface Between MMB0 (Modular EVM Motherboard) and ADC Board

The ADC board has been designed with the intention of interfacing with the MMB0 (modular EVM motherboard), which functions to evaluate the ADS131E08 ADC. The schematic in 図 14 shows the connector on the ADC board. 表 7 shows the interconnection between the ADC board and the MMB0 board.

表 7. Connection From ADC (ADS131E08S) Board to MMB0 Board

ADC BOARD J5 PINS	DESCRIPTION (SIGNAL ON MMB0 BOARD)	MMB0 BOARD J4 PINS
1	5 V from external DC power supply (analog supply)	
2		
3	3.3 V from external DC power supply (digital supply)	
4		
5	Gnd(Clk_sel)	4
6	Spi_Din	11
7		
8	ADC_Start	14
9		
10	CS	1
11		
12	SPI_Clk	3
13	Reset	8
14	SPI_Out	13
15		
16	DRDY	15
17		
18		
19		
20		
21		
22		
23	–5 V from external DC power supply (analog supply)	
24		
25	Gnd	18
26		

5.9 Temperature Sensor

The temperature sensor can measure a range between −50°C to 150°C, which meets the required operation range of −20°C to 105°C. The following schematics in 図 15 and 図 16 show the onboard temperature sensor. The following 表 8 lists the load capacitor and series resistor requirements.

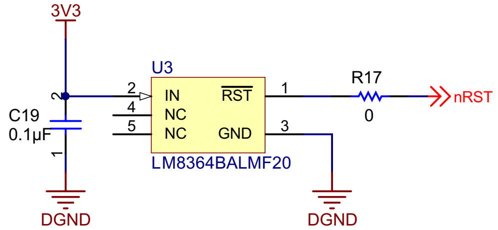


図 15. Onboard Temperature Sensor

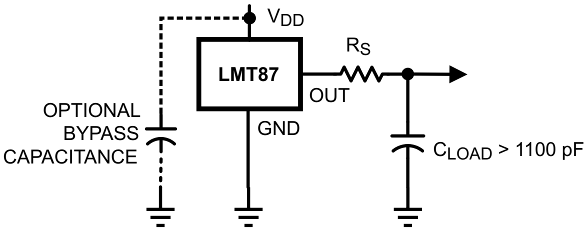


図 16. LMT87 With Series Resistor for Capacitive Loading Greater than 1100 pF

表 8. Capacitive Loading for LMT87

C_{LOAD}	MINIMUM R_S
1.1 nF to 99 nF	3 kΩ
100 nF to 999 nF	1.5 kΩ
1 µF	800 Ω

5.10 *Undervoltage Sensor*

Undervoltage sense input to MCU

The MCU reset timing requirement at V_{CC} = 2 V or 3 V is 2 µs (minimum). The propagation delay of the undervoltage sensor is 60 µs to 300 µs. This configuration is one of the options that the user can implement as a power-on reset (see 図 17). The device has a threshold of 2 V.

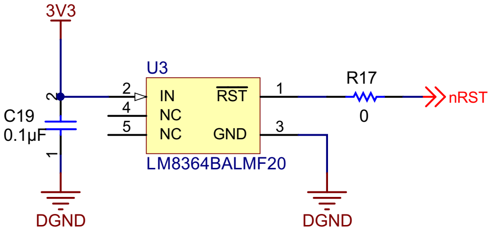


図 17. MCU Reset Control

5.11 *ADS131E08 EVM*

The ADS131E08EVM-PDK is a demonstration kit for the ADS131E08, a simultaneous sampling, 24-bit, ΔΣ ADC with a built-in PGA, internal reference, and an onboard oscillator. The ADS131E08 contains the features commonly required for industrial power monitoring and control but has the flexibility to fit a variety of applications which require an eight-channel, 24-bit ADC. The ADS131E08EVM-PDK demonstration kit is designed to expedite evaluation and system development.

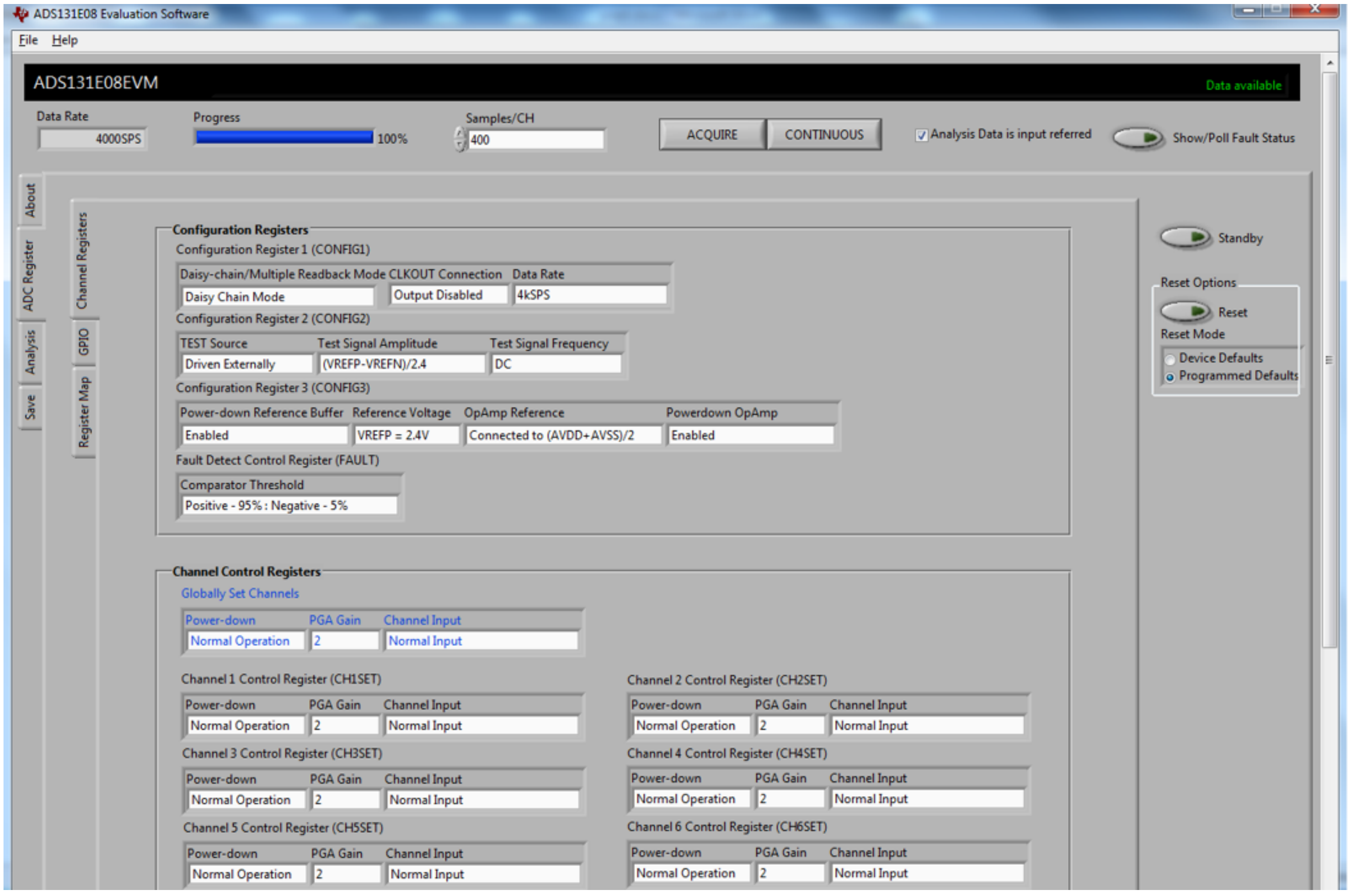
Features

- Easy-to-use evaluation software for Microsoft™ Windows XP or Windows 7
- Built-in analysis tools including oscilloscope, FFT, and histogram displays
- Flexible input configurations
- Optional external reference circuits
- Ability to export data in simple test files for post processing

注: The ADC board has been replaced with the TIDA-00661 ADC board for performance testing.

5.12 Graphical User Interface (GUI)

A graphical user interface (GUI) is used to evaluate the ADC along with the MMB0 board, as 図 18 shows.



Data Rate: 4000SPS

Progress: 100%

Samples/CH: 400

☑ Analysis Data is input referred

Reset Mode

○ Device Defaults

● Programmed Defaults

Configuration Registers

Configuration Register 1 (CONFIG1)

Daisy-chain/Multiple Readback Mode	CLKOUT Connection	Data Rate
Daisy Chain Mode	Output Disabled	4kSPS

Configuration Register 2 (CONFIG2)

TEST Source	Test Signal Amplitude	Test Signal Frequency
Driven Externally	(VREFP-VREFN)/2.4	DC

Configuration Register 3 (CONFIG3)

Power-down Reference Buffer	Reference Voltage	OpAmp Reference	Powerdown OpAmp
Enabled	VREFP = 2.4V	Connected to (AVDD+AVSS)/2	Enabled

Fault Detect Control Register (FAULT)

Comparator Threshold
Positive - 95% : Negative - 5%

Channel Control Registers

Globally Set Channels

Power-down	PGA Gain	Channel Input
Normal Operation	2	Normal Input

Channel 1 Control Register (CH1SET)

Power-down	PGA Gain	Channel Input
Normal Operation	2	Normal Input

Channel 2 Control Register (CH2SET)

Power-down	PGA Gain	Channel Input
Normal Operation	2	Normal Input

Channel 3 Control Register (CH3SET)

Power-down	PGA Gain	Channel Input
Normal Operation	2	Normal Input

Channel 4 Control Register (CH4SET)

Power-down	PGA Gain	Channel Input
Normal Operation	2	Normal Input

Channel 5 Control Register (CH5SET)

Power-down	PGA Gain	Channel Input
Normal Operation	2	Normal Input

Channel 6 Control Register (CH6SET)

Power-down	PGA Gain	Channel Input
Normal Operation	2	Normal Input

図 18. ADS131E08 EVM GUI

The GUI can be used to set the gain, sampling rate, and the number of samples to be captured. Using the GUI, the user can view waveforms and RMS values.

Refer to SBAU200 for additional information.

5.13 Selection of Potential Dividers

The potential divider (resistor voltage divider) is used to divide the AC input (≤ 900-V RMS) to levels that the ADC can measure accurately without saturation. The input to the ADC is protected for overvoltage. Multiple resistors have been used in this design to withstand transient voltage. The designer can optimize the number of resistors depending on the application type and based on testing.

CAUTION

Regarding the high-voltage AC input: An AC input up to 900 V can be applied for measurement purposes. The user must be careful not to touch the board while applying AC voltage.

5.14 Self-Test for ADS131E08S

The SELF-TEST SIGNAL can be generated to test the ADC channels. The signal frequency can be f_{CLK} / 221 or f_{CLK} / 220 Hz. The signal voltage can be ±1 or ±2 mV and the accuracy ±2%.

Test signals (TESTP and TESTN)

Setting CHnSET[2:0] = 101 provides internally-generated test signals for use in the subsystem verification at power up. Test signals are controlled through register settings (see the *CONFIG2: Configuration Register 2* subsection in the *Register Map* section of the SBAS705 datasheet for details). The TEST_AMP register controls the signal amplitude and the TEST_FREQ register controls switching at the required frequency. The test signals are multiplexed and transmitted out of the device at the TESTP and TESTN pins. A bit register (CONFIG2.INT_TEST = 0) deactivates the internal test signals so that the test signal can be driven externally. This feature allows the calibration of multiple devices with the same signal.

5.15 Future Enhancements

5.15.1 Improved Measurement Accuracy With ADS131E08

If a fast startup is not of high importance and a higher measurement accuracy is required to be achieved, the ADS131E08 can be used for measurement. Using the ADS131E08, a ±0.2% measurement accuracy can be achieved for a wide dynamic range of Input. Make the following changes to use the ADS131E08 for testing:

- Populate C26
- Replace C61 with 1 µF
- Change U2 of the TIDA-00661-BE1 ADC board to the ADS131E08
- Replace C17 with 1 µF
- Replace C62 with 1 µF

5.15.2 Interface to TIDA-00499 (DFR AFE)

The TIDA-00499 digital fault recorder (DFR) provides an option for four voltage inputs with a differential amplifier interface.

The output range is 0 V to 5 V and the TIDA-00661 design has the required power output to interface to the TIDA-00499 design for testing a single-ended, 0- to 5-V differential input. The 5V_PRI output can be used for powering the TIDA-00499 board and this provides the required power output. Refer to the TIDUAT7 user's guide for more details on the TIDA-00499.

5.15.3 Interface to TIDA-00555 (Interface for Isolated Voltage and Current Measurement)

The TIDA-00555 design includes a provision to measure isolated current and voltage inputs. The output of the AMC1100 used in TIDA-00555 is compatible with the ADS131E08S device input. The board operates on a 5-V input. The TIDA-00555 and TIDA-00661 boards can be combined for measuring isolated current and voltage inputs. Refer to TIDUA58 for more details on the TIDA-00555.

5.16 Design Guidelines

5.16.1 Layout Guidelines for ADC

Power supplies and grounding

The ADS131E08S has three supplies: AVDD, AVDD1, and DVDD. Both AVDD and AVDD1 must be as quiet as possible. AVDD1 provides the supply to the charge pump block and has transients at f_{CLK}. Therefore, TI recommends that AVDD1 and AVSS1 be star-connected to AVDD and AVSS. Eliminating noise from AVDD and AVDD1 that is non-synchronous with device operation is important. Bypass each ADS131E08S supply with 10- and 0.1-μF solid ceramic capacitors. TI recommends placing the digital circuits, such as digital signal processors (DSPs), microcontrollers, and field-programmable gate arrays (FPGAs), in the system such that the return currents on those devices do not cross the ADS131E08S analog return path. The ADS131E08S can be powered from unipolar or bipolar supplies. The decoupling capacitors can be surface-mount, low-cost, low-profile multi-layer ceramic. In most cases the VCAP1 capacitor can also be a multilayer ceramic; however, in systems where the board is subjected to high- or low-frequency vibration, TI recommends installing a non-ferroelectric capacitor (such as a tantalum or class 1 capacitor, C0G or NPO for example). EIA class 2 and class 3 dielectrics (such as X7R, X5R, and X8R) are ferroelectric. The piezoelectric property of these capacitors can appear as electrical noise coming from the capacitor. When using the internal reference, noise on the VCAP1 node results in performance degradation.

Shielding analog signal paths

As with any precision circuit, a careful PCB layout ensures the best performance. Making short, direct interconnections and avoiding stray wiring capacitance is essential, particularly at the analog input pins and AVSS. These analog input pins are high-impedance and extremely sensitive to extraneous noise. The AVSS pin must be treated as a sensitive analog signal and connected directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the ADS131E08S input bias current if shielding has not been implemented. Digital signals must be kept as far as possible from the analog input signals on the PCB.

5.16.2 Layout Guidelines for DC-DC Converter—LM5160

A proper layout is essential for optimum performance of the circuit. Observe the following guidelines in particular:

- C_{IN}: The loop consisting of the input capacitor (C_{IN}), V_{IN} pin, and PGND pin carries the switching current. Therefore, in both the LM5160 and the LM5160A devices, the input capacitor must be placed close to the IC (directly across the V_{IN} and PGND pins) and the connections to these two pins must be direct to minimize the loop area. In general, placing all of the input capacitances near the IC is not possible. A good layout practice includes placing the bulk capacitor as close as possible to the V_{IN} pin.
- C_{VCC} and C_{BST}: The V_{CC} and bootstrap (BST) bypass capacitors supply switching currents to the high- and low-side gate drivers. These two capacitors must also be placed as close to the IC as possible and the connecting trace length and loop area must be minimized.
- The feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of both LM5160 and the LM5160A devices. Therefore, be careful when routing the feedback trace to avoid coupling any noise into this pin. In particular, the feedback trace must be short and not run close to magnetic components, or parallel to any other switching trace.
- SW trace: The SW node switches rapidly between V_{IN} and GND every cycle, which makes it a source of noise. The SW node area must be minimized. In particular, the SW node must not be inadvertently connected to a copper plane or pour.

5.16.3 Layout Guidelines for DC-DC Converter LM5017

A proper layout is essential for optimum performance of the circuit. Observe the following guidelines in particular:

- C_{IN}: The loop consisting of the input capacitor (C_{IN}), V_{IN} pin, and RTN pin carries switching currents. Therefore, the input capacitor must be placed close to the IC (directly across the V_{IN} and RTN pins) and the connections to these two pins must be direct to minimize the loop area. In general, accommodating all of the input capacitance near the IC is not possible. A good practice is to use a 0.1- or 0.47-µF capacitor directly across the V_{IN} and RTN pins close to the IC and the remaining bulk capacitor, as close as possible.
- C_{VCC} and C_{BST}: The V_{CC} and bootstrap (BST) bypass capacitors supply switching currents to the high- and low-side gate drivers. These two capacitors must also be placed as close to the IC as possible and the connecting trace length and loop area must be minimized.
- The feedback trace carries the output voltage information and a small ripple component that is necessary for proper operation of a LM5017 device. Therefore, be careful when routing the feedback trace to avoid coupling any noise to this pin. In particular, the feedback trace must not run close to magnetic components, or parallel to any other switching trace.

- SW trace: The SW node switches rapidly between V_{IN} and GND every cycle, which makes it a possible source of noise. The SW node area must be minimized

6 Getting Started Hardware

6.1 *Connecting ADC Board*

表 9. ADC Connections

PARAMETERS	DESCRIPTION	CONNECTORS
Voltage	Voltage input 1	J11
	Voltage input 2	J7
	Voltage input 3	J4
Current input	Current input 1	J9
	Current input 2	J6
	Current input 3	J2
	Current input 4	J3
	Current input 5	J1
Neutral (reference input)	Reference	J10
Interface connector	Connected to MCU	J5
Power supply (digital)	3.3 V	J5
Power supply (analog) to ADC	±2.5 V	–2.5-V jumper across J13 – 1:2 2.5-V jumper across J12 – 2:3
	0 to 3 V	0-V jumper across J13 – 3:2 3-V jumper across J12 – 2:1
	0 to 5 V	Remove U5 and populate R54 0-V jumper across J13 – 3:2 5-V jumper across J12 – 2:1
Analog power supply input to LDO	5 V	J5
	–5 V	J5

6.2 *Connecting MCU Board*

表 10. MCU Connections

PARAMETERS	DESCRIPTION	CONNECTORS
Earth fault input	Current input R	J10
	Current input Y	J12
	Current input B	J11
ADC interface	MCU board interface to ADC board	J14
Power input	Rectified current input for self-power	J8 – 3:2
	Auxiliary DC input	J8 – 2:1
JTAG	Programming	J3

7 Test Setup

7.1 Specifications of External CT Used for Testing

CT type: CT1231 medium accuracy, class 0.3, solid core

Turns ratio: 5:2500 (500)

Burden: Up to 30 Ω

7.2 Setup—ADC Board Interfaced to MMB0 DSP Board

The MMB0 is the motherboard used to evaluate the ADS131E08 EVM. A GUI has been developed to capture the waveforms and display the RMS values. The ADS131E08S ADC board has been designed to easily interface with the MMB0 board. The following 図 19 shows the setup. This setup can be used for evaluating the ADC performance. The power supply to the ADC board is applied externally.

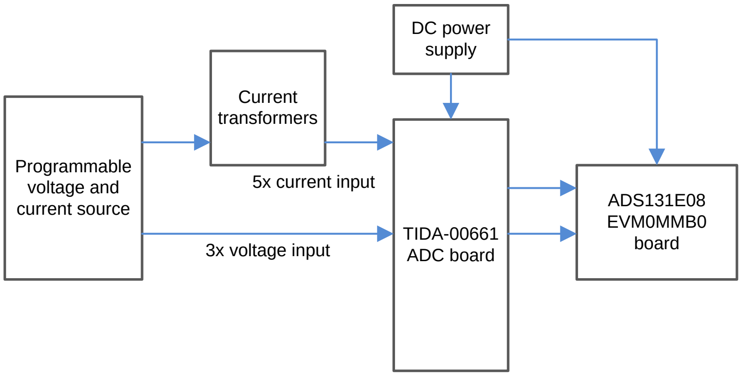


図 19. ADC Board Interfaced to MMB0 Board

7.3 ADC Board Interfaced to MCU (MSP430) Board

This TIDA-00661 TI Design has two boards: An ADC board and MCU board. The MCU board is connected to the ADC board using an interface connector. The MCU board is based on the fast start-up MSP430 MCU and DC-DC converters. This board is required to test the fast start-up performance of the ADC, as 図 20 shows.

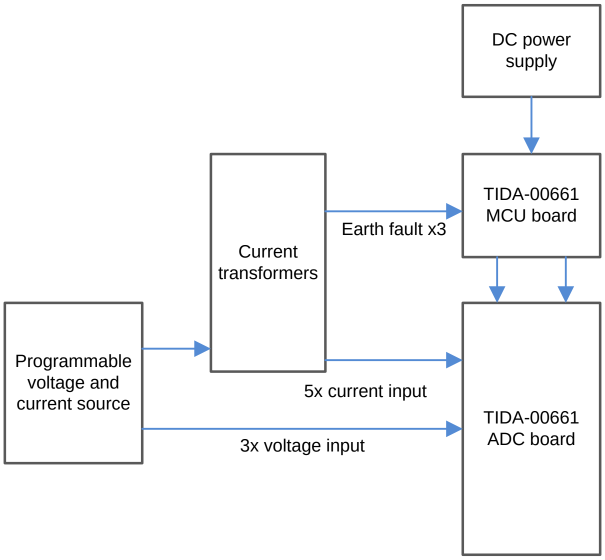


図 20. ADC Board Interfaced to MSP430 MCU-Based Interface Board

7.4 Setup Image

The setup in 図 21 shows the ADC board interfaced to the MMB0 EVM. The current input to the ADC board is applied using an external transformer. The voltage input is directly applied to the ADC board.

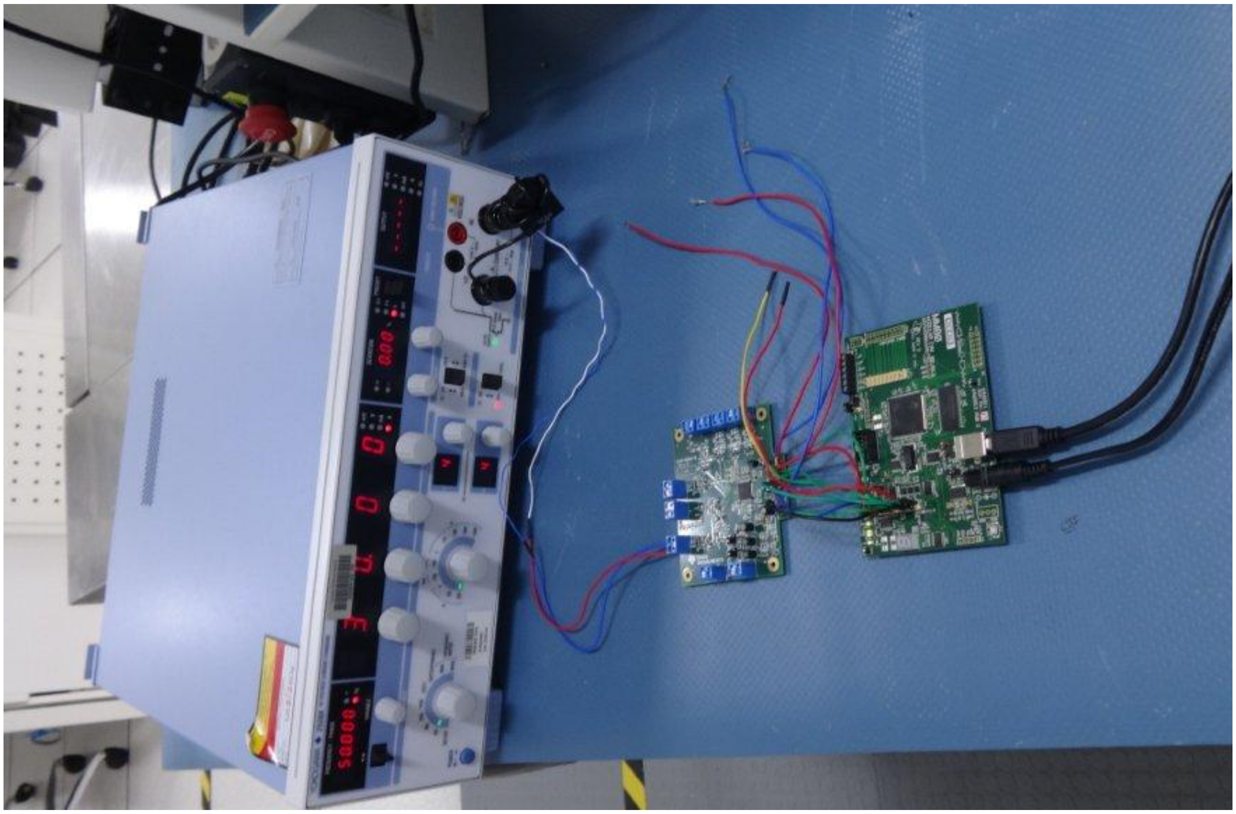


図 21. Setup With Current Source and ADC Board

The AC Voltage Current Standard 2558A has been used for the performance testing. This is a high accuracy source and the specifications are as follows: AC voltage: ±0.04% and AC current: ±0.05%.

7.5 GUI

The ADS131E08 EVM based GUI has been used to conduct the performance evaluation of the ADC board.

Download the GUI and guide from the following links: SBAU200 and ADS131E08EVM-PDK Version 1.0.0 Installation.

8 Test Data

8.1 Functional Testing

This section provides measurements for some of the basic tests such as the power supply, reference voltage output, and differential voltage output. These tests must be performed before conducting the performance tests. Refer to 5 for details on the different voltage rails generated.

8.1.1 DC-DC Converter

表 11. LM5017 Output Test Results

TEST	DESCRIPTION	OBSERVATION
Voltage output	12 V	12.99 V
	5 V	5.54 V
	–5 V	–5.5 V
	V_{PRI}	11.28 V
UVLO – Operate	> 15 V	15.25 V
UVLO – Shutdown	< 12.5 V	12.2 V

表 12. LM5160 Output Test Results

TEST	DESCRIPTION	OBSERVATION
Voltage output	12 V	12.3 V
	5 V	5.38 V
	–5 V	–5.31 V
	V_{PRI}	7.65 V
UVLO – Operate	> 15 V	15 V
UVLO – Shutdown	< 12.5 V	11.6 V

8.1.2 LDO Output

表 13. LDO Output Test Results

TEST	DESCRIPTION	OBSERVATION
MCU board	3.3 V	3.301 V
	5 V	5.027 V
ADC board	2.5 V	2.57 V
	–2.5 V	–2.466 V
	3.0 V	2.987 V

8.1.3 MCU

表 14. MCU Test Results

TEST	DESCRIPTION	OBSERVATION
MCU interface	Programming	Ok
	Current input measurement	Ok
	Op amp output	Ok
	Reference	1.651 V
	Undervoltage for DC-DC	Ok

8.1.4 ADC Board

表 15. ADC Test Results

TEST	DESCRIPTION	OBSERVATION
ADC board	Current input	Ok
	Voltage input	Ok
	Reference 2.4 V	2.4 V
	Reference 4 V	4.0 V
	Temperature sensor at room temperature 2.258 V	2.248 V

8.2 *Performance Testing*

The focus of the TIDA-00661 TI Design is to test the performance of the following devices:

ADS131E08S

The ADC performance was tested by applying voltage and current over a wide range and capturing waveforms for one cycle, three cycles, and then five cycles. The ADC sampling rate was fixed at 4000 samples and the number of samples captured was set to 80, 240, or 400 samples. The accuracy testing was performed with a 2.4-V reference and a 4-V reference.

MSP430F5969

The ADC samples for the earth fault current input was averaged for three cycles.

The following 表 16 shows a summary of all the performance tests conducted for the TIDA-00661 MCU and ADC boards.

表 16. Summary of Performance Tests Conducted

SERIAL NUMBER	TESTS	DETAILS
1	AC voltage measurement with fixed gain	AC voltage measurement up to 750 V, 2.4-V reference
		AC voltage measurement up to 900 V, 4-V reference
2	AC current measurement with fixed gain and differential input	AC current measurement 50 mA to 25 A, 2.4-V reference
		AC current measurement 25 mA to 40 A, 4-V reference
3	AC current measurement with gains changed	AC current measurement 20 mA to 50 A, 4-V reference
4	PGA testing	Check performance of all the programmable gains
5	AC current measurement with fixed gain and single-ended input	AC current measurement 50 mA to 25 A, 2.4-V reference
6	Other tests	60-Hz voltage input testing
		60-Hz current differential input testing
		Half cycle testing
		Testing with different sampling frequency
7	Earth fault current measurement with internal ADC	Measurement of three current inputs
8	$\Delta\Sigma$ start-up after applying auxiliary DC input	< 4 ms

8.2.1 Measurement Error

The measurement error consists of the following errors:

- Source error (current or voltage source)
- Potential divider ratio error

- External CT turns ratio error and burden resistor tolerance
- ADC PGA gain error
- ADC error

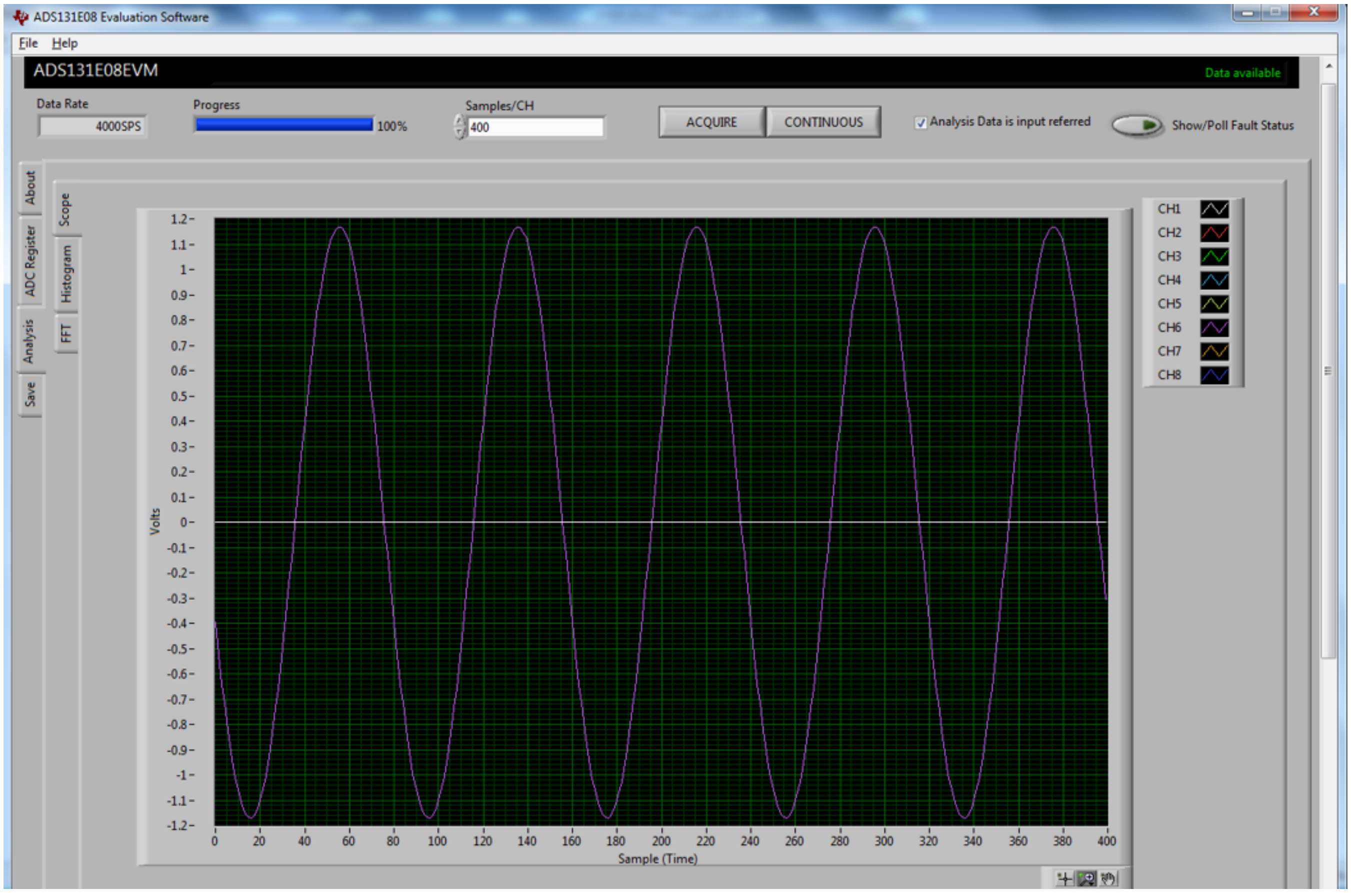
8.2.2 Offset and Gain Compensation

The measured ADC output RMS value in mV was compensated for the following:

Offset—A fixed voltage is subtracted from the measured value.

Gain compensation—A multiplication factor is applied to the measured RMS value. This compensates for the variation in the transformer turns ratio, burden ratio, or the potential divider ratio and the internal PGA gain errors.

8.2.3 Waveforms of ADC Samples



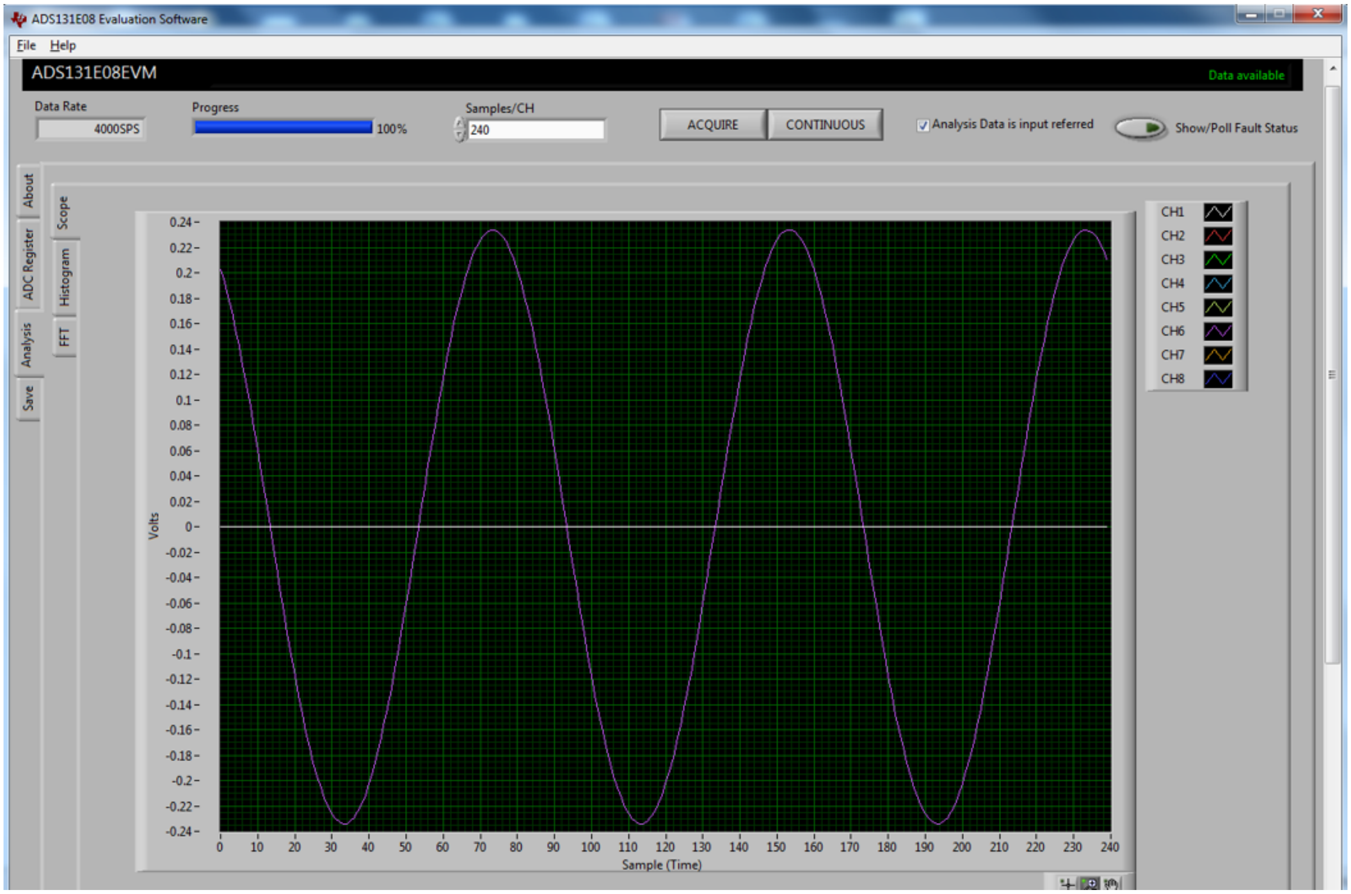
Data Rate: 4000SPS

Progress: 100%

Samples/CH: 400

☑ Analysis Data is input referred

図 22. Waveform With 400 Samples



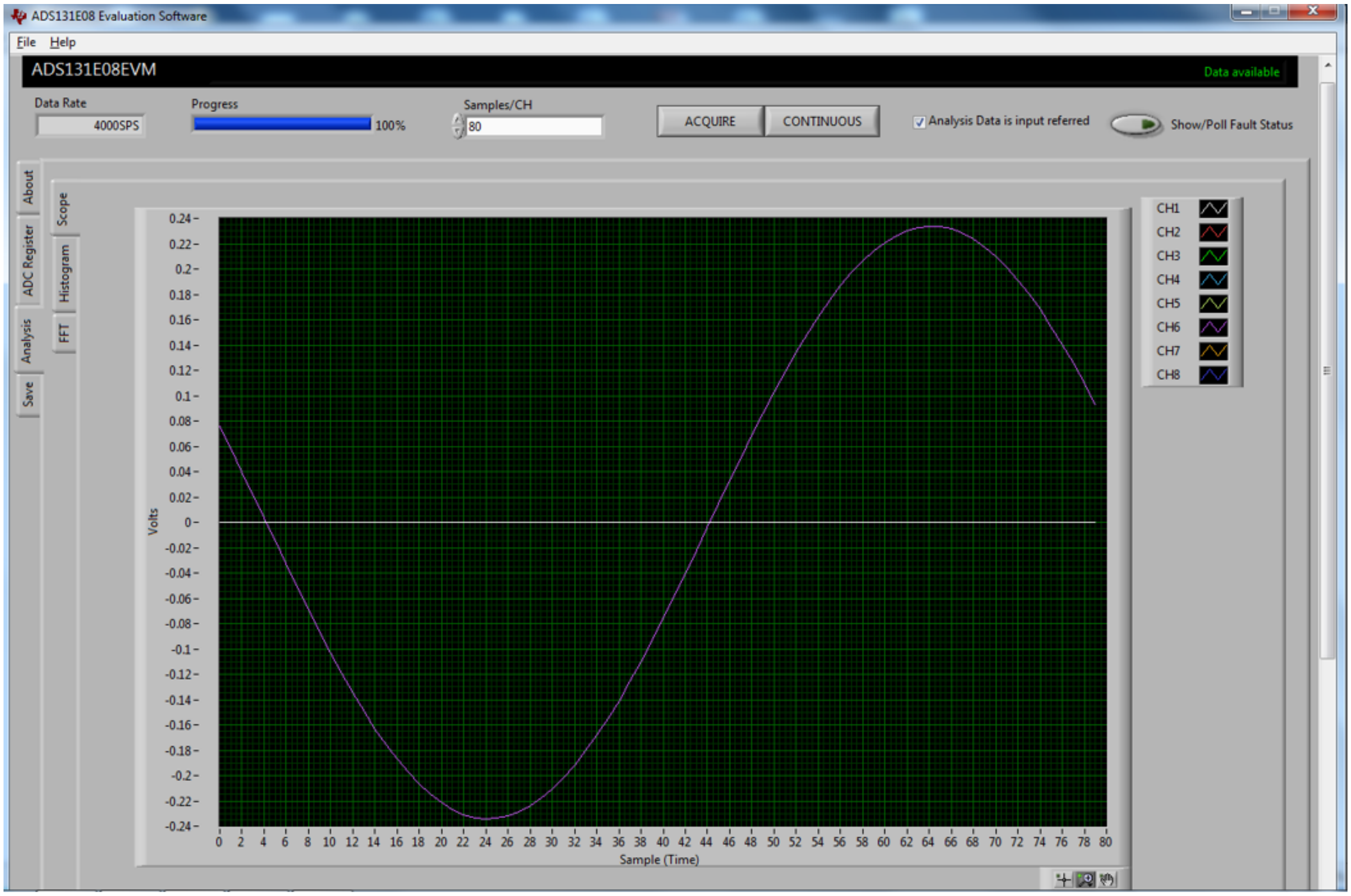
Data Rate: 4000SPS

Progress: 100%

Samples/CH: 240

☑ Analysis Data is input referred

図 23. Waveform With 240 Samples



ADS131E08 Evaluation Software

ADS131E08EVM

Data available

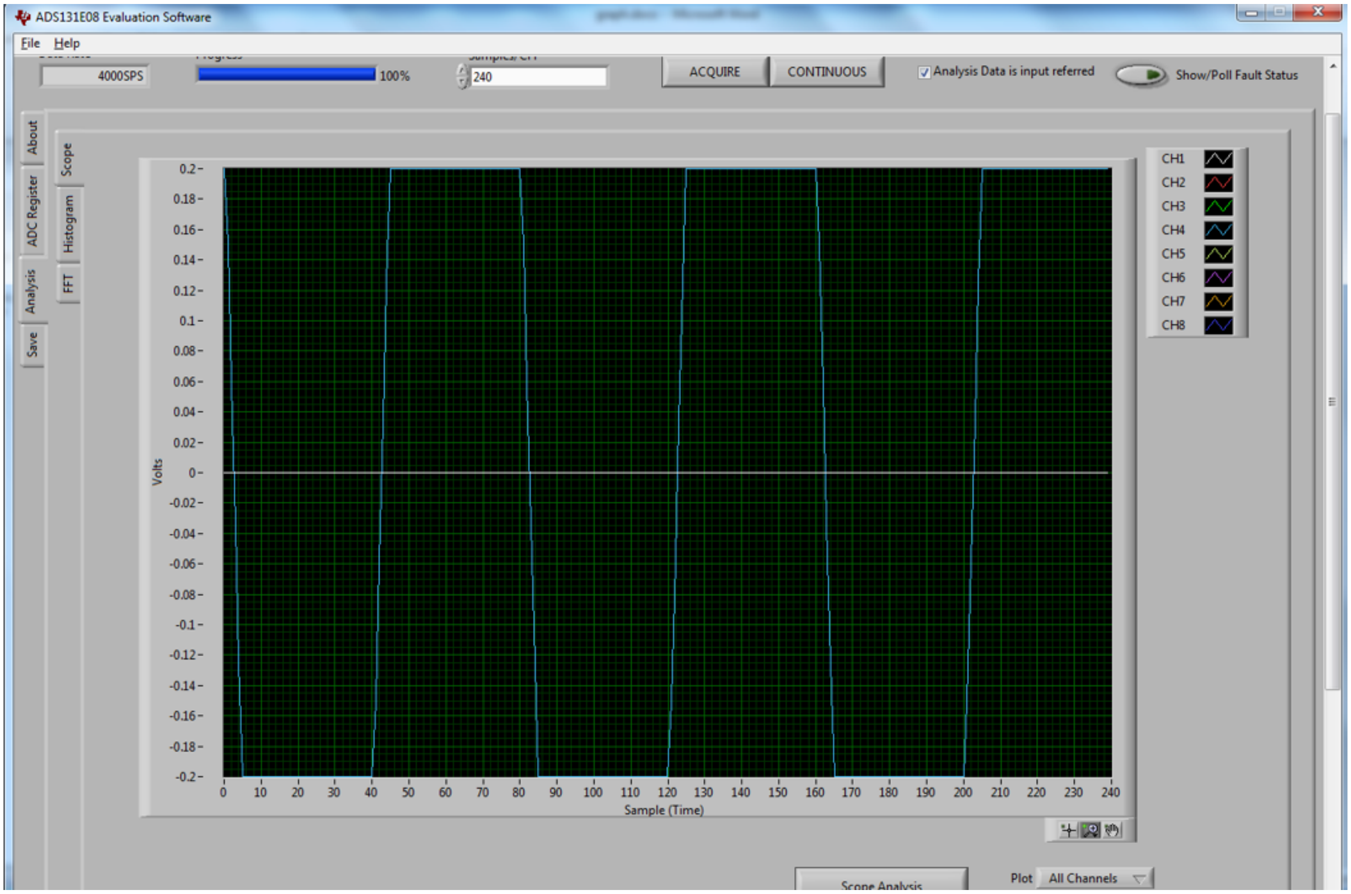
Data Rate: 4000SPS

Progress: 100%

Samples/CH: 80

☑ Analysis Data is input referred

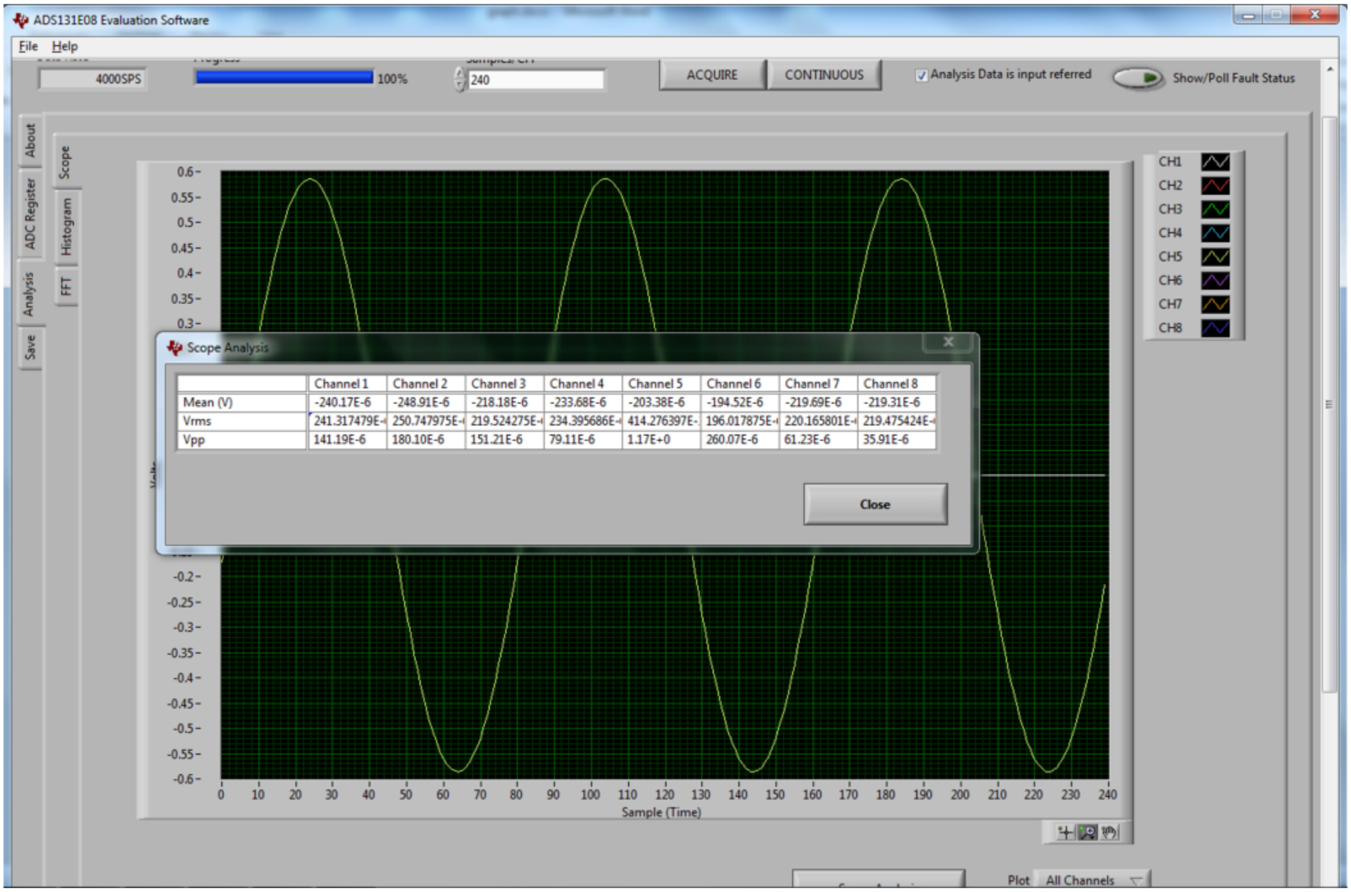
図 24. Waveform With 80 Samples



☑ Analysis Data is input referred

Plot All Channels

図 25. Waveform With Saturated Input



4000SPS

100%

240

☑ Analysis Data is input referred

	Channel 1	Channel 2	Channel 3	Channel 4	Channel 5	Channel 6	Channel 7	Channel 8
Mean (V)	-240.17E-6	-248.91E-6	-218.18E-6	-233.68E-6	-203.38E-6	-194.52E-6	-219.69E-6	-219.31E-6
Vrms	241.317479E-	250.747975E-	219.524275E-	234.395686E-	414.276397E-	196.017875E-	220.165801E-	219.475424E-
Vpp	141.19E-6	180.10E-6	151.21E-6	79.11E-6	1.17E+0	260.07E-6	61.23E-6	35.91E-6

図 26. RMS Readings for Captured Signal

8.2.4 Self-Test

The device features fault detection and a device testing capability.

The ADS131E0x series of devices have a flexible input multiplexer per channel, which can be independently connected to the internally-generated signals for test, temperature, and fault detection. Fault detection can be implemented internal to the device using the integrated comparators with digital-to-analog converter (DAC) controlled trigger levels.

Self-test signal

Signal frequency f_{CLK} / 221 or f_{CLK} / 220

Signal voltage ±1 mV or ±2 mV

Test signals (TestP and TestN)

Setting CHnSET[2:0] = 101 provides internally-generated test signals for use in subsystem verification at power up. Test signals are controlled through register settings (see the *CONFIG2: Configuration Register 2* subsection in the *Register Map* section of the SBAS705 datasheet for details). TEST_AMP controls the signal amplitude and TEST_FREQ controls switching at the required frequency. The test signals are multiplexed and transmitted out of the device at the TESTP and TESTN pins. A bit register (CONFIG2.INT_TEST = 0) deactivates the internal test signals so that the test signal can be driven externally. This feature allows the calibration of multiple devices with the same signal.

8.2.5 Accuracy—AC Voltage Input With Fixed PGA Gain

表 17. Steps to Perform AC Voltage Input Testing

STEPS	DESCRIPTION
Voltage input for 2.4-V reference	Voltage input of 10- to 750-V AC was applied across the potential divider and the PGA is programmed for X2 gain
Voltage input for 4-V reference	Voltage input of 10- to 900-V AC was applied across the potential divider
Capturing of samples	The waveform was captured using ADS131 performance evaluation GUI; graphical and RMS value was observed
Applying voltage input	AC voltage input was varied in steps as the following tables show at a 50-Hz input; voltage input is connected in single-ended mode

2.4-V reference

表 18. ADC Channel 1

VOLTAGE MEASUREMENT 50 Hz – THREE CYCLE, 4000 SAMPLE RATE, 240 s, AND X2 GAIN			
AC VOLTAGE (V)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC1_3C**
750	778.9061	780.7500	–0.2362
600	622.8906	624.6000	–0.2737
500	518.9664	520.5000	–0.2946
400	415.0884	416.4000	–0.3150
300	311.2542	312.3000	–0.3349
200	207.4703	208.2000	–0.3505
100	103.7237	104.1000	–0.3615
50	51.8568	52.0500	–0.3712
25	25.9286	26.0250	–0.3704
10	10.3757	10.4100	–0.3295
5	5.1919	5.2050	–0.2517
VOLTAGE MEASUREMENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, AND X2 GAIN			
AC VOLTAGE (V)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC1_1C**
750	780.4328	780.7500	–0.0406
600	624.1315	624.6000	–0.0750
500	519.9879	520.5000	–0.0984
400	415.8957	416.4000	–0.1211
300	311.8646	312.3000	–0.1394
200	207.8696	208.2000	–0.1587
100	103.9195	104.1000	–0.1734
50	51.9602	52.0500	–0.1725
25	25.9817	26.0250	–0.1665
10	10.3891	10.4100	–0.2004

表 19. ADC Channel 3

VOLTAGE MEASUREMENT 50 Hz – THREE CYCLE, 4000 SAMPLE RATE, 240 s, AND X2 GAIN			
AC VOLTAGE (V)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC3_3C**
600	621.2347	624.6000	–0.5388
500	517.5788	520.5000	–0.5612
400	413.9716	416.4000	–0.5832
300	310.4120	312.3000	–0.6045
200	206.9106	208.2000	–0.6193
100	103.4372	104.1000	–0.6367

表 19. ADC Channel 3 (continued)

VOLTAGE MEASUREMENT 50 Hz – THREE CYCLE, 4000 SAMPLE RATE, 240 s, AND X2 GAIN			
AC VOLTAGE (V)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR_ADC3_3C
50	51.7137	52.0500	–0.6461
25	25.8588	26.0250	–0.6386
10	10.3465	10.4100	–0.6100
5	5.1772	5.2050	–0.5341
VOLTAGE MEASUREMENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, AND X2 GAIN			
AC VOLTAGE (V)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR_ADC3_1C
750	780.3267	780.7500	–0.0542
600	624.0123	624.6000	–0.0941
500	519.8477	520.5000	–0.1253
400	415.7921	416.4000	–0.1460
300	311.7920	312.3000	–0.1627
200	207.8401	208.2000	–0.1729
100	103.9023	104.1000	–0.1899
50	51.9515	52.0500	–0.1892
25	25.9700	26.0250	–0.2112
10	10.3913	10.4100	–0.1801

表 20. ADC Channel 5

VOLTAGE MEASUREMENT 50 Hz – THREE CYCLE, 4000 SAMPLE RATE, 240 s, AND X2 GAIN			
AC VOLTAGE (V)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR_ADC5_3C
750	777.3577	780.7500	–0.4345
600	621.6874	624.6000	–0.4663
500	517.9534	520.5000	–0.4893
400	414.2763	416.4000	–0.5100
300	310.6510	312.3000	–0.5280
200	207.0650	208.2000	–0.5451
100	103.5247	104.1000	–0.5526
50	51.7574	52.0500	–0.5622
25	25.8801	26.0250	–0.5568
10	10.3528	10.4100	–0.5495
5	5.1803	5.2050	–0.4745
VOLTAGE MEASUREMENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, AND X2 GAIN			
AC VOLTAGE (V)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR_ADC5_1C
750	780.4346	780.7500	–0.0404
600	624.1383	624.6000	–0.0739
500	519.9426	520.5000	–0.1071
400	415.8571	416.4000	–0.1304
300	311.9428	312.3000	–0.1144
200	207.8690	208.2000	–0.1590
100	103.9202	104.1000	–0.1727
50	51.9610	52.0500	–0.1710
25	25.9777	26.0250	–0.1818
10	10.3924	10.4100	–0.1690

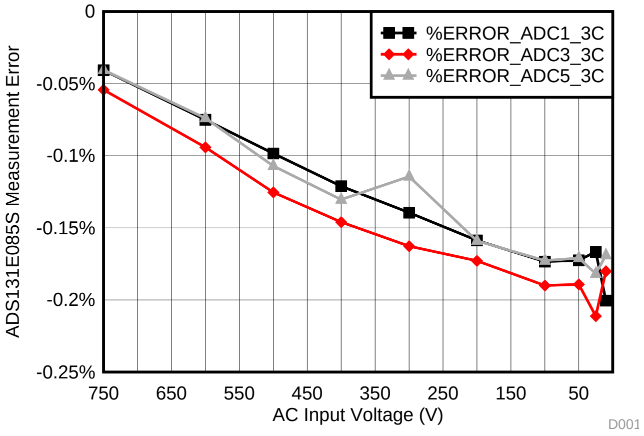


図 27. Input Voltage Vs ADC Measurement Error (2.4-V Reference)

4-V reference

表 21. ADC Channel 1

VOLTAGE MEASUREMENT – ONE CYCLE, 4000 SAMPLE RATE, 80 s, AND X2 GAIN			
AC VOLTAGE (V)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR_ADC1_1C
900	935.7256	936.9000	–0.1253
750	779.4809	780.7500	–0.1625
600	623.4028	624.6000	–0.1917
500	519.4050	520.5000	–0.2104
400	415.4429	416.4000	–0.2299
300	311.5141	312.3000	–0.2516
200	207.6304	208.2000	–0.2736
100	103.7871	104.1000	–0.3006
50	51.8856	52.0500	–0.3159
25	25.9383	26.0250	–0.3331
10	10.3741	10.4100	–0.3449

表 22. ADC Channel 3

VOLTAGE MEASUREMENT – ONE CYCLE, 4000 SAMPLE RATE, 80 s, AND X2 GAIN			
AC VOLTAGE (V)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR_ADC3_1C
900	935.5423	936.9000	–0.1449
750	779.7524	780.7500	–0.1278
600	623.5682	624.6000	–0.1652
500	519.5654	520.5000	–0.1796
400	415.5591	416.4000	–0.2019
300	311.5877	312.3000	–0.2281
200	207.6782	208.2000	–0.2506
100	103.8293	104.1000	–0.2601
50	51.9012	52.0500	–0.2858
25	25.9472	26.0250	–0.2989
10	10.3750	10.4100	–0.3359

表 23. ADC Channel 5

VOLTAGE MEASUREMENT – ONE CYCLE, 4000 SAMPLE RATE, 80 s, AND X2 GAIN			
AC VOLTAGE (V)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR_ADC5_1C
900	935.2636	936.9000	–0.1747
750	779.6781	780.7500	–0.1373
600	623.3951	624.6000	–0.1929
500	519.3811	520.5000	–0.2150
400	415.4117	416.4000	–0.2374
300	311.5044	312.3000	–0.2548
200	207.6274	208.2000	–0.2750
100	103.7976	104.1000	–0.2905
50	51.8958	52.0500	–0.2963
25	25.9493	26.0250	–0.2909
10	10.3815	10.4100	–0.2736

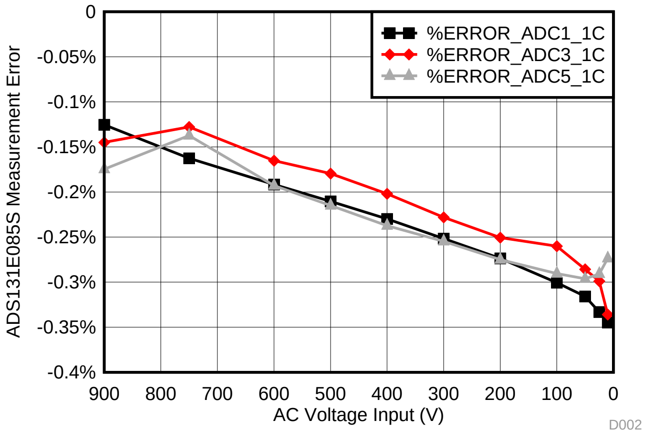


図 28. Input Voltage Vs ADC Measurement Error (4-V Reference)

8.2.6 AC Current—Differential AC Current Input With Fixed PGA Gain

The PGA gain is static for a given nominal current. The following measurements are results for one fixed gain to indicate the dynamic range.

表 24. Steps to Perform AC Current (Differential Input With Fixed Gain) Testing

STEPS	DESCRIPTION
Current input for 2.4-V reference	Current input from 25 mA to 25 A is applied through an external CT and the PGA is programmed for X2 gain
Current input for 4-V reference	Current input from 25 mA to 40 A is applied through an external CT and the PGA is programmed for X2 gain
Capturing of samples	The waveform was captured using ADS131 performance evaluation GUI; graphical and RMS value were observed
Applying current input	AC Current input was varied in steps as the following tables show at a 50-Hz input; the current inputs were connected differentially

2.4-V reference

表 25. ADC Channel 6

AC CURRENT 50 Hz – FIVE CYCLES, 4000 SAMPLE RATE, 400 s, X2 GAIN, AND V_{REF} 2.4 V			
AC CURRENT (A)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR_ADC6_5C
25	827.0934	825.0000	0.2537
20	661.7559	660.0000	0.2660
10	330.9001	330.0000	0.2728
5	165.4386	165.0000	0.2658
2.5	82.7090	82.5000	0.2533
1.25	41.3468	41.2500	0.2347
0.625	20.6666	20.6250	0.2017
0.3125	10.3216	10.3125	0.0882
0.1562	5.1526	5.1546	–0.0388
0.075	2.4677	2.4750	–0.2949
0.05	1.6437	1.6500	–0.3818
0.04	1.3173	1.3200	–0.2045
0.03125	1.0306	1.0313	–0.0630
0.025	0.8291	0.8250	0.4970
0.02	0.6686	0.6600	1.3030

AC CURRENT 50 Hz – THREE CYCLES, 4000 SAMPLE RATE, 240 s, X2 GAIN, AND V_{REF} 2.4 V			
AC CURRENT (A)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR_ADC6_3C
25	825.4424	825.0000	0.0536
20	660.4224	660.0000	0.0640
10	330.2413	330.0000	0.0731
5	165.1043	165.0000	0.0632
2.5	82.5451	82.5000	0.0546
1.25	41.2629	41.2500	0.0313
0.625	20.6210	20.6250	–0.0195
0.3125	10.3020	10.3125	–0.1023
0.1562	5.1394	5.1546	–0.2949
0.075	2.4596	2.4750	–0.6234
0.05	1.6408	1.6500	–0.5569
0.04	1.3135	1.3200	–0.4949
0.03125	1.0250	1.0313	–0.6016
0.025	0.8258	0.8250	0.1024
0.02	0.6643	0.6600	0.6468

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, X2 GAIN, AND V_{REF} 2.4 V			
AC CURRENT (A)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR_ADC6_1C
25	825.8277	825.0000	0.1003
20	660.7348	660.0000	0.1113
10	330.3831	330.0000	0.1161
5	165.1829	165.0000	0.1108
2.5	82.5773	82.5000	0.0938

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, X2 GAIN, AND V_{REF} 2.4 V			
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC6_1C**
1.25	41.2793	41.2500	0.0710
0.625	20.6327	20.6250	0.0374
0.3125	10.3043	10.3125	–0.0793
0.1562	5.1409	5.1546	–0.2662
0.075	2.4666	2.4750	–0.3396
0.05	1.6419	1.6500	–0.4889
0.04	1.3161	1.3200	–0.2937

表 26. ADC Channel 7

AC CURRENT 50 Hz – FIVE CYCLES, 4000 SAMPLE RATE, 400 s, X2 GAIN, AND V_{REF} 2.4 V			
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC7_5C**
25	825.9607	825.0000	0.1164
20	660.7886	660.0000	0.1195
10	330.4166	330.0000	0.1262
5	165.1889	165.0000	0.1145
2.5	82.5807	82.5000	0.0978
1.25	41.2783	41.2500	0.0686
0.625	20.6272	20.6250	0.0107
0.3125	10.3008	10.3125	–0.1135
0.1562	5.1382	5.1546	–0.3182
0.075	2.4585	2.4750	–0.6667
0.05	1.6381	1.6500	–0.7212
0.04	1.3109	1.3200	–0.6894
0.03125	1.0251	1.0313	–0.5964
0.025	0.8234	0.8250	–0.1939
0.02	0.6682	0.6600	1.2424

AC CURRENT 50 Hz – THREE CYCLES, 4000 SAMPLE RATE, 240 s, X2 GAIN, AND V_{REF} 2.4 V			
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC7_3C**
25	825.9183	825.0000	0.1113
20	660.7763	660.0000	0.1176
10	330.3951	330.0000	0.1197
5	165.1833	165.0000	0.1111
2.5	82.5770	82.5000	0.0933
1.25	41.2798	41.2500	0.0722
0.625	20.6279	20.6250	0.0141
0.3125	10.2981	10.3125	–0.1396
0.1562	5.1403	5.1546	–0.2774
0.075	2.4627	2.4750	–0.4970
0.05	1.6387	1.6500	–0.6848
0.04	1.3124	1.3200	–0.5758
0.03125	1.0265	1.0313	–0.4606
0.025	0.8301	0.8250	0.6182
0.02	0.6663	0.6600	0.9545

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, X2 GAIN, AND V_{REF} 2.4 V			
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC7_1C**
25	825.8938	825.0000	0.1083
20	660.7469	660.0000	0.1132
10	330.2828	330.0000	0.0857
5	165.1830	165.0000	0.1109
2.5	82.5817	82.5000	0.0990
1.25	41.2798	41.2500	0.0722
0.625	20.6289	20.6250	0.0189
0.3125	10.3039	10.3125	–0.0834
0.1562	5.1356	5.1546	–0.3686
0.075	2.4641	2.4750	–0.4404
0.05	1.6420	1.6500	–0.4848
0.04	1.3151	1.3200	–0.3712

表 27. ADC Channel 8

AC CURRENT 50 Hz – FIVE CYCLES, 4000 SAMPLE RATE, 400 s, X2 GAIN, AND V_{REF} 2.4 V			
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC8_5C**
25	828.9143	825.0000	0.4745
20	663.1689	660.0000	0.4801
10	331.6008	330.0000	0.4851
5	165.7827	165.0000	0.4744
2.5	82.8828	82.5000	0.4640
1.25	41.4255	41.2500	0.4255
0.625	20.6986	20.6250	0.3568
0.3125	10.3385	10.3125	0.2521
0.1562	5.1572	5.1546	0.0504
0.075	2.4670	2.4750	–0.3232
0.05	1.6422	1.6500	–0.4727
0.04	1.3151	1.3200	–0.3712
0.03125	1.0299	1.0313	–0.1309
0.025	0.8284	0.8250	0.4121
0.02	0.6701	0.6600	1.5303

AC CURRENT 50 Hz – THREE CYCLES, 4000 SAMPLE RATE, 240 s, X2 GAIN, AND V_{REF} 2.4 V			
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC8_3C**
25	826.3767	825.0000	0.1669
20	661.1225	660.0000	0.1701
10	330.3743	330.0000	0.1134
5	165.2769	165.0000	0.1678
2.5	82.6276	82.5000	0.1546
1.25	41.2951	41.2500	0.1094
0.625	20.6388	20.6250	0.0669
0.3125	10.3083	10.3125	–0.0409
0.1562	5.1412	5.1546	–0.2609

AC CURRENT 50 Hz – THREE CYCLES, 4000 SAMPLE RATE, 240 s, X2 GAIN, AND V_{REF} 2.4 V			
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC8_3C**
0.075	2.4622	2.4750	–0.5175
0.05	1.6387	1.6500	–0.6867
0.04	1.3124	1.3200	–0.5795
0.03125	1.0286	1.0313	–0.2565
0.025	0.8266	0.8250	0.1955
0.02	0.6691	0.6600	1.3768

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, X2 GAIN, AND V_{REF} 2.4 V			
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC8_1C**
25	825.6244	825.0000	0.0757
20	660.5819	660.0000	0.0882
10	330.3079	330.0000	0.0933
5	165.1463	165.0000	0.0886
2.5	82.5590	82.5000	0.0716
1.25	41.2725	41.2500	0.0547
0.625	20.6235	20.6250	–0.0074
0.3125	10.3020	10.3125	–0.1016
0.1562	5.1408	5.1546	–0.2686
0.075	2.4621	2.4750	–0.5207
0.05	1.6425	1.6500	–0.4543
0.04	1.3147	1.3200	–0.4000

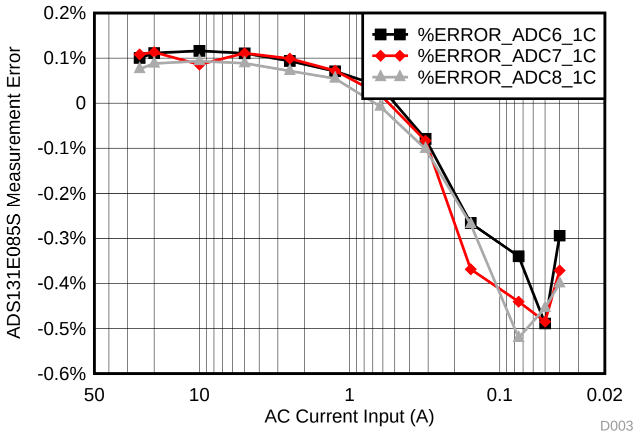


図 29. Input Current Vs ADC Measurement Error

4-V reference

表 28. ADC Channel 6

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, X2 GAIN, AND V_{REF} 4 V			
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC6_1C**
40	1320.9249	1320.0000	0.0701
25	825.9421	825.0000	0.1131
20	660.9926	660.0000	0.1504
10	330.4443	330.0000	0.1346
5	165.2299	165.0000	0.1393
2.5	82.5946	82.5000	0.1146
1.25	41.2938	41.2500	0.1063
0.625	20.6402	20.6250	0.0739
0.3125	10.3139	10.3125	0.0139
0.1562	5.1489	5.1546	–0.1109
0.075	2.4700	2.4750	–0.2040
0.05	1.6460	1.6500	–0.2423
0.04	1.3187	1.3200	–0.1017

表 29. ADC Channel 7

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, X2 GAIN, AND V_{REF} 4 V			
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC7_1C**
40	1321.7270	1320.0000	0.1308
25	826.3902	825.0000	0.1668
20	661.1426	660.0000	0.1731
10	330.5572	330.0000	0.1688
5	165.2695	165.0000	0.1633
2.5	82.6288	82.5000	0.1561
1.25	41.3060	41.2500	0.1358
0.625	20.6432	20.6250	0.0882
0.3125	10.3120	10.3125	–0.0048
0.1562	5.1482	5.1546	–0.1242
0.075	2.4674	2.4750	–0.3071
0.05	1.6453	1.6500	–0.2848
0.04	1.3185	1.3200	–0.1136

表 30. ADC Channel 8

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, X2 GAIN, AND V_{REF} 4 V			
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC8_1C**
40	1318.9480	1320.0000	–0.0797
25	826.0825	825.0000	0.1299
20	660.9103	660.0000	0.1379
10	330.4045	330.0000	0.1226
5	165.2029	165.0000	0.1230
2.5	82.5944	82.5000	0.1144
1.25	41.2898	41.2500	0.0964
0.625	20.6388	20.6250	0.0670
0.3125	10.3112	10.3125	–0.0127

表 **30. ADC Channel 8 (continued)**

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, X2 GAIN, AND V_{REF} 4 V			
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC8_1C**
0.1562	5.1473	5.1546	–0.1411
0.075	2.4692	2.4750	–0.2350
0.05	1.6466	1.6500	–0.2068
0.04	1.3198	1.3200	–0.0152

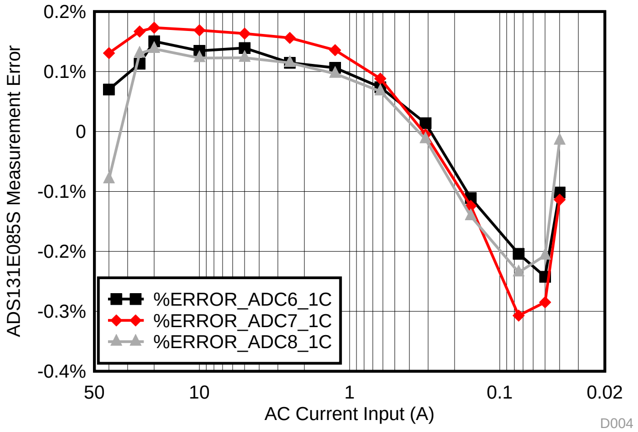


図 **30. Input Current Vs ADC Measurement Error (4-V Reference)**

8.2.7 AC Current Input—Differential AC Current Input With PGA Gain Dynamically Switched

表 **31. Steps to Perform AC Current Testing**

STEPS	DESCRIPTION
Current input for 2.4-V reference	Current input from 10 mA to 50 A is applied through an external CT and the PGA is programmed for X1,X2, and X12 gain
Capturing of samples	The waveform was captured using an ADS131 performance evaluation GUI; graphical and RMS value were observed
Applying current input	AC current input was varied in steps as the following tables show at a 50-Hz input; the current inputs were connected differentially

The user can select the gain to improve accuracy based on the current rating of the breaker. The following measurements show how to improve accuracy over a wider range without changing hardware.

2.4-V reference

表 32. ADC Channel 6

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, AND V_{REF} 2.4 V				
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC6_1C**	**PROGRAMMED ADC GAIN**
50	1650.3000	1650.0000	0.0182	1
25	824.6502	825.0000	-0.0420	2
20	660.4151	660.0000	0.0623	
10	330.2178	330.0000	0.0653	
5	165.1146	165.0000	0.0688	
2.5	82.5514	82.5000	0.0616	
1.25	41.2727	41.2500	0.0546	
0.625	20.6351	20.6250	0.0486	
0.3125	10.3136	10.3125	0.0102	
0.1562	5.1593	5.1546	0.0921	12
0.075	2.4762	2.4750	0.0477	
0.05	1.6502	1.6500	0.0134	
0.04	1.3203	1.3200	0.0240	
0.03125	1.0314	1.0313	0.0098	
0.025	0.8244	0.8250	–0.0774	
0.02	0.6594	0.6600	–0.0895	

表 33. ADC Channel 7

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, AND V_{REF} 2.4 V				
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC7_1C**	**PROGRAMMED ADC GAIN**
50	1650.0290	1650.0000	0.0018	1
25	825.6694	825.0000	0.0803	2
20	660.6425	660.0000	0.0964	
10	330.3598	330.0000	0.1079	
5	165.1721	165.0000	0.1033	
2.5	82.5810	82.5000	0.0972	
1.25	41.2871	41.2500	0.0890	
0.625	20.6407	20.6250	0.0754	
0.3125	10.3182	10.3125	0.0547	
0.1562	5.1627	5.1546	0.1562	12
0.075	2.4750	2.4750	–0.0020	
0.05	1.6492	1.6500	–0.0515	
0.04	1.3191	1.3200	–0.0720	
0.03125	1.0313	1.0313	0.0010	
0.025	0.8254	0.8250	0.0424	
0.02	0.6591	0.6600	–0.1439	

表 34. ADC Channel 8

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, AND V_{REF} 2.4 V				
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC8_1C**	**PROGRAMMED ADC GAIN**
50	1649.6440	1650.0000	–0.0216	1
25	825.6287	825.0000	0.0754	2
20	660.5254	660.0000	0.0788	
10	330.2891	330.0000	0.0867	
5	165.1839	165.0000	0.1104	
2.5	82.5981	82.5000	0.1177	
1.25	41.2972	41.2500	0.1132	
0.625	20.6523	20.6250	0.1309	
0.3125	10.3268	10.3125	0.1376	
0.1562	5.1586	5.1546	0.0772	12
0.075	2.4762	2.4750	0.0486	
0.05	1.6502	1.6500	0.0124	
0.04	1.3201	1.3200	0.0048	
0.03125	1.0308	1.0313	–0.0456	
0.025	0.8250	0.8250	0.0003	
0.02	0.6594	0.6600	–0.0933	

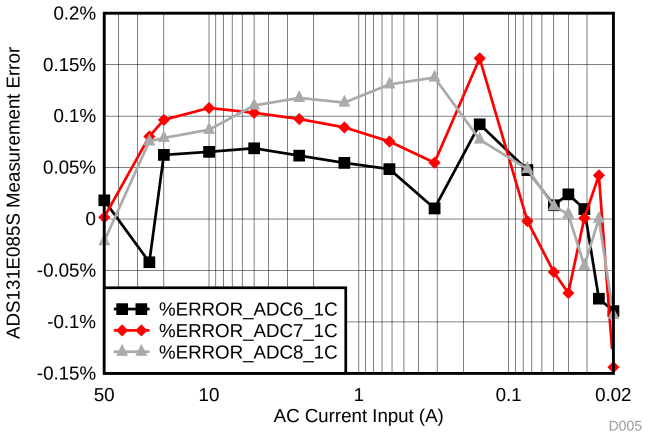


図 31. Input Current Vs ADC Measurement Error (2.4-V Reference)

8.2.8 PGA Testing With Voltage and Current Inputs

For the purposes of PGA testing, a known constant voltage or current input was applied. The input was chosen to ensure that it does not saturate for all of the PGA gains. The PGA gain was changed and subsequent readings were recorded.

Voltage inputs

表 35. ADC Channel 1

VOLTAGE MEASUREMENT WITH DIFFERENT GAINS – ONE CYCLE, 4000 SAMPLE RATE, 80 s, AND X2 GAIN				
AC VOLTAGE (V)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR	GAIN
50	51.8605	52.0500	–0.3641	1
50	51.8570	52.0500	–0.3708	2
50	51.8469	52.0500	–0.3902	4
50	51.8462	52.0500	–0.3915	8
50	51.8563	52.0500	–0.3721	12

表 36. ADC Channel 3

VOLTAGE MEASUREMENT WITH DIFFERENT GAINS – ONE CYCLE, 4000 SAMPLE RATE, 80 s, AND X2 GAIN				
AC VOLTAGE (V)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR	GAIN
50	51.7146	52.05	–0.6444	1
50	51.7142	52.05	–0.6451	2
50	51.7195	52.05	–0.6350	4
50	51.7152	52.05	–0.6432	8
50	51.7104	52.05	–0.6524	12

表 37. ADC Channel 5

VOLTAGE MEASUREMENT WITH DIFFERENT GAINS – ONE CYCLE, 4000 SAMPLE RATE, 80 s, AND X2 GAIN				
AC VOLTAGE (V)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR	GAIN
50	51.7561	52.05	–0.5646	1
50	51.7573	52.05	–0.5623	2
50	51.7524	52.05	–0.5718	4
50	51.7522	52.05	–0.5721	8
50	51.7518	52.05	–0.5729	12

Current inputs

表 38. ADC Channel 6

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, X2 GAIN, AND ADC1				
AC CURRENT (A)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR	GAIN
2	66.1490	66.0000	0.2258	1
2	66.1599	66.0000	0.2423	2
2	66.1586	66.0000	0.2403	4
2	66.1646	66.0000	0.2494	8
2	66.1566	66.0000	0.2373	12

表 39. ADC Channel 7

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, X2 GAIN, AND ADC3				
AC CURRENT (A)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR	GAIN
2	66.0530	66.0000	0.0803	1
2	66.0738	66.0000	0.1118	2
2	66.0604	66.0000	0.0915	4
2	66.0464	66.0000	0.0703	8
2	66.0349	66.0000	0.0529	12

表 40. ADC Channel 8

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, X2 GAIN, AND ADC2				
AC CURRENT (A)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR	GAIN
2	66.2802	66	0.4245	1
2	66.3015	66	0.4568	2
2	66.2995	66	0.4538	4
2	66.2816	66	0.4267	8
2	66.2743	66	0.4156	12

8.2.9 Accuracy—Single-Ended AC Current With Fixed PGA Gain

表 41. Steps to Perform AC Current Input Testing (Single-Ended)

STEPS	DESCRIPTION
Current input for 2.4-V reference	Current input from 31.25 mA to 25 A was applied through an external CT and the PGA is programmed for X2 gain
Capturing of samples	The waveform was captured using an ADS131 performance evaluation GUI; graphical and RMS value were observed
Applying current input	AC current input was varied in steps as the following tables show at a 50-Hz input; one end of the CT was grounded to make the measurement single-ended

表 42. ADC Channel 2

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, AND X2 GAIN			
AC CURRENT (A)	MEASURE VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR_ADC2_1C
25	826.5160	825.0000	0.1838
20	661.2090	660.0000	0.1832
10	330.6385	330.0000	0.1935
5	165.2950	165.0000	0.1788
2.5	82.6455	82.5000	0.1764
1.25	41.3091	41.2500	0.1433
0.625	20.6488	20.6250	0.1154
0.3125	10.3165	10.3125	0.0388
0.1562	5.1506	5.1546	–0.0776
0.075	2.4708	2.4750	–0.1697
0.05	1.6511	1.6500	0.0667
0.04	1.3265	1.3200	0.4924
0.03125	1.0456	1.0313	1.3915

表 43. ADC Channel 4

AC CURRENT 50 Hz – ONE CYCLE, 4000 SAMPLE RATE, 80 s, AND X2 GAIN			
AC CURRENT (A)	**MEASURE VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC4_1C**
25	829.2250	825.0000	0.5121
20	663.3563	660.0000	0.5085
10	331.7632	330.0000	0.5343
5	165.8558	165.0000	0.5187
2.5	82.9218	82.5000	0.5113
1.25	41.4437	41.2500	0.4696
0.625	20.7151	20.6250	0.4368
0.3125	10.3542	10.3125	0.4044
0.1562	5.1666	5.1546	0.2328
0.075	2.4812	2.4750	0.2505
0.05	1.6537	1.6500	0.2242
0.04	1.3255	1.3200	0.4167
0.03125	1.0422	1.0313	1.0618

8.3 Accuracy Testing—Other Tests

8.3.1 AC Voltage Input at 60 Hz

The following tables show the results of accuracy testing for an AC voltage input at 60 Hz.

表 44. ADC Channel 1

VOLTAGE MEASUREMENT 60 Hz – THREE CYCLES, 4000 SAMPLE RATE, 200 s, and X2 GAIN			
AC VOLTAGE (V)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC1_3C**
750	781.2195	780.7500	0.0601
600	624.7490	624.6000	0.0239
500	520.5188	520.5000	0.0036
400	416.3351	416.4000	–0.0156
300	312.1869	312.3000	–0.0362
200	208.0859	208.2000	–0.0548
100	104.0227	104.1000	–0.0742
50	52.0612	52.0500	0.0215
25	26.0059	26.0250	–0.0734
10	10.4043	10.4100	–0.0549
5	5.2073	5.2050	0.0435

表 45. ADC Channel 1

VOLTAGE MEASUREMENT 60 Hz – ONE CYCLE, 4000 SAMPLE RATE, 67 s, and X2 GAIN			
AC VOLTAGE (V)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC1_1C**
750	779.6944	780.7500	–0.1352
600	623.8677	624.6000	–0.1172
500	520.9813	520.5000	0.0925
400	417.2362	416.4000	0.2008
300	312.8125	312.3000	0.1641
200	208.4948	208.2000	0.1416
100	104.2957	104.1000	0.1880
50	52.1323	52.0500	0.1582

表 45. ADC Channel 1 (continued)

VOLTAGE MEASUREMENT 60 Hz – ONE CYCLE, 4000 SAMPLE RATE, 67 s, and X2 GAIN			
AC VOLTAGE (V)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC1_1C**
25	26.0723	26.0250	0.1819
10	10.4246	10.4100	0.1399
5	5.2078	5.2050	0.0531

表 46. ADC Channel 3

VOLTAGE MEASUREMENT 60 Hz – THREE CYCLES, 4000 SAMPLE RATE, 200 s, and X2 GAIN			
AC VOLTAGE (V)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC3_1C**
750	781.1242	780.7500	0.0479
600	624.6559	624.6000	0.0089
500	520.4435	520.5000	–0.0108
400	416.2570	416.4000	–0.0343
300	312.1348	312.3000	–0.0529
200	208.0419	208.2000	–0.0759
100	104.0048	104.1000	–0.0914
50	51.9946	52.0500	–0.1064
25	26.0036	26.0250	–0.0823
10	10.4064	10.4100	–0.0349
5	5.1989	5.2050	–0.1171

表 47. ADC Channel 3

VOLTAGE MEASUREMENT 60 Hz – ONE CYCLE, 4000 SAMPLE RATE, 67 s, and X2 GAIN			
AC VOLTAGE (V)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC3_3C**
750	781.6149	780.7500	0.1108
600	624.6617	624.6000	0.0099
500	520.7668	520.5000	0.0513
400	416.4267	416.4000	0.0064
300	312.1287	312.3000	–0.0548
200	208.0842	208.2000	–0.0556
100	104.1166	104.1000	0.0160
50	52.0500	52.0500	0.0000
25	26.0122	26.0250	–0.0490
10	10.4200	10.4100	0.0963
5	5.2132	5.2050	0.1583

8.3.2 AC Current Input at 60 Hz

The following tables show the results of accuracy testing for an AC current input at 60 Hz.

表 48. ADC Channel 6

AC CURRENT 60 Hz – THREE CYCLES, 4000 SAMPLE RATE, 200 s, X2 GAIN, and V_{REF} 2.4 V			
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC6_3C**
25	825.9576	825.0000	0.1161
20	660.8369	660.0000	0.1268
10	330.4318	330.0000	0.1309
5	165.2172	165.0000	0.1316
2.5	82.6044	82.5000	0.1265
1.25	41.2950	41.2500	0.1092
0.625	20.6420	20.6250	0.0826
0.3125	10.3135	10.3125	0.0100
0.1562	5.1495	5.1546	–0.0993
0.075	2.4700	2.4750	–0.2040
0.05	1.6470	1.6500	–0.1819
0.04	1.3185	1.3200	–0.1168

AC CURRENT 60 Hz – ONE CYCLE, 4000 SAMPLE RATE, 67 s, X2 GAIN, and V_{REF} 2.4 V			
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC6_1C**
25	826.3991	825.0000	0.1696
20	661.7691	660.0000	0.2680
10	330.8767	330.0000	0.2657
5	165.3152	165.0000	0.1910
2.5	82.6222	82.5000	0.1481
1.25	41.3491	41.2500	0.2402
0.625	20.6671	20.6250	0.2042
0.3125	10.2872	10.3125	–0.2449
0.1562	5.1383	5.1546	–0.3155
0.075	2.4674	2.4750	–0.3081
0.05	1.6427	1.6500	–0.4450
0.04	1.3156	1.3200	–0.3302

表 49. ADC Channel 7

AC CURRENT 60 Hz – THREE CYCLES, 4000 SAMPLE RATE, 200 s, X2 GAIN, and V_{REF} 2.4 V			
AC CURRENT (A)	**MEASURED VOLTAGE (mV)**	**ACTUAL VOLTAGE (mV)**	**%ERROR_ADC7_3C**
25	826.3796	825.0000	0.1672
20	661.1474	660.0000	0.1738
10	330.6020	330.0000	0.1824
5	165.2914	165.0000	0.1766
2.5	82.6430	82.5000	0.1733
1.25	41.3146	41.2500	0.1566
0.625	20.6499	20.6250	0.1207
0.3125	10.3167	10.3125	0.0407
0.1562	5.1517	5.1546	–0.0563
0.075	2.4720	2.4750	–0.1212

表 49. ADC Channel 7 (continued)

AC CURRENT 60 Hz – THREE CYCLES, 4000 SAMPLE RATE, 200 s, X2 GAIN, and V_{REF} 2.4 V			
AC CURRENT (A)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR_ADC7_3C
0.05	1.6494	1.6500	–0.0364
0.04	1.3193	1.3200	–0.0530

AC CURRENT 60 Hz – ONE CYCLE, 4000 SAMPLE RATE, 67 s, X2 GAIN, and V_{REF} 2.4 V			
AC CURRENT (A)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR_ADC7_1C
25	826.7761	825.0000	0.2153
20	661.2473	660.0000	0.1890
10	330.3451	330.0000	0.1046
5	165.3226	165.0000	0.1955
2.5	82.6554	82.5000	0.1884
1.25	41.3357	41.2500	0.2078
0.625	20.6549	20.6250	0.1450
0.3125	10.3056	10.3125	–0.0669
0.1562	5.1388	5.1546	–0.3065
0.075	2.4642	2.4750	–0.4364
0.05	1.6415	1.6500	–0.5152
0.04	1.3149	1.3200	–0.3864

8.3.3 Current Input Measurement Accuracy With Half-Cycle Equivalent Samples at 50 Hz

The following 表 50 shows the results of accuracy testing for an AC current input at 50 Hz with half-cycle samples.

表 50. Half-Cycle Accuracy—ADC Channel 6

AC CURRENT 50 Hz – FIVE CYCLES, 4000 SAMPLE RATE, 40 s, X2 GAIN, and V_{REF} 2.4 V			
AC CURRENT (A)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	%ERROR_ADC6
25	827.2887	825.0000	0.2774
20	661.9219	660.0000	0.2912
10	330.7521	330.0000	0.2279
5	165.5511	165.0000	0.3340
2.5	82.8906	82.5000	0.4735
1.25	41.4923	41.2500	0.5874
0.625	20.6487	20.6250	0.1149
0.3125	10.3610	10.3125	0.4703
0.25	8.3502	8.2500	1.2145
0.1562	5.2449	5.1546	1.7518

8.3.4 Current Input Measurement at 50 Hz With Different Sampling Rates

The following 表 51 shows the measurement results of ADC sampling rates in multiple sampling rate configurations.

表 51. Measurement at Different Sampling Rates ADC—Channel 6

AC CURRENT 50 Hz – ONE CYCLE, ADC1, AND X2 GAIN				
AC CURRENT (A)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	SAMPLES	SAMPLING kSPS
5	165.5821	165.0000	320.0000	16
5	165.5517	165.0000	160.0000	8
5	165.4929	165.0000	80.0000	4
5	165.1710	165.0000	40.0000	2
5	165.5594	165.0000	20.0000	1

注: The ADC sampling rates were changed from 1 kSPS to 16 kSPS. The EVM does not allow sampling above 16-K samples.

8.4 *Earth Fault Testing*

The earth fault currents can be measured with an internal 12-bit ADC because of the limited dynamic range.

表 52. Steps to Perform Earth Fault Testing

STEPS	DESCRIPTION
Current input	Current input up to 10 A can be measured with a fixed gain of X 5.7 and internal 12-bit ADC; the AC current input was level shifted by 1.65 V for measurement
Capturing of samples	The samples were captured by an MCU MSP430F5969
Applying current input	AC current input was varied in steps as the following tables show at a 50-Hz input

表 53. Board 1 Current Measurement

AC CURRENT (A)	OP AMP O/P 1 – TP12	OP AMP O/P 2 – TP14	OP AMP O/P 3 – TP15	ADC1 – A10	ADC2 – A12	ADC3 – A14	ADC1 %ERROR	ADC2 %ERROR	ADC3 %ERROR
1	126.9	127	126.5	126.48	127.02	126.683	–0.3310	0.0157	0.1447
2.5	316.6	316.7	315.5	315.82	316.626	315.014	–0.2464	–0.0234	–0.1540
5	633	633	630.5	631.64	632.446	629.333	–0.2148	–0.0875	–0.1851
7	886.1	886.55	882.5	884.61	885.424	881.665	–0.1682	–0.1270	–0.0946
9	1138.5	1140.1	1136	1137.32	1138.403	1133.569	–0.1036	–0.1488	–0.2140

表 54. Board 2 Current Measurement

AC CURRENT (A)	OP AMP O/P 1 – TP12	OP AMP O/P 2 – TP14	OP AMP O/P 3 – TP15	ADC1 – A10	ADC2 – A12	ADC3 – A14	ADC1 %ERROR	ADC2 %ERROR	ADC3 %ERROR
1	126.7	126.7	125.5	126.489	126.489	125.415	–0.1665	–0.1665	–0.0677
2.5	314.25	314.2	312.9	314.477	314.746	312.866	0.0722	0.1738	–0.0109
5	628.3	628.4	626.1	628.686	628.955	626.269	0.0614	0.0883	0.0270
7	879.3	880	877.2	880.859	881.127	877.636	0.1773	0.1281	0.0497
9	1132	1132	1127	1131.42	1132.227	1127.393	–0.0511	0.0201	0.0349

8.5 Testing With ADS131E08

The TIDA-00661 ADC board was used to test the accuracy performance of the ADS131E08. The measurements were taken for 5 cycles at 4 KSPS. Measurements were taken for 2.4-V and 4-V references for both voltage and current inputs.

8.5.1 Voltage Measurement Accuracy

表 55. ADC Channel 1 Voltage With 2.4-V V_{REF}

AC VOLTAGE (V)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	ADC1 _5C % ERROR
900	908.82640	936.900	–2.9964
750	781.24750	780.750	0.0637
600	624.73770	624.600	0.0220
500	520.47840	520.500	–0.0041
400	416.28860	416.400	–0.0267
300	312.15040	312.300	–0.0479
200	208.06570	208.200	–0.0645
100	104.01130	104.100	–0.0852
50	52.00674	52.050	–0.0831
25	26.00408	26.025	–0.0804
10	10.40691	10.410	–0.0297
5	5.20884	5.205	0.0738

注: Voltage measurement: 5 cycles, 4000 samples rate, 400 S, X2 gain, 2.4-V reference

注: Measurement saturates after 750 V.

表 56. ADC Channel 1 Voltage With 4-V V_{REF}

AC VOLTAGE (V)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	ADC1 _5C % ERROR
1000	1040.664000	1041.000	–0.0323
900	936.662100	936.900	–0.0254
750	781.087400	780.750	0.04320
600	624.679300	624.600	0.0127
500	520.450000	520.500	–0.0096
400	416.258600	416.400	–0.0340
300	312.119700	312.300	–0.0577
200	208.046500	208.200	–0.0737
100	103.999300	104.100	–0.0968
50	51.999280	52.050	–0.0974
25	26.000690	26.025	–0.0934
10	10.403860	10.410	–0.0590
5	5.205461	5.205	0.0089

注: Voltage measurement: 5 cycles, 4000 samples rate, 400 S, X2 gain, 4-V reference

8.5.2 Current Measurement Accuracy With 0.1 Class CT

表 57. ADC Channel 2 Current With 2.4-V V_{REF}

AC CURRENT (A)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	ADC2_5C % ERROR
120	792.9668	792.00	0.1221
100	660.8533	660.00	0.1293
80	528.7155	528.00	0.1355
60	396.6487	396.00	0.1638
40	264.3418	264.00	0.1295
20	132.1799	132.00	0.1363
10	66.0866	66.00	0.1313
5	33.0342	33.00	0.1038
2	13.2016	13.20	0.0119
1	6.5997	6.60	–0.0045
0.5	3.2945	3.30	–0.1676
0.25	1.6535	1.65	0.2146

注: AC current 50 Hz, 5 cycles, 4000 sampling rate, 400 S, X2 gain, 2.4-V reference

表 58. ADC Channel 2 Current With 4-V V_{REF}

AC CURRENT (A)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	ADC6_5C % ERROR
120	760.8927	792.00	–3.9277
102	672.5653	673.20	–0.0943
100	659.7455	660.00	–0.0386
80	528.0998	528.00	0.0189
60	396.1439	396.00	0.0363
40	264.2180	264.00	0.0826
20	132.0525	132.00	0.0398
10	66.0499	66.00	0.0756
5	33.0261	33.00	0.0790
2	13.2051	13.20	0.0384
1	6.6014	6.60	0.0206
0.5	3.3013	3.30	0.0405
0.25	1.6503	1.65	0.0176
0.2	1.3205	1.32	0.0399

注: AC current 50 Hz, 5 cycles, 4000 sampling rate, 400 S, X4 gain, 4-V reference

注: Measurement saturates after 102 A.

8.5.3 Current Measurement Accuracy With LPCT Output (333 mV)

表 59. ADC Channel 2 LPCT With 2.4-V V_{REF}

AC CURRENT (A)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	ADC2_5C % ERROR
60	396.4834	396.00	0.1221
50	330.4267	330.00	0.1293
40	264.3578	264.00	0.1355
30	198.3244	198.00	0.1638
20	132.1709	132.00	0.1295
10	66.0899	66.00	0.1363
5	33.0433	33.00	0.1313
2.5	16.5171	16.50	0.1038
1	6.6008	6.60	0.0119
0.5	3.2999	3.30	–0.0045
0.25	1.6472	1.65	–0.1676
0.1	0.6614	0.66	0.2146

注: AC current 50 Hz, 5 cycles, 4000 sampling rate, 400 S, X4 gain, 2.4-V reference

表 60. ADC Channel 2 LPCT With 4-V V_{REF}

AC CURRENT (A)	MEASURED VOLTAGE (mV)	ACTUAL VOLTAGE (mV)	ADC6_5C % ERROR
60	380.4464	396.000	–3.9277
51	336.2827	336.600	–0.0943
50	329.8728	330.000	–0.0386
40	264.0499	264.000	0.0189
30	198.0719	198.000	0.0363
20	132.1090	132.000	0.0826
10	66.0263	66.000	0.0398
5	33.0250	33.000	0.0756
2.5	16.5130	16.500	0.0790
1	6.6025	6.600	0.0384
0.5	3.3007	3.300	0.0206
0.25	1.6507	1.650	0.0405
0.125	0.8251	0.825	0.0176
0.1	0.6603	0.660	0.0399

注: AC current 50 Hz, 5 cycles, 4000 sampling rate, 400 S, X8 gain, 4-V reference

注: Measurement saturates after 51 A.

8.6 Fast Start-up and Fault Detection Testing

8.6.1 Fast Start-up Functionality

The start-up functionality was tested in the following stages:

1. DC–DC converter start-up: The time required for the DC-DC converter to provide the required output after applying the minimum start-up DC voltage.
2. Power-on reset (POR): The time in which the MCU is held in reset condition.
3. MCU start-up after DC-DC converter output reaches 12 V: The time required for the MCU to begin executing instructions after coming out of the reset condition.
4. ΔΣ ADC start-up after MCU start-up: The time after the ADC has been released from reset to measure the input DC voltage within 2% of the applied voltage.

注: The start-up testing was performed with DC input voltage applied. The expected DC voltage range was fixed in the firmware and the measured value was compared against the set limits.

DC-DC converter and MCU start-up time

The following 表 61 provides the DC-DC converter and MCU start-up timing including power-on reset (POR) timing. The tests were repeated multiple times to check for consistency

表 61. DC-DC Converter and MCU Start-up Timing

TEST	CONDITION	MEASUREMENT[1]	OBSERVATION
LM5017 DC-DC converter start-up	DC input voltage: ≥ 14 V DC-DC output: 12 V	≤ 0.65 ms	The start-up time was measured multiple times and checked for consistency
LM5160 DC-DC converter start-up	DC input voltage: ≥ 14 V DC-DC output: 12 V	≤ 0.6 ms	The start-up time was measured multiple times and checked for consistency
MCU power-on reset (undervoltage detection)	MCU POR time (after DC-DC output reaches 12 V)	≤ 0.35 ms	The POR was measured multiple times
MCU start-up	MCU start-up (start of execution of op-code) after POR	≤ 0.5 ms	The start-up time varies between 350 µs to 500 µs after testing multiple times

[1] Measurement uncertainty is ±0.1 ms.

The following waveforms provide information on the DC-DC converter and the MCU start-up timing.

図 32 shows the DC-DC start-up time waveform after the 24-V DC input reaches approximately 14 V. The blue line is connected to a 12-V output and the green line is connected to a 24-V input.

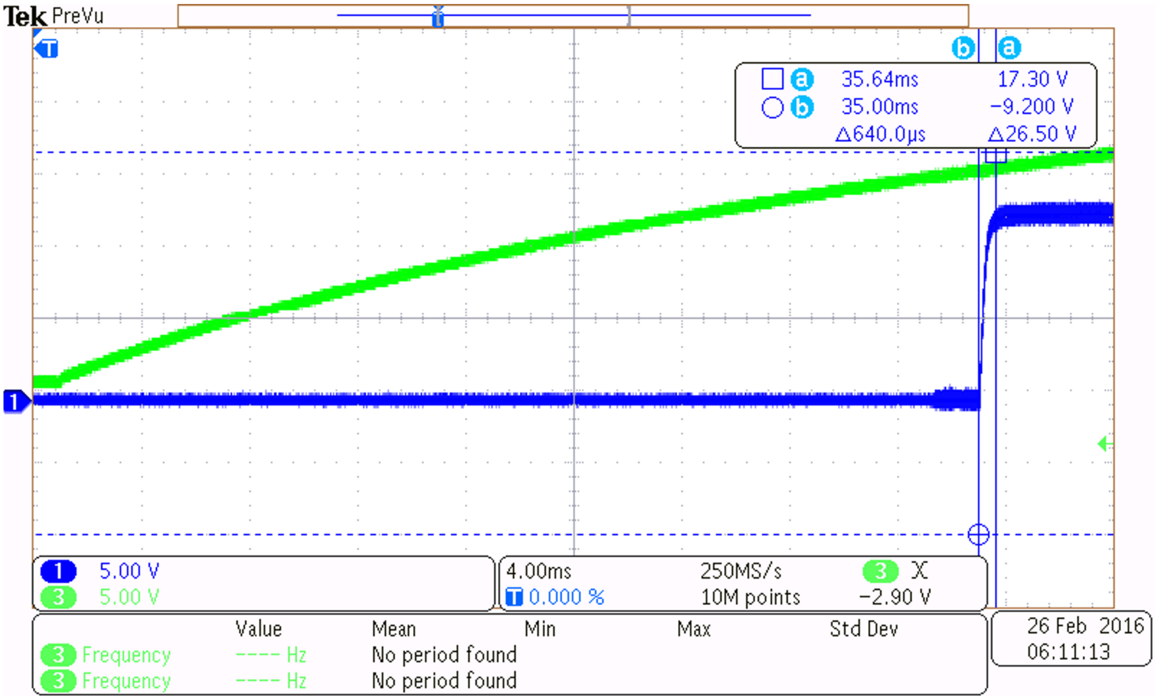
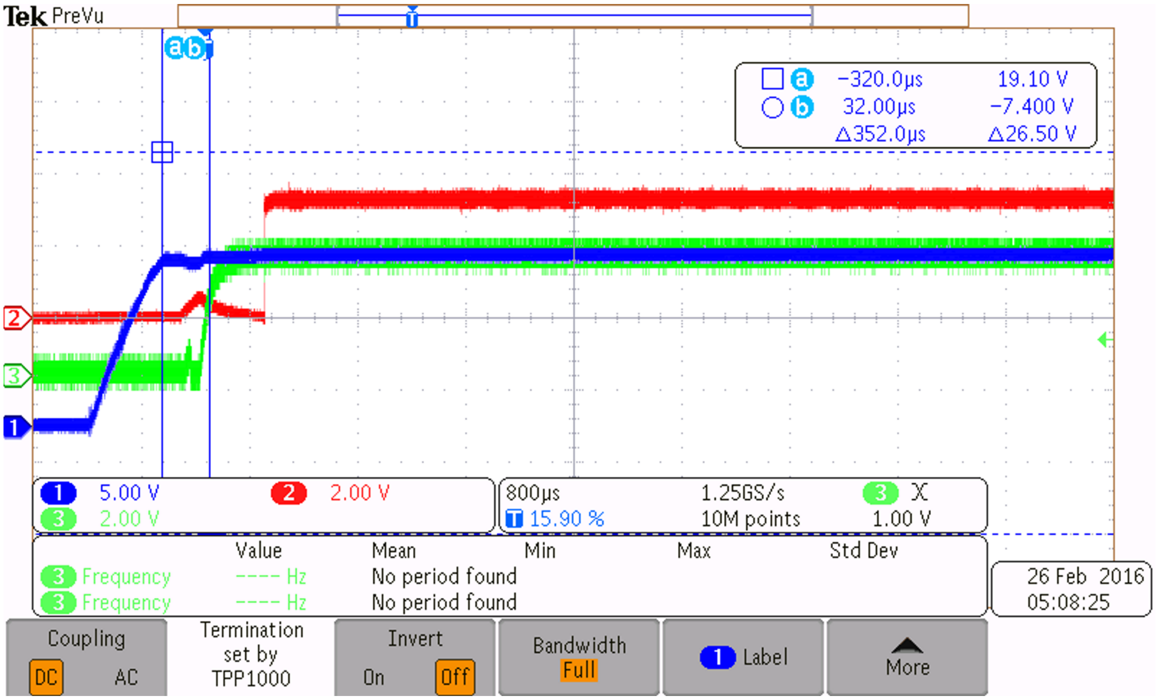


図 32. DC-DC Start-up Time

図 33 shows the MCU start-up time waveform after the DC-DC converter output reaches the 12-V output. The blue line is connected to a 12-V output. The green line is connected to the MCU reset input and the red line represents the MCU start-up.



a −320.0µs 19.10 V
b 32.00µs −7.400 V
Δ352.0µs Δ26.50 V

1 5.00 V 2 2.00 V
3 2.00 V

800µs 1.25GS/s 3 ⨯
T 15.90 % 10M points 1.00 V

	Value	Mean	Min	Max	Std Dev
3 Frequency	---- Hz	No period found			
3 Frequency	---- Hz	No period found			

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05:08:25

図 33. MCU Start-up Time

ADS131E08S ΔΣ ADC start-up

The ADC start-up time is the time for the ADC to provide a conversion samples output within ±2% of the applied input after the device has been initialized by the MCU. The following 表 62 provides the measurement time for the ADC start-up and 表 63 provides the start-up time for different data output rates.

表 62. Measurement Time for ADC Start-up

TEST	SAMPLING FREQUENCY	APPLIED DC INPUT (mv)	MEASURED VALUE (mV)	START-UP TIME (ms)(1)
ADC output measurement with 2.4-V ref	1 kHz	1056.517	1024.822 to 1088.213	4.90 to 4.96
ADC output measurement with 2.4-V ref	1 kHz	2013.557	2034.237 to 2160.066	4.92 to 4.96
ADC output measurement with 4-V ref	1 kHz	1099.312	1066.332 to 1132.291	4.912 to 4.928
ADC output measurement with 4-V ref	1 kHz	2097.087	2034.175 to 2160	4.92
ADC output measurement with 2.4-V ref	4 kHz	1056.517	1024.822 to 1088.213	2.288 to 2.30
ADC output measurement with 2.4-V ref	4 kHz	2013.557	2034.237 to 2160.066	2.532 to 2.534
ADC output measurement with 4-V ref	4 kHz	1099.312	1066.332 to 1132.291	2.532 to 2.534
ADC output measurement with 4-V ref	4 kHz	2097.087	2034.175 to 2160	2.534 to 2.538

(1) Measurement uncertainty is ±0.5 ms.

表 63. Start-up Time Summary

TEST	CONDITION	MEASUREMENT
LM5160 DC-DC converter start-up	DC input voltage: ≥ 14 V DC-DC output: 12 V	≤ 0.6 ms
MCU POR (undervoltage detection)	MCU POR time (after DC-DC output reaches 12 V)	≤ 0.35 ms
MCU start-up	MCU start-up (start of execution of op-code) after POR	≤ 0.5 ms
ADC output measurement with 4-V ref	ADC data output rate set to 4 kHz	2.534 ms to 2.538 ms
Total time for ΔΣ ADC (ADS131E08S) to measure within ±2% of the input voltage, after application of auxiliary DC input		< 4 ms

8.6.2 Fault Detection and Alarm Functionality

Fault detection can be implemented internal to the device using the integrated comparators with DAC-controlled trigger levels.

Refer to the subsection titled *FAULT: Fault Detect Control Register (address = 04h) [reset = 00h]* in the ADS131E08S datasheet (SBAS705) for instructions to configure the comparator high-side threshold and comparator low-side threshold. The DC voltage input was applied to test the fault detection alarm functionality and the DC input voltage was applied and tested using IN4P and IN4N of the ADC.

The following 表 64 shows the timing for detecting the fault input after an ADC reset.

表 64. Fault Detection and Alarm

REGISTER ADDRESS	VOLTAGE THRESHOLD SETTING	DC VOLTAGE APPLIED	OBSERVATION	TIME (FROM ADC POWER-UP)
FAULT (0x04)	0xE0 (70%)	2 V	FAULTP bit3 (channel4 is set)	< 1.6 ms
FAULT (0x04)	0xE0 (70%)	1.6 V	FAULTP bit3 (channel4 is clear)	< 1.6 ms
FAULT (0x04)	0xA0 (80%)	2.2 V	FAULTP bit3 (channel4 is set)	< 1.6 ms
FAULT (0x04)	0xA0 (80%)	1.7 V	FAULTP bit3 (channel4 is clear)	< 1.6 ms

注: The alarm functionality is detected during the first data read cycle.

MCU configuration

The MCU used for evaluating the start-up performance of the ADS131E08S device has been interfaced to the ΔΣ ADC as the following 表 65 shows.

表 65. MCU Configuration

ADC BOARD - J5[1]		MCU BOARD JUMPER – J14		PIN CONFIGURATION AND FUNCTIONALITY
PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	
5	ADC_CLKSEL	5	ADC_CLKSEL	Port configured as output and the level is programmed as low.
7	GPIO4	7	GPIO4	
13	ADC_RESET	13	ADC_RESET	Port configured as output. ADC is held in reset condition after power-up for ≈20 µs by programming the port level low. After the reset period, the level is programmed to high.
17	ADC_PWDN	17	ADC_PWDN	Port configured as output and the level is programmed as high.
6	ADC_SPI_IN	6	UCA0_SIMO	Configured as data out for SPI. This pin is used to transmit data from MCU to ADC.
8	ADC_START	8	ADC_START	Port configured as output and the level is programmed as high after configuring the ADC. Conversions begin when the START pin has been programmed high.
10	ADC_CS	10	ADC_CS	Chip select (CS) selects the ADS131E08S for SPI communication. Port configured as output and the level is programmed as low.
12	ADC_SPI_CLK	12	UCA0_CLK	Configured as clock output for SPI. MCU provides the clock output to ADC for SPI communication.
14	ADC_SPI_DOUT	14	UCA0_SOMI	Configured as data input for SPI. This pin is used to receive data from ADC to MCU.
16	ADC_DRDY	16	ADC_DRDY	Port configured as input. The DRDY output is used as a status signal to indicate when ADC data is ready for read back. DRDY goes low when new data become available.

[1] R94 must be de-populated on the MCU board to communicate with the ADC board.

8.7 IEC Pre-compliance Testing

The following EMC tests were performed:

表 66. EMC Tests

TESTS	STANDARDS
Surge	IEC61000-4-5
ESD	IEC61000-4-2

表 67. Performance Criteria

CRITERIA	PERFORMANCE (PASS) CRITERIA
A	The analog output module continues to operate as intended. No loss of function or performance (even during the test).
B	Temporary degradation of performance is acceptable. After the test, the analog output module continues to operate as intended without manual intervention.
C	During the test, loss of functions is acceptable, but no destruction of hardware or software. After the test, analog output module continues to operate automatically as intended, after manual restart or powering off or powering on.

8.7.1 IEC61000-4-5 Surge Test

The IEC61000-4-5 surge test simulates switching transients caused by lightning strikes or the switching of power systems, including load changes and short circuits. The test requires five positive and five negative surge pulses with a time interval between successive pulses of one minute or less. The unshielded symmetrical data line setup as defined by the IEC61000-4-5 specification was used for this test. The test generator was configured for 1.2/50 μs, 42-Ω surges and diode clamps were used for line-to-ground coupling. A series of five negative and positive pulses, with ten seconds spacing between each pulse, were applied during the test. The board was tested for performance before and after the test. The EUT was able to perform normally after each test.

表 68. Surge Test Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULTS
Surge, DM	IEC 61000-4-5: (1.2 / 50 μs to 8 / 20 μs), 42 Ω to 0.5 μF)	Across the potential divider	± 2 kV	Pass, Criteria B (After the test, the ADC module continued to operate as intended)

表 69. Surge Test Steps

TEST NUMBER	TEST MODE	OBSERVATION
1	1 kV	Pass
2	–1 kV	Pass
3	2 kV	Pass
4	–2 kV	Pass
5	3 kV	Pass
6	–3 kV	Pass

The following 図 34 shows the surge setup for the ADC board.

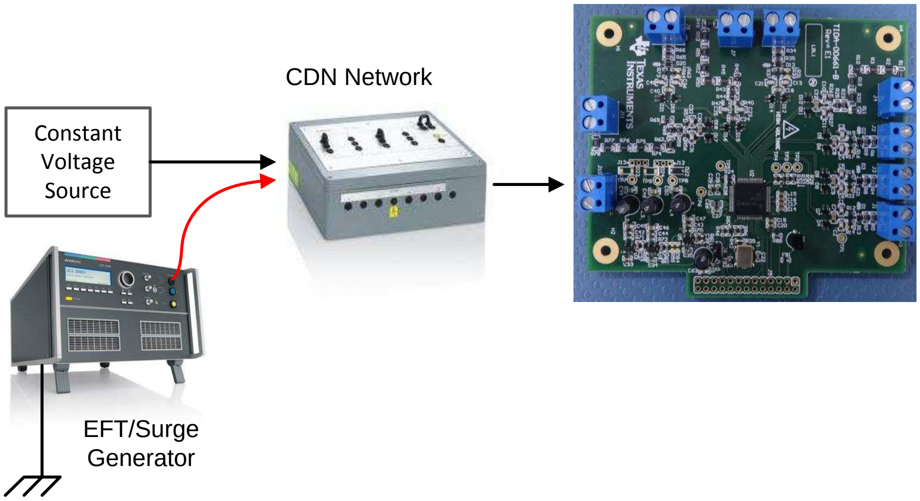

図 34. Surge Setup for ADC Board

8.7.2 IEC61000-4-2 ESD Test

This standard specifies the ability of a system to withstand ESD events. This standard describes the conditions under which direct or air discharge testing is ideally performed. In this application, metallic chassis grounded network connectors were utilized, so the direct coupling method was required. Applications utilizing all plastic chassis and connectors require air discharge testing. Specifications are provided for rise time, current, and impedance control of the voltage applied in the testing. TI's serial communications devices have been designed and tested to withstand ESD energy on a component level as specified in the individual device datasheets. IEC testing is defined for system level testing, which complements the component testing conducted by TI.

To simulate a discharge event, an ESD generator applies ESD pulses to the equipment-under-test (EUT), which can happen through direct contact with the EUT (contact discharge). This ESD pulse was applied across the RJ45 connector. A series of ten negative and positive pulses were applied during the test (contact discharge). After the ESD test, a communication test was performed. The test results show that the EUT was able to withstand the required discharge. The EUT was not permanently damaged.

表 70. ESD Test Steps

TEST NUMBER	TEST MODE	OBSERVATION
1	Contact 2 kV	Pass
2	Contact –2 kV	Pass
3	Contact 4 kV	Pass
4	Contact –4 kV	Pass
5	Contact 6 kV	Pass
6	Contact –6 kV	Pass

表 71. ESD Testing —Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
ESD	IEC 61000-4-2, contact	Across voltage and current input	±4 kV	Pass, Criteria B (After the test, the ADC module continued to operate as intended)

The following 図 35 shows the ESD setup for the ADC board.

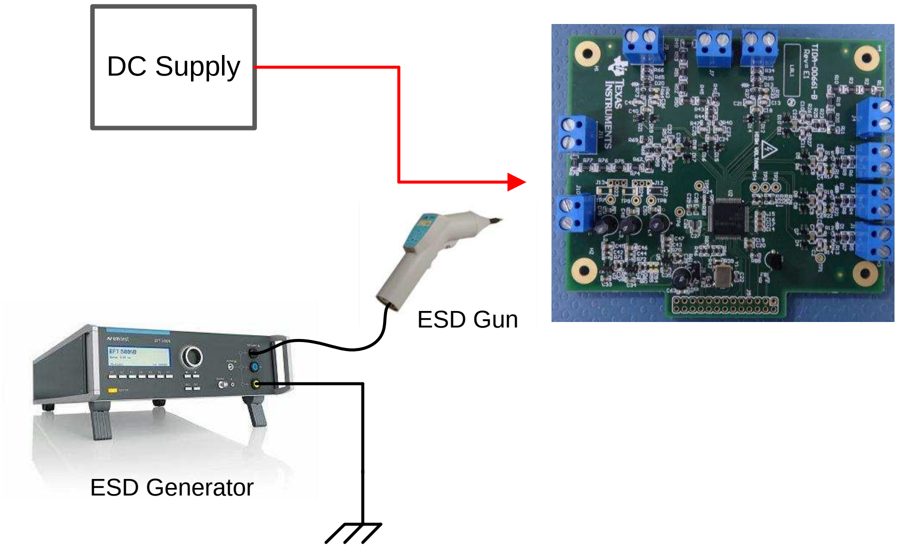

図 35. ESD Setup for ADC Board

8.8 Summary of Test Results

表 72. Test Results Summary

SERIAL NUMBER	PARAMETERS	RESULT
1	Self-power and auxiliary power input functionality	OK
2	DC-DC converter output 2 W and 8 W	OK
3	LDOs on MCU board and ADC board	OK
4	ADC interface to ADS131E08 MMB0 EVM	OK
5	ADC performance at different gains, sampling rates, and analog inputs at 50 Hz and 60 Hz	OK
6	Earth fault current input and op amp functionality	OK
7	MCU functionality and measurement of ADC inputs	OK
8	Measurement accuracy testing for voltage and current input	OK
9	ADC startup time for measuring the input within ±2%	< 4 ms

9 Design Files

9.1 Schematics

To download the schematics for each board, see the design files at TIDA-00661.

9.2 Bill of Materials

To download the bill of materials (BOM) for each board, see the design files at TIDA-00661.

9.3 Layout Prints

To download the layout prints for each board, see the design files at TIDA-00661.

9.4 Altium Project

To download the Altium project files for each board, see the design files at TIDA-00661.

9.5 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00661.

9.6 Assembly Drawings

To download the assembly drawings for each board, see the design files at TIDA-00661.

10 References

1. Texas Instruments, *Signal Processing Front End for Electronic Trip Units Used in ACBs/MCCBs*, TIDA-00498 User's Guide (TIDUA09)
2. Texas Instruments, *Performance Demonstration Kit for the ADS131E08*, ADS131E08EVM-PDK User's Guide (SBAU200)

11 Terminology

ACB— Air circuit breaker

CT— Current transformer

MCB— Miniature circuit breaker

MCCB— Molded-case circuit breaker

MCR— Making current release

PD— Potential divider

ZSI— Zone selective interlocking

12 About the Author

KALLIKUPPA MUNIYAPPA SREENIVASA is a systems architect at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Sreenivasa brings to this role his experience in high-speed digital and analog systems design. Sreenivasa earned his Bachelor of Electronics (BE) in electronics and communication engineering (BE-E&C) from VTU, Mysore, India.

リビジョンBの改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (March 2016) から **Revision B** に変更 **Page**

- *タイトルを「気中遮断器(ACB)用の高分解能、高速スタートアップのアナログ・フロントエンドのリファレンス・デザイン」から* 変更 1
- 「設計リソース」にADS131E08を 追加 1
- 「デザインの特長」に、電流測定精度の箇条書き項目を 追加 1
- 「デザインの特長」に、電圧測定精度の箇条書き項目を 追加 1
- 「デザインの特長」に、LPCTでの測定精度の箇条書き項目を 追加 1
- link to ADS131E08 product page in 4.1.1 追加 20
- 5.15.1: Improved Measurement Accuracy With ADS131E08 追加 47
- 8.5: Testing With ADS131E08 追加 81
- note under 表 55 追加 81
- note under 表 58 追加 82
- note under 表 60 追加 83

リビジョンAの改訂履歴

2016年1月発行のものから更新 **Page**

- 時間の種類を指定するため「スタートアップ」を 追加 1
- 箇条書きの「TI製のMSP430™ MCUにより高速なスタートアップを実現、スタートアップ時間と1サイクルのRMS計算時間の合計は30ms未満」を、現行の「Δ∑ ADC (ADS131E08S)の合計スタートアップ時間が4ms未満で、補助DC入力の印加後に±2%以内の精度で入力電圧を測定」に 変更 1
- 「電源品質アナライザ」を「リクローザ」に 変更 1
- from "applied to the device" to "applied to DC-DC converter 変更 16
- from "Power output" to "Voltage output" 変更 55
- "Operate" to specify which action for UVLO 追加 55
- from "Power output" to "Voltage output" 変更 55
- Serial number 8 row to table 追加 56
- 8.6 *Fast Start-up and Fault Detection Testing* 追加 84
- a row for serial number 9 追加 91

TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関係する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、あるいはTIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。