参考資料

TI Designs: TIDA-00446
三相インバータ向け、小フォーム・ファクタの強化絶縁型IGBTゲート・ドライブのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインは、6つの強化絶縁型IGBTデータ・ドライバと、専用のゲート・ドライブ電源で構成されます。この小型のリファレンス・デザインは、ACドライブ、無停止電源装置(UPS)、ソーラー・インバータなどの三相インバータのIGBTをコントロールします。このデザインは強化絶縁型のIGBTゲート・ドライバと、内蔵のIGBT DESAT検出およびミラー・クランプ保護機能を使用しているため、ゲート・ドライブにユニポーラ電源電圧を使用できます。各ゲート・ドライバ用に、オープン・ループのプッシュプル・トポロジをベースとする電源が存在するため、PCBを柔軟に配線できます。TIDA-00446で使用されるプッシュプル変圧器ドライバは420kHzで動作するため、絶縁トランスのサイズを小さくでき、コンパクトな電源ソリューションを設計できます。ゲート・ドライブの電源を無効にすると、セーフ・トルク・オフ(STO)が容易に実現されます。

リソース

TIDA-00446	デザイン・ファイルを含むツール・フォルダ
SN6505B	プロダクト・フォルダ
ISO5851	プロダクト・フォルダ
TPS70633	プロダクト・フォルダ

TI E2E™ Community

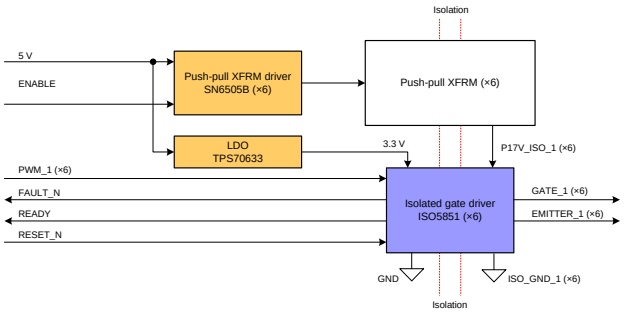
E2Eエキスパートに質問

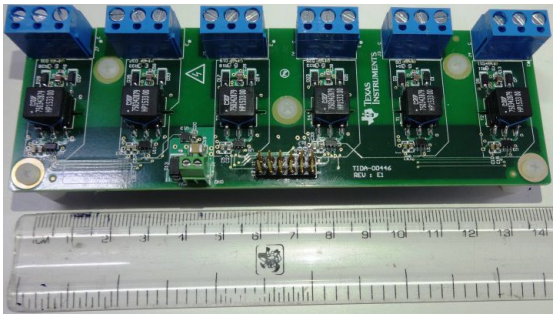
特長

- 低電圧ドライブに最適(400V ACおよび690V AC)
- 内蔵の2.5Aソースおよび5Aシンク電流は、最大50Aの電流によるIGBTモジュールの駆動に最適
- ミラー・クランプ機能を内蔵しているため、IGBTの駆動にユニポーラ電源(17V)を使用可能
- 保護機能を内蔵
  - DESAT検出による短絡保護
  - 電源低電圧保護
- 独立したRg(ON)およびRg(OFF)用の機構
- 8000VPKの強化絶縁
- 非常に高いCMTI、100kV/us超
- 変圧器ドライバの拡散スペクトラム動作によりEMI放射が低減
- PWMおよびゲート・ドライバのフォルト信号をコントローラと直接接続可能(3.3V動作)

アプリケーション

- 速度可変ドライブ
- UPS
- 太陽光インバータ
- 溶接機





1 Key System Specifications

表 1. Key System Specifications

FEATURE	PARAMETER	SPECIFICATION
Gate drive	Voltage	17 V ± 2 V
	Current	2.5 A Source and 5 A Sink
	Output power	1 W/IGBT
Isolation	CMTI	100 kV/µs
	Isolation	3000 Vrms for 1 Minute
	Working voltage	1400 Vp
Interface	Voltage	3.3 V
	Input signals	PWM, RESET and ENABLE_N
	Output signals	READY and FAULT_N
System and drive specifications	Drive input voltage	Up to 690-V AC
	Power supply input Voltage	5 V ± 5%
Protection	IGBT DESAT detection. Indicated by FAULT_N signal	
	Gate driver primary and secondary side power undervoltage lockout. Indicated by READY signal	
	2 A Active Miller Clamp	
	Output Short Circuit Clamping of Gate Driver Output	
	1.7 A Input Current Limit of Push-pull Power Supply	
	Thermal Shutdown of Push-pull Driver	

2 Introduction

IGBT Gate drivers are an inherent part of any 3-phase inverter system. High power inverter systems require isolation for:

- Meeting safety requirements (Standards provided in ISO61800-5-1 for variable speed drives). The output power stage of the drive can have dangerously high voltages. Isolation is used to electrically separate the low voltage operator side from the high voltage drive stage.
- Driving the top switch of an inverter half bridge. In order to drive the top switch of an inverter half bridge, the applied gate voltage has to be with respect to the half bridge phase terminal. This point is floating, meaning the phase terminal switches between the DC bus voltage and the ground.
- Managing voltage level translation. The MCU generates a PWM signal at low-voltage levels, such as 3.3 or 5 V. The gate controls required by the IGBTs are in the range of 15 to 20 V and need high current capability to drive the large capacitive loads offered by those power transistors.
- Avoiding high current ground loops. High current ground loops can be localized in the isolated ground plane, which protects the primary side sensitive electronics from ground bounce and switching noise. This increases EMI/EMC performance by reducing the ground loop area.

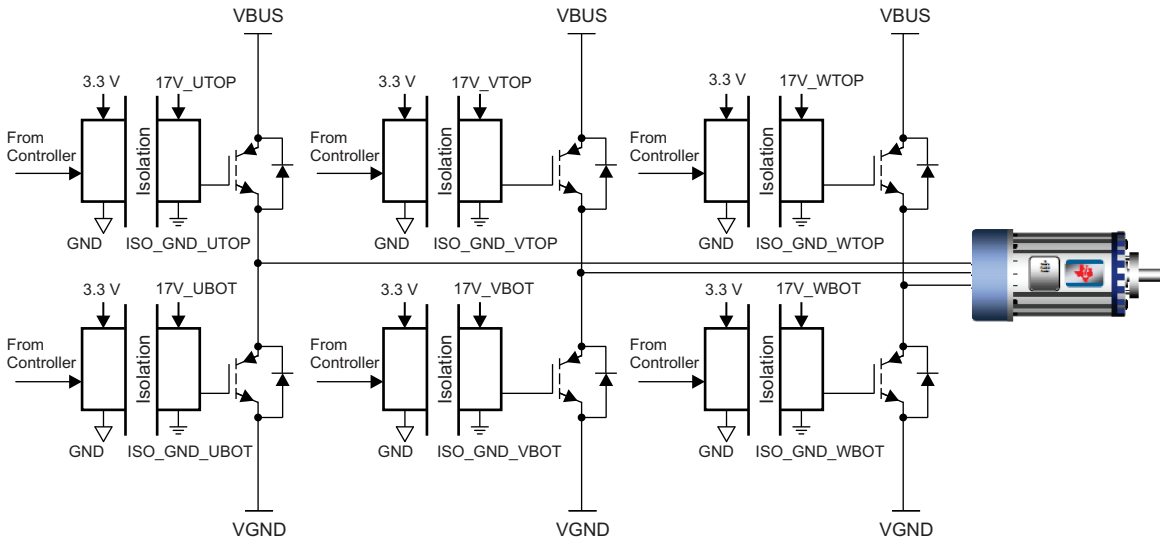


図 1. System Diagram

This reference design provides a tiny form factor reinforced isolated gate driver subsystem for a three phase inverter. The design uses the SN6505B push-pull transformer driver for generating the isolated power supply for the ISO5851 gate driver.

The reference design offers these key benefits:

- Small size of magnetics due to high switching speed (424 kHz) of the SN6505B transformer driver
- Integrated active Miller clamp circuit in the ISO5851 gate driver enabling the use of a unipolar power supply to drive the IGBT
- Low EMI due to spread spectrum clocking of the push-pull transformer driver
- Distributed power supply architecture leading to PCB routing flexibility

Various parameters of the design like load and line regulation, power supply efficiency, IGBT short circuit protection capability of the gate driver, and the active Miller clamp functionality are tested and documented.

3 Block Diagram

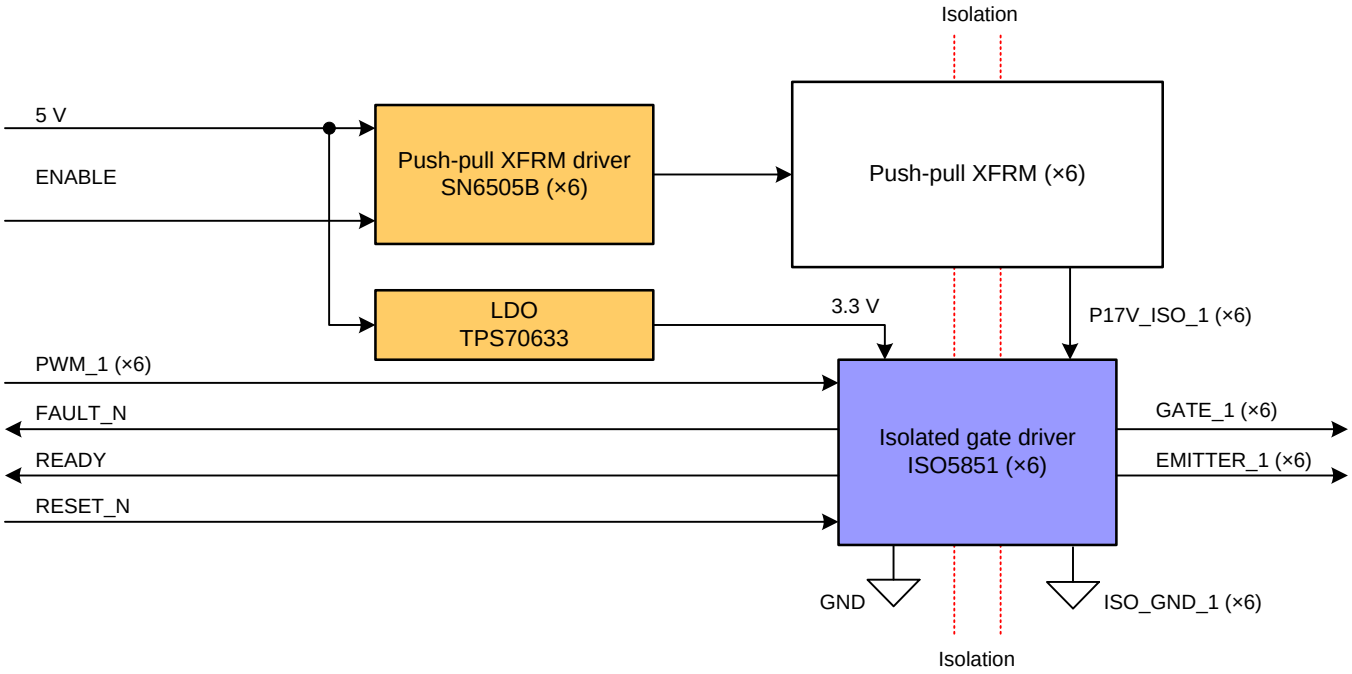


図 2. Block Diagram

The TIDA-00446 board consists of two main circuit blocks: the isolated gate driver (ISO5851) and the isolated power supply (SN6505 & Transformer) for the gate drive. The primary side of the gate driver is powered from 3.3 V power supply and the secondary, high voltage side is powered from a 17 V isolated power supply. The 17 V isolated supply is derived from a 5 V input rail with the help of a push-pull converter. The converter uses the SN6505B push-pull transformer to drive a center tapped transformer to generate an isolated power supply rail.

A 3-phase inverter has six IGBT switches, so the gate drive section is replicated six times in the board. An individual gate drive and isolated power supply per switch helps achieve a distributed architecture, which increases the flexibility of the PCB layout.

The board has eight control signals consisting of six PWM signals, a reset signal, and an enable signal. The board also provides two monitor signals: the fault and the ready signal. All signals are brought out to a two-row, six-column (2 × 6) berg stick connector and can connect to a 3.3 V powered microcontroller. The fault signal is an open-drain, active-low signal from the gate driver, which indicates a short circuit in the associated power switch. All six fault signals are logic ANDed together and the resultant signal is made available on the connector. The ready signal is an open-drain power-good signal, which turns active-high when both the primary and secondary power supplies of the gate driver are good. All six ready signals are also logic ANDed together, with the resultant signal made available on the connector. The enable signal disables SN6505. When the enable signal is high all the power supplies are turned off and the board input power reduces to 1 mW. The reset signal reset the fault latch. A 800 ns low pulse is required to reset the fault latches. The enable and reset signal are common to all the gate drivers.

TPS70633 LDO is used to generate a 3.3-V rail from a 5-V input rail for the primary side of the isolated gate drivers. On drive boards where a 3.3-V rail is available, skip this LDO.

3.1 Highlighted Products

The TIDA-00446 reference design features the following Texas Instruments devices:

- SN6505B — A small form factor, low-noise, low-EMI push-pull transformer driver, 2.25 to 5.5 V input voltage range, 1 A output drive, 1.7 A current limit, switches at 420 kHz, on-chip integrated ground-referenced N-channel power switches, thermal shutdown and soft start features, –55°C to 125°C operating temperature range, extremely small 6-pin SOT23/DBV package.
- ISO5851 — A reinforced isolated gate driver, 2.5 A gate source and 5 A sink current, 3 to 5.5 V primary side input voltage range, 15 to 30 V secondary side input voltage range, inbuilt active Miller clamp, built-in desaturation detection indicated by fault pin, input and output undervoltage lockout indicated by ready pin.
- TPS706 — An ultralow quiescent current LDO, built-in thermal-shutdown, current-limit and reverse-current protection, 2.7 to 6.5 V input voltage range, 3.3 V ± 2 % output, 150 mA output capability.

For more information on each of these devices, see the respective product folders at www.ti.com or click the links for the product folders on the first page of this reference design under Design Resources.

4 System Design Theory

Push-pull converters use center tap transformers to transfer power from the primary side to the secondary side. 図 3 explains how the push-pull converter functions.

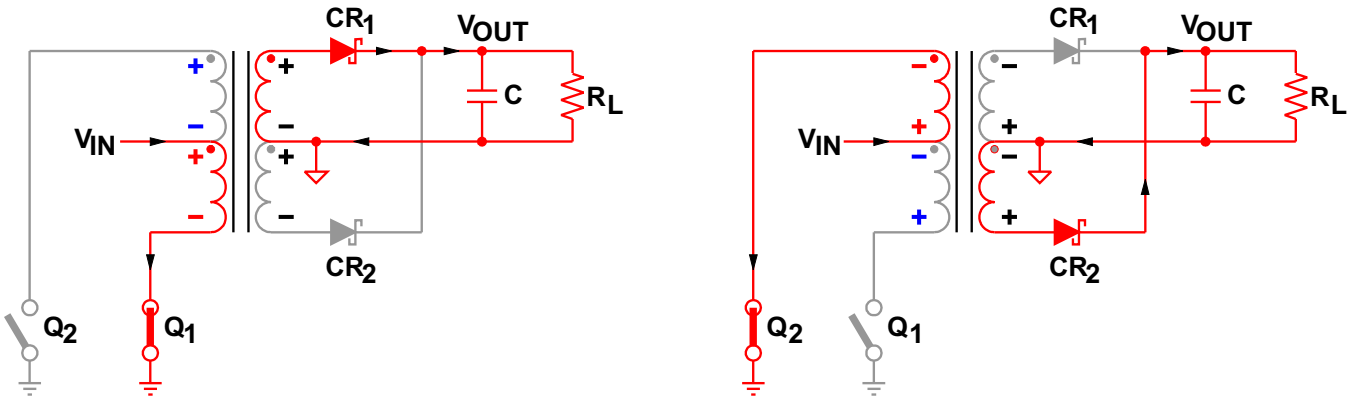


図 3. Push-pull Converter Theory of Operation

When Q1 conducts, current is sourced from VIN into the ground through the lower half of the primary of the transformer, creating a negative potential at the lower half of the primary winding compared to the primary center tap. In order to maintain the previously established current through Q2, which has now been opened, the upper half of the primary winding turns positive compared to the primary center tap. This voltage transfers to the transformer secondary according to the dot convention and the turns ratio of the transformer. CR1 is now forward biased and CR2 is reverse biased, causing a current to flow through the upper half of the secondary winding, passing through CR1 into C, charging the capacitor and returning into the secondary center tap.

Similarly, when Q2 conducts the voltage, polarities at the primary and secondary reverse. CR1 is reverse biased and CR2 is forward biased, which causes a current to flow from the bottom half of the secondary through CR2 into C, charging the output capacitor and returning into the center tap of the transformer. Q1 and Q2 switch alternatively, with approximately 50% duty cycle to transfer power from the primary to the secondary of the transformer.

Before either switch is turned on, there must be a short period during which both transistors are high impedance. This short period, known as break-before-make time, is required to avoid shorting out both ends of the primary.

Another important aspect of push-pull designs is transformer core magnetization. 図 4 shows the ideal magnetizing curve for a push-pull converter with B as the magnetic flux density and H as the magnetic field strength. When Q1 conducts, the magnetic flux is pushed from A to A'. When Q2 conducts, the flux is pulled back from A' to A. The difference in flux and in flux density is proportional to the product of the primary voltage, V_p, and the time, t_{ON}, applied to the primary: $B = V_p * t_{ON}$.

The volt-seconds (V-t) product determines the core magnetization during each switching cycle. If the V-t products of both phases are not identical, an imbalance in flux density swing results in an offset from the origin of the B-H curve. Unless balance is restored, the offset increases with each following cycle and the transformer slowly moves towards the saturation region.

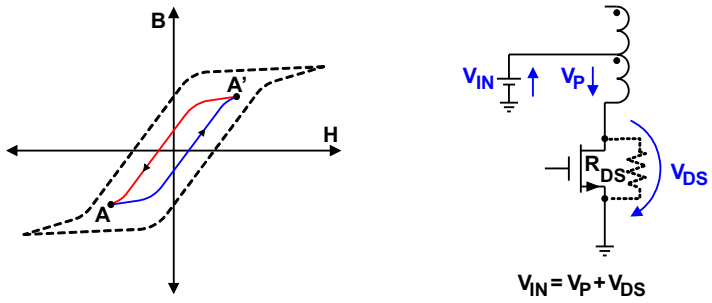


図 4. Push-pull Transformer Core Magentization and Self Regulation Through Positive Temperature Coefficient of R_{DSON}

The SN6505 push-pull transformer driver has integrated MOSFET switches. The positive temperature coefficient of these switches has a self-correcting effect on the V-t imbalance. During a slightly longer on-time, the prolonged current flow through a FET gradually heats the MOSFET, which leads to an increase in R_{DSon}. The higher resistance then causes the drain-source voltage, VDS, to increase. Because the voltage at the primary is the difference between the constant input voltage, V_{IN}, and the voltage drop across the MOSFET, $V_P = V_{IN} – V_{DS}$, V_P is gradually reduced and V-t balance is restored.

4.1 Design of Push-pull Power Supply

This section describes the steps in designing a push-pull power supply with the help of a SN6505B device. 図 5 shows the application circuit. The power supply specifications are given in 表 2.

表 2. Push-pull Power Supply Specification

PARAMETER	SPECIFICATION
V_{in}	5 V ± 5%
V_{out}	17 V
Output ripple	< 200 mV When sourcing 2.5 A for gate drive
P_{out}	1 W

The design requires selection of minimal external discrete components: transformer, rectifier diodes, and input and output bulk capacitors.

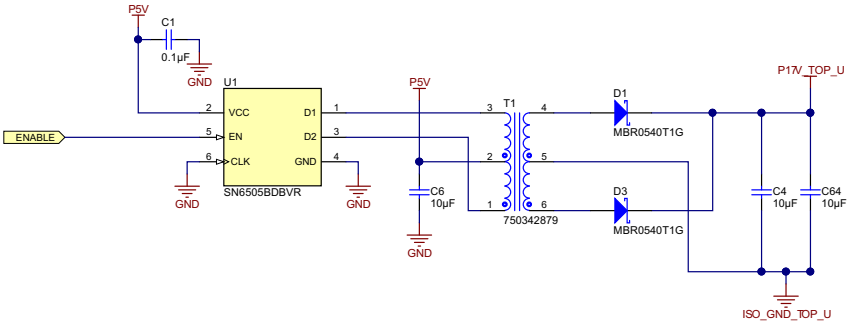


図 5. Isolated Power Supply Based on Push-pull Topology

4.1.1 Rectifier Diode Selection

To increase the efficiency of the push-pull forward converter, the forward voltage drop of the secondary side rectifier diodes should be minimized. Because the SN6505B is a high frequency switching converter, the diode must possess a short recovery time. Schottky diodes are selected as they meet the requirements of low forward voltage drop and fast recovery time. The diode should withstand a reverse voltage of twice the output voltage.

In this design, the nominal reverse voltage across the diode is 34 V. For 1 W at output voltage of 17 V, the output current is approximately 60 mA. 図 6 shows the diode MBR0540T1G forward characteristics. The diode has a forward voltage drop of less than 0.39 V at 25°C. The reverse DC blocking voltage rating of this diode is 40 V.

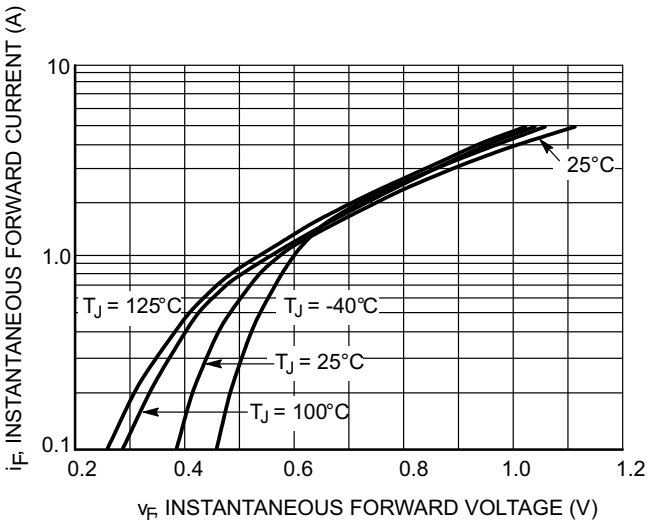


図 6. Instantaneous Current Versus Forward Voltage Drop (MBR0540T1G Datasheet)

4.1.2 Capacitor Selection

Two capacitors are required at the input V_{cc} of SN6505B. A ceramic bypass capacitor of 100 nF is needed close to the power supply pin of the device for noise decoupling because the device is a high speed CMOS IC. Another bulk capacitor is needed at the center tap pin of the primary of the transformer. Large currents are drawn from this capacitor into the primary during the fast switching transients. For minimum ripple select a 10 µF ceramic capacitor.

A bulk capacitor is required at the rectifier output stage to smooth the output voltage. The output voltage ripple specification is 200 mVpp. The maximum current that will be drawn out of this capacitor is 2.5 A_{pk}, which is the gate sourcing capability of the gate driver IC. 式 1 shows how the capacitance required to meet this specification is calculated.

$$C \geq \frac{i \times dt}{dv} = \frac{2.5\,A \times 0.5\,\mu s}{200\,mV} = 6.25\,\mu F \quad (1)$$

Approximately, a 10 µF capacitor meets the ripple requirement. The DC bias effect must be considered when selecting the capacitor. 図 7 shows that for the C3216X7R1V106K160AC capacitor used in this design, the capacitance at 17 V calculates to 4.3 µF. Hence two capacitors are connected in parallel to achieve the required capacitance.

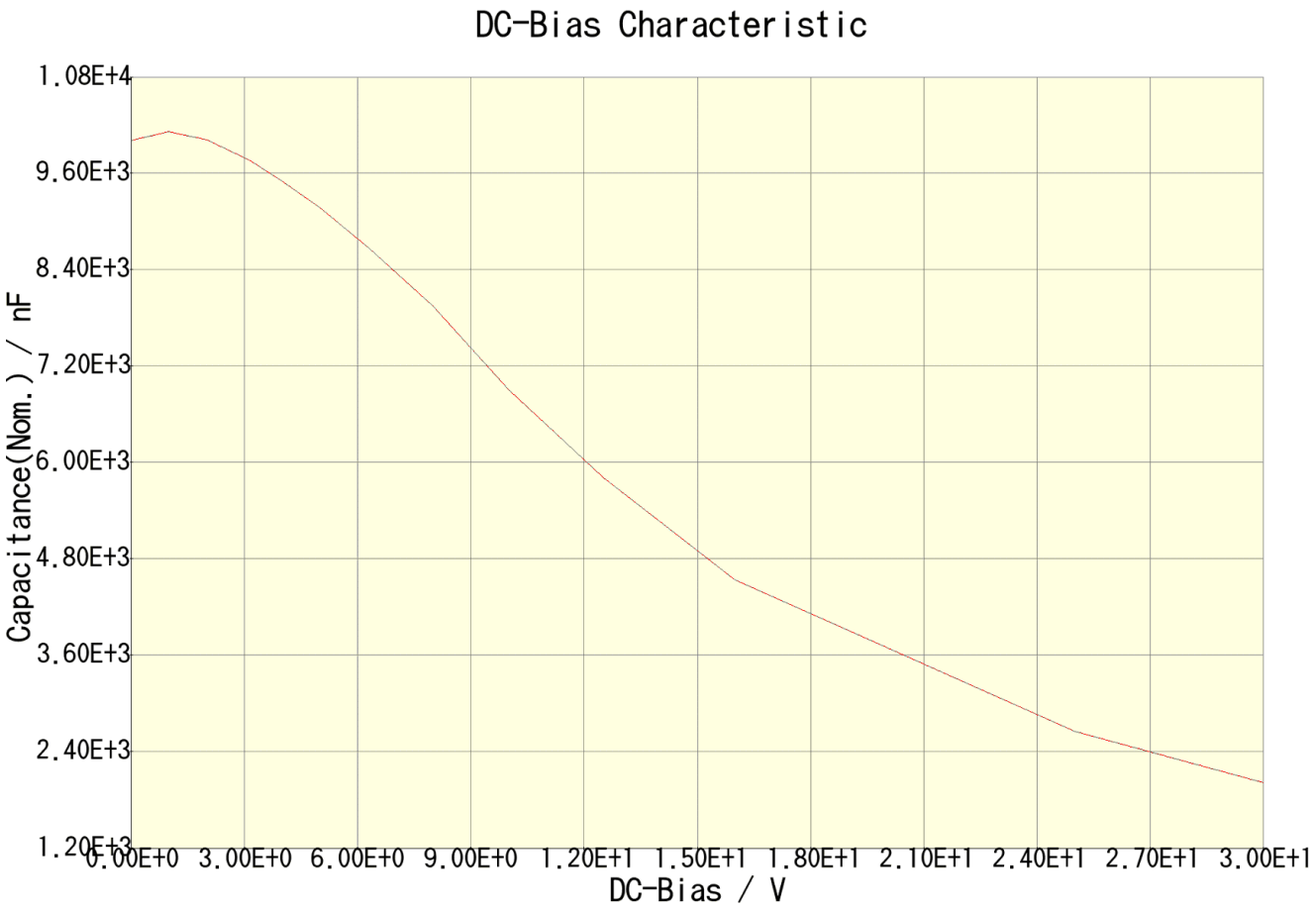


図 7. Variation of Capacitance With Applied DC Bias for C3216X7R1V106K160AC

4.1.3 Transformer Selection

表 3 lists the required specifications of the push-pull transformer, and the subsequent sections explain V-t product and turns ratio calculation.

表 3. Transformer Requirements

PARAMETER	SPECIFICATION
Output power	1 W
Output voltage	17 V
Input voltage	5 V
Minimum operating frequency	348 kHz
Working voltage	1400-V DC
Minimum creepage distance	9.2 mm (per IEC61800-5-1)
Minimum clearance distance	8 mm (per IEC61800-5-1)
Insulation	Reinforced
Operating temperature range	-40°C to 125 °C

4.1.3.1 V-t Product Calculation

The V-t product of the transformer must be greater than the maximum V-t product applied by SN6505B. Failure to meet this criteria leads to transformer core saturation. 式 2 calculates the worst case V-t product applied by SN6505B to the transformer:

$$Vt_{min} \geq V_{IN\_max} \times \frac{T_{max}}{2} = \frac{V_{IN\_max}}{2 \times f_{min}} \quad (2)$$

$$Vt_{min} \geq \frac{5.25\ V}{2 \times 348.48\ kHz} = 7.53\ V\mu s \quad (3)$$

- V_{IN-max} is the maximum input voltage = 5 V + 5% = 5.25 V
- f_{min} is the minimum frequency of operation = $F_{sw-min} – \Delta F_{sw}$ = 363 kHz – 14.52 kHz = 348.48 kHz
- F_{sw-min} is the minimum switching frequency of SN6505B = 363 kHz
- ΔF_{sw} is the spread spectrum frequency spread = 4% of F_{sw} = 4% of 363 kHz = 14.52 kHz

Spread spectrum frequency spread (ΔF_{sw}) is the variation of switching frequency around the average to reduce EMI. The frequency spreading can have different profiles, such as:

- sawtooth
- sinusoidal
- Hershey
- triangular

depending on the device. Spread spectrum clock modulation frequency (F_{SSC}) is the frequency at which frequency spreading (ΔF_{sw}) occurs. 図 8 shows an example triangular frequency spreading profile that explains the parameters of ΔFsw and F_{SSC}:

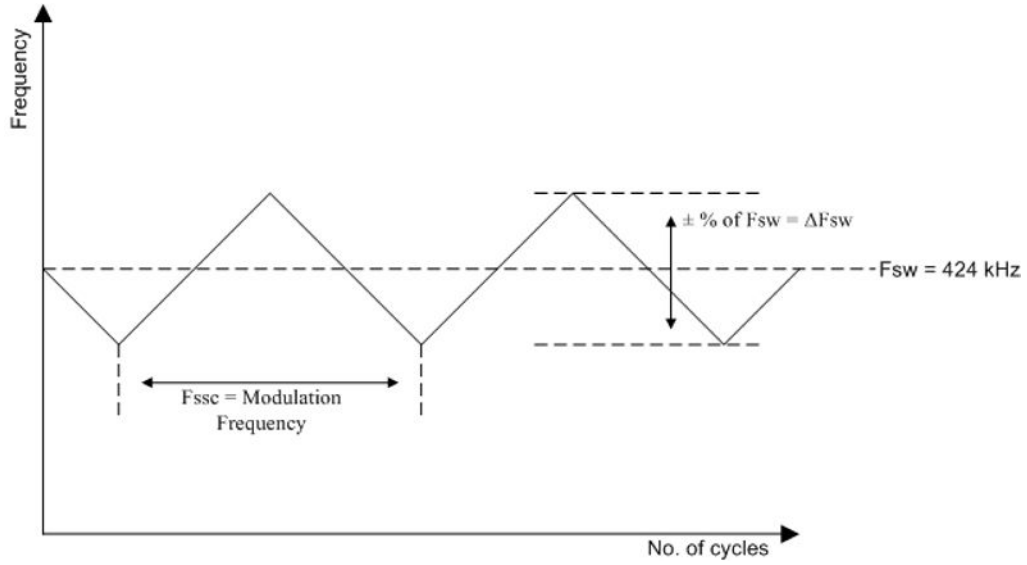


図 8. Modulation Frequency and Spread Spectrum Frequency Spread

4.1.3.2 Turns Ratio Calculation

Calculate the turns ratio of the transformer based on the input and output voltage, the output diodes forward drop, and the ON resistance of the input switches. The following calculation assumes the transformers typical efficiency of 97%:

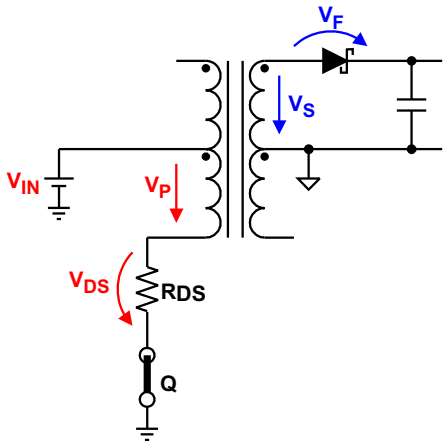


図 9. Establishing Turns Ratio

式 4 provides the output voltage of the converter:

$$V_{OUT\_nom} = V_{S\_nom} - V_f \Rightarrow V_{S\_nom} = V_{OUT\_nom} + V_f \quad (4)$$

- V_f is the forward voltage drop of the rectifier diode
- VS is the voltage across the top half of the secondary of the transformer

式 5 calculates the voltage across the lower half of the primary coil of the transformer:

$$V_{P\_nom} = V_{IN\_nom} - V_{ds} \quad (5)$$

$$V_{P\_nom} = V_{IN\_nom} - \left(I_{P\_nom} \times R_{DS\_on}\right) \quad (6)$$

- V_{ds} is the voltage drop across the integrated lowside switch in SN6505B
- I_p is the current through the primary
- $R_{ds\text{-}on}$ is the on resistance of the integrated lowside switch in SN6505B

式 7 determines the turns ratio of the transformer. The factor 0.97 accounts for typical transformer power transfer efficiency.

$$V_{S\_nom} = V_{P\_nom} \times n_{nom} \times 0.97 \Rightarrow n_{nom} = 1.031 \times \frac{V_{S\_nom}}{V_{P\_nom}} \quad (7)$$

式 8 is derived by substituting 式 4 and 式 6 in 式 7. The turns ratio of the transformer is calculated to be 3.5.

$$n_{nom} = 1.031 \times \frac{V_f + V_{OUT\_nom}}{V_{IN\_nom} - \left(I_{P\_nom} \times R_{DS\_on}\right)} = 1.031 \times \frac{0.35 + 17}{5 - \left(0.1 \times 0.16\right)} = 3.58 \frac{n_s}{n_p} \quad (8)$$

- $R_{DS\text{-}on}$ = 0.16 Ω is the typical value of the switch ON resistance taken from the SN6505B datasheet
- $I_{P\text{-}nom}$ is calculated at 50% load; $I_{p\text{-}nom} = P_{in}/V_{in}$ = 0.5 W / 5 = 0.1 A

A Wurth Electronics transformer, 750342879, is selected for this design. 表 4 provides the specifications of this transformer:

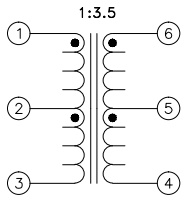


図 10. Push-pull Transformer — 750342879 (Wurth Electronics)

表 4. Selected Transformer Specifications

PARAMETER	SPECIFICATION
Turns ratio (6 – 4):(1 – 3)	3.5:1, ±2 %
DC resistance (1 – 3)	0.33 A_{max} @ 20 °C
DC resistance (6 – 4)	0.75 A_{max} @ 20 °C
Inductance (1 – 2)	50 µH min @ 100 kHz, 10-mV AC
Dielectric (1 – 6)	3000 V_{rms}, 1 minute
Operating temperature range	–40°C to 125°C
Creepage distance (IEC61800-5-1)	9.2 mm
Clearance distance (IEC61800-5-1)	8 mm
Transformer dimensions	12.7 mm × 9.14 mm × 7.62 mm (see 図 11)

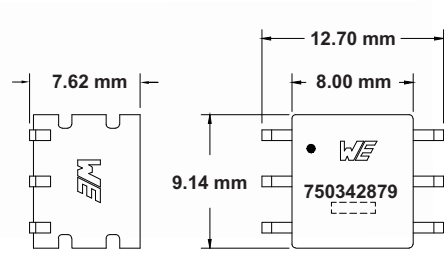


図 11. Transformer Dimensions in mm

4.2 Gate Driver Design

Six gate drivers drive the six power switches of a 3-phase inverter. 表 5 lists the individual gate driver requirements:

表 5. Gate Driver Specifications

PARAMETER	SPECIFICATION
Primary side input voltage	3.3 V ± 5 %
Secondary side input voltage	17 V ± 2 V
Gate drive source current capacity	2.5 A_{max}
Gate drive sink current capacity	5 A_{max}
Maximum output switching frequency	16 kHz
Maximum secondary side output power	1 W
Maximum output power to gate	0.85 W
Short circuit protection capability	Yes
Miller clamp functionality	Yes

表 5. Gate Driver Specifications (continued)

PARAMETER	SPECIFICATION
Undervoltage protection	Yes

Note: For operation above 16 kHz, select higher wattage gate resistors as per 4.2.2.2

ISO5851 meets all the requirements in 表 5. 図 12 implements the reinforced isolated gate driver using ISO5851:

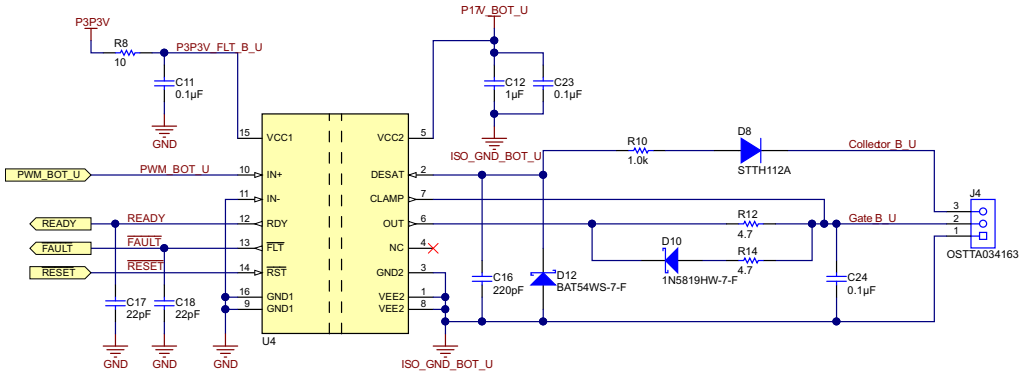


図 12. Isolated Gate Driver Circuit

4.2.1 through 4.2.8 describe in detail the steps for selecting gate driver components:

4.2.1 Power Supply Capacitors

A 3.3-V power supply powers the primary side of the ISO5851. An RC filter filters this 3.3-V rail before connecting to the gate driver power supply.

A 17-V isolated supply rail powers the secondary side of the ISO5851, which is generated from the push-pull power stage described in 4.1. A 1-µF bulk capacitor connects beside the V_{CC2} pin. The gate source current draws from this power pin and the 1-µF bulk capacitor provides large transient current during the switching transient until the power supply capacitors start supplying the current. The design recommends a 0.1-µF high frequency noise decoupling capacitor on the V_{CC2} pin.

4.2.2 Gate Resistor Selection

When designing gate drivers, selecting the right gate resistor is an important part of the process. The value of the gate resistor affects the following parameters:

- IGBT turn-on and turn-off times
- Switching losses
- dv/dt across the IGBT collector to emitter
- di/dt of the IGBT current
- EMI due to IGBT switching

Increasing the value of the gate resistor increases the turn-on and turn-off times of the IGBT, which in turn reduces the dv/dt and di/dt, causing reduced EMI. Higher gate resistance also increases switching losses. Decreasing the gate resistance reduces switching losses but increases EMI.

4.2.2.1 Gate Resistor Calculation

In this TI design the gate resistors selected provide a maximum gate source current of 2.5 A_{pk} and a maximum sink current of 5 A_{pk}. The source and sink currents are controlled independently using the gate drive circuit.

図 13 shows the simplified model of the IGBT gate capacitance charging phase:

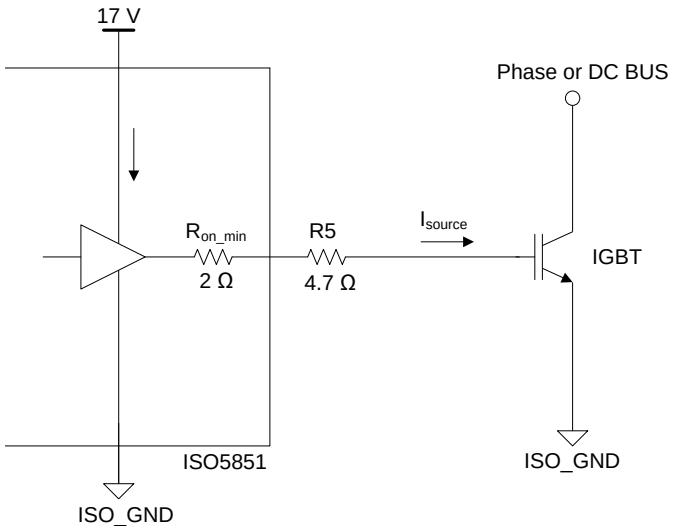


図 13. Simplified Output Model During the IGBT Turn-on Phase

式 9 calculates the gate resistance required to maintain a peak turn-on current of 2.5 A.

$$R_{g\_on} = r_{on\_min} + R5 = \frac{V}{I_{peak\_on}} = \frac{17\ V}{2.5\ A} = 6.8\ \Omega \quad (9)$$

$$R5 = 6.8\ \Omega - 2\ \Omega = 4.8\ \Omega \quad (10)$$

Select R5 = 4.7

- Rg_{on} is the gate resistance during IGBT switch ON phase
- V is the voltage applied to the gate of the IGBT
- I_{peak_on} is the peak current during turn ON
- r_{on_min} is the minimum internal on resistance of the gate driver

図 14 shows the simplified model of the IGBT gate capacitor discharging phase:

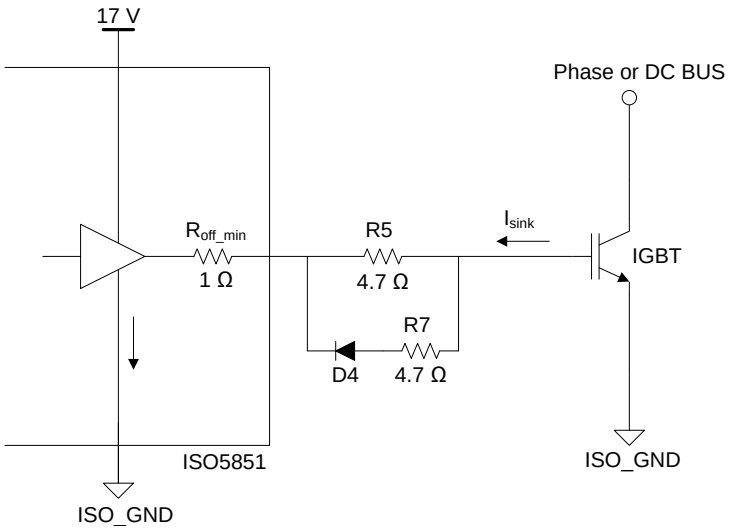


図 14. Simplified Output Model During the IGBT Turnoff Phase

式 11 calculates the gate resistance required to maintain a peak turn-off current of 5 A

$$R_{g\_off} = r_{off\_min} + R5 \,||\, R7 = \frac{V}{I_{peak\_off}} = \frac{17\ V}{5\ A} = 3.4\ \Omega \quad (11)$$

$$R5 \,||\, R7 = 3.4\ \Omega - 1\ \Omega = 2.4\ \Omega \Rightarrow R7 = 4.9\ \Omega \quad (12)$$

Select R7 = 4.7 Ω

- Rg_{off} is the gate resistance during IGBT switch off phase
- V is the voltage applied to the gate of the IGBT
- I_{peak_off} is the peak current during turn off
- r_{off_min} is the minimum internal off resistance of the gate driver

4.2.2.2 Gate Resistor Dimensioning

式 13 calculates the approximate power required to drive an IGBT gate:

$$P_g = Q_g \times V_g \times f_{SW} \quad (13)$$

- P_g is the gate power required
- Q_g is the gate charge required.
- Q_g can be found from the typical gate charge curve of an IGBT module or if the gate charge curve is not provided in the datasheet, approximately calculate Q_g by multiplying the gate capacitance by the gate voltage swing.
- F_{sw} is the gate switching frequency

This design uses a 100-nF capacitor to simulate the gate emitter capacitance of the IGBT.

式 14 calculates the gate charge.

$$Q_g = C_g \times V_g = 100\,nF \times 17\ V = 1.7\,\mu C \quad (14)$$

式 15 calculates power dissipated:

$$P_g = Q_g \times V \times f_{SW} = 1.7\,\mu C \times 17 \times 16\,kHz = 0.4624\ W \quad (15)$$

Assuming symmetrical on and off loses,

- Turn-on gate power = 0.2312 W
- Turn-off gate power = 0.2312 W

Referring 図 13, calculate the wattage of R5 during turn-on by 式 16:

$$P_{R5\_on} = \text{Turn on gate power} \times \frac{R5}{R5 + r_{on\_min}} = 0.2312 \times \frac{4.7}{4.7 + 2} = 0.1622\ W \quad (16)$$

$$P_{R5\_on\_peak} = I_{source}{}^2 R5 = 2.46^2 \times 4.7 = 28.44 \quad (17)$$

- P_{R5_on} is the average power dissipated in R5 during IGBT turn-on
- $P_{R5\_on\_peak}$ is the peak pulse power dissipated in R5 during IGBT turn-on

Referring 図 14, calculate the wattage of R5 and R7 during turnoff by 式 18, 式 19, 式 21 and 式 23

$$P_{R5\_off+R7\_off} = \text{Turn off gate power} \times \frac{R5 \,||\, R7}{(R5 \,||\, R7) + r_{off\_min}} = 0.2312 \times \frac{2.35}{2.35 + 1} = 0.1622\,W \quad (18)$$

$$P_{R5\_off} = \frac{P_{R5\_off+R7\_off}}{2} = 0.081\ W \quad (19)$$

$$P_{R5\_off\_peak} = I_{sink}{}^2 R5 = 2.46^2 \times 4.7 = 28.44 \quad (20)$$

P_{R5_off} is the average power dissipated in R5 during IGBT turnoff

$P_{R5\_off\_peak}$ is the peak pulse power dissipated in R5 during IGBT turnoff

$$P_{R7\_off} = \frac{P_{R5\_off+R7\_off}}{2} = 0.081\ W \quad (21)$$

$$P_{R7\_off\_peak} = I_{sink}{}^2 R7 = 2.46^2 \times 4.7 = 28.44\ W \quad (22)$$

$$P_{R5} = P_{R5\_on} + P_{R5\_off} = 0.1622\ W + 0.081\ W = 0.2432\ W \quad (23)$$

$$P_{R5\_peak} = P_{R5\_on\_peak} + P_{R5\_off\_peak} = 28.44\ W + 28.44\ W = 56.88\ W \quad (24)$$

The selected resistors must have the capability to handle the average power and the high peak pulse power as calculated in 式 22 and 式 24.

Select R5 = 4.7 Ω , 0.333 W, 1206 package. Select RPC1206JT4R670.

Select R7 = 4.7 Ω , 0.25 W, 0805 package. Select RPC0805JT4R70.

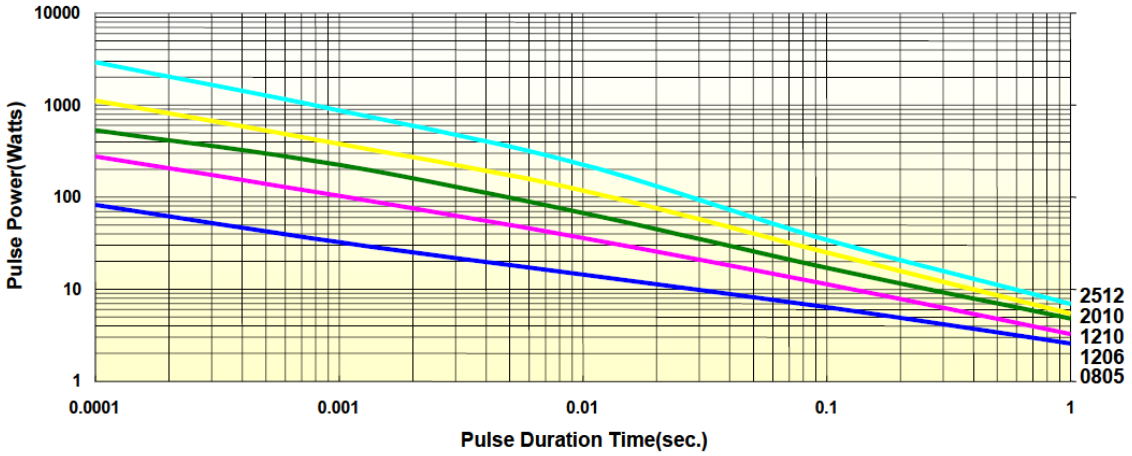


図 15. Peak Power Versus Duration of Power Pulse of Selected Resistors

図 15 presents that the 0805 package has a peak power rating of 90 W and the 1206 package has a peak power rating of 300 W for a 100-µs pulse. The continuous pulse load graph in 図 15 is obtained by applying repetitive rectangular pulses where the pulse period is adjusted so that the average power dissipated in the resistor is equal to its rated power at 70°C. 式 26 infers the maximum allowed frequency of operation.

$$P_{avg} = P_{peak} \times \text{duty cycle} = P_{peak} \times t_{pulse\,width} \times f_{SW} \quad (25)$$

$$f_{SW} = \frac{P_{avg}}{\left(P_{peak} \times t_{pulse\,width}\right)} \quad (26)$$

- P_{avg} is the rated power of the resistor
- P_{peak} is the peak pulse power dissipated in the resistor
- $t_{pulsewidth}$ is the width of the applied pulse
- f_{sw} is the frequency of operation that is the frequency at which the pulses are repeated

図 16 shows the exponential nature of peak power waveforms for gate drive signals. The exponential waveforms are converted into equivalent rectangular pulses, the width of which is equal to half of RC time constant of the exponential waveform. The gate resistor and the gate capacitance determines the RC time constant of the waveform.

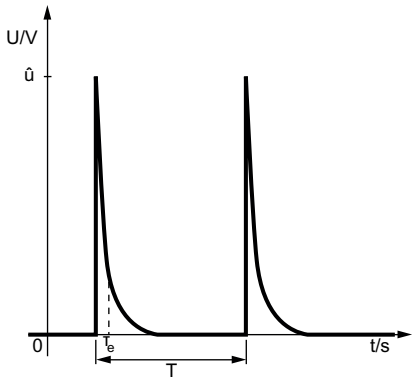


図 16. Exponential Nature of Peak Pulse Power Waveforms

$$\frac{1}{2}\tau_e = \frac{1}{2}RC = \frac{1}{2} \times 4.7\,\Omega \times 0.1\,\mu F = 0.235\,\mu s \tag{27}$$

The pulse width of the equivalent rectangular pulse with amplitude equal to the peak pulse power is 0.235 µs, which has the same power content as the exponential pulse. The 図 15 values are comparable using this parameter.

For resistor R5 from 図 15, 300 W is the peak pulse power at 100 µs pulse width, assuming a minimum of 300 W peak pulse power for 0.235 µs.

$$f_{SW} = \frac{0.33\,W}{(300\,W \times 0.235\,\mu s)} = 4.68\,kHz \tag{28}$$

Resistor R5 can dissipate 300 W pulses of width 0.235 µs at 4.68 kHz. 式 29 calculates the maximum frequency of operation from 56.88 W pulses of the same width.

$$f_{SW} = \frac{0.33\,W}{(56.88\,W \times 0.235\,\mu s)} = 24.68\,kHz \tag{29}$$

The selected resistor is suitable for operation at 16 kHz.

Similarly for R7 from 図 15, 90 W is the peak pulse power at 100 µs pulse width, assuming a minimum of 90 W peak pulse power for 0.235 µs.

$$f_{SW} = \frac{0.25\,W}{(90\,W \times 0.235\,\mu s)} = 11.82\,kHz \tag{30}$$

Resistor R7 can dissipate 90 W pulses of width 0.235 µs at 11.82 kHz. 式 31 calculates the maximum frequency of operation for 28.44 W pulses of the same width.

$$f_{SW} = \frac{0.25\,W}{(28.44\,W \times 0.235\,\mu s)} = 37.40\,kHz \tag{31}$$

The selected resistor is suitable for operation at 16 kHz.

4.2.3 Desaturation Detection Circuit

Desaturation detection technique is a widely used method to detect short circuit conditions in IGBT. A desaturation condition occurs if the IGBT collector emitter voltage rises above 8 V when the IGBT is in the ON condition. ISO5851 detects this desaturation condition and turns off the IGBT switch.

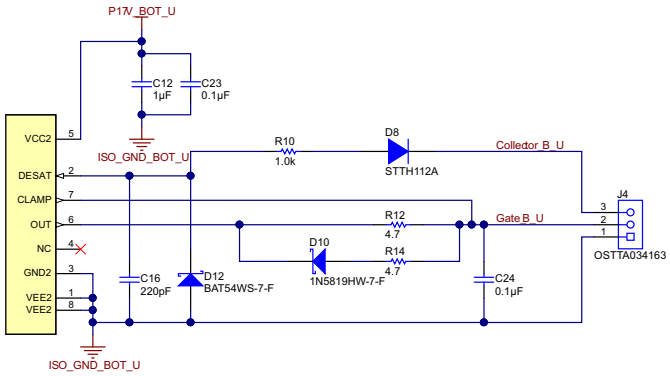


図 17. DESAT Desaturation Circuit

図 17 shows the components D8, R10, C16 and D12, which are part of the desaturation detection circuit. The DESAT diode D8 conducts forward current, which allows sensing of the IGBT's saturated collector to emitter voltage when the IGBT is in the on condition. D8 blocks high voltage when the IGBT is in the OFF condition. In this design, D8 blocks a maximum of 1200 V during the IGBT OFF condition. A 220 pF blanking capacitor C16 is required, which disables the DESAT detection during the off-to-on transition of the power device. 式 32 calculates the blanking time.

$$t_{blank} = \frac{C_{blank} \times V_{DSTH}}{I_{CHG}} = \frac{220\,pF \times 9\,V}{0.5\,mA} = 3.96\,\mu s \tag{32}$$

During the transition time, when the IGBT is changing state, a high dVCE/dt voltage ramp rate occurs across the IGBT. 式 33 calculates the resultant charging current.

$$I_{charge} = C_{D\_DESAT} \times \frac{dV_{CE}}{dt} \tag{33}$$

C_{DDESAT} is the diode capacitance at DESAT. This current charges the blanking capacitor C16. The diode capacitance C_{DDESAT}, along with C16, forms the voltage divider network. This voltage divider network results in IGBT collector voltage transients appearing at the DESAT pin attenuated by the ratio determined by 式 34.

$$V_{DESAT\_transient} = \frac{V_{CE}}{\left(1 + \frac{C16}{C_{D\_DESAT}}\right)} \tag{34}$$

To avoid false DESAT triggering, fast recovery diodes with low capacitance are used. STTH112A is selected in this design. The STTH112A is a 1 A, 1200 VRRM diode with a reverse recovery time of 75 ns. The blanking capacitor chosen must have a large value, as a small value will lead to high transient voltage on the DESAT pin. The voltage at the DESAT pin equals the sum of the forward voltage drop of D8 and the IGBT collector to emitter voltage. 式 35 calculates the V_{CE} level that triggers a fault condition.

$$V_{CE\_FAULT(TH)} = 9 - V_f = 9 - 1.5 = 7.5\,V \tag{35}$$

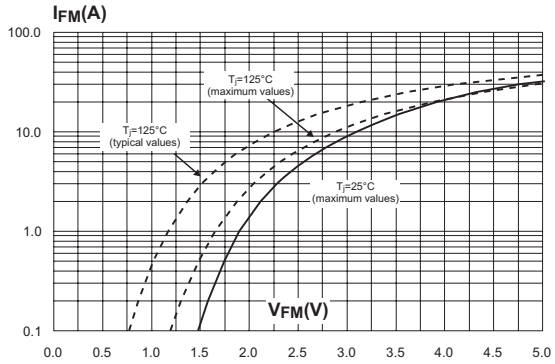


図 18. Forward Current Versus Forward Voltage Drop for STTH112A

A 1 kΩ resistor must be placed in series with the DESAT diode D8. This limits the current during transient conditions. A Schottky diode, connected between the DESAT pin and secondary ground, provides additional protection against negative voltage transients on the isolated ground pin. This ensures clamping of DESAT input (< GND2 – 0.3 V = –0.3 V) to secondary ground during transients.

4.2.4 Miller Clamp Circuit

The collector transient voltage can get coupled to the gate of the IGBT through the parasitic Miller capacitance, leading to false turn on of the IGBT if no negative voltage is applied to the gate. Using an active Miller clamp integrated into the ISO5851 resolves this issue. The Miller clamp provides a low impedance path to ground. The integrated Miller clamp activates when the IGBT is turned off and the gate voltage transitions below 2 V.

A Miller clamp in the gate driver allows the use of a unipolar gate drive supply instead of a bipolar gate drive supply, thus simplifying the power supply design, causing a lower size solution at a reduced cost and smaller board size.

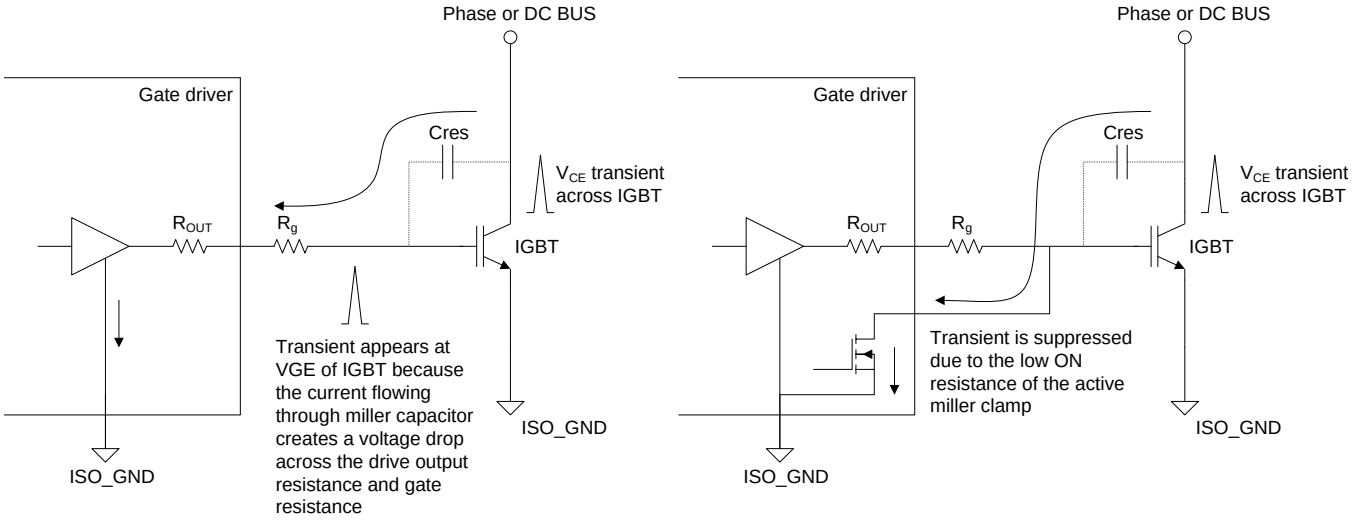


図 19. With and Without Miller Clamp

For the Miller clamp to be effective, the induced current must be less than the Miller clamps current sinking capability. 式 36 calculates the induced current:

$$i = C_{res} \times \frac{dV_{CE}}{dt} \quad (36)$$

- Where C_{res} is the reverse transfer capacitance of the IGBT
- dV_{CE}/dt is the rate of change of voltage across the IGBT collector to emitter

4.2.5 Fault and Ready Pin Circuit

The fault pin notifies the controller that the IGBT has gone into active region due to short circuit. Whenever desaturation of IGBT is detected the fault pin goes low. The fault pin is an active low open drain output and requires a pullup resistor connected to a 3.3 V rail. The six fault pins of six gate drivers are connected together and pulled up to 3.3 V, resulting in the logical ANDing of all the fault pins.

The ready pin indicates the status of the primary and secondary side power supplies. If either side of the device has insufficient supply voltage, lesser than the UV threshold, the ready pin will activate. The ready signal indicates whether the device is ready or not, and is an active logic high signal. The six ready pins of six gate drivers are connected together and pulled up to 3.3 V, resulting in the logical ANDing of all the ready pins.

4.2.6 Shutdown and Reset Circuit

Reset is an active low signal which is used to restart the ISO5851 gate driver after a fault has occurred. Applying a minimum 800 ns low pulse on this pin restarts the gate driver from the locked out condition. The reset pin also has internal filters to reject noise and glitches which can otherwise erroneously enable the gate drivers.

All the gate driver reset pins are connected together and driven by a single controller pin.

4.2.7 Control Inputs

The ISO5851 device has two control inputs: the non-inverting and inverting input. The inverting input connects to primary ground and the non-inverting input connects to the microcontroller. Use low-impedance signal sources to avoid unwanted switching of the ISO5851 driver under extreme common-mode transient conditions. Therefore, the control input must be driven by standard CMOS push-pull drivers; avoid passive circuits like open-drain configurations using pull-up resistors. Glitches up to 20 ns on the control inputs are filtered by an on-chip glitch filter.

4.2.8 Dynamic Output Power

The maximum allowed total dynamic power consumption P_D for ISO5851 is 700 mW at 85°C. This includes the input quiescent power P_{ID}, the output quiescent power P_{OD}, and the output power under load P_{OL}.

$$P_D = P_{ID} + P_{OD} + P_{OL} \quad (37)$$

$$P_{ID} = V_{CC1\_max} \times I_{CC1\_max} = 5.25\,V \times 4.5\,mA = 23.63\,mW \quad (38)$$

- V_{CC1_max} is the maximum primary side input power supply voltage
- I_{CC1max} is the maximum primary side input quiescent current

$$P_{OD} = \left(V_{CC2} - V_{EE2}\right) \times I_{CC2\_max} = \left(16.5\,V - 0\,V\right) \times 6\,mA = 99\,mW \quad (39)$$

- V_{CC2_max} is the maximum secondary side input power supply voltage
- I_{CC2_max} is the maximum secondary side input quiescent current

式 40 calculates the power dissipation budget available for the ISO5851 device under load.

$$P_{OL} = P_D - P_{ID} - P_{OD} = 700\,mW - 23.63\,mW - 99\,mW = 577.37\,mW \quad (40)$$

式 41 calculates the worst case actual power loss under load.

$$P_{OL\_WC} = 0.5 \times f_{INP} \times Q_g \times \left(V_{CC2} - V_{EE2}\right) \times \left(\frac{r_{on\_max}}{r_{on\_max} + R_{g\_on}} + \frac{r_{off\_max}}{r_{off\_max} + R_{g\_off}} \right) \quad (41)$$

Where:

- f_{INP} is the signal frequency at the control input
- Q_g is the gate charge of IGBTVCC2 is the positive output supply with respect to secondary ground
- V_{EE2} is the negative output supply with respect to secondary ground
- r_{on_max} is the worst case output resistance of the internal switch in the on-state
- r_{off_max} is the worst case output resistance of the internal switch in the off-state
- R_{gon} is the external gate resistance during the switch on phase
- R_{goff} is the external gate resistance during the switch off phase

Verify from 式 40 and 式 41 that POL – WC < POL

4.3 5- to 3.3-V Regulator

表 6 provides the specifications of the 5- to 3.3-V regulator:

表 6. 3.3-V Voltage Regulator Specifications

PARAMETER	SPECIFICATION
Input voltage	5 V ± 5 %
Output voltage	3.3 V ± 1 %
Output current	50 mA_{max}

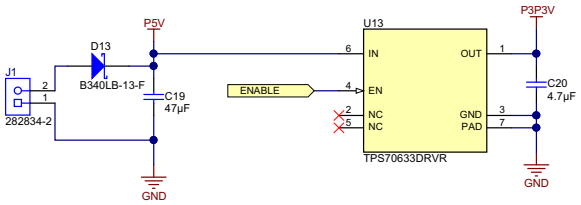


図 20. 5- to 3.3-V Regulator

The maximum load current drawn from the 5 V input supply follows:

- 50 mA into the 3.3-V regulator
- 1.32 A into the six SN6505B driver ICs when the power supplies are fully loaded.

To protect against input reverse polarity, use a D13 Schottky. The Schottky diode B340LB-13-F has a forward voltage drop of 0.3 V maximum at 25°C ambient and decreases with temperature increases. Place a 47 µF bulk capacitor C19 on the power entry point of the board for clean power supply.

Powering the primary side of the isolated gate drivers requires a 3.3 V rail. Where a 3.3-V rail is present on motor drive boards, the LDO can be skipped. In this TI design board, 3.3 V is generated from a 5 V supply using TPS70633. The device has an accuracy of ±1%

For the 3.3 V output of TPS70633 to be stable a low equivalent series resistance (ESR) bulk capacitor C20 must be used. The effective capacitance of C20 must be greater than 1.5 µF and less than 47 µF. Effective capacitance is the minimum capacitance of C20 after considering variations resulting from tolerances, temperature, and DC bias effects. This design uses 4.7 µF. The ESR of C20 should range between 0 Ω and 0.2 Ω for stability.

式 42 calculates the maximum power loss in TPS70633.

$$P_D = \left(V_{IN\_max} - V_{OUT\_min}\right) \times I_{Load} = \left(5.25\,V - 3.23\,V\right) \times 50\,mA = 100\,mW \quad (42)$$

Maximum operating junction temperature of TPS70633 is 125°C. Maximum operating ambient temperature is 85°C. 式 43 calculates the junction temperature rise due to 100 mW power dissipation.

$$\text{Junction temperature rise} = P_D \times R_{\theta JA} = 100\,mW \times 73.1\frac{°C}{W} = 7.31°C \quad (43)$$

$$\text{Junction temperature} = \text{Maximum ambient temperature} + \text{junction temperature rise} = 85°C + 7.31°C = 92.31°C \quad (44)$$

Junction temperature of 92.31°C is safely below the 125°C operating limit.

The ENABLE signal connected to this device provides the option to shutdown the primary side power supply in case of safe torque off event.

4.4 3.3- to 5-V Logic Level Translator

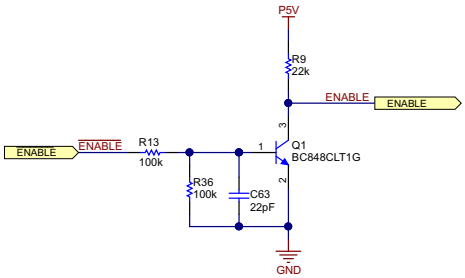


図 21. 3.3- to 5-V Logic Level Translator

A 5-V supply powers SN6505B and a 3.3-V microcontroller drives the enable signal. A level translator is required to make the output logic levels of the microcontroller compatible with the input logic levels of 5-V powered SN6505B. The level translator is designed based on a transistor switch. BC848CL is selected for its low cost and high gain, hFE = 520.

$$I_{Csat} = \frac{V_{IN} - V_{CEsat}}{R9} = \frac{5\,V - 0.25\,V}{22\,k\Omega} = 0.22\,mA \quad (45)$$

- I_{Csat} is collector current during BJT saturation
- V_{CEsat} is the BJT collector emitter voltage during saturation

$$I_{B\_EOS} = \frac{I_{Csat}}{h_{FE\_min}} = \frac{0.22\,mA}{420} = 0.52\,\mu A \quad (46)$$

- EOS is edge of saturation
- h_{FEmin} is minimum DC current gain
- Overdrive factor, ODF, = 10

$$I_B = ODF \times I_{B\_EOS} = 10 \times 0.52\,\mu A = 5.2\,\mu A \quad (47)$$

IB is the BJT base current

$$R13 = \frac{V_{EN} - V_{BE}}{I_B} = \frac{3.3\,V - 0.7\,V}{5.2\,\mu A} = 500\,k\Omega \quad (48)$$

V_{BE} is the BJT base to emitter voltage

Select R13 = 100 kΩ

$$h_{FE\_forced} = \frac{I_{Csat}}{I_B} = \frac{0.22\,mA}{0.026\,mA} = 8.46 \quad (49)$$

For BJT to operate as switch, h_{FE_forced}less than h_{FEmin}. The condition is satisfied in the previous circuit.

As the level translator circuit also inverts the output, the ENABLE signal coming from the microcontroller must be an active low signal. The output of the level translator connects to the LDO U13, and to the enable pins of all the six SN6505B devices. When enable signal from the microcontroller is logic low, the transistor Q1 is turned off and the resistor R9 pulls up all the enable pins to logic high. When the ENABLE signal from the microcontroller is logic high, Q1 turns on and all the device enable pins are pulled logic low. This puts the board into a low-power shutdown state.

The ENABLE signal is used for the safe torque off (STO) function. STO function uses an emergency event to shutdown power to the motor while the drive is still connected to the mains power supply.

5 Test Data

5.1 Getting Started Hardware

5.1.1 Board Description

図 22 shows the size of the complete gate drive solution for six power switches of a three phase inverter and the size of individual gate driver section. A tiny size of 1.53 cm * 3.11 cm is achieved.

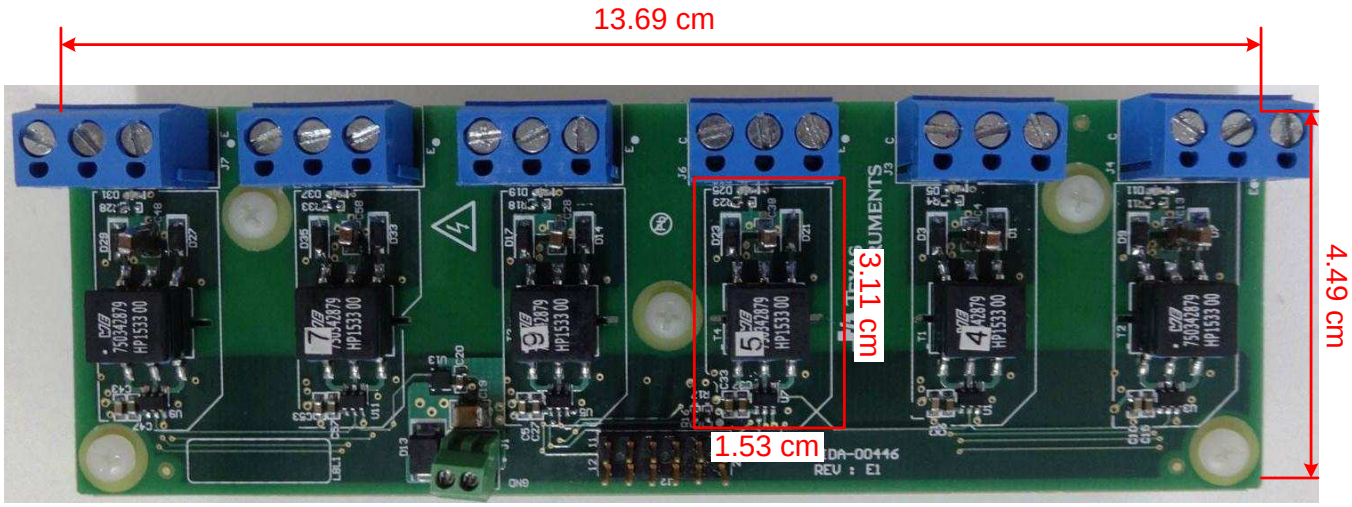


図 22. Complete PCB Board Size and Solution Size

図 23 and 図 24 show the location of the subsections in the block diagram (図 2) on the actual board. Observe that the isolated gate driver is placed directly underneath the isolated power supply section.

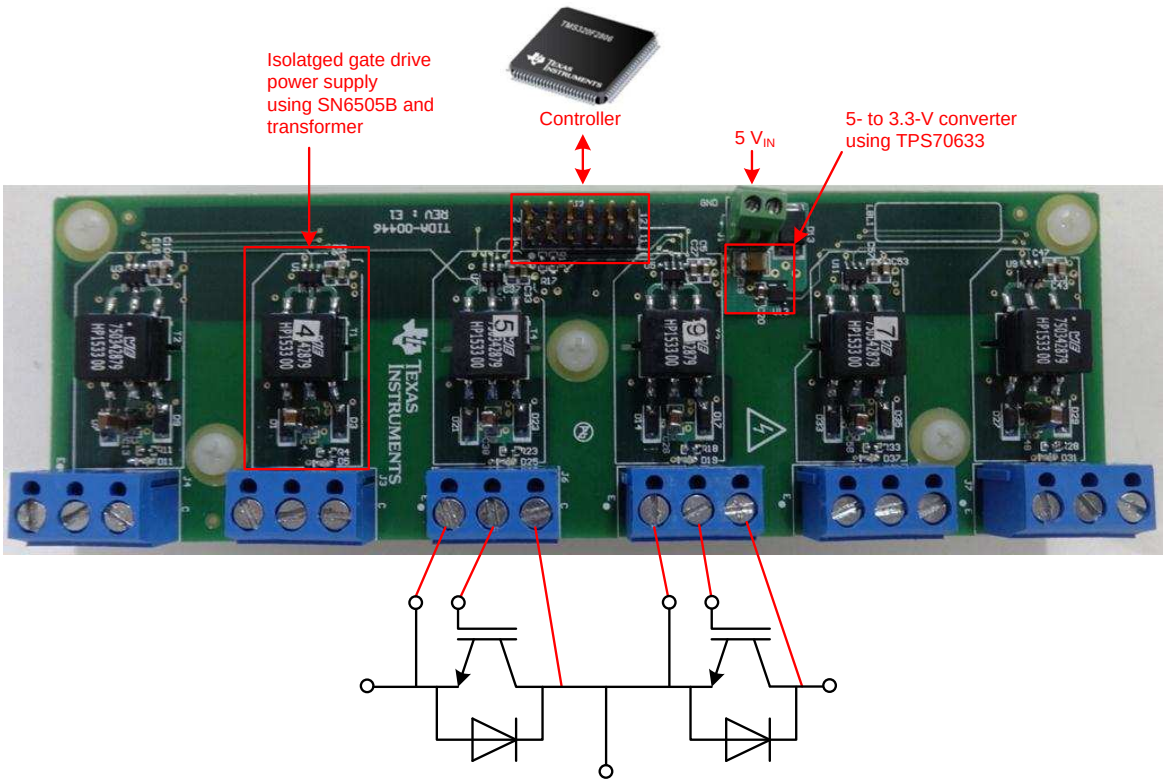


図 23. PCB Top Subsections

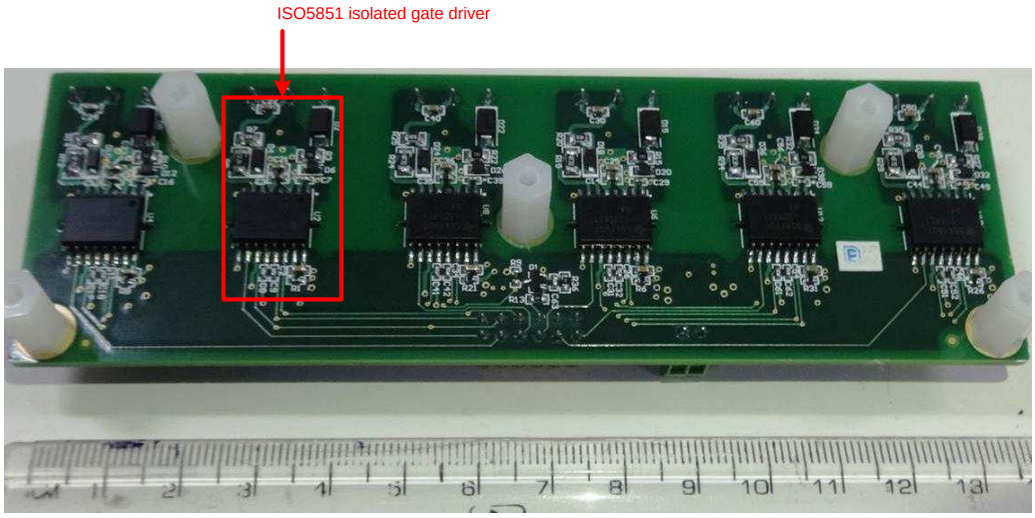


図 24. PCB Bottom Subsections

5.1.2 Connector Description

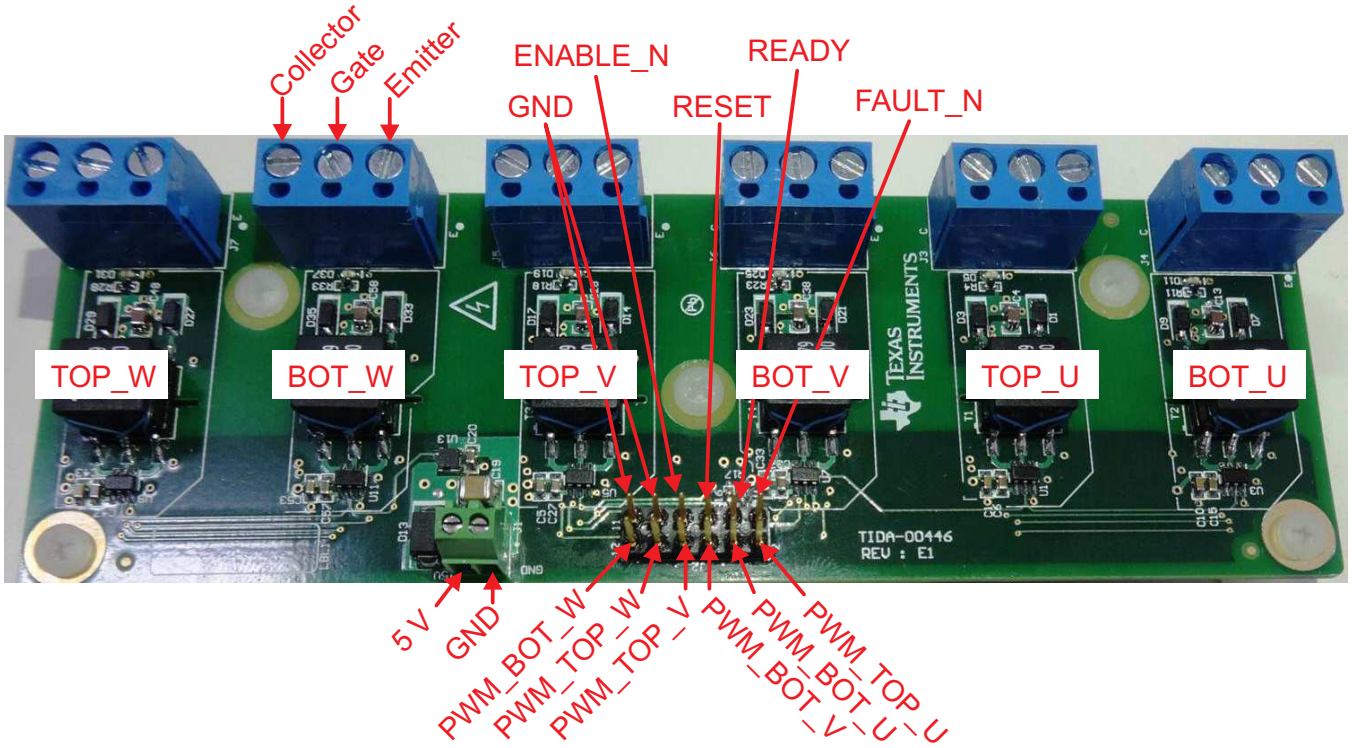


図 25. Connector Description

表 7. Connector Pin Description

PIN NUMBER	PIN NAME	I/O	DESCRIPTION
1	FAULT_N	O	Turns logic low if any one or more of the gate drivers detect desaturation of associated IGBT
2	PWM_TOP_U	I	PWM input to TOP_U section
3	READY	O	Logic high indicates that all the gate driver power supplies are good
4	PWM_BOT_U	I	PWM input to BOT_U section
5	RESET	I	Logic low pulse of 800 ns minimum to reset the fault latch
6	PWM_BOT_V	I	PWM input to BOT_V section
7	ENABLE_N	O	Used to enable/disable the power supplies. Logic high shuts down the supplies
8	PWM_TOP_V	I	PWM input to TOP_V section
9	GND		Primary ground
10	PWM_TOP_W	I	PWM input to TOP_W section
11	GND		Primary ground
12	PWM_BOT_W	I	PWM input to BOT_W section

5.2 Push-pull Power Supply

For all tests in 5.2.1 through 5.2.10, the polarity protection diode D13 is shorted and the gate driver section is not mounted.

5.2.1 Secondary Side Isolated Output Voltage Waveforms

The secondary side output voltage of the isolated power supply is measured at no load and full load . 図 28 to 図 30 show the ripple voltage on the output supply. The waveforms from 図 26 to 図 30 are for an output capacitor of 10 µF (effectively 1.8 µF considering the effect of DC bias).

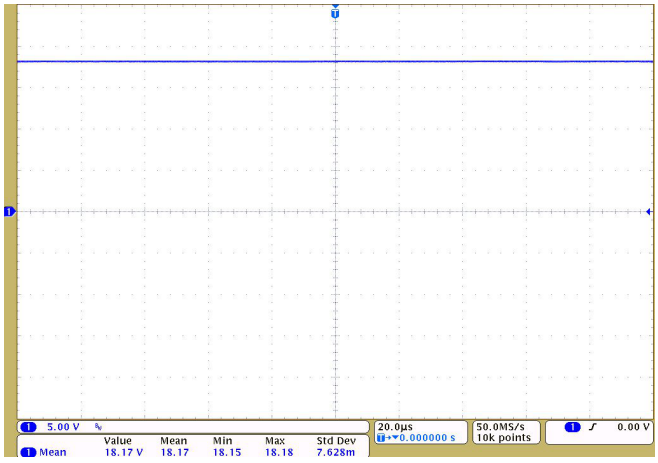


図 26. Output Voltage at no Load and Output Capacitor = 10 µF (18.17 V)

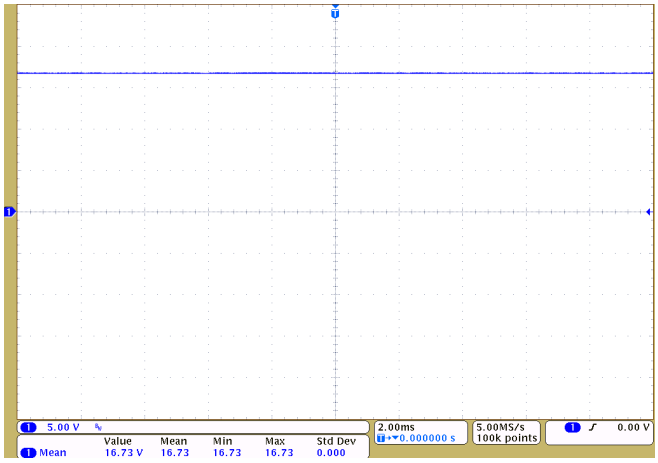


図 27. Output Voltage at Full Load and Output Capacitor = 10 µF (16.73 V)

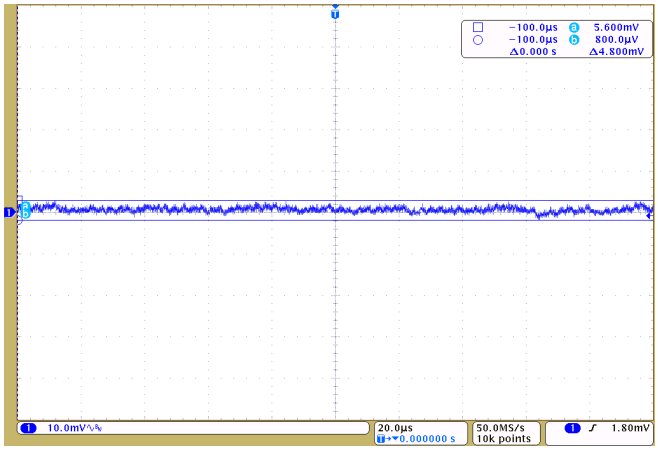


図 28. Output Voltage Ripple at no Load and Output Capacitor = 10 µF (4.8 mV)

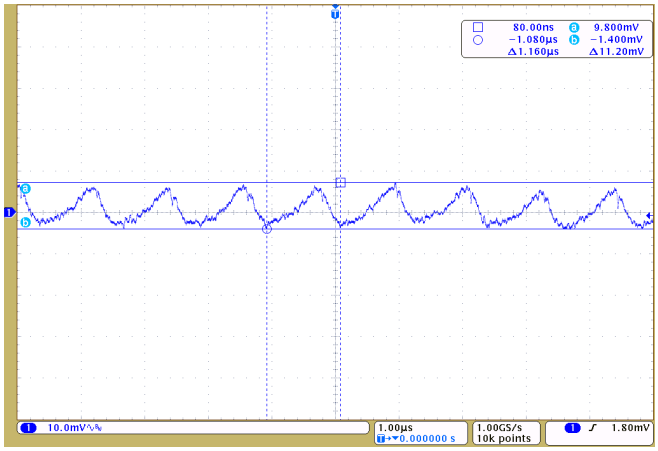


図 29. Output Voltage Ripple at Full Load and Output Capacitor = 10 µF (11.20 mV at 862 kHz)

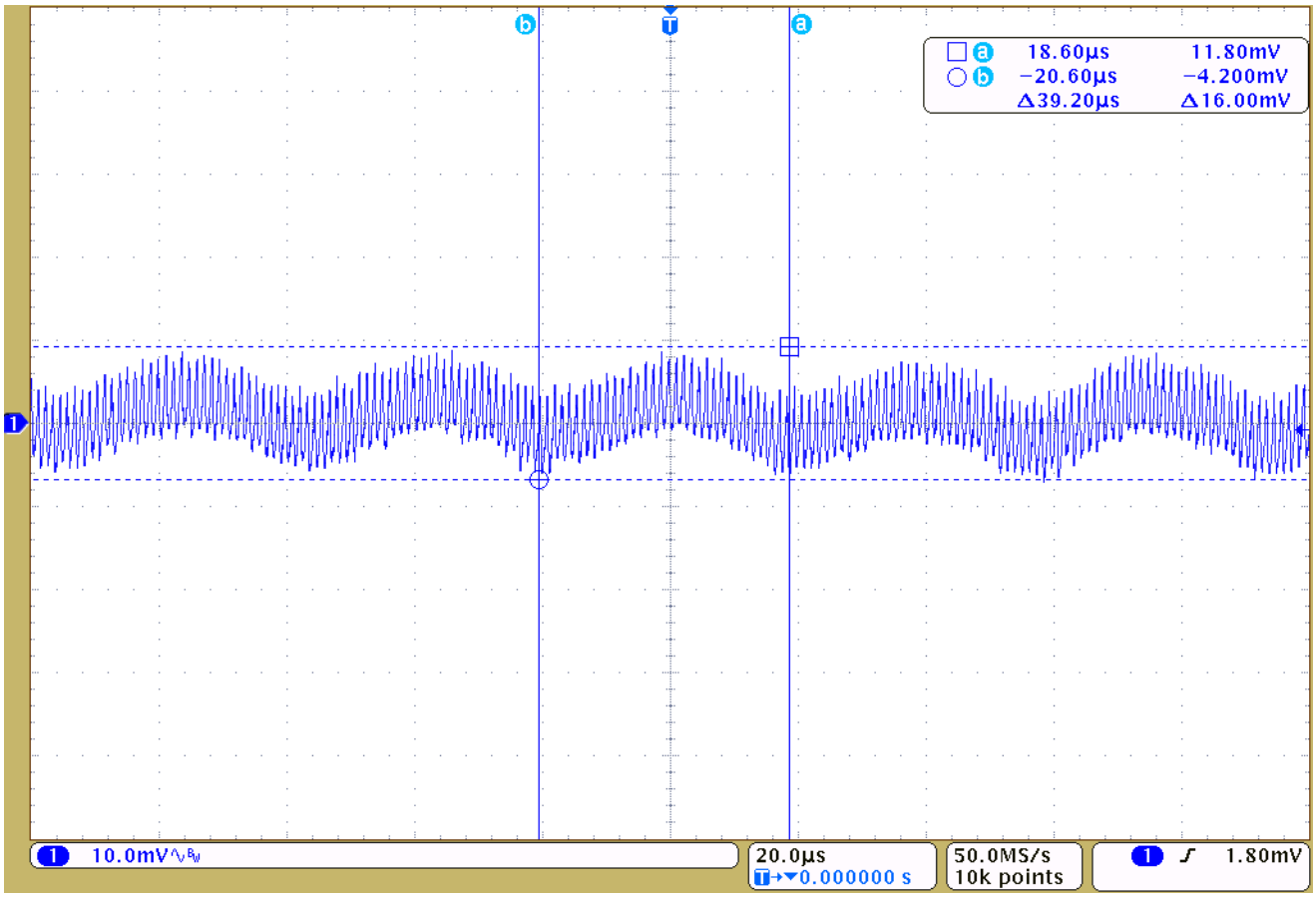


図 30. Low Frequency Output Voltage Ripple due to Spread Spectrum Modulation and Output Capacitor = 10 µF (16 mVpp at 25.51 kHz)

The same waveforms are measured again with an output capacitor of 20 µF (effectively 8.6 µf factoring DC bias). 図 31 to 図 35 show the waveforms. 図 36 shows the output voltage of the TPS70633 5 V to 3.3 V voltage regulator and 図 37 shows the ripple in 3.3 V. Scope noise limits the ripple voltage measurements in 図 33 to 図 35.

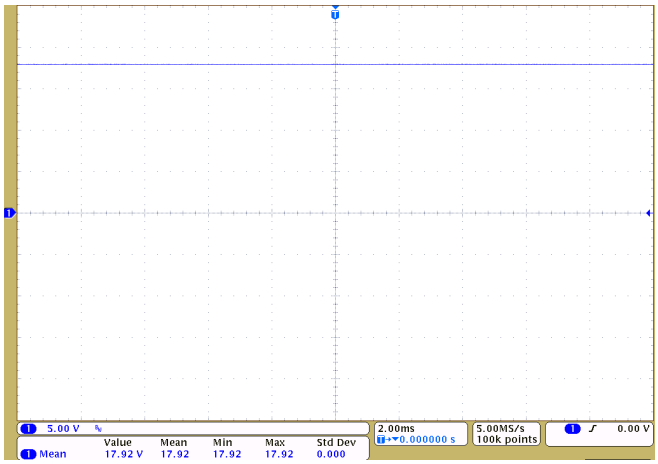


図 31. Output Voltage at No Load and Output Capacitor = 20 µF (17.92 V)

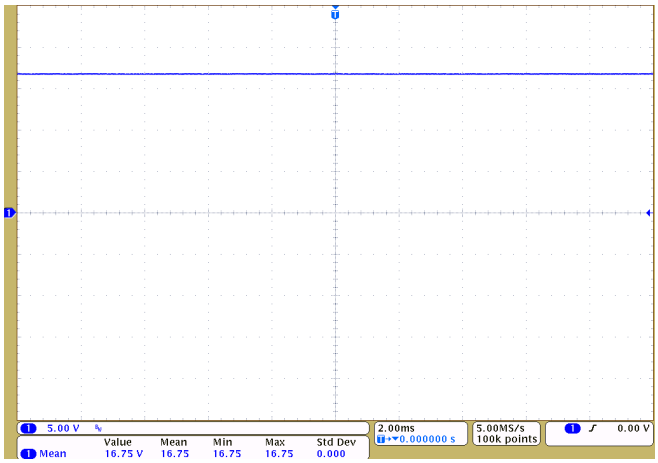


図 32. Output Voltage at Full Load and Output capacitor = 20 µF (16.75 V)

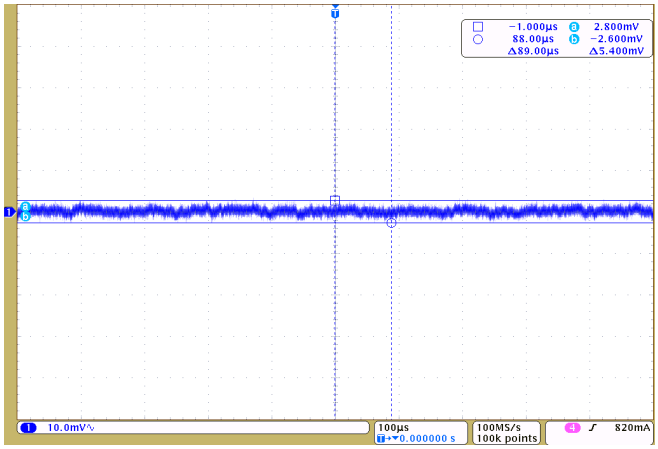


図 33. Output Voltage Ripple at No Load and Output Capacitor = 20 µF

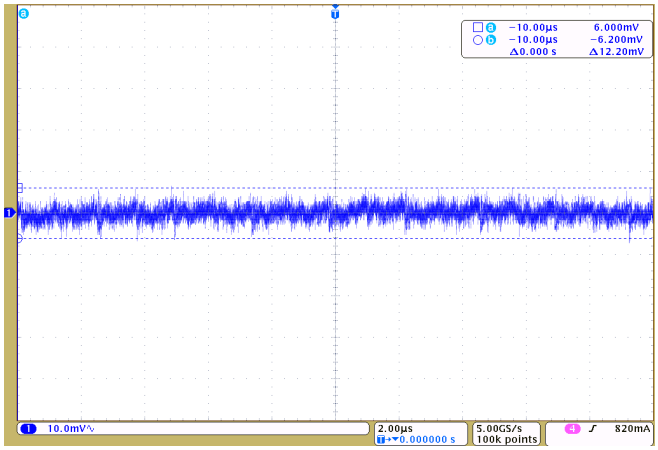


図 34. Output Voltage Ripple at Full Load and Output Capacitor = 20 µF

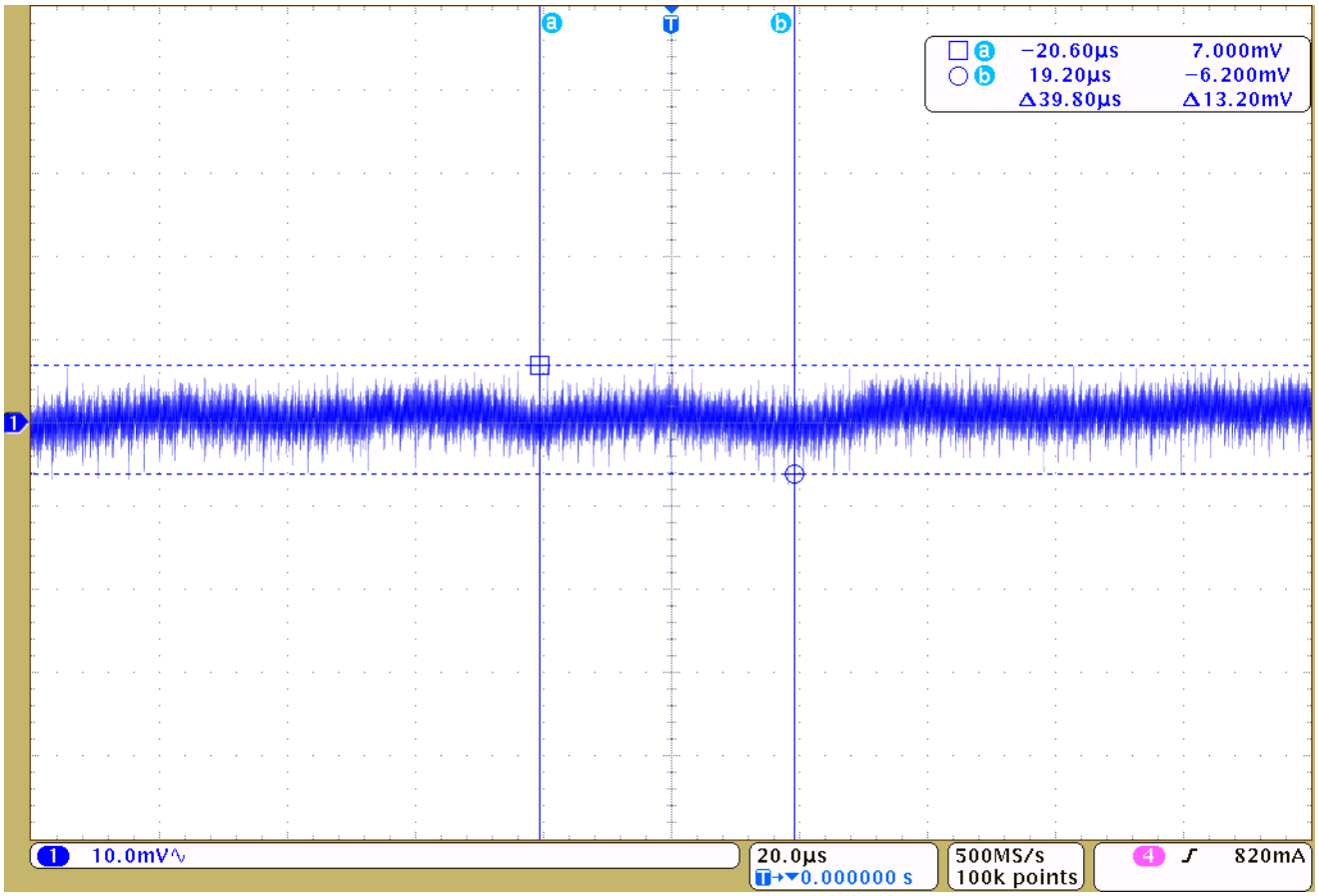


図 35. Low Frequency Output Voltage Ripple due to Spread Spectrum Modulation and Output Capacitor = 20 µF

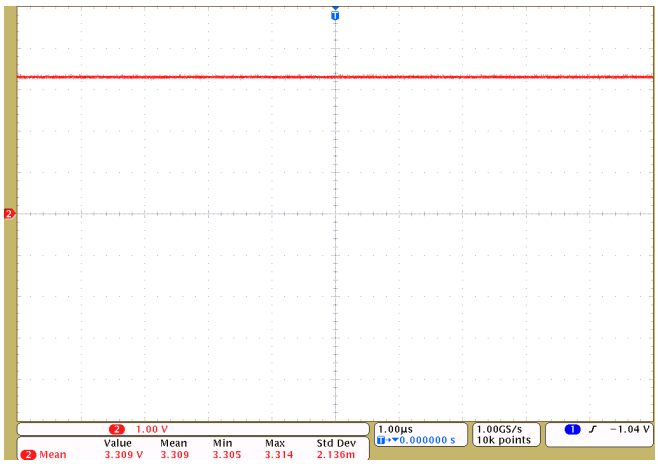


図 36. 3.3-V Output of TPS70633 (3.309 V)

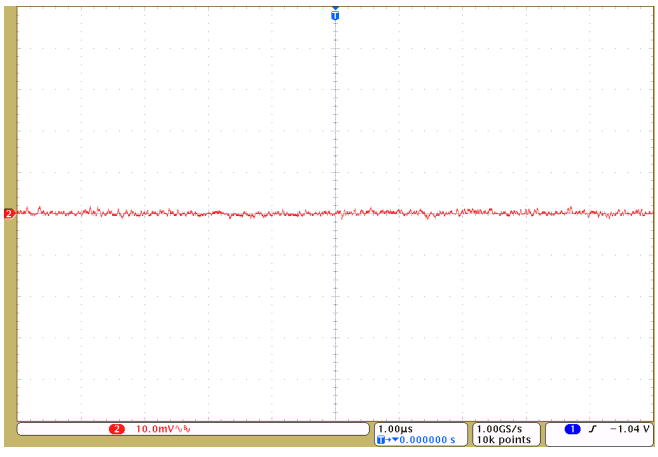


図 37. Ripple in 3.3-V Output of TPS70633

5.2.2 5-V Primary Side Input Voltage Waveforms

図 38 and 図 39 measure the primary side input voltage to the push-pull converter at no load and full load conditions. 図 40 and 図 41 measure the input voltage ripple due to push-pull transformer switching.

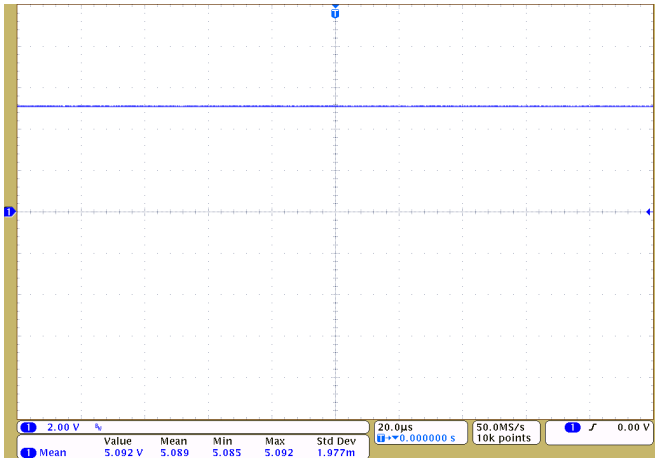


図 38. Input Voltage Waveform at no Load (5.09 V)

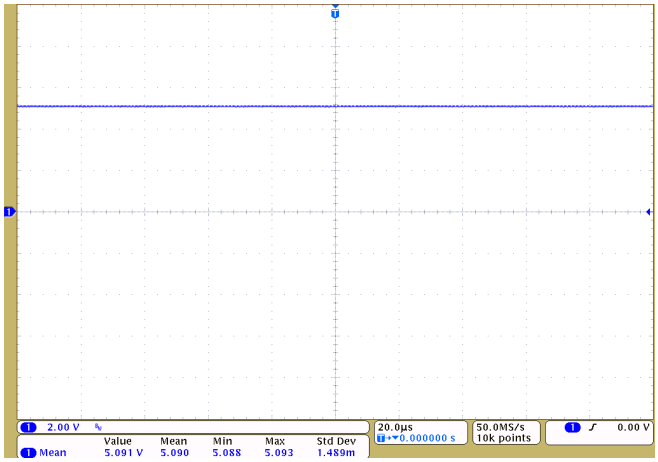


図 39. Input Voltage Waveform at Full Load (5.090 V)

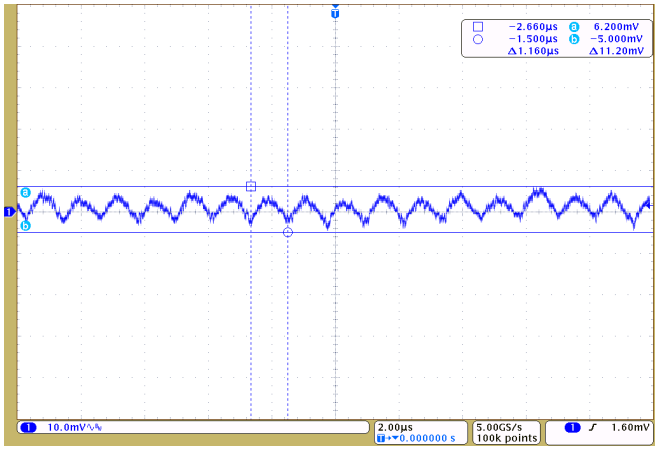


図 40. Input Voltage Ripple at no Load (11.2 mVpp at 862 kHz)

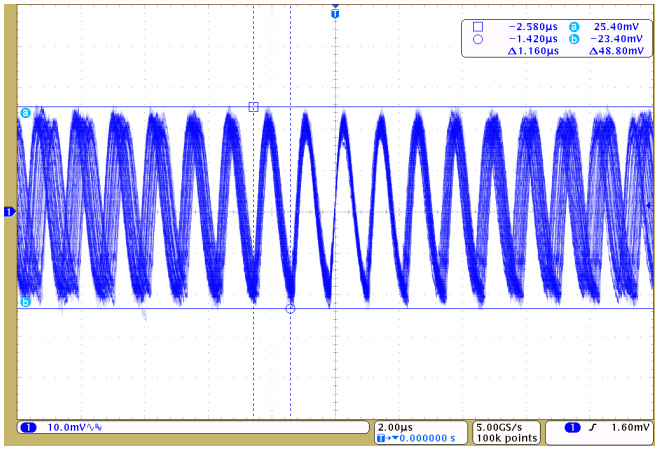


図 41. Input Voltage Ripple at Full Load Showing Spread Spectrum Switching (48.8 mVpp at 862 kHz)

5.2.3 Transformer Switching Waveforms

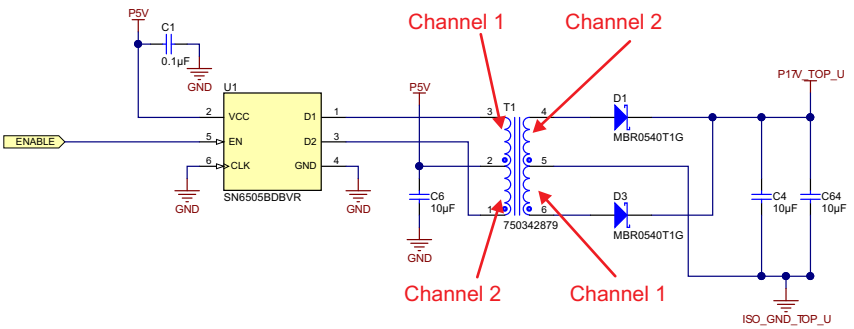


図 42. Push-pull Power Supply (Schematic)

図 43 to 図 47 show the switching voltages across the primary windings of the transformer with respect to the primary centertap at no load and full load conditions. Channel 1 is the voltage measured across pins 2 and 3 of the transformer and channel 2 is the voltage measured across pins 1 and 2.

図 48 to 図 52 show the switching voltages across the secondary windings of the transformer with respect to the secondary centertap at no load and full load conditions. Channel 1 is the voltage measured across pins 5 and 6 of the transformer and channel 2 is the voltage measured across pins 4 and 5.

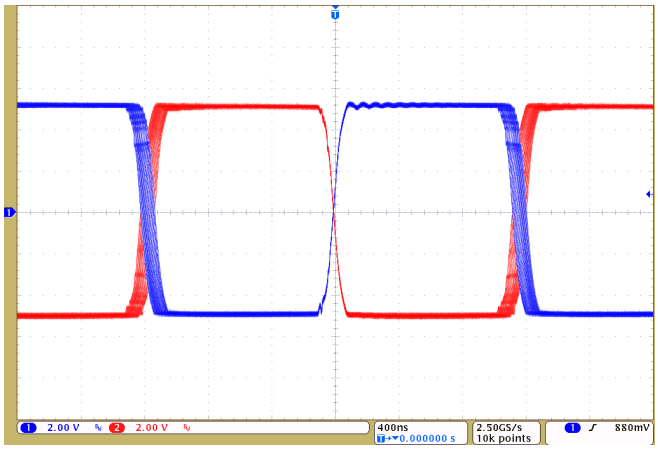


図 43. Primary Side Transformer Switching Waveform With Respect to Primary Centertap Showing Spread Spectrum Clocking at no Load

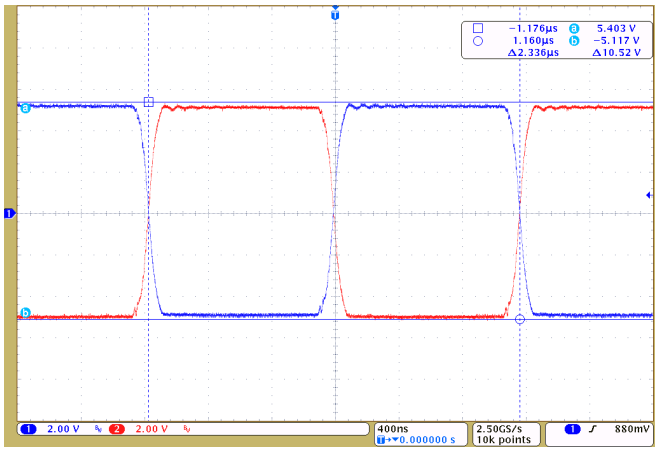


図 44. Primary Side Transformer Switching Waveform With Respect to Primary Centertap at no Load

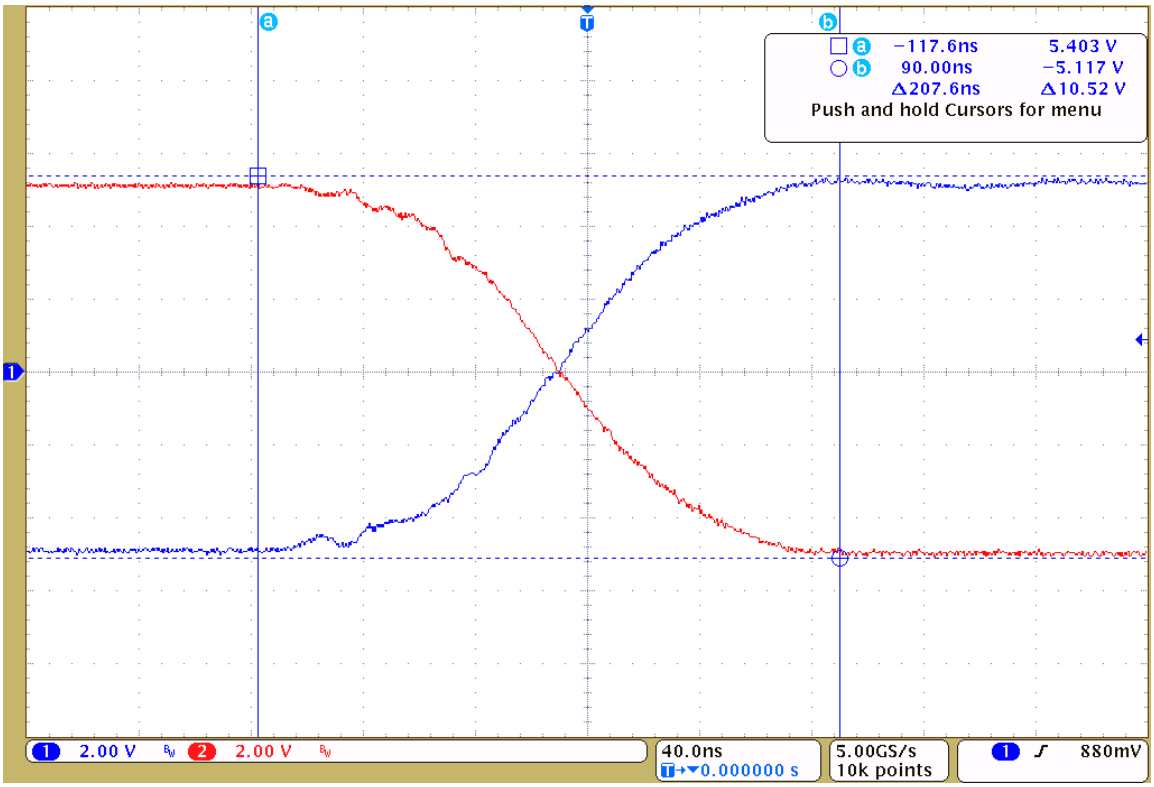


図 45. Zoomed in Version of 図 41 Showing Rise and Fall Times

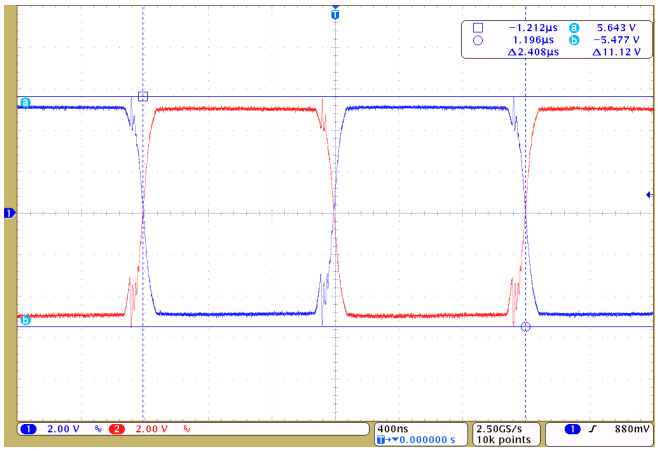


図 46. Primary Side Transformer Switching Waveform With Respect to Primary Centertap at Full Load

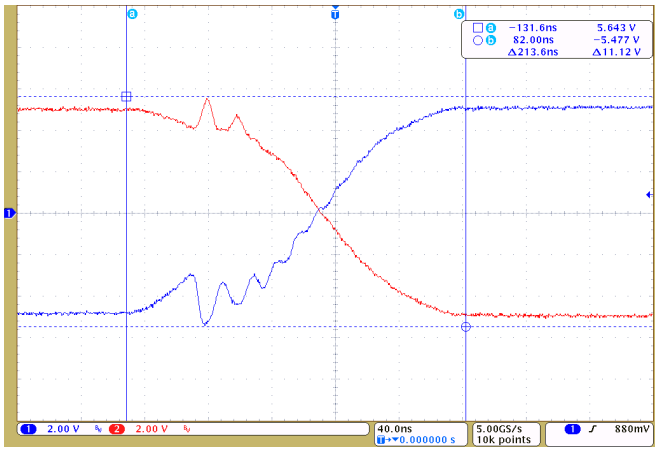


図 47. Zoomed in Version of 図 43 Showing Rise and Fall Times

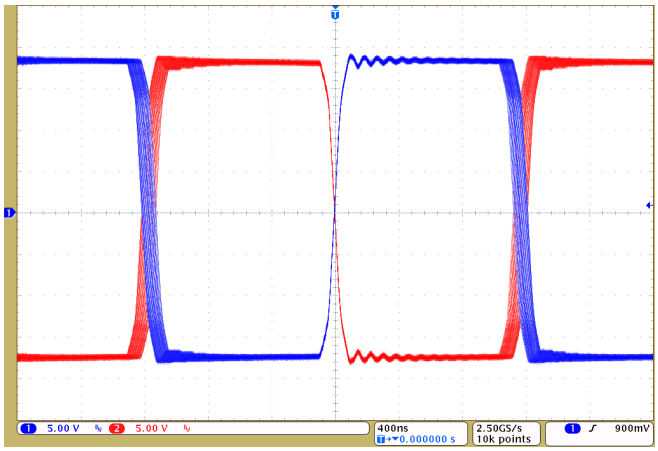


図 48. Secondary Side Transformer Switching Waveform With Respect to Secondary Centertap Showing Spread Spectrum Clocking at no Load

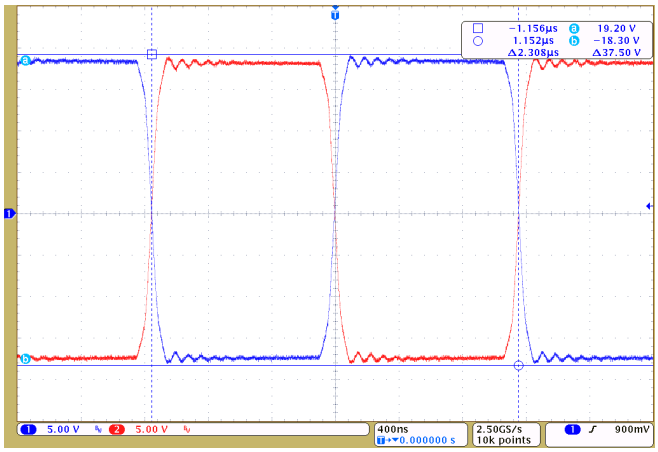


図 49. Secondary Side Transformer Switching Waveform With Respect to Secondary Centertap at no Load

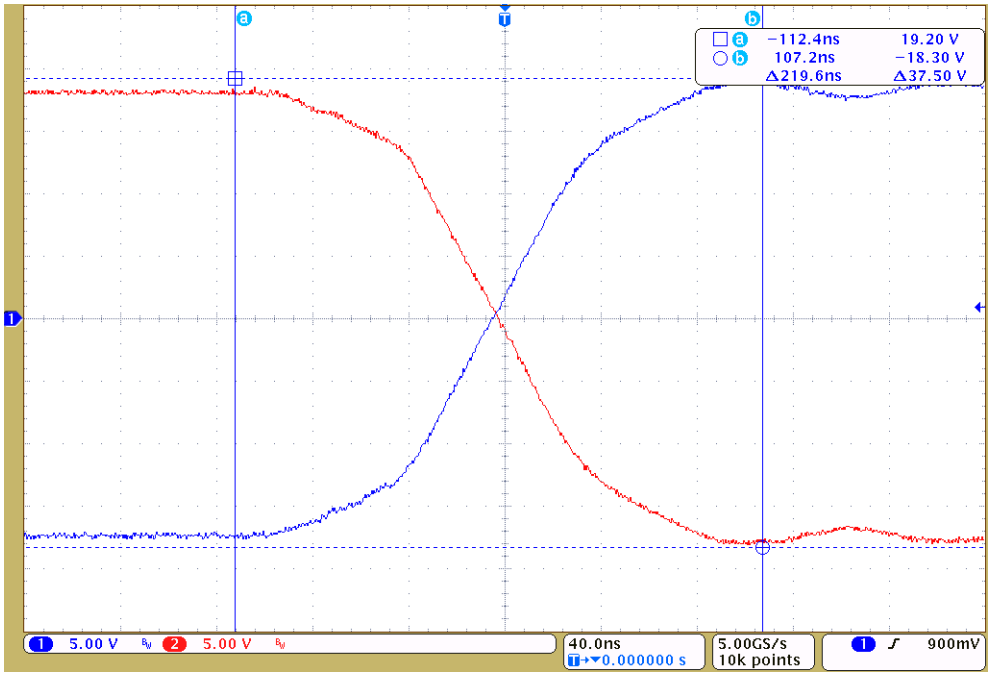


図 50. Zoomed in Version of 図 46 Showing Rise and Fall Times

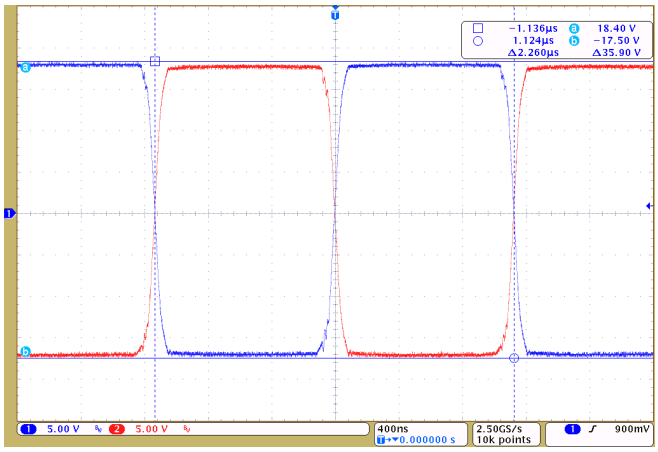


図 51. Secondary Side Transformer Switching Waveform With Respect to Secondary Centertap at Full Load

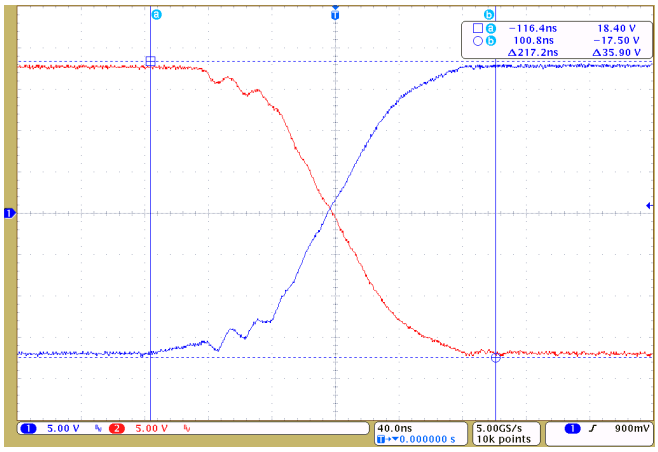


図 52. Zoomed in Version of 図 48 Showing Rise and Fall Times

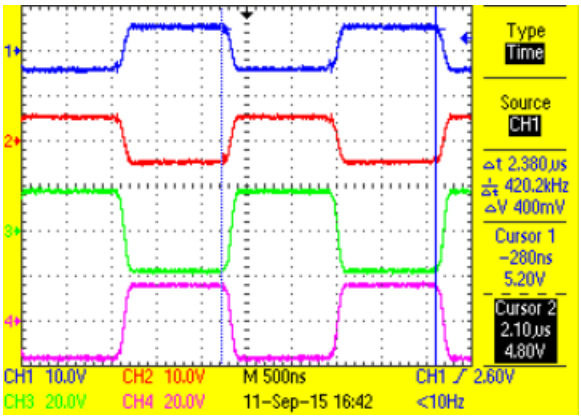


図 53. Primary and Secondary Side Waveforms of Transformer Referenced to Primary and Secondary Transformer Centertaps

In 図 53, as referred in 図 42:

- Channel 1 – Across pins 2 and 3 of transformer
- Channel 2 – Across pins 2 and 1 of transformer
- Channel 3 – Across pins 6 and 5 of transformer
- Channel 4 – Across pins 4 and 5 of transformer

5.2.4 Transformer Current Waveforms

図 54 and 図 55 show the primary side current into the transformer primary.

図 56 and 図 57 show the secondary side current into the transformer secondary centertap.

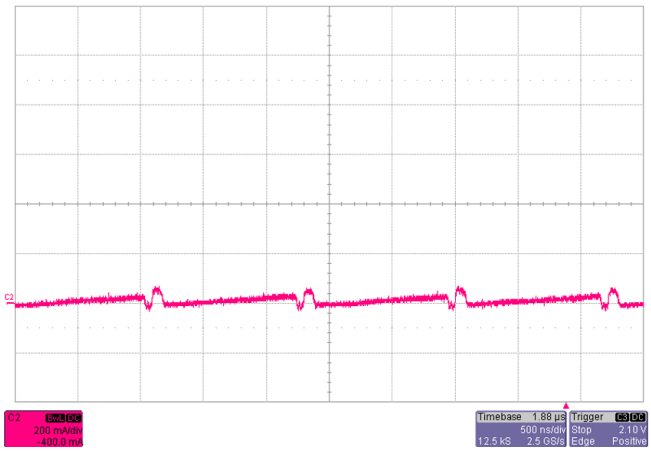


図 54. Current Flowing Into Transformer Primary Centertap From Input Bulk Capacitor at no Load

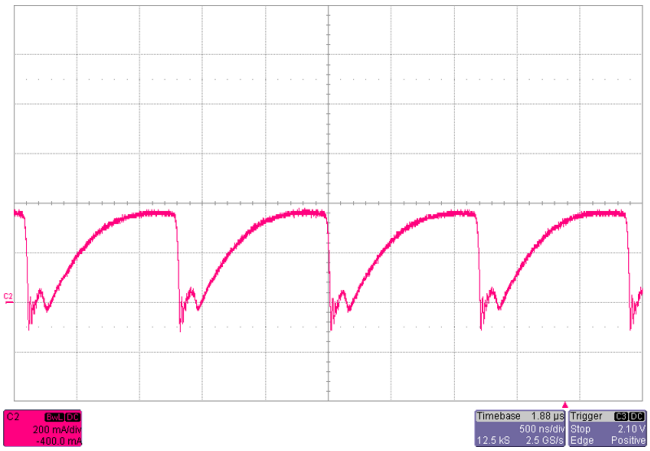


図 55. Current Flowing Into Transformer Primary Centertap From Input Bulk Capacitor at Full Load

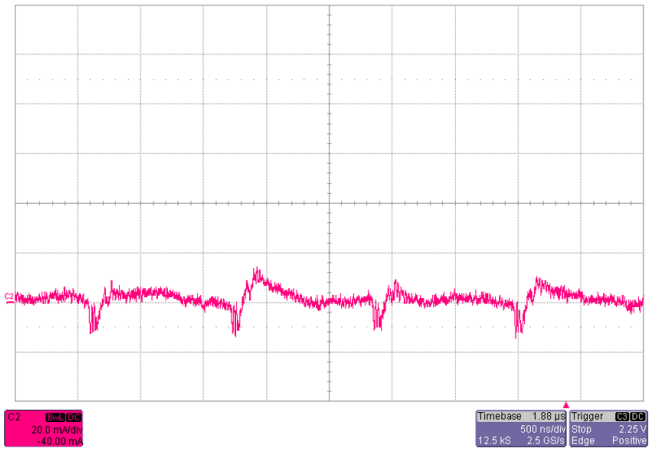


図 56. Current Flowing out of Transformer Secondary Centertap Into the Output Bulk Capacitor at no Load

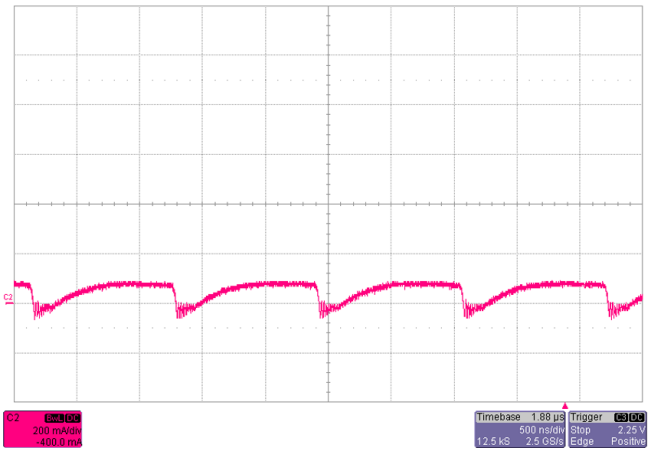


図 57. Current Flowing out of Transformer Secondary Centertap Into the Output Bulk Capacitor at Full Load

5.2.5 Spread Spectrum Modulation Waveforms

SN6505B has spread spectrum clocking function. 図 58 to 図 60 show the waveform captured across pins 3 and 2 of the transformer. The frequency spread is measured to be 29.83 kHz and the modulation frequency 27.02 kHz

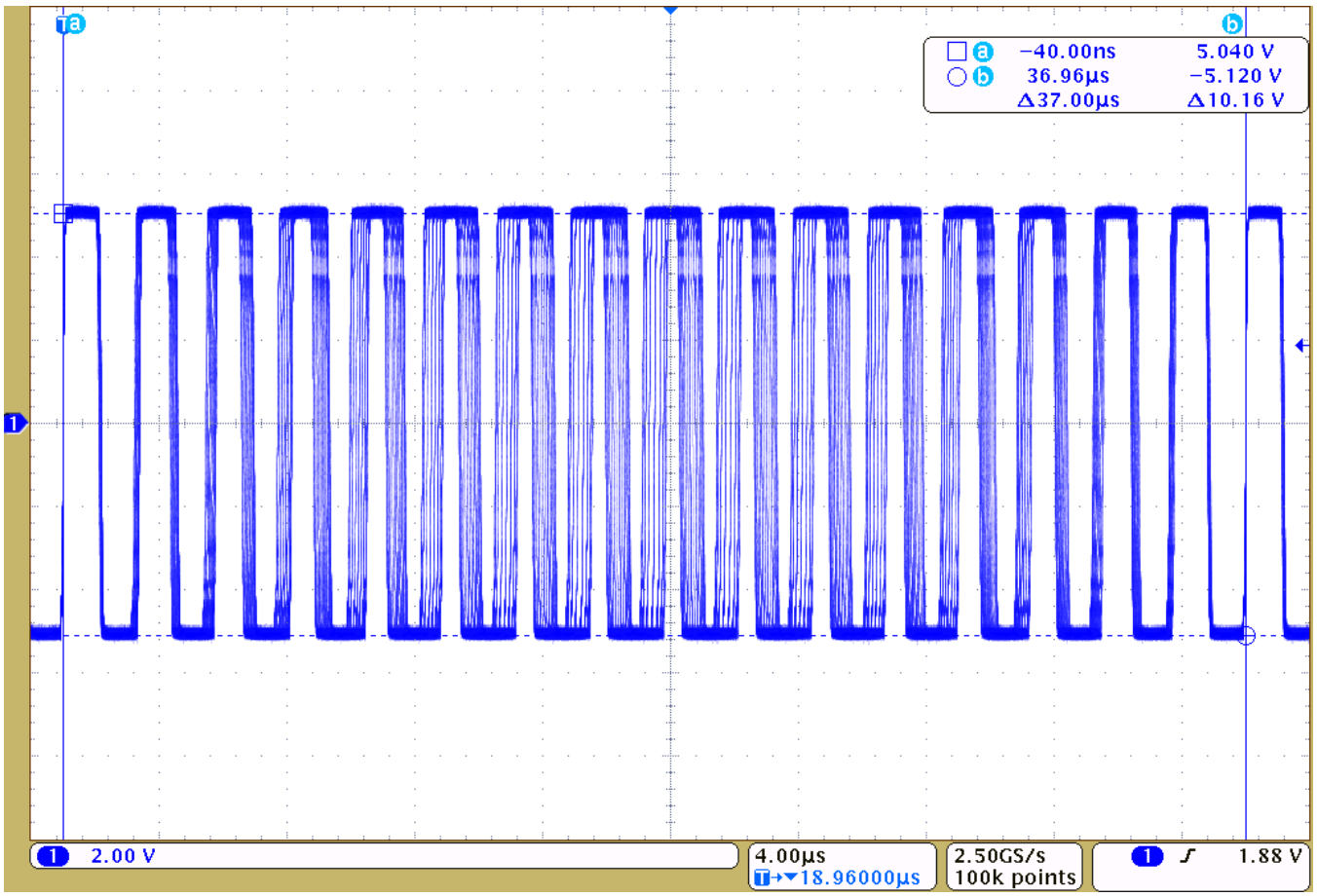


図 58. Transformer Primary Side Waveform Showing Modulation Frequency (27.02 kHz)

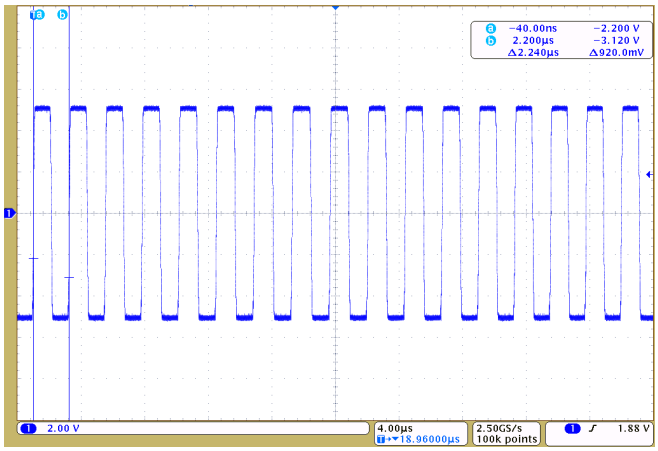


図 59. Maximum Switching Frequency (446.43 kHz)

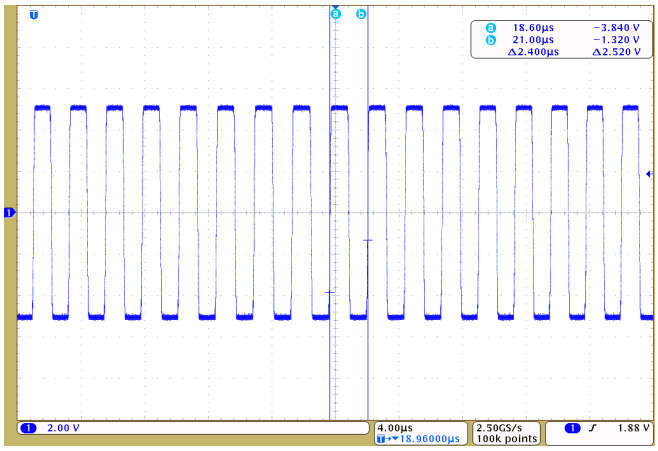


図 60. Minimum Switching Frequency (416.6 kHz)

5.2.6 Power Supply Shutdown Waveforms

In 図 61, channel 2 marks the switching pulse across switch D1 inside SN6505B and channel 1, the power supply enable signal, which is an active low signal. Pulling the enable signal high turns off the push-pull power supply. The delay from the instant the enable signal is forced high to the instant the SN6505B stops switching is 1.06 µs.

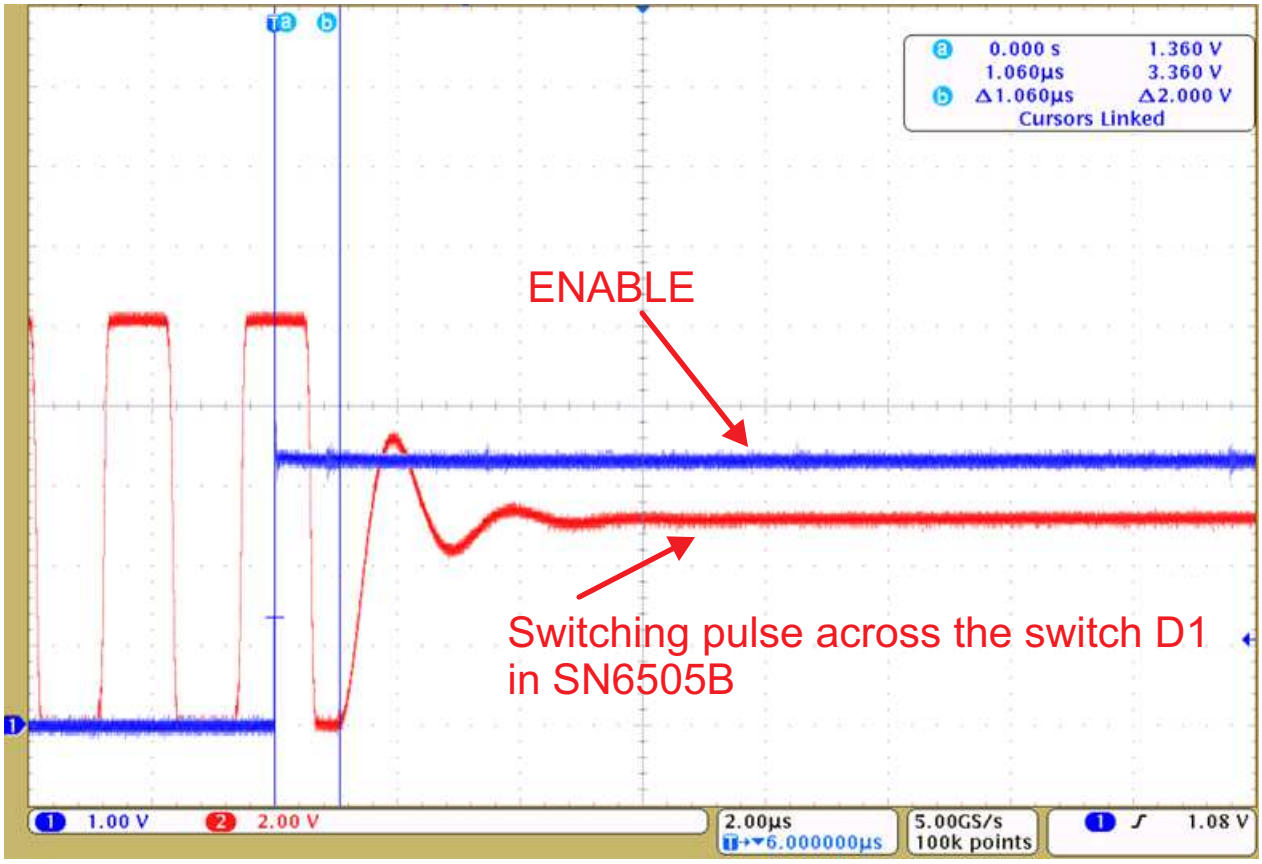


図 61. Time Delay to Shutdown of SN6505B (1.060 µs)

5.2.7 Total Input Power Consumed When Power Supply is Enabled or Disabled

Calculate the total input power consumed by the TIDA-00446 board when the power supplies are disabled by pulling the ENABLE signal high by:

- V_{in} = 5 V
- I_{in} = 0.226 mA
- P_{in} = 1.13 mW

Note that approximately 95% of this standby power is consumed by the 3.3- to 5-V level translator. 図 21 shows that most of the current consumed during the shutdown phase flows through resistor R9.

The total input power consumed by the entire board when the power supply is enabled but none of the gate drivers are driving PWM signals. The board is enabled by pulling down the ENABLE signal low:

- V_{in}= 5 V
- I_{in}= 182 mA
- P_{in} = 0.91 W approximately (46.83 mW + 55.44 mW + (0.3672/0.45) W)

0.45 is the efficiency at 3.6 mA load for the push-pull converter.

The quiescent current of ISO5851 measures 3.6 mA.

表 8. Power Consumption in the Quiescent Mode Operation

VOLTAGE RAIL	5 V	3.3 V	17 V
DEVICE	CURRENT CONSUMED	CURRENT CONSUMED	CURRENT CONSUMED
ISO5851 * 6		2.8 mA * 6 = 16.8 mA	3.6 mA * 6 = 21.6 mA
SN6505B * 6	1.56 mA * 6 = 9.36 mA		
TPS70633	1 uA * 6 = 6 uA		
TOTAL POWER	46.83 mW	55.44 mW	0.3672 W

5.2.8 Soft Start Waveforms

SN6505B has the soft start feature which helps reduce the inrush current into large output load capacitors. In 図 62 and 図 63 channel 1 is the enable input for the power supply and channel 2 is the isolated output voltage.

The soft start delay from the instant when the power supply is enabled to the instant when the output voltage reaches 90% of the final value is measured in 図 62. The soft start time measured from 10% to 90% of the final value is measured in 図 63.

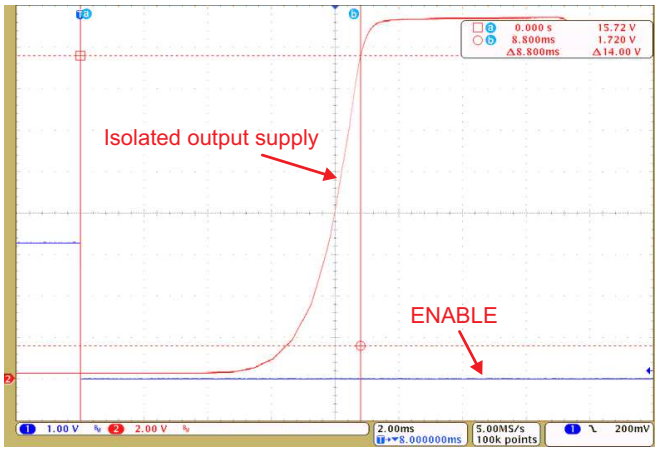


図 62. Soft Start Delay From Power Enable to 90% Transition Time on V_{OUT} (8.8 ms)

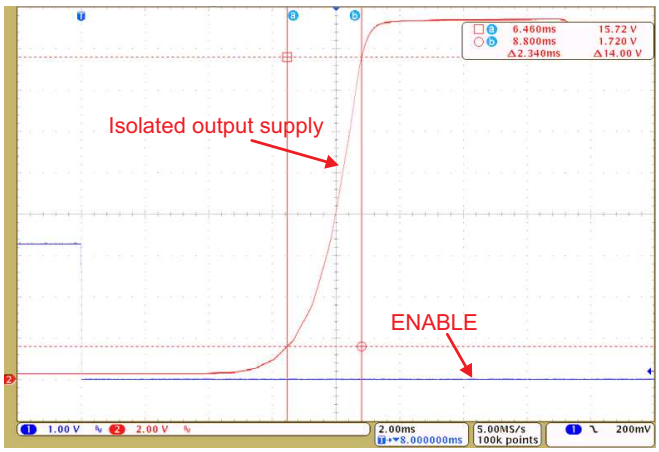


図 63. Soft Start Time from 10% to 90% Transition Time on V_{OUT} (2.34 ms)

5.2.9 Efficiency

The efficiency of the SN6505B based push pull power supply is tested. Two tests are conducted; in the first test the input voltage is maintained constant and the output load is varied, and in the second test the output load is kept constant and the input voltage is varied. The test results are shown in 図 64 and 図 65 respectively.

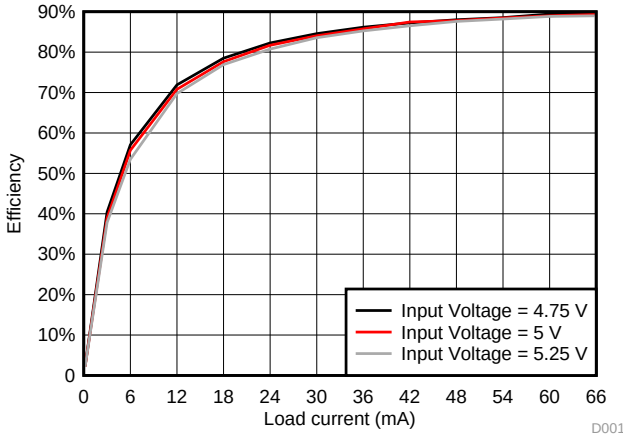


図 64. Efficiency versus Output Load

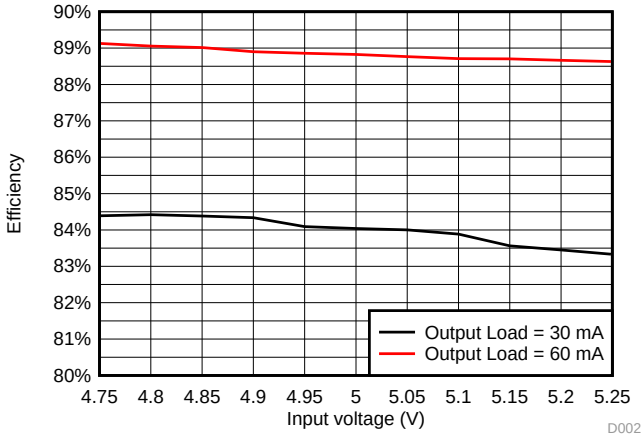


図 65. Efficiency versus Input Voltage

5.2.10 Line Regulation

図 66 shows the effect of change in input voltage of the push pull power supply on the output voltage at different output load conditions.

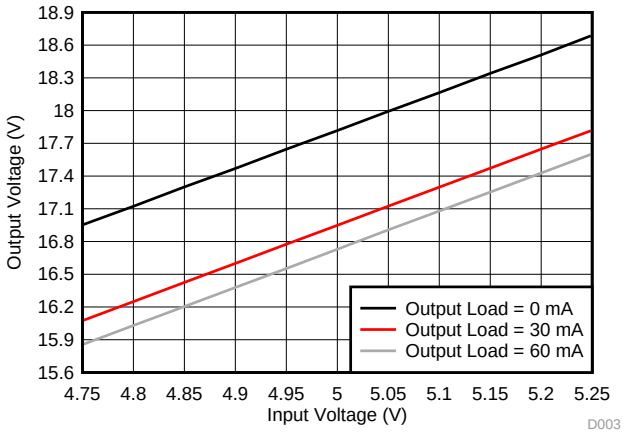


図 66. Power Supply Line Regulation at Difference Output Load Currents

5.2.11 Load Regulation

図 67 shows the effect of change in output load on the output voltage at different input voltages:

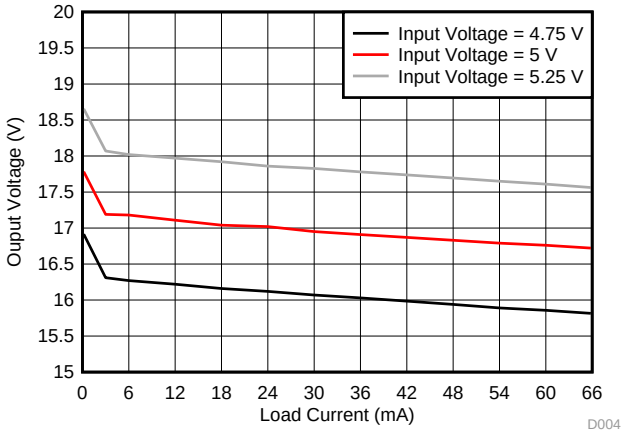


図 67. Power Supply Load Regulation at Different Input Voltages

5.2.12 Power Supply Regulation Versus Gate Driver Switching Frequency

The PWM input to the gate driver is varied from 0 Hz to 16 kHz. The change in output voltage with different switching frequencies is plotted in 図 68. In this test the gate emitter capacitance is simulated with a 0.1 µF capacitor C22, the gate resistors R5 and R7 are 4.7 Ω and the power supply input voltage is 5 V.

Note: Short the collector and emitter together if using a capacitor to simulate the gate to emitter capacitance instead of IGBT.

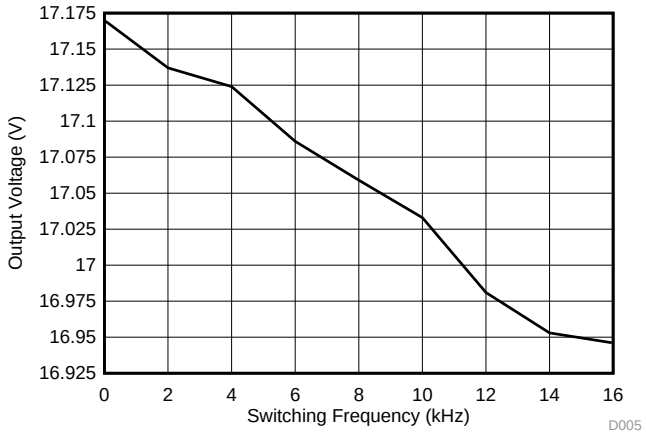


図 68. Regulation Versus Switching Frequency

5.3 Gate Driver Tests

The PWM propagation delay from the primary side to the secondary side for both the rising edge and the falling edge is measured in 図 69 to 図 70 at two different switching frequencies. Channel 1 is the PWM input to the gate driver and channel 3 is the gate driver PWM output. Measure the delay from 50% to 50% transition of the respective voltages.

図 71 and 図 72 show the ripple voltage on the isolated power supply due to sourcing 2 A and sinking 4 A by the gate driver. The tests are completed with an external 0.1 µF capacitor to simulate the IGBT gate emitter capacitance.

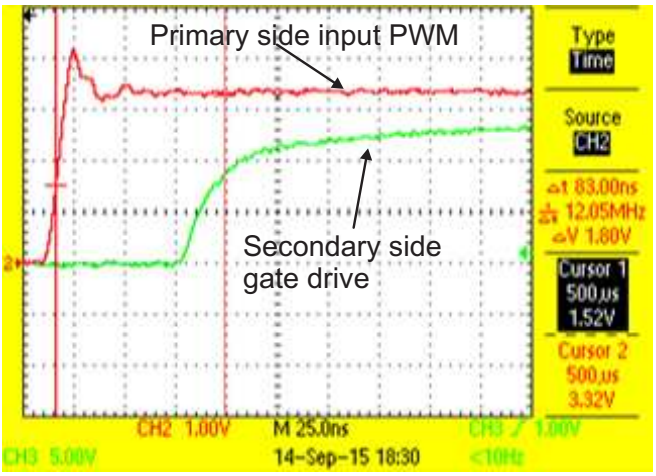


図 69. Turn On Delay From Input to Output of Gate Driver at 2 kHz (83.00 ns)

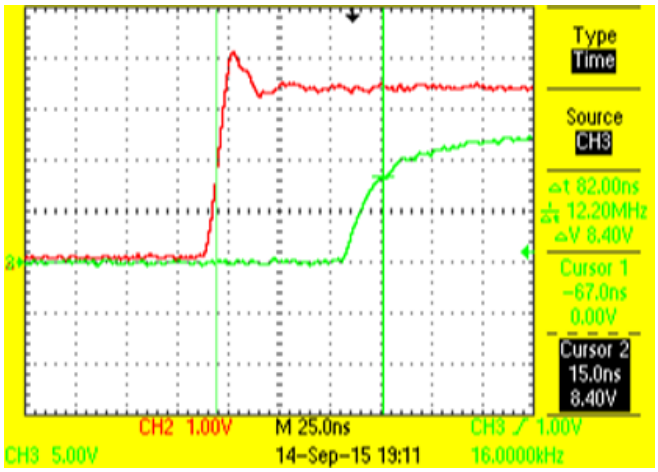


図 70. Turn On Delay From Input to Output of Gate Driver at 16 kHz (82.00 ns)

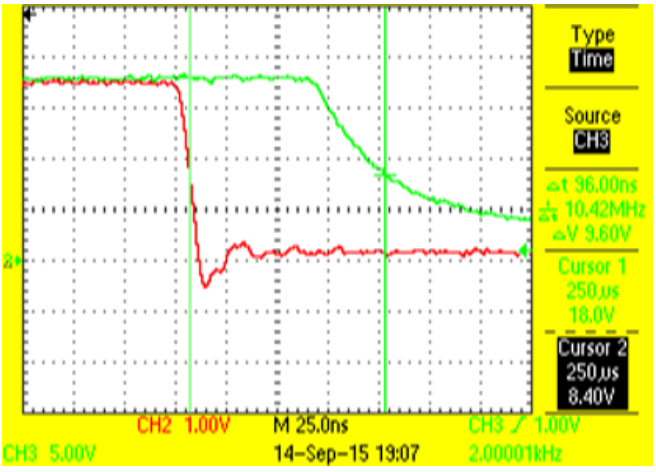


図 71. Turn Off Delay From Input to Output of Gate Driver at 2 kHz (96.00 ns)

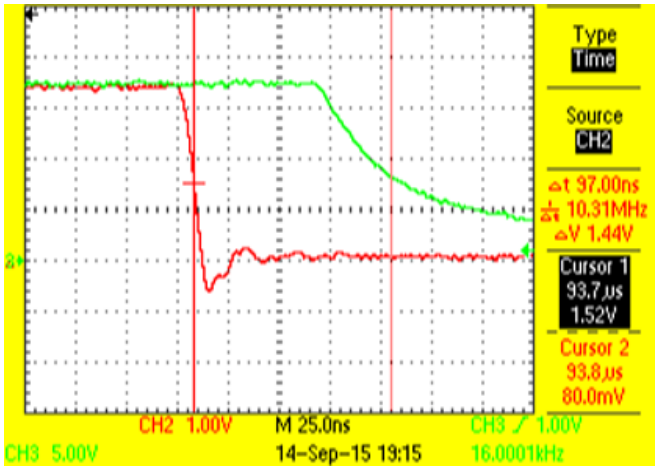


図 72. Turn Off Delay From Input to Output of Gate Driver at 16 kHz (97.00 ns)

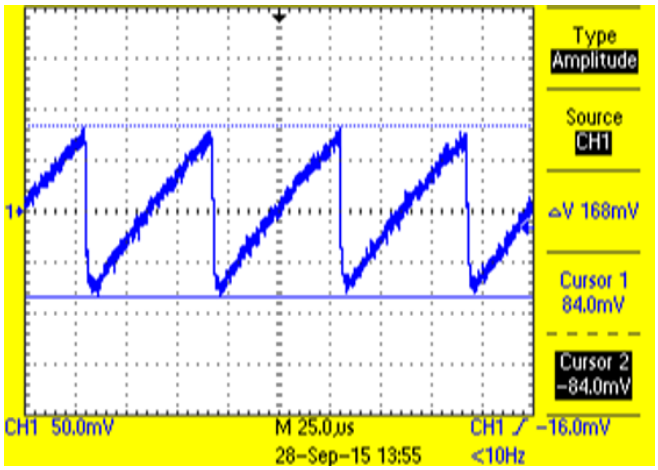


図 73. Amplitude of Voltage Ripple on Isolated Power Supply When Sourcing and Sinking 2.5 A and 5 A respectively at 16 kHz

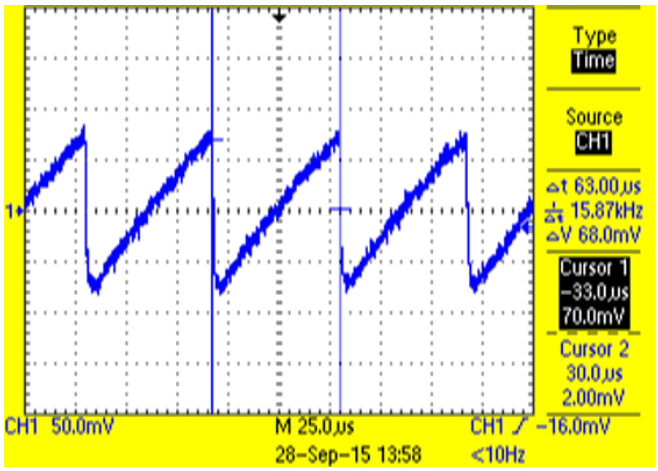


図 74. Frequency of Voltage Ripple on Isolated Power Supply When Sourcing and Sinking 2.5 A and 5 A Respectively at 16 kHz

5.3.1 Active Miller Clamp Waveforms

The six-pack IGBT module used for testing the Miller clamp and desaturation detection capability of the gate driver is FS50R12KT4_B15 (Infineon). The test setup is shown in 図 75 and 図 76. 図 77 shows the IGBT module connection. Use short twisted cable pairs for all connections. All waveforms are captured using spring ground leads instead of long ground wires to reduce parasitic inductance of the ground lead of oscilloscope probe. Using long ground leads will lead to increased noise capture; so using spring leads are recommended.

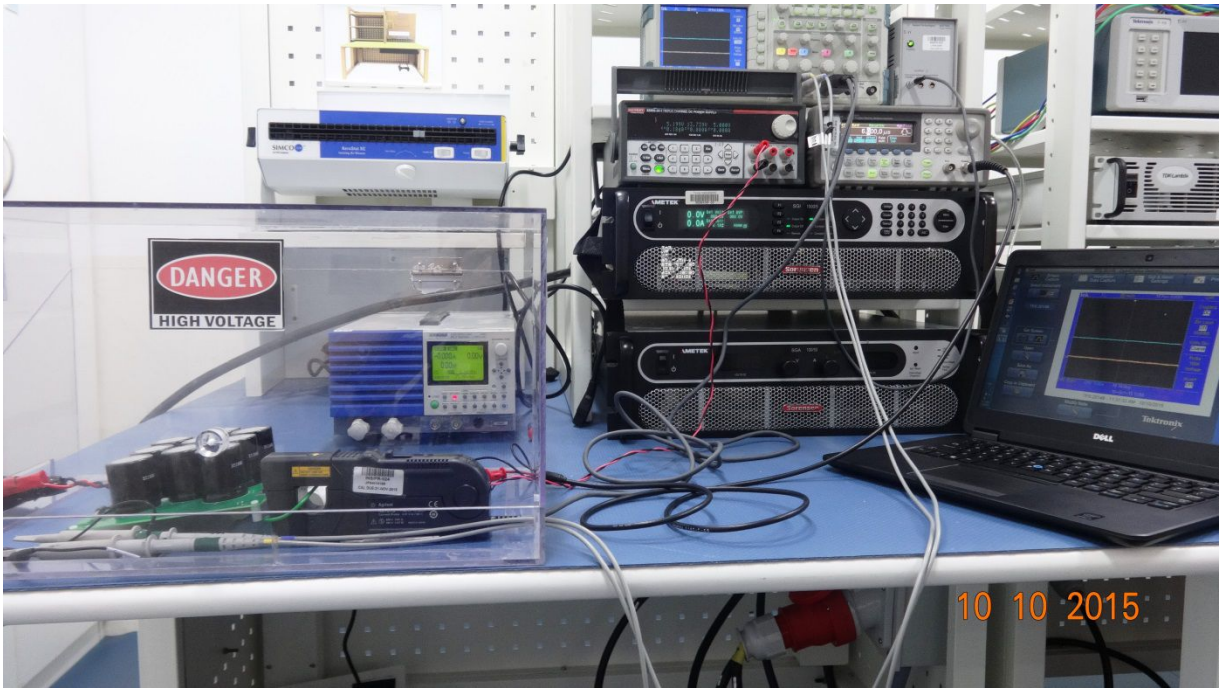


図 75. Miller Clamp and Desaturation Detection Test Setup

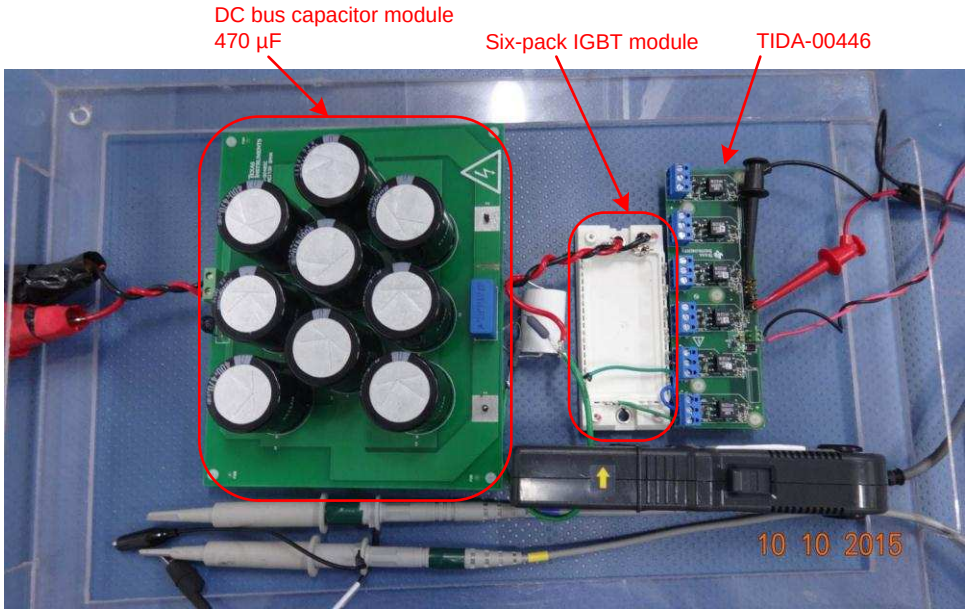


図 76. Setup Connected to IGBT Module

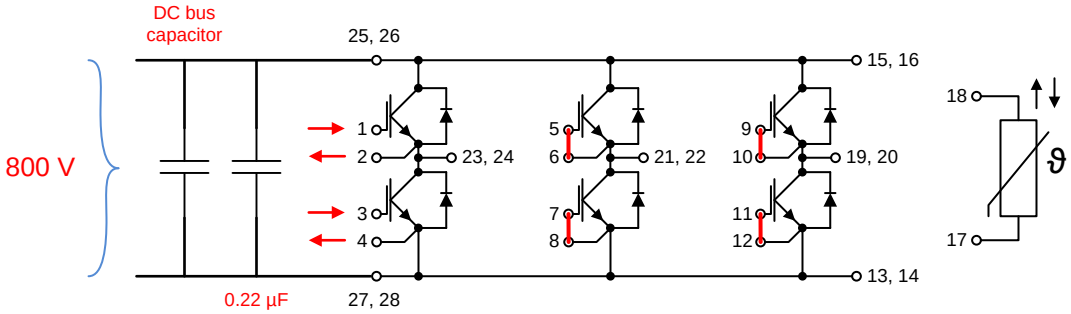


図 77. Connections to the IGBT Module

To capture the effect of the Miller clamp, first generate a high induced voltage across the V_{GE} of the IGBT. Using one half bridge of the three half bridges inside the module, keep the bottom IGBT off and pulse the top IGBT once. Short all unused IGBT gate-to-emitter terminals. Connect a load of 660 Ω between pins 23 and 27. When the top IGBT is pulsed, the voltage V_{CE} across the collector-to-emitter terminal of the bottom IGBT rises. The dV_{CE}/dt caused due to this induces a voltage in the gate-to-emitter terminal of the lower IGBT by conducting current through the Miller capacitor of the lower IGBT.

The gate driver ISO5851 disables the Miller clamp by lifting pin 7. 図 78, 図 80, 図 82, and 図 84 show the induced voltage without the Miller clamp at different points in the PCB. A voltage of 5.76 V is induced and this voltage is the same when measured at the IC pad, the connector pin, or at the module gate-to-emitter terminal.

図 79, 図 81, 図 83, and 図 85 show the effect of the Miller clamp on the induced voltage at different points of the PCB. The presence of the Miller clamp decreases the induced voltage from 5.84 V to 952 mV. This prevents false triggering of the lower IGBT and enables the use of unipolar supply instead of bipolar supply for driving the IGBT. Ringing is seen at the gate-to-emitter terminal of the module but this ringing is not observed at the gate driver pin. This ringing occurs due to the parasitic inductance of the Miller clamping trace. Therefore, keep this trace length as small as possible. Increasing the trace thickness reduces the inductance.

For the following waveforms, the blue line refers to the V_{CE} of lower IGBT and the pink line refers to the V_{GE} of lower IGBT. The first two figures (図 78 and 図 79) are labeled accordingly.

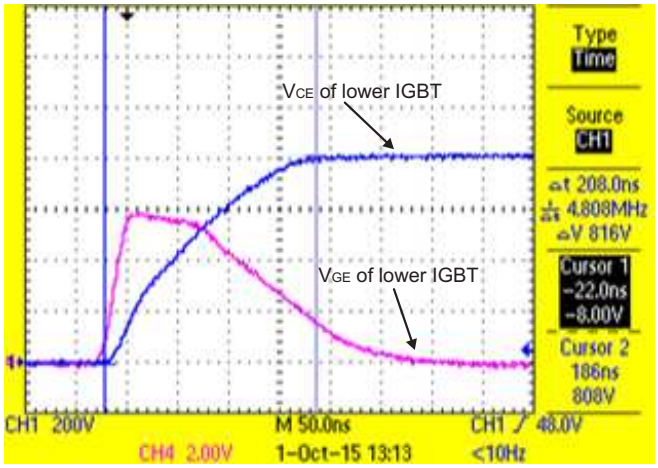


図 78. 4 kV/us dV_{CE}/dt Across the Lower IGBT Without Miller Clamp

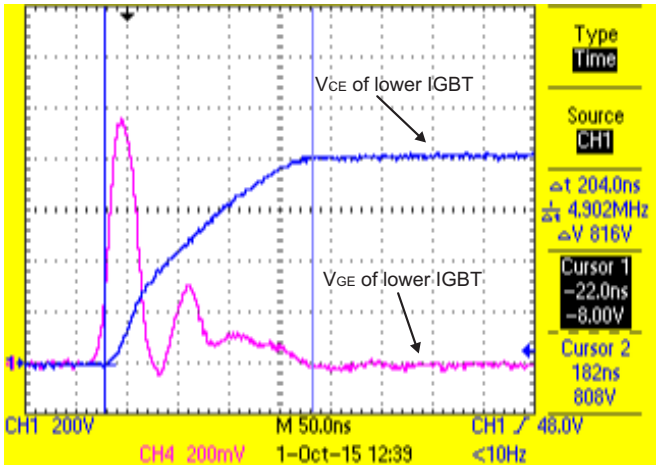


図 79. dV_{CE}/dt With Miller Clamp (4 kV/us dv/dt)

注: VGE Scale of 図 79 is 1/10th of 図 78

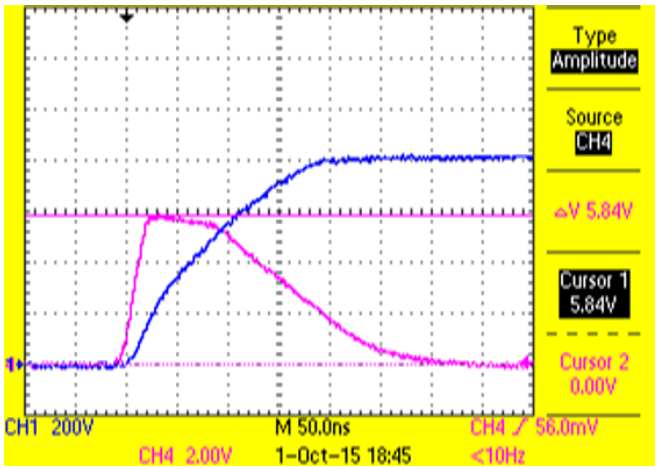


図 80. Induced Voltage Measured at Gate-to-Emitter of Module Without Miller Clamp (5.84 V)

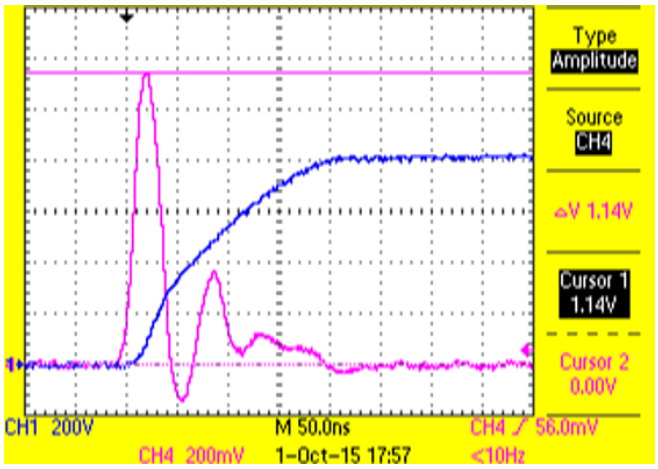


図 81. Induced Voltage Measured at the Gate to Emitter of Module With Miller Clamp (1.14 V)

注: VGE scale of 図 81 is 1/10th of 図 80

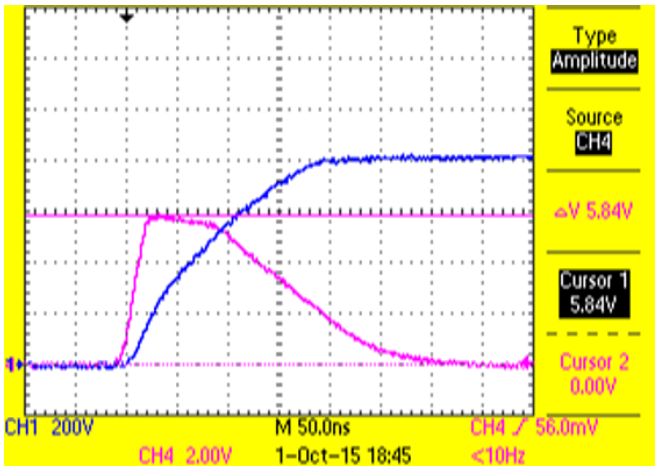


図 82. Induced Voltage Measured at Connector Without Miller Clamp (5.84 V)

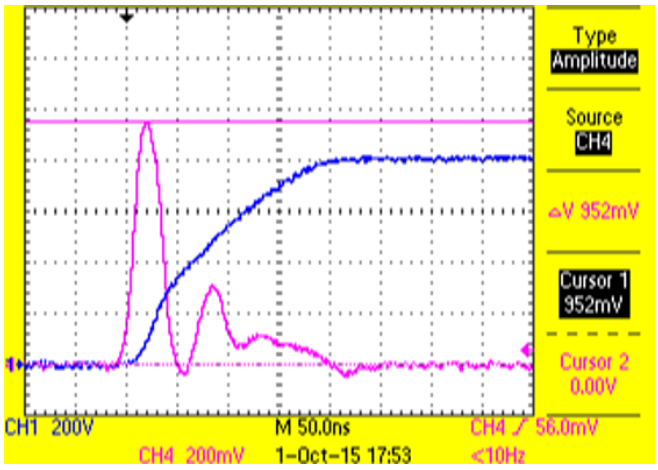


図 83. Induced Voltage Measured at Connector With Miller Clamp (952 mV)

注: VGE scale of 図 83 is 1/10th of 図 82

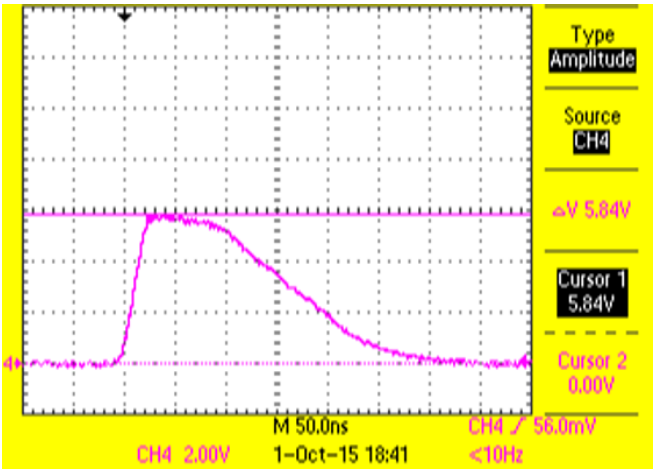


図 84. Induced Voltage Measured at the IC Pin Without Miller Clamp (5.84 V)

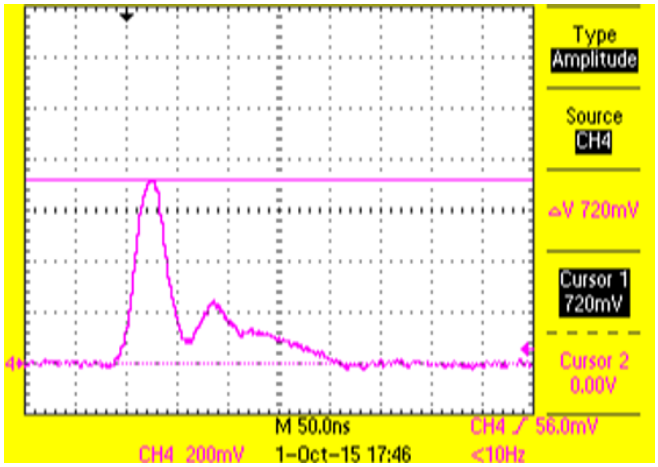


図 85. Induced Voltage Measured at the IC Pin With Miller Clamp (720 mV)

注: VGE scale of 図 85 is 1/10th of 図 84

5.3.2 Desaturation Detection

Use one of the half bridges out of the three inside the IGBT module to complete the short circuit detection test. Unused IGBT gate-to-emitter terminals are shorted. A large DC bus capacitor provides the short circuit current. Ensure all the external connections are as short as possible and they should be twisted cable pairs. All waveforms are captured with the help of spring ground leads on the oscilloscope probes. Using long ground leads will lead to increased parasitic inductance and the captured waveform will have a lot of noise. Two 1 Ω resistors are connected between the DC bus and the module. Measure the current through one of the resistors due to the limited measurement range of the current probe.

Keep the top IGBT ON and pulse the bottom IGBT with a pulse of width 6 µs. Disable the desaturation detection circuit of the top IGBT by unmounting the high voltage blocking diode and by connecting the open side of the 1 kΩ resistor to secondary side ground. When a short circuit occurs, the DC bus voltage of 800 V is shared equally between the top and bottom IGBTs. This increase in V_{CE} across the bottom IGBT is detected by the desat pin of the gate driver, which ramps up till the desat threshold is reached.

In 図 86, channel 1 is the signal at the desat pin of the ISO5851, channel 2 is the short circuit current and channel 4 is the voltage across the collector to emitter terminal of the lower IGBT. The short circuit current is measured to be 300 A (150 A * 2).

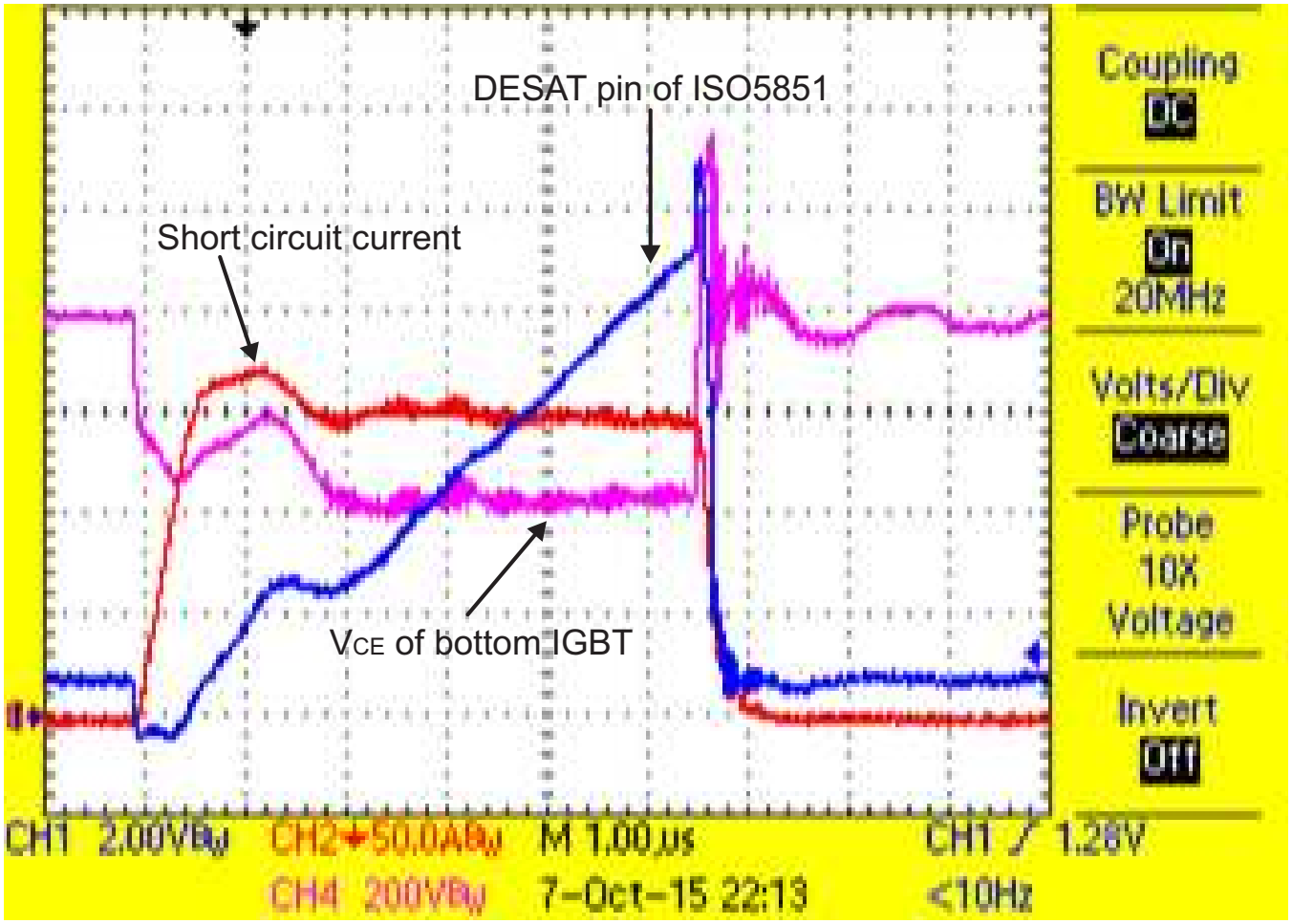


図 86. V_{CE} of IGBT During Short Circuit

図 87 measured the delay between the desat threshold being reached to the gate driver going low at 360 ns.

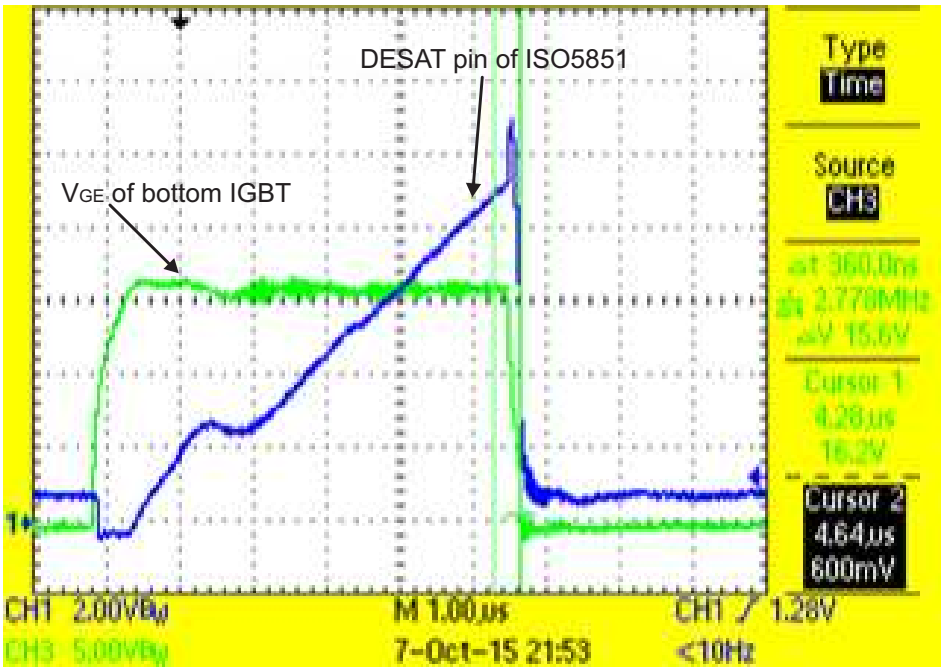


図 87. Desat Sense to 10 Percent Gate Drive Output Low delay (360 ns)

図 88 measured the delay between the desat signal being detected to the fault signal going low at 1.72 µs.

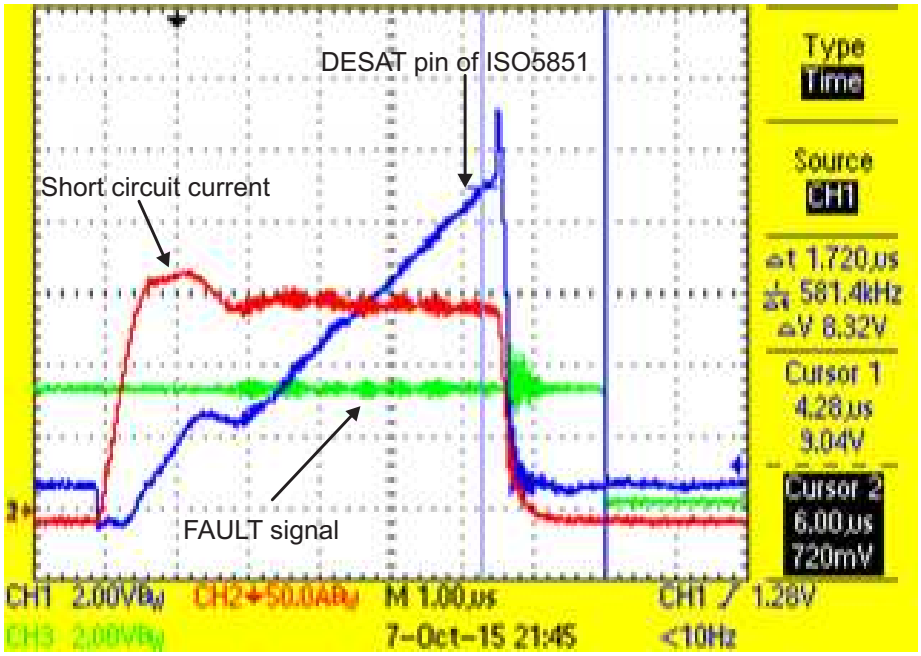


図 88. Desat Sense to Fault Signal Toggle Delay (1720 ns)

5.3.3 Temperature Rise

図 89 captures the infrared temperature of the push-pull power supply output loaded at 1 W for 0.5 hours at room temperature of 25°C.

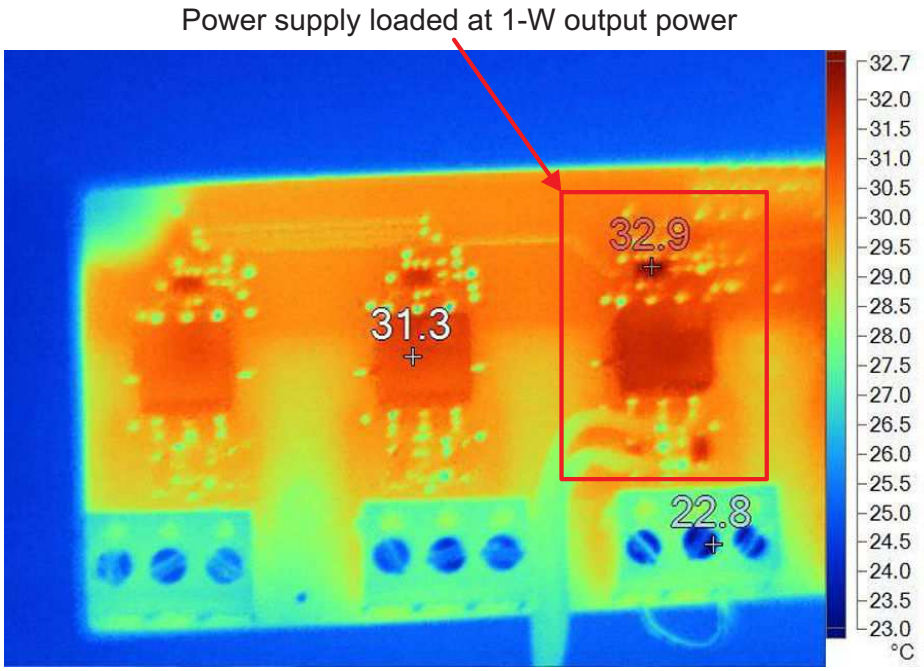


図 89. Temperature of Push-pull Power Supply After Running at Full Load for 0.5 hours

The PWM input to the gate driver is set at 16 kHz. The gate resistors are 4.7 Ω and the simulated gate emitter capacitance is 0.1 uF. The test is run for 0.5 hours at a room temperature of 25°C. 図 90 captures the infrared temperature picture.

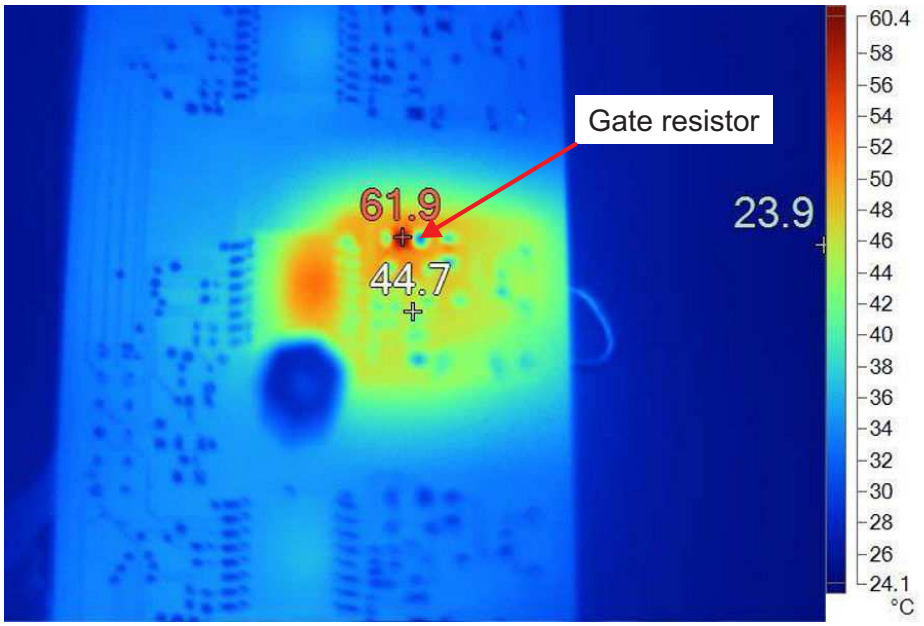


図 90. Temperature of Gate Driver After Switching at 16 kHz for 0.5 hours

6 Design Files

6.1 Schematics

Download the schematics for the board, see the design files at TIDA-00446.

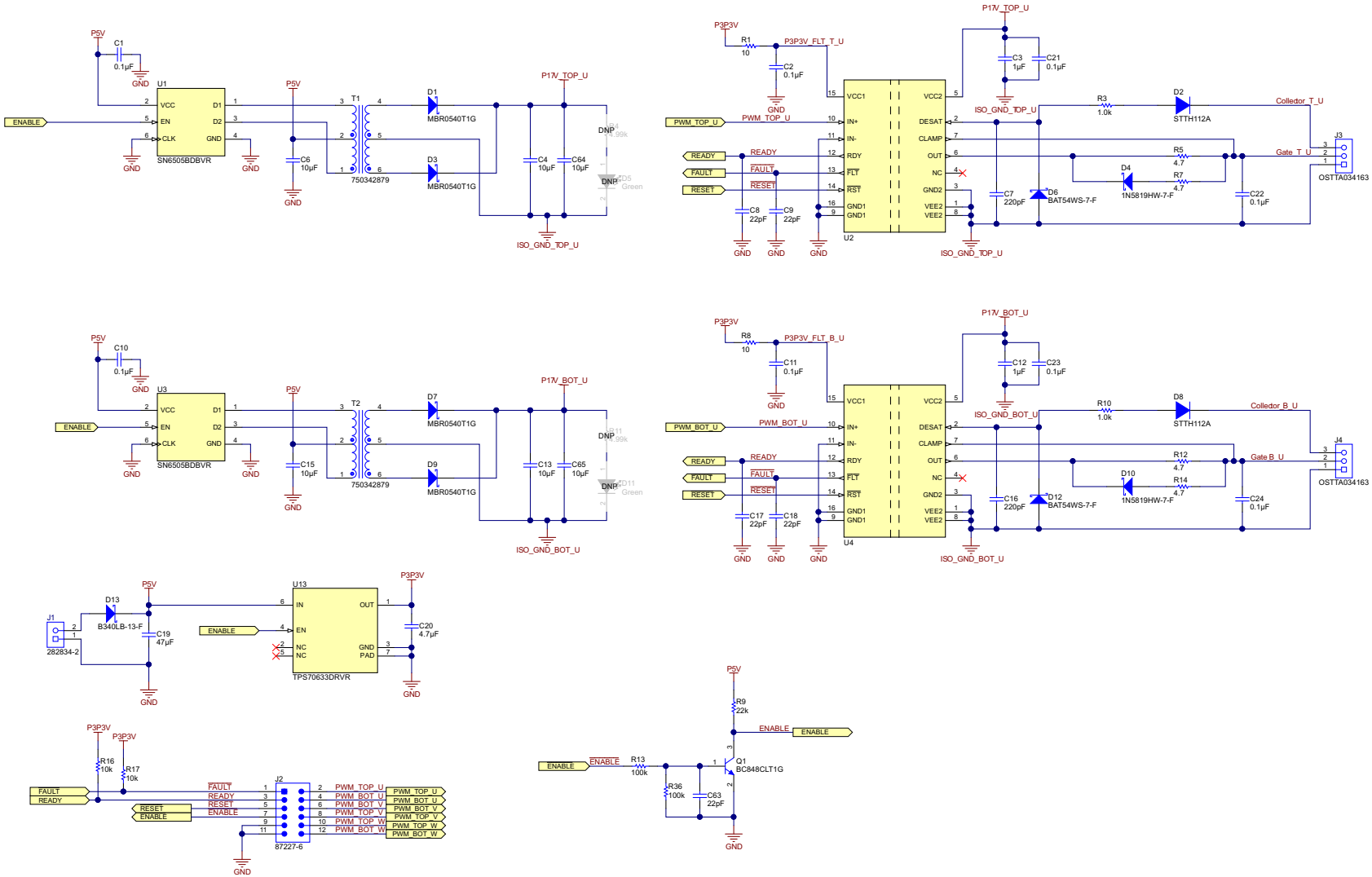


図 91. Schematics 1

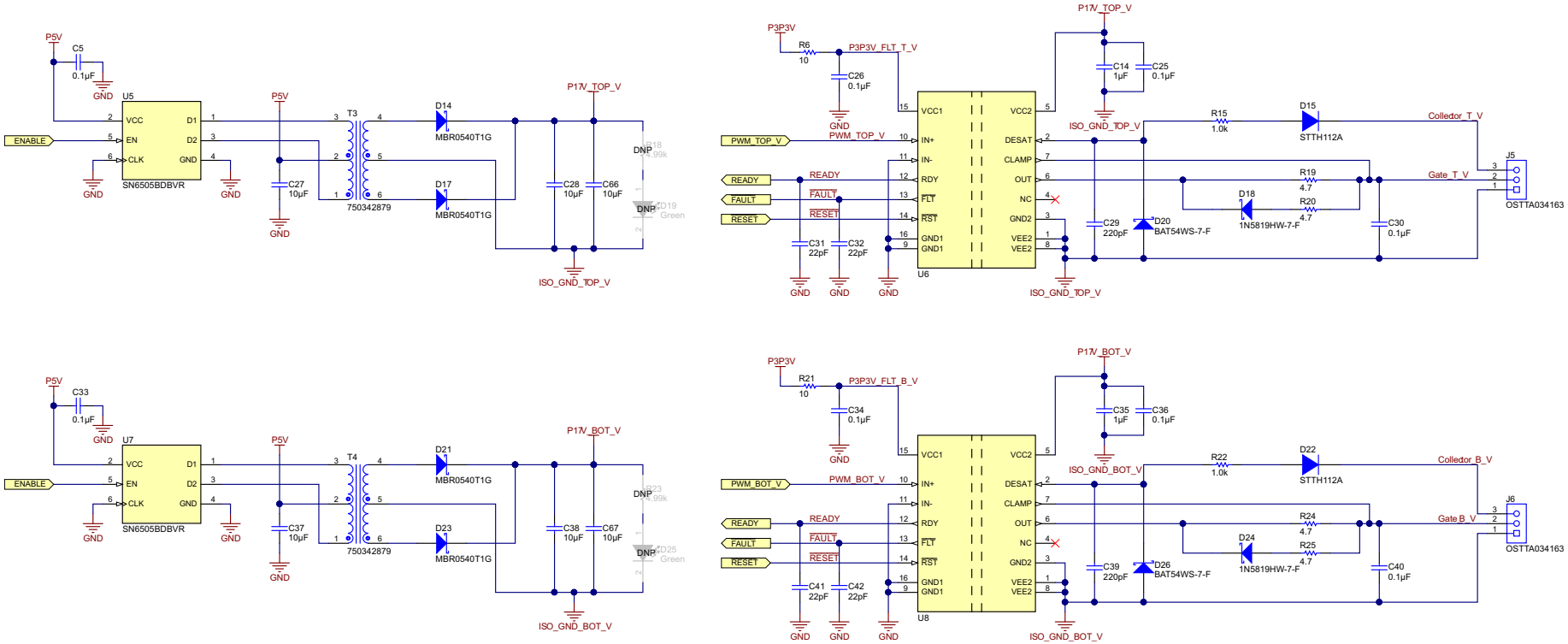


図 92. Schematics 2

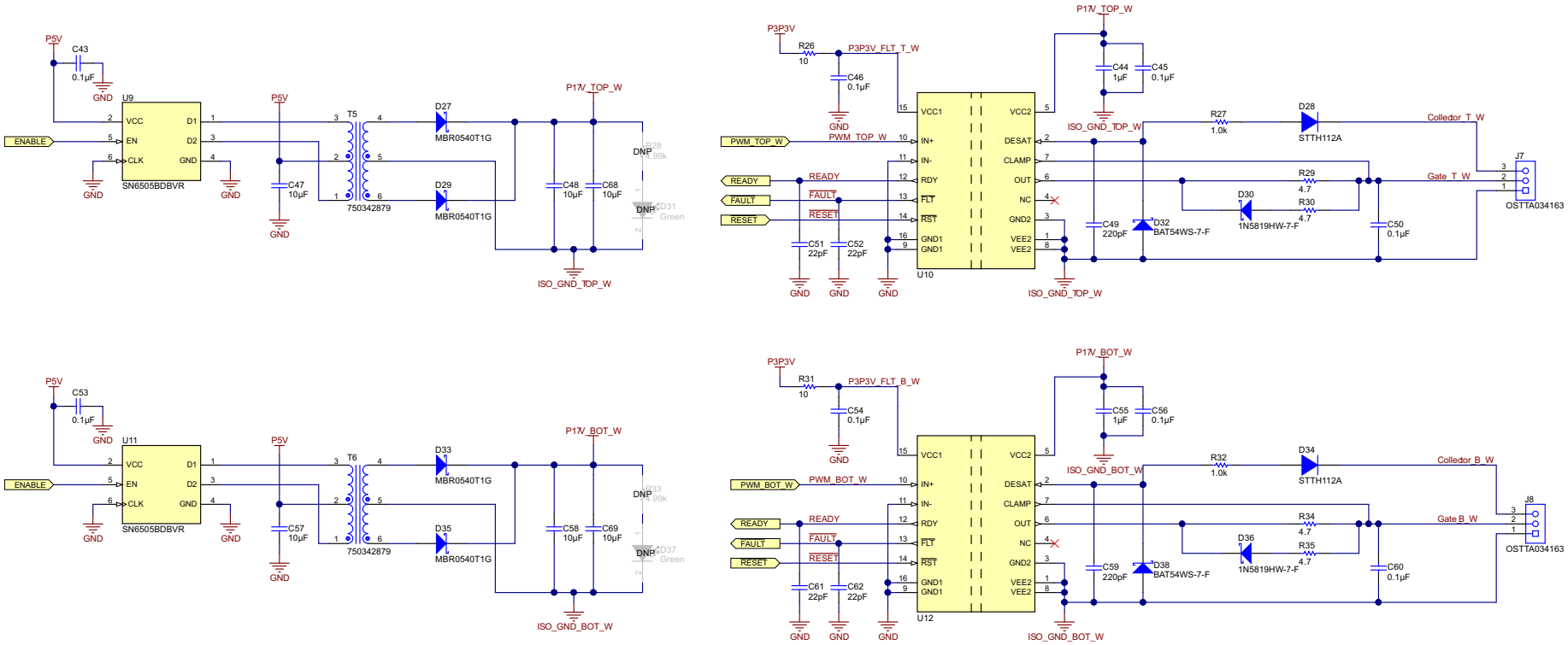


図 93. Schematics 3

6.2 Bill of Materials

Download the bill of materials (BOM), see the design files at TIDA-00446.

6.3 PCB Layout Recommendations

Layout is very important for proper and reliable operation of the circuit. The switching loops must be kept to a minimum to reduce EMI.

6.3.1 Layout Recommendations for SN6505B Based Push-pull Power Supply

- SN6505B switches at 424 kHz.
  To reduce loop inductance, the switching loops on both the input and output sides should have minimum area as shown in 図 94 and 図 95. 図 94 shows the primary and secondary side switching loops when D1 (pin 1 of SN6505B) is ON and 図 95 shows the primary and secondary side switching loops when D2 (pin 3 of SN6505B) is ON. Both the loop areas are kept minimum to reduce EMI.

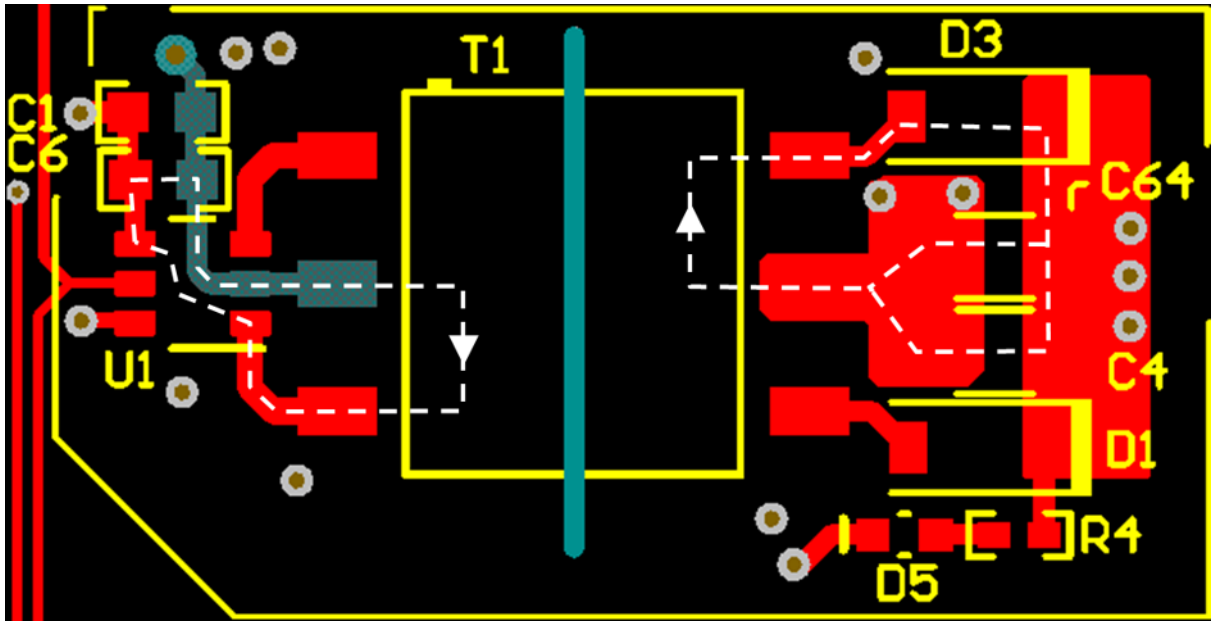


図 94. Switching Loops When D1 is on

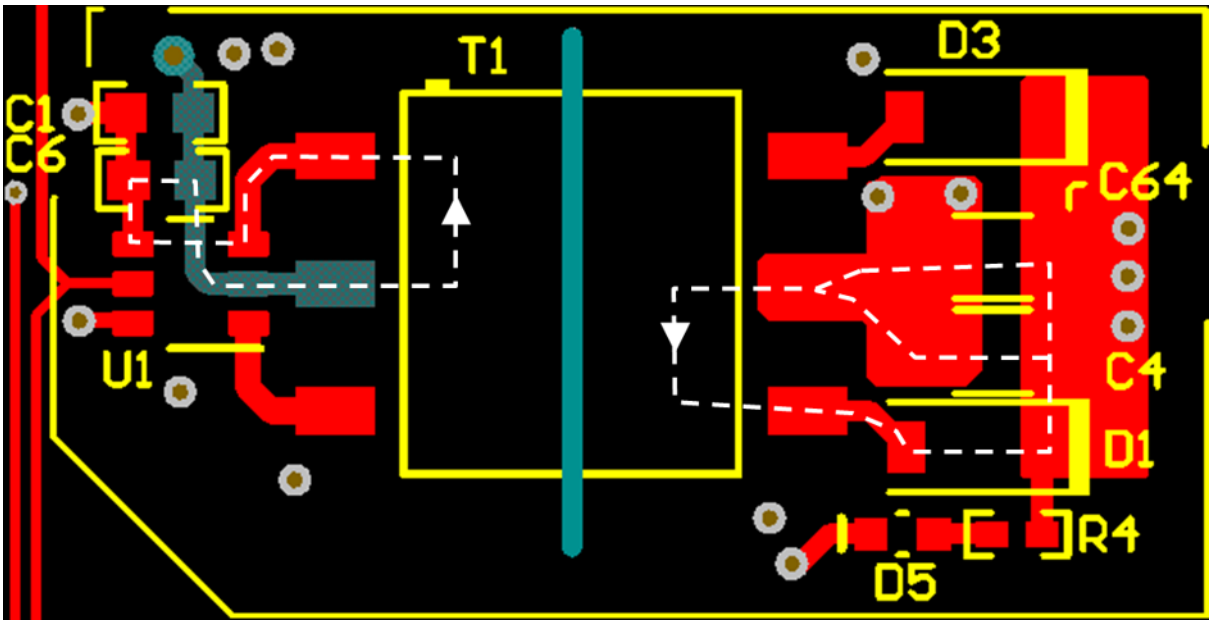


図 95. Switching Loop When D2 is On

- The SN6505B device U1 needs to be placed very close to the transformer T1
- The 10 µF bulk capacitor C6 should be kept close to the U1 power pin and GND
- Place at least two vias from the output bulk capacitor C4, C64 to the power planes. This provides a low inductance connection to the power planes.

6.3.2 Layout Recommendations for ISO5851 Isolated Gate Driver IC

- Place the 1 µF bulk capacitor C3 close to the power supply pin of the device
- Put a slot of 20 mil width right below the center of the IC. This is done to increase the creepage distance between the primary and secondary side for reinforced isolation
- 図 96 shows the path while sourcing current to the IGBT gate during IGBT turn ON. Keep this loop area to a minimum
- 図 97 shows the path while sinking current from the IGBT gate during IGBT turn OFF. Keep this loop area also to a minimum
- The Miller clamping trace from pin 7 of the IC to the gate of the power switch should be kept short or the trace made thick to reduce the parasitic trace inductance to reduce the induced voltage at the gate of the power switch.

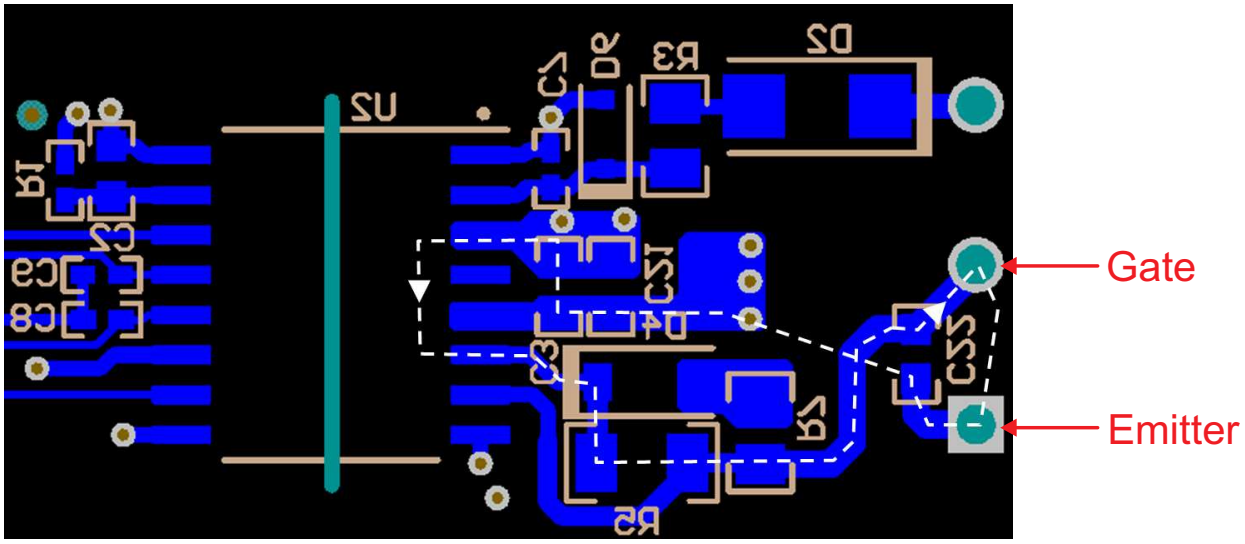


図 96. Gate Source Current Path

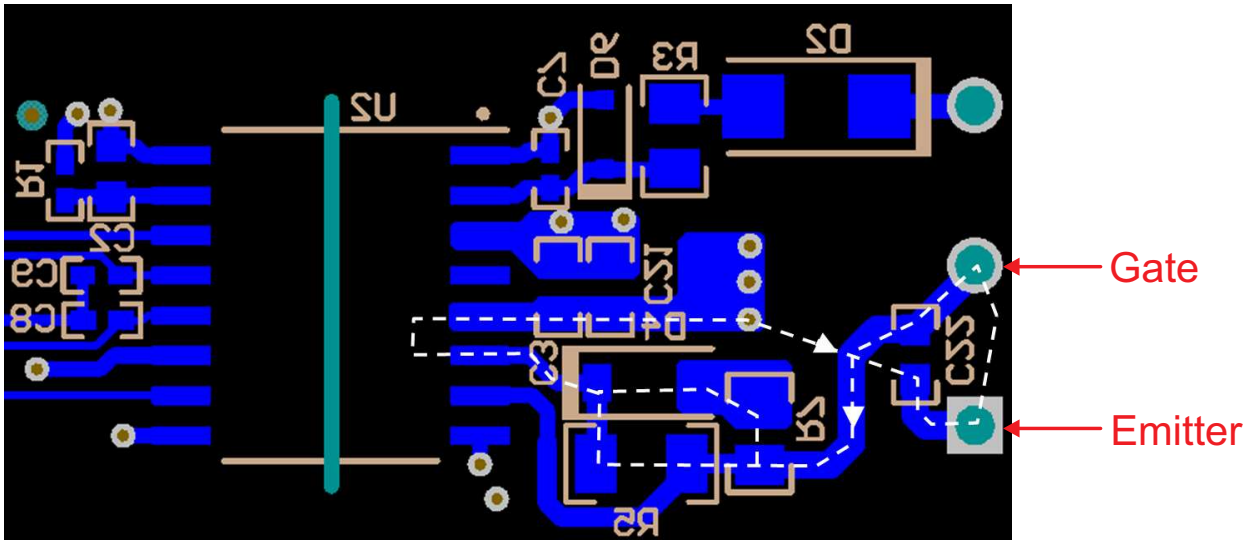


図 97. Gate Sink Current Path

6.4 Layout Prints

The PCB board size is 4.49 cm * 13.69 cm. The board area is 61.45 cm2.

To download the Layout Prints the board, see the design files at TIDA-00446.

6.5 Altium Project

To download the Altium project files, see the design files at TIDA-00446.

6.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00446.

6.7 Assembly Drawings

To download the Assembly Drawings for the board, see the design files at TIDA-00446.

7 Related Documentation

1. Texas Instruments, *High-Voltage Reinforced Isolation: Definitions and Test Methodologies*, White Paper (SLYY063)
2. Texas Instruments, *Isolated IGBT Gate Driver Evaluation Platform for 3-Phase Inverter System* , TIDA-00195 Reference Design (TIDUA15)

8 Terminology

IGBT— Insulated-gate bipolar transistor

CMTI— Common-mode transient immunity

DESAT— Desaturation

PWM— Pulse-width modulation

9 Acknowledgments

The authors would like to thank Baranwal Shailendra and Kamath Anant for their technical contributions to this design.

10 About the Author

PAWAN NAYAK is a Systems Engineer at Texas Instruments where he is responsible for developing reference design solutions for the Motor Drive segment within Industrial Systems.

N. NAVANEETH KUMAR is a Systems Architect at Texas Instruments, where he is responsible for developing subsystem solutions for motor controls within Industrial Systems. N. Navaneeth brings to this role his extensive experience in power electronics, EMC, Analog, and mixed signal designs. He has system-level product design experience in drives, solar inverters, UPS, and protection relays. N. Navaneeth earned his Bachelor of Electronics and Communication Engineering from Bharathiar University, India and his Master of Science in Electronic Product Development from Bolton University, UK.

改訂履歴 A–B

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (December 2015) から Revision B に変更 **Page**

- row for transformer dimensions 追加 12
- "Transformer Dimensions in mm" figure 追加 12

改定履歴C

Revision B (January 2016) から Revision C に変更 **Page**

- 「リソース」セクションのリンクを、TI.comの正しい場所に 変更 1
- all links in *Highlighted Products* section to correct locations on TI.com 変更 5
- all links in *Design Files* section to correct location on TI.com 変更 54

TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関係する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、あるいはTIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。