参考資料

TI Design: TIDA-01351
超音波CWドップラー用の高分解能、高SNR、真のrawデータ変換のリファレンス・デザイン

概要

このリファレンス・デザインは、超音波イメージング・システム(64、128、192、256チャネルの超音波システム)用の、連続波(CW)電圧信号コンディショニング・サブシステムです。この設計は20ビットの完全差動同時サンプリングを行い、真のrawデータを処理用に生成します。このTI Designは、Iチャネルと Qチャネル用の完全差動信号パスで構成され、各チャネルは、高性能のSARアナログ/デジタル・コンバータ(ADC)(ADS8900B)、完全差動高精度アンプ(THS4551)、低ノイズ、低ドロップアウト(LDO)のデュアル電圧レギュレータ(TPS7A8801)、高精度の基準電圧(REF5050)を使用します。TIDA-01351は、multiSPI™デジタル・インターフェイス経由でPH1-EVMコントローラと接続でき、任意のPCからUSBインターフェイスにより、PCベースのアプリケーション(GUI)を使用して性能を評価できます。

リソース

TIDA-01351	デザイン・フォルダ
ADS8900B	プロダクト・フォルダ
ADS8910B	プロダクト・フォルダ
ADS8920B	プロダクト・フォルダ
THS4551	プロダクト・フォルダ
TPS7A88	プロダクト・フォルダ
REF5050	プロダクト・フォルダ
OPA376	プロダクト・フォルダ
LM7705	プロダクト・フォルダ

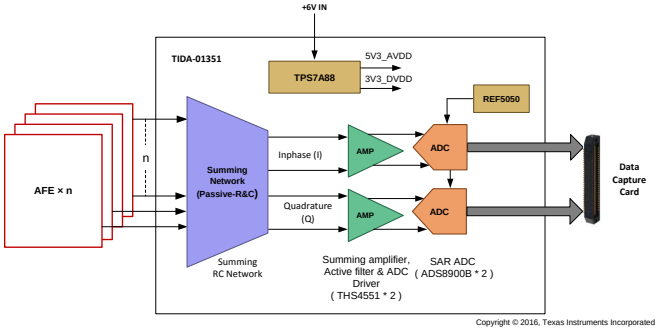
特長

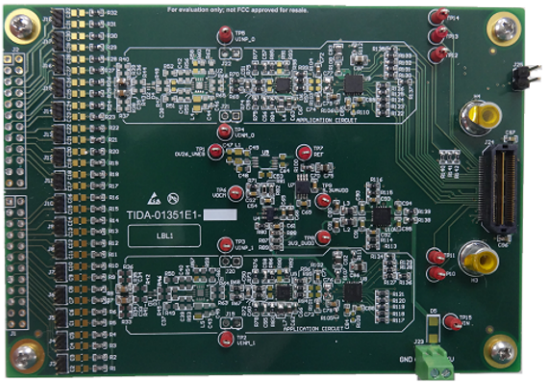
- 2つのチャネル(AFEからのIおよびQ電圧出力)の完全差動シグナル・チェーンを同時に使用できるため、ゼロ・レイテンシで真のrawデータを生成し、101.2dBのSNRと、16.45のENOBを実現
- 8チャネルの加算、フィルタリング、バッファリング、ゲインを単一段の高帯域幅、低消費電力、低ノイズ、単一電源の完全差動アンプに実装(THS4551)
- 高いサンプリング・レート(1MSPS)により、ポスト・プロセッシングを柔軟に行え、SNRと分解能を改善
- 50Hz～20kHzの周波数範囲にバンドパス・フィルタを適用
- 単一の6V電源で動作し、合計消費電力258mW
- ADS89x0B (20/18/16ビット)を使用し、1ppmのINLと、104.5dBのSNRで設計

アプリケーション

- 医療用超音波スキャナ
- 産業用イメージング
- SONARイメージング機器
- 非破壊検査機器

TI E2E™ Community　E2E™エキスパートに質問





1 System Description

Ultrasound imaging systems use high-frequency sound waves (several MHz or more) to image internal structures by the differing reflected signals produced when a beam of sound waves is projected into the body and bounces back at the interfaces between those structures. Ultrasound diagnosis differs from radiological diagnosis in that there is no ionizing radiation involved. The use of ultrasound to create images is based on the reflection and transmission of a wave at a boundary. When an ultrasound wave travels inside an object that is made up of different materials with varying densities (such as the human body), part of the wave is reflected and part of it is transmitted each time the wave encounters a boundary (for example, between bone and muscle or muscle and fat). The reflected rays are detected and used to construct an image of the object.

The ultrasound imaging system (図 1) front-end consists of two main sections: a transmit section and a receive section. The transmit section has a linear or pulse transmitter, which generates excitation pulses for ultrasound transducers of frequencies typically ranging from 1 to 15 MHz of amplitude ±2.5 to ±100 V. On the transmit (Tx) side, the Tx beam former determines the delay pattern and pulse train that set the desired transmit focal point. Ultrasound transducers are piezoelectric transducers that undergo mechanical deformation on the application of electrical pulses, which, in turn, produce ultrasound waveforms and the reverse process of an ultrasound wave at the surface of the transducer. The received ultrasound wave excites the transducer element to generate equivalent electrical energy. The reflected signal received by the transducer is conditioned by the receive (Rx path). There is a T/R switch, generally a diode bridge, which blocks the high voltage Tx pulses and protects the Rx circuit. This T/R switch can be either stand alone or integrate in the transmit pulsers. The T/R switch is followed by the receive AFE. The AFE usually incorporates a low-noise amplifier (LNA), voltage-controlled amplifier (VCA), programmable-gain amplifier (PGA), and an ADC to produce digitized output and, given to the receive beam former FPGA and then to the DSP for processing, image formation and display. Time gain control, which provides increased gain for signals from deeper in the body (and therefore arriving later), is under operator control and used to maintain image uniformity. Time gain control is implemented by controlling the gain of the VCA.

The CW Doppler has a very large dynamic range. During CW, a sine wave transmits continuously by half of the transducer array, and the other half receives. There is a strong tendency for the Tx signal to leak into the Rx side, and there are strong reflections coming from stationary body parts that are close to the surface. This action tends to interfere with examination of, for example, blood flow in a vein deep in the body with concomitant very weak Doppler signals. The CW Doppler signals cannot be processed through the main imaging (B-mode) and pulsed-wave (PW) Doppler (F-mode) path in a digital beamforming system; for this reason, images may be formed as either a sequence of analog levels that are delayed with analog delay lines, summed, and converted to digital after summation, which is indicated as CW Doppler processing. Receive AFE also integrates CW mixer and a low noise summer to form a CWD beam former. LNA output is passed through the CW mixer to demodulate the Doppler frequencies and produces I and Q signals, all these I and Q signals from all the channels in the same AFE are summed at a low-noise summer. Sixteen selectable phase delays can be applied to each analog input signal.

The most common use of ultrasound is in creating images, which have industrial and medical applications. Ultrasound systems have different forms or variants available in the market including cart-based, portable, or handheld.

図 1 shows the block diagram of an ultrasound imaging system.

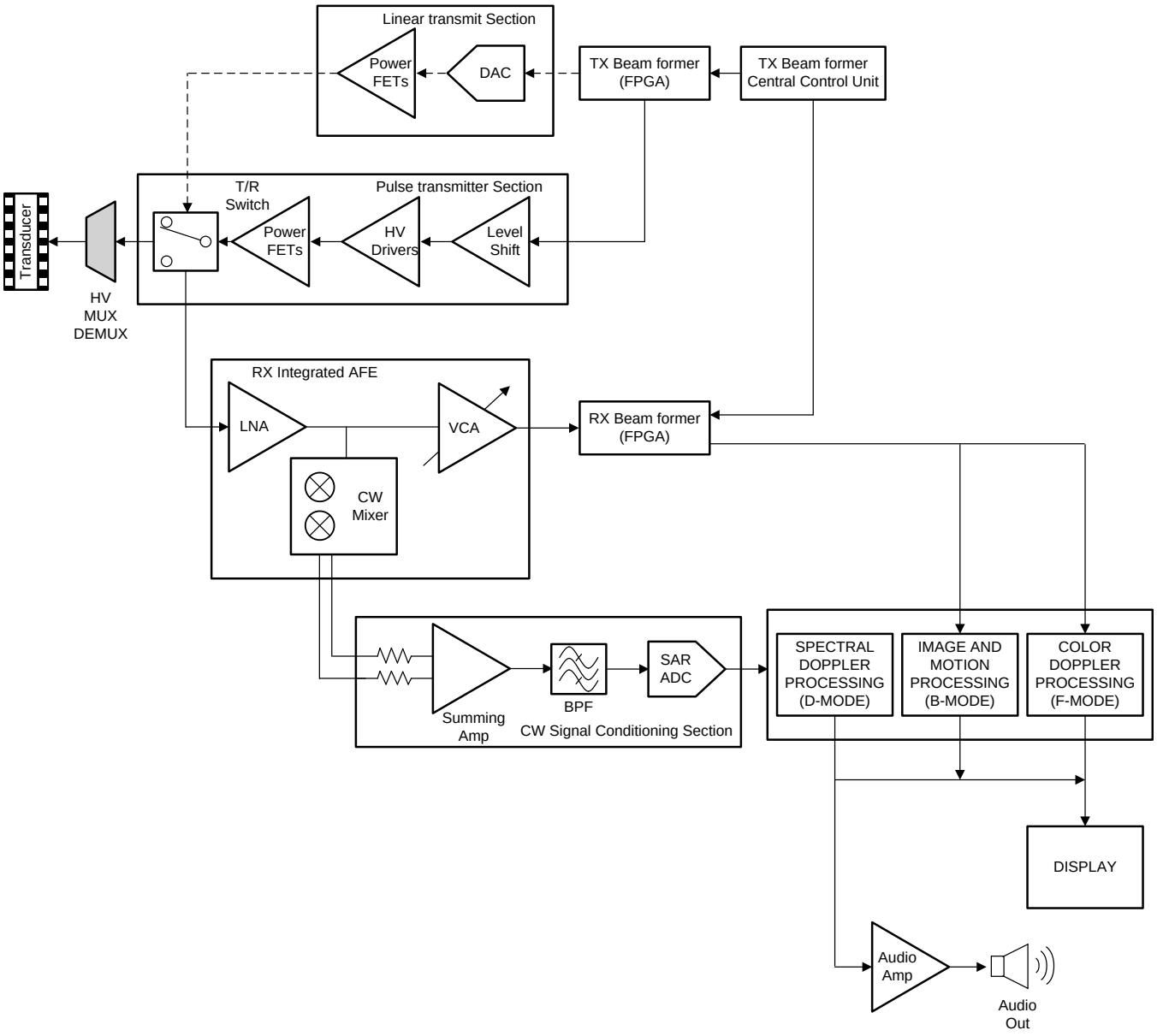


図 1. Ultrasound Imaging System Block Diagram

The TIDA-01351 design is a CW voltage output signal conditioning subsystem for ultrasound imaging systems, which features 20-bit fully-differential simultaneous sampling with true raw data available for processing. This TI Design has a fully differential signal path using high-performance SAR ADCs (ADS8900B), a fully-differential precision amplifier (THS4551), a dual, low-noise LDO voltage regulator (TPS7A88), and a precision voltage reference (REF5050). The TIDA-01351 can be interfaced with the PH1-EVM controller through the multiSPI digital interface, and the performance can be evaluated using a PC-based application (GUI) from any PC, through the USB interface. This TI Design can be used for both cart-based and portable ultrasound systems where simultaneous sampling and true raw data availability are the key selection requirements.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Number of channels	Two, simultaneous sampling
Input type	Differential
Input range	±10 µVp-p to ±500 mVp-p, fully differential
Resolution	20 bit
SNR	101.2 dB at 2-kHz signal input (gain = 1) 92.3 dB at 2-kHz signal input (gain = 10) 92.1 dB at 20-kHz signal input (gain = 10)
ENOB	16.45 at 2-kHz signal input (gain = 1) 15.44 at 2-kHz signal input (gain = 10) 15.01 at 20-kHz signal input (gain = 10)
Power	258 mW
Form factor	120 mm × 85 mm

This reference design supports only I and Q voltage outputs from AFE; the AFEs must be configured for I and Q voltage outputs. I and Q current outputs are not supported by this reference design. 表 2 shows the TI AFEs compatible with this reference design.

表 2. AFEs Compatible With TIDA-01351

AFE	CW OUTPUT
AFE5808	Voltage or current output
AFE5808A	Voltage or current output
AFE5807	Voltage or current output
AFE5809	Voltage or current output
AFE5818	Voltage or current output
AFE5812	Voltage or current output
AFE58JD18	Voltage or current output

表 3 compares the performance of the different TI SAR ADCs versus their resolution. These devices are drop-in replacement with pin compatibility. For test result details, see 3.2.2.3.

表 3. Comparison of TI SAR ADC Performance versus Resolution

SAR ADC	BITS	SNR
ADS8900B	20	94.3 dB at 2-kHz input signal, 90.7 dB at 20-kHz input signal (with gain = 10)
ADS8910B	18	94.1 dB at 2-kHz input signal, 88.8 dB at 20-kHz input signal (with gain = 10)
ADS8920B	16	92.7 dB at 2-kHz input signal, 88.4 dB at 20-kHz input signal (with gain = 10)

2 System Overview

2.1 Block Diagram

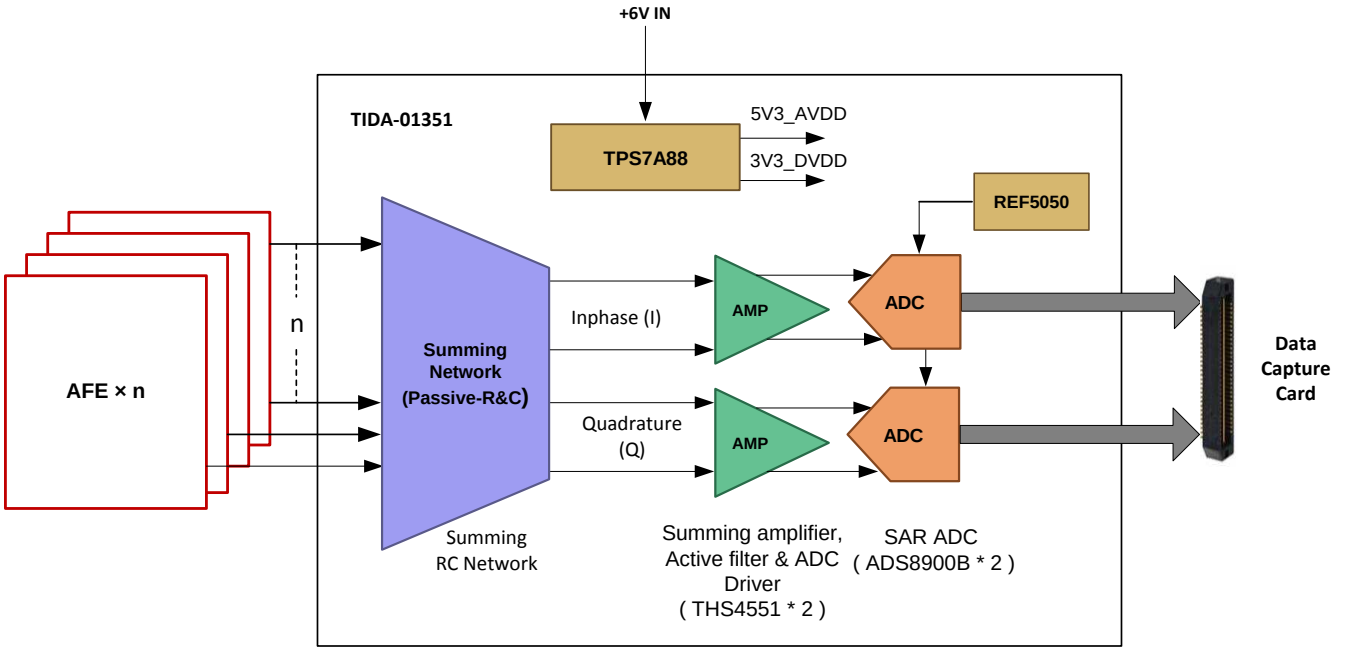


図 2. Block Diagram

2.2 Highlighted Products

2.2.1 ADS890xB

The ADS8900B, ADS8902B, and ADS8904B (ADS890xB) belong to a family of pin-to-pin compatible, high-speed, high-precision successive-approximation-register (SAR) ADCs with an integrated reference buffer and integrated LDO regulator. These devices support unipolar, fully-differential analog input signals with ±1-ppm INL and 104.5-dB SNR specifications under typical operating conditions. The integrated LDO enables single-supply operation with low-power consumption. The integrated reference buffer supports burst-mode data acquisition with 20-bit precision for the first sample. External reference voltages in the range of 2.5 to 5 V are supported, which offers a wide selection of input ranges without additional input scaling. The integrated multiSPI digital interface is backward-compatible to the traditional SPI protocol. Additionally, configurable features simplify board layout, timing, and firmware and support high throughput at lower clock speeds. The multiSPI digital interface allows for easy interface with a variety of microcontrollers (MCUs), digital signal processors (DSPs), and field-programmable gate arrays (FPGAs). The ADS890xB family is offered in a space-saving, 4-mm × 4-mm VQFN package and is specified over the extended temperature range of –40°C to 125°C.

2.2.2 THS4551

The THS4551 fully-differential amplifier offers an easy interface from single-ended sources to the differential output required by high-precision ADCs. Designed for exceptional DC accuracy, low noise, and robust capacitive load driving, this device is well suited for data acquisition systems where high precision is required along with the best signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR) through the amplifier and ADC combination. The THS4551 features the negative rail input required when interfacing a dc-coupled, ground-centered source signal to a single-supply differential input ADC. Very-low DC error and drift terms support the emerging 16- to 20-bit SAR input requirements. A wide-range output common-mode control supports the ADC running from 1.8- to 5-V supplies with ADC common-mode input requirements from 0.7 V to greater than 3.0 V. The THS4551 device is characterized for operation over the wide temperature range of –40°C to 125°C and is available in 8-pin VSSOP, 16-pin VQFN, and 10-pin WQFN packages.

2.2.3 TPS7A88

The TPS7A88 is a dual, low-noise (3.8 μV_{RMS}) LDO voltage regulator capable of sourcing 1 A per channel with only 200 mV of maximum dropout. The TPS7A88 provides the flexibility of two independent LDOs and approximately 50% smaller solution size than two single-channel LDOs. Each output is adjustable with external resistors from 0.8 to 5.0 V. The TPS7A88 wide input-voltage range supports operation as low as 1.4 V and up to 6.5 V. With 1% output voltage accuracy (over line, load, and temperature) and soft-start capabilities to reduce in-rush current, the TPS7A88 is ideal for powering sensitive analog low-voltage devices [such as voltage-controlled oscillators (VCOs), ADCs, digital-to-analog converters (DACs), high-end processors, and FPGAs]. The TPS7A88 is designed to power up noise sensitive components such as those found in high-speed communication, video, medical, or test and measurement applications. The very-low 4-μV_{RMS} output noise and wideband PSRR (40 dB at 1 MHz) minimizes phase noise and clock jitter. These features maximize performance of clocking devices, ADCs, and DACs.

2.2.4 OPA376

The OPA376 family represents a new generation of low-noise operational amplifiers with e-trim™, which offer outstanding DC precision and AC performance. Rail-to-rail input and output (RRIO), low offset (25 μV, maximum), low noise (7.5 nV/√Hz), a quiescent current of 950 μA (maximum), and a 5.5-MHz bandwidth make this part very attractive for a variety of precision and portable applications. In addition, this device has a reasonably wide supply range with excellent PSRR, making it attractive for applications that run directly from batteries without regulation. The OPA376 (single version) is available in MicroSIZE SC70-5, SOT-23-5, and SOIC-8 packages. The OPA2376 (dual) is offered in the DSBGA-8, VSSOP-8, and SOIC-8 packages. The OPA4376 (quad) is offered in a TSSOP-14 package. All versions are specified for operation from –40°C to 125°C.

2.2.5 LM7705

The LM7705 device is a switched capacitor voltage inverter with a low-noise, –0.23-V fixed negative voltage regulator. This device is designed to be used with low-voltage amplifiers to enable the amplifiers output to swing to zero volts. The −0.23 V is used to supply the negative supply pin of an amplifier while maintaining less than 5.5 V across the amplifier. Rail-to-rail output amplifiers cannot output 0 V when operating from a single-supply voltage and can result in error accumulation due to amplifier output saturation voltage being amplified by following gain stages. A small negative supply voltage will prevent the amplifiers output from saturating at 0 V and will help maintain an accurate zero through a signal processing chain. Additionally, when an amplifier is used to drive an input of the ADC, the amplifier can output a zero voltage signal and the full input range of an ADC can be used. The LM7705 device has a shutdown pin to minimize standby power consumption.

2.2.6 REF5050

The REF50xx is a family of low-noise, low-drift, and very-high precision voltage references. These references are capable of both sinking and sourcing current and have excellent line and load regulation. Excellent temperature drift (3 ppm/°C) and high accuracy (0.05%) are achieved using proprietary design techniques. These features, combined with very-low noise, make the REF50xx family ideal for use in high-precision data acquisition systems. Each reference voltage is available in both high grade (REF50xxIDGK and REF50xxID) and standard grade (REF50xxAIDGK and REF50xxAID). The reference voltages are offered in 8-pin VSSOP and SOIC packages and are specified from –40°C to 125°C.

2.3 System Design Theory

The system consists of a summing stage, active filter, ADC driver, charge kickback filter, and a SAR ADC. Two such stages are used in this TI Design, one for I and other for Q voltage output signal, which demonstrates simultaneous sampling of I and Q signals received from receive AFEs. The I and Q voltage outputs from different receive AFEs are summed and filtered before digitizing. The TIDA-01351 design demonstrates the summing of I and Q signals from eight receive AFEs. The ADC used in this TI Design is a 1-MSPS, 20-bit fully-differential SAR ADC. The SAR ADC provides true raw data with low latency and good SNR. For even higher SNR, an external digital filter can be used. The TIDA-01351 filter design is designed to have a completely flat passband for the audio band ranging from 54 Hz to 20 kHz. This TI Design also has a complete low-noise power supply solution.

2.3.1 Summing Stage, Active Filter, ADC Driver, and Charge Kickback Filter

図 3 shows the summing stage, active filter, gain stage, ADC driver, charge kickback filter, and ADC. The same circuit is replicated for both I and Q channels.

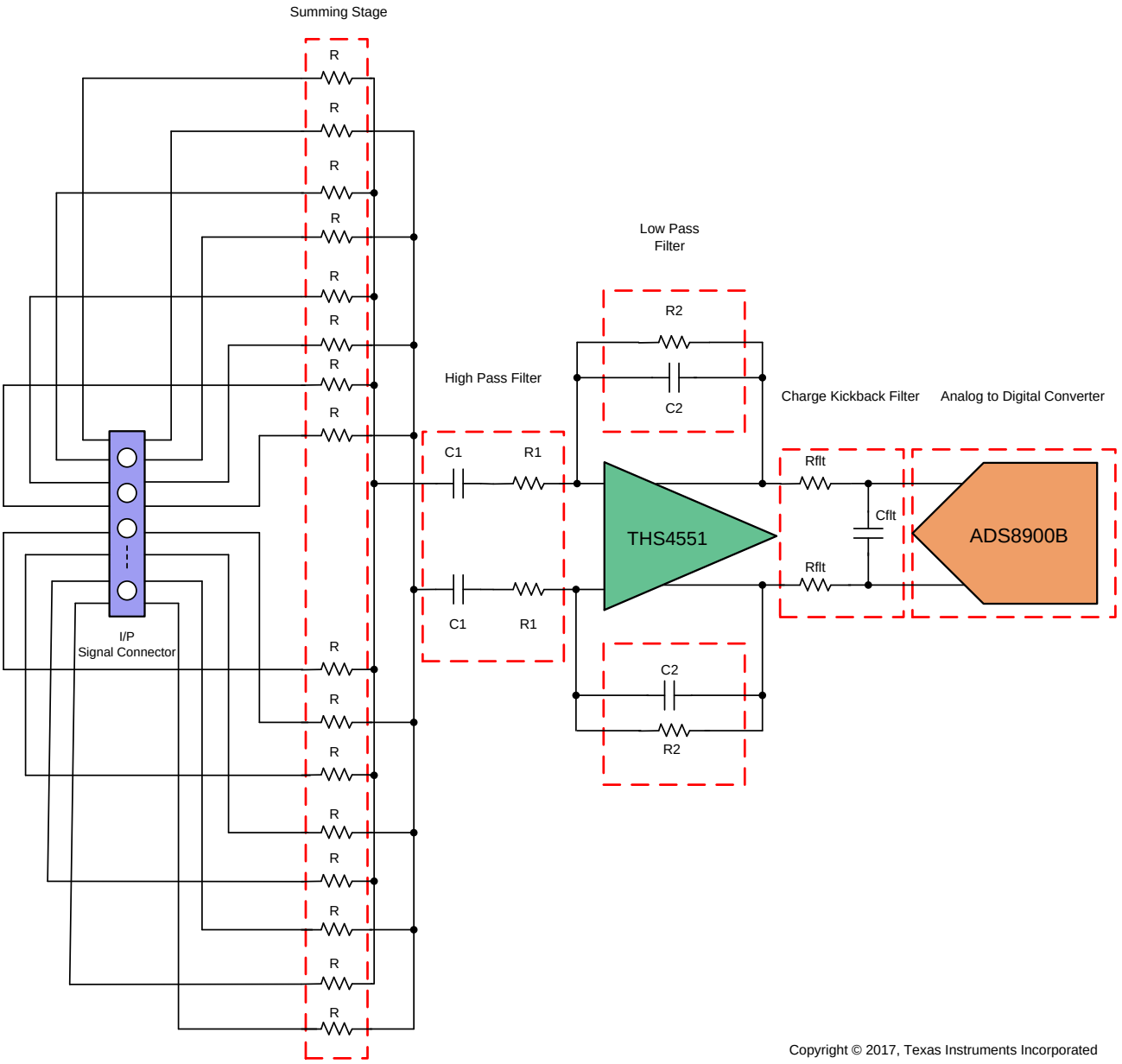


図 3. Summing Stage, Active Filter, ADC Driver, and Charge Kickback Filter Circuit

2.3.1.1 Summing Circuit and Gain Stage

Summing circuit is designed to sum all the I and Q voltage outputs from eight receive AFEs of ultrasound system. Each input signal is differential, and the same circuit is used for both I and Q signals. Assuming the same input is coming from the receive AFEs, the Thevenin equivalent of all summing resistor R (1 kΩ; see 図 3) is Rth 120 Ω (see 図 4). This Rth (120 Ω), R1 (887 Ω), and R2 (10 kΩ) forms a gain of 10 [R2 / (Rth + R1)]. In some applications if the input signal level is low, such a high gain is required.

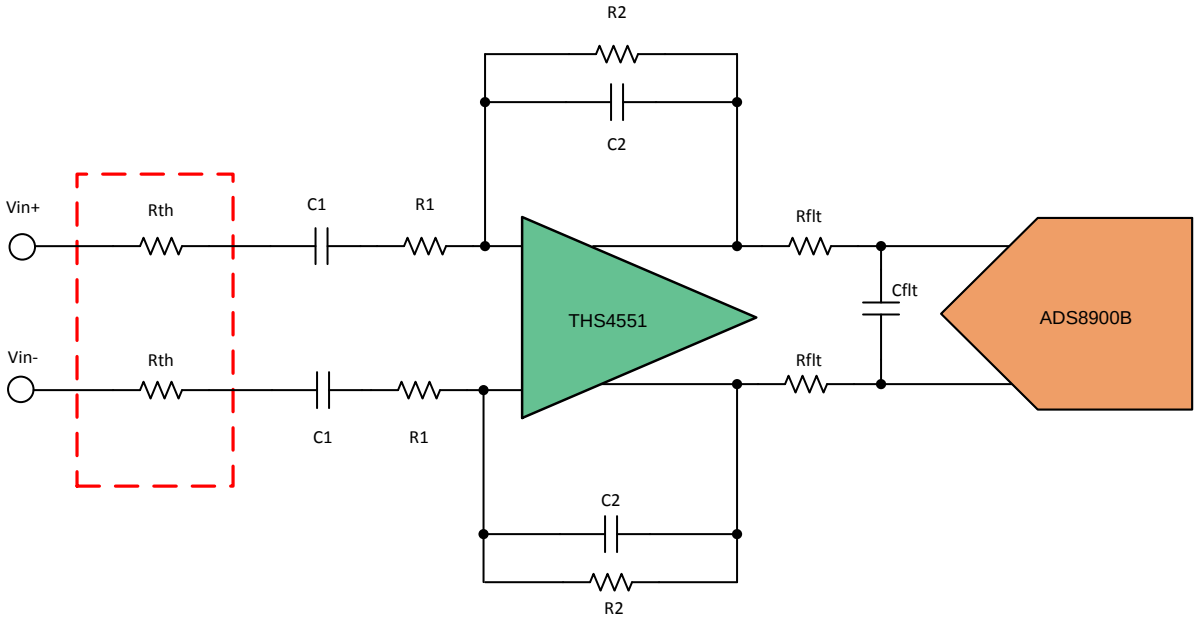


図 4. Thevenin Equivalent of Summing Stage

2.3.1.2 *Input High-Pass Band Limiting Filter*

In reference to 図 3, the high-pass filter, R1, and C1 are calculated for a 54-Hz, –3-dB cutoff frequency.

For RC filter cutoff frequency, use 式 1.

$$f_{-3dB\_RC\_CUTOFF} = \frac{1}{2\pi \times R1 \times C1} \quad (1)$$

Where:

- R1 = 887 Ω
- C1 = 3.3 µF

$$f_{-3dB\_RC\_CUTOFF} = \frac{1}{2\pi \times R1 \times C1} = \frac{1}{2 \times 3.14 \times 887 \times 3.3 \times 10^{-6}} = 54\ Hz$$

2.3.1.3 Input Low-Pass Band Limiting Filter

In reference to 図 3, the low-pass filter, R2, and C2 are calculated for 285 kHz, –3-dB cutoff frequency.

For RC filter cutoff frequency, use 式 2.

$$f_{-3dB\_RC\_CUTOFF} = \frac{1}{2\pi \times R2 \times C2} \quad (2)$$

Where:

- R2 = 10 kΩ
- C2 = 56 pF

$$f_{-3dB\_RC\_CUTOFF} = \frac{1}{2 \times 3.14 \times 10 \times 10^{3} \times 56 \times 10^{-12}} = 285\ kHz$$

2.3.1.4 Input Driver Circuit

2.3.1.4.1 Input Buffer Amplifier

The input driver circuit for a high-precision ADC consists of two main parts: a driving amplifier and a flywheel RC filter. The amplifier is used for signal conditioning of the input signal. The driving amplifier's low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched capacitor input stage of the ADC and functions as a charge kickback filter to band-limit the wideband noise.

The input op amp must support following key specifications:

1. RRIO
2. Low power, low noise
3. High, small-signal bandwidth with low distortion at high frequencies

The THS4551 is designed to drive precision (16-, 18- and 20-bit) SAR ADCs at sample rates up to 1 MSPS. The combination of low-output impedance (10 Ω at 10 kHZ to 1 MHz). low THD, low noise (3 nV/√Hz), and fast settling time (18-bit settling time: 4-V step, < 500 ns) make the THS4551 the ideal choice for driving the SAR ADC inputs. The THS4551 is a fully differential amplifier; hence, only one op amp is required to drive an ADC. The device also has independent control over output common mode. THS4551 provides a very good noise figure of 3 nV/√Hz, with single-ended op amps the noise figure will be 1.414 times the value specified for the op amp. In this TI Design, two THS4551 devices can be replaced with a single dual FDA THS4552. See the THS4552 datasheet[4] for more details.

2.3.1.4.1.1 Settling Time

For DC signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurate settling of the signal at the inputs of the ADC during the small acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier datasheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired 20-bit accuracy. Therefore, always verify the settling behavior of the input driver by TINA-TI™ SPICE-based simulations before selecting the amplifier.

In 図 5, C_{FLT} is connected as differential capacitor across the input of the ADC. This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample and-hold capacitors during the acquisition process. Generally, the value of this capacitor must be at least 20 times the specified value of the ADC sampling capacitance. For the ADS8900B, the input sampling capacitance is equal to 60 pF; therefore, it is recommended to keep greater than 1200 pF. The capacitor must be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, low-voltage coefficient, and stable electrical characteristics under varying frequency, and time. Besides reducing the sampling charge injection, the RC filter helps to band-limit the noise fed into the input of the ADC. See the *Precision Analog Applications Seminar*[2] for details on driving the SAR ADC.

図 5 shows the input circuit of a typical SAR ADC. During the acquisition phase, the SW switch closes and connects the sampling capacitor (C_{SH}) to the input driver circuit. This action introduces a transient on the input pins of the SAR ADC. An ideal amplifier with 0 Ω of output impedance and infinite current drive can settle this transient in zero time. For a real amplifier with non-zero output impedance and finite drive strength, this switched capacitor load may create stability issues.

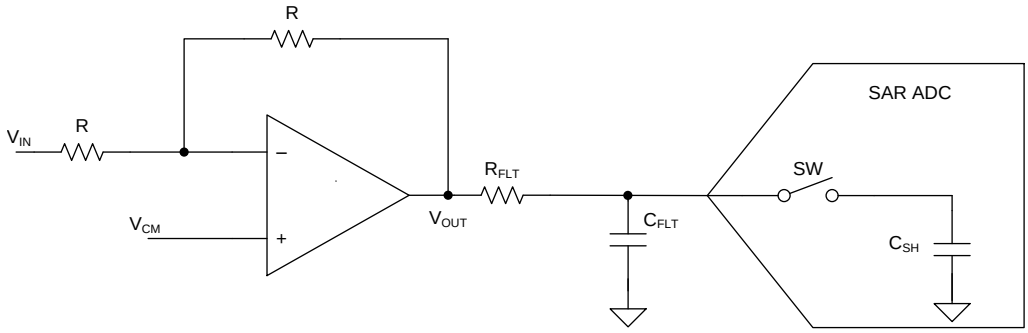


図 5. Input Sample and Hold Circuit for Typical SAR ADC

The RC charge kickback filter helps address these issues. The capacitor C_{FLT} helps reduce the sampling charge-kickback at the ADC input and provides a charge bucket to quickly charge the input capacitor C_{SH} during the sampling process.

When SW closes, the worst-case voltage difference between the sampling capacitor (C_{SH}) and the filter capacitor (C_{FLT}) is the full-scale input range supported by the SAR ADC (that is, V_{REF}). The charge required for the ADC sampling capacitor is given by 式 3.

$$Q_{SH} = C_{SH} \times Vref \tag{3}$$

As a general rule, the value of the capacitor C_{FLT} must be selected such that it provides this charge without dropping its voltage by more than 5% (see 式 4).

$$Q_{FLT} = C_{FLT} \times \Delta V_{FLT} \le C_{FLT} \times \left(0.05 \times V_{REF}\right) \tag{4}$$

By the principle of charge conservation, the charge required by the sampling capacitor must be equal to the charge provided by the filter capacitor. Using this principle, derive 式 5, 式 6, and 式 7.

$$Q_{SH} = Q_{FLT} \tag{5}$$

$$\rightarrow C_{SH} \times V_{REF} \le C_{FLT} \times \left(0.05 \times V_{REF}\right) \tag{6}$$

$$\rightarrow C_{FLT} \ge 20 \times C_{SH} \tag{7}$$

注: Driving capacitive loads can degrade the phase margin of the input amplifiers, thus, making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors (R_{FLT}) are used at the output of the amplifiers. A higher value of R_{FLT} is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion of the design.

2.3.1.4.1.2 RC Filter Passive Components Selection

The critical passive components are resistor (R_{FLT}) and capacitor (C_{FLT}) for RC filter. The resistor tolerance must be less than 1% because use of differential capacitor at input balances the effect due to any resistor mismatch. The type of capacitor should be COG (NPO) because this capacitor has high-Q and low-temperature coefficient and stable electrical characteristics over voltage, frequency, and time variations.

2.3.1.4.1.3 To Select C_{FLT}

The input capacitance for the ADS8900B is 60 pF. The filter capacitor C_{FLT} should be 20 times greater than the sampling capacitor of ADC (式 7).

$$C_{FLT} \geq 20 \times C_{SH} = 20 \times 60\ pF = 1.2\ nF \tag{8}$$

2.3.1.4.1.4 To Select R_{FLT}

Minimum value of R_{FLT} can be derived as 式 9.

$$R_{FLT} \geq \frac{R_0}{9} \tag{9}$$

Considering the effect of RC filter on op amp stability using A_{OL} response, the output resistance of THS4551 is R_o = 10 Ω and substituted in .

$$R_{FLT} \geq \frac{R_0}{9} = \frac{10}{9} = 1.1\ \Omega$$

So, the value of R_{FLT} can be chosen greater than 1.11 Ω.

The R_{FLT} and C_{FLT} are calculated for 15-MHz, –3-dB cutoff frequency with R_{FLT} and C_{FLT} value consideration. For the RC filter cutoff frequency, see 式 10.

$$f_{-3dB\_RC\_CUTOFF} = \frac{1}{2\pi \times C_{FLT} \times R_{FLT}} \tag{10}$$

Where:

- C_{FLT} = 2 nF
- f_{-3dB} = 15 MHz

$$R_{FLT} = \frac{1}{2 \times \pi \times C_{FLT} \times f_{-3dB\_RC\_CUTOFF}} \tag{11}$$

$$R_{FLT} = \frac{1}{2 \times 3.14 \times 2 \times 10^{-9} \times 15 \times 10^{6}} = 5.1\ \Omega$$

2.3.2 Analog-to-Digital Conversion

The ADS8900B is a fully-differential, 20-bit, 1-MSPS SAR ADC with integrated reference buffer, integrated LDO, and multiSPI digital interface. The SAR ADC provides true raw data with low latency and good SNR. For even higher SNR, an external digital filter can be used.

ADC SPI (multiSPI): The ADS8900B has integrated multiSPI that is backward compatible with the traditional SPI and configurable SDO lines (one, two, three, and four) . The configurable feature simplifies board layout, timing and firmware, and achieves high throughput at lower clock speeds, thus, allowing easy interface with embedded MCUs, DSPs, and FPGAs. 図 6 shows the logical connection for simultaneous I and Q sampling. 図 7 shows the configuration for independent I or Q channel sampling. Detailed information on multiSPI can be found in ADS8900B datasheets[5].

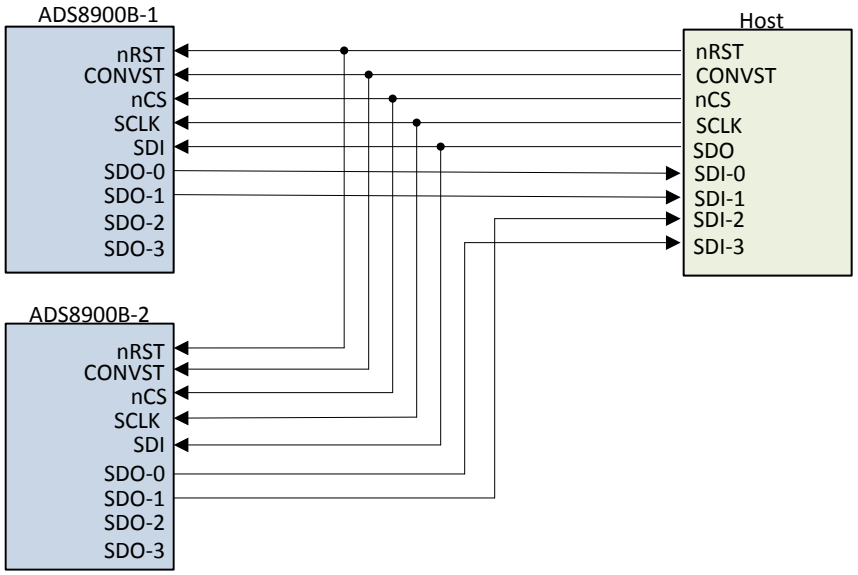


図 6. MultiSPI Configuration for Simultaneous I and Q Sampling

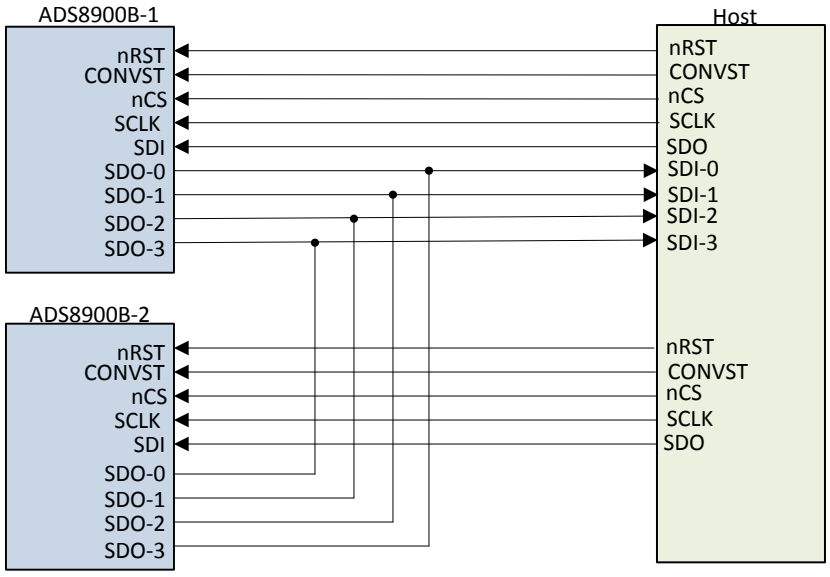


図 7. MultiSPI Configuration for Independent I or Q Channel Sampling

2.3.3 Reference Voltage Generation and CM Voltage Generation

The onboard 5-V reference REF5050 (ultra-low noise, low drift, and high precision) generates both ADC common-mode voltage and ADC reference voltage. To exercise the complete dynamic range of the ADS8900B, the common-mode voltage at the ADS8900B inputs is established at a value of 2.5 V (5 V / 2) by using the VCOM pins of the THS4551 amplifier's onboard reference REF5050. The reference buffer can be realized using a single amplifier having high bandwidth, low open-loop output impedance, low offset, and low drift specifications, as shown in 図 8. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 160 Hz for CM voltage generation.

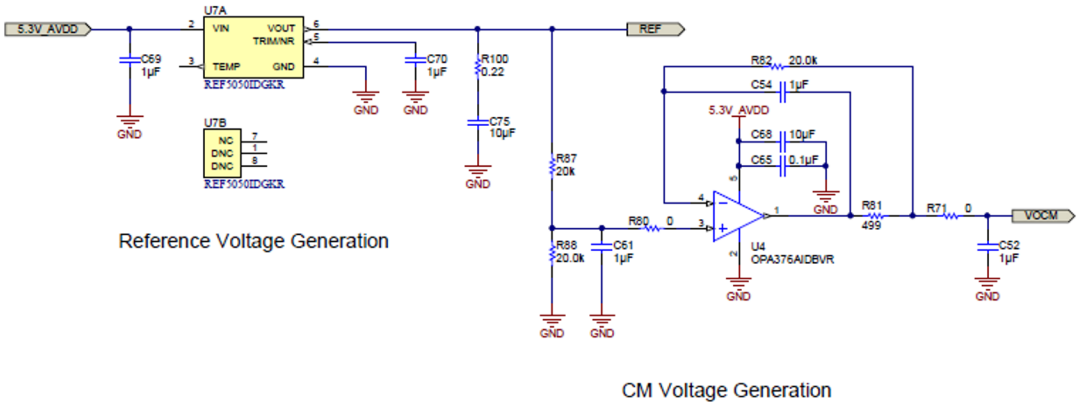


図 8. Reference Voltage Generation and CM Voltage Generation

2.3.4 Power Supply

The TPS7A88 is selected is to convert 6-V input to 5.3 V and 3.3 V. With The TPS7A88's flexibility of having two independent LDOs, it is possible to generate a voltage output of 5.3 V for the analog section and 3.3 V for the digital section of the ADC. The TPS7A88 has 1-A, low noise (3.8 μV_{RMS}), and wideband PSSR capability, which makes it well suited for this TI Design.

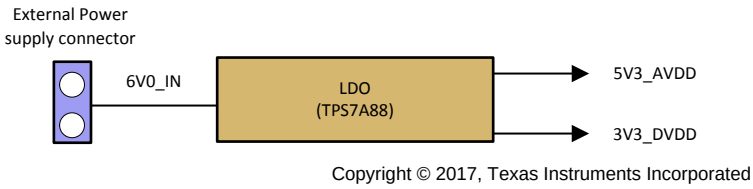


図 9. The Power Tree

The EEPROM on the ADS8900BEVM uses a 3.3-V power supply generated directly by the precision host interface (PHI). The ADC and analog input drive circuits are powered by the TPS7A88 onboard, which is a low-noise linear regulator that uses the 6-V input to generate a cleaner 5.3-V and 3.3-V output. The 3.3 V is supplied to the digital section of the ADC. The power supply for each active component on board is bypassed with a ceramic capacitor placed close to that component.

To get better noise rejection, ferrite beads are used at the output of both 5V3 and 3V3 power supplies.

2.3.5 Host Interface

PHI is TI's SAR ADC evaluation platform, which supports the entire TI SAR ADC family. By using PHI, the TIDA-01351 easily communicates with the host PC using a USB interface. PHI supports the ADS8900B multiSPI and onboard configuration I²C EEPROM interface. PHI GUI software can be used to evaluate both AC and DC parameter of the ADS8900B. For more information on PHI, refer to the ADS8900BEVM-PDK quick start guide[6]. The TIDA-01351 board along with the PHI controller board enables the accompanying computer software to communicate with the ADC over USB for data capture and analysis. The PHI board primarily serves three functions:

- Provides a communication interface from the TIDA-01351 board to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS8900B
- Supplies power to all EEPROM on TIDA-01351 board

The TIDA-01351 board interfaces with the PHI that, in turn, communicates with the computer over USB. There are two devices on board with which the PHI communicates: the ADS8900B ADC (over SPI or multiSPI) and the EEPROM (over I^2C). Once the hardware is initialized, the EEPROM is no longer used.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

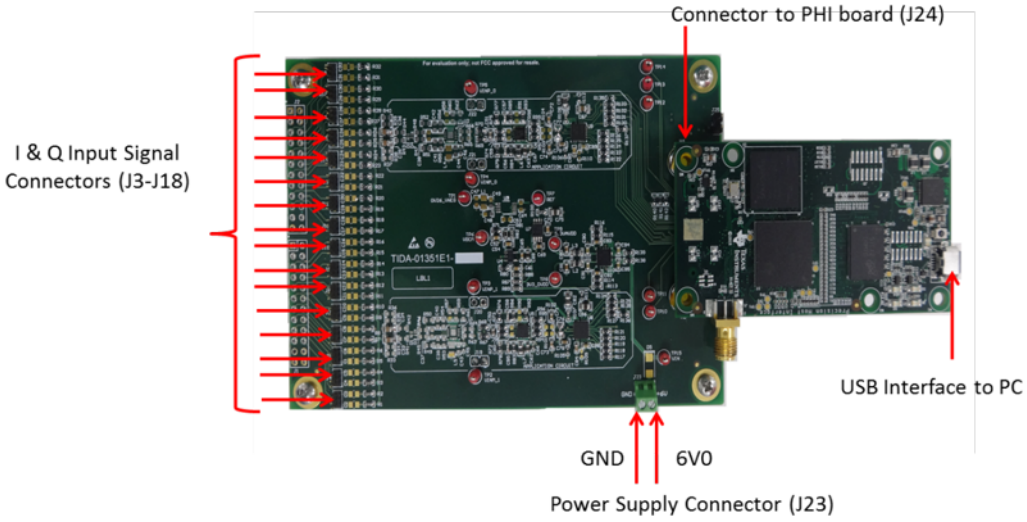


図 10. TIDA-01351 PCB Connector Configuration

- Power supply connector (J23): This pin is used to connect the input power supply. Set power supply to 6 V with 1-A current limit.
- Input signal (J3-J18): Eight differential input signals are fed to the board using the connectors from J3 to J18. These signals will be summed, filtered, and amplified before digitizing.
- PHI board interface connector (J24): The PHI interface connector uses the TIDA-01351 to communicate with the host through USB interface. By using PHI, the TIDA-01351 easily communicates with the host PC using a USB interface. PHI supports the ADS8900B multiSPI and onboard configuration I^2C EEPROM interface.
- Programming interface: The PHI interface connector uses the TIDA-01351 to communicate with the host through USB interface. By using PHI, the TIDA-01351 easily communicates with the host PC using a USB interface. PHI supports the ADS8900B multiSPI and onboard configuration I^2C EEPROM interface. See 2.3.5 for more details.

3.1.2 Software

3.1.2.1 ADS8900BGUI Panel

The ADS8900B GUI software, which is based on the LabVIEW™ platform, validates the reference design.

図 11 and 図 12 show the available test options in ADS8900B GUI.

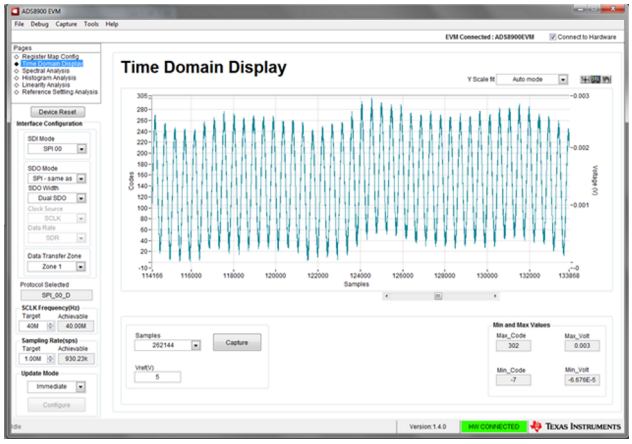


図 11. ADS8900B GUI Demonstrate AC Parameter—Time Domain Display

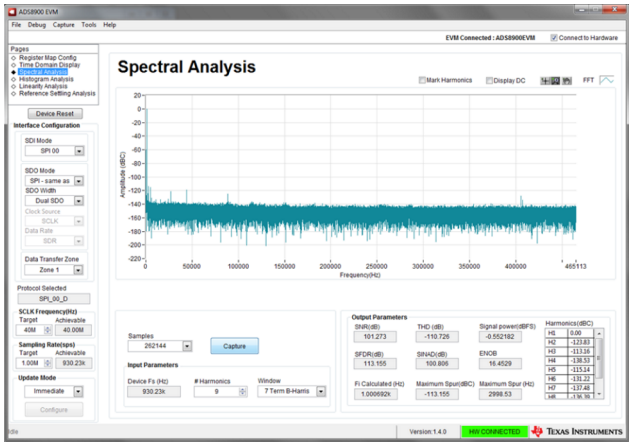


図 12. ADS8900B GUI Demonstrate AC Parameter—Spectral Analysis

The ADS8900B GUI can be used to validate the following system key specifications:

1. Linearity analysis
   - DNL
   - INL
   - Accuracy
2. Histogram analysis
   - Effective resolution
3. Spectral analysis
   - SNR
   - THD
   - SFDR
   - SINAD
   - ENOB

ADS8900B GUI software can be found at the ADS8900B product folder.

3.1.2.2 ADS8900B Software Start-up Instruction

1. Download the latest version of the ADS8900B EVM GUI Installer[7] from the *Tools and Software* folder of the ADS8900B, and run the GUI installer to install the EVM GUI software on the user's computer.
2. Accept the license agreements and follow the on-screen instructions to complete the installation.
3. See the *ADS8900BEVM-PDK User's Guide*[8] to install the software GUI.
4. See the *ADS8900BEVM-PDK User's Guide*[8] for GUI settings for ADC control and results capture.

3.2 Testing and Results

3.2.1 Test Setup

図 13 shows the TIDA-01351 test setup to validate the ultrasound CW voltage output signal conditioning unit. The test must evaluate the performance of a high-speed (1-MSPS) and high-resolution (20-bit) system that is compliant with testing requirements. The setup has an audio precision AP2700 waveform generator, which is capable of generating a sine pattern with a signal frequency up to 200 kHz. The device requires high precision with very-low ripple power supply to power entire system. This design requires 6-V DC at 43 mA with high precision and low-ripple power. The 6-V DC voltage is generated using Keithley triple output power supply (2230G). The power supply is capable of generating up to 30 V with 0.03% voltage accuracy and 0.1% current accuracy with simultaneous voltage and current indication. The data capturing is established using USB 2.0 interface.

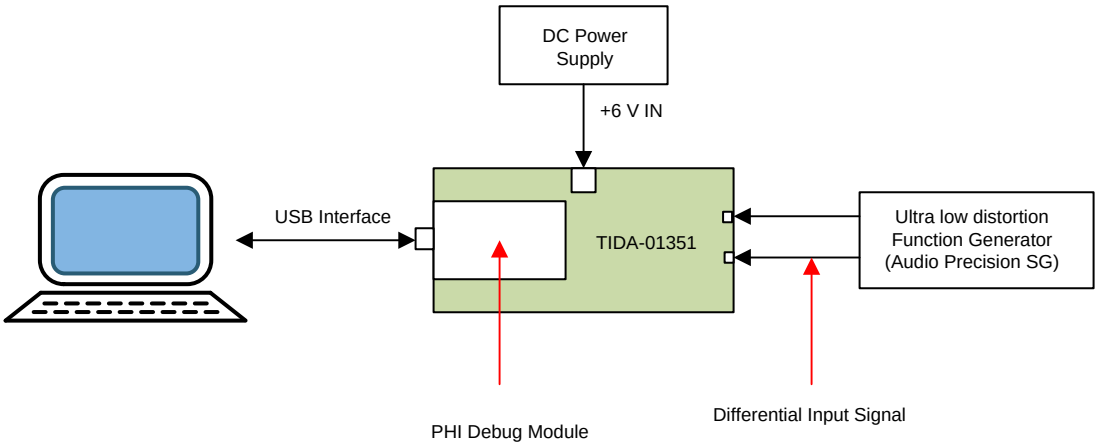


図 13. TIDA-01351 Test Setup

図 14 shows the connections used in testing the TIDA-01351

The ADS8900B GUI software must be installed in the host computer before testing.

1. Plug the PHI interface board to the connector J24.
2. Connect 6-V DC of power to the J23 connector. Ensure the positive terminal is connected to the positive input of J23 and the negative terminal is connected to the negative input of J23.
3. Connect the differential output of function generator to the differential input terminal (J3 connector only) of the TIDA-00732 board (for a 2-kHz input signal frequency, 500 mVp-p). The test was done by using only one differential input for both I and Q channel. Hence, the resistors, R (図 3), used on the board was 120 Ω, which is the Thevenin equivalent of eight 1-kΩ resistors used for the eight different channels. The identical circuit was used for both I and Q signals. Also, make sure both differential signals are balanced and configured, as shown in 表 4.

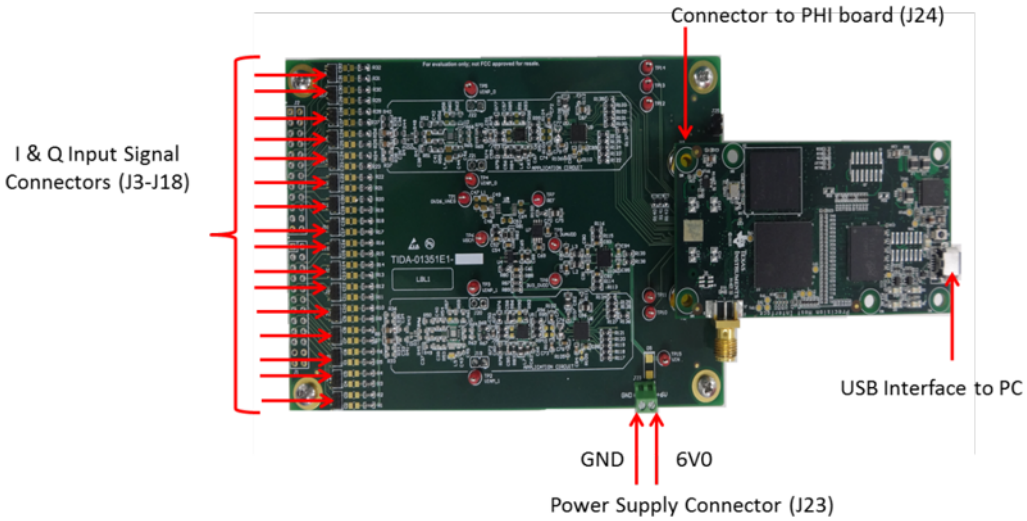


図 14. TIDA-01351 Control Through PHI Controller Using ADS8900B GUI

表 4. Function Generator Settings

FUNCTION GENERATOR	
Pattern	Sine
Voltage	500 mVp-p at 2 kHz, 20 kHz 10 uVp-p at 2 kHz
Frequency	2 kHz, 20 kHz
Source impedance	40 Ω

To evaluate the performance of TIDA-01351, the following test cases were created:

1. Generate as sine wave of 500 mVp-p (adjust to cover full dynamic input range, 2 kHz and 20 kHz).
2. Run ADS8900B GUI.
3. Capture the spectral analysis results (SNR, THD, and ENOB) and time domain display results.

The test results are taken for 2-kHz and 20-kHz input frequency for a 500-mVp-p input voltage and a 2-kHz input frequency for 10 µVp-p.

3.2.2 Test Data

3.2.2.1 ADC Sensitivity Measured With 2-kHz Input Signal

図 15 shows the ADC's minimum detectable capability. The capability was captured with a 2-kHz input signal with a gain of 10. This test confirms that ADC can discern a 10-µVp-p signal.

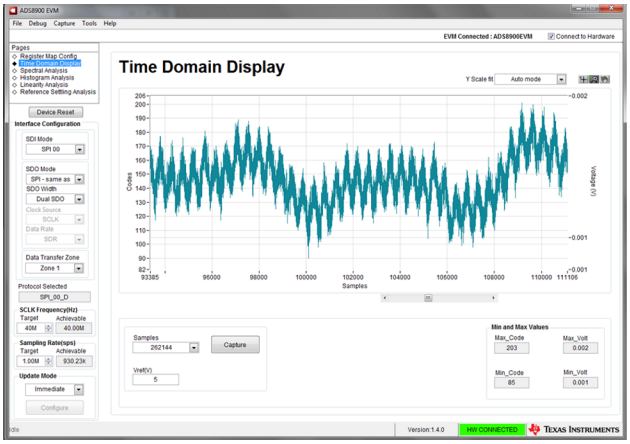


図 15. ADC Sensitivity Measured With 10-µVp-p Input Signal at 2 kHz

3.2.2.2 ADC AC Performance (SNR and ENOB) With Gain of 1

図 16 shows the ADC performance (SNR, THD, and ENOB) with a gain of 1 at 2 kHz. The SNR is 101.2 dB at a high speed of 1 MSPS, ENOB is 16.45.

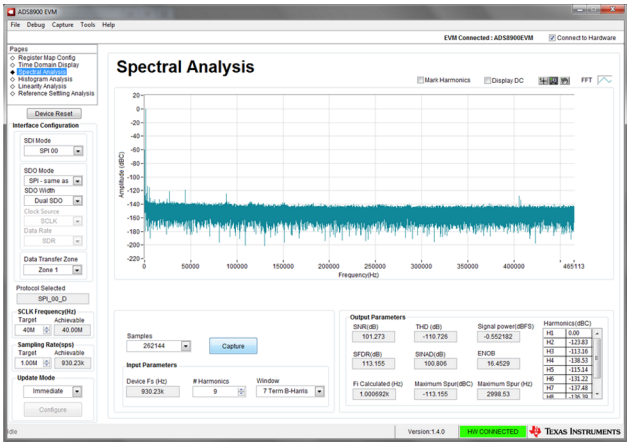


図 16. ADC Performance at 2-kHz Input With Gain of 1

3.2.2.3 ADC AC Performance (SNR, THD, and ENOB) With Gain of 10

図 17 shows the ADC performance (SNR, THD, and ENOB) with a gain of 10 at 2 kHz. The SNR is 94.8 dB at a high speed of 1 MSPS, ENOB is 15.44, and THD is equal to –113.1 dB.

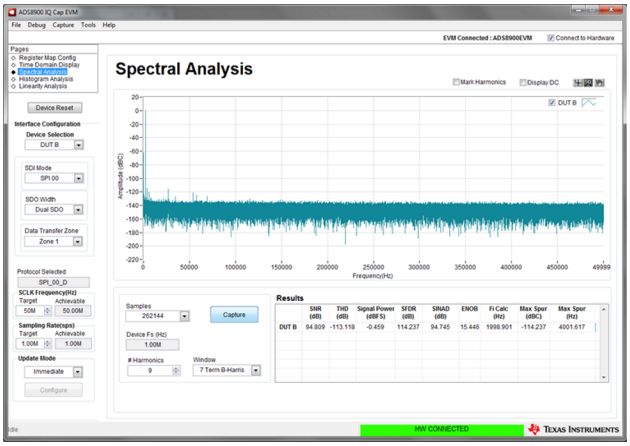


図 17. ADC AC Performance With a Gain of 10 at 2 kHz

図 18 shows the ADC performance (SNR, THD, and ENOB) with a gain of 10 at 20 kHz. The SNR is 92.1 dB at a high speed of 1 MSPS, ENOB is 15.01, and THD is equal to 110.12 dB.

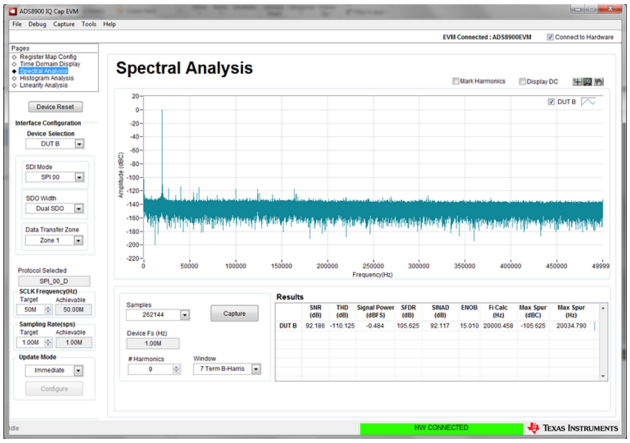


図 18. ADC AC Performance With a Gain of 10 at 20 kHz

図 19 shows the phase-shifted time domain display of I and Q signals. One channel is given an attenuation and phase shift compared to the other channel.

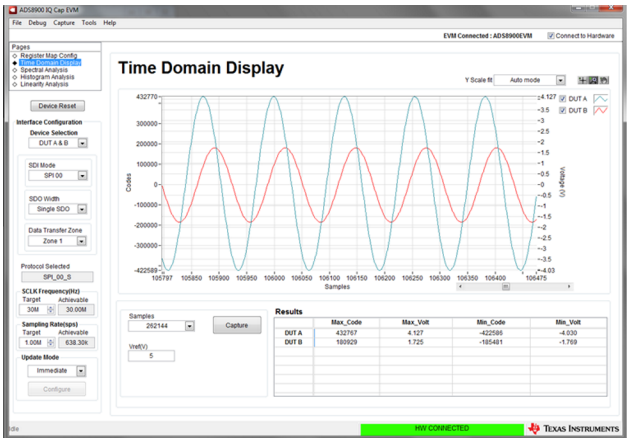


図 19. Time Domain Display of I and Q Signals (With Attenuation and Phase Shift Given on One Channel)

図 20 shows the time domain display of 20-kHz I and Q signals. Both signals are in phase and have the same gain.

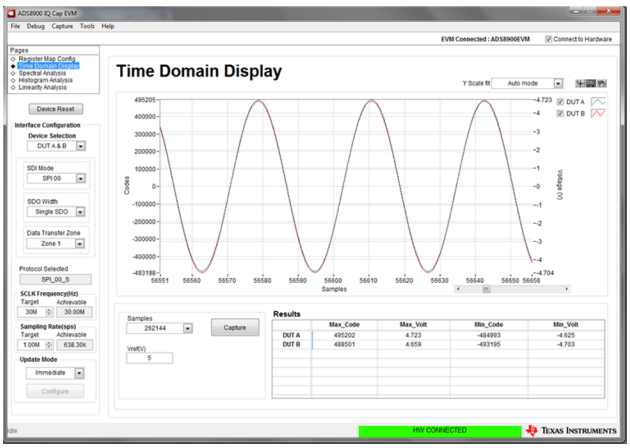


図 20. Time Domain Display of I and Q Signals at 20 kHz

図 21 shows the ADC performance (SNR, THD, and ENOB) with simultaneous sampling of I and Q signals (Gain = 10 at 20 kHz). The SNR is 89.4 dB and 89.9 dB at a high speed of 1 MSPS, ENOB is 14.5 and 14.6, and THD is equal to –104.5 dB and –107.1 dB.

図 21. ADC AC Performance With Gain of 10 at 20 kHz (Same Gain on Both Channels)

図 22 shows the time domain display of 2 kHz I and Q signals. Both signals are in phase and have the same gain.

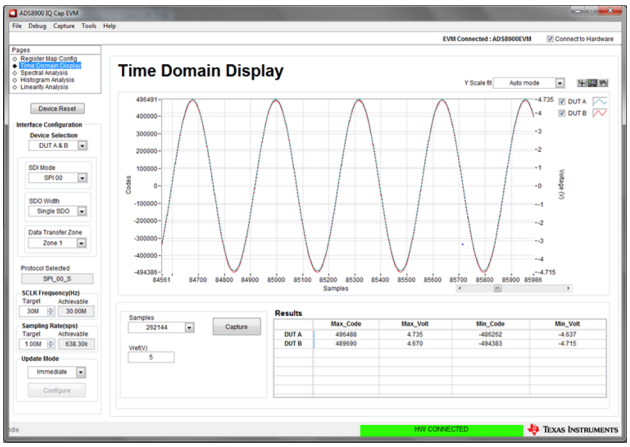


図 22. Time Domain Display of I and Q signals at 2 kHz

図 23 shows the ADC performance (SNR, THD, and ENOB) with simultaneous sampling of I and Q signals (Gain = 10 at 2 kHz). The SNR is 91.3 dB and 92.1 dB at a high speed of 1 MSPS, ENOB is 14.8 and 14.9, and THD is equal to –105.4 dB and 108.5 dB.

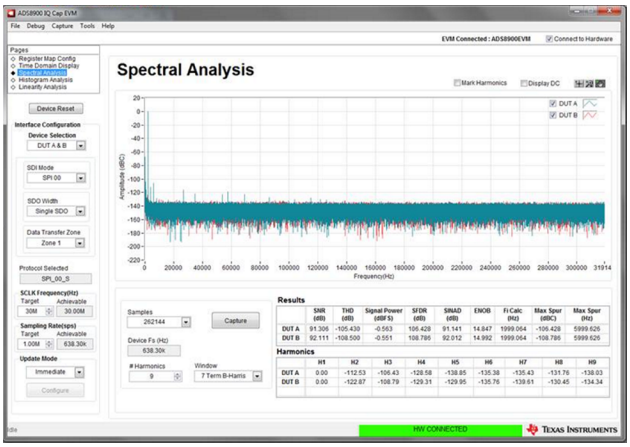


図 23. ADC Performance With Gain of 10 at 2 kHz (Same Gain on Both Channels)

図 24 shows time domain display of I and Q signals at 20 kHz. One channel is given twice the gain compared to the other channel.

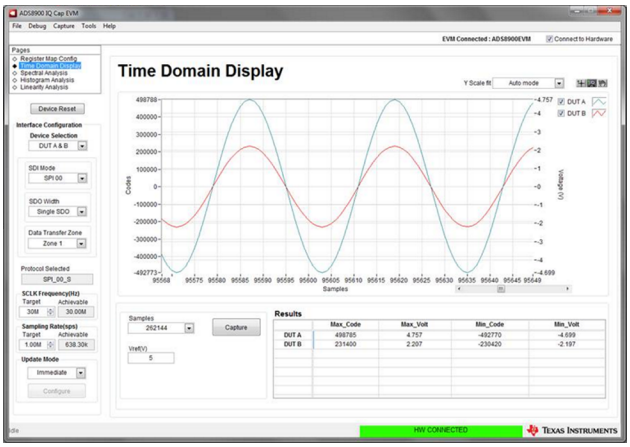


図 24. Time Domain Display of I and Q Signals at 20 kHz (One Channel is Given Half of the Gain Compared to the Other Channel)

図 25 shows time domain display of I and Q signals at 2 kHz. One channel is given half of the gain compared to the other channel.

図 25. Time Domain Display of I and Q Signals at 2 kHz (One Channel is Given Half of the Gain Compared to the Other Channel)

図 26 shows the ADC performance (SNR, THD, and ENOB) with simultaneous sampling of I and Q signals (gain = 10 at 2 kHz) using the 18-bit ADC ADS8910B. The SNR is 94.5 dB and 94.1 dB at a high speed of 1 MSPS, ENOB is 15.3 and 15.3, and THD is equal to –112 dB and –115 dB.

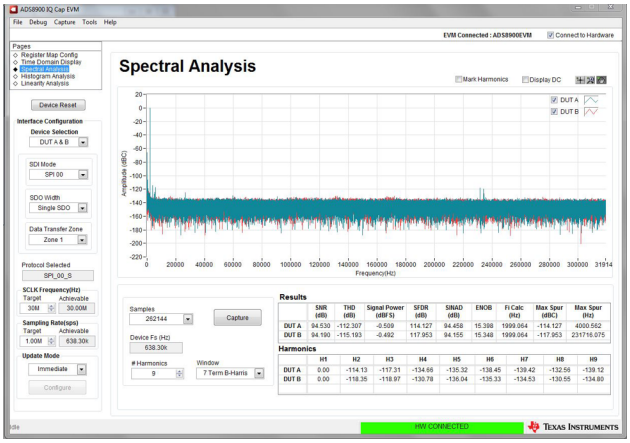


図 26. ADC AC Performance With a Gain of 10 at 2 kHz Using 18-Bit ADS8910B

図 27 shows the ADC performance (SNR, THD, and ENOB) with simultaneous sampling of I and Q (gain = 10 at 20 kHz) using the 18-bit ADC ADS8910B. The SNR is 88.8 dB and 88.7 dB at a high speed of 1 MSPS, ENOB is 14.4 and 14.4, and THD is equal to –111 dB and –114 dB.

図 27. ADC AC Performance With a Gain of 10 at 20 kHz Using 18-Bit ADS8910B

図 28 shows the ADC performance (SNR, THD, and ENOB) with simultaneous sampling of I and Q (gain = 10 at 2 kHz) using the 16-bit ADC ADS8920B. The SNR is 92.7 dB and 92.6 dB at a high speed of 1 MSPS, ENOB is 15.1 and 15.0, and THD is equal to –112 dB and –115 dB.

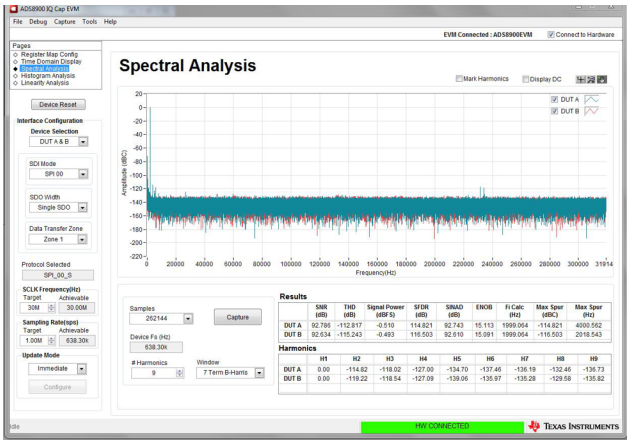


図 28. ADC AC Performance With a Gain of 10 at 2 kHz Using 16-Bit ADS8920B

図 29 shows the ADC performance (SNR, THD, and ENOB) with simultaneous sampling of I and Q (gain = 10 at 20 kHz) using the 16-bit ADC ADS8920B. The SNR is 88.4 dB and 88.2 dB at a high speed of 1 MSPS, ENOB is 14.3 and 14.3, and THD is equal to –111 dB and –114 dB.

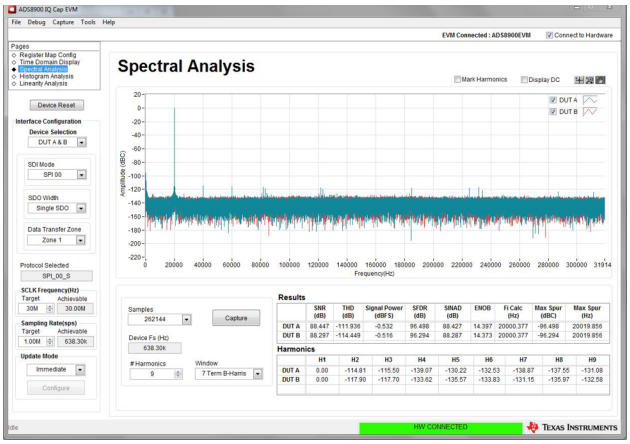


図 29. ADC AC Performance With a Gain of 10 at 20 kHz Using 16-Bit ADS8920B

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01351.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01351.

4.3 PCB Layout Recommendations

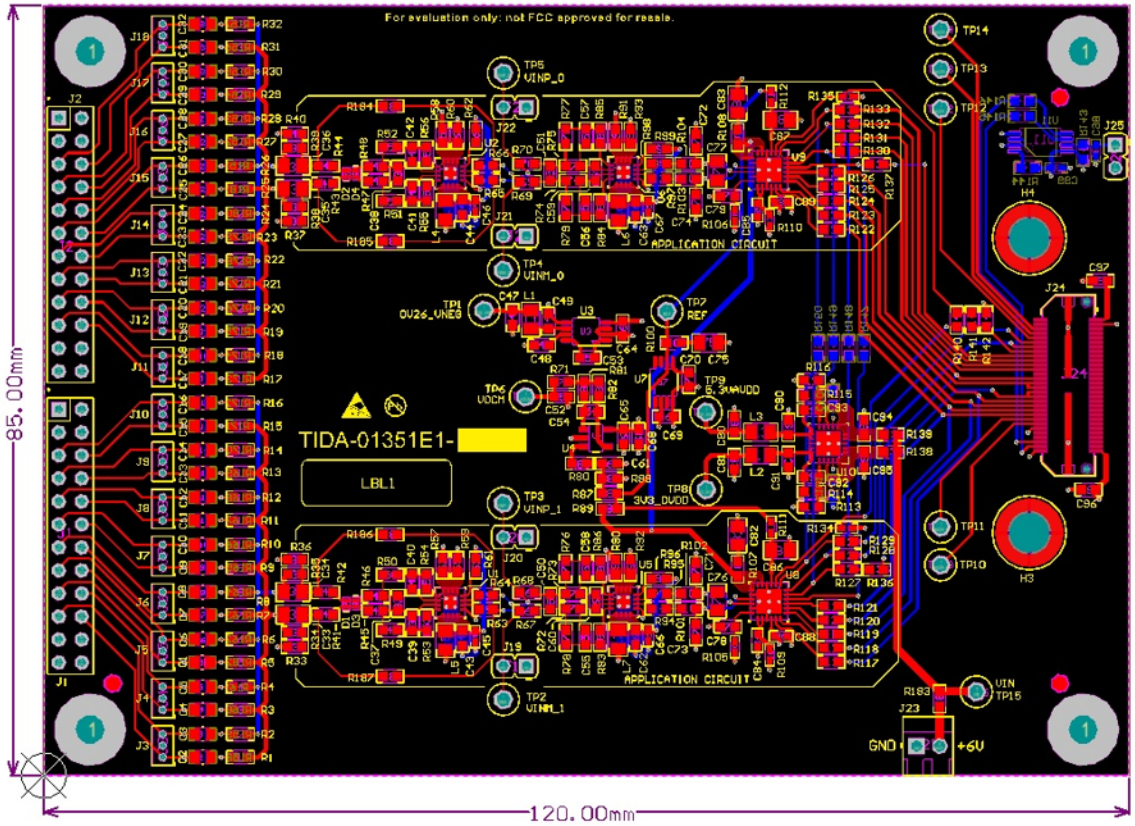


図 30. TIDA-01351 Layout Recommendations

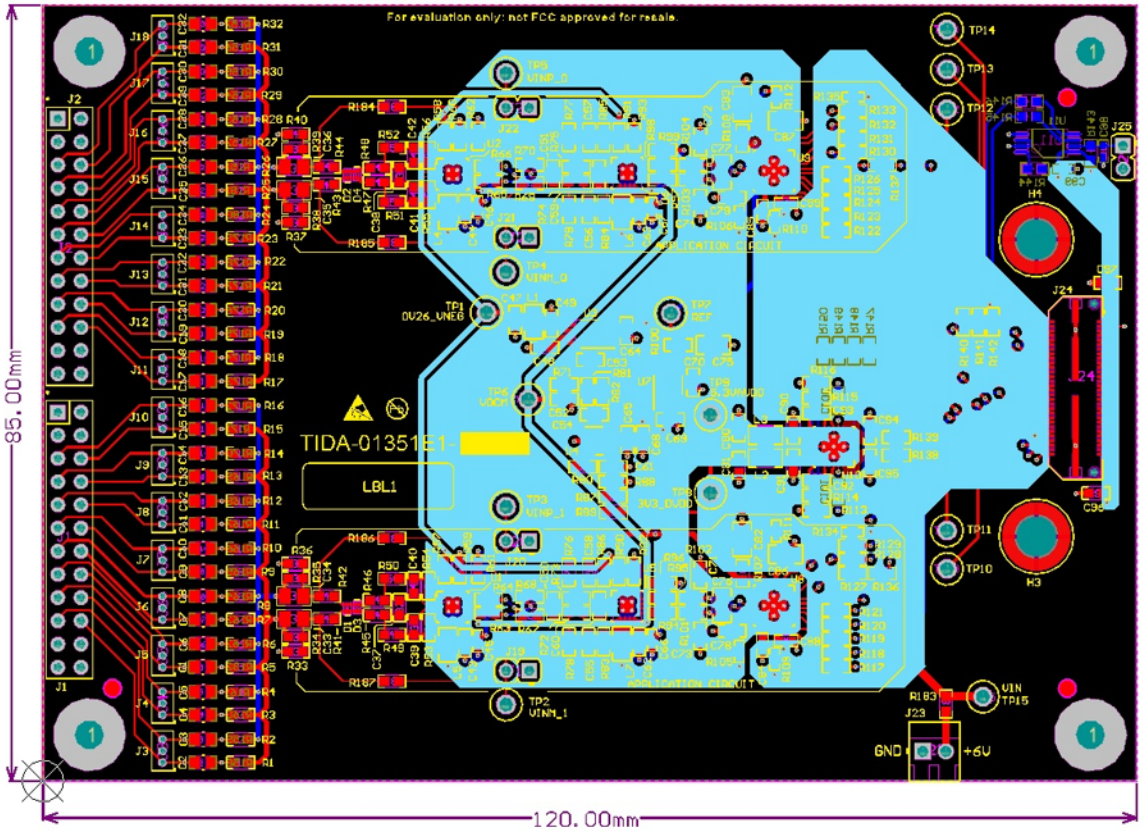


図 31. TIDA-01351 Power Supply Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01351.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01351.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01351.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01351.

5 Software Files

To download the software files, see the design files at TIDA-01351.

6 Related Documentation

1. Texas Instruments, *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise*, TIPD115 Design Guide (SLAU515)
2. Texas Instruments, *Seminars View Precision Analog Applications Seminar*, Seminar (SLYP166)
3. Texas Instruments, *WEBENCH Design Center*
4. Texas Instruments, *THS4552 Dual-Channel, Low-Noise, Precision 150-MHz, Fully Differential Amplifier*, THS4552 Datasheet (SBOS831)
5. Texas Instruments, *ADS890xB 20-Bit, High-Speed SAR ADCs With Integrated Reference Buffer, Integrated LDO, and multiSPI Digital Interface*, ADS8900B, ADS8902B, ADS890B Datasheet (SBAS728)
6. Texas Instruments, *Quick Start Guide: ADS8900BEVM-PDK*, Quick Start (SLYU041)
7. Texas Instruments, *ADS8900B EVM GUI Installer*, Software (SBAC156)
8. Texas Instruments, *ADS8900BEVM-PDK User's Guide*, User's Guide (SBAU269)

6.1 商標

7 About the Authors

LENI SKARIAH is a systems engineer at Texas Instruments, where she is responsible for developing subsystem design solutions for the Medical, Healthcare and Fitness sector. Leni brings her experience in precision analog and mixed signal designs to this role. Leni earned her Bachelor of Technology in Electronics and Communication Engineering from the University of Kannur and her Master of Technology in Digital Electronics and Communication Systems from Visvesvaraya Technological University, Karnataka.

SANJAY PITHADIA is a systems engineer at Texas Instruments, where he is responsible for developing subsystem design solutions for the Medical, Healthcare and Fitness sector. Sanjay has been with TI since 2008 and has been involved in designing products related to energy, smart grid, industrial motor drives, and medical imaging. Sanjay brings his experience in analog design, mixed signal design, industrial interfaces, and power supplies to this role. Sanjay earned his Bachelor of Technology in Electronics Engineering at VJTI, Mumbai.

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (June 2017) から **Revision B** に変更 **Page**

- ADS8910Bを「リソース」に 追加 1
- ADS8920Bを「リソース」に 追加 1
- 「特長」で、「20ビット、1MSPSのSAR ADC (ADS8900B)を使用し、1ppmのINLと、104.5dBのSNRで設計」を「ADS89x0B (20/18/16ビット)を使用し、1ppmのINLと、104.5dBのSNRで設計」に 変更 1
- Table 2: *AFEs Compatible With TIDA-01351* 追加 4
- Table 3: *Comparison of TI SAR ADC Performance versus Resolution* 追加 4
- Figure 26: *ADC AC Performance With a Gain of 10 at 2 kHz Using 18-Bit ADS8910B* 追加 28
- Figure 27: *ADC AC Performance With a Gain of 10 at 20 kHz Using 18-Bit ADS8910B* 追加 29
- Figure 28: *ADC AC Performance With a Gain of 10 at 2 kHz Using 16-Bit ADS8920B* 追加 29
- Figure 29: *ADC AC Performance With a Gain of 10 at 20 kHz Using 16-Bit ADS8920B* 追加 30

2016年12月発行のものから更新 **Page**

- structure to fit current style guide 変更 2

TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関係する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、あるいはTIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。