参考資料

TI Designs: TIDA-01427
超音波用の2.3nV/√Hz、差動、時間ゲイン制御DACのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインでは、複数のAFEデバイスを並列構成で駆動するための、時間変位制御電圧(V_{CNTL})を生成するため使用される、差動信号チェーンを紹介します。TIの医療向け超音波用の低ノイズ・フロントエンド(AFE)には、時間ゲイン制御(TGC)機能があり、超音波アプリケーションで可能な最良の信号対雑音比(SNR)を達成するため役立ちます。このリファレンス・デザインでは、デュアルのマルチプライDAC (DAC8802)に続けて電流/電圧コンバータ(OPA2209)を使用し、20Vのスイングを生成します。この20Vスイングは、複数の帰還フィルタ(THS4130)によりフィルタ処理されてから、パッシブ・アッテネータにより1.5Vに減衰されます。このデザインは、±15または5V電源を使用して駆動できます(オンボードの Fly-Buck™コンバータ LM5160により、5V入力が±15Vレールに変換されます)。TPS7A39およびTPS7A47を使用して、信号チェーン全体にわたってクリーンな電源が生成されます。DACの±10V基準電圧は、REF5010およびOPA2209を使用して生成されます。

リソース

TIDA-01427	デザイン・フォルダ
DAC8802	プロダクト・フォルダ
OPA2209	プロダクト・フォルダ
THS4130	プロダクト・フォルダ
TPS7A39	プロダクト・フォルダ
TPS7A47	プロダクト・フォルダ
REF5010	プロダクト・フォルダ
LM5160	プロダクト・フォルダ

特長

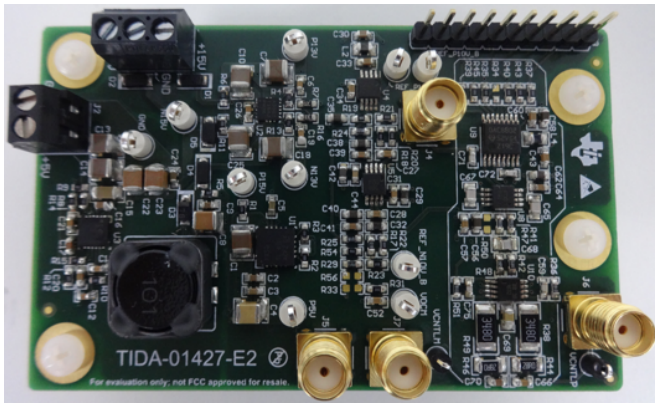
- 低ノイズ(2.3nV/√Hz)、差動TGC信号により、TIのAFE58xxシリーズのデバイスは小さな振幅の信号を増幅し、超音波画像処理でより深い貫通深度を実現可能
- AFEが低ノイズでデータを解決できるため、高解像度の超音波画像を生成
- 信号チェーン全体の伝搬遅延が5µs未満で、システムの総合的な応答時間が短縮
- fc = 150kHzの、2次バターワース・アクティブ・ローパス・フィルタにより、制御信号がスムーズに遷移可能
- 最大64チャネル以上のAFEを駆動可能
- 出力同相電圧を0～2.5Vに設定できるため、各種の制御電圧要件を持つAFEに対応可能

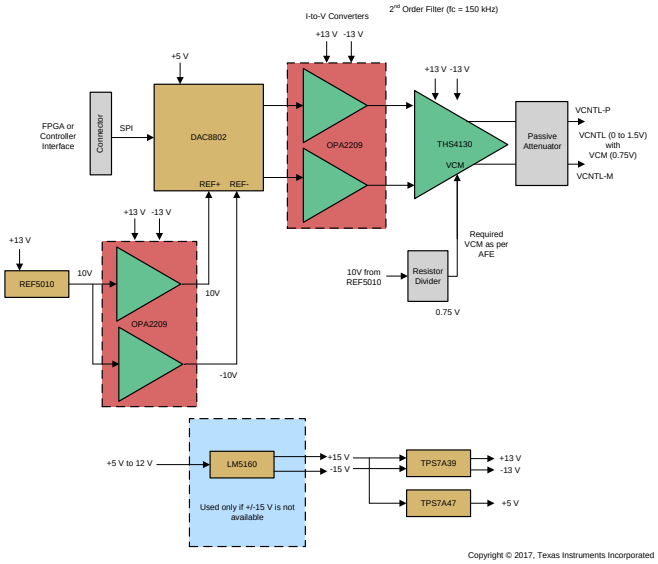
アプリケーション

- 携帯用、ミドルエンド、ハイエンド、最高級の各種医療用超音波スキャナ
- ソナー受信機
- レーダー受信機

TI E2E™ Community

E2Eエキスパートに質問





1 System Description

This reference design realizes a fully differential signal chain circuit for driving a TGC signal for ultrasound AFEs.

Medical ultrasound imaging is a widely-used diagnostic technique that enables visualization of internal organs, their size, structure, and blood flow estimation. An ultrasound system uses a focal imaging technique that involves time shifting, scaling, and intelligently summing the echo energy using an array of transducers to achieve high imaging performance. The concept of focal point imaging provides the ability to focus on a single point in the scan region. By subsequently focusing at different points, an image is assembled. When initiating an imaging, a pulse is generated and transmitted from multiple transducer elements. The pulse, now in the form of mechanical energy, propagates through the body as sound waves, typically in the frequency range of 1 to 15 MHz. The sound waves are attenuated as they travel through the objects being imaged. Most medical ultrasound systems use the reflection imaging mode. As the signal travels, portions of the wave front energy are reflected back towards the transducer.

Sonar imaging equipments transmit sound pulses and convert the returning echoes into digital images, much like a medical ultrasound sonogram. The advantage is that they can "see" what is going on through dark or turbid (cloudy) water in zero visibility conditions. Because the principle of operation is the same as ultrasound scanners, the TGC requirements are also similar.

1.1 Key System Specifications

表 1 shows different characteristics and their specifications of the reference design board.

表 1. Key System Specifications for TIDA-01427 Board

CHARACTERISTICS	SPECIFICATIONS
Input voltage (V_{IN})	±15 V or 5 V
V_{CNTL} (V_{CNTLP} – V_{CNTLM})	0 to 1.5 V
Common-mode voltage for V_{CNTL}	0.75 V
Output voltage noise	< 2.5 nV/√Hz
Reference for DAC1	10 V
Reference for DAC2	–10 V
Digital supply (VDD) for DACs	5 V
Positive supply for op amps	13 V
Negative supply for op amps	–13 V
MFB low-pass filter (LPF) order	Second order
MFB LPF cutoff frequency	150 kHz
Digital-to-analog converter (DAC) interface	SPI
Interface to FPGA or controller	10-pin connector

2 System Overview

2.1 Block Diagram

The system block diagram for this reference design is shown in 図 1.

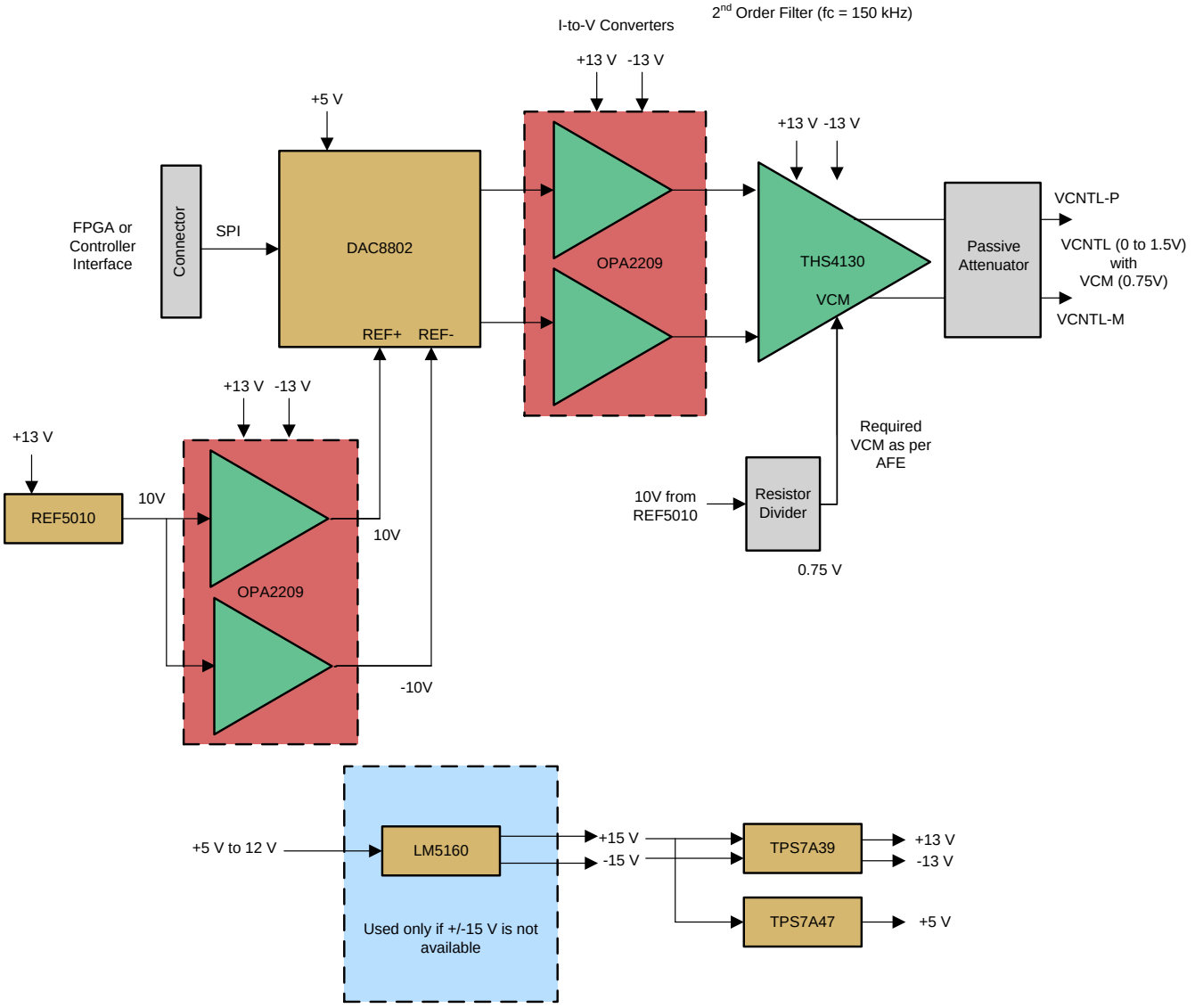


図 1. System Level Block Diagram of TIDA-01427

TI's low-noise AFEs for medical ultrasound have a TGC feature that helps achieve the best possible SNR for ultrasound applications. This reference design provides a solution for fully differential signal chain used for generating a time-varying control voltage (V_{CNTL}) to drive multiple AFE receiver chips in a parallel configuration.

This differential reference design uses dual multiplying DACs (DAC8802) followed by current-to-voltage converters (OPA2209) to generate a 20-V swing. After filtering this 20-V swing with a multiple feedback filter (THS4130), the swing is attenuated to 1.5 V using a passive attenuator. The noise specifications dictated by Rx AFEs are very stringent. The passive attenuator helps not only in attenuating the signal amplitude, but also the noise at the output of the DACs.

This design can be powered using a ±15- or 5-V supply (onboard Fly-Buck converter LM5160 converts a 5-V input to ±15-V rails). The clean power supplies for the entire signal chain are generated using the TPS7A39 (for ±13 V) and TPS7A47 (for 5 V). The buffered ±10-V references for DAC are generated using the REF5010 and OPA2209.

2.2 Highlighted Products

2.2.1 DAC8802

The DAC8802 is a dual, 14-bit, current-output DAC designed to operate from a single 2.7- to 5.5-V supply. The applied external reference input voltage V_{REF} determines the full-scale output current. (It can support a 2-mA full-scale current ±20% with V_{REF} = ±10 V). An internal feedback resistor (RFB) provides temperature tracking for the full-scale output when combined with an external I-to-V precision amplifier. The DAC has a 0.5-ms settling time and output spot noise of 12 nV/Hz at 1 kHz.

2.2.2 OPA2209

The OPA2209 operational amplifier (op amp) achieves very low-voltage noise density (2.2 nv/√Hz at 1 kHz) with rail-to-rail output swing to maximize the dynamic range. This op amp is specified over a wide dual power supply range of ±2.25 to ±18 V.

2.2.3 THS4130

The THS4130 is a fully-differential amplifier providing very low noise (1.3 nV/√Hz) to ensure maximum SNR and dynamic range. With a slew rate of 51 V/µs and gain bandwidth product of 150 MHz, it is able to operate with a ±2.5- to ±15-V supply.

2.2.4 TPS7A39

The TPS7A39 integrates a positive and a negative LDO designed to simplify the power supply design of the signal chain. The outputs of the TPS7A39 have built-in startup tracking to power split-rail systems, solving many floating conditions or sequencing problems common in split-rail systems. The negative output can regulate down to near 0 V improving the common-mode range for signal chain applications. Both regulators are controlled with a single positive logic enable pin for interfacing with standard digital logic. The input voltages range from ±3 to ±33 V and output voltages range from 1.2 to 30 V and 0 to –30 V.

2.2.5 TPS7A47

The TPS7A47 is a family of positive voltage (up to 36 V), ultra-low noise (4 μV_{RMS}) low-dropout linear regulators capable of sourcing a 1-A load. The output voltage can be configured using a printed circuit board (PCB) layout without the need of external resistors or feed-forward capacitors, thus reducing overall component count. The device has ≥ 55-dB PSRR with built-in current limit and thermal shutdown.

2.2.6 REF5010

The REF5010 is a low-noise, low-drift, very high-precision voltage reference. This reference is capable of both sinking and sourcing current and have excellent line and load regulation. The REF5010 has excellent temperature drift (3 ppm/°C) and high accuracy (0.05%). The noise is 3 μV_{PP}/V.

2.2.7 LM5160

The LM5160 device is a 65-V, 2-A synchronous step-down converter with integrated high-side and low-side MOSFETs. Peak and valley current limit circuits protect against overload conditions. The undervoltage lockout (EN/UVLO) circuit provides independently adjustable input undervoltage threshold and hysteresis. The LM5160 is programmed through the FPWM pin to operate in continuous conduction mode (CCM) from no load to full load or to automatically switch to discontinuous conduction mode (DCM) at a light load for higher efficiency. Forced CCM operation supports multiple output and isolated Fly-Buck applications using a coupled inductor.

2.3 Design Considerations

2.3.1 Challenges for RX AFE

Signals that are reflected immediately after transmission are very strong because they are from reflections close to the surface; reflections that occur long after the transmit pulse are very weak because they are reflecting from deep in the body. As a result of the limitations on the amount of energy that can be put into the imaging object, the industry developed extremely sensitive receive electronics with wide dynamic range. Received echoes from focal points close to the surface require little, if any, amplification. This region is referred to as the near field. However, echoes received from focal points deep in the body are extremely weak and must be amplified by a factor of 100 or more. This region is referred to as the far field. The receiver AFE has this unique challenge. It should be capable to adapt to both weak (far field) and strong (near field) received signals. This means that any strong echo must be conditioned so as to not saturate and distort the receive chain and any weak echo must be amplified while inducing minimal noise to determine the source of the echo. For this purpose, most of the receiver AFEs consists of:

- A highly linear low-noise amplifier (LNA) whose gain is digitally programmable. Sometimes it also has programmable input impedance for improved ultrasound probe matching characteristics.
- A voltage-controlled attenuator (VCAT) controlled through high-bandwidth analog pins, allowing for fast control. This block is capable of increasing or decreasing the gain (linear in dB) using external signal. Typically, a differential control structure is used to reduce common-mode noise.

注: Some devices also provide digital attenuation control along with analog control. The digital control feature can eliminate the noise from the V_{CNTL} circuit and ensure better SNR and phase noise for the TGC path. However, this design guide talks about the analog approach only.

The function of increasing and decreasing the gain according to the linear in dB scale is termed as time gain control, or TGC. 図 2 shows the simplified block diagram of the Ultrasound Receiver, Analog Front End AFE58JD18 from Texas Instruments. 図 2 shows these blocks (in grey) that help in TGC functionality.

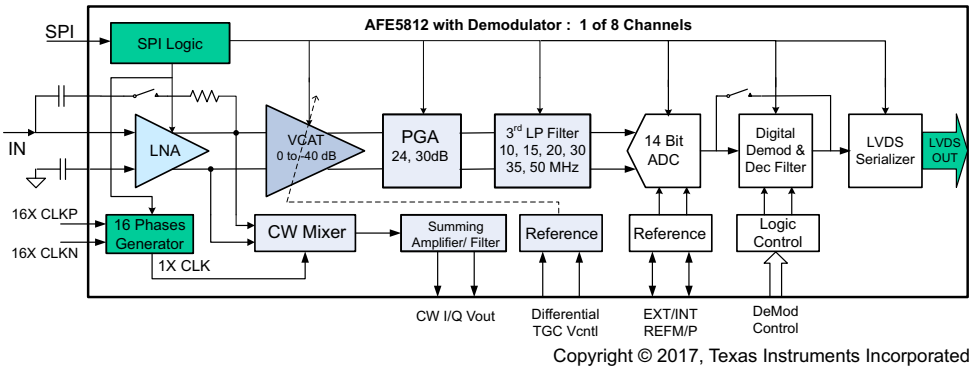


図 2. Simplified Block Diagram of AFE58JD18

2.3.2 What is TGC?

If an ultrasound element in the transducer is approximated as a point transmitter, then the transmit wave spreads in that area while the power density of the wave-front falls off in a classic case as inversely proportional to the square of the distance from the transducer. Reflecting from a tissue target, the return signal also diminishes in the same proportions. Thus, the total round-trip spreading signal attenuation varies as the inverse of the transducer-to-target distance to the fourth power. Body tissue reduces the signal due to scattering and dissipation. Note that such an attenuation varies as 1 dB/MHz/cm of tissue thickness. While high-frequency signals are desirable because they provide higher resolution due to their shorter wavelength, they are more rapidly attenuated, which decreases the SNR of deep penetrating signals.

During an ultrasound send-receive cycle, the magnitude of reflected signal depends on the depth of penetration. The purpose of TGC is to normalize the signal amplitude with time, compensating for depth. When the image is displayed, similar material must have similar brightness, regardless of depth; this is achieved by "Linear-in-dB" gain, which means the decibel gain is a linear function of the control voltage. 図 3 shows such an example of TGC for an ultrasound image.

図 3. TGC for Ultrasound Image

2.3.2.1 How Does Attenuation Work?

Using the AFE5812 from TI as an example, the voltage-controlled attenuator is typically designed to have a linear-in-dB attenuation characteristic; that is, the average gain loss in dB (see 図 4) is constant for each equal increment of the control voltage (V_{CNTL}).

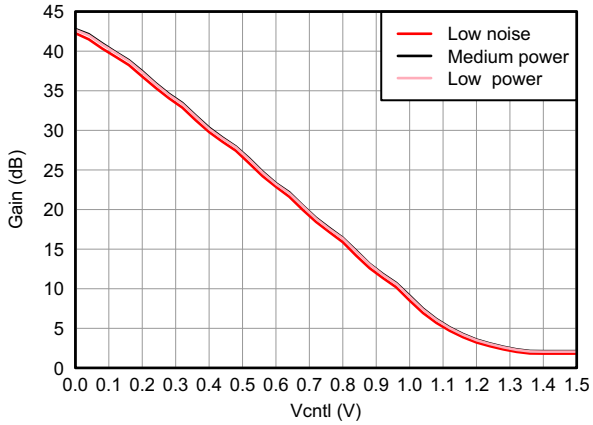


図 4. Gain versus Control Voltage Graph Demonstrating Linear-in-dB Attenuation Characteristic

2.3.3 TGC Drive Circuit

図 5 shows the signal chain of the AFE5818 analog front end. The TGC is implemented using an attenuator that can be controlled with V_{CNTL}. External circuitry is comprised of a DAC and an op amp to generate the control signal. The input signal for the DAC is a time-varying digital control from a field-programmable gate array (FPGA) that could also handle the beamforming operation required in an ultrasound application.

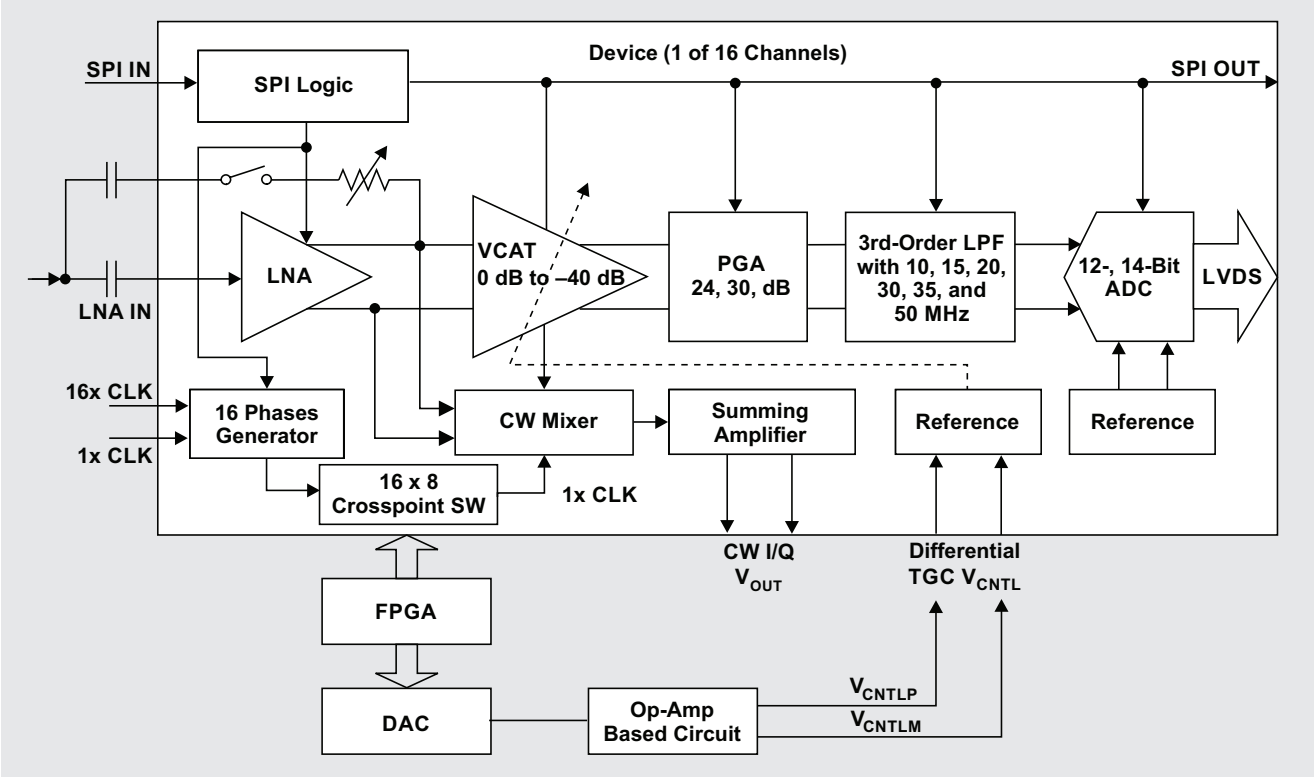


図 5. Signal Chain of AFE5818 and Analog Control for TGC Operation

2.3.4 V_{CNTL} Attributes From Point of View of AFE

The V_{CNTL} signal needs to be within some specifications dictated by the AFEs. The control voltage input (V_{CNTLM} and V_{CNTLP} pins) represents a high-impedance input. The V_{CNTLM} and V_{CNTLP} pins of multiple AFEs can be connected in parallel with no significant loading effects.

2.3.4.1 Signal Levels on Control Pins of AFE

For the AFE5818, V_{CNTL} is a differential input, V_{CNTLP} and V_{CNTLM}. When the V_{CNTL} level (defined as $V_{CNTLP} – V_{CNTLM}$) is above 1.5 V or below 0 V, the attenuator continues to operate at its maximum attenuation level or minimum attenuation level, respectively. As shown in 図 6, V_{CNTL} has a range of 1.5 to 0 V, and results in a gain-control range of 40 dB.

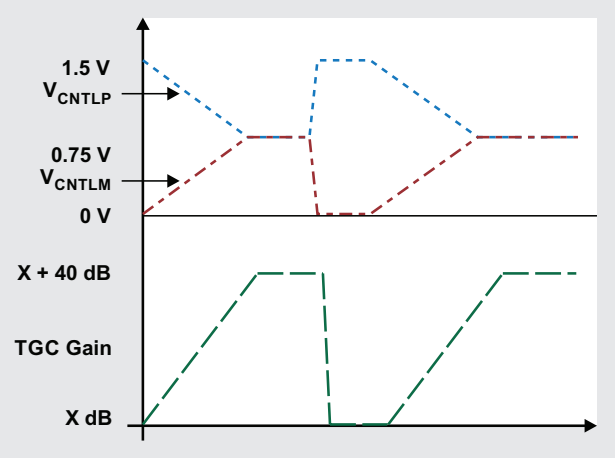


図 6. Gain Control Over Signal Range of V_{CNTL}

2.3.4.2 Input-Referred Noise

As the received ultrasound signal decreases as a function of elapsed time, V_{CNTL} also decreases to reduce the attenuation and increase the channel gain. 図 7 shows the benefit of the TGC circuit. As V_{CNTL} decreases and the channel gain increases, the input-referred noise of the receiver also continues to decrease. The reduced noise helps arrest the SNR fall related to the declining amplitude of the receiver signal.

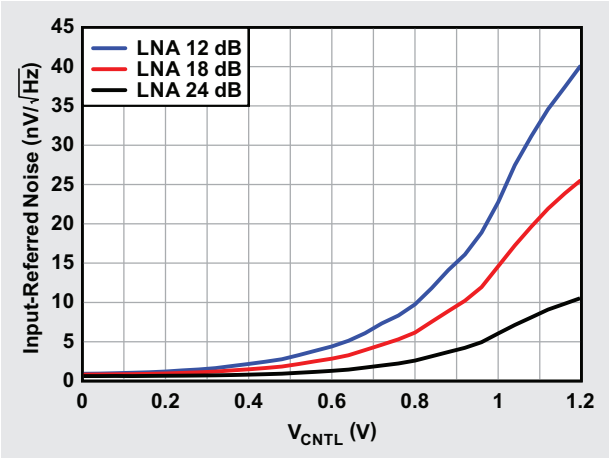


図 7. Input-Referred Noise versus V_{CNTL}

2.3.4.3 Noise Requirement for Multiple Channels

One key consideration in the design of the V_{CNTL} drive circuit is the noise specification on V_{CNTL}. Because V_{CNTL} is a common control voltage across multiple channels of the AFE (and possibly shared with the channels of other AFE chips), any noise on V_{CNTL} shows up as a source of noise that is correlated across the multiple AFE channels that share that same V_{CNTL}. 図 8 shows the allowed noise on V_{CNTL} as a function of the number of channels sharing the same V_{CNTL} drive.

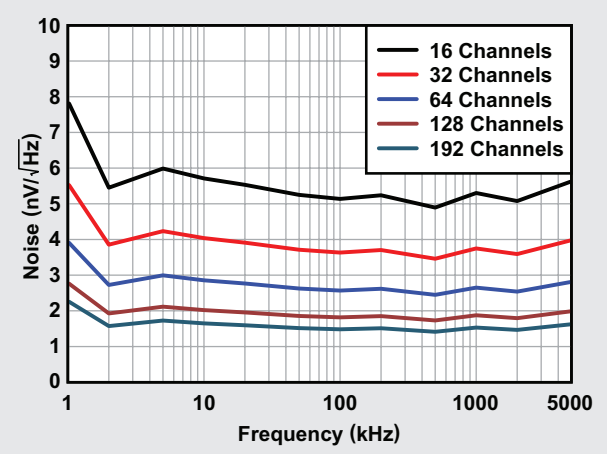


図 8. Allowed Noise on V_{CNTL} Signal Across Frequency and Different Channels

2.4 System Design Theory

This section explains the design theory and equations for each of the devices used in this reference design.

2.4.1 Selecting Devices

The specifications and attributes explained in 2.3.4 define the choice of the signal chain as well as power components on this reference design.

The DAC must have the following specifications:

- Resolution and V_{REF} decide the DAC output voltage ($V_{REF}/2^n$), typically 12 to 14 bits
- Settling time: sub 1 µs
- Sampling rate: > 1 MSPS
- Interface: Mostly the digital signals come from FPGA or controller, so SPI is preferred to reduce the number of interface lines and complexity.
- Channel count: 2 (to implement pseudo differential signal chain)
  - Must be able to accept a V_{REF} up to ±10 V.
- Noise: < 15 nV/√Hz

The DAC8802 is a device that meets all of these conditions. It is a current-output multiplying DAC, so there is a need for a current-to-voltage converter.

The op amp used for I-to-V conversion must have low-voltage noise as well as low-current noise density. The current density helps in reducing the overall noise performance because of the DAC output configuration. Because the DAC output can go up to ±10 V, the op amp must have bipolar operation and a power supply option. The OPA2209 is a precision op amp with a voltage noise density of 2.2 nV/√Hz and a current noise density of 500 fA/√Hz. The device can accept a wide supply range of ±2.25 to ±18 V and provide rail-to-rail output.

There is a typical requirement to have a Butterworth low-pass filter using a differential amplifier to smoothen out the DAC output. The device must be able to drive the passive attenuator load of ≈ 750 Ω. It must accept bipolar supply voltage and be very low noise. The THS4130 is a fully differential, 1.3-nV/√Hz op amp with a wide supply range of ±2.5 to ±15 V.

To operate the DAC at full code, the reference signal needs to be ±10 V, which can be generated by using the REF5010 and two buffers (one inverting and one non-inverting). The noise of the reference and buffers are directly reflected at the output of DAC, so it is important to have lowest noise components selected for the same.

To operate the signal chain circuit, it has to have a bipolar supply of ±13 V generated from a good PSRR LDO regulator. The TPS7A39 is wide-V_{IN} (±33 V), 150-mA, wide-V_{OUT} (±30 V), and tracking positive and negative LDO voltage regulator for signal-chain applications. It has output voltage noise of 15 μV_{RMS} and has PSRR of 72 dB.

The digital supply for DAC8802 needs to be 5 V, designed using TPS7A47. It is a 36-V, 1-A, 4.17-μV_{RMS} LDO voltage regulator.

2.4.2 Circuit Design

2.4.2.1 DAC8802 + OPA2209

図 9 shows the circuit diagram for the DAC8802 followed by two op amps used as I-to-V converters (in a single-package OPA2209).

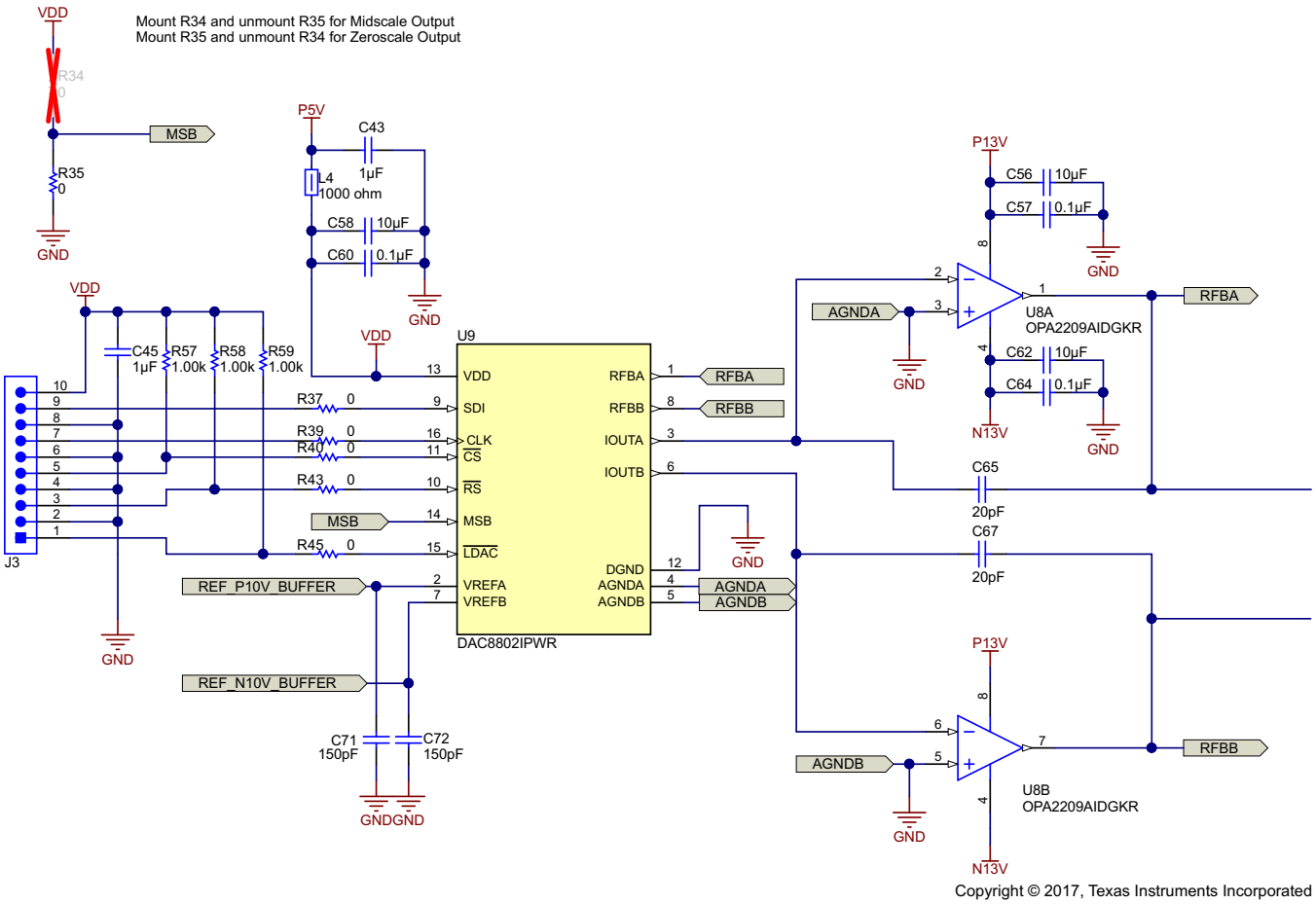


図 9. 14-Bit Dual DAC8802s and I-to-V Converters Using OPA2209

The DAC8802 contains two 14-bit, current-output DACs. The device uses a three-wire, SPI-compatible serial data interface, with a configurable asynchronous RS pin for half-scale (MSB = 1) or zero-scale (MSB = 0) preset. In addition, an LDAC strobe enables two-channel simultaneous updates for hardware-synchronized output voltage changes. Each DAC contains a matching feedback resistor for use with an external I-to-V converter amplifier. The RFBX pin is connected to the output of the external amplifier. The IOUTX terminal is connected to the inverting input of the external amplifier. The AGNDX pin must be Kelvin-connected to the load point in the circuit requiring the full 14-bit accuracy.

The DAC is designed to operate with both negative and positive reference voltages. The VDD power pin is only used by the logic to drive the DAC switches on and off. Note that a matching switch is used in series with the internal 5-kΩ feedback resistor. The DAC output voltage is determined by V_{REF} and the digital data (D) according to 式 1:

$$V_{OUT} = -V_{REF} \times \frac{D}{16384} \quad (1)$$

Note that the output polarity is opposite of the V_{REF} polarity for DC reference voltages.

The DAC is also designed to accommodate ac reference input signals. The DAC8802 accommodates input reference voltages in the range of –15 to 15 V. The reference voltage inputs exhibit a constant nominal input resistance of 5 kΩ, ±20%. On the other hand, DAC outputs IOUTA and IOUTB are code-dependent and produce various output resistances and capacitances.

The OPA2209 is used for converting the current output from the DAC8802. The choice of an external amplifier must take into account the variation in impedance generated by the DAC8802 on the inverting input node of the amplifiers. The feedback resistance, in parallel with the DAC ladder resistance, dominates output voltage noise. For multiplying mode applications, an external feedback compensation capacitor, CFB (4 to 20 pF typical), may be needed to provide a critically damped output response for step changes in reference input voltages.

2.4.2.2 ±10-V Reference Generation for DAC8802

The ±10-V reference voltages for the DAC8802 are generated using the REF5010 and OPA2209 as shown in 図 10, 図 11, and 図 12.

The REF5010 can accept voltage inputs up to 15 V. The input is filtered using a CLC filter. One 1-µF capacitor is used for TRIM/NR pin. The output capacitor needs to have an ESR of 1 to 1.5 Ω. R19 (= 1 Ω) is used in series with C35 (10 µF) for stability.

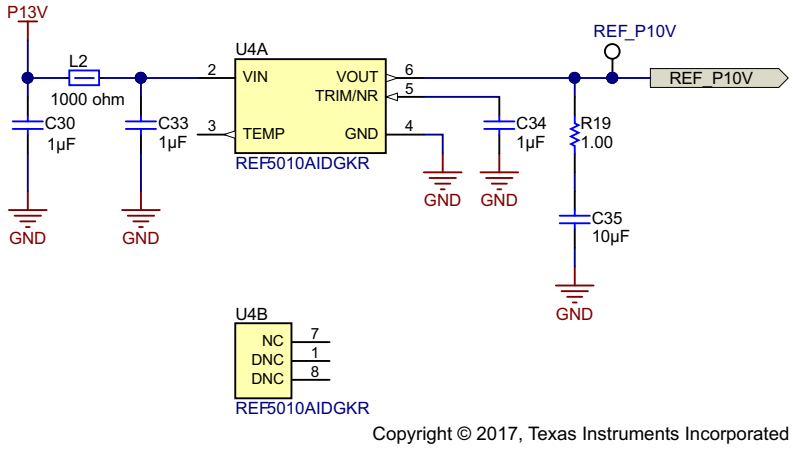


図 10. REF5010 to Generate 10-V Reference

The output of the REF5010 is buffered to generate a 10-V reference for the DAC8802, as shown in 図 11. The input of the op amp is filtered by a low-pass filter (R24 and C38) with a cutoff frequency of 15.9 Hz. "REF_P10V_B" is the buffered and filtered 10-V reference, which goes to the DAC8802.

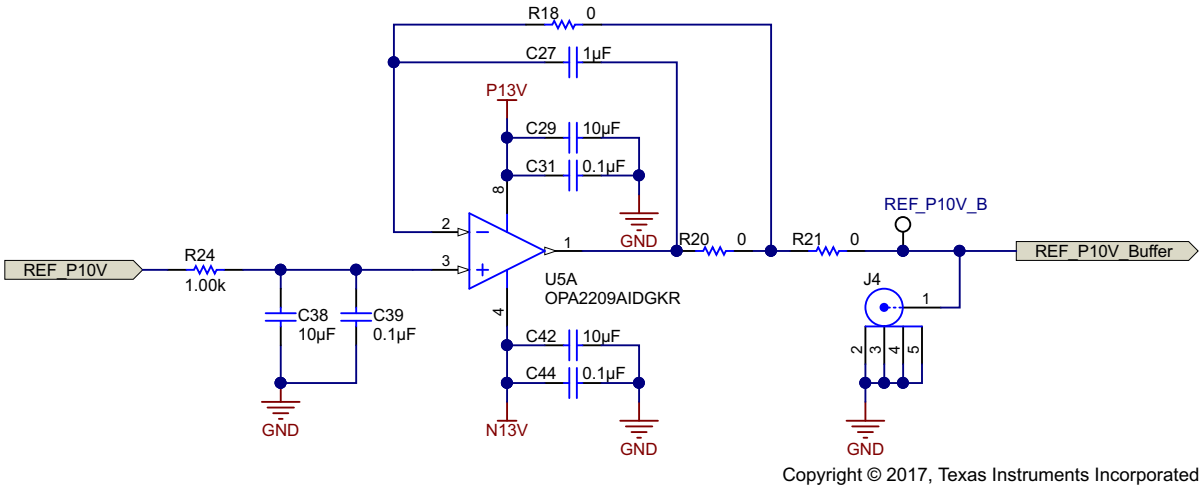


図 11. Positive Buffer to Generate 10-V Reference for DAC8802

The output of REF5010 is buffered to generate a –10-V reference for DAC8802 as shown in 図 12. The input of the op amp is filtered by a low-pass filter (R25 and C40) with a cutoff frequency of 15.9 Hz. "REF_N10V_B" is the buffered and filtered –10-V reference, which goes to the DAC8802. The inverting amplifier is prone to instability when it has such high (10 µF) capacitor at the input terminal. To compensate for it, the feedback needs to have a capacitor equal or higher than the value at the input terminal (C32 and C28 are used for this purpose).

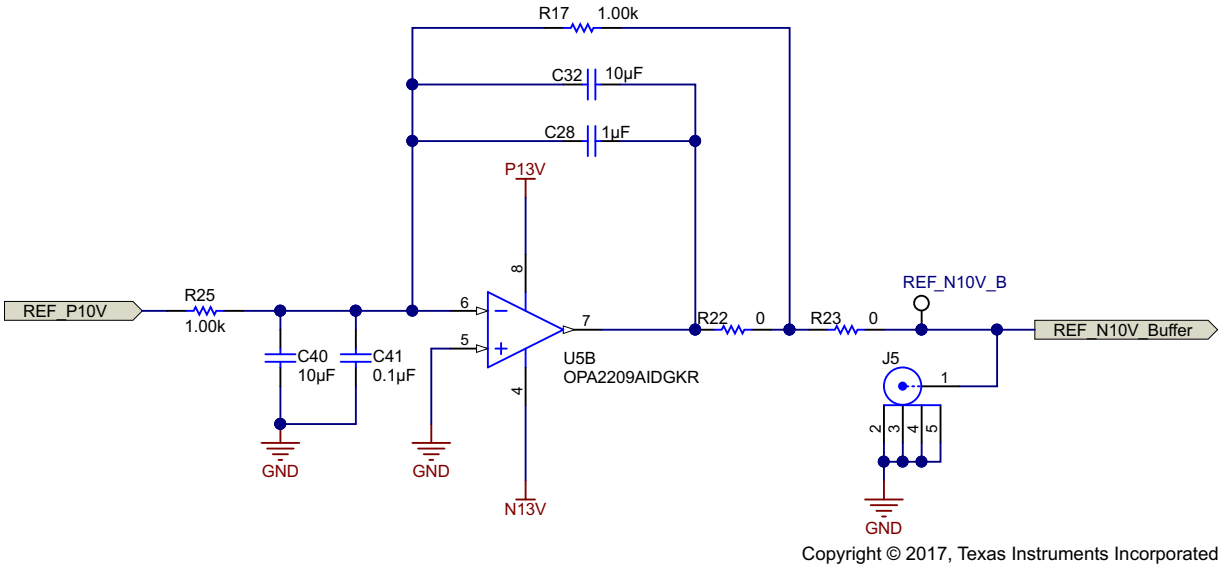


図 12. Negative Buffer to Generate –10-V Reference for DAC8802

2.4.2.3 Second-Order Butterworth LPF Using THS4130

To remove high-frequency noise and make the shape of the output signal from DAC8802 smooth, it is important to use an active low-pass filter with a cutoff frequency around 100 to 200 kHz. This reference design uses a multiple feedback LPF Butterworth filter using THS4130 as shown in 図 13. The THS4130 is a differential amplifier with a noise level of 1.3 nV/√Hz. The gain of the filter is set to be unity and cutoff frequency is set to 150 kHz. For a TINA-TI™ simulation for the filter and the frequency response, see 3.2.1.

The output common-mode voltage (V_{OCM}) is set by the voltage on the VOCM input pin. It is set to 0.75 V as explained in 2.4.2.4.

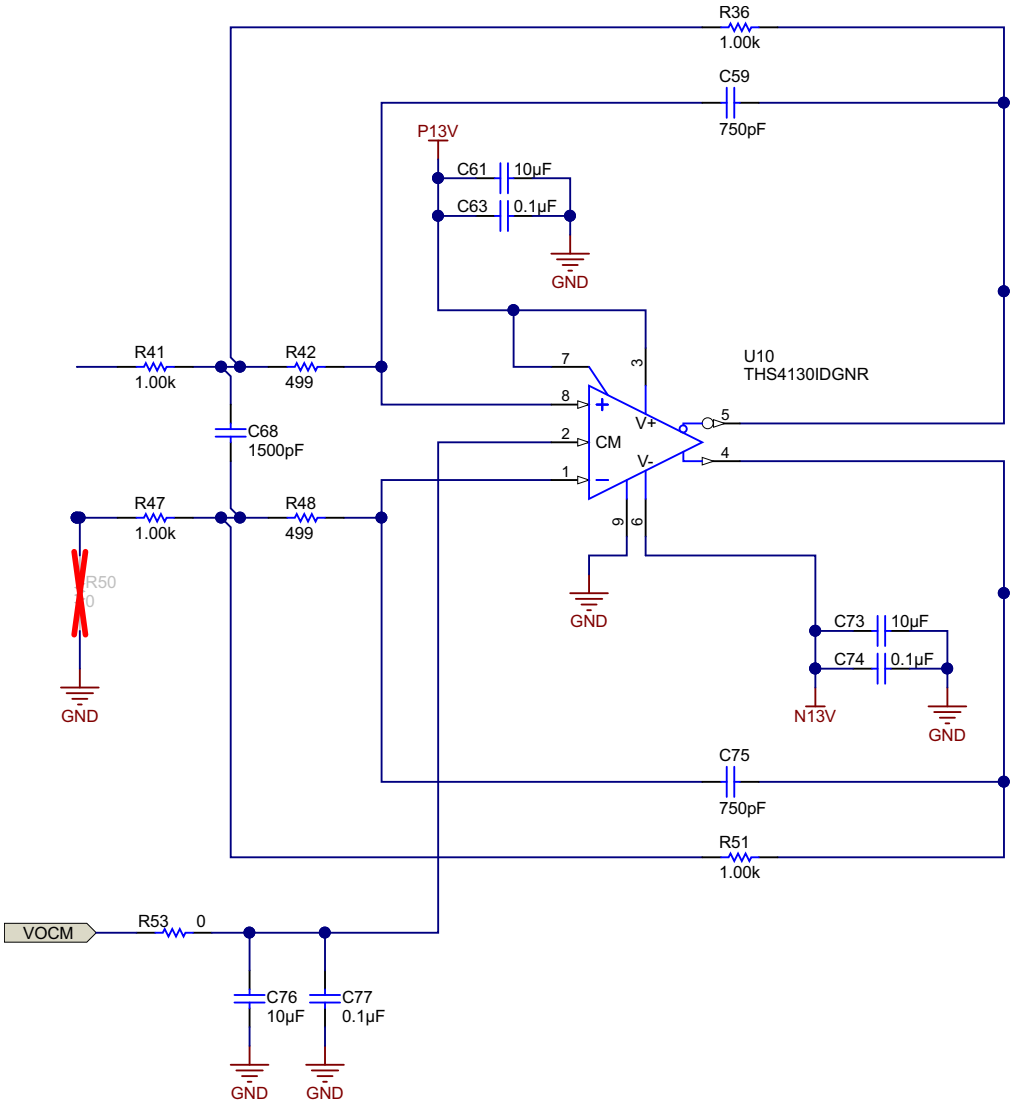


図 13. 150-kHz LPF Using THS4130 Schematic

Note the output swing capability of the THS4130 op amp. The capability depends on the supply voltage rails, differential load resistance, and feedback resistors as shown in 図 14.

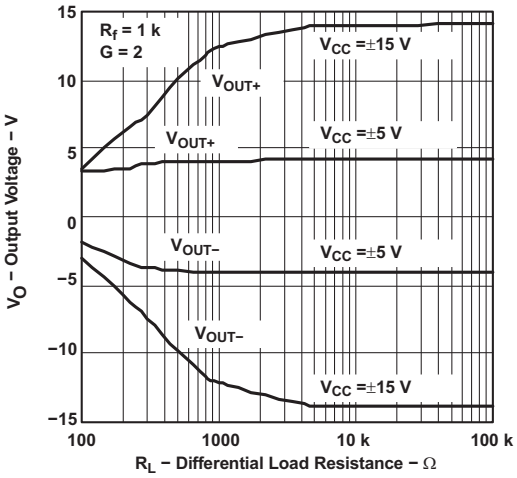


図 14. Output Voltage versus Differential Load Resistance

2.4.2.4 V_{OCM} Generation

The output common-mode voltage (V_{OCM}) for V_{CNTL} is specified to be 0.75 V. The voltage is generated using the REF5010 reference and a resistor divider as shown in 図 15.

$$V_{OCM} = \frac{374}{4.02\,k + 590 + 374} \times 10 = 0.75\ V \quad (2)$$

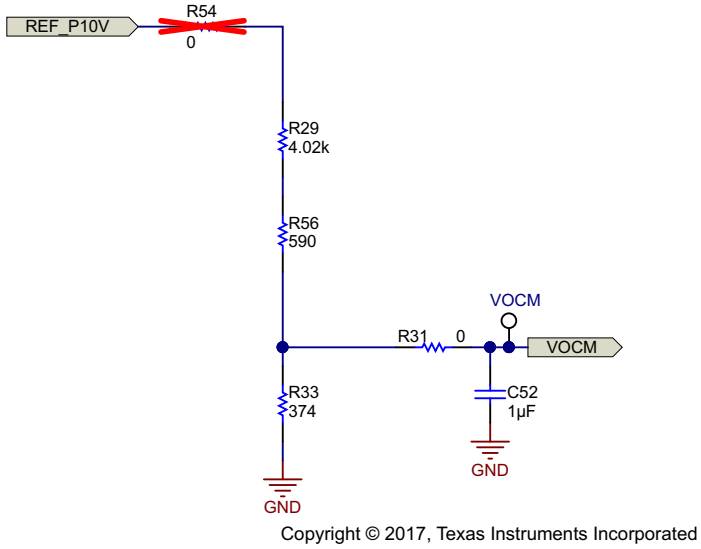


図 15. V_{OCM} Signal Generation Using Resistor Divider

2.4.2.5 V_{CNTL} Generation Using Passive Filter

The V_{CNTL} signal is generated using passive attenuator, as shown in 図 16. Even though the V_{CNTL} ranges from 0 to 1.5 V, the signal chain starts off with a much higher reference voltage. An attenuation circuit reduces the range to the desired range of V_{CNTL}. This approach of starting off with a high reference voltage and high DAC full-scale range followed by attenuation helps to attenuate the noise contributions from the reference circuit, the DAC, and other op amps used in the signal conditioning.

The required attenuation is provided by 式 3:

$$\text{Attenuation} = \frac{20}{1.5} = 13.33 \quad (3)$$

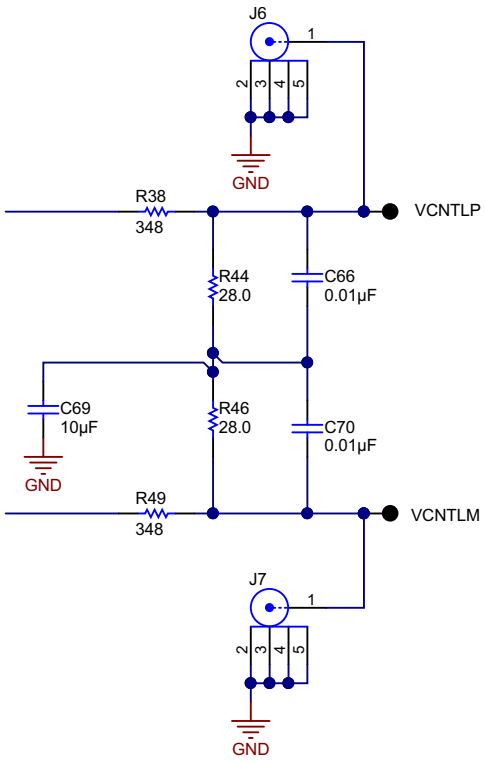


図 16. Passive Attenuator to Generate V_{CNTL} Signal

2.4.2.6 ±15-V Rails

This reference design accepts two types of inputs: ±15 V (VIN-A) in 図 17 or 5 to 12 V (VIN-B) in 図 18.

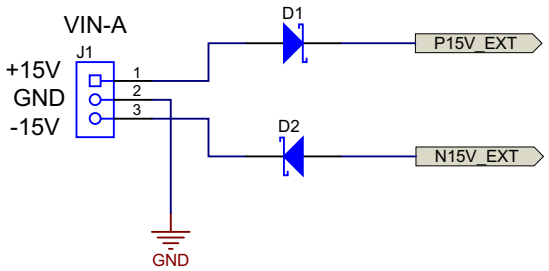


図 17. ±15-V Input for TIDA-01427

As shown in 図 18, the LM5160 is used in Fly-Buck configuration to generate –15.7 V. A coupled inductor is used for generating 15.7 V. Note that the diode drops are counted while designing, so actual outputs will be around ±15 V. The power supply operates at a switching frequency of 200 kHz and has UVLO = 3 V.

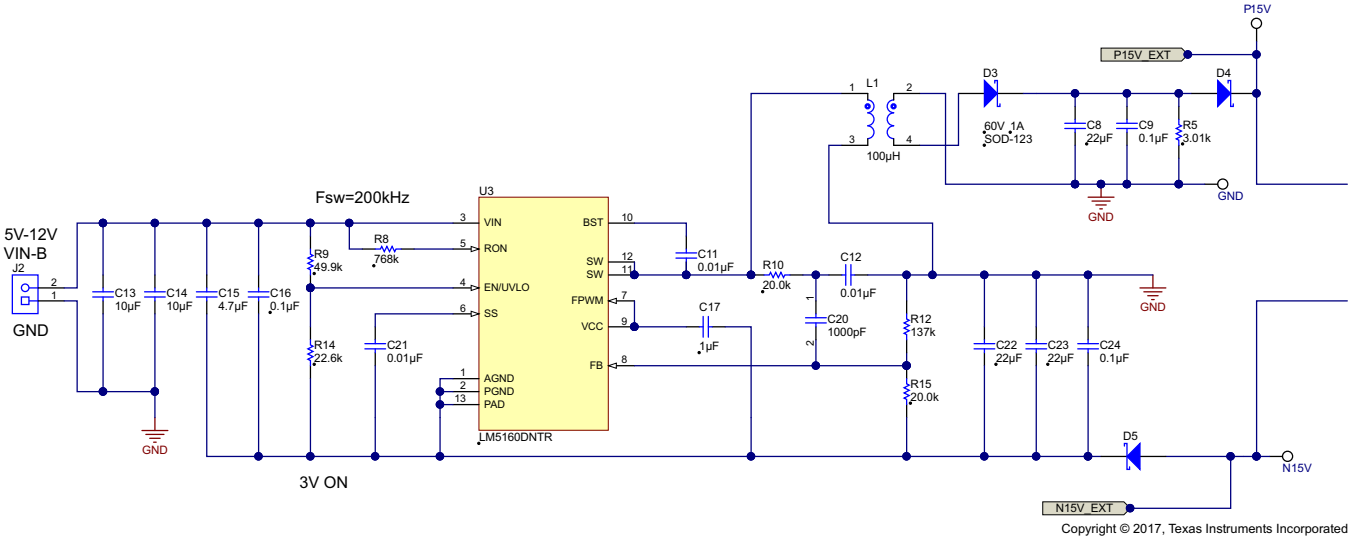


図 18. ±15-V Generation Using LM5160

注: VOUT1 is the absolute value of –VOUT1 in all the equations in this section.

The switching frequency and on-resistor (R_{ON}) are related as per 式 4.

$$R_{ON} = \frac{V_{OUT}}{F_{SW} \times 1 \times 10^{-10}} = \frac{15.7}{200\,k \times 1 \times 10^{-10}} = 785\,k\Omega \quad (4)$$

The output for the primary side is calculated as per 式 5:

$$V_{OUT} = \frac{V_{REF} \times (R_{FB2} + R_{FB1})}{R_{FB1}} V \quad (5)$$

For V_{OUT} = 15.5 V and V_{REF} = 2 V, R_{FB1} (R15) = 20 kΩ and R_{FB2} (R12) = 137 kΩ. The duty cycle is calculated to be 0.758 as shown in 式 6:

$$D = \frac{V_{OUT1}}{V_{IN} + V_{OUT1}} = \frac{15.7}{5 + 15.7} = 0.758 \quad (6)$$

The inductor currents primary inductor current (I_{L1}) and secondary inductor current (I_{L2}) are calculated using 式 7 and 式 8:

$$I_{L1} = \frac{I_{OUT1} + \frac{N2}{N1} I_{OUT2}}{1 - D} = \frac{0.175 + 0.175}{1 - 0.758} = 1.44\ A \quad (7)$$

$$I_{L2} = I_{OUT2} = 0.175\ A \quad (8)$$

The primary winding peak-to-peak current ripple is calculated in 式 9:

$$\Delta I_{L1} = \frac{1}{L1 \times f_W} \times \frac{V_{IN(MAX)} \times V_{OUT1}}{V_{IN(MAX)} + V_{OUT1}} = \frac{1}{100\,\mu \times 200\,k} \times \frac{12 \times 15.7}{12 + 15.7} = 0.34\ A \quad (9)$$

The peak current in high-side FET and primary winding is calculated in 式 10:

$$i_{L1(peak)} = \frac{1}{1-D}\left(I_{OUT1} + \frac{N2}{N1} I_{OUT2}\right) + \frac{\Delta_{IL1}}{2} = \frac{1}{1-0.758}(0.175 + 0.175) + \frac{0.34}{2} = 1.61\,A \quad (10)$$

2.4.2.7 ±13-V Power Supply Rails Generated Using TPS7A39

The TPS7A39 contains two LDOs: one for positive output and one for negative output. The output voltage range of the positive LDO is V_{REF} to 30 V, while the output voltage range of the negative LDO is 0 to –30 V (see 図 19).

The feedback resistors are dependent on the outputs for both the sections, which are calculated as shown in 式 11 and 式 12, respectively:

$$R_4 = \left(\frac{V_{OUTP}}{V_{FBP}} - 1\right) \times R_7 = \left(\frac{13}{1.188} - 1\right) \times 10.2\,k \times = 102\,k \quad (11)$$

$$R_{13} = -\frac{V_{OUTN}}{V_{BUF}} \times R_{16} = -\left(\frac{13}{-1.188}\right) \times 10.5\,k = 115\,k\Omega \quad (12)$$

The minimum bias current through both feedback networks is 5 μA, ensuring stability. This bias current limits R16 and R13 to a maximum value of 240 kΩ. The minimum value of R13 is 10 kΩ as the reference buffer can drive up to 120 μA and remain within specifications.

The device is designed to be stable using ceramic capacitors with low equivalent series resistance (ESR) at the input and output pins. The device is also designed to be stable with aluminum polymer and tantalum polymer capacitors with ESR < 75 mΩ.

Along with higher ESR polymer capacitors, electrolytic capacitors can also be used if capacitors that meet the minimum capacitance and ESR requirements are used in parallel.

Although a feed-forward capacitor (CFFx) from the FBx pin to the OUTx pin is not required to achieve stability, a 10-nF external CFFx optimizes the transient, noise, and PSRR performance. C6 and C19 are used as feed-forward capacitors.

Although a noise-reduction and soft-start capacitor (CNR/SS) from the REF pin to GND is not required, CNR/SS is highly recommended to control the start-up time and reduce the noise-floor of the device. Start-up tracking may not function correctly if CNR/SS becomes too small because the start-up time of the positive and negative error amplifiers will be longer than the rise time of V_{REF}.

While designing this power supply, note these important points:

- Do place at least one, low ESR, 10-μF capacitor as close as possible to both the IN and OUT terminals of the regulator to the GND pin.
- Do provide adequate thermal paths away from the device.
- Do not place the input or output capacitor more than 10 mm away from the regulator.
- Do not exceed the absolute maximum ratings.
- Do not float the Enable (EN) pin.

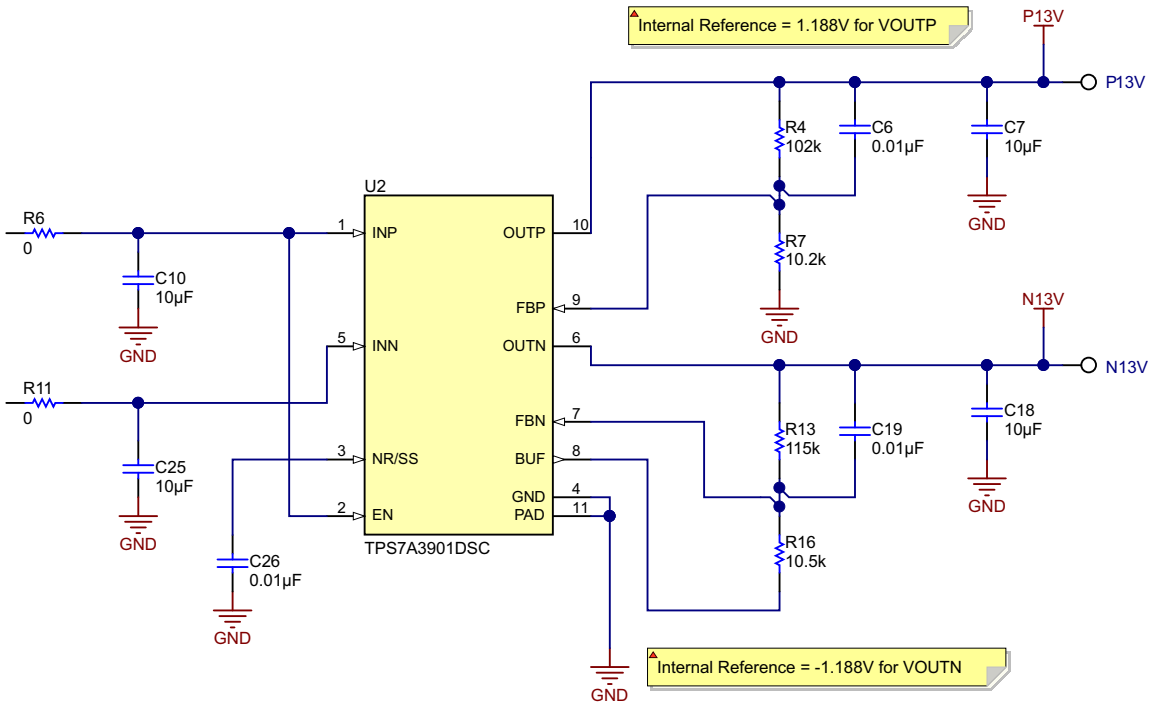


図 19. ±13-V Generation Using TPS7A39

2.4.2.8 5-V Power Supply Rails Generated Using TPS7A47

The VDD supply (5 V) for DAC8802 is generated using the TPS7A47 as shown in 式 13. The TPS7A4700 has an ANY-OUT operation, which does not use external resistors to set the output voltage, but uses devices pins to program the output voltage. The ANY-OUT programming is set by 式 13 as the sum of the internal reference voltage (V_{REF} = 1.4 V) plus the accumulated sum of the respective voltages assigned to each active pin; that is, 100 mV (pin 12), 200 mV (pin 1), 400 mV (pin 10), 800 mV (pin 9), 1.6 V (pin 8), 3.2 V (pin 6), 6.4 V (pin 5), or 6.4 V (pin 4).

$$V_{OUT} = V_{REF} + \left(\sum \text{ANY-OUT Pins to Ground}\right) \quad (13)$$

In this case, the output is set at 5 V by grounding only the 3P2V and 0P4V pins.

The LDOs are designed to be stable using low ESR ceramic capacitors at the input, output, and at the noise reduction pin (NR, pin 14).

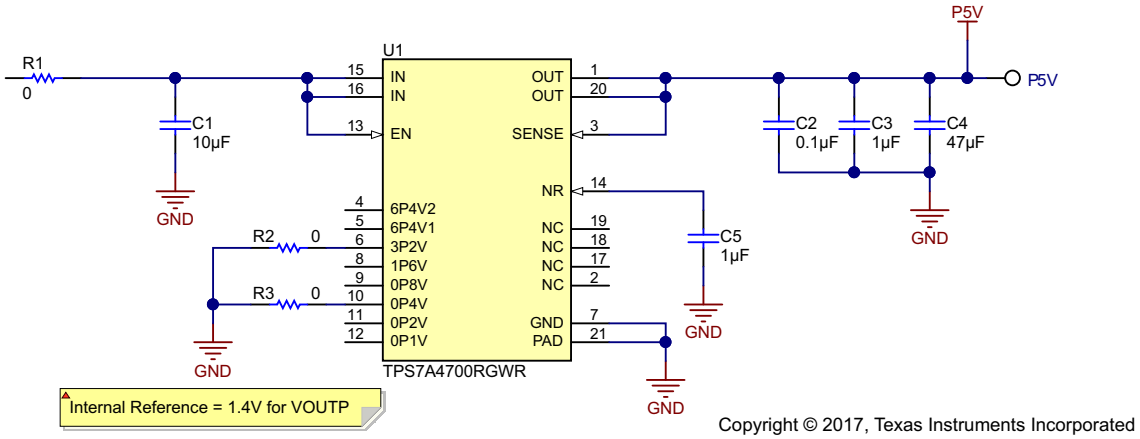


図 20. 5-V Generation Using TPS7A47

3 Hardware, Software, Testing Requirements, Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

図 21 and 図 22 show the top and bottom views of the design PCB, respectively.

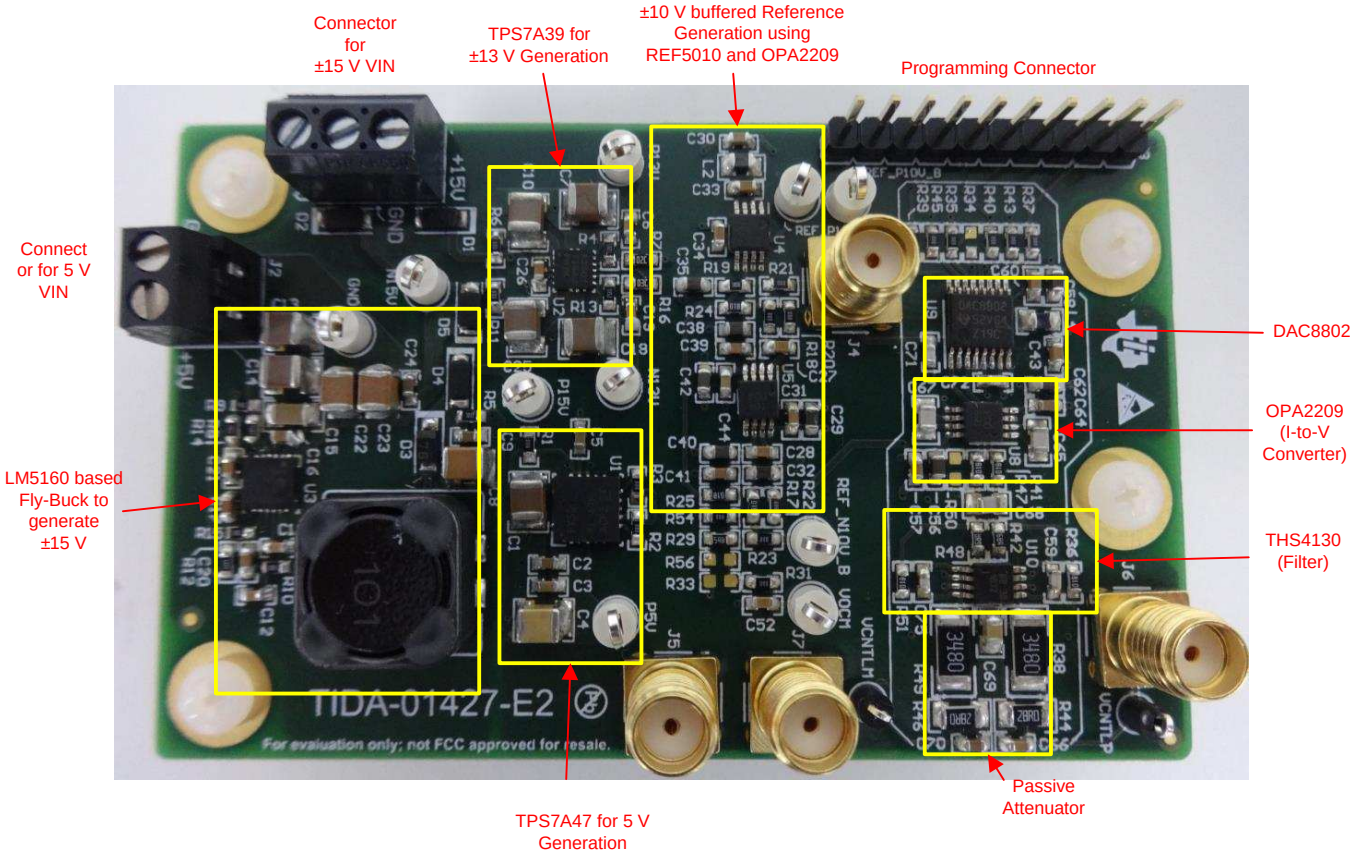


図 21. TIDA-01427 PCB—Top View

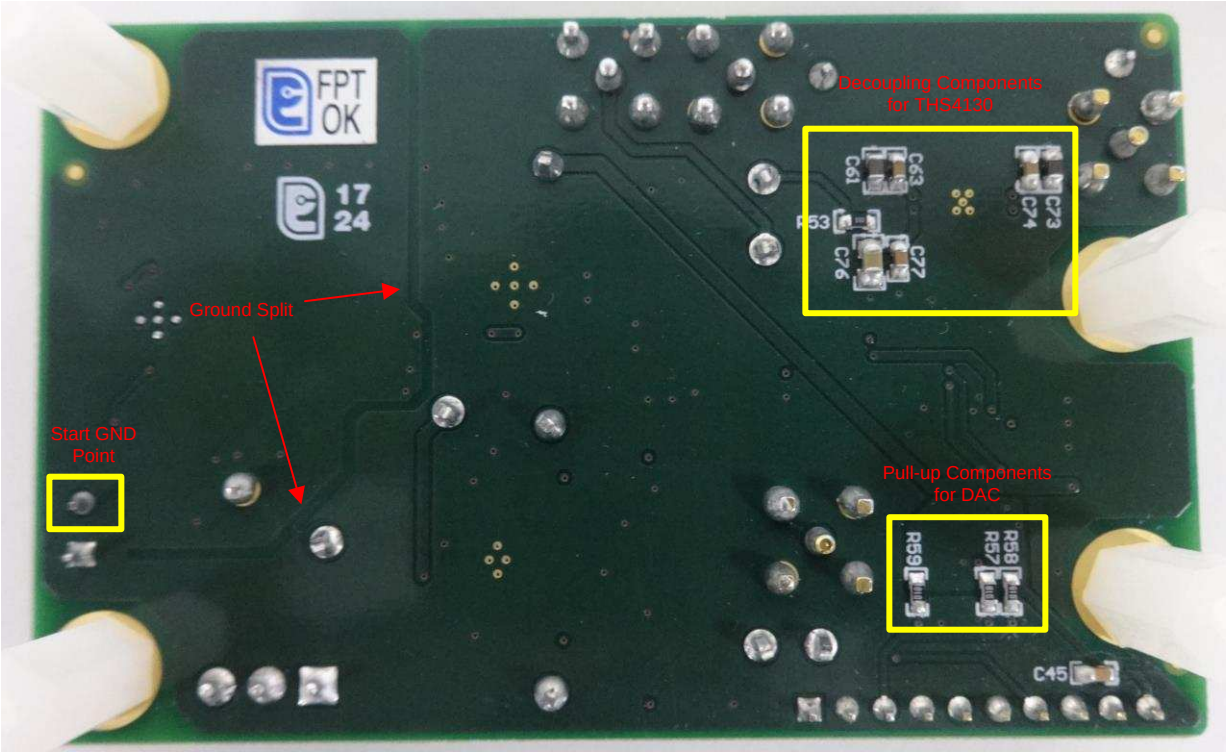


図 22. TIDA-01427 PCB—Bottom View

3.1.2 Software

3.1.2.1 DAC Programming

図 23 shows the flow chart for programming the DACs. The DAC8802 uses a three-wire (CS, SDI, CLK) SPI-compatible serial data interface. Serial data of the DAC8802 is clocked into the serial input register in a 16-bit data-word format. MSB bits are loaded first. 表 2 defines the 16 data-word bits for the DAC8802. Data is placed on the SDI pin, and clocked into the register on the positive clock edge of CLK subject to the data setup and data hold time requirements specified in the Interface Timing specifications of the Electrical Characteristics table in the DAC8802 datasheet (SBAS351). Data can only be clocked in while the CS chip select pin is active low. For the DAC8802, only the last 16 bits clocked into the serial register are interrogated when the CS pin returns to the logic high state. Because most microcontrollers output serial data in 8-bit bytes, two right-justified data bytes can be written to the DAC8802. Keeping the CS line low between the first and second byte transfer results in a successful serial register update. Once the data is properly aligned in the shift register, the positive edge of the CS initiates the transfer of new data to the target DAC register, determined by the decoding of address bits A1 and A0.

表 2. Serial Input Register Data Format, Data Loaded MSB First

BIT	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0(LSB)
DATA	A1	A0	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

For 表 2, only the last 16 bits of data clocked into the serial register (address + data) are inspected when the /CS line positive edge returns to logic high. At this point, an internally-generated load strobe transfers the serial register data contents (bits D13-D0) to the decoded DAC-input-register address determined by bits A1 and A0 (see 表 3). Any extra bits clocked into the DAC8802 shift register are ignored; only the last 16 bits clocked in are used.

表 3. Address Code

A1	A0	DAC DECODE
0	0	None
0	1	DAC A
1	0	DAC B
1	1	DAC A and DAC B

Two additional pins, RS and MSB, provide hardware control over the preset function and DAC register loading. If these functions are not needed, the RS pin can be tied to logic high. The asynchronous input RS pin forces all input and DAC registers to either the zero-code state (MSB = 0) or the half-scale state (MSB = 1).

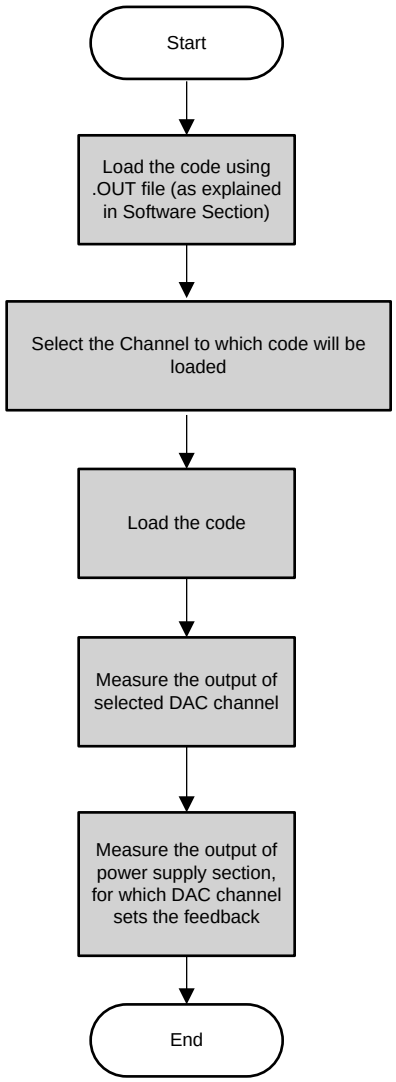


図 23. Flow Chart for Programming DAC8802

3.1.2.2 Software Loading for TIDA-01427

To test and obtain the results for this reference design, the following software tools are used:

- Code Composer Studio™ (CCS) version 6.1.2.00015 or higher
- LaunchPad™ based on MSP430™ (MSP-EXP430G2)

After installing CCS and GUI Composer on the PC, perform the following:

1. Download the firmware from the TIDA-01427 product page. The firmware contains output file (.OUT).
2. Open CCS and connect the LaunchPad to PC and turn on the power supply of the TIDA-01427 PCB.
3. Create a new target configuration with "User defined File Name, ccxml" through following path: File → New → Target Configuration File.
4. Select "MSP430G2553" in the "Board or Device" menu and save the file.
5. Click on "View" in the main CCS toolbar and open "Target Configurations."
6. In the Target Configurations window, select "User Defined File Name. ccxml" under the User Defined menu and run the debugger.
7. In the Debug Console window, right click on "User Defined File Name. ccxml" and select "Connect Target."
8. Click on the "Run" option in the main toolbar and go to Load → Load Program.
9. Once the .OUT file is loaded, look for "Expressions" tab in CCS. It should show "channel_sel," "V_Iadj," and "update" variables. If not, the user can write these expressions.
10. The variable "channel_sel" selects the DAC channel as "0 for no selection," "1 for selecting Channel-1," "2 for selecting Channel-2," and "3 for selecting both the channels."
11. The variable "V_Iadj" shows the output of the selected DAC channel (varies from 0 to 10 V).
12. The variable "update" writes the input code into the DAC8802. Until the "update" variable is set to "1," the DAC8802 will not be loaded with the code.
13. Note the default values for the following variables:
    - channel_sel = 3
    - V_Iadj = 0
    - update = 0

3.2 Testing and Results

This section shows the test setup and test results for this reference design.

3.2.1 Simulation Results Using TINA-TI Software

The entire signal chain (including the DAC8802, OPA2209 for I-to-V conversion, low-pass filter using the THS4130, and the passive attenuator) with the reference generation circuit are simulated for DC analysis and noise analysis using TINA-TI. 図 24 shows the DC analysis and DC values of all the voltages. 図 25 shows the noise simulation for the V_{CNTL} output. The simulated noise is < 2.5 nV from a 1-kHz to 5-MHz frequency range.

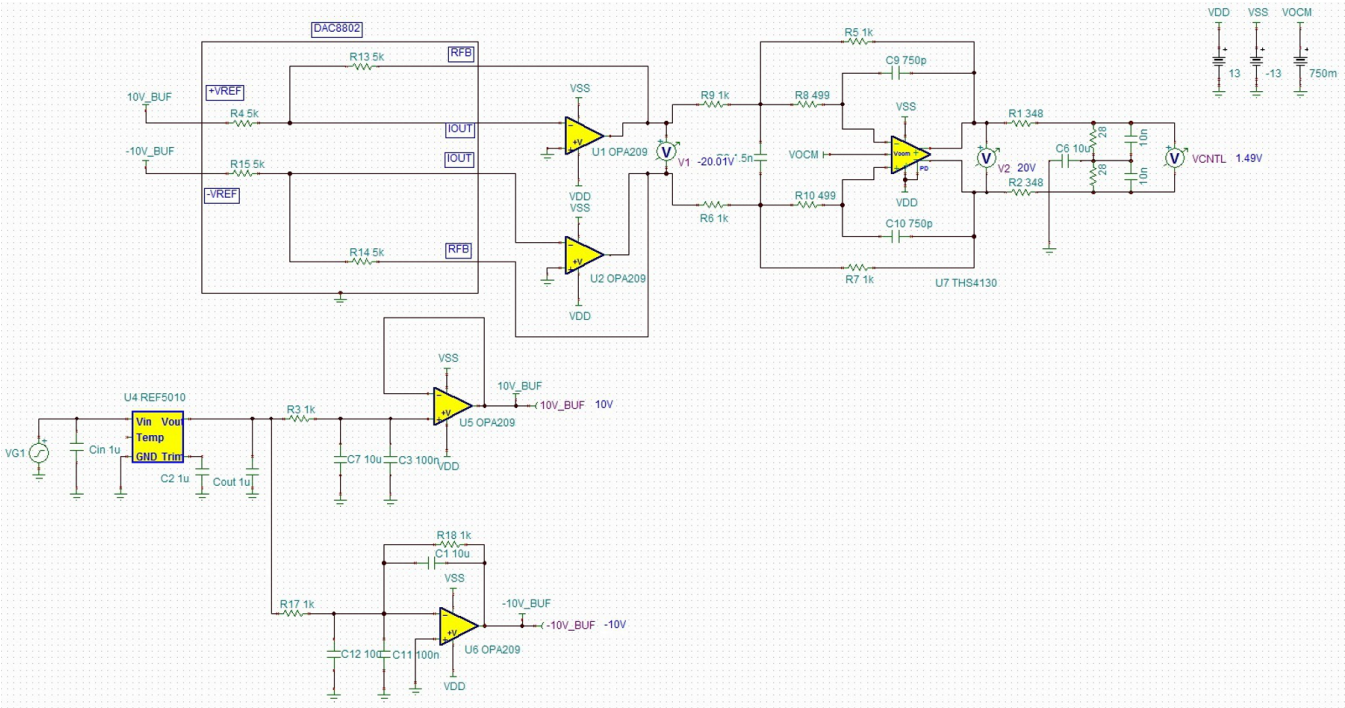


図 24. TINA-TI Simulation for DC Analysis Showing V_{CNTL}

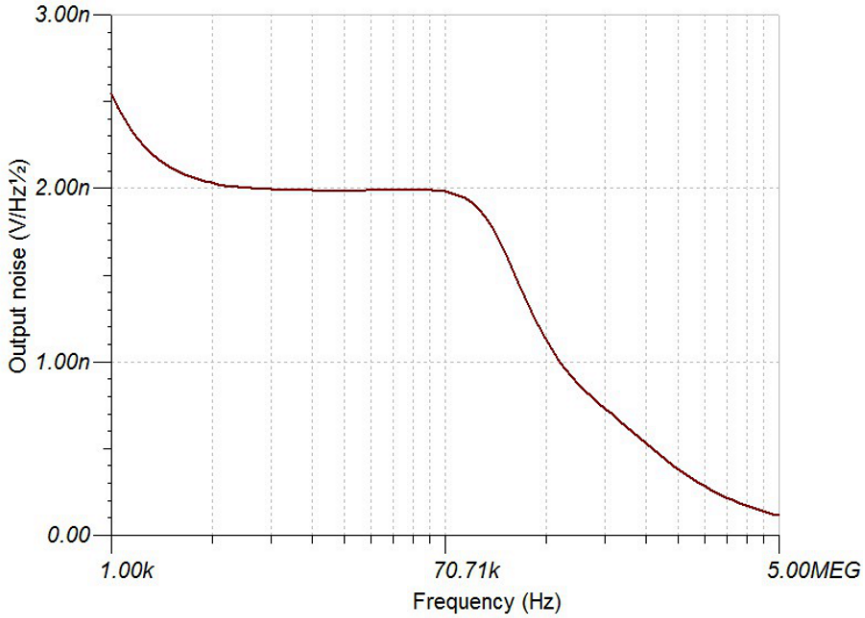


図 25. Noise Simulation Plot

The second-order Butterworth low-pass filter is also simulated with TINA-TI. 図 26 shows the 150-kHz LPF circuit, and 図 27 shows the frequency response for the same.

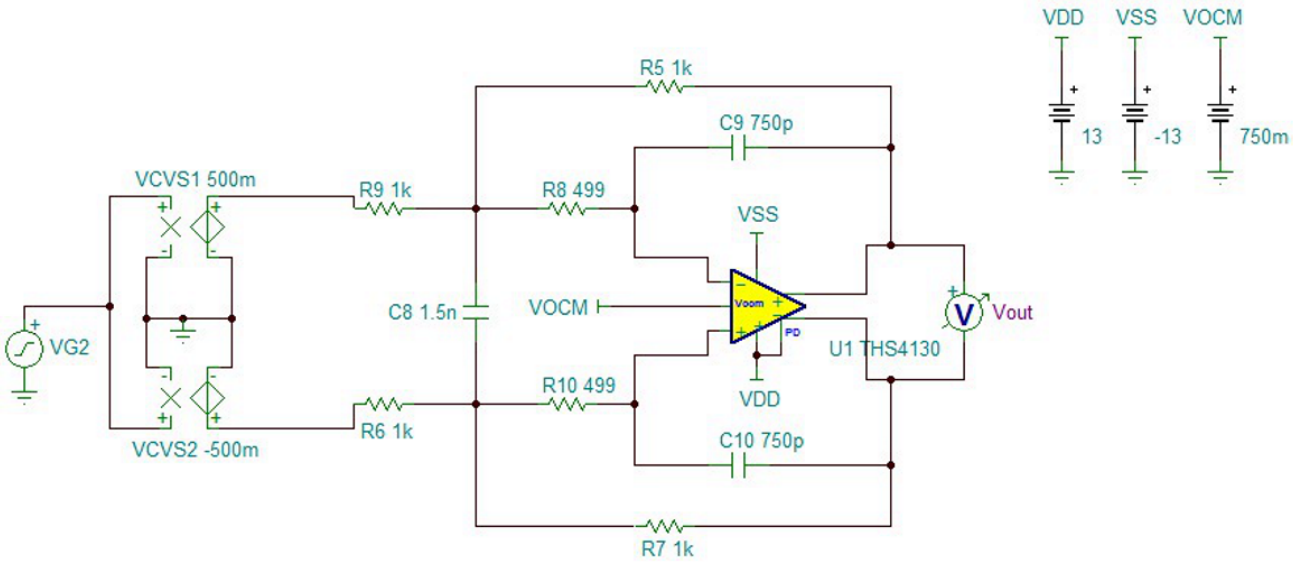


図 26. 150-kHz LPF Using THS4130

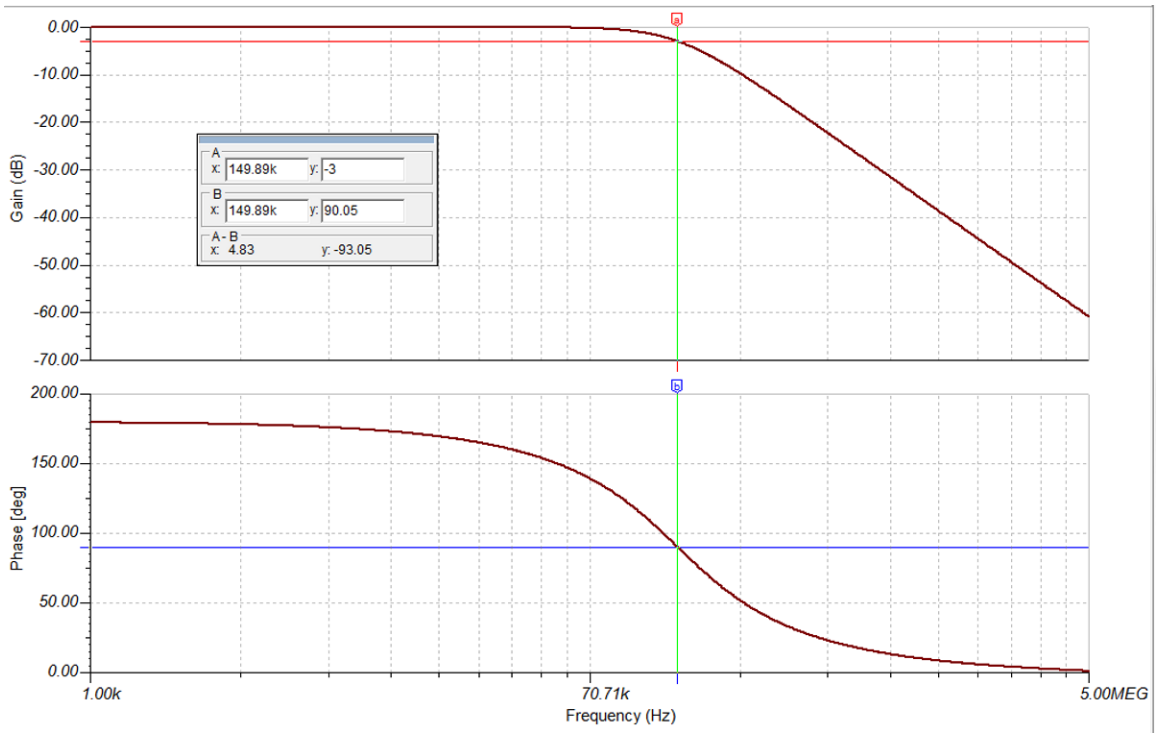


図 27. Frequency Response for Filter

3.2.2 Power Supply and Reference Rails

There are a total of eight voltage rails available on the design. 表 4 shows the voltage rails and their figure numbers.

表 4. Voltage Rails and Respective Figures

RAIL	FIGURE
±13-V power supply rails generated using TPS7A39	図 28
5-V power supply rail generated using TPS7A47	図 29
±10-V reference signals for DAC, generated using REF5010 and OPA2209	図 30
0.75-V output common-mode signal generated using resistor divider	図 31
±15-V power supply rails generated using LM5160	図 40

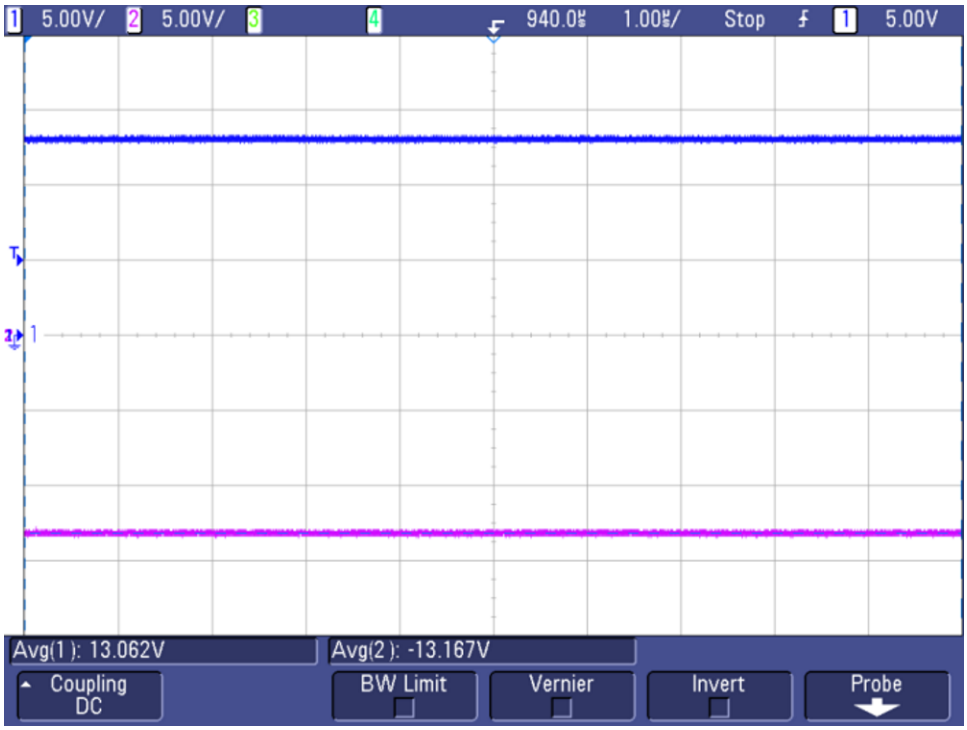


図 28. ±13-V Power Rails Generated Using TPS7A39

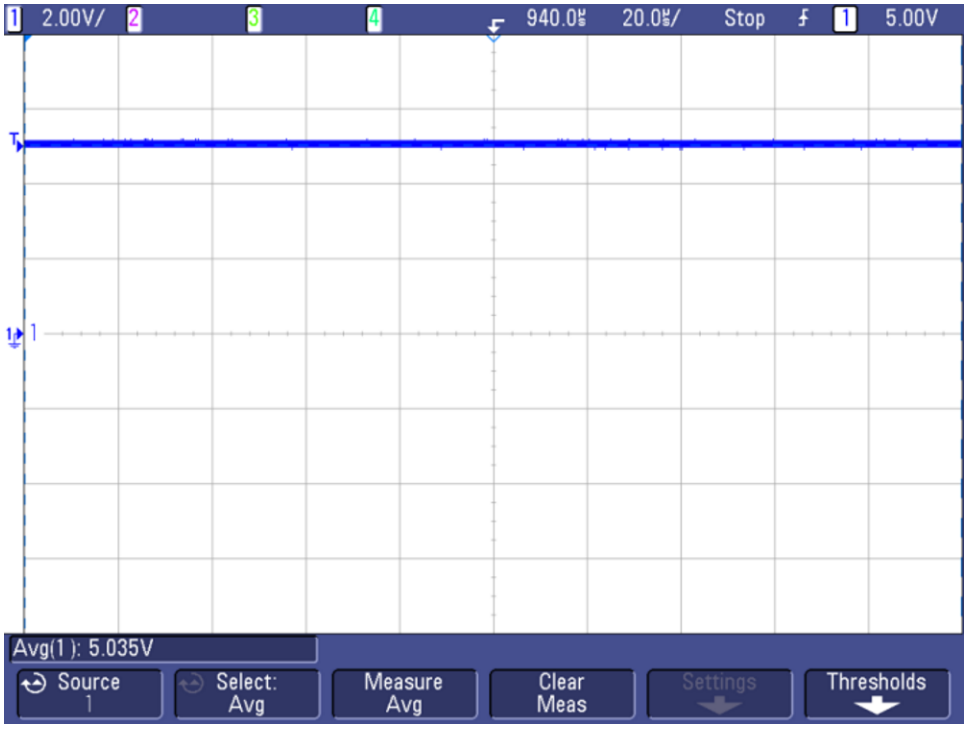


図 29. 5-V Power Supply Rail Generated Using TPS7A47

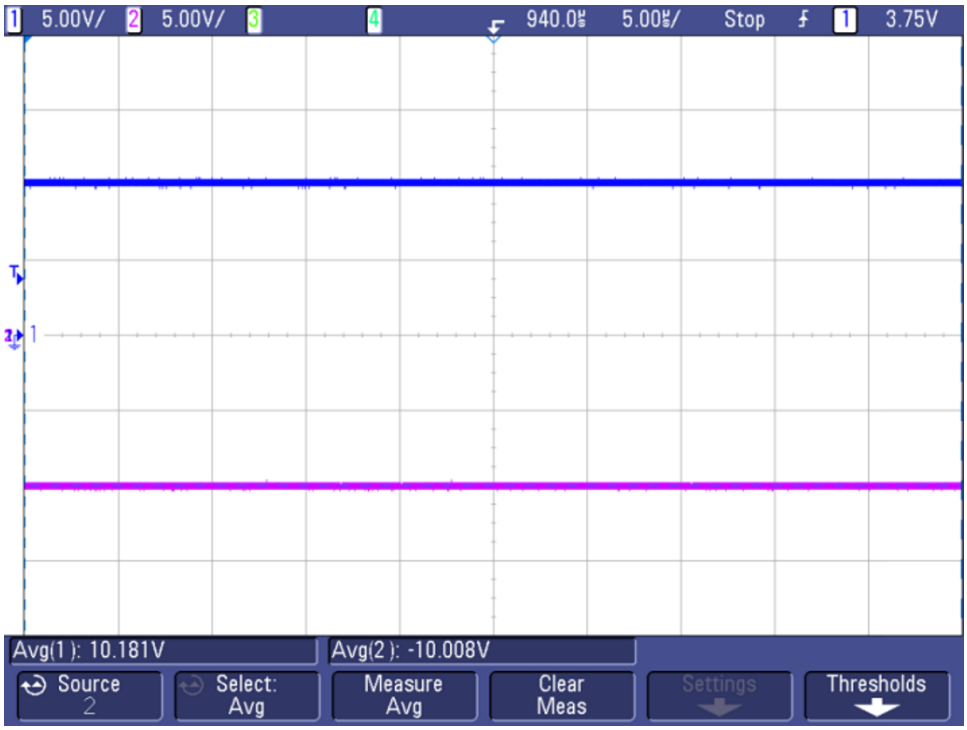


図 30. ±10-V Reference Signals for DAC, Generated Using REF5010 and OPA2209

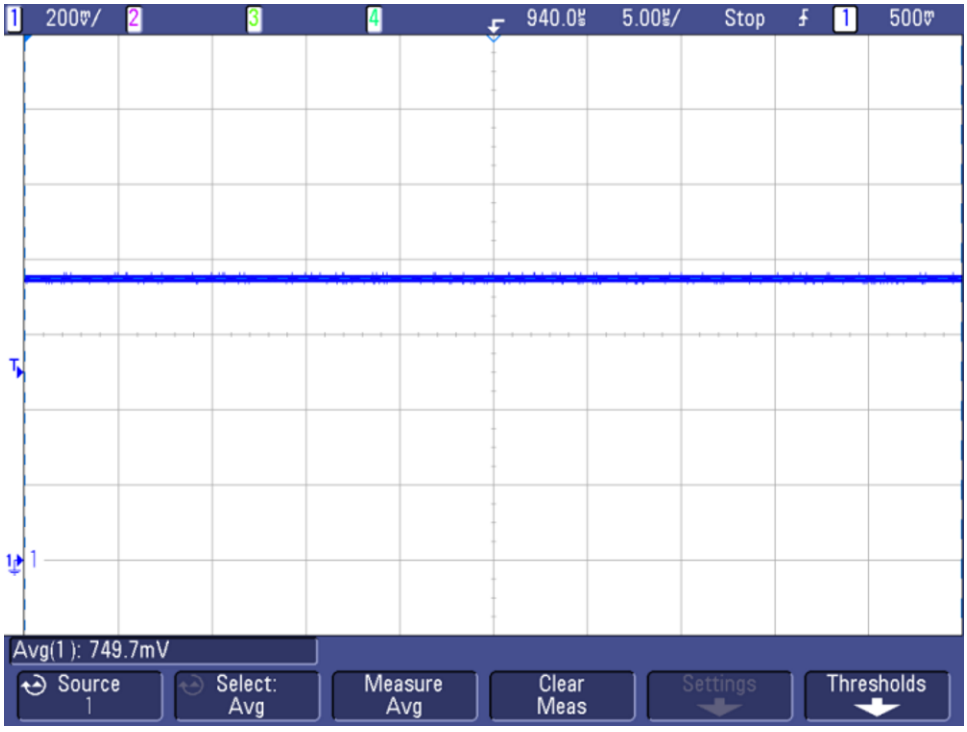


図 31. 0.75-V Output Common-Mode Signal Generated Using Resistor Divider

3.2.3 Signal Chain and V_{CNTL} Linearity

The DAC8802 is loaded with full code for the output V_{CNTL} to be at 1.5 V. For this reference design, the DAC8802 and THS4130 outputs go up to 20 V at full code. 図 32 shows the linearity graph for the DAC8802 output and THS4130 output versus the digital code loaded into the DAC8802.

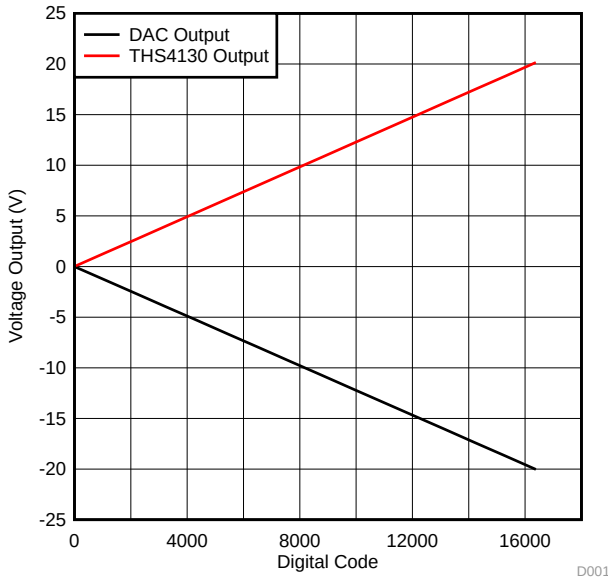


図 32. Linearity Graph for DAC8802 Output and THS4130 Output versus Code

図 33 shows linearity graph for V_{CNTL} voltage versus the digital code. From zero code to full code, the V_{CNTL} output varies from 0 to 1.5 V.

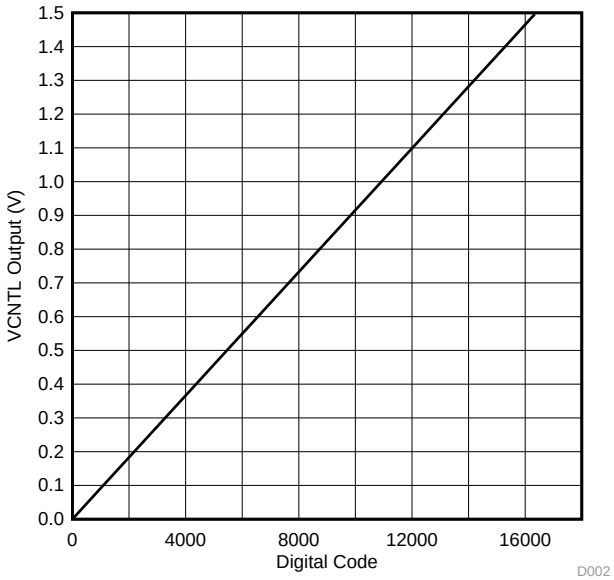


図 33. V_{CNTL} Voltage versus Code Linearity

3.2.4 Measuring Signal Chain Delay

図 34 and 図 35 show the graph for the V_{CNTL} signal going from minimum to maximum and maximum to minimum, respectively.

Also, 表 5 shows the delay numbers for the entire signal chain. The overall delay for both the conditions is less than 5 µs.

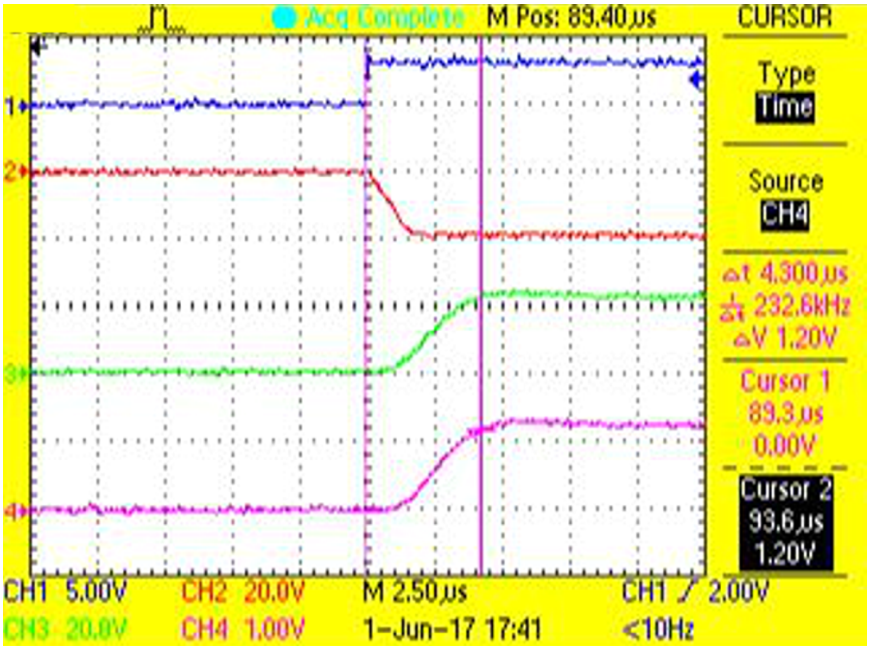


図 34. V_{CNTL} Delay While Going From Low to High

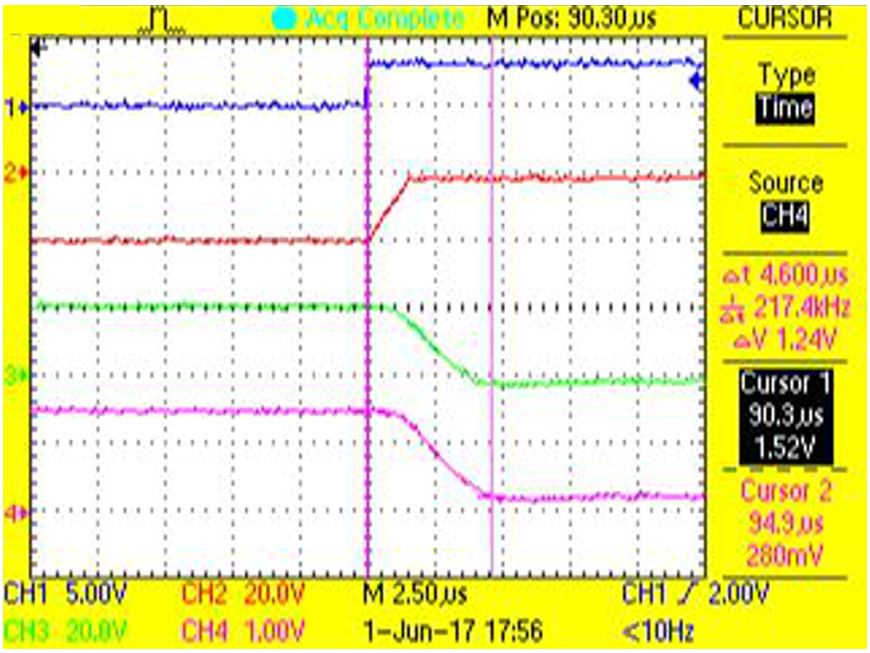


図 35. V_{CNTL} Delay While Going From High to Low

表 5. Signal Delay Measurement Numbers

CONDITION		TIME DELAY (µs)
From minimum to maximum	DAC8802 /CS to output of OPA2209 (I-to-V converter)	1.3
	THS4130 filter delay	3.0
	Overall signal chain delay	4.3
From maximum to minimum	DAC8802 /CS to output of OPA2209 (I-to-V converter)	1.3
	THS4130 filter delay	3.2
	Overall signal chain delay	4.6

3.2.5 Noise Measurement

As highlighted in 2.3.4.3, the voltage spot noise is important for the entire circuit to achieve a better performance. 図 36 shows the test setup for noise measurement. A special post amplifier circuit is used for such noise measurement (see 6 for more details on this circuit). The output of this reference design is given to the post amplifier and then to the spectrum analyzer. To make sure that the ambient noise does not affect the performance, the entire test setup is kept inside a Faraday cage.

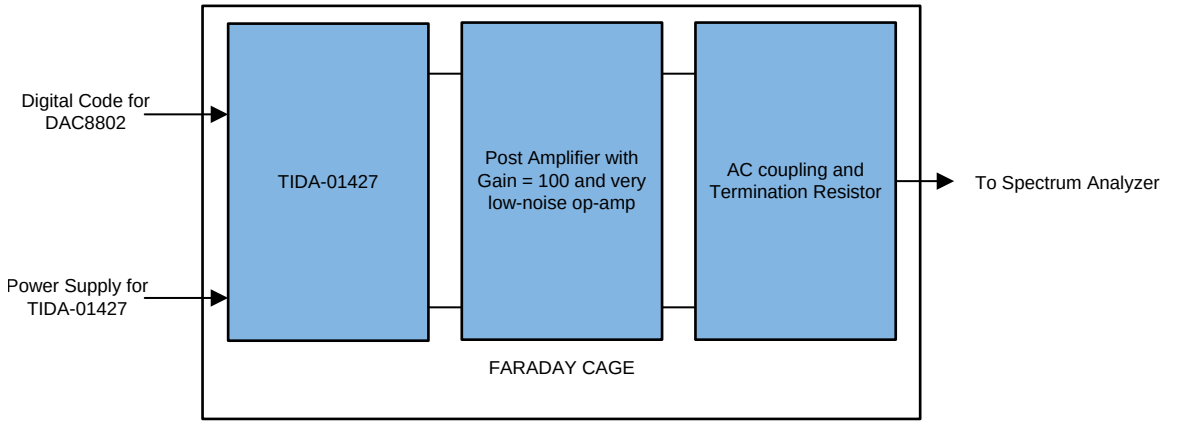


図 36. Test Setup for Noise Measurement

The noise measurement is done to frequencies up to 30 kHz for:

- REF5010 output (10 V)
- Buffered 10-V reference
- Buffered –10-V reference
- Output of DAC8802 + I-to-V converter using OPA2209
- Output of THS4130-based low-pass filter
- V_{CNTL} output

図 37 shows the noise plots at different signal chain points. 図 38 shows that the overall V_{CNTL} noise numbers are < 2.5 nV for the frequency range of 1 to 30 kHz.

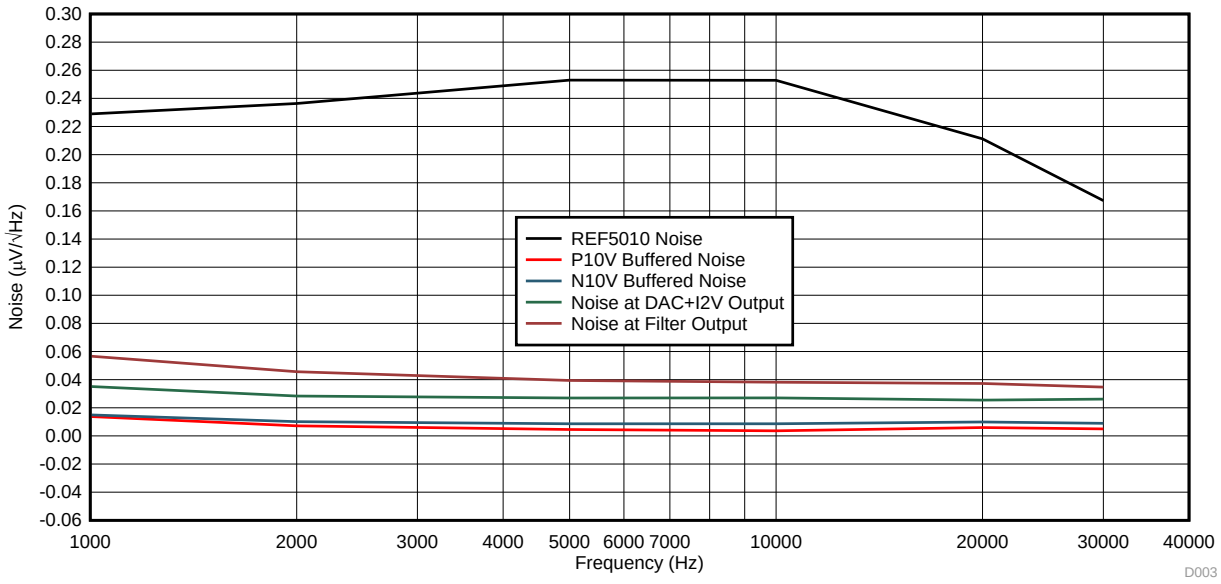


図 37. Noise Plots

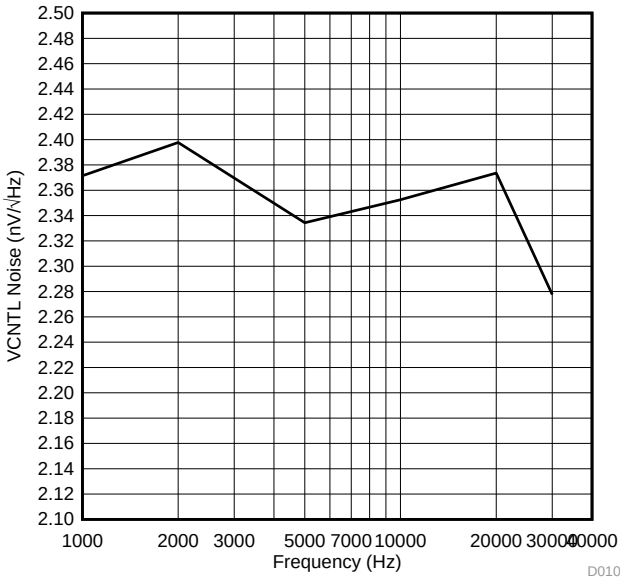


図 38. Noise Plot for V_{CNTL} Signal

3.2.6 Functional Tests for LM5160-Based Fly-Buck Converter

The TIDA-1427 design is powered using a ±15- or 5-V input. If the ±15-V input is not available, the 5-V input is converted to ±15 V by using the Fly-Buck converter, which uses the LM5160.

図 39 shows the switching waveform and output voltage ripple waveforms. The peak-to-peak ripple voltage is 106 mV for the –15-V output and 131 mV for the 15-V output. 図 40 shows the voltage rails.

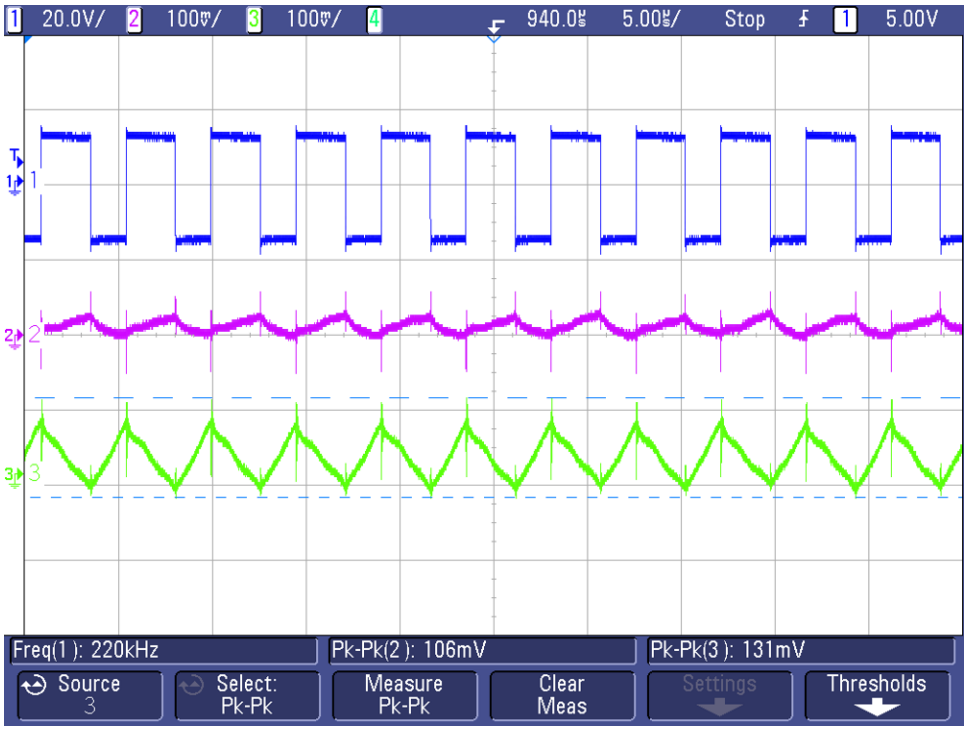


図 39. SW Node Waveforms and Output Voltage Ripple for ±15-V Rails

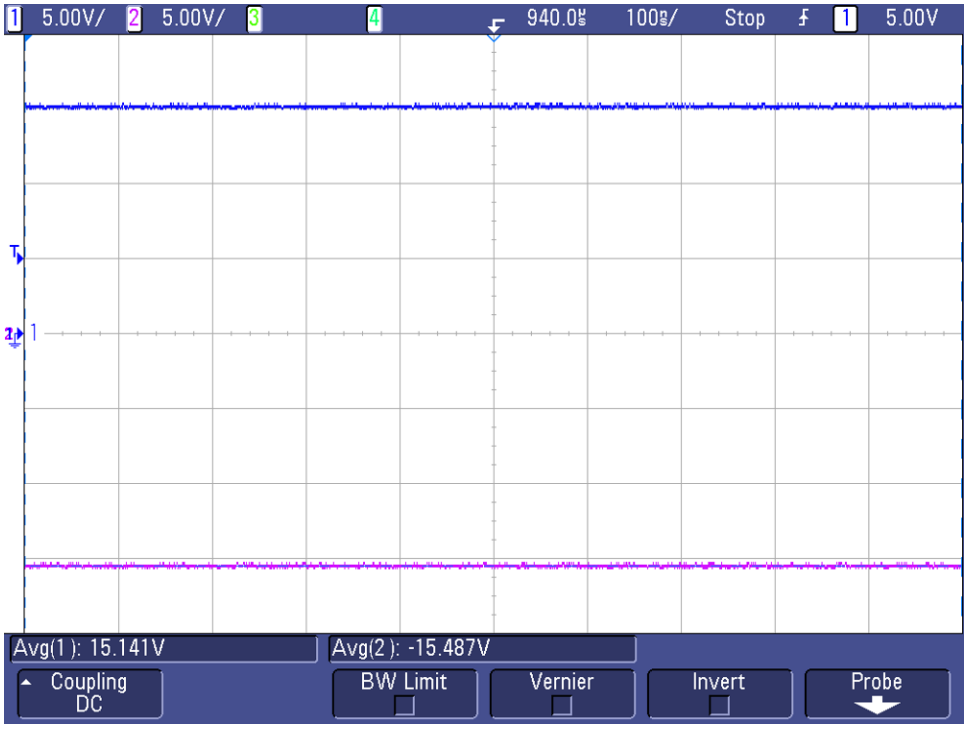


図 40. ±15-V Power Supply Rails Generated Using LM5160

図 41 and 図 42 show the efficiency with unbalanced loads, meaning only one output is full loaded and another output is at no load. 図 43 shows the efficiency at balanced load, meaning both the outputs are fully loaded.

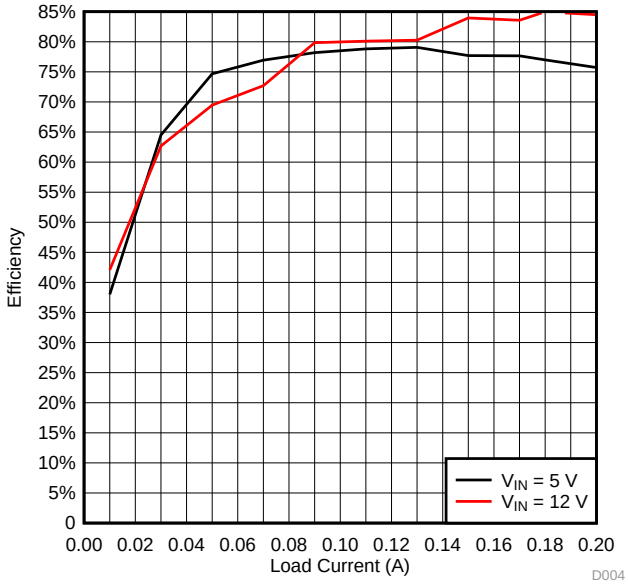


図 41. Efficiency for LM5160-Based Design: I_{PRI} = 0 A, I_{SEC} Loaded

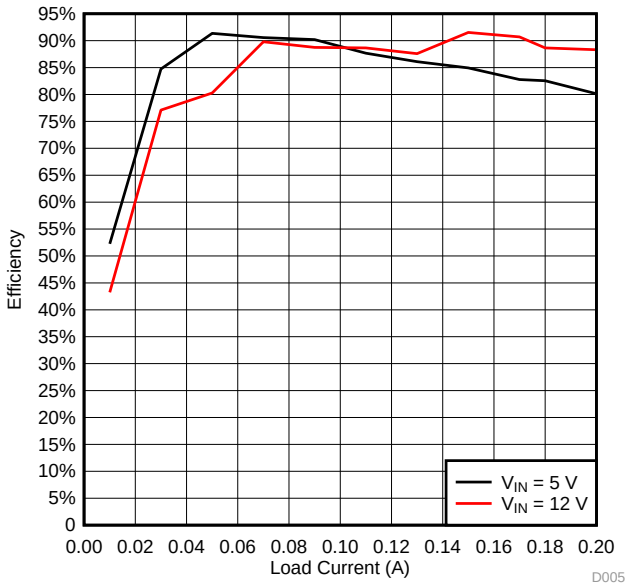


図 42. Efficiency for LM5160-Based Design: I_{SEC} = 0 A, I_{PRI} Loaded

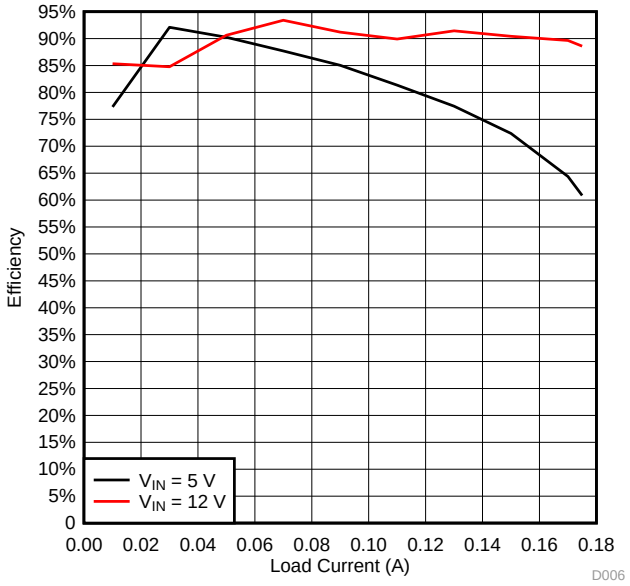


図 43. Efficiency for LM5160-Based Design: I_{PRI} and I_{SEC} Both Loaded

図 44 and 図 45 show the load regulation with unbalanced loads, meaning only one output is full loaded and another output is at no load. 図 46 shows the efficiency at balanced load, meaning both the outputs are fully loaded.

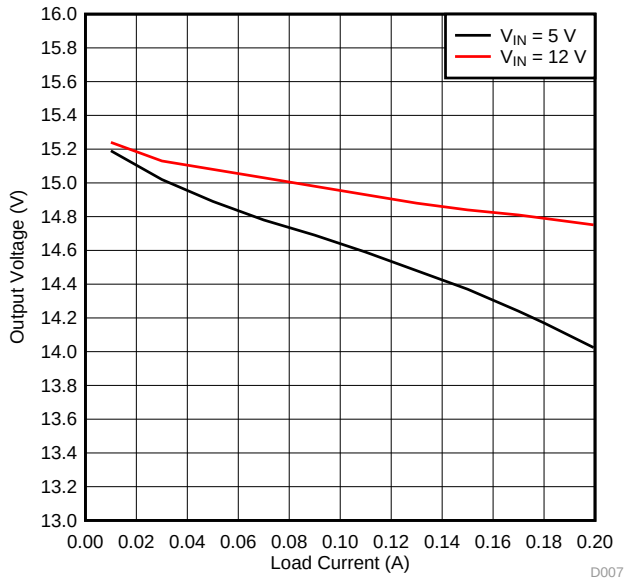


図 44. Load Regulation for LM5160-Based Design: I_{PRI} = 0 A, I_{SEC} Loaded

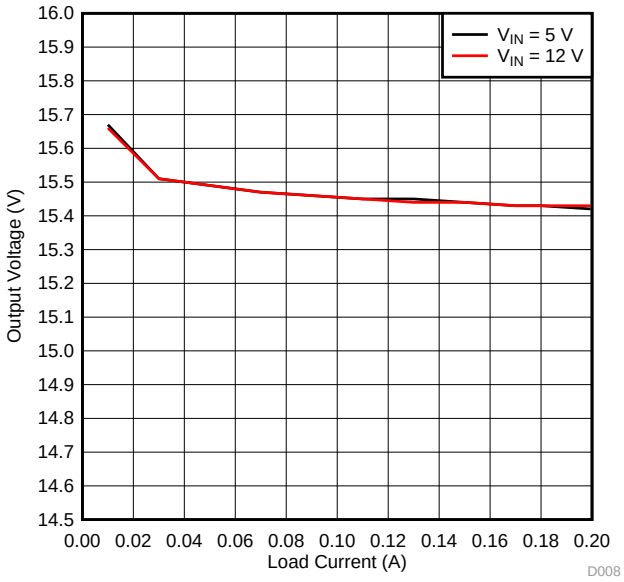


図 45. Load Regulation for LM5160-Based Design: I_{SEC} = 0 A, I_{PRI} Loaded

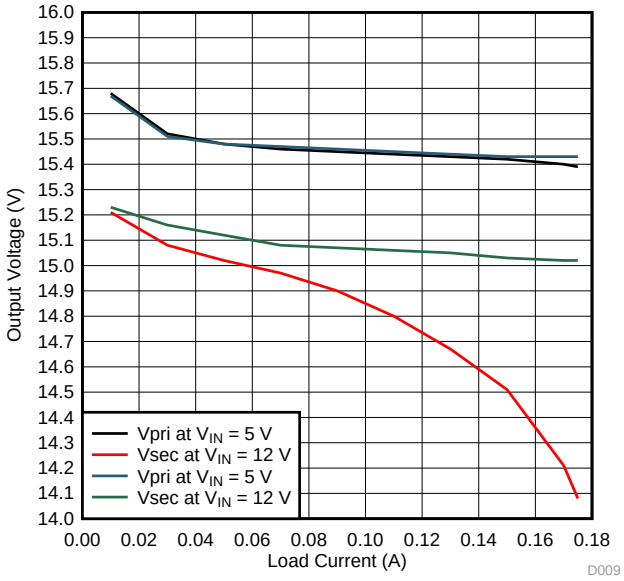


図 46. Load Regulation LM5160-Based Design: I_{PRI} and I_{SEC} Both Loaded

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01427.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01427.

4.3 PCB Layout Recommendations

For device specific layout guidelines for each individual TI part used in this reference design, see their corresponding datasheets.

図 21 and 図 22 show top and bottom views of TIDA-01427 PCB, respectively. The important sections are highlighted with red arrows and captions.

The DAC8802 is a high-accuracy DAC that can have its performance compromised by grounding and PCB lead trace resistance. The 14-bit DAC8802 with a 10-V full-scale range has an LSB value of 610 μV. The ladder and associated reference and analog ground currents for a given channel can be as high as 2 mA. With this 2-mA current level, a series wiring and connector resistance of only 305 mW causes 1 LSB of voltage drop. The preferred PCB layout for the DAC8802 is to have all AGNDX pins connected directly to an analog ground plane at the unit. The non-inverting input of each channel I-to-V converter must also either connect directly to the analog ground plane or have an individual sense trace back to the AGNDX pin connection. The feedback resistor trace to the I-to-V converter must also be kept short with low resistance to prevent IR drops from contributing to gain error. This attention to wiring ensures the optimal performance of the DAC8802.

Note that the compensation capacitor should be connected between the inverting pin and the output of the op amp so that the impedance of the entire feedback loop is compensated. The output of the op amp must be tapped at the FB pin of the DAC so that the voltage drop across the external feedback trace is not reflected in the output. 図 47 shows the layout for the signal chain.

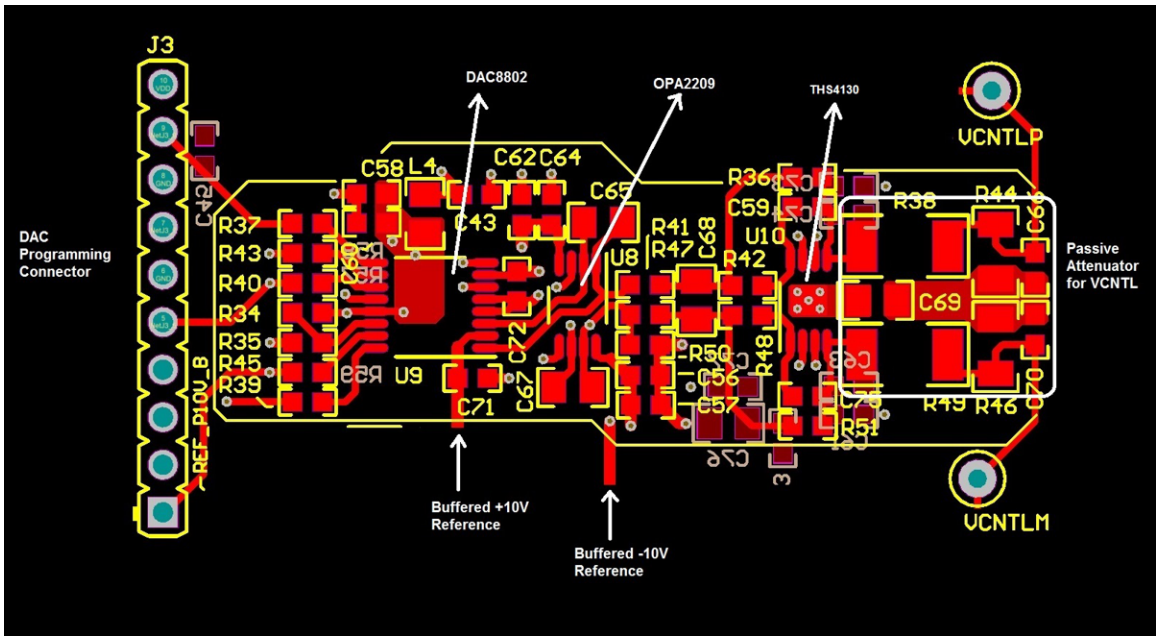


図 47. Layout for DAC + I-to-V Converter + Filter + Passive Attenuator

The quite power supplies for the signal chain are generated using the TPS7A39 and TPS7A47. Route these devices properly to reduce any noise pick-ups. 図 48 shows the layout for the same. Both the LDOs have PowerPAD™ at the bottom, which needs to be connected to ground plane with proper number of vias as shown in the layout. The placement of input and output capacitors are also important for optimum performance.

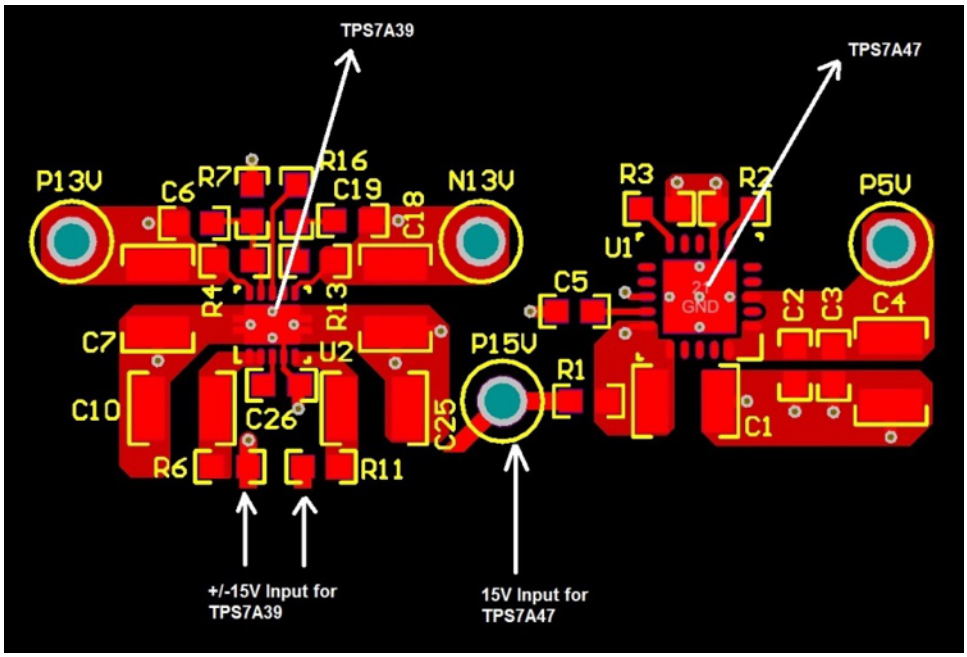


図 48. Layout for TPS7A39 and TPS7A47

図 49 shows the layout for LM5160 based Fly-Buck converter. The Fly-Buck converter on the primary side appears similar to the buck converter. The VIN loop for Fly-Buck is a high di/dt loop just like in a buck converter; however, the VPRI loop has a very different current flow than in a buck converter. In addition to the magnetization current of the primary inductor, this loop also has the reflected current from the secondary windings. The reflected current has only the leakage inductance of the coupled inductor in its path and therefore has much higher di/dt than the magnetization current of the inductor. Therefore, it is important to minimize the loop area of VPRI loop as well. For the same reason, the secondary output loop consisting of the secondary inductor winding, rectifier diode, and secondary output capacitor also needs to be minimized because it has high di/dt current flowing through it. Also note that when laying out a Fly-Buck converter, the secondary winding also has a switch node. This secondary switch node is high dv/dt node and has a voltage transition of V_{IN} × (N2/N1). Therefore, keep the switch node trace area small to keep it from radiating noise.

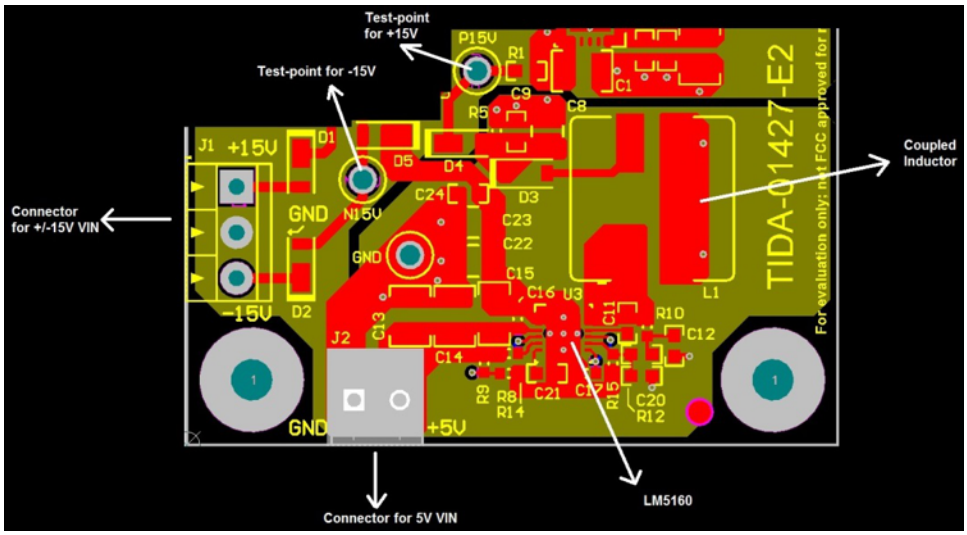


図 49. Layout for LM5160-Based Fly-Buck Converter

図 50 and 図 51 show the power plane and ground plane for the TIDA-01427. The ground plane also shows how STAR ground is implemented below connector J2.

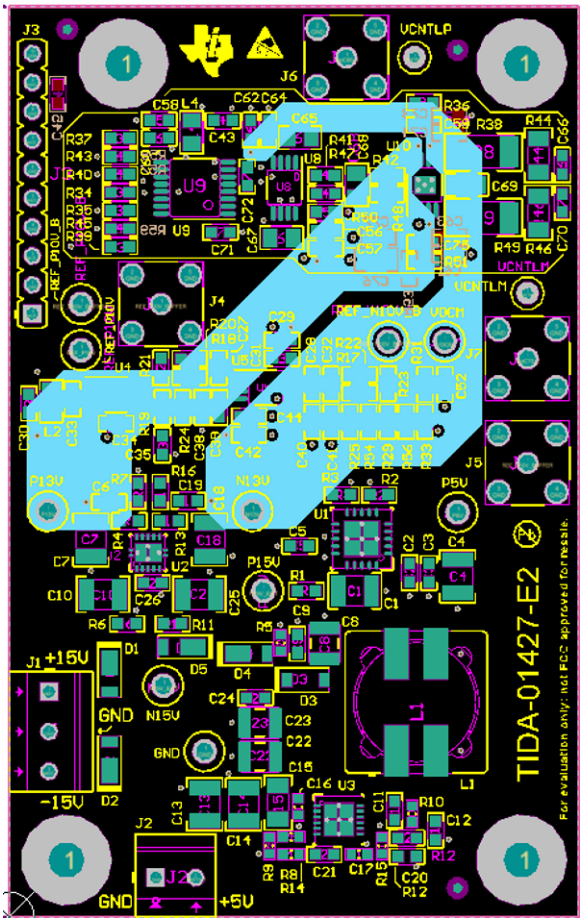


図 50. Power Plane

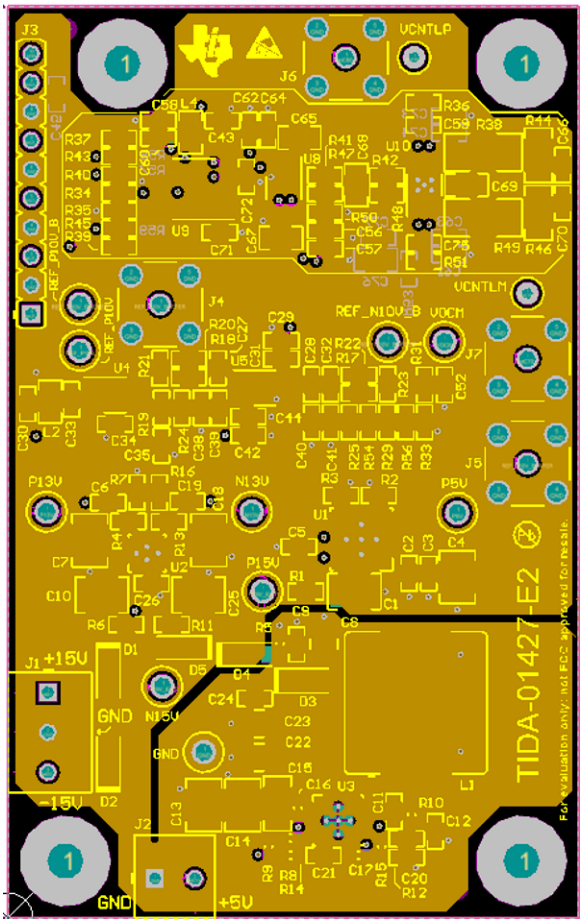


図 51. Ground Plane

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01427.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01427.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01427.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01427.

5 Software Files

To download the software files, see the design files at TIDA-01427.

6 Related Documentation

1. Texas Instruments, *Time Gain Control (Compensation) in Ultrasound Applications*, Application Report (SLAA724)
2. Texas Instruments, *Design and analysis of a time-gain-control (TGC) circuit to drive the control voltage for TI's ultrasound AFE*, Technical Brief (SLYT721)
3. Texas Instruments, *Noise Measurement Post-Amp*, TIPD147 Design Guide (TIDU016)
4. Texas Instruments, *Op amp stability and input capacitance*, Technical Brief (SLYT087)
5. Texas Instruments, *Noise Analysis in Operational Amplifier Circuits*, Application Report (SLVA043)
6. Texas Instruments, *Active Low-Pass Filter Design* (SLOA049)
7. Texas Instruments, *Fly-Buck converter PCB layout tips*, TI E2E Community (https://e2e.ti.com/blogs_/b/powerhouse/archive/2014/04/01/flybuck-pcb-layout-tips)
8. Product Design and Development, *Inverting Fly-Buck Design Simplifies Bipolar Rail Generation* (https://www.pddnet.com/article/2015/03/inverting-fly-buck-design-simplifies-bipolar-rail-generation)

6.1 商標

7 About the Author

SANJAY PITHADIA is a systems engineer at Texas Instruments, where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Sanjay has been with TI since 2008 and has been involved in designing products related to Energy, Smart Grid, Industrial Motor Drives, and Medical Imaging. Sanjay brings to this role his experience in analog design, mixed signal design, industrial interfaces, and power supplies. Sanjay earned his bachelor of technology in electronics engineering at VJTI, Mumbai.

7.1 Acknowledgment

The author would like to thank **ADITYA PANDEY** for helping and supporting development of MSP430-based code for testing DAC8802 for the TIDA-01427. Aditya is a project intern in Industrial Systems Engineering at Texas Instruments, where he is learning to develop reference design solutions for the industrial systems.

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