参考資料

TI Designs: TIDA-01449
3.3V、1Aでコスト効率の優れた、デュアル・レイヤで効率90%のTO-220 LDO代替品のリファレンス・デザイン

概要

このリファレンス・デザインでは、主要な家電製品でLDOの代替品となる、小型、高効率で低EMIのDC/DCモジュールのソリューションを紹介します。LDOをDC/DCモジュールに交換することで、システム効率が劇的に向上し、ソリューションのサイズが小さくなり、BOMコストが低減すると同時に、ヒート・シンクも不要になります。このモジュールはTO-220パッケージとほぼ同じ容積で、TO-220 LDOとピン互換なため、迅速な評価が可能で、市場投入までの期間を短縮できます。TPS561201電力コンバータは、全負荷、低負荷、およびスタンバイ動作において、より大きな出力電流と、低い消費電力を実現します。

このモジュールはTO-220 LDOとサイズおよびピン互換なため、迅速に評価を行え、市場投入までの期間を短縮できます。

リソース

TIDA-01449	デザイン・フォルダ
TPS561201	プロダクト・フォルダ

TI E2E™ Community

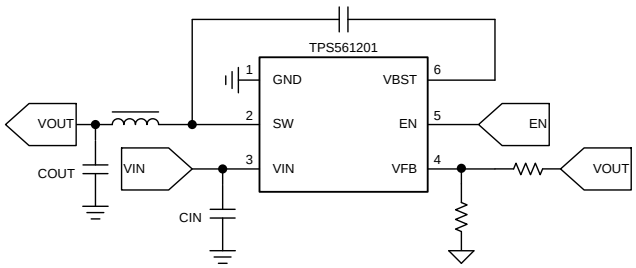
E2Eエキスパートに質問

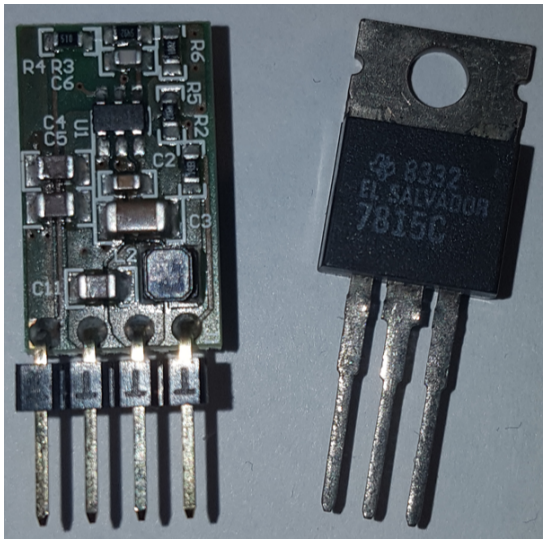
特長

- 3.3Vにレギュレートされた、最大1Aの出力負荷
- 90%の効率
- スタンバイ電流2.3µA、無負荷時電流414µA
- 小型のフォーム・ファクタ: TO-220とサイズおよびピン互換で、より小型(10.5mm×18.3mm)
- 全負荷時に30℃未満の温度上昇、ヒート・シンク不要
- オンボードDC/DC設計の複雑性を低減、スイッチング電源のEMC設計の研究開発の期間と労力を削減(市場投入までの期間短縮)

アプリケーション

- 洗濯機、乾燥機
- 冷蔵庫、冷凍庫
- 食器洗い機
- エアコンの室内機





1 System Description

Traditionally, low dropout regulators (LDO) are used in home appliances to generate 5 V or 3.3 V from the 12-V rail. These LDOs are chosen mainly for their cost and size.

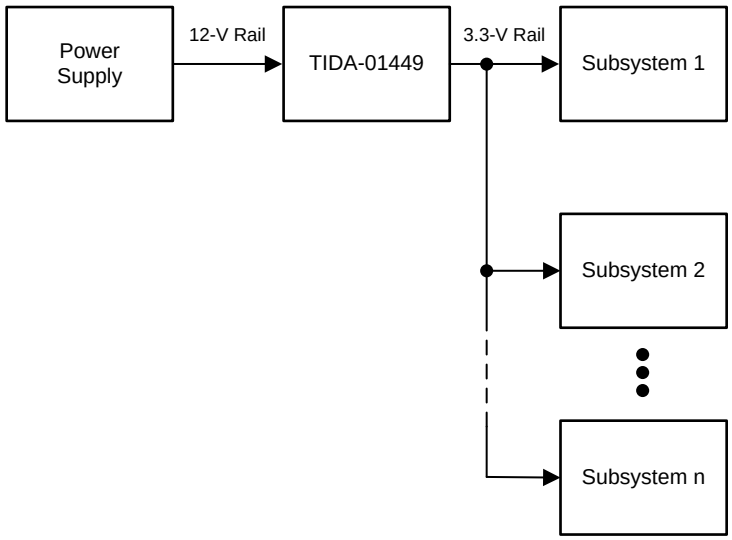


図 1. System Diagram

With the tightening requirements on active and standby power consumption and the increasing current needs due to the addition of new features (for example, the Wi-Fi® module), the LDOs become an obstacle to achieving stringent energy ratings.

The TIDA-01449 design is developed to answer this need of higher efficiency and current capability with the additional benefit of saving space by eliminating the heat sink, which is normally used to allow the LDOs to dissipate the losses.

1.1 Key System Specifications

The specifications of the TIDA-01449 design are listed in 表 1:

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage range	6.5 to 20 V	—
Output voltage and max current	3.3 V at 1 A	—
Efficiency (full load, rated load, and light load)	90%: 12 V → 3.3 V at 1 A, 89%: 12 V → 3.3 V at 500 mA, 76%: 12 V → 3.3 V at 10 mA	3.2.2.1
EMI performance	EN55022 class B, >4-dB margin	3.2.2.10
Regulation (line and load)	±3% across the input range and load current range	3.2.2.3
Transient response	±5% from 0.1 to 1.0 A	3.2.2.5
Protections	Short-circuit, hiccup mode OCP for both FETs, OTP, OVP	3.2.2.7
Operating ambient temperature	–30°C to 85°C	3.2.2.2

2 System Overview

2.1 Block Diagram

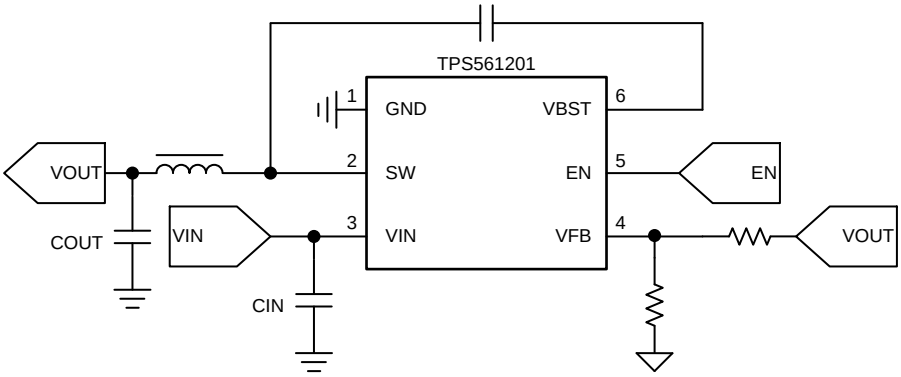


図 2. Block Diagram

2.2 Highlighted Products

2.2.1 TPS561201

The TPS561201 is a simple, easy-to-use, 1-A synchronous step-down converters in a SOT-23 package. The devices are optimized to operate with minimum external component counts and also optimized to achieve low standby current.

These switch mode power supply (SMPS) devices employ D-CAP2™ mode control providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

The TPS561201 operates in pulse skip mode, which maintains high efficiency during light load operation. The TPS561201 is available in a 6-pin 1.6×2.9-mm SOT (DDC) package and specified from –40°C to 125°C of junction temperature.

Features:

- 1-A converter integrated 140-mΩ and 84-mΩ FETs
- D-CAP2 mode control with fast transient response
- Input voltage range: 4.5 to 17 V
- Output voltage range: 0.76 to 7 V
- Pulse-skip mode
- 580-kHz switching frequency
- Low shutdown current less than 10 µA
- 2% feedback voltage accuracy (25°C)
- Startup from pre-biased output voltage
- Cycle-by-cycle overcurrent limit
- Hiccup-mode overcurrent protection
- Non-latch UVP and TSD protections

- Fixed soft-start: 1.0 ms

2.3 System Design Theory

LDOs are devices that regulate the output voltage, while the output current is the same as the input current. This implies losses are proportional to the dropout between input and output voltage and the output current, as shown in 式 1. These losses are the root cause of poor efficiency in LDOs. This translates to a limitation of the ratio between input and output voltage and maximum output current as well as the need of a heat sink. That heat sink adds cost and size to the overall solution.

A DC/DC switch mode power supply, including a Buck topology as in this project, present the advantage of having a higher efficiency, allowing them to be used in a wider variety of applications as well as being competitive with an LDO-based design with respect to cost and size (including all components and heat sink). Find more details on how a Buck topology works in the application report *Understanding Buck Power Stages In Switchmode Power Supplies* (SLVA057).

Compare the efficiency of the TIDA-01449 and an LDO-based design. The efficiency data for the TIDA-01449 design can be found in 3.2.2.1. In an LDO, the power to be dissipated can be estimated by 式 1.

$$P_{DISSIPATED} = \left(V_{IN} - V_{OUT}\right) \times I_{OUT} \quad (1)$$

Now calculate the power dissipated by a 12-V input, 3.3-V output design at 1 A, 500 mA, and 100 mA to see what the performances are for the TIDA-01449 and for the LDO-based design.

For 1 A, the efficiency of the TIDA-01449 is 90% (10% loss). With 5 W at the output, 0.5 W are dissipated. For the LDO-based design, 式 1 gives 8.7 W to be dissipated by the LDO.

For 500 mA, the efficiency of the TIDA-01449 is 89% (11% loss). With 2.5 W at the output, 0.275 W are dissipated. This is to be compared with 4.35 W for the LDO.

Finally for 100 mA, 0.12 W needs to be dissipated for the TIDA-01449 (76% efficiency) versus 0.87 W for the LDO-based design.

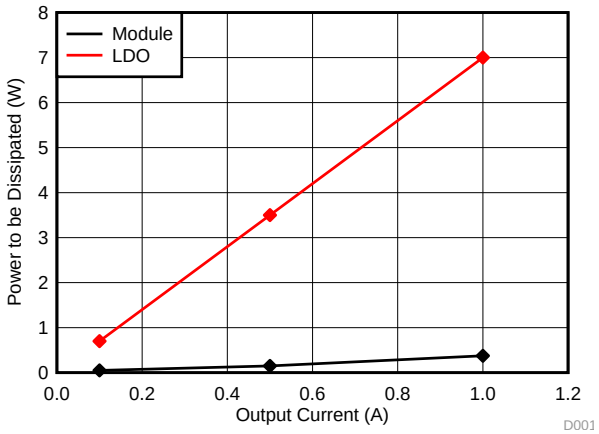


図 3. Comparison of Power Dissipated

As shown in 図 3, the LDO-based design needs to dissipate much more power than the TIDA-01449 design, which impacts both power consumption and cost and size due to the necessity of a heat sink.

2.4 Design Considerations

2.4.1 Part and Topology Selection

The first step of the design is to select the circuit topology. As cost and space are key in home appliance design and no isolation is needed for the 12-V to 3.3-V conversion, a Buck topology is chosen. Still, with the aim to reduce bill of material cost and size, a synchronous converter with integrated FET is preferred.

With this in mind, as well as the specification in 表 1, the TPS561201 is chosen. The converter includes two integrated switching FETs, internal loop compensation, and a 1-ms internal soft start to reduce component count. It integrates a 140-mΩ and a 84-mΩ MOSFET for up to 1-A continuous output current.

2.4.2 Design Steps and Passive Components Selection

The first step is to set the output voltage, which is adjusted by the resistor divider (R3 and R6). Set the range of the resistors; higher values decrease the losses in the resistor divider but make the feedback signal more sensitive to noise, while lower values will make the feedback signal more robust against noise but increase losses. On this project, a good trade-off is setting R6 at 10 kΩ and use 式 2 to calculate R3. A 51-Ω resistor (R4) is added to measure the loop stability. R4 is not needed in the final design and can be shorted.

$$R_3 = \left(\frac{V_{OUT}}{0.768} - 1 \right) \times R_6 \tag{2}$$

where:

- R6 = 10 kΩ
- V_{OUT} = 3.3 V
- V_{REF} = 0.768 V

式 2 gives R3 = 32.969 kΩ. A resistor value of 33.2 kΩ is then used for R3.

Then comes the choice of the output filter, including the output inductor (L1) and output capacitors (C3 and C4). The LC filter used as the output filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{3}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low-frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of 式 3 is located below the high frequency zero but close enough that the phase boost provided be the high-frequency zero provides adequate phase margin for a stable circuit.

The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using 式 4, 式 5, and 式 6. The inductor saturation current rating must be greater than the calculated peak current, and the RMS or heating current rating must be greater than the calculated RMS current. Use 580 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of 式 5 and the RMS current of 式 6.

$$II_{p-p} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \tag{4}$$

$$I_{peak} = I_O + \frac{I_{p-p}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_o^2 + \frac{1}{12} I_{p-p}^2} \quad (6)$$

For this TI Design, the inductor used is a Coilank ABG06A45M3R3 (3.3 µH) with a saturation current rating of 6.08 A and an RMS current rating of 3.81 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS561201 is intended for use with ceramic or other low-ESR capacitors. Recommended values range from 20 to 68 µF. Use to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_o \times f_{SW}} \quad (7)$$

For this design, two MURATA 22-µF output capacitors are used.

Next step is to set the input capacitor. The TPS561201 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from pin 3 to ground is optional to provide additional high-frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

As required, a bootstrap capacitor (C1) of 0.1 µF (X7R or X5R) has to be added between the BOOT pin and the SW pin.

The last step is to select the input filter. Considering the rated input RMS current, this TI Design uses the ABG03A15M4R7 (4.7 µH) with a saturation current rating of 1.13 A and an RMS current rating of 1.12 A as the input inductor and a 47-µF capacitor as the input capacitor.

Finally a 0-Ω resistor (R1) is added next to the bootstrap for test purposes (EMC tests). The results of these tests show that this resistor is not needed.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 PCB Overview

A picture of the PCB with the functional blocks is shown in 図 4.

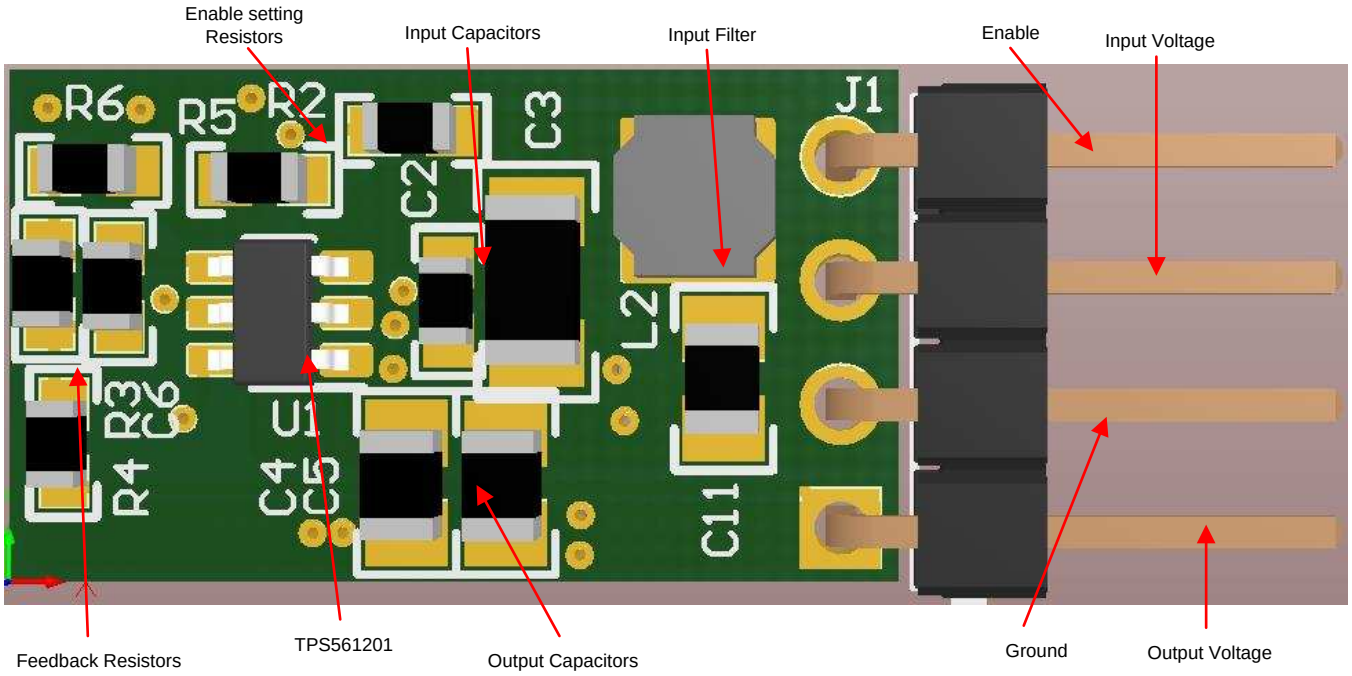


図 4. TIDA-01449 PCB With Functional Blocks

The inductor and bootstrap capacitor are placed on the bottom side of the board.

3.1.2 Connectors Settings

表 2. Connector Settings

CONNECTOR	FUNCTION
J1-1	V_{OUT}
J1-2	GND
J1-3	V_{IN}
J1-4	EN

3.2 Testing and Results

3.2.1 Test Setup

図 5 shows the setup and the test equipment used.

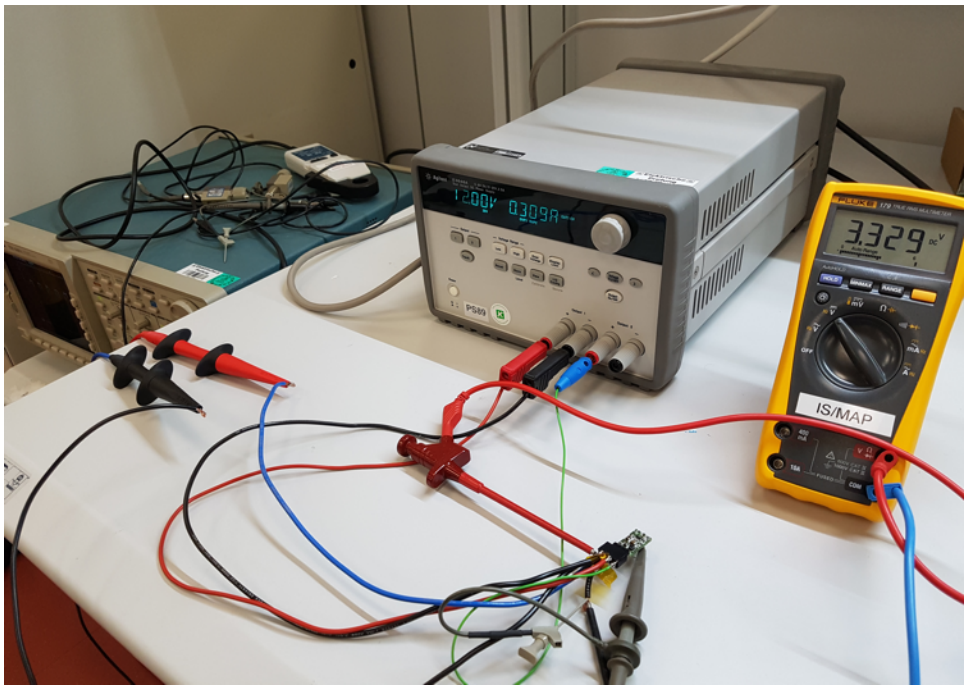


図 5. Picture of Test Setup for TIDA-01449

表 3 lists the test equipment used to test the TIDA-01449.

表 3. Test Equipment

TEST EQUIPMENT	PART NUMBER
Oscilloscope	Tektronix TDS 640A
Voltage probe	Tektronix P6139A
Current probe	LEM PR 30
Multimeter	Fluke 179 and 87 III
Power supply	Agilent E3648A
Electronic load	Chroma 63103 and 63104
Passive load	SNE350x40S2 D040
Temperature chamber	Voetsch VT4002
Thermal camera	Fluke TI40

3.2.2 Test Results

3.2.2.1 Efficiency

To test the efficiency, four multimeters are used: two are set up as voltmeters to measure the input and output voltages, and two are set up as ammeters to measure the input and output currents.

The measurements are done at a room temperature of 23ºC and with the enable setting resistors (R2 and R5) not populated, with 6 V applied to the Enable pin.

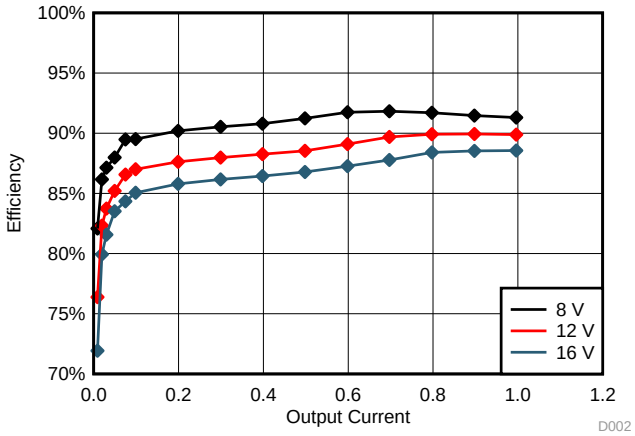


図 6. TIDA-01449 Efficiency

表 4, 表 5, and 表 6 list the details of the efficiency curves shown in 図 6.

表 4. Efficiency With 8-V Input

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	η
7.950	0.4525	3.297	0.9962	0.913018910
7.960	0.4068	3.300	0.8975	0.914648834
7.960	0.3608	3.303	0.7973	0.916960739
7.960	0.3153	3.306	0.6971	0.918249908
7.970	0.2708	3.309	0.5984	0.917447815
7.970	0.2285	3.335	0.4982	0.912336470
7.980	0.1837	3.344	0.3980	0.907898489
7.980	0.1389	3.354	0.2992	0.905356263
7.990	0.0927	3.357	0.1990	0.901940532
7.990	0.0463	3.355	0.0987	0.895121331
7.990	0.0351	3.355	0.0748	0.894829363
7.990	0.0235	3.351	0.0493	0.879846084
7.990	0.0144	3.353	0.0299	0.871355688
7.990	0.0095	3.354	0.0195	0.861642843
7.995	0.0046	3.354	0.0090	0.820784730

表 5. Efficiency With 12-V Input

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	η
11.970	0.3067	3.312	0.9963	0.898819595
11.970	0.2764	3.315	0.8976	0.899361283
11.970	0.2458	3.318	0.7973	0.899129231
11.970	0.2157	3.322	0.6971	0.896913199
11.975	0.1875	3.343	0.5984	0.890945559
11.980	0.1574	3.351	0.4982	0.885353289
11.980	0.1264	3.358	0.3980	0.882591767
11.980	0.0955	3.364	0.2992	0.879746174
11.990	0.0637	3.363	0.1990	0.876236476
11.990	0.0318	3.361	0.0987	0.870040285
11.990	0.0242	3.358	0.0748	0.865660778
11.990	0.0162	3.357	0.0493	0.852048003
11.990	0.0100	3.358	0.0299	0.837399500
11.990	0.0066	3.358	0.0194	0.823226426
11.990	0.0033	3.358	0.0090	0.763818333

表 6. Efficiency With 16-V Input

V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	η
15.97	0.2338	3.319	0.9963	0.885621110
15.97	0.2109	3.322	0.8976	0.885321429
15.97	0.1878	3.325	0.7974	0.884030761
15.98	0.1662	3.344	0.6971	0.877715074
15.98	0.1438	3.351	0.5984	0.872630426
15.98	0.1206	3.357	0.4982	0.867822651
15.98	0.0969	3.363	0.3980	0.864389310
15.99	0.0731	3.366	0.2992	0.861608273
15.99	0.0488	3.364	0.1990	0.857908119
15.99	0.0244	3.362	0.0987	0.850504414
15.99	0.0186	3.358	0.0747	0.843412213
15.99	0.0124	3.359	0.0493	0.835192862
15.99	0.0077	3.359	0.0299	0.815721677
15.99	0.0051	3.360	0.0194	0.799323106
15.99	0.0026	3.360	0.0089	0.719295714

3.2.2.2 Thermal

The thermal pictures in 図 7 and 図 8 were taken at a room temperature of 26°C, with a 12-V input, 3.3 V at 1-A output without airflow.

The hottest point of the design is the TPS561201 at 52.4°C. This is an increase of 26.4°C. Because the acceptable ambient temperature range is –30°C to 85°C, no heat sink is required for the TIDA-01449 to function properly.

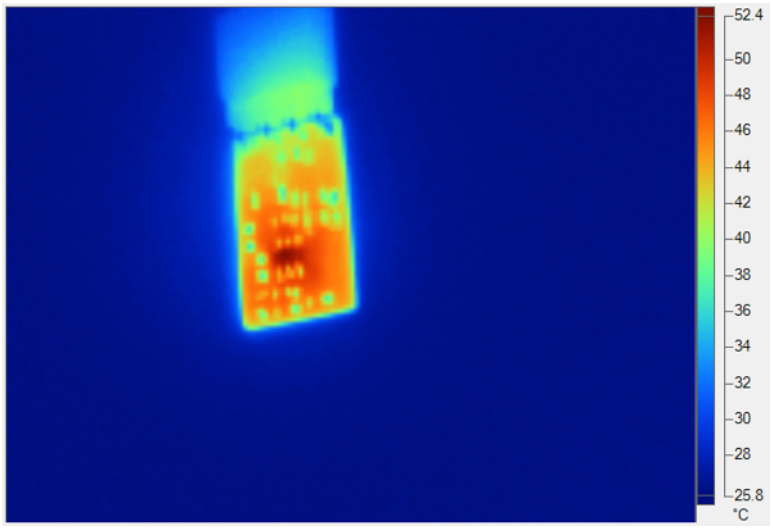


図 7. Top-Side Thermal Picture With 12-V_{IN}, 3.3 V at 1-A Output

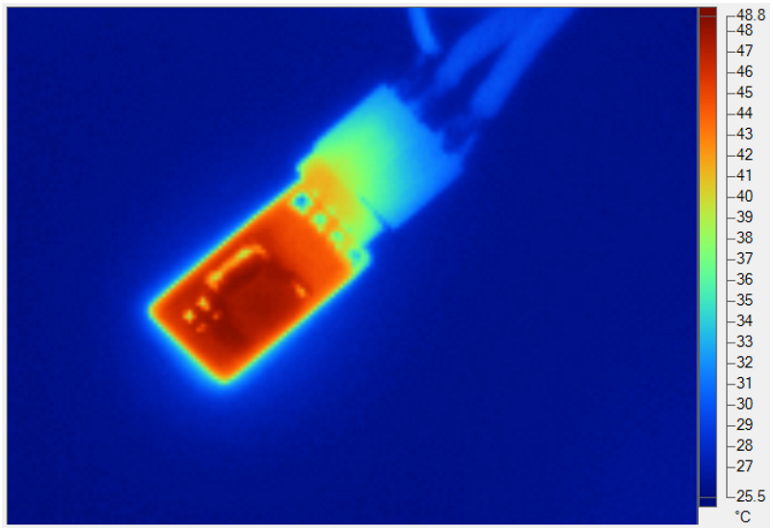


図 8. Bottom-Side Thermal Picture With 12-V_{IN}, 3.3 V at 1-A Output

3.2.2.3 Line and Load Regulation Over Temperature

図 9, 図 10, and 図 11 show the output voltage variation, depending load current and input voltage across –30ºC to 85ºC.

Across all input voltages, output currents, and temperature conditions, the output voltage varies between 3.38 and 3.29 V. This is 2.72% of the output voltage, which is below the initial target of ±3%.

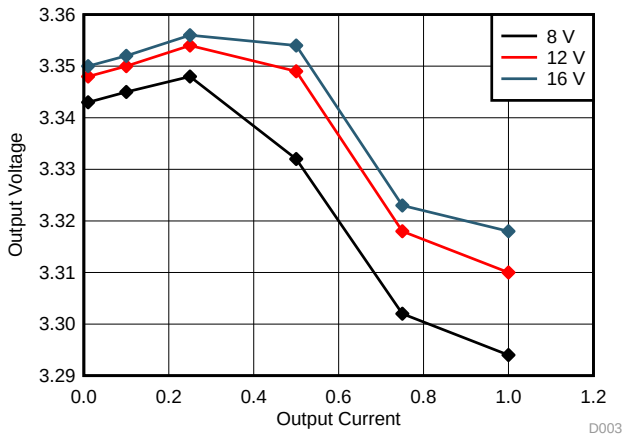


図 9. Line and Load Regulation at 85ºC

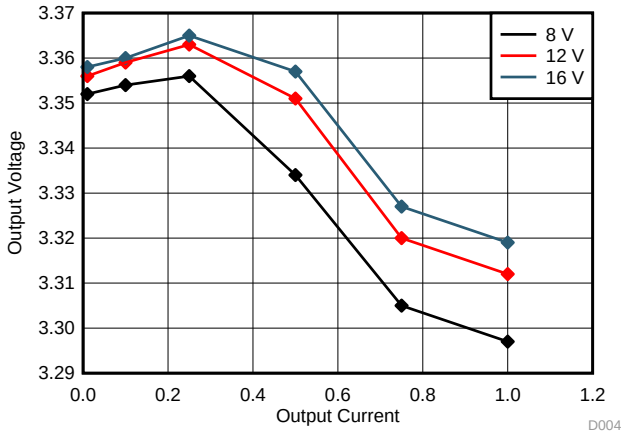


図 10. Line and Load Regulation at 23ºC

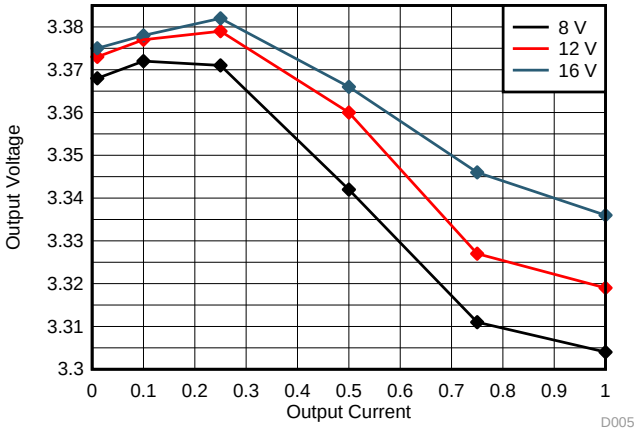


図 11. Line and Load Regulation at –30ºC

表 7, 表 8, and 表 9 list the details of the line and load regulation over temperature curves shown in 図 9, 図 10, and 図 11.

表 7. Line and Load Regulation at 85ºC

V_{IN}	V_{OUT}	I_{OUT}
16	3.318	1.00
16	3.323	0.75
16	3.354	0.50
16	3.356	0.25
16	3.352	0.10
16	3.350	0.01
12	3.310	1.00
12	3.318	0.75
12	3.349	0.50
12	3.354	0.25
12	3.350	0.10
12	3.348	0.01
8	3.294	1.00
8	3.302	0.75
8	3.332	0.50
8	3.348	0.25
8	3.345	0.10
8	3.343	0.01

表 8. Line and Load Regulation at 23ºC

V_{IN}	V_{OUT}	I_{OUT}
16	3.319	1.00
16	3.327	0.75
16	3.357	0.50
16	3.365	0.25
16	3.360	0.10
16	3.358	0.01
12	3.312	1.00
12	3.320	0.75
12	3.351	0.50
12	3.363	0.25
12	3.359	0.10
12	3.356	0.01
8	3.297	1.00
8	3.305	0.75
8	3.334	0.50
8	3.356	0.25
8	3.354	0.10
8	3.352	0.01

表 9. Line and Load Regulation at –30ºC

V_{IN}	V_{OUT}	I_{OUT}
16	3.336	1.00
16	3.346	0.75
16	3.366	0.50
16	3.382	0.25
16	3.378	0.10
16	3.375	0.01
12	3.319	1.00
12	3.327	0.75
12	3.360	0.50
12	3.379	0.25
12	3.377	0.10
12	3.373	0.01
8	3.304	1.00
8	3.311	0.75
8	3.342	0.50
8	3.371	0.25
8	3.372	0.10
8	3.368	0.01

3.2.2.4 Output Voltage Ripple

The output voltage ripple remains below 75 mVpp under full load (1 A), low load (10 mA), or no load. This ripple is well below the initial requirements of ±1%.

Measurements are done at 23ºC room temperature with a 12-V input voltage. The upper curve (1) is the output voltage with an oscilloscope in AC-coupling mode with 50 mV/div. The lower curve (2) is the switch node (pin 2 of the TPS561201) with 5 V/div.

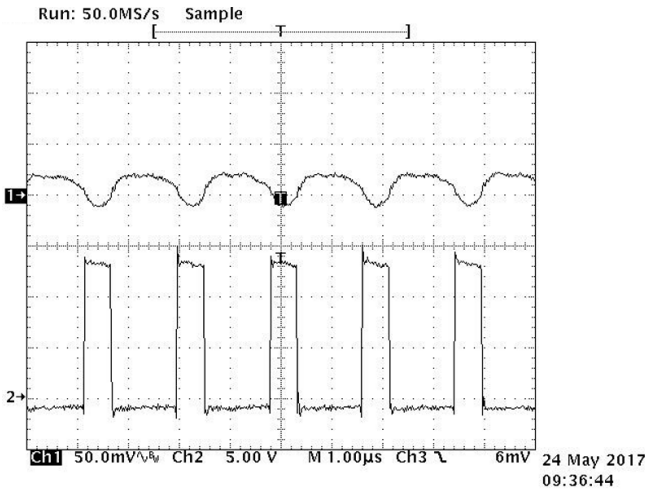


図 12. Output Voltage Ripple at 1-A Output Load

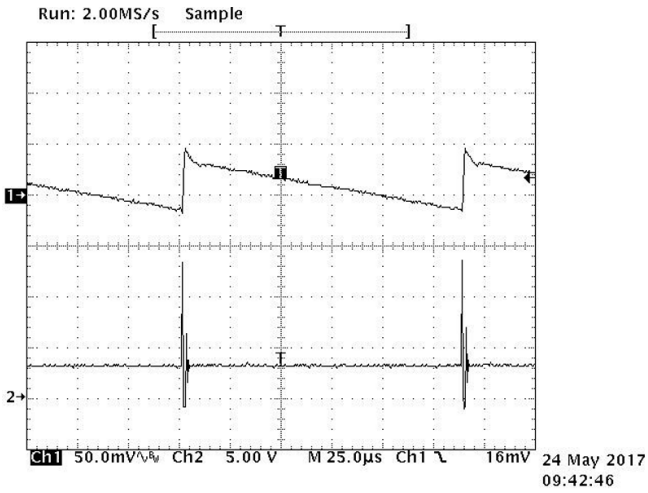


図 13. Output Voltage Ripple at 10-mA Output Load

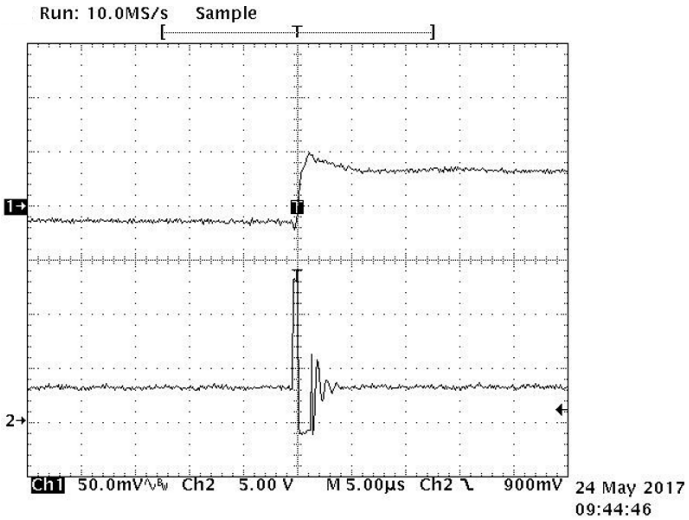


図 14. Output Voltage Ripple at No Load Output

3.2.2.5 Transient Response

The transient response is below ±165 mV for load steps between 10 mA and 1 A, which are the design requirements (±5%).

Measurements are done at 23°C room temperature with a 12-V input voltage. The upper curve (1) is the output voltage with an oscilloscope in AC-coupling mode with 100 mV/div. The lower curve (2) is the output current with the current probe of 100 mV/A with 200 mV/div. The load step is applied with a 250-mA/μs slew rate.

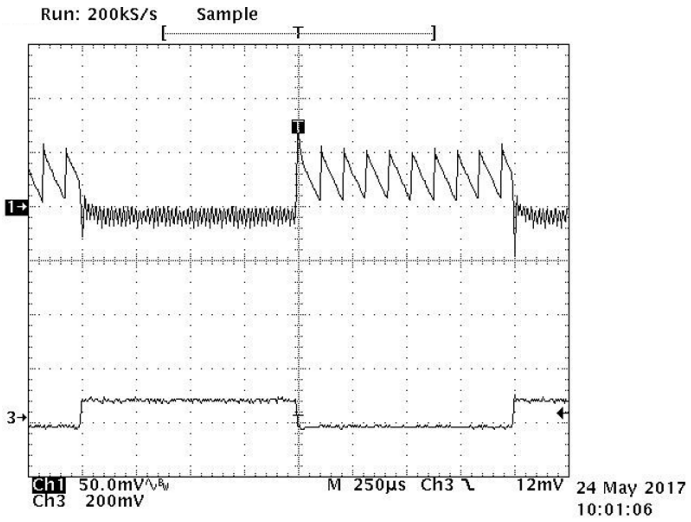


図 15. Transient Response From 10-mA to 1-A Output Load

3.2.2.6 Start-up and Shutdown

For the start-up and the shutdown behavior, 12 V is applied at the input with a 1-A load at the output. The EN setting resistors (R2 and R5) are not populated, and the Enable pin is controlled with a 6-V signal.

Measurements are done at 23ºC room temperature. The upper curve (1) is the Enable signal with 5 V/div. The lower curve (2) is the output voltage with an oscilloscope in DC-coupling mode with 2 V/div.

The TIDA-01449 design takes 1.5 ms to provide 3.3 V at the output after the EN pin is enable. The output voltage is reached without overshoot.

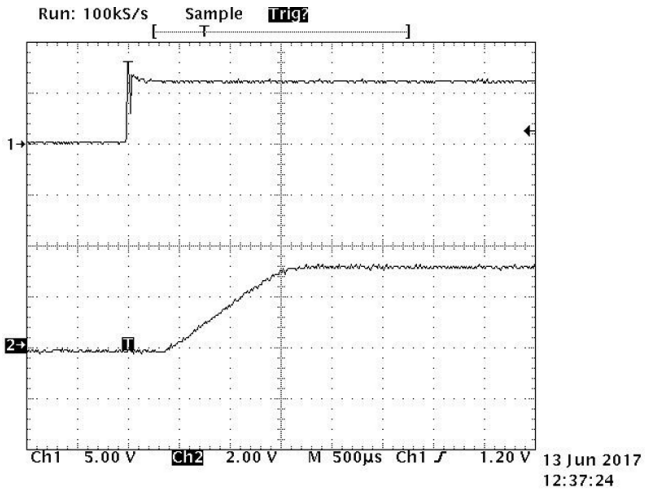


図 16. Start-up at 12-V Input and 1-A Output Load

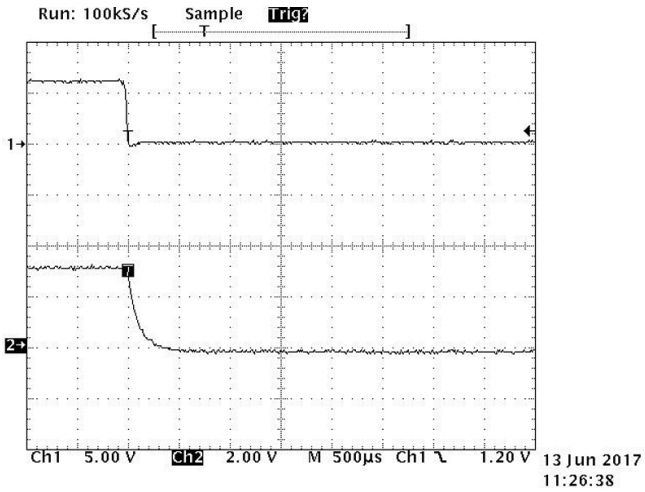


図 17. Shutdown at 12-V Input and 1-A Output Load

3.2.2.7 Overcurrent and Short-Circuit Test

The overcurrent protection is tested by having a transient load from a 1- to 3-A output current while the board is supplied with 12 V. The short-circuit protection is tested by shorting the output pin to ground.

The upper curve (1) is the output voltage with an oscilloscope in DC-coupling mode with 2 V/div (図 18) and 100 mV/div (図 19). The lower curve (2) is the output current with the current probe of 100 mV/A with 200 mV/div.

As shown in 図 18 and 図 19, when the current is rising to the current limit level, the device enters overcurrent protection as described in the TPS561201 datasheet (SLVSC95). After waiting the pre-programmed time, the device tries to restart. Once the fault condition is removed, the device starts normally.

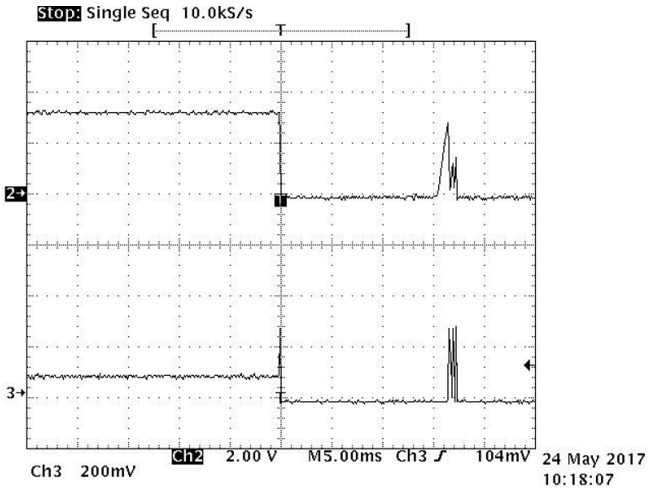


図 18. Overcurrent Protection

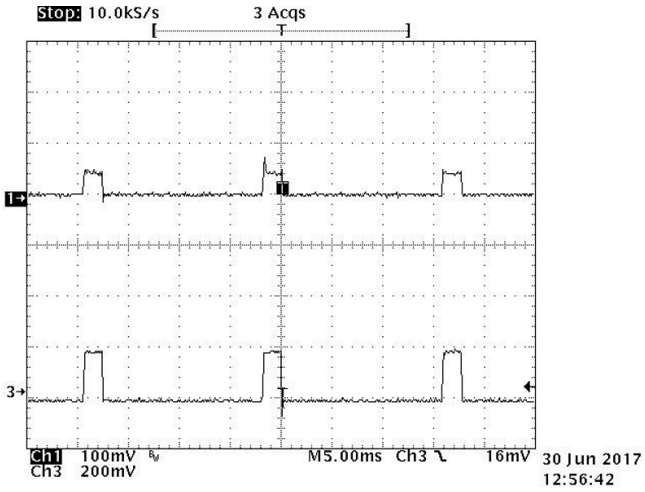


図 19. Short-Circuit Protection

3.2.2.8 Overvoltage Test

The overvoltage protection is tested by applying 3.65 V at the output of the TIDA-01449 board while the board is supplied with 12 V and with a 1-A output load.

The upper curve (2) is the output voltage with an oscilloscope in DC-coupling mode with 2 V/div. The middle curve (3) is the current coming out of the TIDA-01449 with the current probe at 100 mV/A with 50 mV/div. The lower curve (1) is voltage at the switch node with 1 V/div.

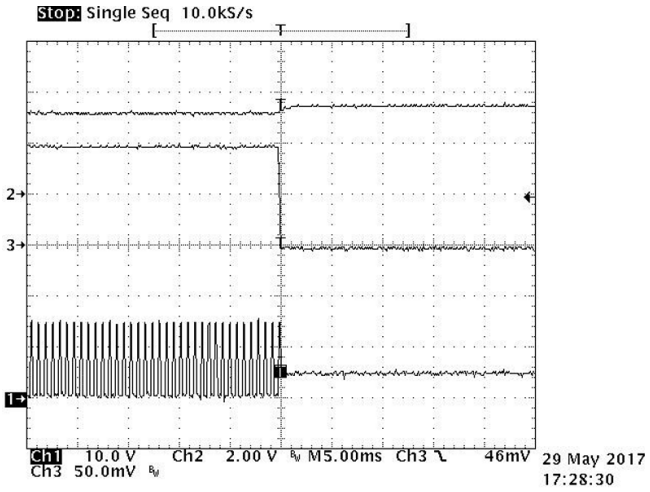


図 **20. Overvoltage Protection From 3.3 to 3.65 V**

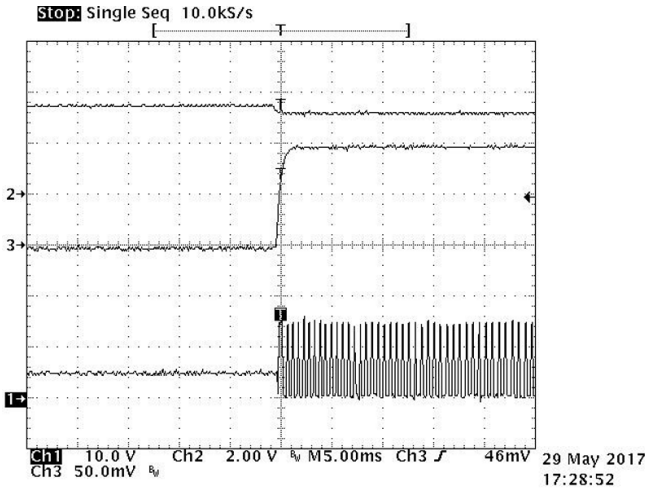


図 **21. Overvoltage Protection From 3.65 to 3.3 V**

3.2.2.9 Standby and No-Load Currents

The standby current is measured with an ammeter at 23°C room temperature with a 12-V input voltage. The enable pin was set low through the connector, and the enable setting resistors (R2 and R5) not populated. The standby current was measured at 2.3 μA.

The no-load current was measured with an ammeter at 23°C room temperature with a 12-V input voltage, with the enable setting resistors (R2 and R5) populated and no load attached at the output. The no-load current was measured at 414 μA.

3.2.2.10 EMC Tests

The TIDA-01449 TI Design has been tested for EMI according to EN55022 Class B conducted and radiated emissions. The EMC tests were performed by CSA Group Bayern GmbH (Germany).

3.2.2.10.1 Conduction Emission

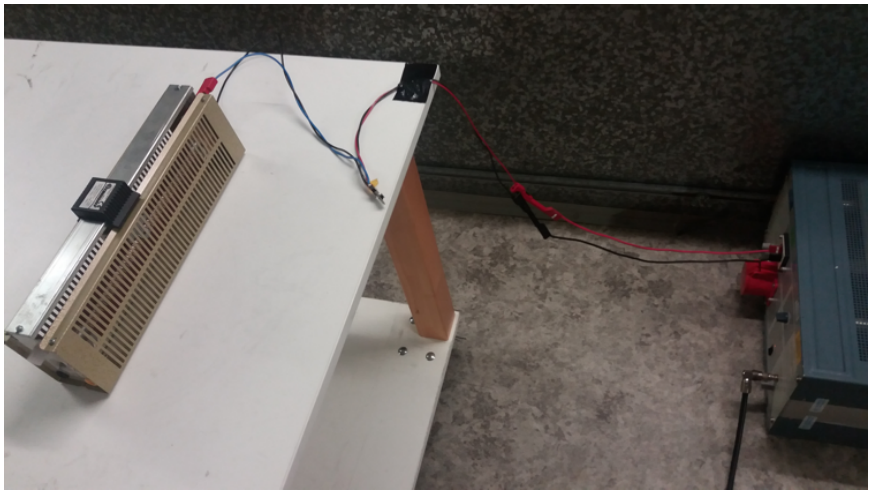


図 22. Conducted Emission Test Setup

The board passed the conducted emission test with more than 4 dB of margin.

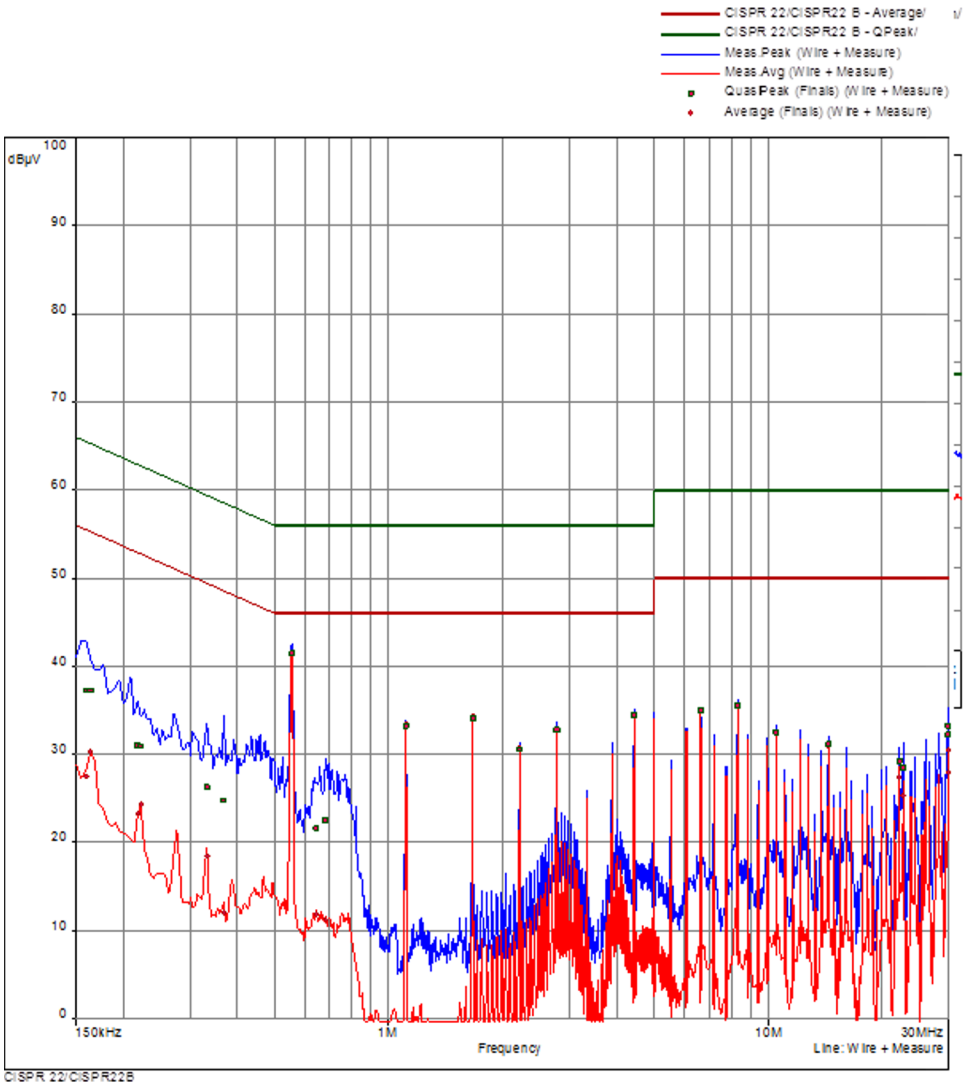


図 23. Conducted Emission Test Result With Filter (Wire +)

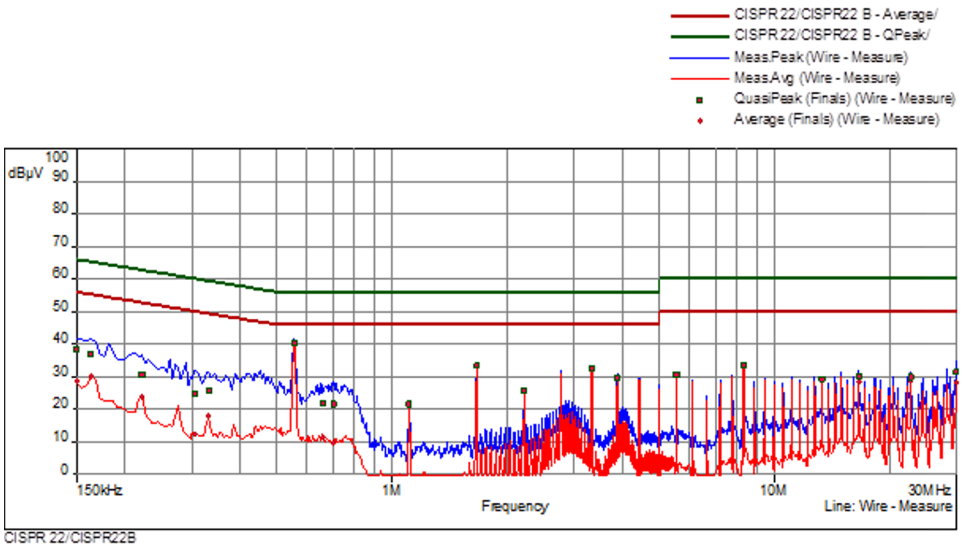


図 24. Conducted Emission Test Result With Filter (Wire –)

表 10. Conducted Emission Test Result With Filter

FREQ (MHz)	SR	QP (dBµV)	MARGIN (dB)	LIMIT (dB)	AV (dBµV)	MARGIN (dB)	LIMIT (dB)	LINE	CORR (dB)
0.1590	1	37.24	28.28	65.52	27.50	28.02	55.52	Wire + Measure	10.21
0.1635	1	37.24	28.05	65.28	30.23	25.05	55.28	Wire + Measure	10.21
0.2175	1	31.03	31.88	62.91	23.24	29.67	52.91	Wire + Measure	10.22
0.2220	1	30.93	31.82	62.74	24.28	28.46	52.74	Wire + Measure	10.22
0.3315	2	26.26	33.16	59.41	18.42	30.99	49.41	Wire + Measure	10.23
0.3675	2	24.78	33.78	58.56	11.96	36.60	48.56	Wire + Measure	10.23
0.5565	2	41.44	14.56	56.00	41.54	4.46	46.00	Wire + Measure	10.24
0.6450	3	21.60	34.40	56.00	11.74	34.26	46.00	Wire + Measure	10.24
0.6810	3	22.51	33.49	56.00	11.23	34.77	46.00	Wire + Measure	10.24
1.1085	3	33.18	22.82	56.00	33.48	12.52	46.00	Wire + Measure	10.24
1.6635	4	34.06	21.94	56.00	34.35	11.65	46.00	Wire + Measure	10.26
2.2170	4	30.58	25.42	56.00	30.74	15.26	46.00	Wire + Measure	10.28
2.7735	5	32.77	23.23	56.00	32.75	13.25	46.00	Wire + Measure	10.31
4.4385	5	34.40	21.60	56.00	34.36	11.64	46.00	Wire + Measure	10.39
6.6540	6	34.95	25.05	60.00	35.14	14.86	50.00	Wire + Measure	10.51
8.3190	6	35.49	24.51	60.00	35.59	14.41	50.00	Wire + Measure	10.64

表 10. Conducted Emission Test Result With Filter (continued)

FREQ (MHz)	SR	QP (dBµV)	MARGIN (dB)	LIMIT (dB)	AV (dBµV)	MARGIN (dB)	LIMIT (dB)	LINE	CORR (dB)
10.5360	7	32.54	27.46	60.00	32.49	17.51	50.00	Wire + Measure	10.66
14.4195	7	31.12	28.88	60.00	30.86	19.14	50.00	Wire + Measure	10.96
22.1835	8	29.27	30.73	60.00	27.37	22.63	50.00	Wire + Measure	11.48
22.7370	8	28.41	31.59	60.00	25.34	24.66	50.00	Wire + Measure	11.52
29.9505	8	33.25	26.75	60.00	30.44	19.56	50.00	Wire + Measure	11.79
29.9550	8	32.26	27.74	60.00	27.89	22.11	50.00	Wire + Measure	11.79
0.1500	9	38.49	27.51	66.00	28.77	27.23	56.00	Wire – Measure	10.21
0.1635	9	36.88	28.41	65.28	30.15	25.14	55.28	Wire – Measure	10.21
0.2220	9	30.68	32.06	62.74	23.85	28.89	52.74	Wire – Measure	10.22
0.3045	10	24.95	35.17	60.12	12.41	37.71	50.12	Wire – Measure	10.23
0.3315	10	25.65	33.77	59.41	18.03	31.39	49.41	Wire – Measure	10.23
0.5565	10	40.26	15.74	56.00	40.28	5.72	46.00	Wire – Measure	10.24
0.6585	11	21.86	34.14	56.00	11.46	34.54	46.00	Wire – Measure	10.24
0.7035	11	21.67	34.33	56.00	9.77	36.23	46.00	Wire – Measure	10.24
1.1085	11	21.56	34.44	56.00	21.76	24.24	46.00	Wire – Measure	10.24
1.6635	12	33.34	22.66	56.00	33.62	12.38	46.00	Wire – Measure	10.26
2.2170	12	25.73	30.27	56.00	25.76	20.24	46.00	Wire – Measure	10.28
3.3270	13	32.55	23.45	56.00	32.72	13.28	46.00	Wire – Measure	10.33
3.8850	13	29.53	26.47	56.00	29.34	16.66	46.00	Wire – Measure	10.36
5.5470	14	30.60	29.40	60.00	30.75	19.25	50.00	Wire – Measure	10.44
8.3190	14	33.56	26.44	60.00	33.55	16.45	50.00	Wire – Measure	10.64
13.3125	15	29.28	30.72	60.00	29.10	20.90	50.00	Wire – Measure	10.87
16.6425	15	30.04	29.96	60.00	28.48	21.52	50.00	Wire – Measure	11.32
22.7415	16	29.95	30.05	60.00	28.67	21.33	50.00	Wire – Measure	11.52
29.9505	16	31.58	28.42	60.00	28.37	21.63	50.00	Wire – Measure	11.79

3.2.2.10.2 Radiated Emission

The radiated emission is tested first with a prescan test with an antenna at 3 m and a threshold higher from 10 dB. This pretest identifies the critical points (less than 20 dB of margin) for the 10-m test.

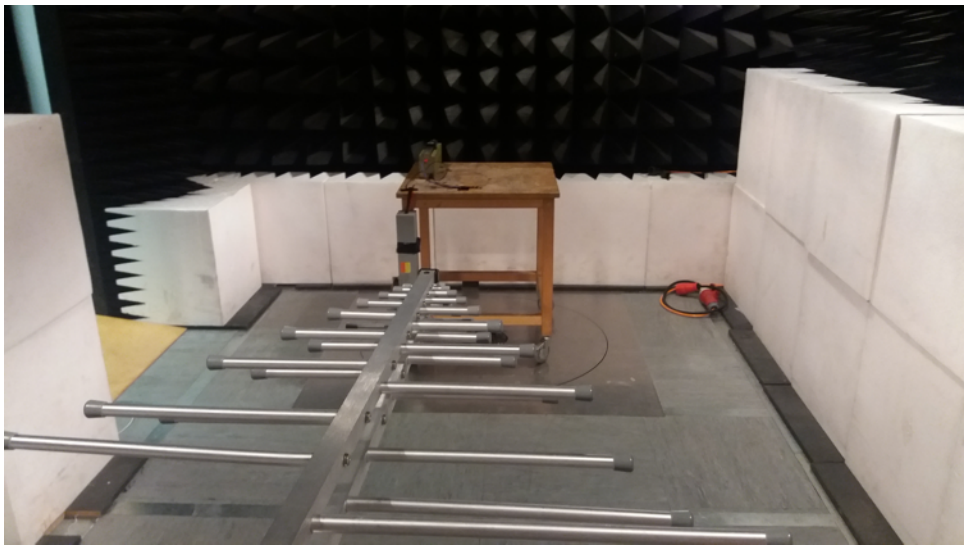


図 25. Radiated Emission 3-m Prescan Test Setup

CAUTION

For the prescan, due to the shorter distance (3 m instead of 10 m), the threshold for radiated EMI of EN55022 is higher by 10 dB.

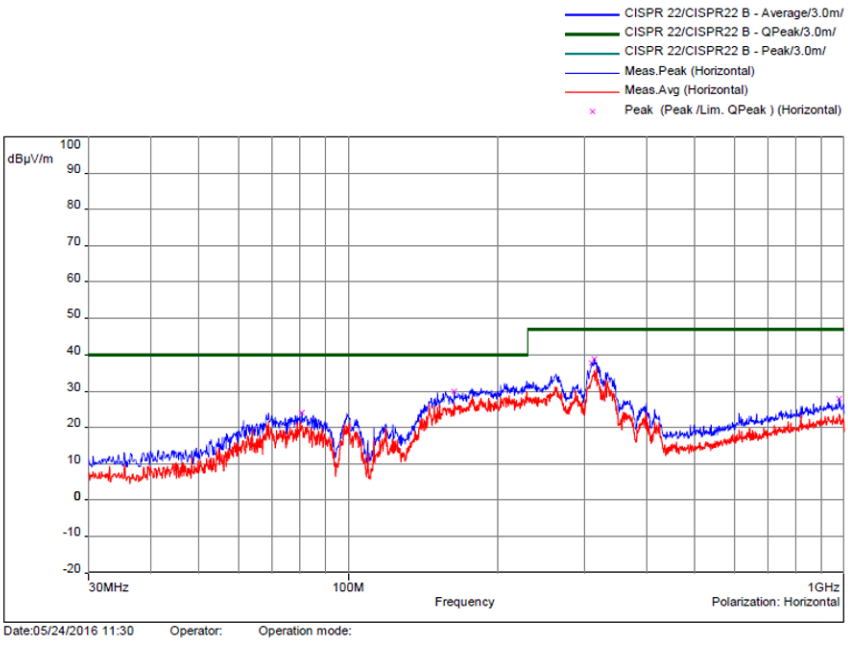


図 26. Radiated Emission 3-m Prescan Test Horizontal Polarization

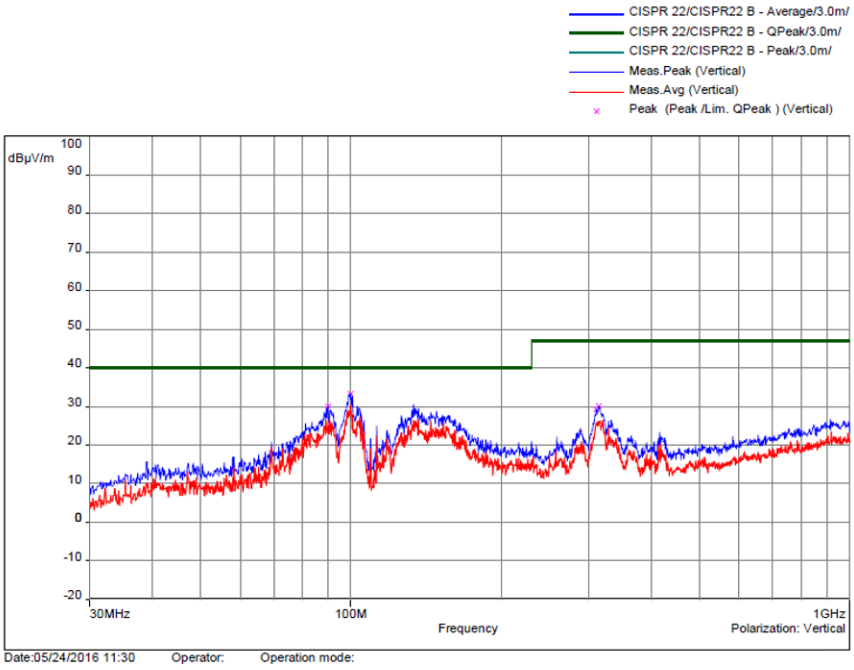


図 27. Radiated Emission 3-m Prescan Test Vertical Polarization

表 11. Radiated Emission 3-m Prescan List of Critical Points

FREQ (MHz)	SR	PK (dBµV/m)	LIMIT QP (dBµV/m)	MARGIN (dB)	ANGLE (°)	POLARIZATION	CORR
48.236	1	20.65	40.00	–19.35	129.50	Horizontal polarization	–5.39
73.262	1	20.94	40.00	–19.06	109.40	Horizontal polarization	–8.85
141.550	1	21.58	40.00	–18.42	299.40	Horizontal polarization	–6.24
307.905	1	27.82	47.00	–19.18	139.30	Horizontal polarization	–4.72
557.195	1	30.21	47.00	–16.79	239.40	Horizontal polarization	1.00
861.290	1	43.83	47.00	–3.17	319.40	Horizontal polarization	5.74
554.091	2	27.85	47.00	–19.15	190.70	Vertical polarization	0.41
855.858	2	41.77	47.00	–5.23	210.70	Vertical polarization	5.28

Those critical points are then tested in the typical 10-m setup.

図 28. Radiated Emission 10-m Test Setup

During the scan, the board passes the radiated emission test with more than 4 dB of margin.

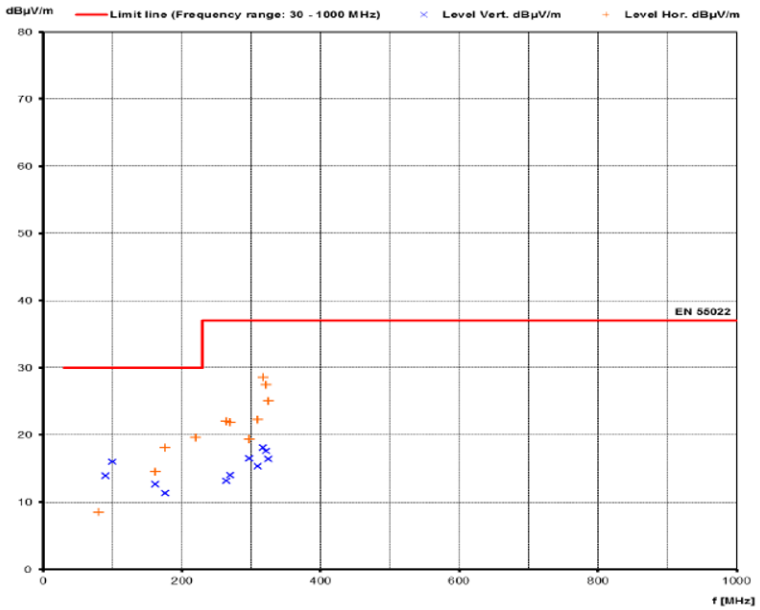


図 29. Radiated Emission 10-m Test Result

表 12. Radiated Emission 10-m Test Result

FREQ (MHZ)	READING VERT (dBµV)	READING HOR (dBµV)	CORRECT VERT (dB/m)	CORRECT HOR (dB/m)	LEVEL VERT (dBµV/m)	LEVEL HOR (dBµV/m)	LIMIT (dBµV/m)	D_{LIMIT} (dB)
30.00	5.5	4.8	13.2	13.2	18.7	18.0	30.0	–11.3
37.30	6.7	5.3	14.2	14.2	20.9	19.5	30.0	–9.1
48.23	7.2	7.1	14.5	14.5	21.7	21.6	30.0	–8.3
57.93	5.1	4.8	14.3	14.3	19.4	19.1	30.0	–10.6
73.26	6.2	7.9	10.3	10.3	16.5	18.2	30.0	–11.8
83.86	5.9	6.6	10.6	10.6	16.5	17.2	30.0	–12.8
137.31	13.7	8.7	10.2	10.2	23.9	18.9	30.0	–6.1
141.55	5.4	5.4	10.1	10.1	15.5	15.5	30.0	–14.5
176.85	5.1	5.0	11.6	11.6	16.7	16.6	30.0	–13.3
250.35	5.5	6.5	15.2	15.2	20.7	21.7	37.0	–15.3
276.05	7.1	8.1	16.0	16.0	23.1	24.1	37.0	–12.9
307.90	6.5	6.6	17.0	17.0	23.5	23.6	37.0	–13.4
514.50	9.1	7.0	22.0	22.0	31.1	29.0	37.0	–5.9
557.19	7.5	6.8	22.8	22.8	30.3	29.6	37.0	–6.7
577.39	8.0	7.0	23.2	23.2	31.2	30.2	37.0	–5.8
613.69	7.0	9.0	23.8	23.8	30.8	32.8	37.0	–4.2

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01449.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01449.

4.3 PCB Layout Recommendations

In switch mode DC/DC, take special care to avoid coupling between the different loops. In a Buck topology, the input loop is particularly critical; for this reason, place the input capacitors as close as possible to the TPS561201.

This is done by separating the noise sensitive loop (Feedback and Enable) from the high di/dt loops (input, switch node, bootstrap). Separate these loops by placing the components and traces of the feedback and enable loop as far as possible from components and traces with high di/dt.

Also give special attention to the ground plane; try to make it as large and as solid as possible to both reduce noise sensitivity and help thermal dissipation.

With regards to thermal dissipation, the input and output voltage planes must also be made as large and solid as possible to help keep the board as cool as possible.

Lastly, the soldering pad for the inductor was slightly enlarged to allow the tests of several inductors.

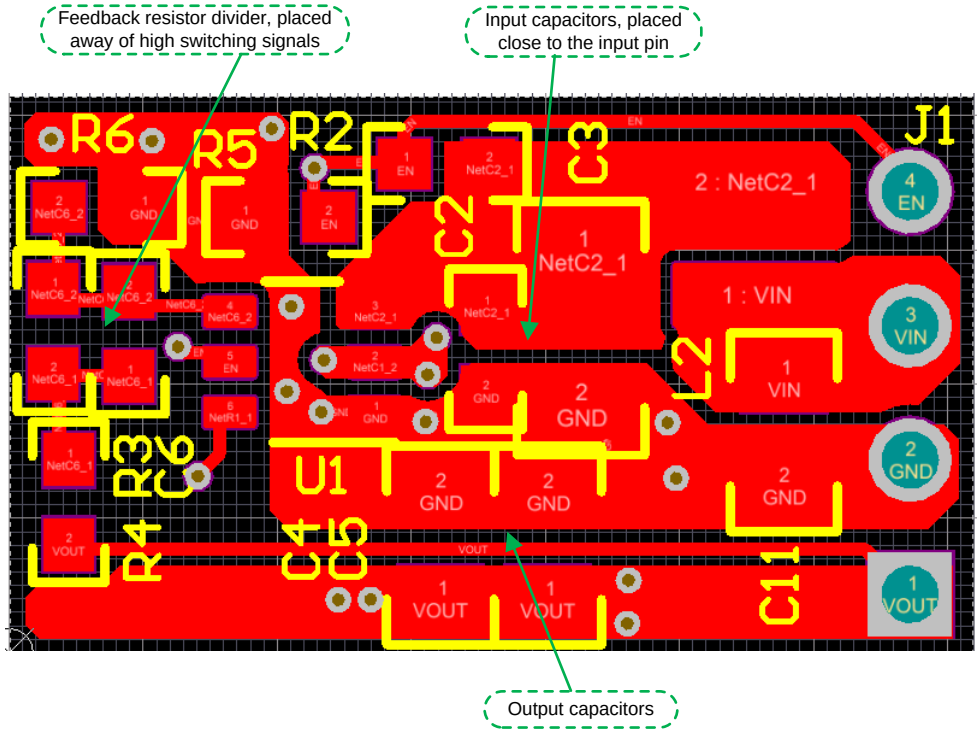


図 30. Top Layer

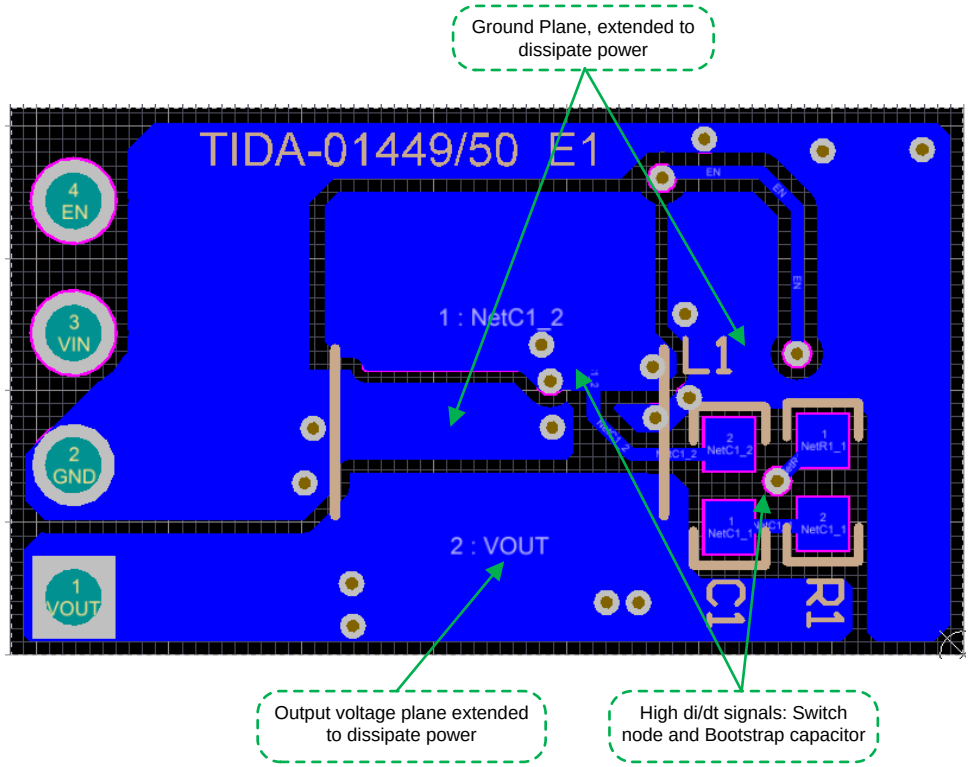


図 31. Bottom Layer (Flipped)

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01449.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01449.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01449.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01449.

5 Related Documentation

1. Texas Instruments, *Understanding Buck Power Stages In Switchmode Power Supplies*, Application Report (SLVA057)
2. Texas Instruments, *Layout Tips for EMI Reduction in DC / DC Converters*, AN-2155 Application Report (SNVA638)
3. Texas Instruments, *Simple Success With Conducted EMI From DCDC Converters*, AN-2162 Application Report (SNVA489)

5.1 商標

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6 About the Author

KEVIN STAUDER is a system engineer in the Industrial Systems team at Texas Instruments, responsible for developing TI Designs for industrial applications.

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お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、あるいはTIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

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お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

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