

## TI Designs: TIDA-01450

# 5V、1Aでコスト効率の優れた、デュアル・レイヤで効率92.5%のTO-220 LDO代替品のリファレンス・デザイン



### 概要

このリファレンス・デザインでは、主要な家電製品でLDOの代替品となる、小型、高効率で低EMIのDC/DCモジュールのソリューションを紹介します。LDOをDC/DCモジュールに交換することで、システム効率が劇的に向上し、ソリューションのサイズが小さくなり、BOMコストが低減すると同時に、ヒート・シンクも不要になります。このモジュールはTO-220パッケージとほぼ同じ容積で、TO-220 LDOとピン互換なため、迅速な評価が可能で、市場投入までの期間を短縮できます。TPS561201電力コンバータは、全負荷、低負荷、およびスタンバイ動作において、より大きな出力電流と、低い消費電力を実現します。

このモジュールはTO-220 LDOとサイズおよびピン互換なため、迅速に評価を行え、市場投入までの期間を短縮できます。

### リソース

TIDA-01450  
TPS561201

デザイン・フォルダ  
プロダクト・フォルダ



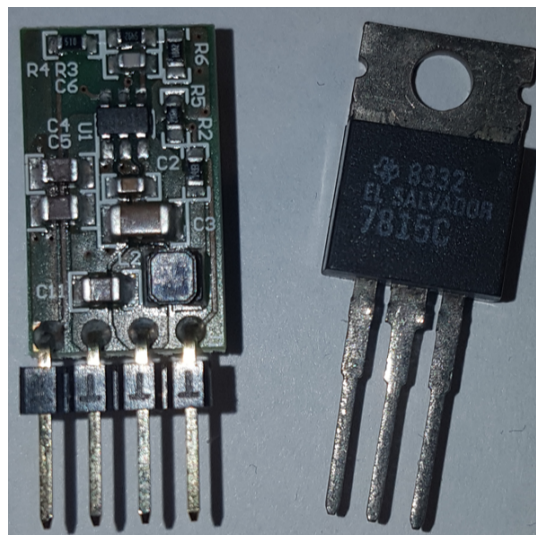
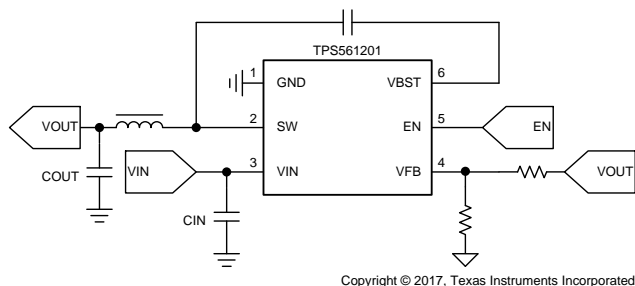
E2Eエキスパートに質問

### 特長

- 5Vにレギュレートされた、最大1Aの出力負荷
- 92.5%の効率
- スタンバイ電流2.6μA、無負荷時電流456μA
- 小型のフォーム・ファクタ: TO-220とサイズおよびピン互換で、より小型(10.5mm×18.3mm)
- 全負荷時に30°C未満の温度上昇、ヒート・シンク不要
- オンボードDC/DC設計の複雑性を低減、スイッチング電源のEMC設計の研究開発の期間と労力を削減(市場投入までの期間短縮)

### アプリケーション

- 洗濯機、乾燥機
- 冷蔵庫、冷凍庫
- 食器洗い機
- エアコンの室内機

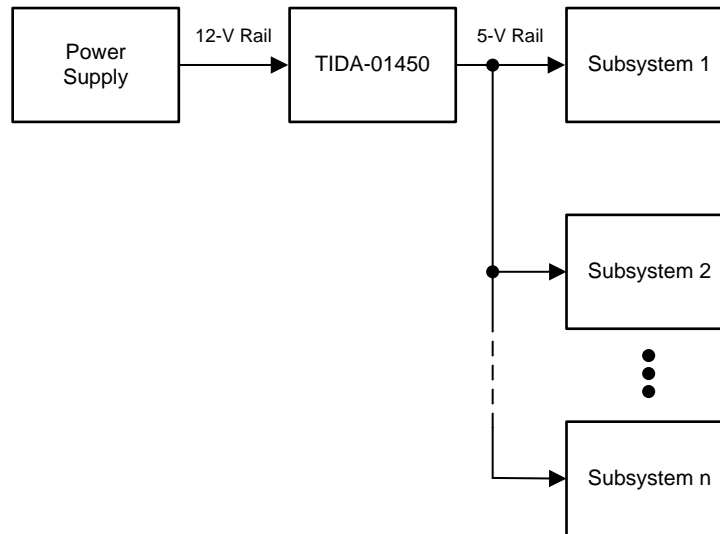




使用許可、知的財産、その他免責事項は、最終ページにあるIMPORTANT NOTICE(重要な注意事項)をご参照くださいますようお願いいたします。英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

## 1 System Description

Traditionally, low dropout regulators (LDOs) are used in home appliances to generate 5 V or 3.3 V from the 12-V rail. These LDOs are chosen mainly for their cost and size.



Copyright © 2017, Texas Instruments Incorporated

図 1. System Diagram

With the tightening requirements on active and standby power consumption and the increasing current needs due to adding new features (for example, the Wi-Fi® module), the LDOs become an obstacle to achieving stringent energy ratings.

The TIDA-01450 design is developed to answer this need of higher efficiency and current capability with the additional benefit of saving space by eliminating the heat sink, which is normally used to allow the LDOs to dissipate the losses.

### 1.1 Key System Specifications

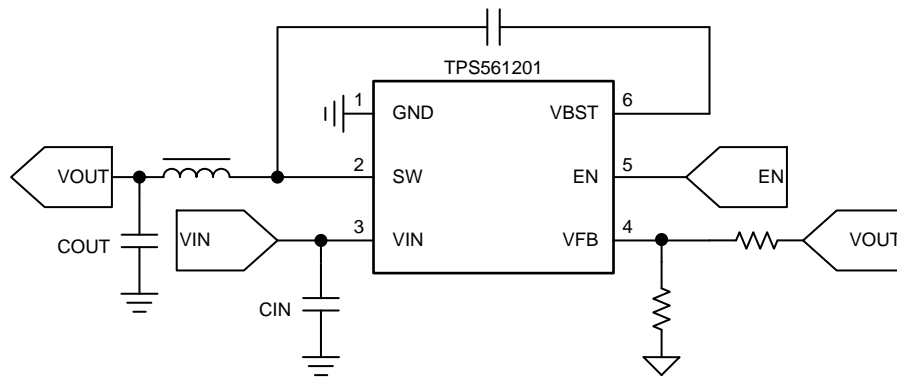
The specifications of the TIDA-01450 design are listed in 表 1:

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage range	6.5 to 17 V	—
Output voltage and max current	5 V at 1 A	—
Efficiency (full load, rated load, and light load)	92.5%: 12 V → 5 V at 1 A, 91%: 12 V → 5 V at 500 mA, 81%: 12 V → 5 V at 10 mA	3.2.2.1
EMI performance	EN55022 class B, >6-dB margin	3.2.2.10
Regulation (line and load)	±3% across the input range and load current range	3.2.2.3
Transient response	±5% from 0.1 to 1.0 A	3.2.2.5
Protections	Short-circuit, hiccup mode OCP for both FETs, OTP, OVP	3.2.2.7
Operating ambient temperature	−30°C to 85°C	3.2.2.2

## 2 System Overview

### 2.1 Block Diagram



Copyright © 2017, Texas Instruments Incorporated

図 2. Block Diagram

### 2.2 Highlighted Products

#### 2.2.1 TPS561201

The TPS561201 is a simple, easy-to-use, 1-A synchronous step-down converters in a SOT-23 package. The devices are optimized to operate with minimum external component counts and to achieve low standby current.

These switch mode power supply (SMPS) devices employ D-CAP2™ mode control providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

The TPS561201 operates in pulse skip mode, which maintains high efficiency during light load operation. The TPS561201 is available in a 6-pin, 1.6x2.9-mm SOT (DDC) package and specified from -40°C to 125°C of junction temperature.

Features:

- 1-A converter integrated 140-mΩ and 84-mΩ FETs
- D-CAP2 mode control with fast transient response
- Input voltage range: 4.5 to 17 V
- Output voltage range: 0.76 to 7 V
- Pulse-skip mode
- 580-kHz switching frequency
- Low shutdown current less than 10 μA
- 2% feedback voltage accuracy (25°C)
- Startup from pre-biased output voltage
- Cycle-by-cycle overcurrent limit
- Hiccup-mode overcurrent protection
- Non-latch UVP and TSD protections

- Fixed soft-start: 1.0 ms

### 2.3 System Design Theory

LDOs are devices that regulate the output voltage, while the output current is the same as the input current. This implies losses are proportional to the dropout between input and output voltage and the output current, as shown in 式 1. These losses are the root cause of poor efficiency in LDOs. This translates to a limitation of the ratio between input and output voltage and maximum output current as well as the need of a heat sink. That heat sink adds cost and size to the overall solution.

A DC/DC switch mode power supply, including a Buck topology as in this project, present the advantage of having a higher efficiency, allowing them to be used in a wider variety of applications as well as being competitive with an LDO-based design with respect to cost and size (including all components and heat sink). Find more details on how a Buck topology works in the application report [Understanding Buck Power Stages In Switchmode Power Supplies](#) (SLVA057).

Compare the efficiency of the TIDA-01450 and an LDO-based design. The efficiency data for the TIDA-01450 design can be found in 3.2.2.1. In an LDO, the power to be dissipated can be estimated by 式 1.

$$P_{DISSIPATED} = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{1}$$

Now calculate the power dissipated by a 12-V input, 5-V output design at 1 A, 500 mA, and 100 mA to see what the performances are for the TIDA-01450 and for the LDO-based design.

For 1 A, the efficiency of the TIDA-01450 is 92.5% (7.5% loss). With 5 W at the output, 0.375 W are dissipated. For the LDO-based design, 式 1 gives 7 W to be dissipated by the LDO.

For 500 mA, the efficiency of the TIDA-01450 is 91% (9% loss). With 2.5 W at the output, 0.225 W are dissipated. This is to be compared with 3.5 W for the LDO.

Finally for 100 mA, 0.05 W needs to be dissipated for the TIDA-01450 (90% efficiency) versus 0.7 W for the LDO-based design.

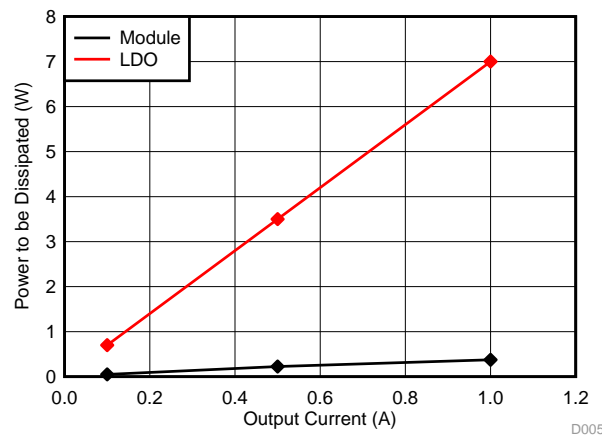


図 3. Comparison of Power Dissipated

As shown in 図 3, the LDO-based design needs to dissipate much more power than the TIDA-01450 design, which impacts both power consumption and cost and size due to the necessity of a heat sink.

## 2.4 Design Considerations

### 2.4.1 Part and Topology Selection

The first step of the design is to select the circuit topology. As cost and space are key in home appliance design and no isolation is needed for the 12-V to 5-V conversion, a Buck topology is chosen. Still, with the aim to reduce bill of material cost and size, a synchronous converter with integrated FET is preferred.

With this in mind, as well as the specification in 表 1, the TPS561201 is chosen. The converter includes two integrated switching FETs, internal loop compensation, and a 1-ms internal soft start to reduce component count. It integrates a 140-mΩ and a 84-mΩ MOSFET for up to 1-A continuous output current.

### 2.4.2 Design Steps and Passive Components Selection

The first step is to set the output voltage, which is adjusted by the resistor divider (R3 and R6). Set the range of the resistors; higher values decrease the losses in the resistor divider but make the feedback signal more sensitive to noise, while lower values will make the feedback signal more robust against noise but increase losses. On this project, a good trade-off is setting R6 at 10 kΩ and use 式 2 to calculate R3. A 51-Ω resistor (R4) is added to measure the loop stability. R4 is not needed in the final design and can be shorted.

$$R_3 = \left( \frac{V_{OUT}}{0.768} - 1 \right) \times R_6 \quad (2)$$

where:

- R6 = 10 kΩ
- V<sub>OUT</sub> = 5 V
- V<sub>REF</sub> = 0.768 V

式 2 gives R3 = 55.104 kΩ. A resistor value of 54.9 kΩ is then used for R3.

Then comes the choice of the output filter, including the output inductor (L1) and output capacitors (C3 and C4). The LC filter used as the output filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a -40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high-frequency zero that reduces the gain roll off to -20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of 式 3 is located below the high frequency zero but close enough that the phase boost provided by the high-frequency zero provides adequate phase margin for a stable circuit.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 式 4, 式 5, and 式 6. The inductor saturation current rating must be greater than the calculated peak current, and the RMS or heating current rating must be greater than the calculated RMS current. Use 580 kHz for f<sub>SW</sub>. Make sure the chosen inductor is rated for the peak current of 式 5 and the RMS current of 式 6.

$$I_{p-p} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$I_{\text{peak}} = I_O + \frac{I_{\text{p-p}}}{2} \quad (5)$$

$$I_{\text{LO(RMS)}} = \sqrt{I_O^2 + \frac{1}{12} I_{\text{p-p}}^2} \quad (6)$$

For this TI Design, the inductor used is a Coilank ABG06A45M4R7 (4.7  $\mu\text{H}$ ) with a saturation current rating of 5.12 A and an RMS current rating of 3.4 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS561201 is intended for use with ceramic or other low-ESR capacitors. Recommended values range from 20 to 68  $\mu\text{F}$ . Use to determine the required RMS current rating for the output capacitor.

$$I_{\text{CO(RMS)}} = \frac{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}{\sqrt{12} \times V_{\text{IN}} \times L_o \times f_{\text{SW}}} \quad (7)$$

For this design, two MURATA 22- $\mu\text{F}$  output capacitors are used.

The next step is to set the input capacitor. The TPS561201 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10  $\mu\text{F}$  for the decoupling capacitor. An additional 0.1- $\mu\text{F}$  capacitor (C3) from pin 3 to ground is optional to provide additional high-frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

As required, a bootstrap capacitor (C1) of 0.1  $\mu\text{F}$  (X7R or X5R) has to be added between the BOOT pin and the SW pin.

The last step is to select the input filter. Considering the rated input RMS current, this TI Design uses the ABG03A15M4R7 (4.7  $\mu\text{H}$ ) with a saturation current rating of 1.13 A and an RMS current rating of 1.12 A as the input inductor and a 47- $\mu\text{F}$  capacitor as the input capacitor.

Finally a 0- $\Omega$  resistor (R1) is added next to the bootstrap for test purposes (EMC tests). The results of these tests show that this resistor is not needed.

### 3 Hardware, Testing Requirements, and Test Results

#### 3.1 Required Hardware

##### 3.1.1 PCB Overview

A picture of the PCB with the functional blocks is shown in 図 4.

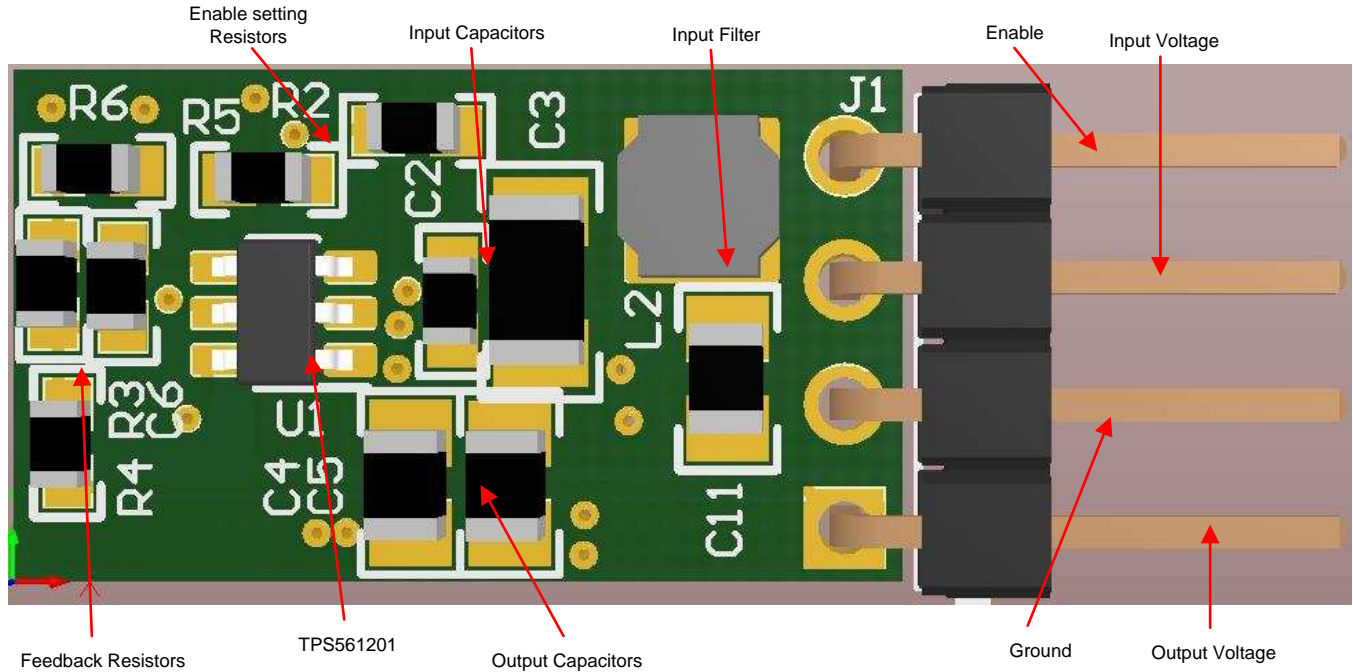


図 4. TIDA-01450 PCB With Functional Blocks

The inductor and bootstrap capacitor are placed on the bottom side of the board.

##### 3.1.2 Connectors Settings

表 2. Connector Settings

CONNECTOR	FUNCTION
J1-1	$V_{OUT}$
J1-2	GND
J1-3	$V_{IN}$
J1-4	EN

## 3.2 Testing and Results

### 3.2.1 Test Setup

Figure 5 shows the setup and the test equipment used.

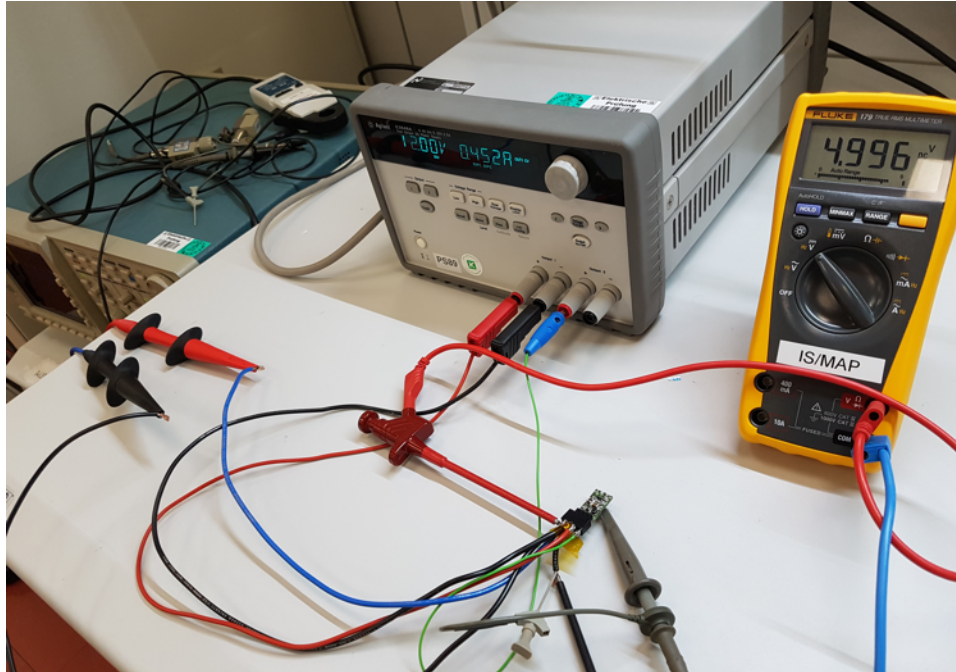


Figure 5. Picture of Test Setup for TIDA-01450

Table 3 lists the test equipment used to test the TIDA-01450.

Table 3. Test Equipment

TEST EQUIPMENT	PART NUMBER
Oscilloscope	Tektronix TDS 640A
Voltage probe	Tektronix P6139A
Current probe	LEM PR 30
Multimeter	Fluke 179 and 87 III
Power supply	Agilent E3648A
Electronic load	Chroma 63103 and 63104
Passive load	SNE350x40S2 D040
Temperature chamber	Voetsch VT4002
Thermal camera	Fluke TI40



### 3.2.2 Test Results

#### 3.2.2.1 Efficiency

To test the efficiency, four multimeters are used: two are set up as voltmeters to measure the input and output voltages, and two are set up as ammeters to measure the input and output currents.

The measurements are done at a room temperature of 23°C and with the enable setting resistors (R2 and R5) not populated, with 6 V applied to the Enable pin.

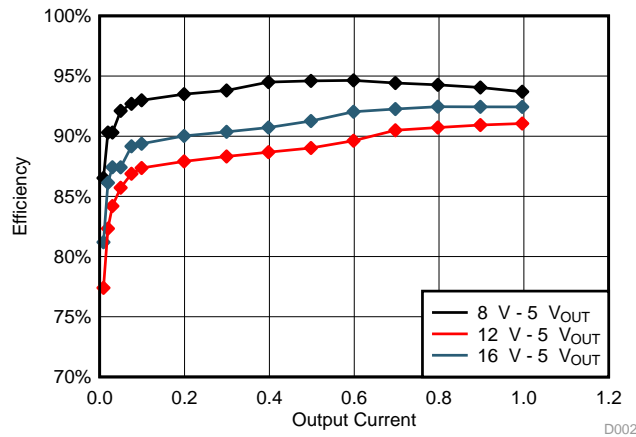


図 6. TIDA-01450 Efficiency

表 4, 表 5, and 表 6 list the details of the efficiency curves shown in 図 6.

表 4. Efficiency With 8-V Input

V <sub>IN</sub> (V)	I <sub>IN</sub> (A)	V <sub>OUT</sub> (V)	I <sub>OUT</sub> (A)	η
7.770	0.6970	5.0720	0.9970	0.933728
7.800	0.6230	5.0730	0.8990	0.938516
7.820	0.5500	5.0740	0.7995	0.943191
7.850	0.4770	5.0750	0.6990	0.947382
7.870	0.4070	5.0760	0.6000	0.950832
7.890	0.3370	5.0770	0.5000	0.954707
7.910	0.2680	5.0775	0.4000	0.958073
7.930	0.2010	5.0780	0.3010	0.958937
7.950	0.1345	5.0790	0.2010	0.954739
7.980	0.0680	5.0810	0.1010	0.945712
7.980	0.0520	5.0810	0.0770	0.942831
7.990	0.0360	5.0820	0.0520	0.918732
7.990	0.0230	5.0830	0.0320	0.885106
7.990	0.0158	5.0840	0.0218	0.877927
7.995	0.0080	5.0850	0.0110	0.874531

**表 5. Efficiency With 12-V Input**

$V_{IN}$ (V)	$I_{IN}$ (A)	$V_{OUT}$ (V)	$I_{OUT}$ (A)	$\eta$
11.81	0.4620	5.0680	0.9980	0.926990
11.83	0.4140	5.0690	0.8990	0.930458
11.85	0.3670	5.0700	0.7990	0.931473
11.87	0.3190	5.0710	0.6985	0.935446
11.89	0.2730	5.0730	0.6000	0.937717
11.90	0.2270	5.0740	0.5000	0.939177
11.92	0.1815	5.0750	0.4000	0.938303
11.94	0.1370	5.0770	0.3010	0.934219
11.96	0.0925	5.0780	0.2010	0.922605
11.98	0.0480	5.0810	0.1010	0.892427
11.98	0.0370	5.0820	0.0768	0.880516
11.99	0.0250	5.0820	0.0512	0.868051
11.99	0.0160	5.0830	0.0320	0.847873
11.99	0.0110	5.0830	0.0210	0.809334
11.99	0.0060	5.0875	0.0110	0.777905

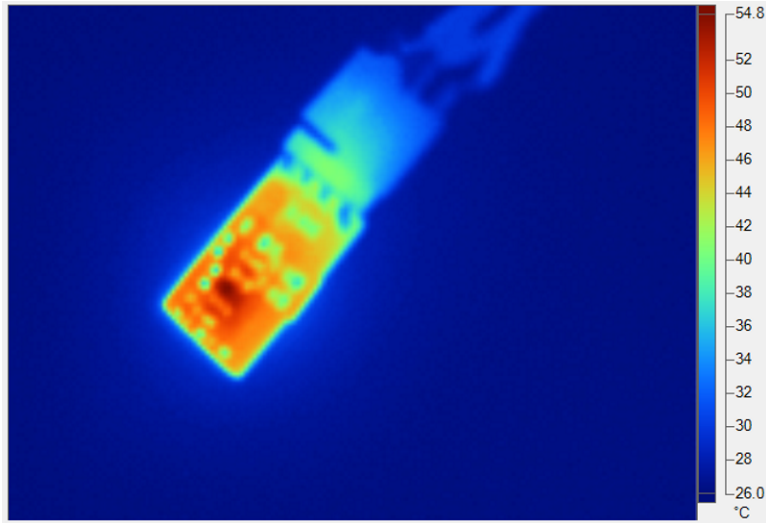
**表 6. Efficiency With 16-V Input**

$V_{IN}$ (V)	$I_{IN}$ (A)	$V_{OUT}$ (V)	$I_{OUT}$ (A)	$\eta$
19.88	0.2810	5.059	0.9970	0.902895
19.90	0.2530	5.060	0.8990	0.903518
19.91	0.2245	5.062	0.7990	0.904860
19.92	0.1960	5.064	0.6990	0.906620
19.93	0.1680	5.066	0.6000	0.907820
19.94	0.1400	5.068	0.5000	0.907723
19.95	0.1130	5.070	0.4000	0.899594
19.96	0.0860	5.072	0.3010	0.889379
19.97	0.0585	5.074	0.2010	0.872997
19.98	0.0300	5.079	0.1010	0.855821
19.98	0.0230	5.080	0.0768	0.848988
19.99	0.0160	5.083	0.0513	0.815276
19.99	0.0100	5.082	0.0320	0.813527
19.99	0.0070	5.084	0.0210	0.762981
19.99	0.0040	5.090	0.0110	0.700225

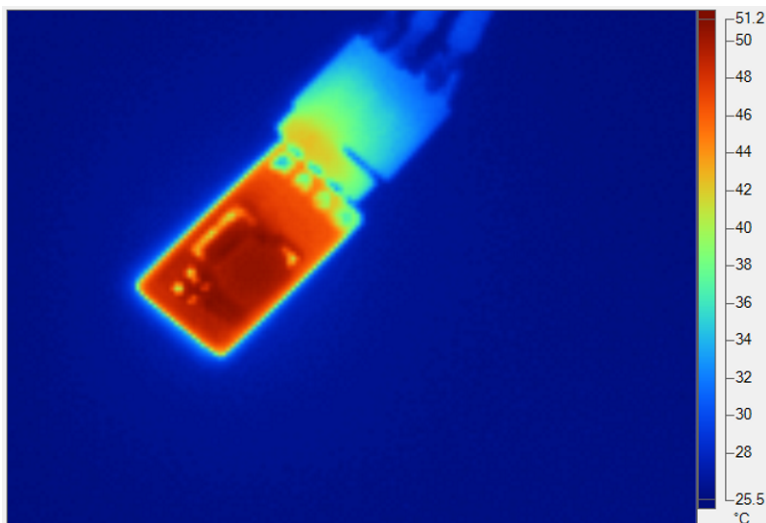
### 3.2.2.2 Thermal

The thermal pictures in [Figure 7](#) and [Figure 8](#) were taken at a room temperature of 26°C, with a 12-V input, 5 V at 1-A output without airflow.

The hottest point of the design is the TPS561201 at 54.8°C. This is an increase of 28.8°C. Because the acceptable ambient temperature range is -30°C to 85°C, no heat sink is required for the TIDA-01450 to function properly.



**Figure 7. Top-Side Thermal Picture With 12-V<sub>IN</sub>, 5 V at 1-A Output**



**Figure 8. Bottom-Side Thermal Picture With 12-V<sub>IN</sub>, 5 V at 1-A Output**

### 3.2.2.3 Line and Load Regulation Over Temperature

Figure 9, Figure 10, and Figure 11 show the output voltage variation, depending on load current and input voltage across  $-30^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

Across all input voltages, output currents, and temperature conditions, the output voltage varies between 5.14 and 4.98 V. This is 3% of the output voltage, which is below the initial target of  $\pm 3\%$ .

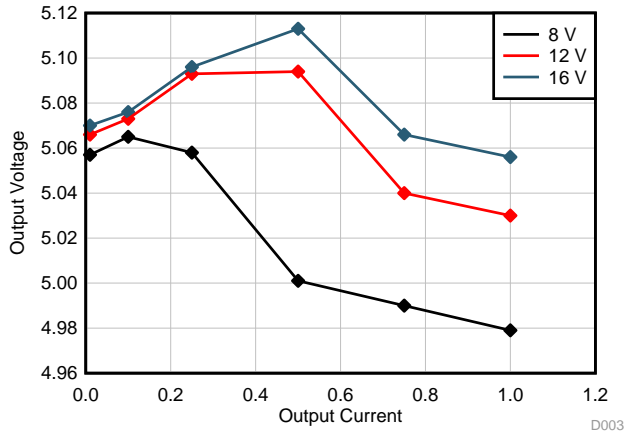


Figure 9. Line and Load Regulation at 65°C

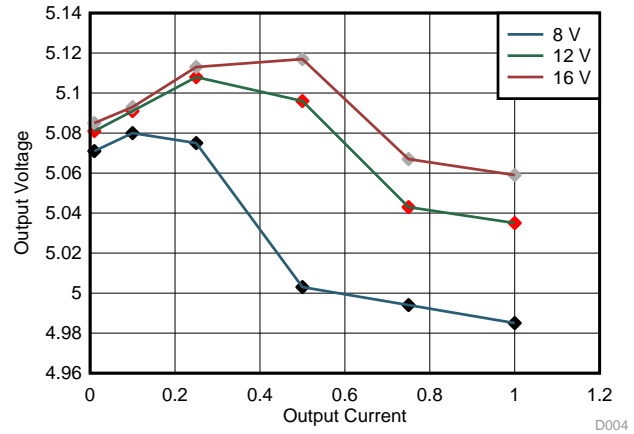


Figure 10. Line and Load Regulation at 22.5°C

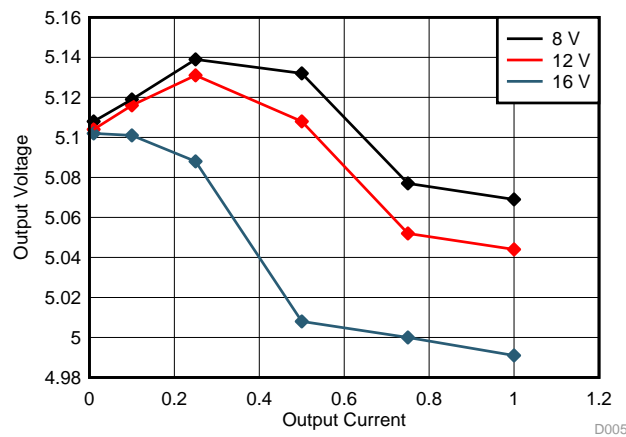


Figure 11. Line and Load Regulation at  $-30^{\circ}\text{C}$

表 7, 表 8, and 表 9 list the details of the line and load regulation over temperature curves shown in 図 9, 図 10, and 図 11.

**表 7. Line and Load Regulation at 65°C**

$V_{IN}$	$V_{OUT}$	$I_{OUT}$
20	5.0570	1.00
20	5.0605	0.75
20	5.0660	0.50
20	5.0710	0.25
20	5.0770	0.10
20	5.0890	0.01
12	5.0640	1.00
12	5.0670	0.75
12	5.0710	0.50
12	5.0750	0.25
12	5.0780	0.10
12	5.0840	0.01
8	5.0690	1.00
8	5.0710	0.75
8	5.0735	0.50
8	5.0760	0.25
8	5.0780	0.10
8	5.0830	0.01

**表 8. Line and Load Regulation at 22.5°C**

$V_{IN}$	$V_{OUT}$	$I_{OUT}$
20	5.060	1.00
20	5.064	0.75
20	5.068	0.50
20	5.073	0.25
20	5.079	0.10
20	5.090	0.01
12	5.068	1.00
12	5.071	0.75
12	5.074	0.50
12	5.078	0.25
12	5.081	0.10
12	5.088	0.01
8	5.073	1.00
8	5.075	0.75
8	5.077	0.50
8	5.079	0.25
8	5.081	0.10
8	5.085	0.01

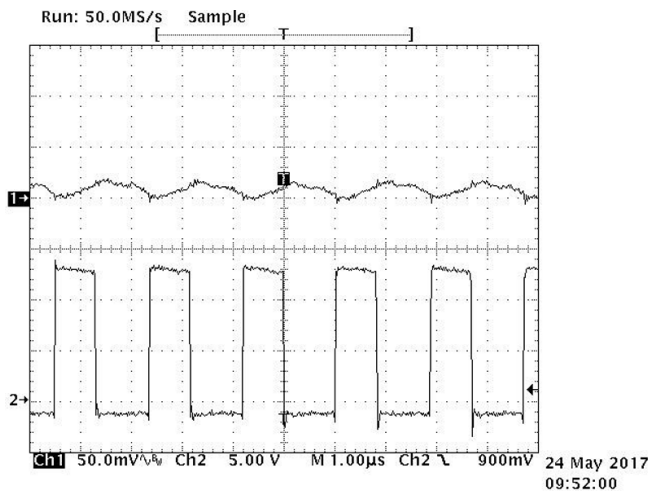
**表 9. Line and Load Regulation at -30°C**

$V_{IN}$	$V_{OUT}$	$I_{OUT}$
20	5.0600	1.00
20	5.0635	0.75
20	5.0670	0.50
20	5.0700	0.25
20	5.0750	0.10
20	5.0900	0.01
12	5.0700	1.00
12	5.0720	0.75
12	5.0750	0.50
12	5.0780	0.25
12	5.0800	0.10
12	5.0870	0.01
8	5.0750	1.00
8	5.0750	0.75
8	5.0780	0.50
8	5.0800	0.25
8	5.0810	0.10
8	5.0850	0.01

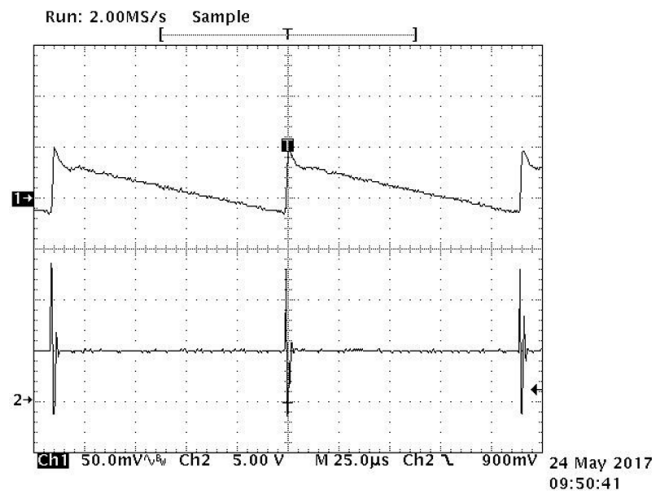
### 3.2.2.4 Output Voltage Ripple

The output voltage ripple remains below 70 mVpp under full load (1 A), low load (10 mA), or no load. This ripple is well below the initial requirements of  $\pm 1\%$ .

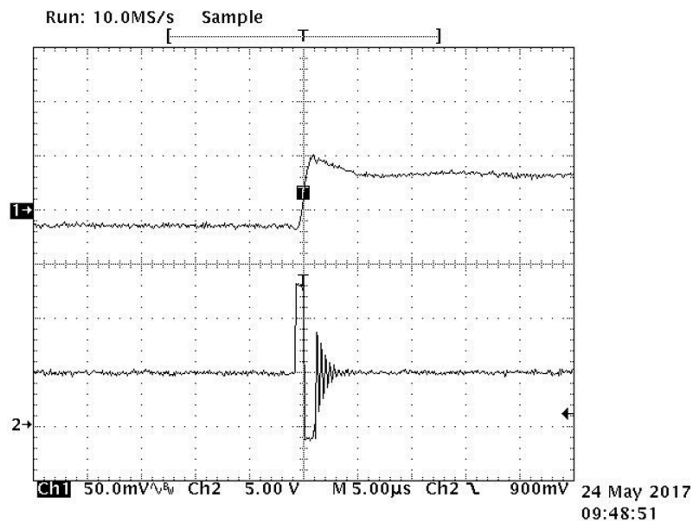
Measurements are done at 23°C room temperature with a 12-V input voltage. The upper curve (1) is the output voltage with an oscilloscope in AC-coupling mode with 50 mV/div. The lower curve (2) is the switch node (pin 2 of the TPS561201) with 5 V/div.



⊠ 12. Output Voltage Ripple at 1-A Output Load



⊠ 13. Output Voltage Ripple at 10-mA Output Load



⊠ 14. Output Voltage Ripple at No Load Output

### 3.2.2.5 Transient Response

The transient response is below  $\pm 250$  mV for load steps between 10 mA and 1 A, which are the design requirements ( $\pm 5\%$ ).

Measurements are done at 23°C room temperature with a 12-V input voltage. The upper curve (1) is the output voltage with an oscilloscope in AC-coupling mode with 100 mV/div. The lower curve (2) is the output current with the current probe of 100 mV/A with 200 mV/div. The load step is applied with a 250-mA/ $\mu$ s slew rate.

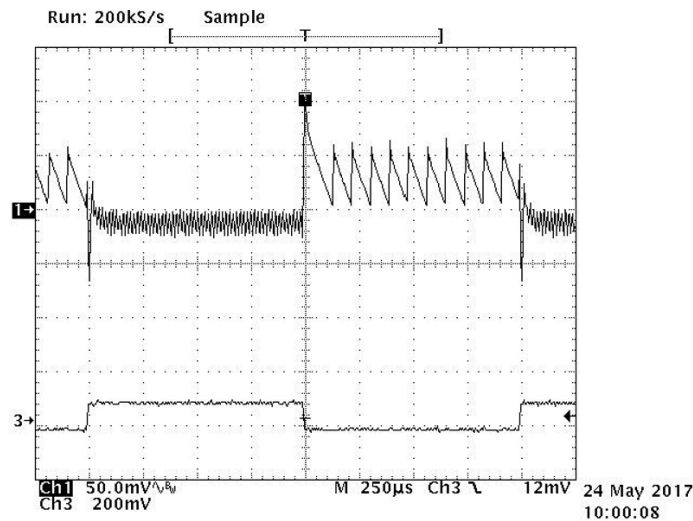


図 15. Transient Response From 10-mA to 1-A Output Load

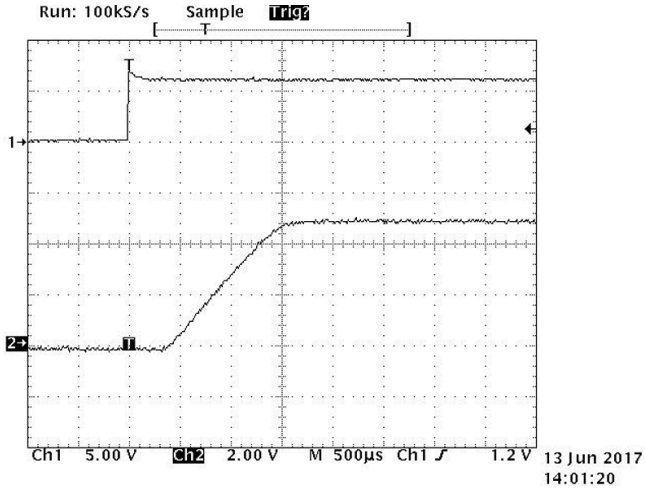
### 3.2.2.6 Start-up and Shutdown

For the start-up and the shutdown behavior, 12 V is applied at the input with a 1-A load at the output. The EN setting resistors (R2 and R5) are not populated, and the Enable pin is controlled with a 6-V signal.

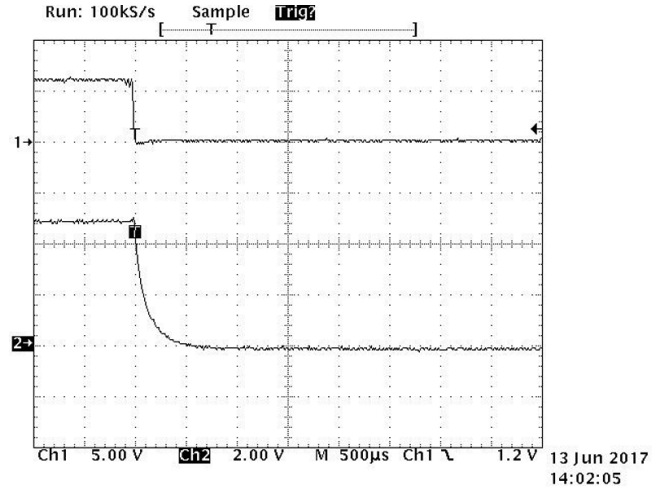
Measurements are done at 23°C room temperature. The upper curve (1) is the Enable signal with 5 V/div. The lower curve (2) is the output voltage with an oscilloscope in DC-coupling mode with 2 V/div.

The TIDA-01450 design takes 1.5 ms to provide 5 V at the output after the EN pin is enable. The output voltage is reached without overshoot.





☒ 16. Start-up at 12-V Input and 1-A Output Load



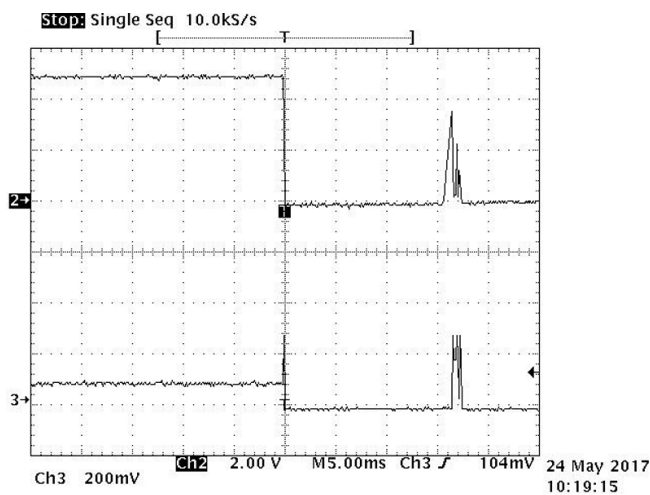
☒ 17. Shutdown at 12-V Input and 1-A Output Load

### 3.2.2.7 Overcurrent and Short-Circuit Test

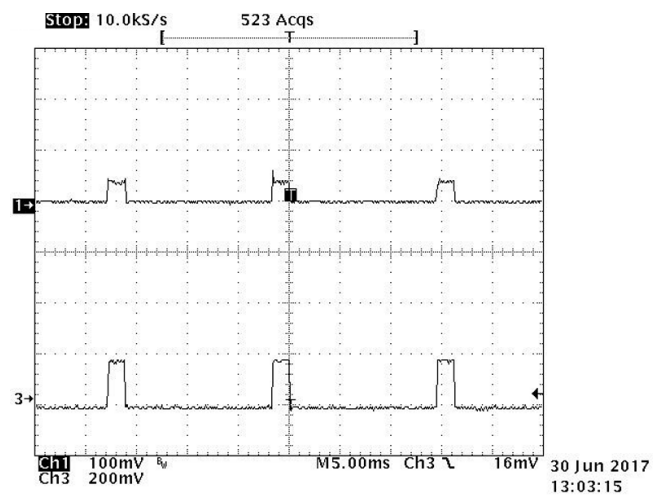
The overcurrent protection is tested by having a transient load from a 1- to 3-A output current while the board is supplied with 12 V. The short-circuit protection is tested by shorting the output pin to ground.

The upper curve (1) is the output voltage with an oscilloscope in DC-coupling mode with 2 V/div (☒ 18) and 100 mV/div (☒ 19). The lower curve (2) is the output current with the current probe of 100 mV/A with 200 mV/div.

As shown in ☒ 18 and ☒ 19, when the current is rising to the current limit level, the device enters overcurrent protection as described in the [TPS561201 datasheet](#) (SLVSC95). After waiting the pre-programmed time, the device tries to restart. Once the fault condition is removed, the device starts normally.



☒ 18. Overcurrent Protection

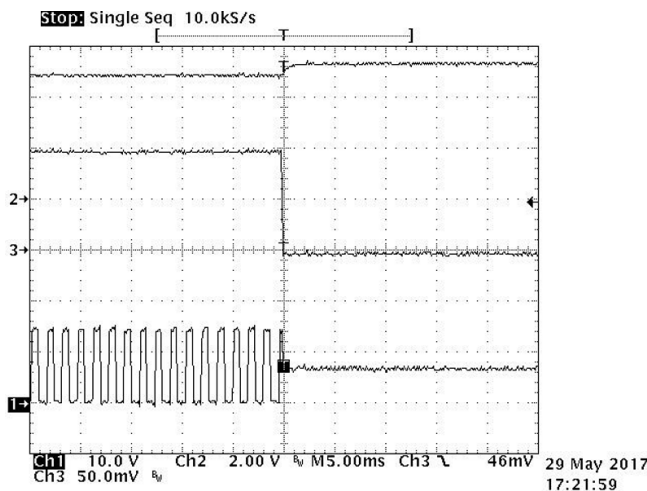


☒ 19. Short-Circuit Protection

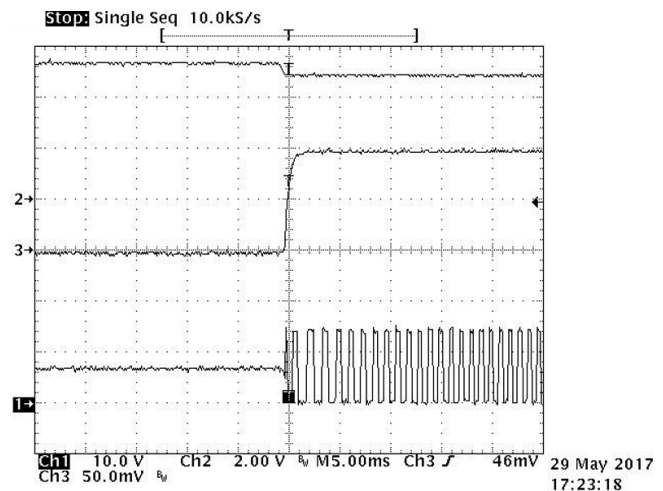
### 3.2.2.8 Overvoltage Test

The overvoltage protection is tested by applying 5.5 V at the output of the TIDA-01450 board while the board is supplied with 12 V and with a 1-A output load.

The upper curve (2) is the output voltage with an oscilloscope in DC-coupling mode with 2 V/div. The middle curve (3) is the current coming out of the TIDA-01450 with the current probe at 100 mV/A with 50 mV/div. The lower curve (1) is voltage at the switch node with 1 V/div.



☒ 20. Overvoltage Protection From 5 to 5.5 V



☒ 21. Overvoltage Protection From 5.5 to 5 V

### 3.2.2.9 Standby and No-Load Currents

The standby current is measured with an ammeter at 23°C room temperature with a 12-V input voltage. The Enable pin was set low through the connector, and the Enable setting resistors (R2 and R5) not populated. The standby current is measured at 2.6  $\mu$ A.

The no-load current is measured with an ammeter at 23°C room temperature with a 12-V input voltage, with the enable setting resistors (R2 and R5) not populated, with a 6-V apply to the Enable pin and no load attached at the output. The no-load current was measured at 456  $\mu$ A.

### 3.2.2.10 EMC Tests

The TIDA-01450 TI Design has been tested for EMI according to EN55022 Class B conducted and radiated emissions. The EMC tests are performed by CSA Group Bayern GmbH (Germany).

#### 3.2.2.10.1 Conduction Emission

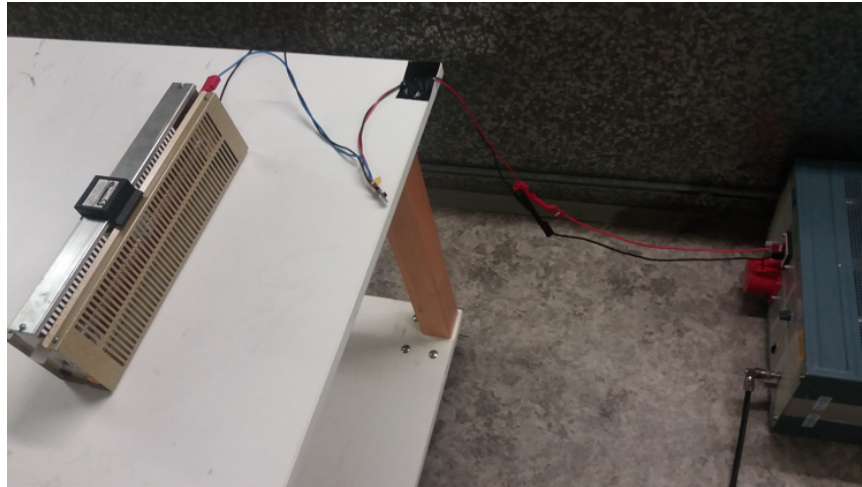


図 22. Conducted Emission Test Setup

The board passed the conducted emission test with more than 7 dB of margin.

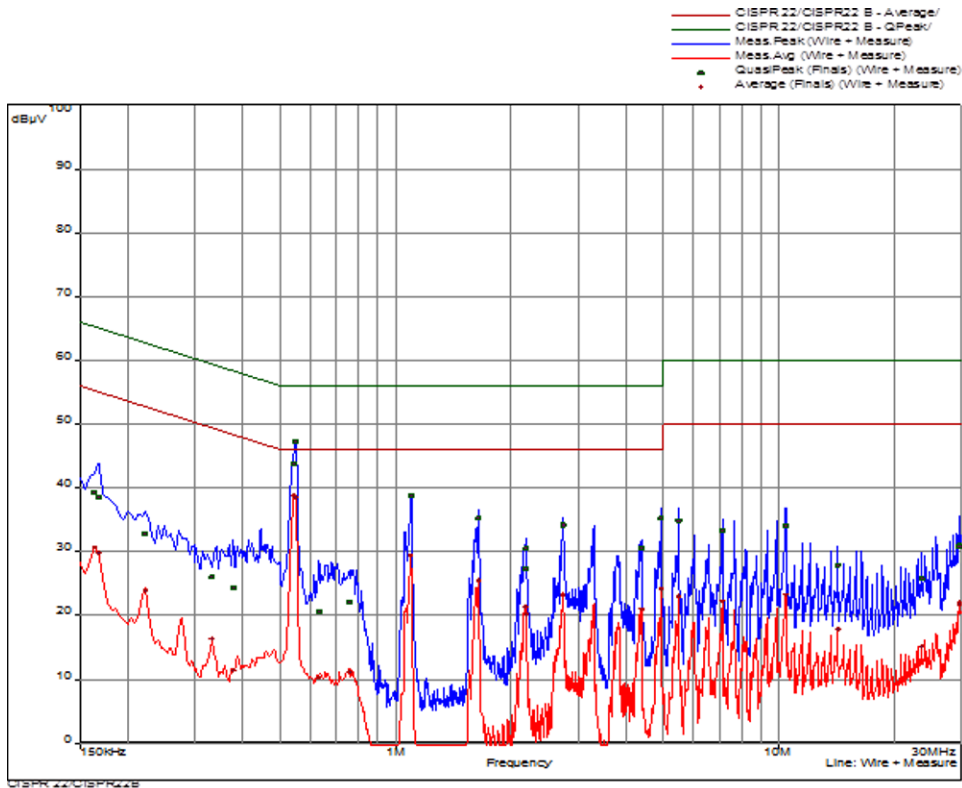


図 23. Conducted Emission Test Result (Wire +)

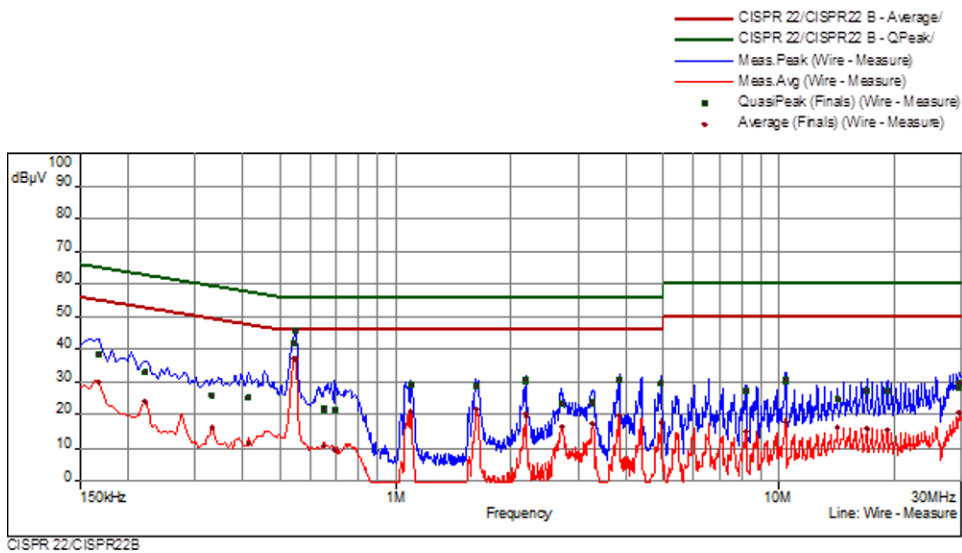


図 24. Conducted Emission Test Result (Wire -)

表 10. Conducted Emission Test Result

FREQ (MHz)	SR	QP (dBμV)	MARGIN (dB)	LIMIT (dB)	AV (dBμV)	MARGIN (dB)	LIMIT (dB)	LINE	CORR (dB)
0.1635	1	39.37	25.92	65.28	30.70	24.59	55.28	Wire + Measure	10.21
0.1680	1	38.58	26.48	65.06	29.77	25.29	55.06	Wire + Measure	10.21
0.2220	1	32.84	29.90	62.74	23.93	28.81	52.74	Wire + Measure	10.22
0.3315	2	25.99	33.43	59.41	16.36	33.05	49.41	Wire + Measure	10.23
0.3765	2	24.31	34.05	58.36	11.43	36.93	48.36	Wire + Measure	10.23
0.5430	2	43.77	12.23	56.00	38.88	7.12	46.00	Wire + Measure	10.24
0.5475	2	47.26	8.74	56.00	38.59	7.41	46.00	Wire + Measure	10.24
0.6315	3	20.67	35.33	56.00	10.28	35.72	46.00	Wire + Measure	10.24
0.7575	3	22.11	33.89	56.00	11.17	34.83	46.00	Wire + Measure	10.24
1.0950	3	38.76	17.24	56.00	29.49	16.51	46.00	Wire + Measure	10.24
1.6455	4	35.21	20.79	56.00	25.55	20.45	46.00	Wire + Measure	10.26
2.1765	4	27.41	28.59	56.00	21.40	24.60	46.00	Wire + Measure	10.28
2.1945	4	30.51	25.49	56.00	20.23	25.77	46.00	Wire + Measure	10.28
2.7420	5	34.17	21.83	56.00	23.22	22.78	46.00	Wire + Measure	10.30
4.3845	5	30.45	25.55	56.00	20.97	25.03	46.00	Wire + Measure	10.38
4.9350	6	35.29	20.71	56.00	24.19	21.81	46.00	Wire + Measure	10.41
5.4840	6	34.93	25.07	60.00	23.07	26.93	50.00	Wire + Measure	10.44
7.1310	6	33.33	26.67	60.00	22.25	27.75	50.00	Wire + Measure	10.55
10.4235	7	34.11	25.89	60.00	23.25	26.75	50.00	Wire + Measure	10.65
14.2665	7	27.90	32.10	60.00	17.87	32.13	50.00	Wire + Measure	10.95
23.6010	8	25.75	34.25	60.00	15.18	34.82	50.00	Wire + Measure	11.59
29.6355	8	31.04	28.96	60.00	22.02	27.98	50.00	Wire + Measure	11.76
29.6400	8	30.79	29.21	60.00	21.82	28.18	50.00	Wire + Measure	11.76
0.1680	9	38.54	26.52	65.06	29.93	25.13	55.06	Wire - Measure	10.21
0.2220	9	32.87	29.87	62.74	23.96	28.78	52.74	Wire - Measure	10.22
0.3315	10	26.01	33.41	59.41	16.41	33.00	49.41	Wire - Measure	10.23
0.4125	10	25.16	32.44	57.60	11.74	35.85	47.60	Wire - Measure	10.24
0.5430	10	41.97	14.03	56.00	37.18	8.82	46.00	Wire - Measure	10.24

**表 10. Conducted Emission Test Result (continued)**

FREQ (MHz)	SR	QP (dB $\mu$ V)	MARGIN (dB)	LIMIT (dB)	AV (dB $\mu$ V)	MARGIN (dB)	LIMIT (dB)	LINE	CORR (dB)
0.5475	10	45.48	10.52	56.00	37.01	8.99	46.00	Wire - Measure	10.24
0.6495	11	21.62	34.38	56.00	10.83	35.17	46.00	Wire - Measure	10.24
0.6945	11	21.47	34.53	56.00	9.66	36.34	46.00	Wire - Measure	10.24
1.0950	11	29.34	26.66	56.00	20.95	25.05	46.00	Wire - Measure	10.24
1.6230	12	28.79	27.21	56.00	21.85	24.15	46.00	Wire - Measure	10.26
2.1900	12	30.08	25.92	56.00	20.19	25.81	46.00	Wire - Measure	10.28
2.1945	12	30.65	25.35	56.00	19.43	26.57	46.00	Wire - Measure	10.28
2.7060	13	23.14	32.86	56.00	16.83	29.17	46.00	Wire - Measure	10.30
3.2730	13	23.58	32.42	56.00	17.77	28.23	46.00	Wire - Measure	10.33
3.8400	13	30.72	25.28	56.00	19.80	26.20	46.00	Wire - Measure	10.36
4.9350	14	29.66	26.34	56.00	18.20	27.80	46.00	Wire - Measure	10.41
8.2290	14	27.25	32.75	60.00	15.54	34.46	50.00	Wire - Measure	10.63
10.4235	15	30.33	29.67	60.00	18.35	31.65	50.00	Wire - Measure	10.65
10.4280	15	30.51	29.49	60.00	18.32	31.68	50.00	Wire - Measure	10.65
14.2665	15	24.61	35.39	60.00	16.54	33.46	50.00	Wire - Measure	10.95
17.0115	15	27.34	32.66	60.00	16.23	33.77	50.00	Wire - Measure	11.35
19.2045	16	27.04	32.96	60.00	15.63	34.37	50.00	Wire - Measure	11.53
29.5950	16	28.22	31.78	60.00	20.61	29.39	50.00	Wire - Measure	11.75
29.6400	16	29.56	30.44	60.00	20.60	29.40	50.00	Wire - Measure	11.76

### 3.2.2.10.2 Radiated Emission

The radiated emission is tested first with a prescan test with an antenna at 3 m and a threshold higher from 10 dB. This pretest identifies the critical points (less than 20 dB of margin) for the 10-m test.

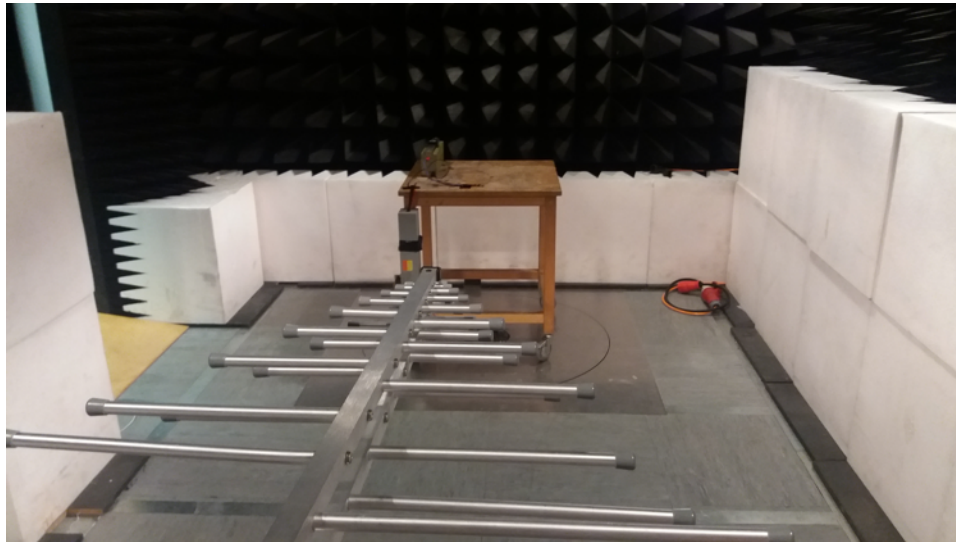


図 25. Radiated Emission 3-m Prescan Test Setup

**CAUTION**

For the prescan, due to the shorter distance (3 m instead of 10 m), the threshold for radiated EMI of EN55022 is higher by 10 dB.

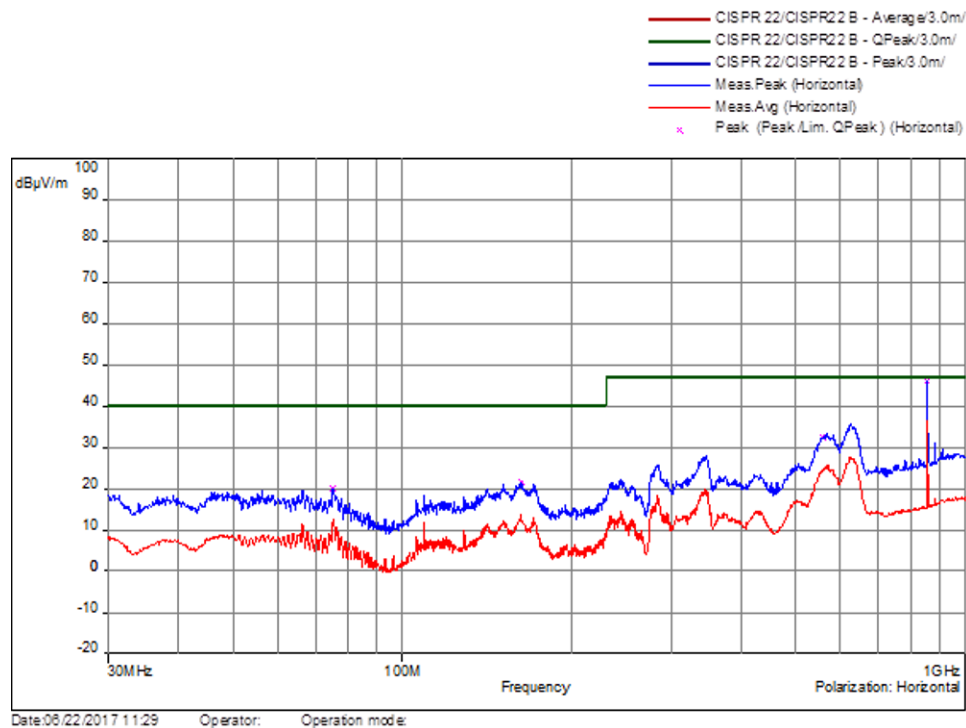
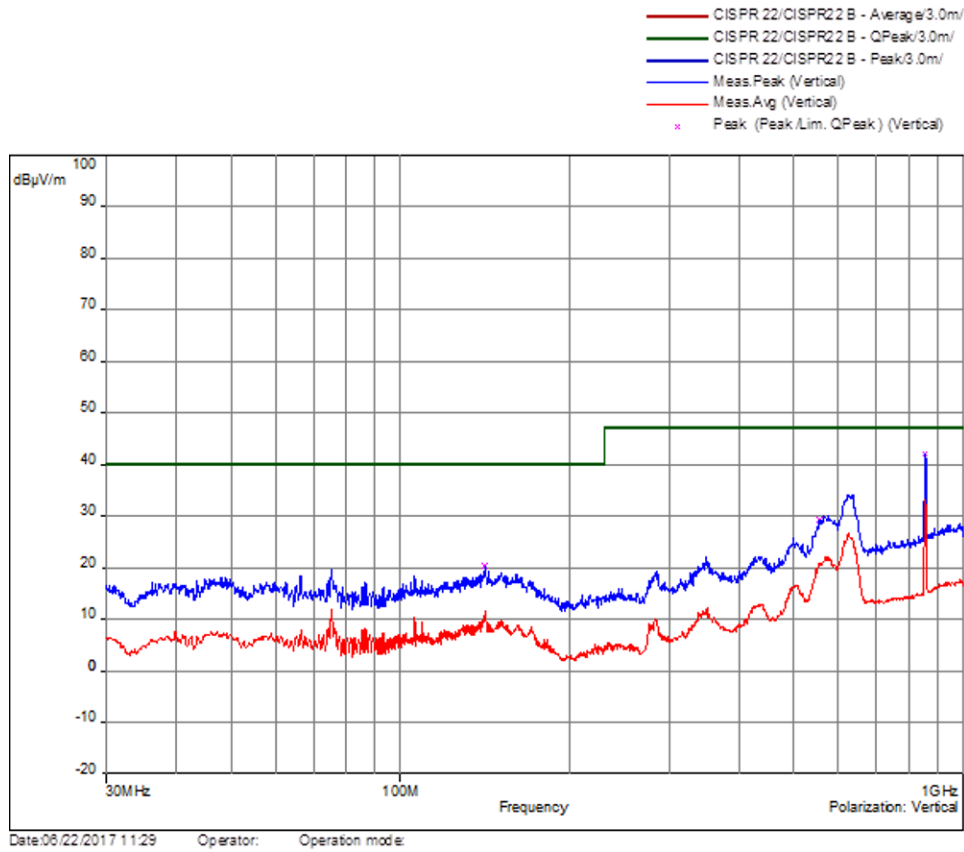


図 26. Radiated Emission 3-m Prescan Test Horizontal Polarization





☒ 27. Radiated Emission 3-m Prescan Test Vertical Polarization

表 11. Radiated Emission 3-m Prescan List of Critical Points

FREQ (MHz)	SR	PK (dB $\mu$ V/m)	LIMIT QP (dB $\mu$ V/m)	MARGIN (dB)	ANGLE (°)	POLARIZATION	CORR
75.202	1	20.08	40.00	-19.92	310.60	Horizontal polarization	-9.22
162.405	1	21.54	40.00	-18.46	290.70	Horizontal polarization	-5.85
557.971	1	32.42	47.00	-14.58	290.70	Horizontal polarization	1.01
855.373	1	45.92	47.00	-1.08	120.60	Horizontal polarization	5.53
141.356	2	20.35	40.00	-19.65	329.40	Vertical polarization	-5.31
554.770	2	29.38	47.00	-17.62	0.70	Vertical polarization	0.42
856.246	2	42.06	47.00	-4.94	249.40	Vertical polarization	5.28

Those critical points are then tested in the typical 10-m setup.

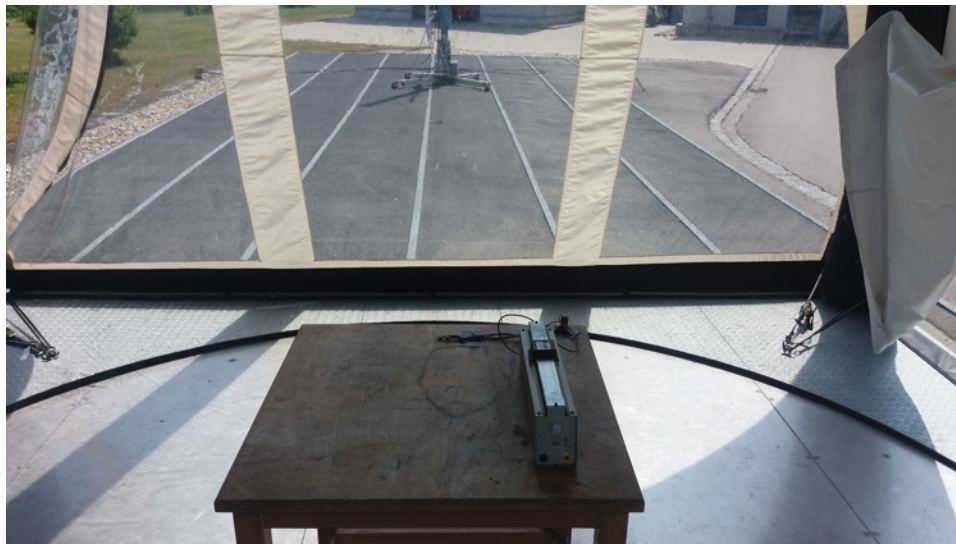


図 28. Radiated Emission 10-m Test Setup

During the scan, the board passed the radiated emission test with more than 4 dB of margin.

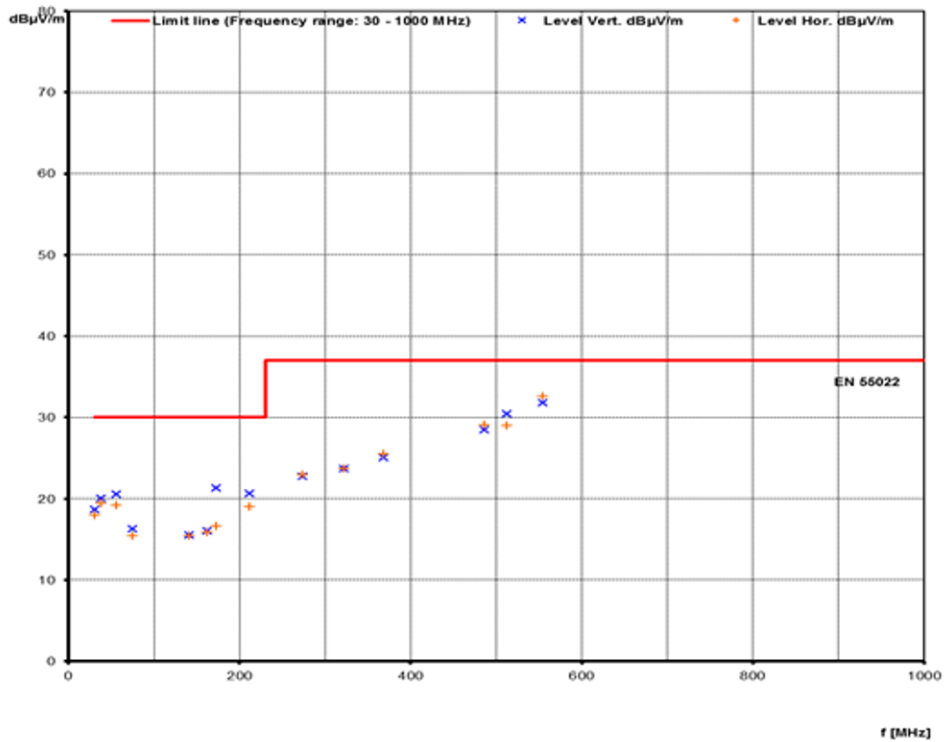


図 29. Radiated Emission 10-m Test Result

表 12. Radiated Emission 10-m Test Result

FREQ (MHZ)	READING VERT (dBµV)	READING HOR (dBµV)	CORRECT VERT (dB/m)	CORRECT HOR (dB/m)	LEVEL VERT (dBµV/m)	LEVEL HOR (dBµV/m)	LIMIT (dBµV/m)	D <sub>LIMIT</sub> (dB)
30.00	5.5	4.8	13.2	13.2	18.7	18.0	30.0	-11.3
38.40	5.8	5.2	14.3	14.3	20.1	19.5	30.0	-9.9
55.30	6.2	4.8	14.4	14.4	20.6	19.2	30.0	-9.4
75.20	6.1	5.2	10.2	10.2	16.3	15.4	30.0	-13.7
141.35	5.4	5.3	10.1	10.1	15.5	15.4	30.0	-14.5
162.40	5.3	5.1	10.7	10.7	16.0	15.8	30.0	-14.0
172.76	10.0	5.3	11.4	11.4	21.4	16.7	30.0	-8.6
211.76	6.9	5.3	13.7	13.7	20.6	19.0	30.0	-9.4
273.46	6.9	7.0	15.9	15.9	22.8	22.9	37.0	-14.1
321.56	6.4	6.4	17.3	17.3	23.7	23.7	37.0	-13.3
368.06	6.5	7.0	18.5	18.5	25.0	25.5	37.0	-11.5
485.46	7.1	7.7	21.4	21.4	28.5	29.1	37.0	-7.9
512.56	8.5	7.0	22.0	22.0	30.5	29.0	37.0	-6.5
554.57	9.1	9.8	22.8	22.8	31.9	32.6	37.0	-4.4

## 4 Design Files

### 4.1 Schematics

To download the schematics, see the design files at [TIDA-01450](#).

### 4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-01450](#).

### 4.3 PCB Layout Recommendations

In switch mode DC/DC, take special care to avoid coupling between the different loops. In a Buck topology, the input loop is particularly critical; for this reason, place the input capacitors as close as possible to the TPS561201.

This is done by separating the noise sensitive loop (Feedback and Enable) from the high di/dt loops (input, switch node, bootstrap). Separate these loops by placing the components and traces of the feedback and enable loop as far as possible from components and traces with high di/dt.

Also give special attention to the ground plane; try to make it as large and as solid as possible to both reduce noise sensitivity and help thermal dissipation.

With regards to thermal dissipation, the input and output voltage planes must also be made as large and as solid as possible to help keep the board as cool as possible.

Lastly, the soldering pad for the inductor is slightly enlarged to allow the tests of several inductors.

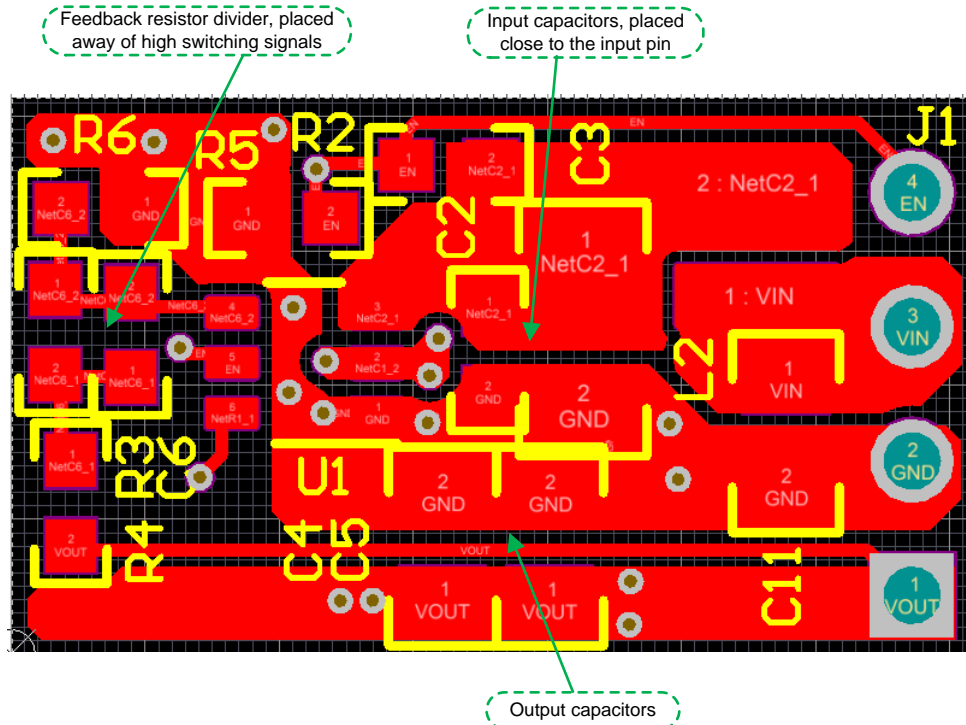


図 30. Top Layer

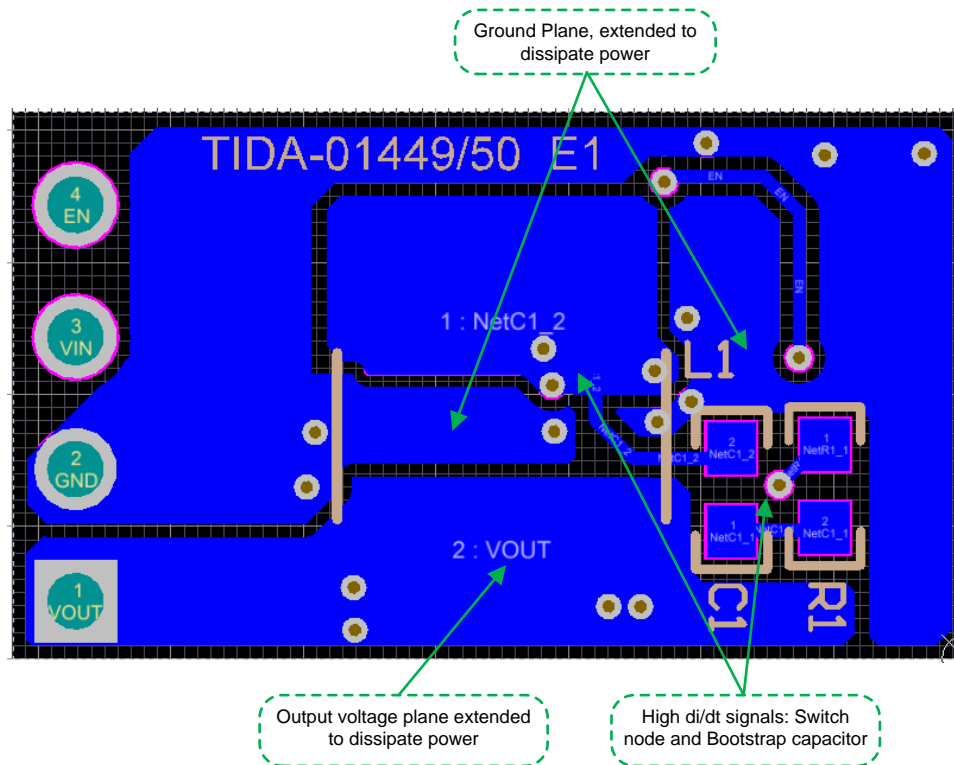


図 31. Bottom Layer (Flipped)

#### 4.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-01450](#).

#### 4.4 Altium Project

To download the Altium project files, see the design files at [TIDA-01450](#).

#### 4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-01450](#).

#### 4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-01450](#).

### 5 Related Documentation

1. Texas Instruments, [Understanding Buck Power Stages In Switchmode Power Supplies](#), Application Report (SLVA057)
2. Texas Instruments, [Layout Tips for EMI Reduction in DC / DC Converters](#), AN-2155 Application Report (SNVA638)
3. Texas Instruments, [Simple Success With Conducted EMI From DCDC Converters](#), AN-2162 Application Report (SNVA489)

## 5.1 商標

D-CAP2 is a trademark of Texas Instruments.

Wi-Fi is a registered trademark of Wi-Fi Alliance.

すべての商標および登録商標はそれぞれの所有者に帰属します。

## 6 About the Author

**KEVIN STAUDER** is a system engineer in the Industrial Systems team at Texas Instruments, responsible for developing TI Designs for industrial applications.

## TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的で、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジーまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、あるいはTIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的にかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示的保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁済または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際の、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(<http://www.ti.com/sc/docs/stdterms.htm>)、評価モジュール、およびサンプル(<http://www.ti.com/sc/docs/sampterm.htm>)についてのTIの標準条項が含まれますが、これらに限られません。