参考資料

TI Designs: TIDA-01516
Bluetooth® Low Energy 5.0対応シングルMCU、18V/600W BLDCモータ制御のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインは、5セルのリチウムイオン・バッテリで動作する電動工具などの産業用アプリケーションにおいて、*Bluetooth*® 5.0 SimpleLink™オプションを提供し、優れた産業ノイズ耐性と広い電圧範囲、低消費電力を実現します。この電力段のリファレンス・デザインは、1つのBluetooth Low Energy (BLE) MCUをワイヤレス接続と三相ブラシレスDC (BLDC)モータの台形制御の両方に使用するものであり、1つの基板に設計されているため、BOMおよび総コストを低減できます。電力段がモータを駆動していてもBLE受信感度－96dBmを達成し、堅牢なRF性能を示しています。また、MOSFET V_{DS}センシングによる過電流および短絡保護機能を備えた小型の電力段でもあります。

リソース

TIDA-01516	デザイン・フォルダ
CSD88584Q5DC	プロダクト・フォルダ
DRV8323	プロダクト・フォルダ
CC2640R2F	プロダクト・フォルダ
TPS709	プロダクト・フォルダ
LMT87-Q1	プロダクト・フォルダ
TPD1E10B06	プロダクト・フォルダ

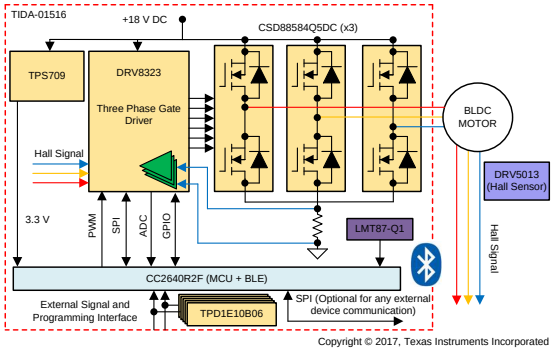
TI E2E™ Community　E2E™エキスパートに質問

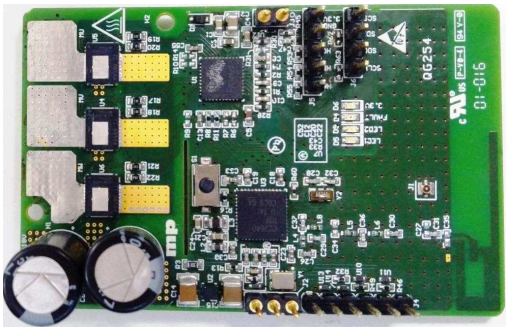
特長

- 1つのMCUにモータ制御機能とBLE接続機能を統合
- BLDCモータ用の600Wドライブで、センサ・ベースの台形制御をサポート
- 6V～21.6Vで動作する設計
- ヒート・シンクなしで27A_{RMS}の連続巻線電流をサポート
- 70mm×45mmの小型PCBフォーム・ファクタ
- スマート・ゲート・ドライバを使用する単一PWM制御により、MCUのオーバーヘッドを低減
- 61µA/MHzのCortex-M3 MCUに独自のコア・ベース・センサ・コントローラを追加したBluetooth 5.0 SimpleLinkソリューションを提供
- BLEによる超低消費電力動作: 接続間隔1秒で平均10µA未満、スリープ電流1µA
- モータ動作時も最高水準の受信感度を実現: －96dBm (概算値)
- 過電流およびモータのストール電流をサイクル単位で非ラッチ制限、およびV_{DS}センシングによる短絡ラッチ保護
- 動作時周囲温度: －20℃～＋55℃

アプリケーション

- コードレス電動工具
- コードレス園芸用具
- コードレス掃除機
- 電動アシスト自転車





1 System Description

Power tools are used in various industrial and household applications such as drilling, grinding, cutting, polishing, driving fasteners, various garden applications, and so on. Power tools can be either corded or cordless (battery powered). Corded power tools use the mains power (the grid power) to power up the AC or DC motors. The cordless tools use battery power to drive DC motors. Cordless tools use brushed or brushless DC (BLDC) motors. The BLDC motors are more efficient and have less maintenance, low noise, and longer life.

These tools are getting smarter with the use of wireless connectivity. The wireless connectivity option gives many smart features such as:

- Tool authentication
- Tool tracking
- Intelligent inventory management
- Immediate fault reporting from the tool
- Understanding the status of the tool like the battery conditions and total operating duration

This option also enables online configuration of parameters like torque limit, type of material drilling, and so on.

The most common solution for wireless connectivity used in power tools, garden tools, and vacuum cleaners is Bluetooth low energy (BLE). The Bluetooth low energy option is provided as a separate module or as integrated part of the tool. This reference design uses TI's latest chip CC2640R2F, offering Bluetooth low energy 5.0. This version comes with long range, low power consumption, best RF performance and good industrial immunity.

This reference design uses the single microcontroller (MCU), CC2640R2F, to do both BLDC trapezoidal motor control and Bluetooth connectivity. This reference design uses TI's latest smart three-phase gate driver DRV8323, which comes with advanced features like single PWM control, eliminating a lot overhead from the MCU. The design uses the CSD88584Q5DC NexFET™ power block featuring a very low R_{DS_ON} of 0.68 mΩ in a SON5×6 SMD package. The power block with high-side and low-side FETs in a single package helps to achieve a very small form factor and better switching performance. The three-phase gate driver DRV8323 is used to drive the three-phase MOSFET bridge, which can operate from 6 V to 60 V and support a programmable gate current with a maximum setting of 2-A sink and 1-A source. The SPI provides detailed fault reporting and flexible parameter settings such as gain options for the current shunt amplifier, slew rate control of the gate drivers, and various protection features. The TPS709 LDO, featuring a low quiescent current (< 1 µA), generates the low-noise, stable, 3.3-V power supply for the MCU.

The test report evaluates the RMS current capability, peak current capability and thermal performance of the board, FET switching waveforms, and overcurrent protection features such as cycle-by-cycle control and latch control of the DRV8323. The test results also shows the robust RF performance with low power consumption. A low noise coupling or interference from the motor drive side enables the designers to integrate Bluetooth low energy along with the motor control with much lower noise interference, lowering the overall cost.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATION
Input voltage	18-V DC (6-V min to 21-V max), five-cell Li-Ion battery
Rated output power	600 W
RMS winding current	27 A
Control method	Sensor-based trapezoidal
Inverter switching frequency	20 kHz (adjustable from 5 kHz to 100 kHz)
Feedback signals	DC bus voltage, Hall sensor, low-side DC bus current
Protections	Cycle-by-cycle overcurrent, input undervoltage, over-temperature
Cooling	Natural cooling only, no heat sink
Operating ambient	–20°C to +55°C
Board specification	70 mm × 45 mm, four-layer, 1-oz copper
Efficiency	> 98.5%
Bluetooth	Bluetooth low energy 5.0
Maximum TX power	5 dBm
RX sensitivity	–96 dBm, 1 Mbps, BER < 0.1%

2 System Overview

2.1 Block Diagram

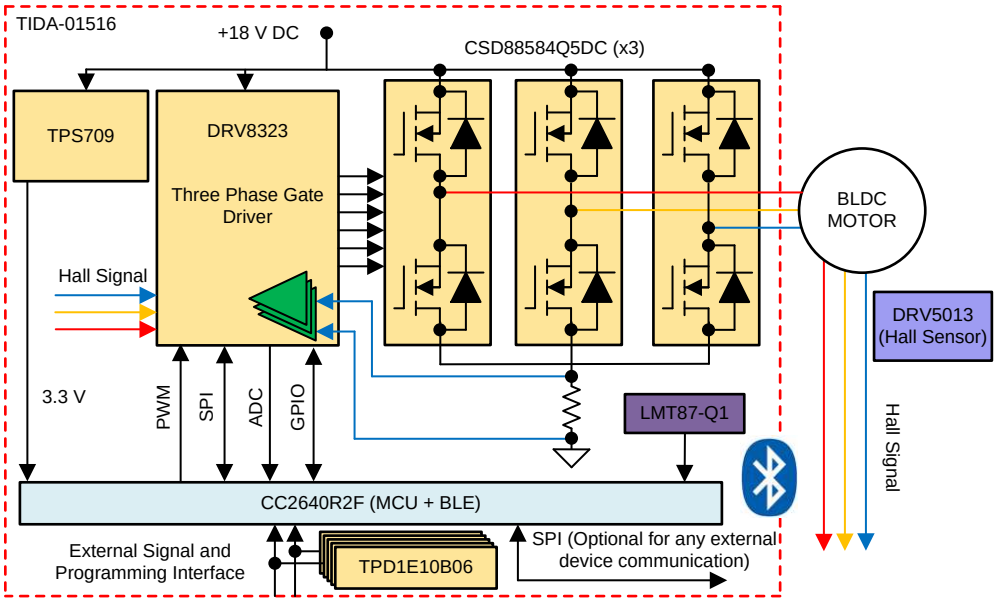


図 1. TIDA-01516 Block Diagram

2.2 Highlighted Products

2.2.1 CSD88584Q5DC

The key requirements in selecting the MOSFET are:

- High efficiency (MOSFET with low losses under operating condition)
- Small size to reduce the solution form factor
- Better heat dissipation
- High peak current capability
- Better switching performance to ensure reliable operation under short circuit or worst case switching conditions

The CSD88584Q5DC 40-V power block is the best option to meet these requirements for high-current motor control applications such as hand held, cordless garden, and power tools. This device uses TI's patented stacked die technology to minimize parasitic inductances while offering a complete half bridge in a space-saving, thermally enhanced, DualCool™ 5-mm × 6-mm package. With an exposed metal top, this power block device allows a simple heat sink application to draw heat out through the top of the package and away from the PCB for a superior thermal performance at the higher currents demanded by many motor control applications.

Integration of low-side and high-side MOSFETs in the same package allow the automatic thermal equalization between the top and bottom MOSFETs, even if the MOSFETs have different power losses.

This device integrates low-side and high-side MOSFETs in the same package to equalize their temperature automatically, even if the MOSFETs have different power losses.

2.2.2 DRV8323

The key requirements in selecting the gate driver are:

- Three-phase gate driver with high level of integration to reduce the form factor
- Sufficient source and sink current to reduce the switching losses
- Sufficiently high gate drive voltage to enable the MOSFET conducts at the minimum R_{DS_ON}
- High level of overcurrent and other protections to enable a reliable system operation under worst case conditions like motor stall, short circuit, and so on

The DRV8323 three-phase gate driver can be used to meet the above requirements. The device provides three half-bridge drivers, each capable of driving one high-side and one low-side N-channel MOSFET. The DRV832x generates the proper gate voltage drive for both the high-side and low-side FETs using a charge pump. The DRV832x supports up to 1 A source and 2 A sink peak gate drive current capability. The DRV832x can operate from a single power supply and supports a wide input supply range from 6 to 60 V. The DRV8323 includes three current shunt amplifiers for accurate current measurements, supports 100% duty cycle and have multiple levels of protection.

2.2.3 CC2640R2F

The CC2640R2F device is a wireless MCU targeting Bluetooth 4.2 and Bluetooth 5.0 low-energy applications. The device is a member of the SimpleLink ultra-low-power CC26xx family of cost-effective, 2.4-GHz RF devices. Very low active RF and MCU current and low-power mode current consumption provide excellent battery lifetime.

The SimpleLink Bluetooth low energy CC2640R2F device contains a 32-bit Arm® Cortex®-M3 core that runs at 48 MHz as the main processor and a rich peripheral feature set that includes a unique ultra-low-power sensor controller. This sensor controller is ideal for interfacing external sensors and for collecting analog and digital data autonomously while the rest of the system is in sleep mode. Thus, the CC2640R2F device is great for a wide range of applications where long battery lifetime, small form factor, and ease of use is important.

Bluetooth low energy controller and host libraries are embedded in ROM and run partly on an Arm Cortex-M0 processor. This architecture improves overall system performance and power consumption and frees up significant amounts of flash memory for the application. 図 2 shows the functional block diagram of the CC2640R2F.

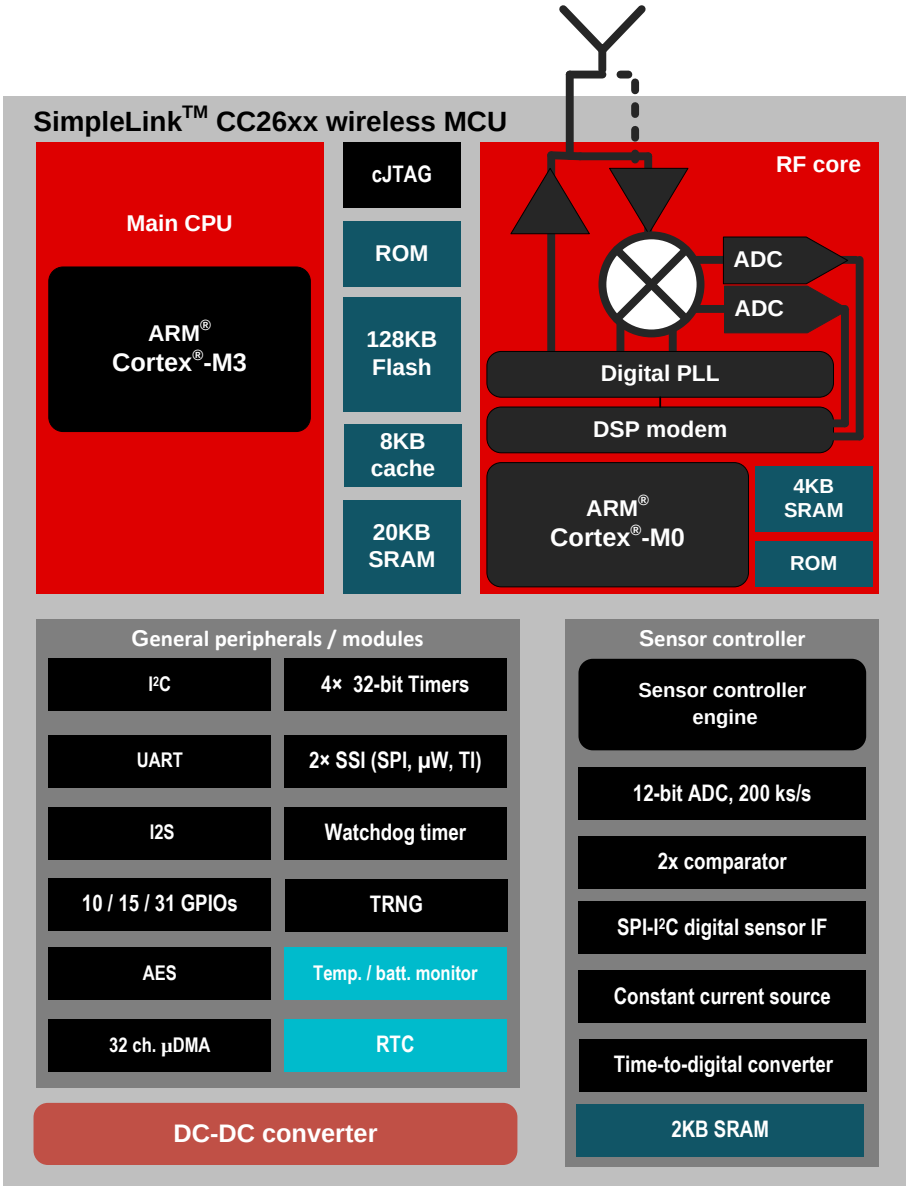


図 2. Functional Block Diagram of CC2640R2F

The sensor controller, general peripherals, and modules help the designer to easily integrate the motor control functions on top of the RF functions. The peripherals in the sensor controller include the following:

- The low-power clocked comparator can be used to wake the device from any state in which the comparator is active.
- Capacitive sensing functionality is implemented through the use of a constant current source, a time to-digital converter, and a comparator.
- The ADC is a 12-bit, 200-ksamples/s ADC with eight inputs and a built-in voltage reference. The ADC can be triggered by many different sources, including timers, I/O pins, software, the analog comparator, and the RTC.
- The sensor controller also includes an SPI to I^{2}C digital interface.

- The analog modules can be connected to up to eight different GPIOs. The peripherals in the sensor controller can also be controlled from the main application processor.

The I/O controller controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable).

General peripherals and modules include the following:

- The synchronous serial interfaces (SSIs) are synchronous serial interfaces that are compatible with SPI, MICROWIRE, and Texas Instruments' SSIs. The SSIs support both SPI master and slave up to 4 MHz.
- The UART implements a universal asynchronous receiver and transmitter function and supports flexible baud rate generation up to a maximum of 3 Mbps.
- Timer 0 is a general-purpose timer module (GPTM), which provides two 16-bit timers. The GPTM can be configured to operate as a single 32-bit timer, dual 16-bit timers, or as a PWM module. Timer 1, Timer 2, and Timer 3 are also GPTMs. Each of these timers is functionally equivalent to Timer 0.
- In addition to these four timers, the RF core has its own timer to handle timing for RF protocols; the RF timer can be synchronized to the RTC.
- The I^2C interface capable of 100-kHz and 400-kHz operation and can serve as both I^2C master and I^2C slave.
- The TRNG module provides a true, non-deterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements.
- The watchdog timer is used to regain control if the system fails due to a software error after an external device fails to respond as expected.

2.2.4 TPS709

The TPS709 linear regulator is an ultra-low, quiescent current device designed for power-sensitive applications. The LDO can work up to a 30-V input voltage, which makes it ideal for a five-cell Li-ion battery supply application. A precision band-gap and error amplifier provides 2% accuracy over temperature. A quiescent current of only 1 µA makes this LDO ideal for battery-powered, always-on systems that require very little idle-state power dissipation. This device has thermal-shutdown, current-limit, and reverse-current protections for added safety. The TPS709 linear regulator is available in WSON-6 and SOT-23-5 packages.

2.2.5 LMT87-Q1

The LMT87-Q1 is a precision CMOS integrated-circuit temperature sensor with an analog output voltage that is linearly and inversely proportional to temperature. The sensor can operate down to a 2.7-V supply with 5.4-µA power consumption. Package options including through-hole TO-92 package allows the LMT87-Q1 to be mounted onboard, off-board, to a heat sink, or on multiple unique locations. The LMT87-Q1 has accuracy specified in the operating range of −50°C to +150°C.

2.2.6 TPD1E10B06

The TPD1E10B06 device is a single-channel electrostatic discharge (ESD) transient voltage suppression (TVS) diode in a small 0402 package. This TVS protection product offers ±30-kV contact ESD, ±30-kV IEC air-gap protection, and has an ESD clamp circuit with a back-to-back TVS diode for bipolar or bidirectional signal support. Typical applications of this ESD protection product are circuit protection for general-purpose I/O ports.

2.3 System Design Theory

The three-phase BLDC motor needs a three-phase electronic drive to energize the motor based on the rotor position. The electronic drive in this reference design consists of the following:

- Power stage with a three-phase inverter having the required power capability
- MCU to implement the motor control algorithm and having Bluetooth low energy capability
- Position sensor for accurate motor current commutation
- Gate driver for driving the three-phase inverter
- Power supply to power up the MCU

2.3.1 Power Stage Design—Battery Power Input to the Board

図 3 shows the section for the battery power input. The input bulk aluminum electrolytic capacitors C6 and C7 provide the ripple current, and its voltage rating is de-rated by 20% for better life. These capacitors are rated to carry high-ripple current. C11 is used as a high-frequency bypass capacitor. D1 is the TVS having a breakdown voltage of 30 V.

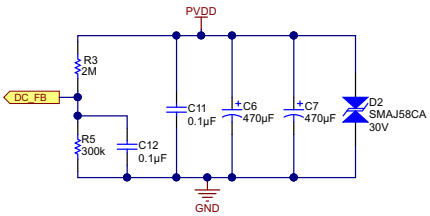


図 3. Schematic of Battery Power Input Section

The input supply voltage PVDD is scaled using the resistive divider network, which consists of R3, R5 and C12, and fed to the MCU. Considering the maximum voltage for the MCU ADC input as 3.3 V, the maximum DC input voltage measurable by the MCU is calculated as in 式 1:

$$V_{DC}^{max} = V_{ADC\_DC}^{max} \times \frac{(300\ k\Omega + 2000\ k\Omega)}{300\ k\Omega} = 3.3 \times \frac{(300\ k\Omega + 2000\ k\Omega)}{300\ k\Omega} = 25.3\ V \quad (1)$$

Considering 15% headroom for this value, the maximum recommended voltage input to the system is 25.3 × 0.85 = 21.5. So for a power stage with maximum operating voltage of 21 V, this voltage feedback resistor divider is ideal. Also, this choice gives optimal ADC resolution for a system operating from 6 V to 21 V.

2.3.2 Power Stage Design—Three-Phase Inverter

The three-phase inverter is realized using three MOSFET power blocks. Each power block consists of two MOSFETs connected as a high-side and low-side FET, which can be used as one leg of the inverter. 図 4 shows one leg of the power stage. This stage consists of one power block and the decoupling capacitor C40 placed close across power blocks to reduce the ringing in the supply lines because of the parasitic inductance added by the sense resistor and the power track.

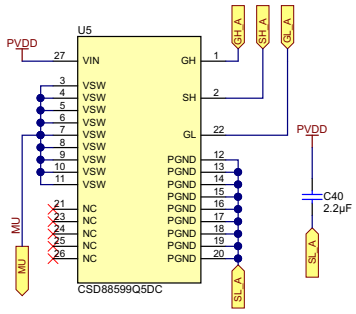


図 4. Schematic of One Half Bridge of Three-Phase MOSFET Inverter

注: Connect the decoupling capacitors very near to the corresponding MOSFET legs for better decoupling. An improper layout or position of the decoupling capacitors can cause undesired V_{DS} switching voltage spikes.

The design measures DC bus current using the shunt resistors R23 and R24 mounted on the DC bus return path, as shown in 図 5. The sensed currents are fed to the MCU through the current shunt amplifiers .

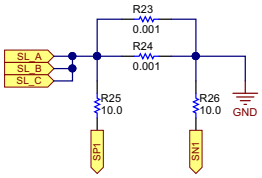


図 5. Schematic of External Shunt for Current Sensing

Power dissipation in sense resistors and the input offset error voltage of the op amps are important in selecting the sense resistance values. The sense resistors are designed to carry a maximum continuous RMS current of 35 A with a peak current of 60 A for 2 seconds. A high sense resistance value increases the power loss in the resistors. The internal current shunt amplifiers of the DRV8323 have an input offset error of 4 mV. The DRV8323 has the DC offset voltage calibration feature. In case the amplifier is used without offset calibration, it is required to select the sense resistor such that the sense voltage across the resistor is sufficiently higher than the offset error voltage to reduce the effect of the offset error. Selecting a 0.5-mΩ resistor as the sense resistor, the power loss in the resistor at 35-A_{RMS} is given by 式 2:

$$\text{Power loss in the resistor} = I_{RMS}^2 \times R_{SENSE} = 35^2 \times 0.0005 = 0.6125 \text{ W} \quad (2)$$

At a 60-A peak current, using 式 2, the power loss in the resistor = 1.8 W (for 2 seconds). This reference design uses two 1-mΩ, 3-W resistors in parallel.

注: The user can consider reducing the sense resistor further down to reduce the power loss and use the current sense amplifier in maximum gain.

2.3.3 Power Stage Design—DRV8323 Gate Driver

図 6 shows the schematic of the DRV8323 gate driver. C5 is the DVDD decoupling capacitor that must be placed close to the device. PVDD is the DC supply input; in this case, it is a battery voltage of 18 V. A 4.7-µF capacitor (C2) is used as the PVDD capacitor. The diode D1 helps to decouple the gate driver power supply in case the battery voltage dips during short-circuit conditions. The presence of D1 enables the PVDD capacitor C2 to hold the voltage under small duration dips in supply voltage from battery and makes sure that the gate driver does not enter an undesired undervoltage lockout (UVLO). C3 and C4 are charge pump capacitors. The EN_GATE of DRV8323 is connected to the MCU. This connection helps the MCU to enable or disable the gate drive outputs of the DRV8323. For the voltage rating and selection of these capacitors, see the *DRV8323 6 to 60-V Three-Phase Smart Gate Driver Data Sheet*.

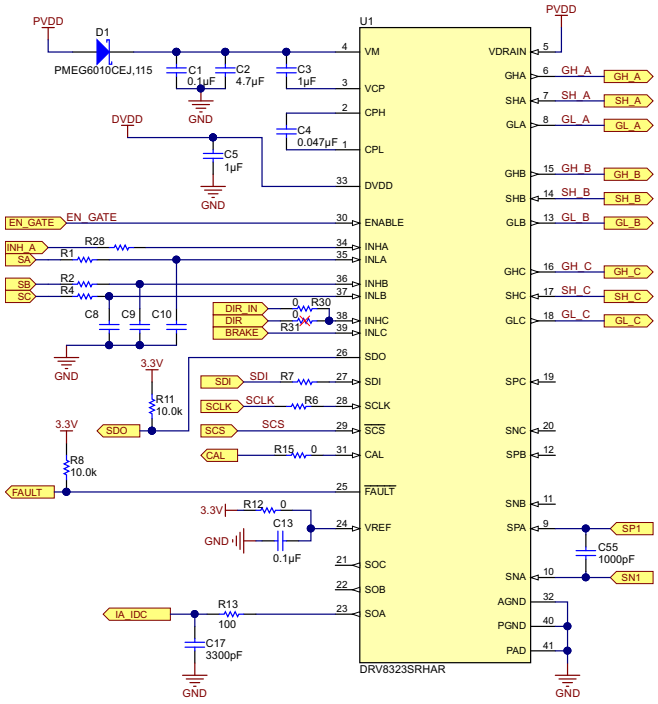


図 6. Schematic of DRV8323 Gate Driver

2.3.3.1 Features of DRV8323

The DRV8323 integrates three half-bridge gate drivers, each capable of driving high- and low-side N-channel MOSFETs. A doubler charge pump provides the proper gate bias voltage to the high-side MOSFET across a wide operating voltage range in addition to providing 100% duty cycle support. An internal LDO provides the gate bias voltage for the low-side MOSFETs. The DRV8323 implements a smart gate drive, which allows the user to adjust the gate drive current on the fly without requiring current-limiting gate drive resistors. Current is adjustable through the SPI or on the IDRIVE pin for the hardware interface.

The gate drivers support adjustable peak current and duration settings through the IDRIVE and TDRIVE settings. This support allows for adjusting the external MOSFET slew rate and provides additional system protection. The peak source and sink current of the DRV8323 gate drivers is adjustable either through the device registers or by an external pin, IDRIVE. Control of the MOSFET V_{DS} slew rates is an important parameter for optimizing emitted radiations and system efficiency. The rise and fall times also influence the energy and duration of the diode recovery spikes and dV/dt related turnon. When changing the state of the gate driver, the peak current (IDRIVE source or sink) is applied for a fixed period of time (TDRIVE) during which the gate capacitances are charged or discharged completely. After TDRIVE has expired, a fixed holding current (IHOLD) holds the gate at the desired state (pulled up or pulled down). During high-side turnon, the low-side gate is pulled low with a strong pulldown. This pulldown prevents the gate-to-source capacitance of the low-side MOSFET from inducing turnon.

The fixed TDRIVE time ensures that under abnormal circumstances like a short on the MOSFET gate or the inadvertent turnon of a MOSFET V_{GS} clamp, the high peak current through the DRV8323 gate drivers is limited to the energy of the peak current during TDRIVE. Limiting this energy helps to prevent damage to the gate drive pins and external MOSFET. The TDRIVE time must be selected to be longer than the time need to charge or discharge the MOSFET gate capacitances. IDRIVE and TDRIVE must be initially selected based on the parameters of the external MOSFET used in the system and the desired rise and fall times. TDRIVE does not increase the PWM time and will terminate if a PWM command is received while it is active. A recommended starting point is to select a TDRIVE that is approximately two times longer than the external MOSFET's switching rise and fall times.

The DRV8323 integrate the following protections, which help in making a reliable power stage:

- V_M UVLO
- V_{CP} UVLO
- V_{DS} overcurrent protection
- SENSE overcurrent protection
- Thermal shutdown
- Thermal warning

For more details, refer to the *DRV8323 6 to 60-V Three-Phase Smart Gate Driver Data Sheet*.

2.3.3.2 Current Shunt Amplifier in DRV8323

The SOx pin on the DRV8323 and DRV8323R outputs an analog voltage equal to the voltage across the SPx and SNx pins multiplied by the gain setting (GCSA). The gain setting is adjustable between four different levels (5 V/V, 10 V/V, 20 V/V, and 40 V/V). The current shunt amplifiers can be programmed and calibrated independently and can support bidirectional and unidirectional current sensing with programmable output bias scaling VREF or VREF/2. The amplifier can monitor the current through the half-bridges, and the current is approximately calculated as in 式 3.

$$SO_X = \frac{VREF}{2} + \left(I \times CSA\_GAIN \times R_{DS\_ON}\right) \quad (3)$$

図 7 shows the current sense amplifier configuration.

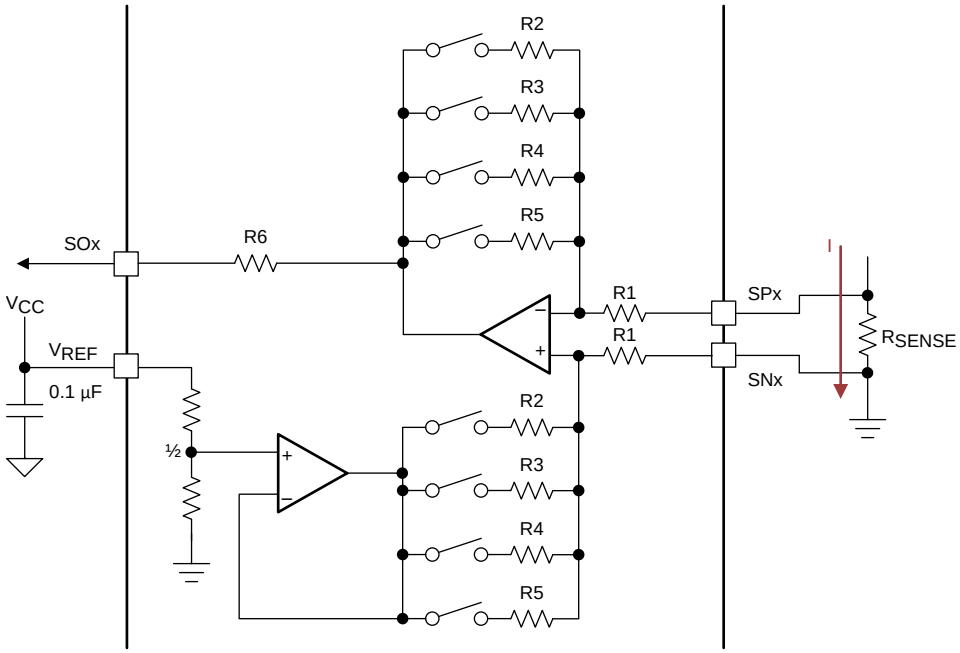


図 7. DRV8323 Current Shunt Amplifier Configuration

2.3.4 LDO—3.3-V Generation

The reference design uses the ultra-low quiescent current, low-dropout linear regulator TPS709 to generate the 3.3-V power supply for the MCU from the input voltage of 18 V. 図 8 shows the schematic of the LDO circuit.

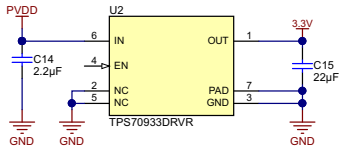


図 8. Schematic of 3.3-V LDO

The selection of LDO depends on the wide input voltage support (in this design, from 6 V to 21 V), the load current, and power dissipation. Power dissipation depends on input voltage and load conditions. Power dissipation (P_{diss}) is equal to the product of the output current and the voltage drop across the output pass element, as shown in 式 4:

$$P_{diss} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Assuming a nominal LDO load current of 30 mA, the power dissipation at V_{IN} = 21 V can be calculated as: P_{diss} = (21 – 3.3) × 0.03 = 0.531 W. 表 2 shows the specification of the LDO used for this reference design.

表 2. Specification of Buck Converter

PARAMETER	SPECIFICATION
Input voltage	6 V to 21 V (18-V nominal)
Output voltage	3.3 V
Maximum output current (for this reference design)	50 mA

For the detailed design of LDO, refer to the *TPS709 150-mA, 30-V, 1-μA IQ Voltage Regulators with Enable Data Sheet*.

2.3.5 Power Stage Design—Microcontroller CC2640R2F

図 9 shows the schematic for configuring the CC2640R2F MCU. The VDSS power supply for the MCU 3.3 V derived using a stable LDO with good power supply rejection ration (PSRR). The 3.3-V power supply is connected to the VDSS through L2 (a GHz Noise Suppression Chip Ferrite Bead), providing a low-noise supply to the MCU. C18, C19, C20, and C21 are the decoupling capacitors.

The VDDR power supply is generated using the internal DC/DC of CC2640R2F, and L3, C22, C23, and C24 form the filter components for the same. Y1 is the 24-MHz, high-frequency external clock and Y2 is the 32-kHz, low-frequency external clock. The GPIO pins of the CC2640R2F MCU (DIO_0 to DIO_30) interface with different functions such as ADC inputs, SPI communication, LED drives, PWM generation, and so on.

The RF front end is used in differential-ended configurations with internal biasing. The filter components are used at the RF front end and tuned for application. J1 is the JSC connector for conducted RF measurements. C27 and C31 share a single pad. To connect the antenna, mount C31, while for conducted RF measurements mount C27 and remove C31.

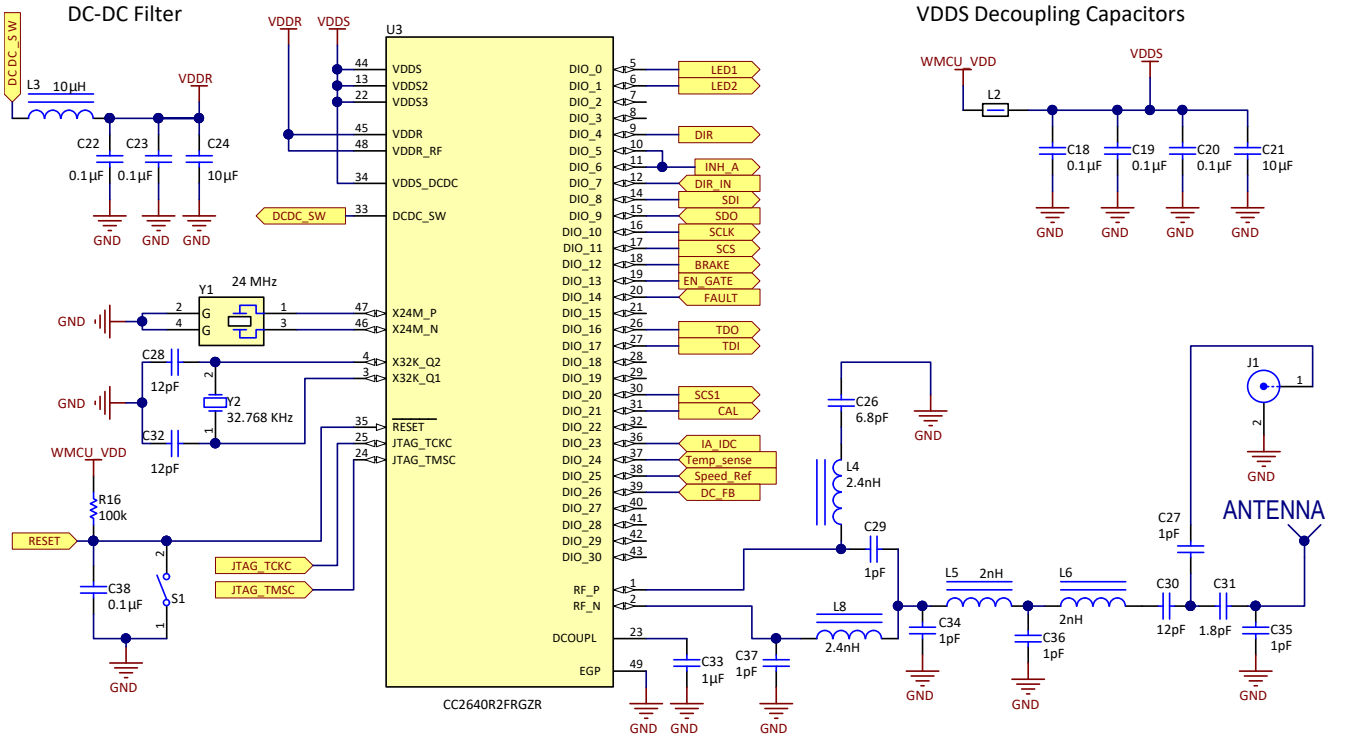


図 9. CC2640R2F Schematic

2.3.6 Power Stage Design—Hall Sensor Interface

図 10 shows the Hall sensor interface from the motor to the board. The 3.3 V is used as the power supply for the Hall sensor. Usually, the Hall sensors have an open drain or open collector configuration. R53, R54, and R55 are used as the pullup resistors.

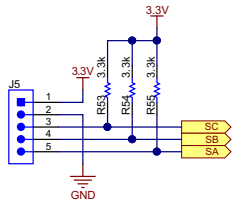


図 10. Schematic of Hall Sensor Connector

注: The Hall sensor connection must match with the winding connection for proper operation of the BLDC motor.

2.3.7 Temperature Sensing

図 11 shows the temperature sensor circuit used to measure the PCB temperature. The LMT87-Q1 is an analog output temperature sensor. The amplifier has a simple push-pull output stage, thus providing a low-impedance output source. The average output sensor gain is 13.6 mV/°C. The temperature sensor placed near the MOSFET to detect the close MOSFET temperature.

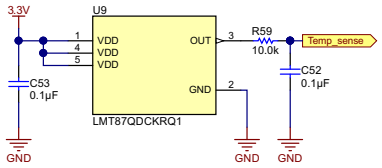


図 11. Schematic of Temperature Sensor

2.3.8 Power Stage Design—External Interface Options and Indications

2.3.8.1 Speed Control of Motor

The speed control is done using a potentiometer (POT), and the POT voltage is fed to the ADC of the MCU. 図 12 shows the schematic of the circuit. The POT is supplied from the 3.3-V supply. A 20k POT can be connected externally to the jumper J2. Connect the fixed terminals of the POT to terminal 1 and 3 of J1 and mid-point to terminal 2 of J2.

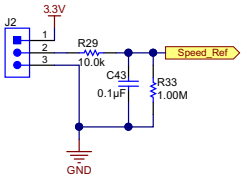


図 12. Schematic of Potentiometer Connection for Speed Control

The resistor R33 is used to ensure that the speed control reference is zero if the POT terminal is open.

2.3.8.2 Direction of Rotation—Digital Input

The jumper J3 (shown in 図 13) sets the direction of rotation of the motor. Close or open the jumper to change the direction of rotation. The pin is connected to the MCU. The MCU GPIO is connected to the direction control input of the DRV8323. The DIR_IN is also connected to the DRV8323 through R30 (see 図 7). The selection between R30 and R31 enable the direction control through MCU or directly by the jumper J3.

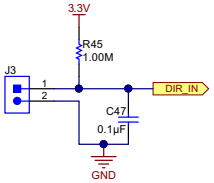


図 13. Schematic of Digital Input to Change Direction of Rotation

2.3.8.3 ESD Protection

The reference design uses ESD diodes for transient voltage protection at the digital pins that are accessible by the external user.

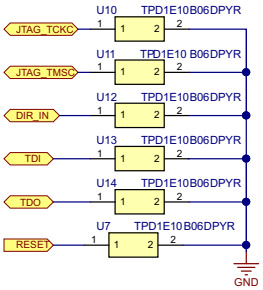


図 14. Schematic of ESD Protection

3 Hardware, Firmware, Testing Requirements, and Test Results

3.1 Required Hardware and Firmware

3.1.1 Hardware

3.1.1.1 Connector Configuration of TIDA-01516

図 15 shows the connector configuration of this reference design, which features the following:

- Two-terminal input for power supply: This pin is used to connect the input DC supply from the battery. The positive and negative terminals can be identified as shown in 図 15.
- Three-terminal output for motor winding connection: The phase output connects to the three-phase BLDC motor winding, marked as PHASE W, PHASE V, and PHASE U, as shown in 図 15.
- JSC connector J1: This connector is provided for conducted RF measurements. Connect C27 and disconnect C31 for conducted measurements.
- Three-pin connector J2: This connector can interface an external potentiometer for speed reference. The two fixed terminals of the potentiometer must be connected to the 3V3 pin and GND pin. The mid-point of the potentiometer must be connected to the POT pin of the connector.
- Two-pin connector J3: This connector is used for the motor direction change. Externally shorting or opening this connector changes the direction of the rotation of the motor.
- Six-pin connector J4: This is the programming connector for the MCU. The two-wire Spy-Bi-Wire protocol programs the CC2640R2. TDI and TDO lines are not required in this case.
- Five-pin connector J5: This is the interface for connecting the Hall position sensors from the motor.
- Four-pin connector J6: This connector is provided as an optional SPI for any external controller.

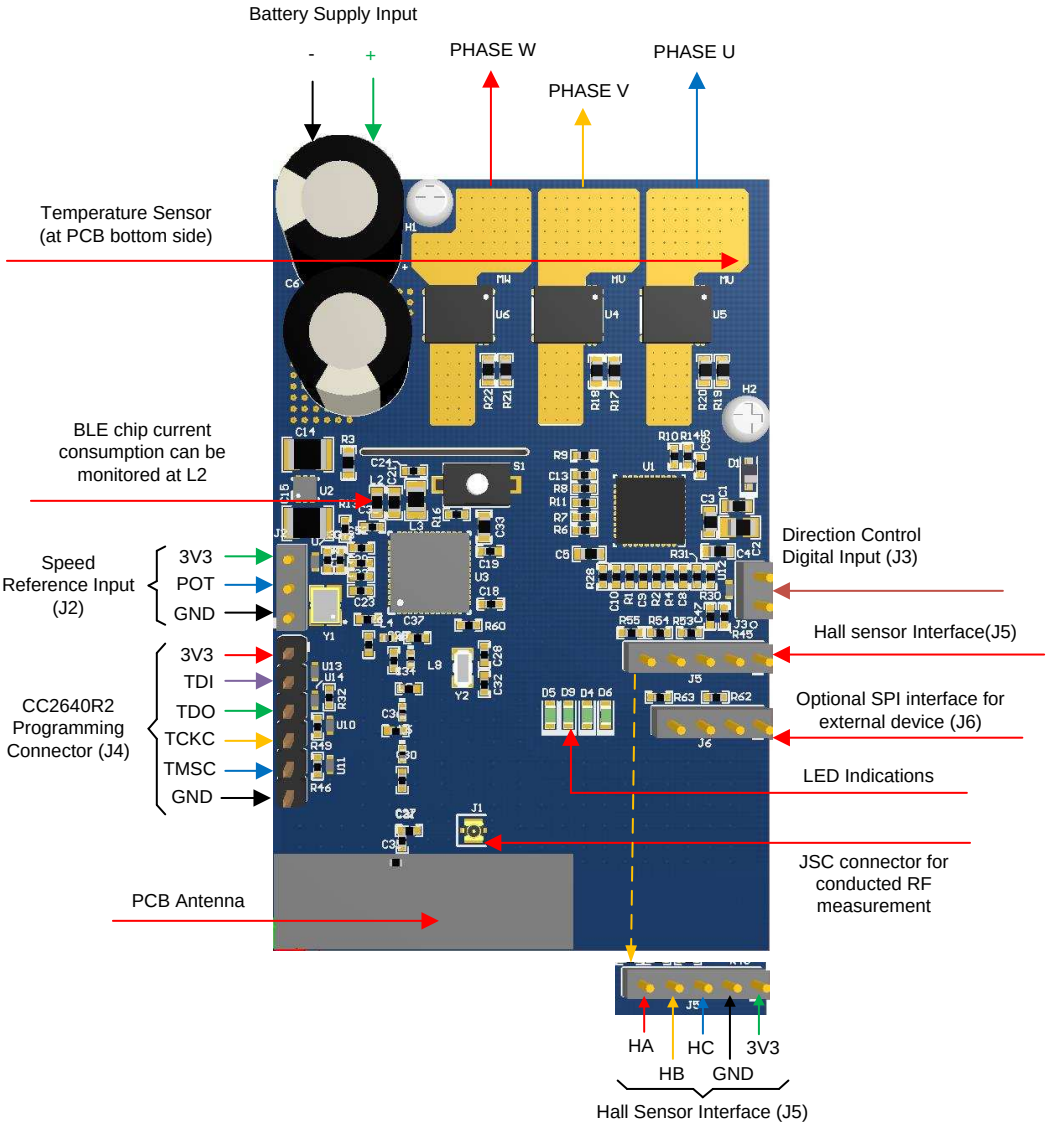


図 15. TIDA-01516 PCB Connectors

3.1.1.2 Programming of CC2640R2F

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface. The reference design uses the two-wire Spy-Bi-Wire protocol to program the CC2640R2F MCU. 図 16 shows the interface in the reference design board.

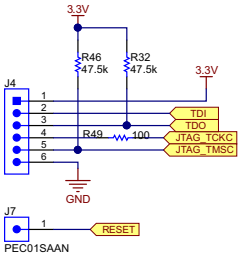


図 16. Schematic of CC2640R2F Programming Connector

See the CC-DEBUGGER product page for the programming options with an external JTAG interface.

The following list outlines the steps to program the CC2640R2 MCU when the programming supply voltage is provided by the board itself:

1. Remove the motor connections from the board and power on the input DC supply. Make sure that a minimum of a 6-V DC input is applied and 3.3 V is generated in the board.
2. Connect the programmer to the board.
3. Open the CCS software and then build and debug the code to program the MCU.

3.1.1.3 Procedure for Board Bring-up and Testing

The following list details the procedure for board bring-up and testing:

1. Remove the motor connections from the board and power on the input DC supply. Make sure that a minimum of a 6-V DC input is applied and the 3.3 V is generated in the board.
2. Program the MCU as detailed in 3.1.1.2.
3. Remove the programmer, and switch off the DC input supply.
4. Connect the inverter output to the motor winding terminals. Connect the position Hall sensor inputs to the connector J5, and make sure that the winding connection and Hall sensor connections match.
5. Connect the POT at the interface J2 and set the speed reference.
6. Use a DC power supply with current limit protection and apply 8-V DC to the board. If the Hall sensors and winding are connected properly in the matching sequence, then the motor starts running at a speed set by the POT.
7. If the motor is not rotating and takes high current or rotates and draw distorted peak winding current waveform (proper waveform shape is as shown in 図 26), then check the winding and Hall sensor connection matching. If wrong, correct it.
8. Adjust the POT voltage for change in speed.
9. To change direction, switch off the DC input, close the jumper J3, and switch on the DC input.

3.1.2 Firmware

3.1.2.1 High-Level Description of Application Firmware

The firmware of this reference design runs on Bluetooth low energy 5.0 stack. The firmware also configures the DRV8323 over SPI and execute BLDC motor trapezoidal control by configuring the PWMs and ADCs.

表 3 lists the system components for the firmware of this reference design .

表 3. TIDA-01516 Firmware System Components

SYSTEM COMPONENT	DESCRIPTION
Development and emulation	Code Composer Studio™ (CCS) v7.2
Target controller	CC2640R2F
RF measurement platform	SmartRF™ Studio
PWM frequency	20-kHz PWM (default), programmable for higher and lower frequencies
PWM generation—timer configuration	TIMER clock = 48 MHz Mode: PWM duty cycle is defined in TIMER counts
Bluetooth low energy RF configuration	Differential RF with internal bias
ADC channel assignment	DIO23 → Low-side DC bus current sensing DIO24 → PCB or FET temperature feedback DIO25 → Speed reference from the external potentiometer DIO26 → DC bus voltage sensing
DRV8323—SPI programming pins connection	DIO8 → SDI DIO9 → SDO DIO10 → SCLK DIO11 → SCS
DRV8323—Digital inputs and outputs	DIO6 → PWM DIO7 → Direction Input DIO12 → BRAKE DIO13 → EN_GATE (ENABLE for DRV8323) DIO14 → FAULT DIO21 → CAL (Calibration for DRV8323 amplifier)
MCU digital inputs and outputs	DIO4 → Direction of motor rotation, DIO0 and DIO1 → LED

3.1.2.2 Prerequisites for Developing and Running the TIDA-01516_Firmware_1.0 Application

This reference design board can work as a stand-alone board once the MCU firmware is flashed and downloaded to the onboard CC2640R2F MCU. To develop and debug the firmware using TI's CCS Integrated Development Environment (IDE), an XDS emulator is needed for emulating JTAG and UART lines over USB. 図 17 shows the hardware interconnections needed between the design board and the LaunchPad™ (using as an XDS emulator) for flashing the code in this reference design.

A potentiometer can be used to control the speed of the motor. Also, a Bluetooth-enabled phone (with a Bluetooth low energy scanner application) is required to interact with the reference design over Bluetooth low energy.

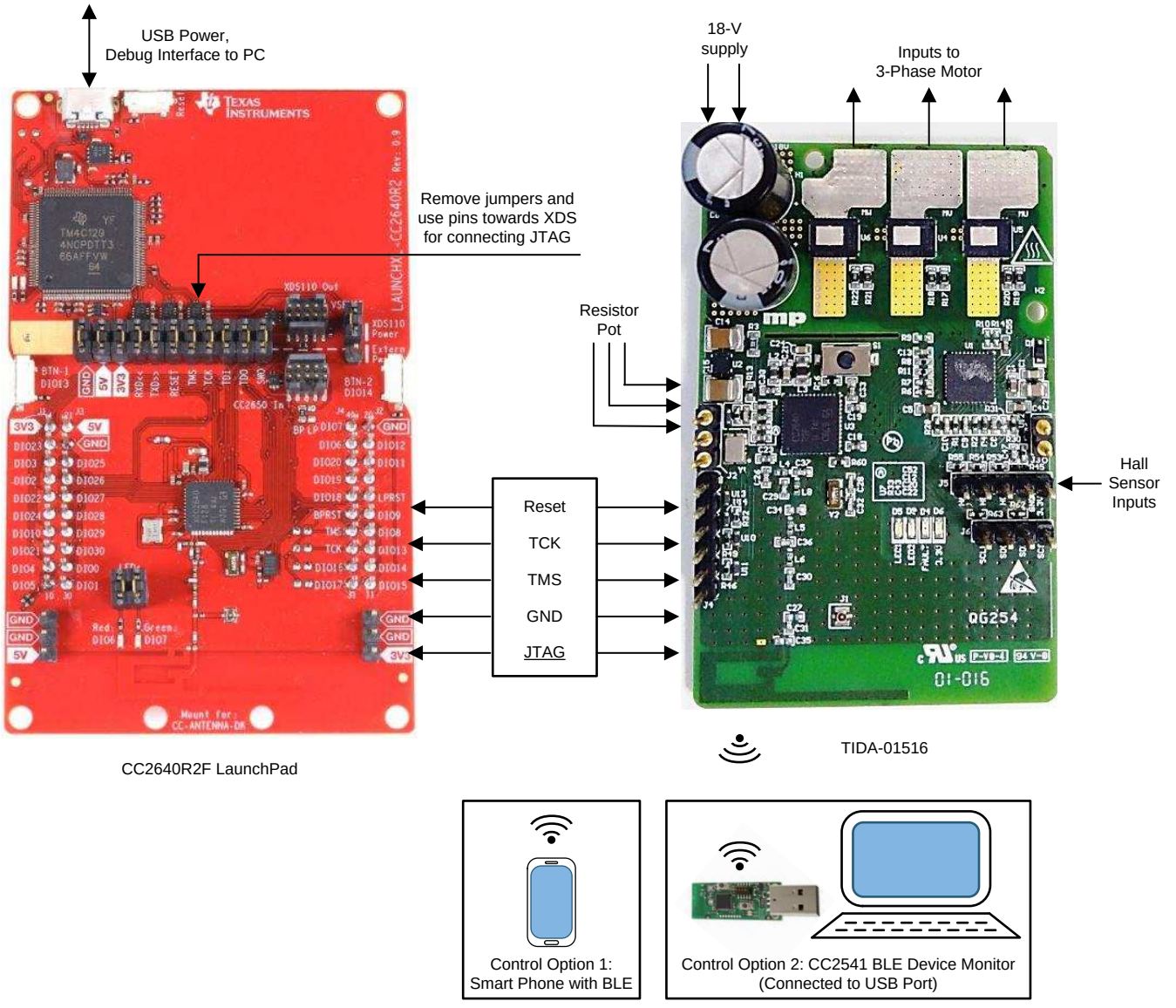


図 17. TIDA-01516 Interfacing With XDS Emulator and External Bluetooth Devices

Ensure the following prerequisites are downloaded and installed:

- CCS Version 7.20.00013 or above
- SIMPLELINK-CC2640R2-SDK_1_35_00_33

注: The application firmware for this reference design is developed using the mentioned SDK version. Check if later versions are available. Porting the application firmware to the new SDK version might require some changes. The "simple_peripheral" application in the SDK examples is used as a starting point for developing the firmware application for this design. 3.1.2.3 to 3.1.2.5 detail the required steps.

3.1.2.3 Porting the simple_peripheral Application

To port and run the "simple_peripheral" application on this reference design, remap the peripheral pins as per the schematics of the design by following these steps:

1. Duplicate the "CC2640R2_LAUNCHXL" directory in the following path:

   <SDK_INSTALL_DIR>\source\ti\ble5stack\boards\CC2640R2_LAUNCHXL

   Give it a unique, meaningful name for the development platform. In this example, call it "CC2640R2_MYBOARD".
2. In the :CC2640R2_MYBOARD" folder, replace the existing files with example files of CC2640R2_MYBOARD.c, CC2640R2_MYBOARD.h, and Board.h. These files are available in the TIDA-01516_Firmware_V1.0 zip package downloadable from the TIDA-01516 product page.
3. Modify the board.c and board.h files in <SDK_INSTALL_DIR>\source\ti\ble5stack\target:
   a. In board.h, add the following lines before "#else" statement:

      #elif defined(CC2640R2_MYBOARD)

      #include "./../boards/CC2640R2_MYBOARD/Board.h"
   b. In board.c, add the following lines before "#else" statement:

      #elif defined(CC2640R2_MYBOARD)

      #include "./../boards/CC2640R2_MYBOARD/Board.h"

      #include "./../boards/CC2640R2_MYBOARD/ CC2640R2_MYBOARD.c"

3.1.2.4 Building and Running the Ported simple_peripheral Application

- Import the "simple_peripheral" application from the SDK. This step also automatically imports the "simple_peripheral_stack_library" to the IDE. As a first step, build the stack_library by right clicking on the project in the project explorer and selecting "Build Project".
- Replace "CC2640R2_LAUNCHXL" with "CC2640R2_MYBOARD" in the project's application predefined symbols (see <SDK_INSTALL_DIR>\docs\ble5stack\ble_user_guide\html\cc2640\developing_in_ccs.html or <SDK_INSTALL_DIR>\docs\ble5stack\ble_user_guide\html\cc2640\developing_in_iar.html)
- Build and run the application. The device goes into advertising mode and can be connected to and controlled using the "BLE Scanner" application on the mobile phone. For detailed information on "simple_peripheral" application, refer to the "README.html" in the following path in the SDK:

  <SDK_INSTALL_DIR>\examples\rtos\CC2640R2_LAUNCHXL\ble5stack\simple_peripheral\README.html

3.1.2.5 Developing and Running the TIDA-01516_Firmware_V1.0

1. Modify the PWM driver "PWMTimerCC26XX.c" from the SDK to enable application call back on the rising edge of the PWM signal, which can be used to trigger the start of conversion signal for the ADC in the CC2640R2F MCU.

   Replace the contents of the PWMTimerCC26XX.c file in <SDK_INSTALL_DIR>\source\ti\drivers\pwm with the content from TIDA-01516_Firmware_V1.0\PWMTimerCC26XX.c.
2. Right click on the project in CCS IDE, click on "Add Files", select the modified file, which could be either copied or linked.
3. In the CCS IDE workspace, replace the content of the files "main.c", "simple_peripheral.c", "simple_gatt_profile.h", "simple_gatt_profile.c", and "app_ble.cfg" in the CCS project with the content from the same files available in the TIDA-01516_Firmware_V1.0 package.
4. Build and run the application. The device goes into advertising mode and can be connected to and controlled using the Bluetooth low energy scanner application on the mobile phone.

注: For more options and features on the application program, refer to the README_TIDA-01516.html file in the TIDA-01516_Firmware_V1.0 zip package.

3.2 Testing and Results

3.2.1 Functional Tests

3.2.1.1 3.3-V Power Supply Generated by LDO

図 18 shows the 3.3 V generated from the LDO and the ripple in the 3.3-V rail during the 100-ms, three-channel advertisement mode in the CC2640R2F MCU.

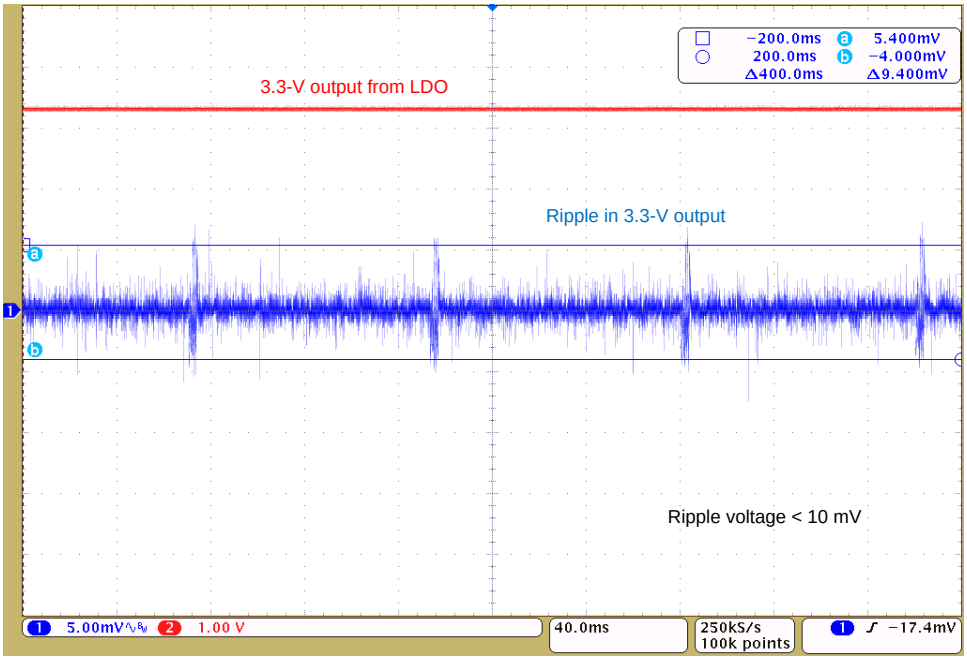


図 18. Output Voltage of 3.3 V From LDO and 3.3-V Voltage Ripple

3.2.1.2 PWM Generated by Gate Driver in Single PWM Mode

図 19 shows PWM generated by the DRV8323 in single PWM mode. The gate driver is configured for active freewheeling mode.

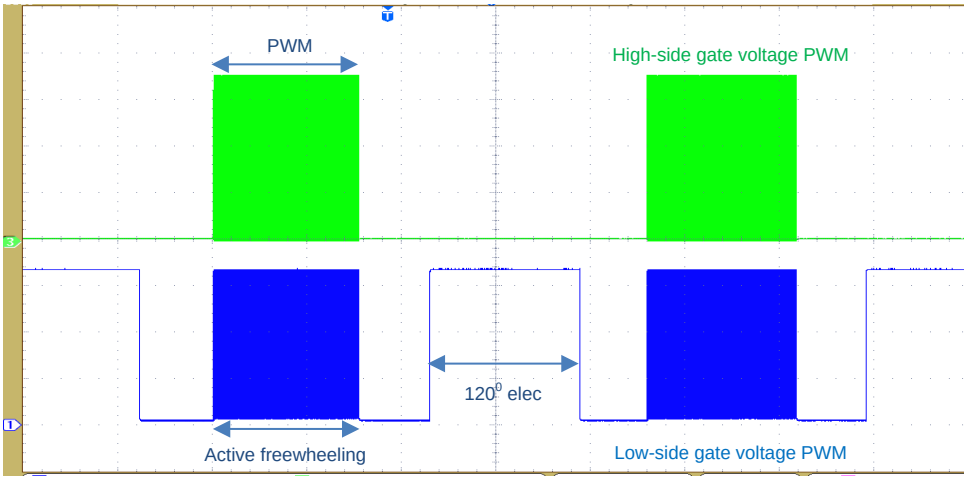


図 19. Low- and High-Side FET Gate Voltage Generated by Gate Driver for Trapezoidal Control

3.2.1.3 MOSFET Switching Waveforms

図 20 to 図 23 show the V_{DS} and V_{GS} waveforms of the low-side and high-side MOSFETs at a gate current of the DRV8323 (IDRIVE), which is set at a 190-mA source and 880-mA sink for the high-side FET and a 820-mA source and 880-mA sink for the low-side FET. Switching waveforms are clean without much overvoltage ringing due to the following:

- The power block has both the high-side and low-side switches in same package, which reduces the parasitic inductance and hence reduces the phase node voltage ringing.
- The current controlled gate driver with slew rate control helps to optimize the switching.
- The IDRIVE and TDRIVE features of the gate driver help shape the gate current to optimize the switching.

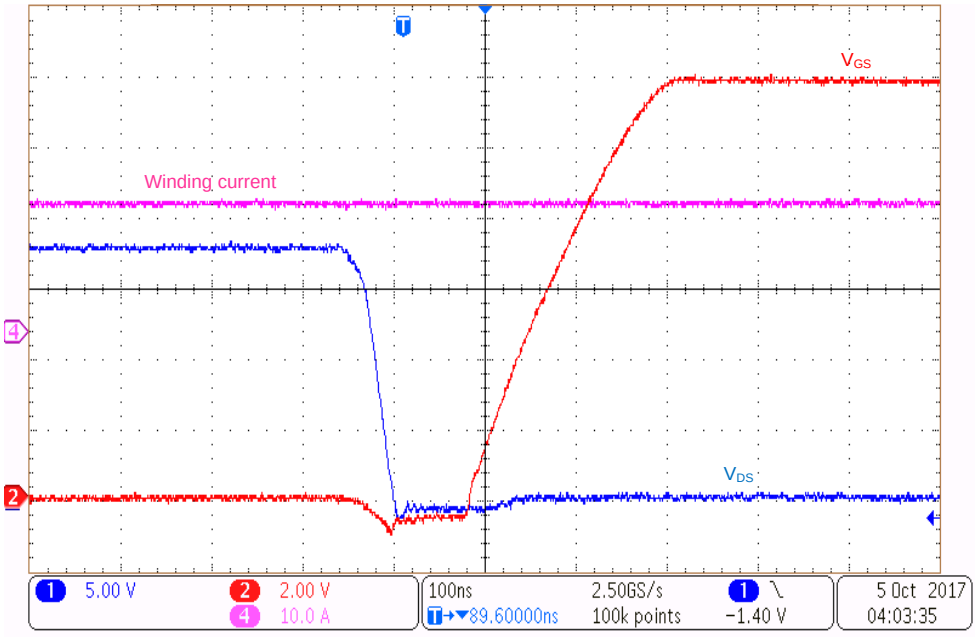


図 20. Turnon—Low-Side V_{GS} and V_{DS} at 20-A Winding Current

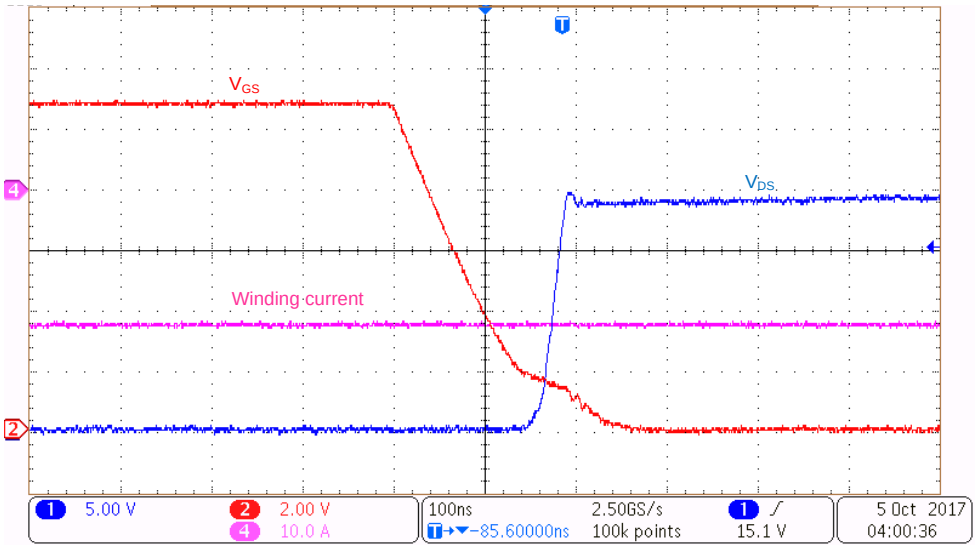


図 21. Turnoff—Low-Side V_{GS} and V_{DS} at 20-A Winding Current

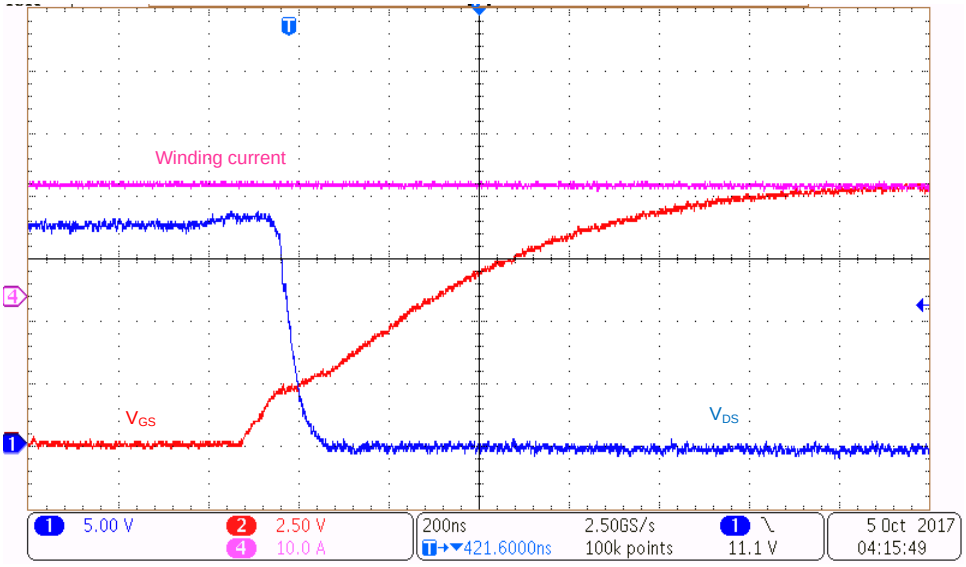


図 22. Turnon—High-Side V_{GS} and V_{DS} at 20-A Winding Current

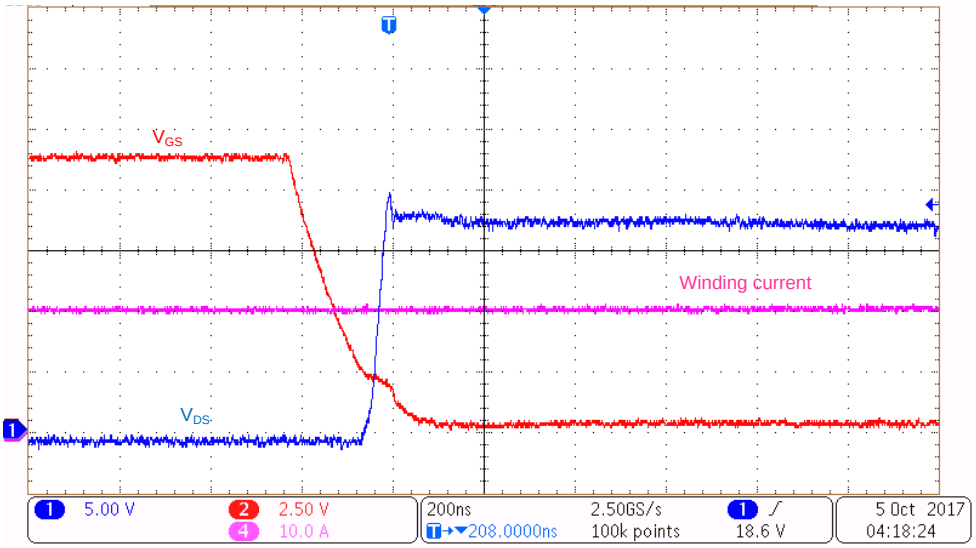


図 23. Turnoff—High-Side V_{GS} and V_{DS} at 20-A Winding Current

3.2.2 Power Stage Load Test

The reference design board is tested with an external BLDC motor and load using the test setup in 図 24.

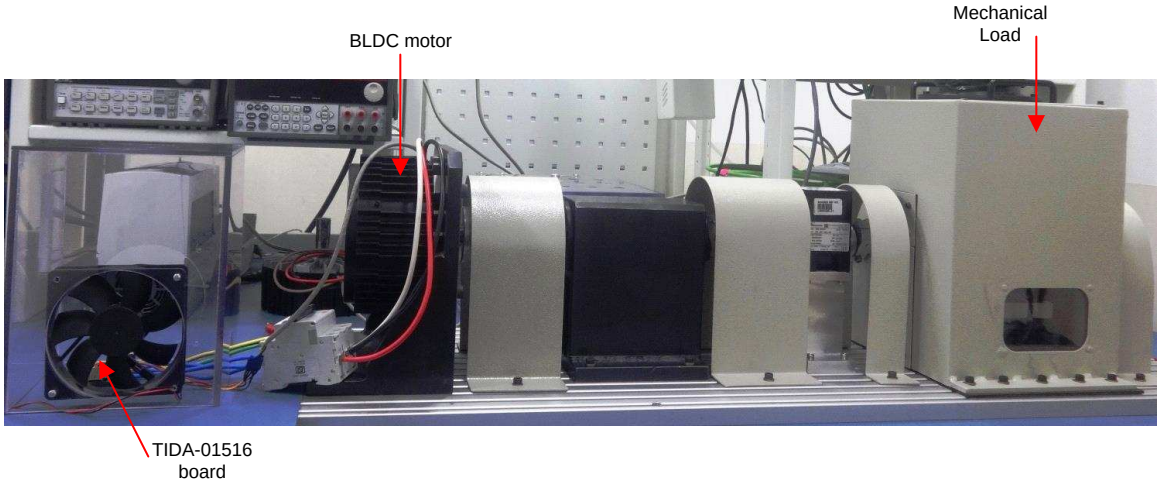


図 24. Motor Load Test Setup in Lab

Testing is done without heat sink and without airflow at different duty cycles. 図 25 shows the motor current and winding voltage waveforms at a 50% duty cycle and 26.4-A_{RMS} current. 図 26 shows the waveforms at a 100% duty cycle and 27-A_{RMS} winding current.

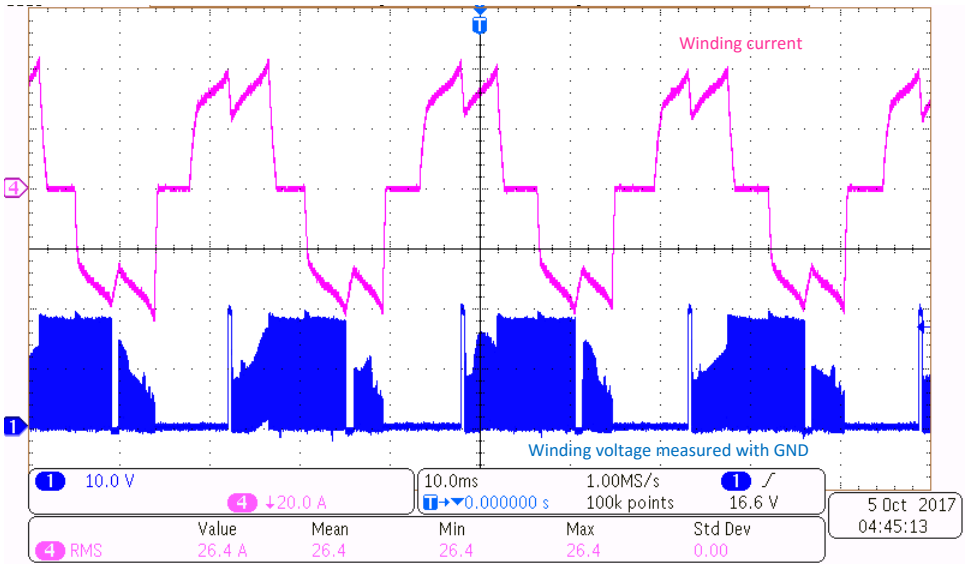


図 25. Motor Waveforms at 18-V DC Input, 26.4-A_{RMS} Winding Current, 50% Duty Cycle

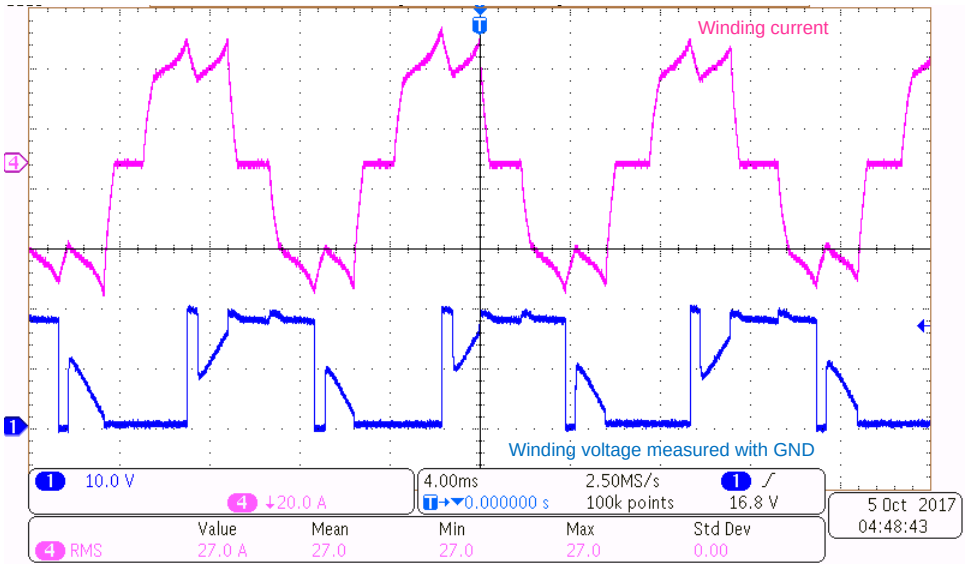


図 26. Motor Waveforms at 18-V DC Input, 27-A_{RMS} Winding Current, 100% Duty Cycle

表 4 shows the load test results at a 25.6-A_{RMS} winding current. Testing is done at 100% duty cycle. 図 27 shows the steady state thermal image of the board at the same condition, captured after 10 minutes of continuous running. The maximum FET temperature observed is 95°C.

表 4. Load Test Results at 100% Duty Cycle Without Heat Sink

VDC (V)	IDC (A)	WINDING CURRENT (RMS) (A)	INPUT POWER (W)	MAXIMUM FET TEMPERATURE (°C)
18	30.4	25.6	547	92

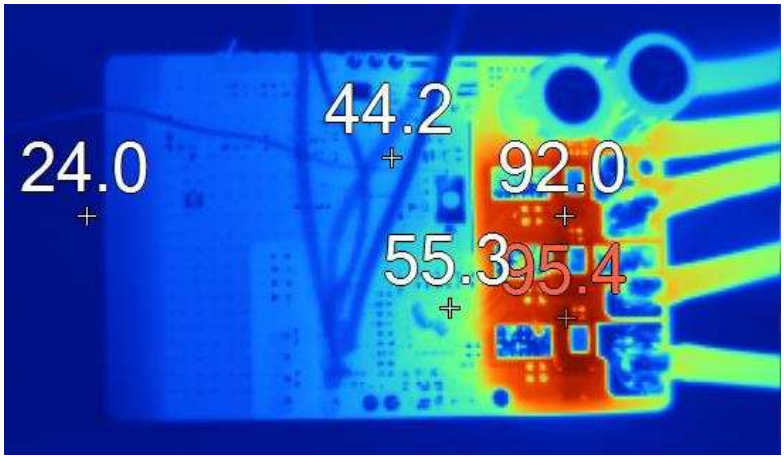


図 27. Thermal Image at 18-V DC Input, 25.6-A_{RMS} Winding Current, 100% Duty Cycle

3.2.3 Cycle-by-Cycle Overcurrent Protection by DRV8323 V_{DS} Monitoring

図 28 shows the cycle-by-cycle peak current limit by the DRV8323, when the motor is loaded more than the set current limit. The test conditions are specified in 表 5.

表 5. Test Condition for Cycle-by-Cycle Overcurrent Protection by DRV8323

PARAMETER	VALUE
Measured MOSFET R_{DS_ON} at 25°C	0.8 mΩ
V_{DS} threshold	0.06 V
DRV8323—TDRIVE	2 µs
Duty cycle Deglitch time (OCP_DEG)	4 µs
DRV8323—TDRIVE overcurrent protection mode (OCP_MODE)	Overcurrent causes an automatic retrying fault

Assuming the junction temperature of 100°C, the R_{DS_ON} at 100°C ≈ 1.136 mΩ (approximately 1.42 times the R_{DS_ON} at 25°C, from *CSD88584Q5DC 40-V Half-Bridge NexFET™ Power Block*):

Current limit threshold = V_{DS} threshold / R_{DS_ON} = 52.8 A

図 28 shows that the current is limited approximately at 35 A. 図 29 shows the zoomed view where the PWM is shuts off during current limit action and a fault signal is generated. The fault reset at the next PWM rising edge.

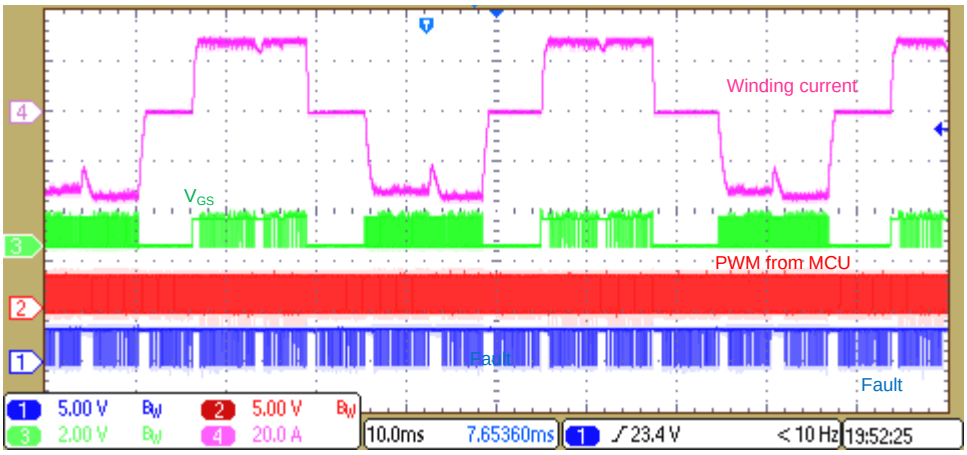


図 28. Cycle-by-Cycle Current Limit by DRV8323

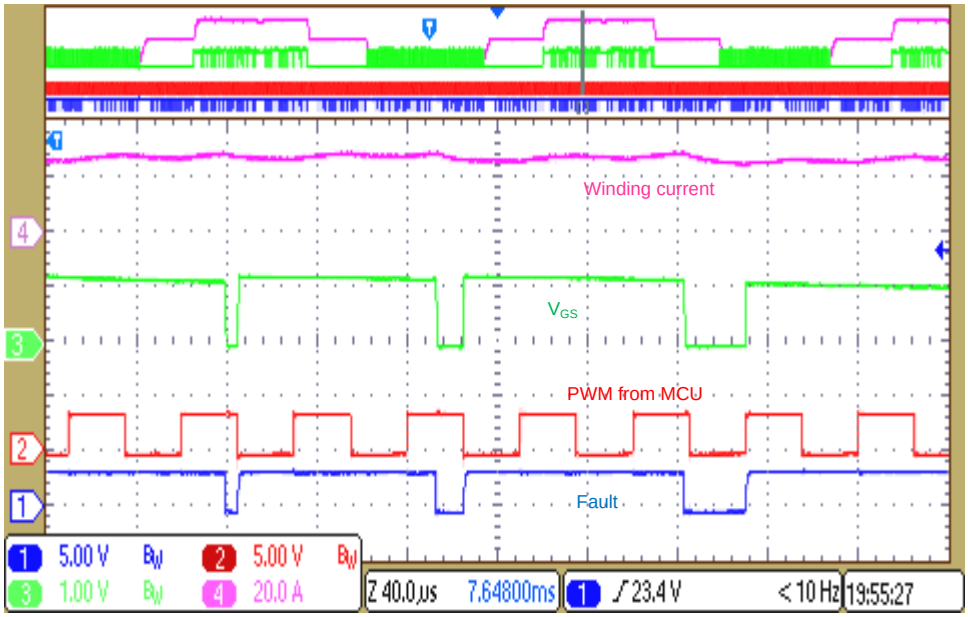


図 29. Cycle-by-Cycle Overcurrent Limit Showing PWM Shutoff

3.2.4 RF Measurements

3.2.4.1 RX Sensitivity Measurement

This test measures the Bluetooth RX sensitivity of this reference design. The test is executed as per the method mentioned in the application note *ETSI EN 300 328 RX Blocking Test for Bluetooth® Low Energy*. The testing is done with and without enabling the gate driver and the motor.

図 30 shows the lab test setup to measure the RX sensitivity. The test is set up for conducted measurements. The PCB antenna in the reference design board is disconnected for testing by removing C31 and connecting C27 so that the JSC connector J1 is available for conducted RF measurements. The reference design board, and XDS emulator are kept inside a shielded box to eliminate the effect of radiation.

The test setup uses the RF signal generator R&S®SMU200A. The Bluetooth low energy packets are emulated using the I_Q waveform, R&S_IQ_BLE_1Mbps_1pkt_70ms_guard.wv, as mentioned in the application note *ETSI EN 300 328 RX Blocking Test for Bluetooth® Low Energy*.

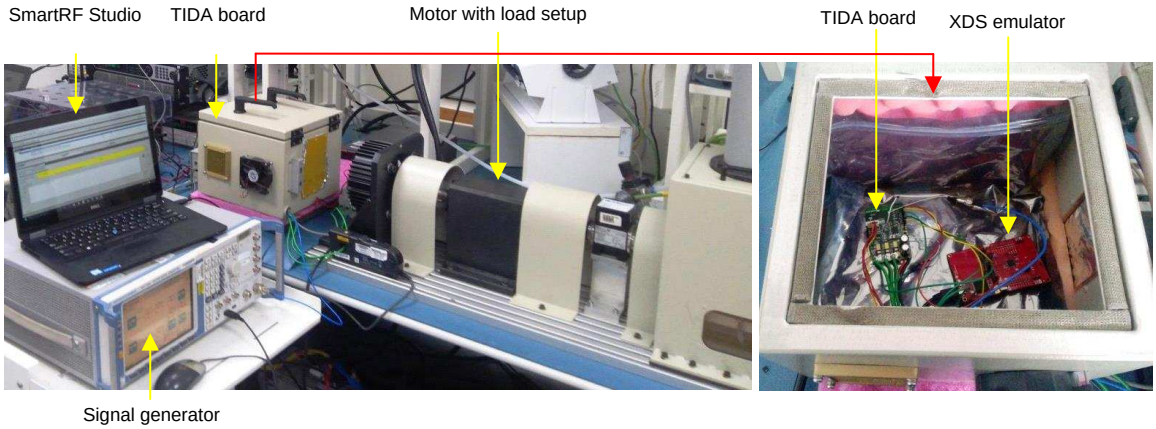


図 30. Test Setup to Measure RX Sensitivity When Motor is Running

To evaluate the performance of the Bluetooth low energy chip and the effect of the motor running, the following test conditions are executed as shown in 図 31 and 図 32.

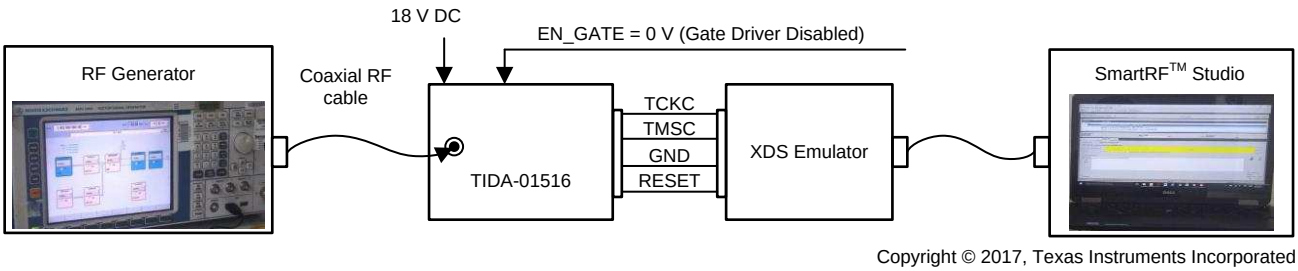


図 31. Test Setup for RX Sensitivity Measurement—Gate Driver Disabled and Motor Not Rotating

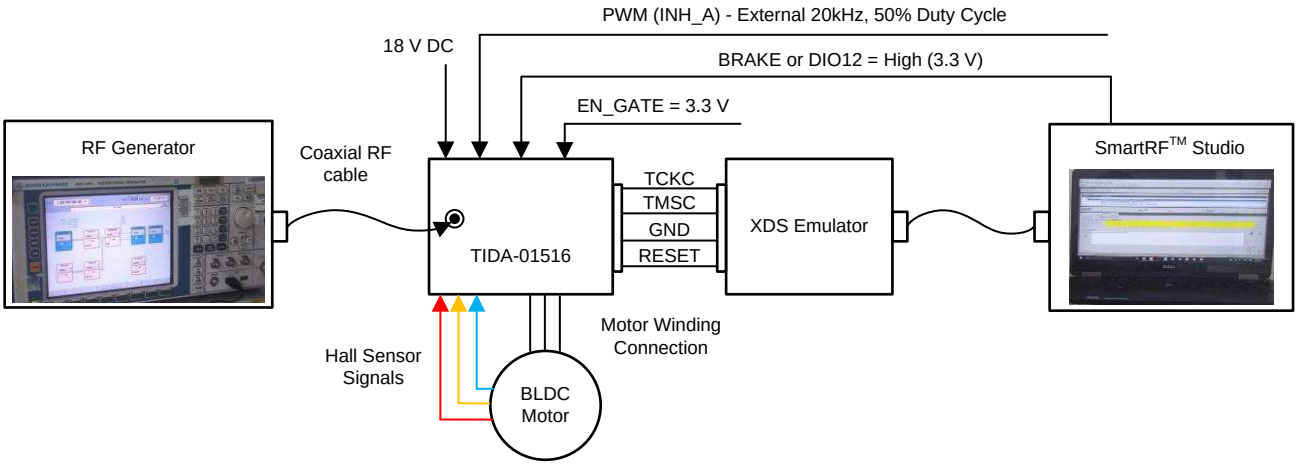


図 32. Test Setup for RX Sensitivity Measurement—Gate Driver Enabled and Motor Rotating at 50% Duty Cycle

The test is performed at three channels (2402 MHz, 2440 MHz, and 2480 MHz). The Bluetooth low energy specification specifies a packet error rate (PER) limit at 30.8% (1038 OK packages out of 1500 packages). Power loss in the cables, coupler, and so on from the signal generator to the reference design in the test setup needs to be measured and compensated for accurate measurement. The cable loss is measured using a spectrum analyzer at different Bluetooth channel test frequencies. The difference between the TX source power from the RF signal generator and the power applied to the TIDA-01516 board is calculated to be 2.4 dB at 2402 MHz, 2.65 dB at 2440 MHz, and 3.1 dB at 2480 MHz; these measurements are used to compensate the results given in 表 6.

表 6. RX Sensitivity Measurement

FREQUENCY (MHz)	PEP (dBm)	LEVEL	GATE DRIVER DISABLED, MOTOR OFF		GATE DRIVER ENABLED, MOTOR ON (4-A CURRENT)		GATE DRIVER ENABLED, MOTOR ON (15-A CURRENT)	
			PACKETS RECEIVED OK	PER (%)	PACKETS RECEIVED OK	PER (%)	PACKETS RECEIVED OK	PER (%)
2440	–90.79	–113.5	1479	1.4	1470	2	1446	3.6
	–91.79	–114.5	1374	8.4	1356	9.6	1329	11.4
	–92.29	–115	1293	13.8	1269	15.4	1248	16.8
	–92.79	–115.5	1110	26	1053	29.8	1032	31.2
	–93.29	–116	948	36.8	870	42	867	42.2
2402	–90.79	–113.5	1470	2	1443	3.8	1437	4.2
	–91.79	–114.5	1395	7	1365	9	1344	10.4
	–92.29	–115	1203	19.8	1170	22	1152	23.2
	–92.79	–115.5	1023	31.8	933	37.8	900	40
	–93.29	–116	753	49.8	690	54	687	54.2
2480	–90.79	–113.5	1461	2.6	1455	3	1455	3
	–91.79	–114.5	1317	12.2	1311	12.6	1305	13
	–92.29	–115	1215	19	1206	19.6	1188	20.8
	–92.79	–115.5	1014	32.4	1005	33	987	34.2
	–93.29	–116	810	46	804	46.4	768	48.8

The RX sensitivity measurements without enabling the motor drive and at different motor load conditions are plotted in 図 33, 図 34, and 図 35 at frequencies of 2480 MHz, 2440 MHz, and 2402 MHz, respectively.

The received signal strength indication (RSSI) is calculated after compensating the cable loss from the observed PEP given in 表 6. Considering a PER limit of 30.8% and after compensating the cable loss, the RSSI with gate driver disabled (motor off) can be read from 図 33 through 図 35 as more than –95.1 dBm at the three frequencies.

The sensitivity levels do not have a noticeable difference when the motor is rotating and when the motor drive part is disabled. The observed maximum difference in RSSI is less than 0.3 dBm across the frequencies with and without enabling the motor drive.

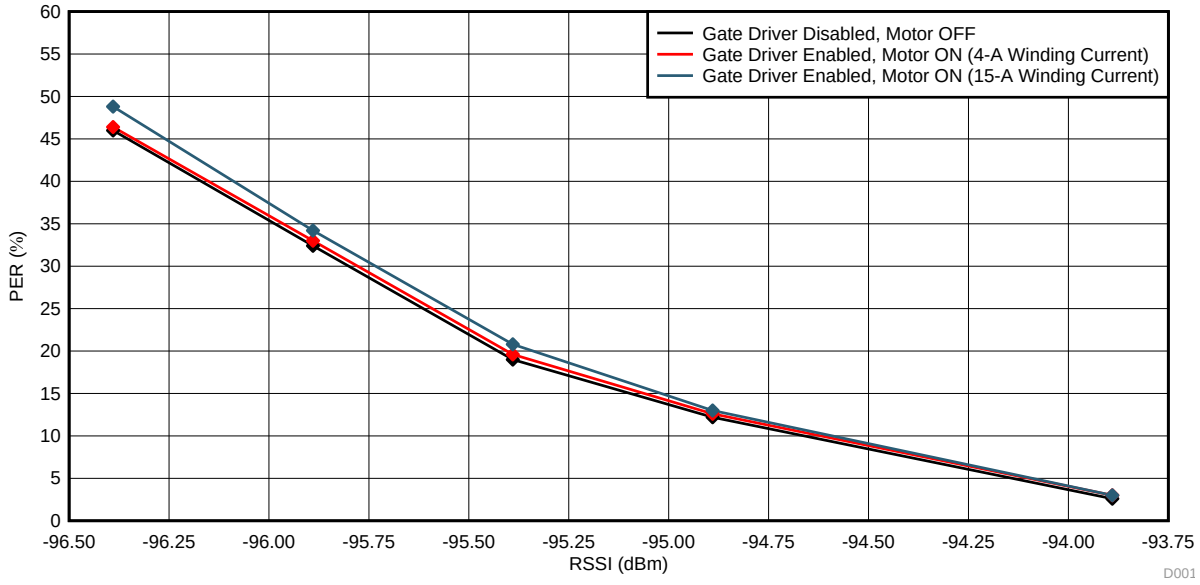


図 33. RX Sensitivity Measurement at 2480 MHz

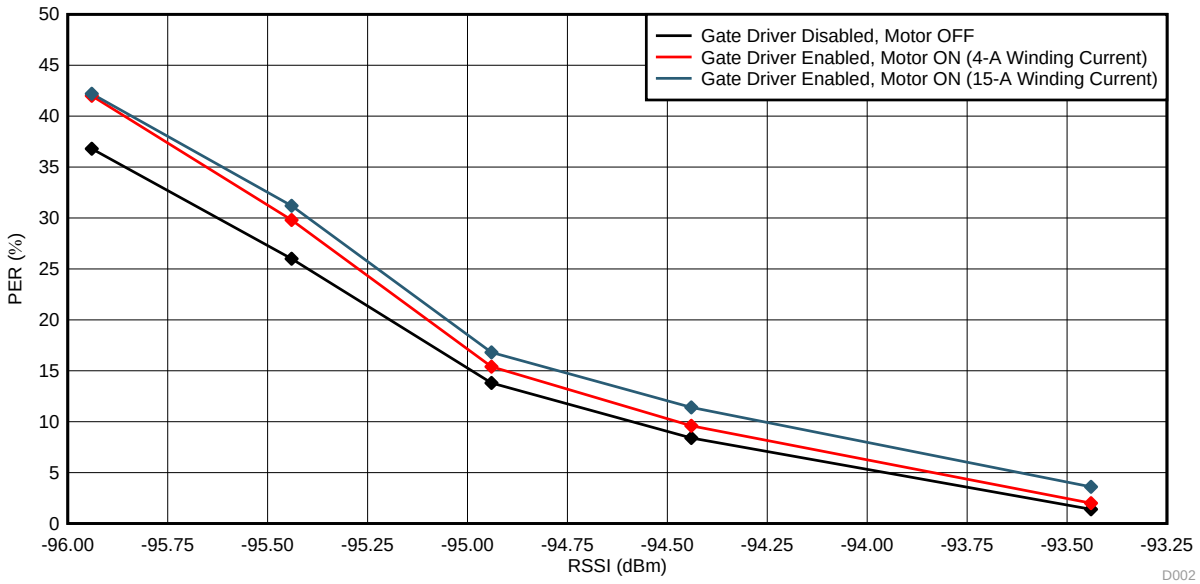


図 34. RX Sensitivity Measurement at 2440 MHz

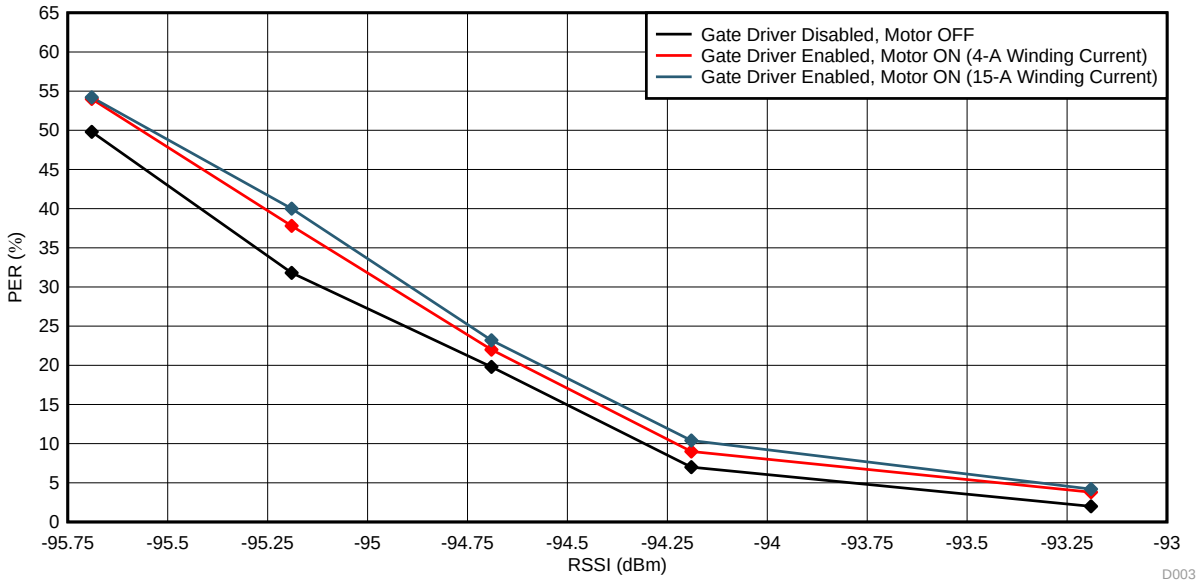


図 35. RX Sensitivity Measurement at 2402 MHz

3.2.4.2 TX Power Measurement

This test verifies that the transmitted output power of the reference design conforms to the standards limit and makes sure that the only minimum loss happens in the impedance matching filters between the CC2640R2 and the antenna. 図 36 shows the test setup used for the measurement.

図 37 shows the experimental setup in the lab to evaluate the performance. The PCB antenna in the reference design board is disconnected for testing by removing C31 and connecting C27 so that the JSC connector J1 is available for conducted RF measurements.

This test uses the spectrum analyzer E4445A Agilent, which has the following settings during measurement, unless otherwise specified:

- Span = 200 MHz
- Resolution bandwidth = 3 kHz

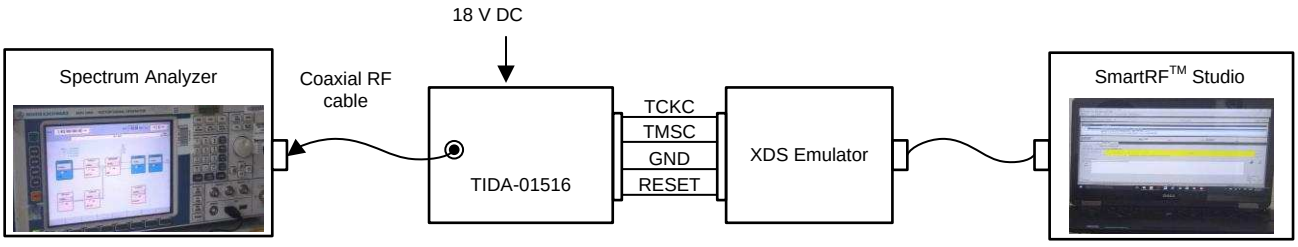


図 36. Test Setup for TX Channel Power Measurement

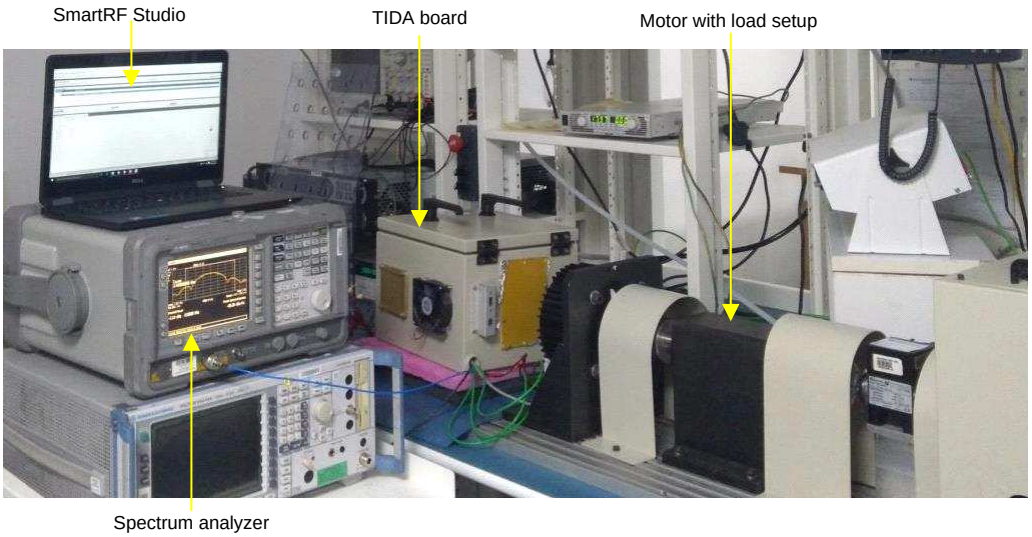


図 37. Lab Test Setup for TX Power Measurement

The SmartRF Studio platform sets the TX power level and Bluetooth channel frequency. For measurement, connect the instruments and the reference design as shown in 図 37. In the SmartRF Studio window, set the EM to modulated, continuous TX mode with the appropriate output power level. Measure the output power level on the spectrum analyzer to confirm the output power programmed on the EM.

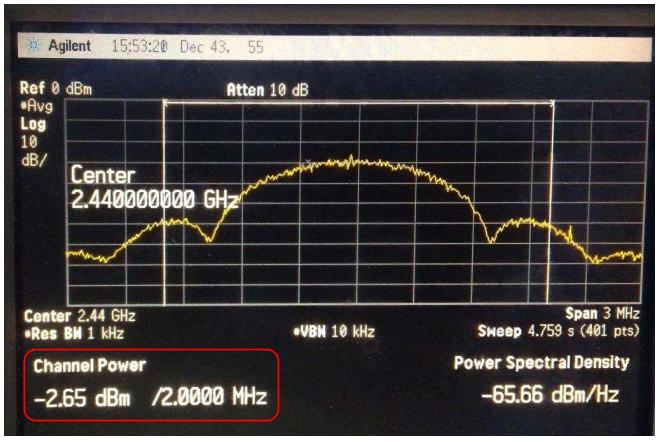


図 38. Measured TX Channel Power Measurement at 2440 MHz, 0-dBm Level

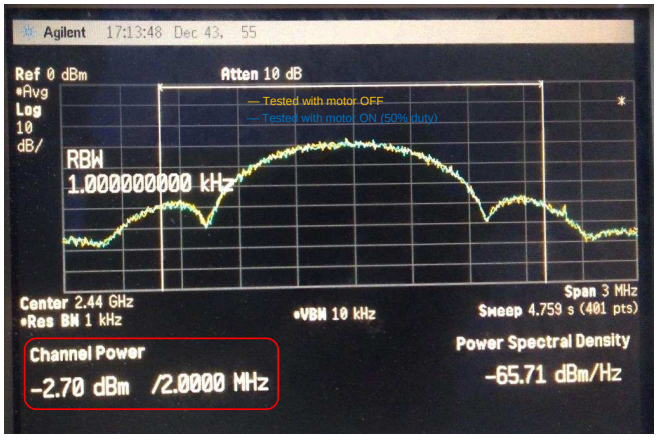


図 39. Measured TX Channel Power Measurement at 2440 MHz, 0-dBm Level With Motor ON and OFF

3.2.4.3 TX Power Measurement to Identify Any Noise Coupling

This test verifies the RF performance with and without the gate driver and motor drive enabled.

The same test setup as shown in 図 37 evaluates performance using conducted measurement. 図 40 and 図 41 shows the test setup to evaluate the TX power measurement with different motor conditions.

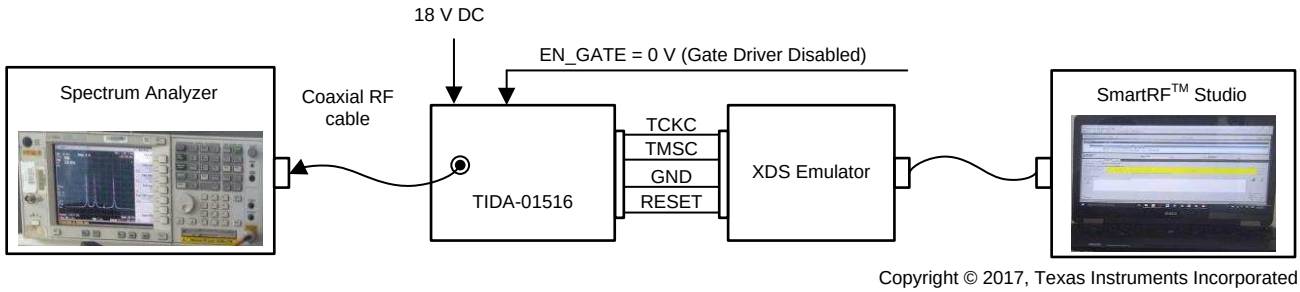


図 40. Test Setup for TX Power Measurement—Gate Driver Disabled and Motor Not Running

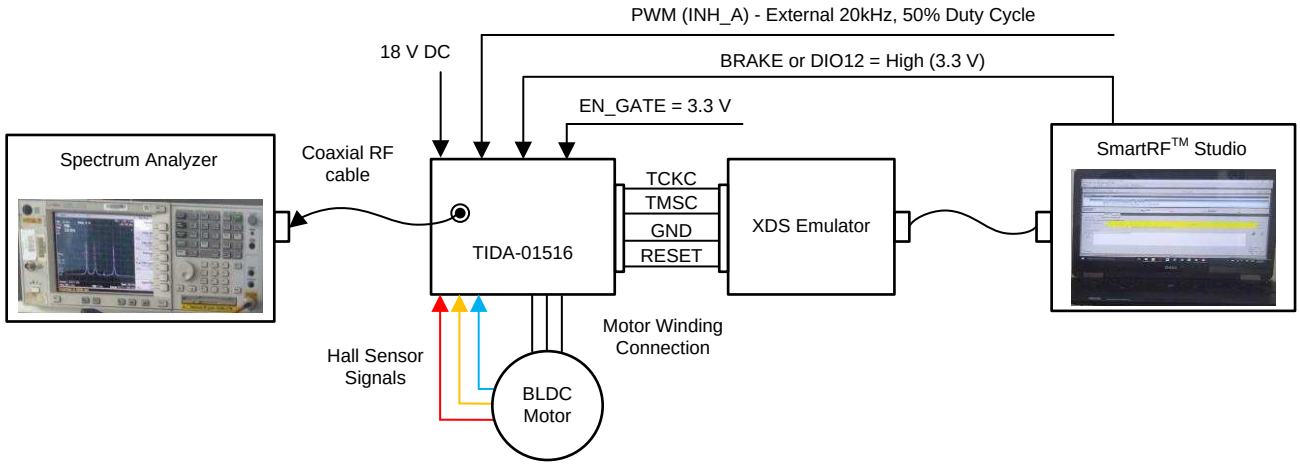


図 41. Test Setup for RX Sensitivity Measurement—Gate Driver Enabled and Motor Rotating at 50% Duty Cycle

The test is performed at the lowest and highest channels (2402 MHz and 2480 MHz). 図 42 shows the TX performance with a Bluetooth channel frequency of 2480 MHz. The noise floor is at –107.7 dBm. The blue plot corresponds to TX performance tested with the gate driver disabled and the motor drive off. The yellow plot corresponds to TX performance tested with the gate driver enabled and the motor rotating at a 100% duty cycle.

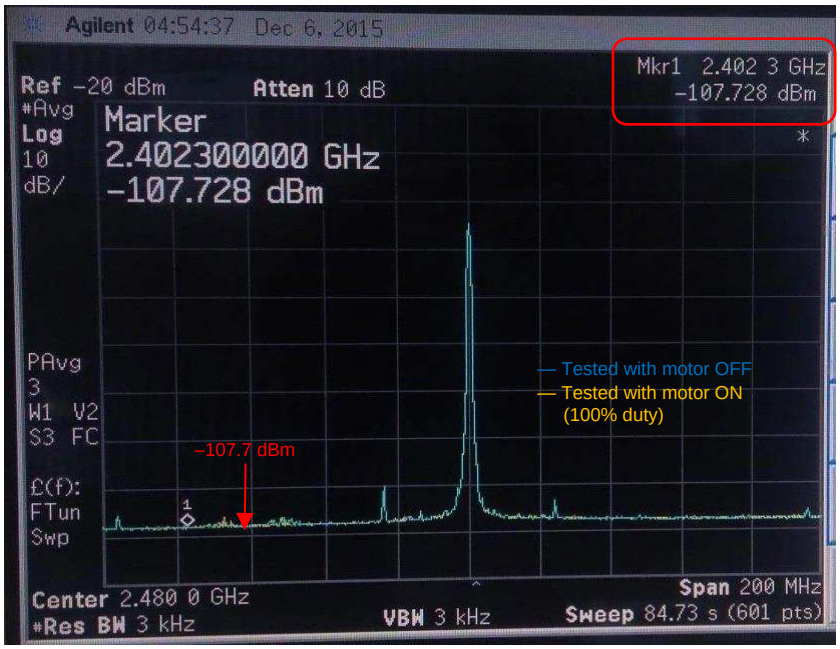


図 42. TX Performance With Bluetooth Channel Frequency of 2480 MHz

図 43 shows the TX performance with a Bluetooth channel frequency of 2402 MHz. The noise floor is at –107.8 dBm. The blue plot corresponds to TX performance tested with the gate driver disabled and the motor drive off. The yellow plot corresponds to TX performance tested with the gate driver enabled and the motor rotating at a 100% duty cycle.

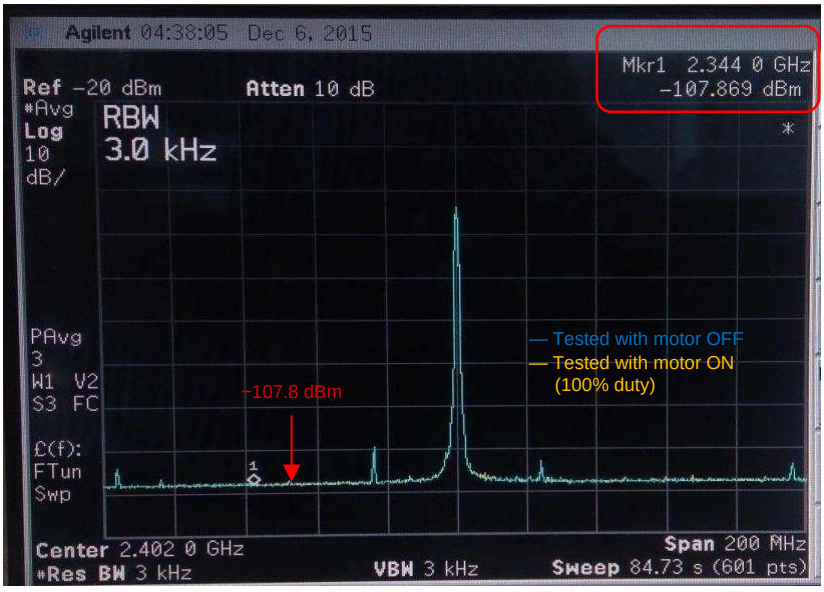


図 43. TX Performance With Bluetooth Channel Frequency of 2402 MHz

The TX performance is evaluated in the Bluetooth low energy advertising mode as well. 図 44 shows the test setup, and the performance is evaluated using the spectrum analyzer in the conducted mode.

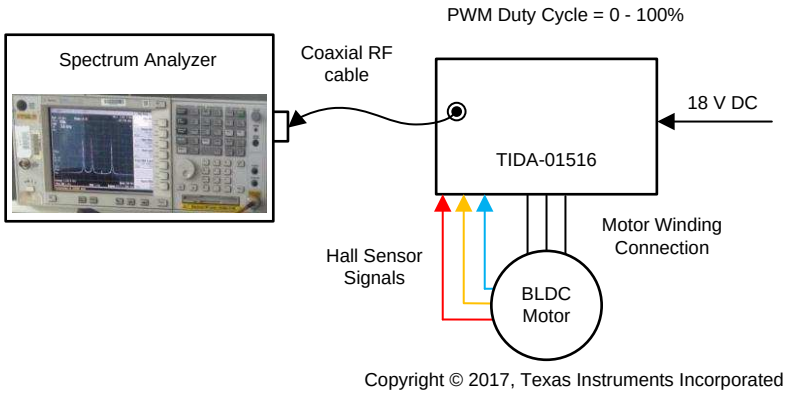


図 44. Test Setup to Evaluate TX Performance in Advertising Mode

図 45 shows the TX performance in the three-channel advertising mode. The noise floor is at –107.5dBm. The blue plot corresponds to TX performance tested with the gate driver disabled and the motor drive off. The other plot corresponds to TX performance tested with the gate driver enabled and the motor rotating at a 80% duty cycle.

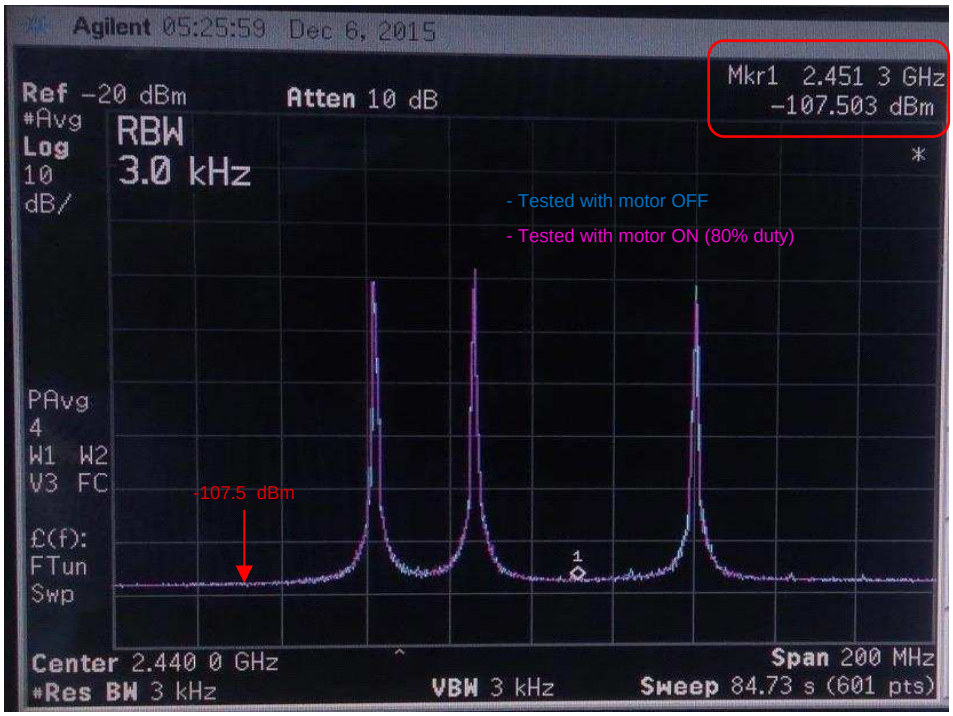


図 45. TX Performance With CC2640R2F in Advertising Mode

The performance with and without enabling the motor drive coincides exactly in every test condition, which means the Bluetooth low energy performance is not affected by the motor drive. The spurious emissions in the spectrum is mainly coming from the 24-MHz clock and is well within the limit of Bluetooth low energy spectrum standards.

3.2.4.4 Bluetooth low energy Power Measurement

To measure the current consumption of the Bluetooth low energy chip, L2 in the reference design board is replaced by a 10-Ω resistance and the voltage drop across 10 Ω is measured. 図 46 shows the hardware change to measure the current consumption by the Bluetooth low energy chip in this reference design.

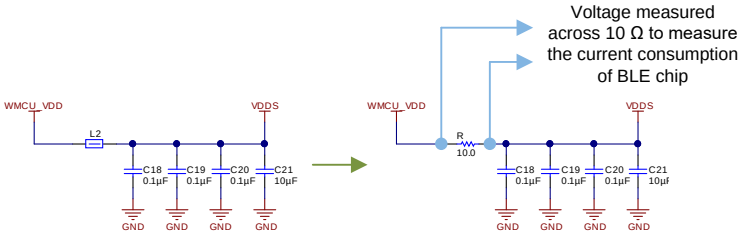


図 46. Using 10-Ω Resistor in Place of L2 to Measure BLE Chip Current Consumption

This measurement uses the following equipment:

- A 6½ digit multimeter measures the average current consumption of the Bluetooth low energy chip by observing the voltage drop across the 10-Ω resistor.
- A 100-MHz oscilloscope measures the current consumption of the Bluetooth low energy chip during the Bluetooth low energy advertising and connection mode.

3.2.4.4.1 Bluetooth low energy Chip Current Measurement—Gate Driver Enabled, Motor Running

The current consumption by the CC2640R2F is measured when the gate driver is enabled and the motor is running. The CC2640 executes the Bluetooth low energy connectivity application, gives the PWM signal to the DRV8323 gate driver, and controls a couple of GPIOs. The Bluetooth low energy chip is in the active mode where the Cortex-M3 CPU is executing code. Active mode provides a normal operation of the processor and all of the peripherals that are currently enabled.

図 47 shows the current consumption when the motor is running and Bluetooth low energy in three-channel advertising mode with a 100-ms duration. The TX power is set to 0 dBm. The average current consumption is found at 3.52 mA.

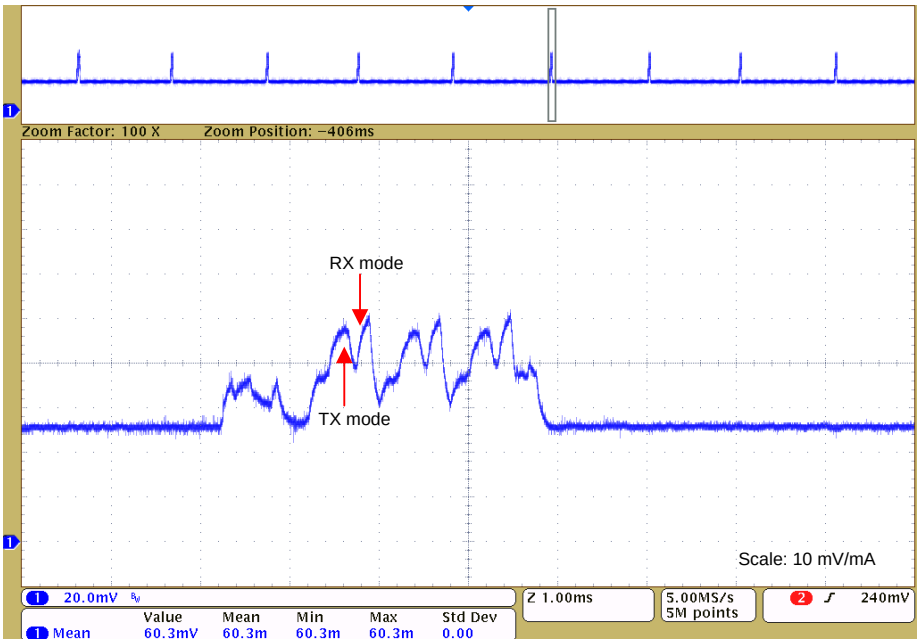


図 47. Bluetooth low energy Chip Current Consumption: Three-Channel 100-ms Interval Advertising Mode When Motor is Running

図 48 shows the current consumption when the motor is running and Bluetooth low energy chip is in connection mode with 1-s connection intervals. The TX power is set to 0 dBm. The average power consumption is found at 3.42 mA.

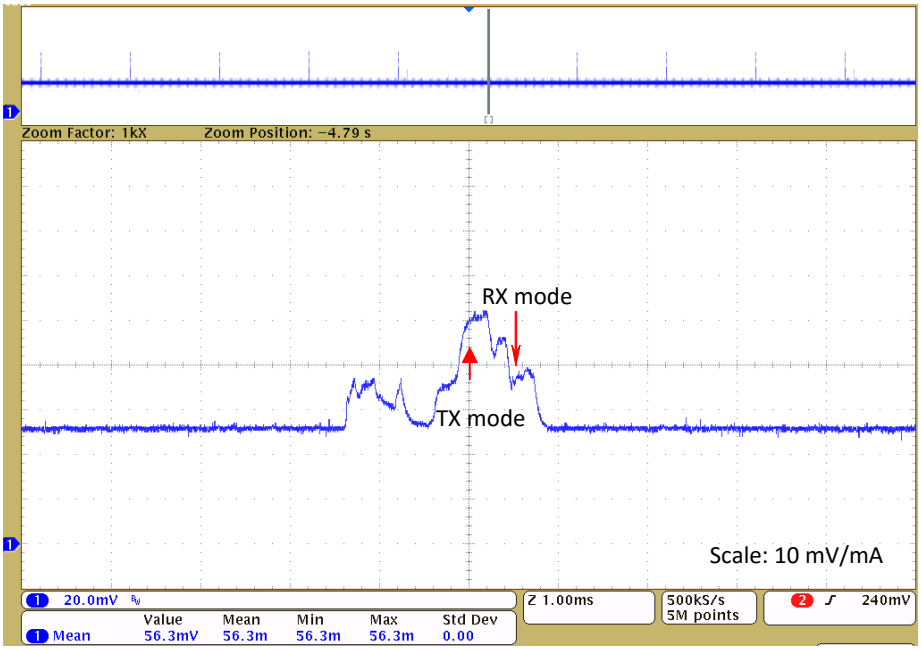


図 48. Bluetooth low energy Chip Current Consumption: 1-s Interval Connection Mode When Motor is Running

3.2.4.4.2 Bluetooth low energy Chip Current Measurement—Gate Driver Disabled, BLE Only Mode

This test measures the power consumption when the Bluetooth low energy chip is executing only the Bluetooth low energy connectivity application. The testing is done by executing only the Bluetooth low energy stack. All the peripherals of the CC2640R2F are in high impedance or low power mode.

注: For more details on the accurate RF power measurement, refer to *Measuring Bluetooth Low Energy Power Consumption*.

図 49 and 図 50 show the test results with advertising and connection modes, respectively.

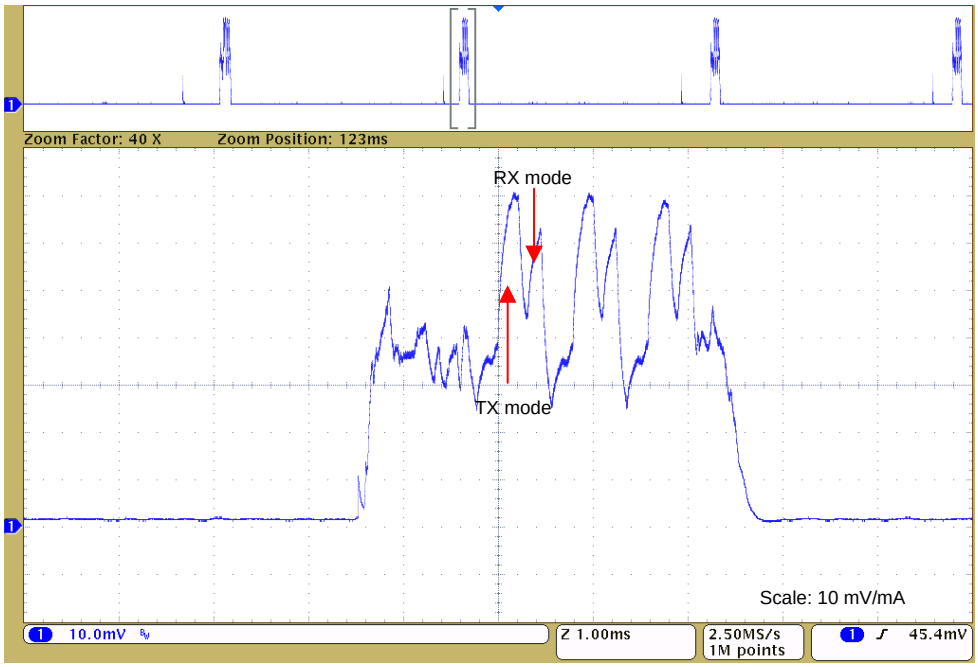


図 49. Bluetooth low energy Chip Current Consumption: Three-Channel, 100-ms Interval Advertising, BLE Only Mode

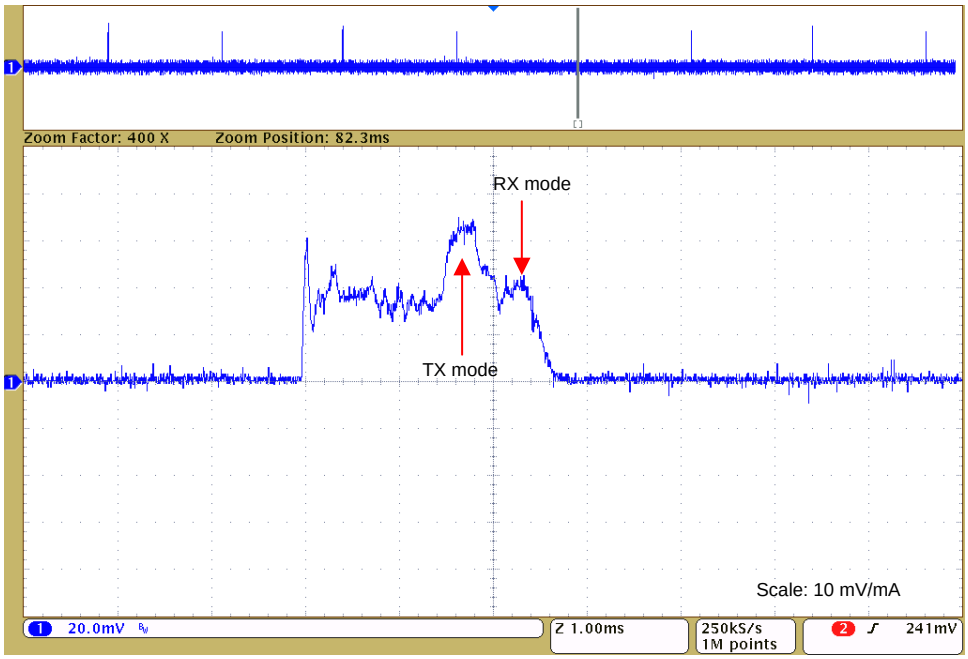


図 50. Bluetooth low energy Chip Current Consumption: 1-s Interval Connection Mode, BLE Only Mode

The 1-s interval connection mode current consumption is less than 10 µA.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01516.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01516.

4.3 PCB Layout Recommendations

Use the following layout recommendations when designing the Bluetooth low energy section of the PCB.

- Do not mix up the GND plane of the Bluetooth low energy chip with the gate driver and the power GND. Define a separate GND plane for the Bluetooth low energy chip and join with the power supply GND at one stable point as done in this reference design.
- Ensure that the substrate height (thickness of the dielectric layer between the layout pattern and the underlying ground plane) corresponds to the reference design being copied. Make sure that the layer stack-up is done to achieve a 50-Ω impedance on the RF lines.
- Ensure that the layout of the RF components closely follows the reference design.
- All RF components connected to ground must have multiple ground vias close to their ground pads to minimize ground impedance.
- Ensure there is an uninterrupted and solid ground plane under all the RF components, stretching from the antenna and all the way back to the ground vias. There must not be any traces under the RF path.
- Place the balun and RF filter as close to the CC2640R2F as possible.
- Place the antenna matching components as close to the antenna as possible.
- Place decoupling capacitors as close to the respective VDD pins as possible. It is also important that the ground return path from the decoupling caps and back to the CC2640R2F is as short and direct as possible.
- Place the DC/DC components (10-µH inductor and 10-µF capacitor) close to the DCDC_SW pin. Equally important is the ground connection from the DC/DC capacitor to the CC2640R2F ground. This connection must be as short and direct as possible to avoid ground switching noise.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01516.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01516.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01516.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01516.

5 Software Files

To download the software files, see the design files at TIDA-01516.

6 Related Documentation

1. Texas Instruments, *Understanding IDRIVE and TDRIVE in TI Motor Gate Drivers Application Report*
2. Texas Instruments, *Sensored 3-Phase BLDC Motor Control Using MSP430™ Application Report*
3. Texas Instruments, *ETSI EN 300 328 RX Blocking Test for Bluetooth® Low Energy Application Report*
4. Texas Instruments, *Measuring Bluetooth Low Energy Power Consumption Application Report*
5. Texas Instruments, *Crystal Oscillator and Crystal Selection for the CC26xx and CC13xx Family of Wireless MCUs Application Report*

6.1 商標

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7 Terminology

BER— Bit error rate

BLDC— Brushless DC motor

BLE— Bluetooth low energy

ESD— Electrostatic discharge

FETs, MOSFETs—Metal-oxide-semiconductor field-effect transistor

MCU— Microcontroller unit

PEP— Peak envelop power

PER— Packet error rate

PSRR— Power supply rejection ratio

PWM— Pulse width modulation

RF— Radio frequency

RMS— Root mean square

RSSI— Received signal strength indication

SPI— Serial peripheral interface

8 About the Authors

MANOJA VINNAKOTA is a lead firmware engineer at Texas Instruments, where she is responsible for system design and ROM development for PHY layer of Wi-Fi® devices targeted towards Internet of Things (IoT) applications. She also has experience in developing and testing middleware for IoT applications. She has a master of technology in telecommunication systems engineering from Indian Institute of Technology Kharagpur, India, and has a bachelor of engineering in electronics and communications engineering from Andhra University College of Engineering, India.

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TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

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