参考資料

TI Designs: TIDA-01503
20W、100～425V DC、85%効率、マルチ出力補助電源のリファレンス・デザイン

概要

この20W、マルチ出力の補助電源のリファレンス・デザインは、広い入力電圧範囲(100～425V DC)のAC/DC産業用電源をサポートします。このデザインは、TIのUCC28704フライバック・コントローラの不連続導通モード(DCM)バレー・スイッチングと、1次側レギュレーションを使用して、85%のピーク効率を実現しています。小型の設計で、部品数が最小限であり、システムを出力過電流や出力短絡などから保護するために役立ちます。ハードウェアは、外部EMIフィルタを使用して、伝導EMI規格EN55022 Class Aを満たすことをテスト済みです。

リソース

TIDA-01503	デザイン・フォルダ
UCC28704	プロダクト・フォルダ

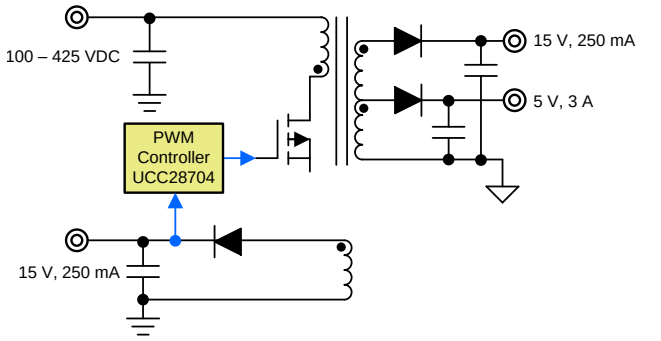
TI E2E™ Community　E2E™エキスパートに質問

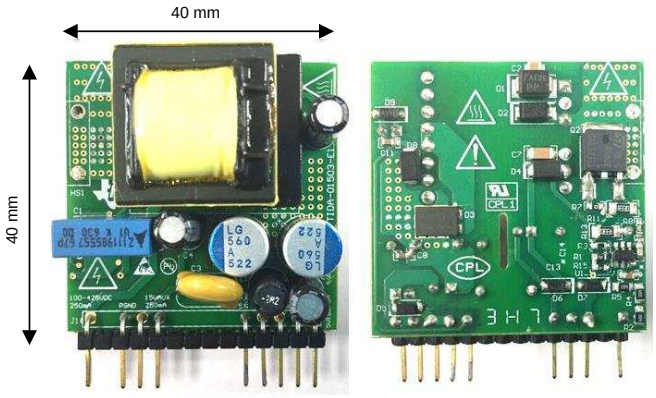
特長

- ピーク電力変換効率: 400V DC、全負荷で85%
- 広い入力電圧範囲で動作するよう設計: 100～425V DC
- 動作電圧範囲の全体にわたって、最大出力20Wを供給
- 出力を設定可能: 15V (1次側基準)、5Vおよび15V (絶縁)
- 低いスタンバイ電力: 100mW未満
- 小型のフォーム・ファクタで電力密度の高いソリューションを実現: 40mm×40mm
- 広範な保護機能が組み込まれた堅牢な設計: 入力ブラウンアウト、出力OC、SC、出力OV

アプリケーション

- AC/DC用の補助電源
- サーバー用電源
- テレコム整流器
- UPSおよび産業用電源





Top view　Bottom View

1 System Description

High-power converters used in server, telecom, and industrial systems need auxiliary power supplies to support housekeeping needs of the power supply unit (PSU). An auxiliary power supply is commonly used to power the internal control electronics and voltage and current feedback sensing electronics of the PSU. It is an isolated DC-DC converter generating multiple outputs to power primary- and secondary-side control devices. The typical usage of an auxiliary power supply of an industrial AC/DC system is shown in 図 1.

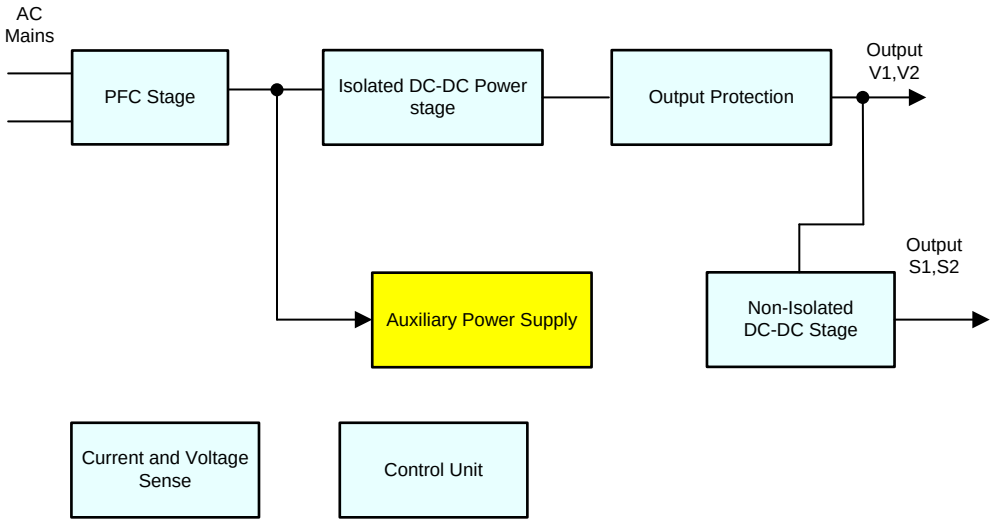


図 1. Typical Block Diagram of Industrial AC/DC Power Supply

The auxiliary power supplies are independent isolated DC-DC converters because PSUs have an EMI filter, a diode-bridge rectifier, and a bulk capacitor present in the system, generating a rectified DC bus. These supplies operate over a wide input range from 100- to 450-V DC and need to keep system electronics powered under all conditions to detect faults such as undervoltage, overvoltage, and overcurrent. Typically, auxiliary power supplies generate multiple outputs delivering power from 5 to 40 W, supporting system fans and auxiliary output.

This reference design is a 20-W auxiliary power supply, designed specifically to meet low standby power needs of 100 mW, peak efficiency of 85% at 400-V DC. This reference design is a simple, low-component, low-cost, primary-side regulated (PSR) flyback converter implemented using the UCC28704 device that regulates constant-voltage (CV) and constant-current (CC) output and uses discontinuous conduction mode (DCM) valley. The design operates over wide input range of 100- to 425-V DC, delivering a total power of 20 W from three outputs (15 V, 5 V_ISO, 15 V_ISO).

This reference design meets the key challenges of the auxiliary power supply to provide safe and reliable power while delivering high performance with low power consumption and low bill of material (BOM) cost.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS					
Input voltage (V_{IN})	—	100	350	425	V
No load power (P_{NL})	V_{IN} = 400 V, I_{OUT} = 2 mA	—	—	0.1	W
OUTPUT CONDITIONS					
Output1 voltage	Referred to primary	—	15	—	VDC
Output1 current	—	—	—	0.25	A
Output1 line regulation	—	—	—	5	%
Output1 load regulation	—	—	—	8	%
Output1 ripple	Peak to peak	—	—	500	mV
Output2 voltage	Isolated	—	15	—	VDC
Output2 current	—	—	—	0.25	A
Output2 line regulation	—	—	—	5	%
Output2 load regulation	—	—	—	8	%
Output2 ripple	Peak to peak	—	—	500	mV
Output3 voltage	Isolated	—	5	—	VDC
Output3 current	—	—	—	3	A
Output3 line regulation	—	—	—	5	%
Output3 load regulation	—	—	—	5	%
Output3 ripple	Peak to peak	—	—	75	mV
Output power (Total from all outputs)	—	—	—	20	W
SYSTEM CHARACTERISTICS					
Efficiency (η)	V_{IN} = V_{NOM} and full load on all the outputs	—	85	—	%
Operating ambient	—	–10	25	55	°C
Board size	Length × Breadth × Height		40 × 40 × 20		mm

2 System Overview

2.1 Block Diagram

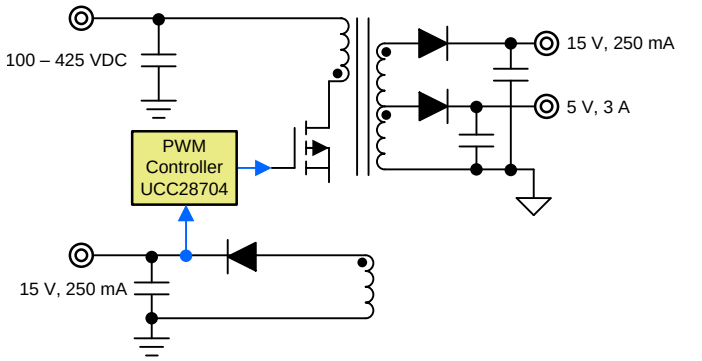


図 2. Block Diagram for 20-W Auxiliary Power Supply

図 2 shows the high-level block diagram of circuit. The main part of this design is the PWM controller UCC28704. This design board has a flyback power stage implemented using the UCC28704 PSR CC-CV flyback controller to deliver three outputs, where one of the outputs (15 V/0.25 A) is referred to the primary ground of the transformer, and two are isolated outputs (5 V/3 A, 15 V/0.25 A). The design operates over a wide input range of 100- to 425-V DC, delivering a total power of 20 W.

2.2 Highlighted Products

This reference design features the following devices, which are selected based on their specifications and appropriateness for this design. The key features of the highlighted products are mentioned as follows. For more information on each of these devices, see their respective product folders at TI.com or click on the links for the product folders under リソース on the first page of this design guide.

2.2.1 UCC28704

To implement the high-performance, small form factor flyback design at 20-W power, the UCC28704 is a good choice as it offers a series of benefits to address the auxiliary power supply needs with reduced feedback loops. Because the device uses PSR, it eliminates the need for an optocoupler and secondary feedback components.

The UCC28704 off-line flyback controller is a highly integrated, 6-pin primary-side regulated PWM controller for designing high-efficiency AC-to-DC power supplies with low standby power consumption to comply with global efficiency standards. The controller has ultra-low current consumption at startup to enable designs with <30-mW no-load input power and save standby mode energy consumption. Intelligent primary-side sensing and control enables 5% output voltage and current control without using an optocoupler or secondary-side feedback circuits. Key features that make this device unique are:

- PSR eliminates optocoupler and secondary feedback components
- ±5% output voltage (CV) and current (CC) regulation
- Enhanced dynamic load response
- Constant current output undervoltage protection (CCUV) with auto-restart response
- 85-kHz maximum switching frequency
- DCM valley-switching operation

- Clamped gate drive output for MOSFET
- NTC resistor interface
- Resistor or external HV depletion-mode FET start-up
- Fault protections: Input low line, output overvoltage, overcurrent, and short-circuit
- SOT23-6 package

2.3 System Design Theory

This reference design provides 20 W of continuous power over a wide DC input range from 100- to 425-V DC. The design has a flyback power stage implemented using the UCC28704 PSR CC-CV flyback controller to deliver three outputs, where one of the outputs (15 V/0.25 A) is referred to the primary ground of the transformer, and two are isolated outputs (5 V/3 A, 15 V/0.25 A). The system efficiency is around 85% with a 400-V DC input under full load condition. In addition, several protections are embedded into this design, which includes input undervoltage protection and output short-circuit protection.

Overall, the main focus of this design is to achieve high efficiency and very low standby power in a compact form factor to address high power density converters.

2.3.1 DCM Flyback Converter With PSR

Flyback converters provide a cost effective solution for DC-DC conversion needs. They are widely used for DC-DC converters up to 150 W. There are three modes of operation, namely discontinuous mode (DCM), QR mode, and continuous conduction mode (CCM). For lower power applications, DCM or QR mode is preferred as they have reduced power losses and optimal peak currents in low power applications. As the output wattage increases, the CCM becomes more efficient due to the reduced peak and RMS currents.

2.3.1.1 Primary Side Regulation (PSR)

In primary-side control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. As shown in 図 3, during this time, the auxiliary winding voltage has a down slope representing a decreasing total rectifier forward voltage drop VF and resistance voltage drop ($I_S R_S$) as the secondary current decreases to zero. To achieve an accurate representation of the secondary output voltage on the auxiliary winding, the discriminator reliably blocks the leakage inductance reset and ringing, continuously samples the auxiliary voltage during the down slope after the ringing is diminished, and captures the error signal at the time the secondary winding reaches zero current.

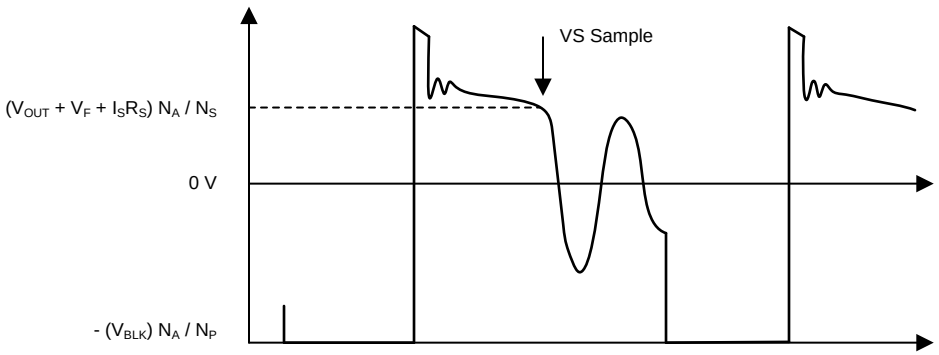


図 3. Auxiliary Winding Voltage

Flyback converters designed with PSR flyback controllers eliminate the use of conventional optocoupler based feedback. The PSR flyback controllers sense the voltage feedback through auxiliary winding and current feedback through current sense resistor used in series with switching FET. In addition, PSR flyback controllers provide wide range of protections and accurate limiting of both current and power. The UCC28704 controller has PSR feedback eliminating opto-feedback, thus reducing the component count.

2.3.2 Flyback Circuit Component Design

The UCC28704 is a flyback power supply controller that provides accurate CV and CC regulation with primary-side feedback, eliminating the need for optocoupler feedback circuits. The controller operates in DCM with valley switching to minimize switching losses. The modulation scheme is a combination of frequency and primary peak current modulation to provide high conversation efficiency across the load range.

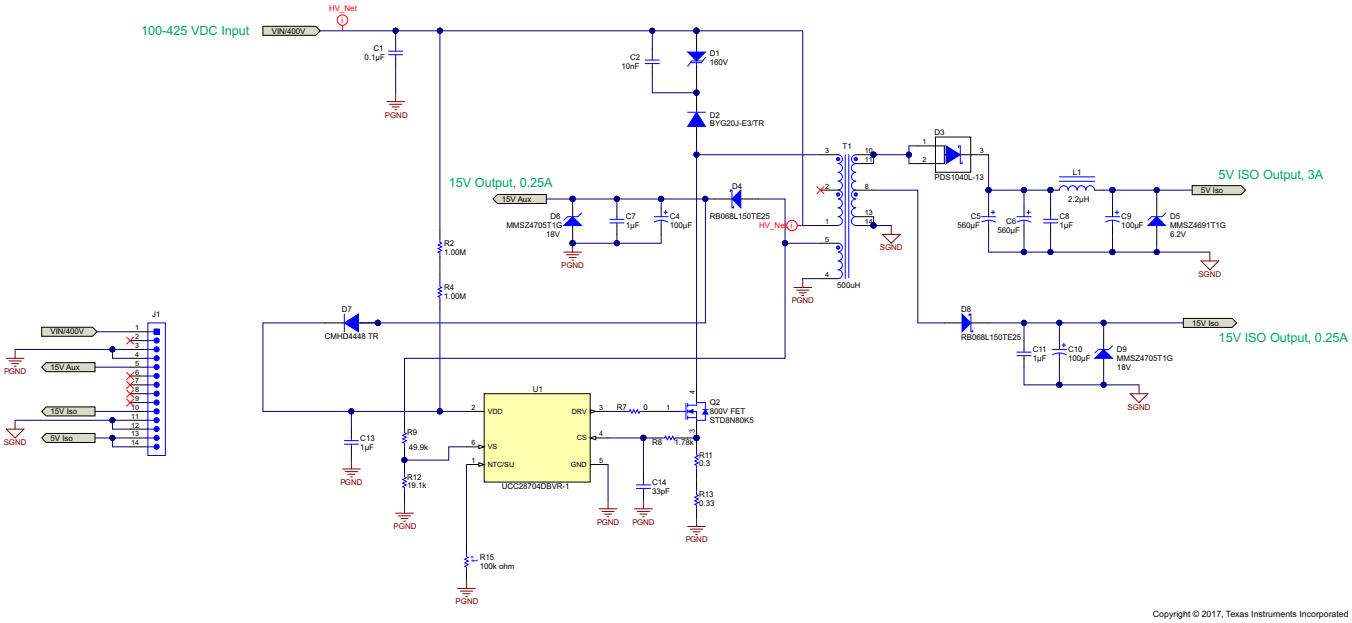


図 4. UCC28704 Circuit Component Design

表 2. Flyback Converter Design Parameters

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS					
Input voltage (V_{IN})	—	100	350	425	V
OUTPUT CONDITIONS					
Output1 voltage	Referred to primary	—	15	—	VDC
Output1 current	—	—	—	0.25	A
Output1 ripple	Peak to peak	—	—	500	mV
Output2 voltage	Isolated	—	15	—	VDC
Output2 current	—	—	—	0.25	A
Output2 ripple	Peak to peak	—	—	500	mV
Output3 voltage	Isolated	—	5	—	VDC
Output3 current	—	—	—	3	A
Output3 ripple	Peak to peak	—	—	50	mV
Output power (Total from all outputs)	—	—	—	20	W
SYSTEM CHARACTERISTICS					
Efficiency (η)	V_{IN} = 400 V and full load on both all the outputs	—	85	—	%
Switching frequency (f_{MAX})	—	—	—	85	kHz

2.3.2.1 Transformer Turns Ratio and Inductance Calculations

The maximum primary-to-secondary turns ratio can be determined by the target maximum switching frequency at full load, the minimum input capacitor bulk voltage, and the estimated DCM resonant time.

Initially, determine the maximum available total duty cycle of the on-time and secondary conduction time based on target switching frequency and DCM resonant time. For DCM resonant time, assume 500 kHz if there are no estimates from previous designs. For the transition mode operation limit, the period required from the end of secondary current conduction to the first valley of the VDS voltage is ½ of the DCM resonant period, or 1 µs assuming a 500-kHz resonant frequency. D_{MAX} can be determined using 式 1.

$$D_{MAX} = 1 - \left(\frac{t_R \times f_{MAX}}{2} \right) - D_{MAGCC} \quad (1)$$

Where:

- t_R is the estimated period of the LC resonant frequency at the switch node
- D_{MAGCC} is defined as the secondary-diode conduction duty cycle during CC operation and is fixed internally by the UCC28704 at 0.475

Using t_R = 2 µs , f_{MAX} = 85 kHz, and D_{MAGCC} = 0.475, D_{MAX} comes out to be 0.44.

Once D_{MAX} is known, the maximum turns ratio of the primary to secondary can be determined with 式 2. The total voltage on the secondary winding needs to be determined, which is the sum of output voltage V_{OCV}, the secondary rectifier V_F, and the cable compensation voltage (V_{OCBC}).

$$N_{PS(MAX)} = \left(\frac{D_{MAX} \times V_{BULK(min)}}{D_{MAGCC} \times (V_{OCV} + V_F + V_{OCBC})} \right) \quad (2)$$

V_{OCBC} is the additional voltage drop of post filter inductor and any other target cable-compensation voltage added to V_{OCV}. In this design, V_{OCV} is set to 0.3 V.

- For a 5-V/3-A output, N_{PS} comes out to be 15.97.

A similar procedure is repeated for a 15-V/0.25-A auxiliary output and 15-V/0.25-A isolated output.

- For 15-V/0.25-A auxiliary output, N_{PSaux} = 5.98
- For 15-V/0.25-A isolated output, N_{PS2} = 5.98

The primary transformer inductance can be calculated using the standard energy storage equation (式 3) for flyback transformers, which includes the primary peak current (I_{PPK}), maximum switching frequency (f_{MAX}), output power (P_{OUT}), and power supply efficiency (Ɲ). Initially determine the transformer primary current (see 2.3.2.2).

A standard value of 500 µH is used in this design.

$$L_P = \frac{2 \times P_{OUT}}{\eta \times I_{PP}^2 \times f_{MAX}} \quad (3)$$

2.3.2.2 Primary Peak Current Calculation

For 20 W of output power and minimum input voltage (V_{DC_MIN} = 100 V), the average input current is given by 式 4.

$$I_{AVG} = \frac{P_{OUT}}{\eta \times V_{DC\_MIN}} \quad (4)$$

I_{AVG} = 0.235 A

Peak primary current (I_{PPK}) is given by 式 5:

$$I_{PEAK} = \frac{2 \times I_{AVG}}{D_{MAX}} \quad (5)$$

I_{PPK} = 1.07 A

R_{CS} is used to program the primary-peak current with 式 6:

Where:

- $V_{CST(max)}$ is maximum current sense threshold voltage (typical ≈ 0.75 V)

R_{CS} comes out to be 0.7 Ω

Actual value used in the design is R_{CS} = 0.63 Ω is selected; this is implemented by series combination of 0.3 Ω and 0.33 Ω (R11 and R13) in the schematic to adjust its value easily.

$$R_{CS} = \frac{V_{CST(max)}}{I_{PEAK}} \quad (6)$$

With this value of current sense resistor, the peak primary current is expected to be 1.19 A (by using 式 6). For further calculations, the value of primary peak current (I_{PPK}) used is 1.19 A.

2.3.2.3 Transformer Parameter Verification

The transformer turns ratio selected affects the MOSFET V_{DS} and secondary rectifier reverse voltage, so these must be reviewed.

The reflected voltage on the primary side is given by 式 7:

$$V_{REF} = (V_{OUT} + V_F) \times N_{PS} \quad (7)$$

With N_{PS1} = 15.97, the reflected voltage is:

V_{REF} = (5 + 0.5 + 0.3) × 15.97 = 92.626

The MOSFET V_{DS} stress is given by 式 8, which includes an estimated leakage inductance voltage spike (V_{LK}).

$$V_{DSPK} = V_{IN(max)} + (V_{OCV} + V_F + V_{OCBC}) \times N_{PS} + V_{LK} \quad (8)$$

For $V_{IN(MAX)}$ = 425 V, V_{OCV} = 5 V, V_F = 0.5 V, V_{OCBC} = 0.3 V, N_{PS1} = 15.97 and V_{LK} = 30% of V_{REF}:

V_{DSPK} = 425 + (5 + 0.5 + 0.3) × 15.97 + 27.78 = 545.4

The secondary rectifier voltage stress is given by 式 9:

$$V_{REV} = \frac{V_{IN(max)}}{N_{PS}} + (V_{OCV} + V_{OCBC}) \quad (9)$$

For $V_{IN(MAX)}$ = 425 V, V_{OCV} = 5 V, V_F = 0.5 V, V_{OCBC} = 0.3 V, N_{PS1} = 15.97

V_{REV} = (425/15.97) + 5 + 0.3 = 31.91 V

式 10 and 式 11 are used to determine for the minimum t_{ON} target of 0.3 µs and minimum de-mag time, $t_{DMAG(min)}$, target of 1.7 µs.

$$t_{ON(min)} = \frac{L_P}{V_{IN(max)}} \times \frac{I_{PP(max)}}{K_{AM}} \quad (10)$$

$$t_{DMAG(min)} = \frac{t_{ON(min)}}{N_{PS}} \times \frac{V_{IN(max)}}{(V_{OCV} + V_F)} \quad (11)$$

Where K_{AM} is AM control ratio (typical value = 4).

To determine the optimum turns ratio (NPS), design iterations are generally necessary to optimize and evaluate system-level performance trade-offs and parameters mentioned in 2.3.2.1 to 2.3.2.3.

2.3.2.4 Transformer Peak Current and RMS Current Calculations

Considering the transformer current waveform as shown in 図 5, the transformer primary RMS current (I_{PRMS}) is calculated using 式 12.

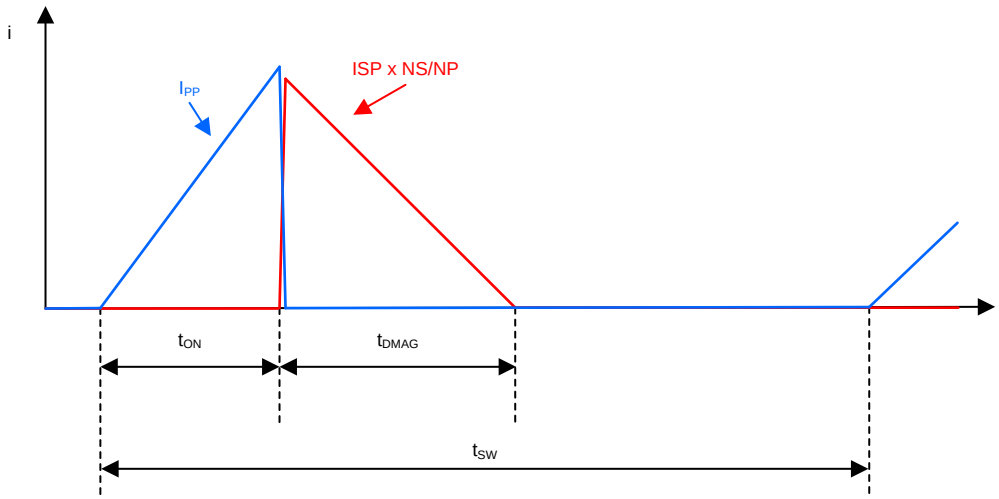


図 5. Transformer Current

$$I_{PRMS} = I_{PP(nom)} \times \sqrt{\frac{D_{MAX}}{3}} \quad (12)$$

I_{PRMS} comes out be 0.46 A.

Calculate the transformer secondary peak currents and RMS currents using 式 13 and 式 14, respectively.

$$I_{SPKx} = \frac{2 \times P_{OUTx}}{V_{OUTx} \times D_{MAG}} \quad (13)$$

$$I_{SRMSx} = I_{SPKx} \times \sqrt{\frac{D_{MAG}}{3}} \quad (14)$$

For the 5-V/3-A isolated output, the values of secondary peak and RMS currents are 12.63 A and 5.025 A, respectively. For the 15-V/0.25-A isolated output, the value of secondary peak and RMS currents are 1.05 A and 0.417 A, respectively. For the 15-V/0.25-A auxiliary output, the value of secondary peak and RMS currents are 1.05 A and 0.417 A, respectively.

Based on these calculations, a Würth Elektronik transformer is designed for this application:

- Part number 750343661
- N_{PS1} = 16 ; N_{PS2} = 5.8; N_{PAUX} = 5.8
- L_P = 500 µH ;L_{LK} = 7 µH (primary leakage inductance)

The inductor saturation current rating must be greater than the calculated peak current. This leaves margin for transient conditions if the peak inductor current increases above the steady state value. The RMS or heating current rating must be greater than the calculated RMS current.

2.3.2.5 Main Switching Power MOSFET Selection

The drain-to-source RMS current, I_{DS_RMS}, through the switching FET is same as the transformer primary RMS current as calculated earlier using 式 12. Select a MOSFET with higher current rating than the I_{DS_RMS} calculated.

The maximum voltage across the FET can be estimated using 式 8. Considering a margin of 25%, the voltage rating of the MOSFET used here is 800 V.

For this design, the STD8N80K5 800-V 6-A MOSFET is used.

2.3.2.6 Zener Clamp Circuit

During turnoff, a high-voltage spike due to the transformer's leakage inductance appears on MOSFET. This excessive voltage spike on the MOSFET may lead to an avalanche breakdown and eventually failure of the MOSFET. A clamping circuit placed across the primary winding helps to limit the voltage spike caused by this leakage inductance to a safe value.

The easiest way is to use a Zener clamp circuit that consist of a diode and high-voltage Zener or transient voltage suppressor (TVS) diode. The Zener diode effectively clips the voltage spike until the leakage energy is totally dissipated in the Zener diode. The advantage of using this circuit is that it only clamps whenever the combined V_R (Reflected Voltage) and V_{SPIKE} is greater than its breakdown voltage. At low line and lighter loads where the spike is relatively low, the Zener may not clamp at all; therefore, there is no power dissipated on the clamp.

2.3.2.7 Rectifier selection

The secondary output diode reverse voltage or blocking voltage needed ($V_{DIODE\_BLOCKING}$) is calculated using 式 15.

$$V_{DIODE\_BLOCKING} = \frac{V_{IN(max)}}{N_{PS}} + \left(V_{OCV} + V_{OCBC}\right) \tag{15}$$

For the 5-V/3-A ISO output rail, the blocking voltage comes out to be 32.36 V. For this output, a 40-V, 10-A Schottky diode is used.

For the 15-V/250-mA ISO and 15-V/250-mA auxiliary output rails, the blocking voltage comes out to be V = 88.8 V. For these outputs, the 150-V, 2-A Schottky diode is used.

These diodes are selected based on high current rating and low cost to minimize the forward drop of diode and hence reduce power loss.

2.3.2.8 VS Resistor Divider and NTC

The VS divider resistors determine the output voltage regulation point of the flyback converter. Also, the high-side divider resistor (R_{S1}) determines the line voltage at which the controller enables continuous DRV operation. R_{S1} is initially determined based on the transformer auxiliary-to-primary turns ratio and the desired input voltage operating threshold.

$$R_{S1} = \frac{V_{IN(run)}}{N_{PA} \times I_{VSL(run)}} \tag{16}$$

Where:

- $V_{IN(run)}$ is the converter input startup (run) voltage around 100-V DC
- $I_{VSL(run)}$ is the VS line-sense run current = 220 μA (see UCC28704 datasheet)
- N_{PA} the transformer primary-to-auxiliary turns ratio

Using these values, R_{S1} comes out to be 78.1 kΩ. The actual value used for R_{S1} (R9) is 49.9 kΩ.

The low-side VS pin resistor is selected based on desired output voltage regulation as seen by 式 17.

$$R_{S2} = \frac{R_{S1} \times V_{VSR}}{N_{AS} \times (V_{OCV} + V_F) - V_{VSR}} \quad (17)$$

Where:

- V_{VSR} is the CV regulating level at the VS input (= 4.05 V; UCC28704 datasheet)
- N_{AS} is the transformer auxiliary-to-secondary turns ratio = 2.76 (N_{PS1} /N_{PAUX} = 16/5.8)
- V_{OCV} is the regulated output voltage of the converter (= 5 V)
- V_F is the secondary rectifier diode forward voltage drop at near-zero current (= 0.5 V)

Substituting these values in 式 17 gives R_{S2} = 18.15 kΩ. The actual value used is R_{S2} (R12) = 19.1 kΩ.

The NTC function on NTC/SU-pin is to program with a NTC resistor for the desired overtemperature shutdown threshold. The shutdown threshold is 0.95 V with an internal 105-µA current source, which results in a 9.05-kΩ thermistor shutdown threshold. This pin must be left floating if not used.

2.3.2.9 Output Capacitor Selection

The output capacitors and their total ESR are the main factors to determine the output voltage ripple. 式 18 provides a formula to determine required ESR value R_{ESR}, and 式 19 provides a formula to determine required capacitance. The total output ripple is the sum of these two parts with scale factors and 10 mV to consider other noise as shown in 式 20:

$$R_{ESR} = \frac{1}{I_{pp(max)} \times N_{PS}} \times V_{RIPPLE\_R} \quad (18)$$

$$C_{OUT} = \frac{L_P \times I^2_{PP(max)}}{4 \times (V_{OCV} + V_{OCBC})} \times \frac{1}{V_{RIPPLE\_C}} \quad (19)$$

$$V_{RIPPLE} = 0.81 \times V_{RIPPLE\_R} + 1.15 \times V_{RIPPLE\_C} + 10\,mV \quad (20)$$

The output capacitor RMS current is given by 式 21:

$$I_{COUTx\_RMS} = \sqrt{\left(I^2_{RMSx}\right) - \left(I^2_{OUTx}\right)} \quad (21)$$

The UCC28704 incorporates internal voltage-loop compensation circuits so that external compensation is not necessary, provided that the value of C_{OUT} is high enough. 式 22 determines a minimum value of C_{OUT} necessary to maintain a phase margin of about 40 degrees over the full-load range.

$$C_{OUT} \geq 100 \times \frac{I_{OCC}}{V_{OCV} \times f_{MAX}} \quad (22)$$

For a 5-V/3-A output, the required ripple is V_{RIPPLE} = 50 mV, so assume 0.81 × V_{RIPPLE_R} = 1.15 × V_{RIPPLE_C} = 20 mV, then R_{ESR} = 1.69 mΩ, and C_{OUT} = 1156 µF.

The RMS current is 3.9 A. The minimum output capacitance for stability is 731 µF.

Two standard 560-µF, 10-V capacitors are connected in parallel for the 5-V/3-A output rail.

Similar calculations are done for the 15-V/0.25-A isolated rail and 15-V/0.25-A auxiliary rail. The ripple requirement for these rails is 150 mV, so assume 0.81 × V_{RIPPLE_R} = 1.15 × V_{RIPPLE_C} = 70 mV, then R_{ESR} = 16.3 mΩ, and C_{OUT} = 114.5 µF.

The RMS current is 0.134 A. The minimum output capacitance for stability is 8.24 µF.

A standard 100-µF, 25-V capacitor is used for these output rails.

2.3.2.10 Capacitance on VDD Pin

The capacitance on V_{DD} needs to supply the device operating current until the output of the converter reaches the target minimum operating voltage. At this time, the auxiliary winding can sustain the voltage to the UCC28704.

With a startup resistance (R_{STR}) of 2 MΩ and a desired startup time (dt_{CVDD}) of 1 s, calculate the C_{VDD} using 式 23:

$$C_{VDD} = \left(\frac{V_{IN(min)}}{R_{STR}} - I_{START} \right) \times \frac{dt_{CVDD}}{V_{DD(on)}} \tag{23}$$

Where:

- I_{START} is the startup bias supply current = 1.5 μA
- $V_{DD(on)}$ is the UVLO turnon voltage threshold = 21 V

The chosen value of the C_{VDD} (C13) capacitor is 1 μF.

2.3.3 Flyback Converter Losses

The major energy losses of the flyback converter are:

- In the output diode rectifier
- Conduction losses in the power MOSFET
- Loss due to leakage inductance of the coupled inductor (Flyback transformer)
- Switching losses of the main switch of the converter

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

This section explains the top and bottom views of the PCB for this reference design showing all the different sections. It also explains the power supply requirement and connectors used to connect the external world.

3.1.1 TIDA-01503 PCB Overview

図 6 and 図 7 show the top and bottom view of the TIDA-01503 PCB, respectively.

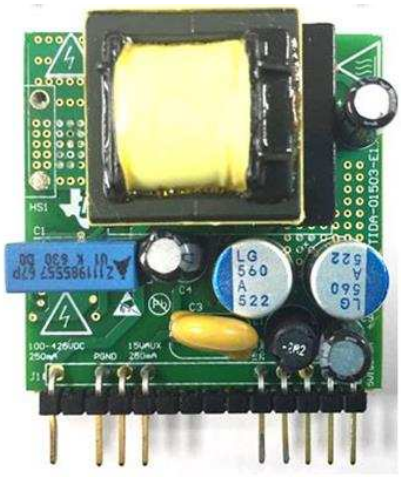


図 6. Top View of TIDA-01503

図 7. Bottom View of TIDA-01503

3.1.2 Connectors

表 3 shows the connectors used on the TIDA-01503 PCB and their purpose.

表 3. Connectors

CONNECTOR	PIN NO	PIN NAME	PURPOSE
J1	1	VIN/400V	Input 100- to 425-V DC
	2	NC	Not connected
	3	PGND	Primary ground
	4	PGND	Primary ground
	5	15V Aux	Non-isolated 15-V auxiliary output
	6	NC	Not connected
	7	NC	Not connected
	8	NC	Not connected
	9	NC	Not connected
	10	15V Iso	Isolated 15-V output
	11	SGND	Secondary ground
	12	SGND	Secondary ground
	13	5V Iso	Isolated 5-V output
	14	5V Iso	Isolated 5-V output

3.1.3 Test Setup

図 8 shows the test setup for evaluating the board.

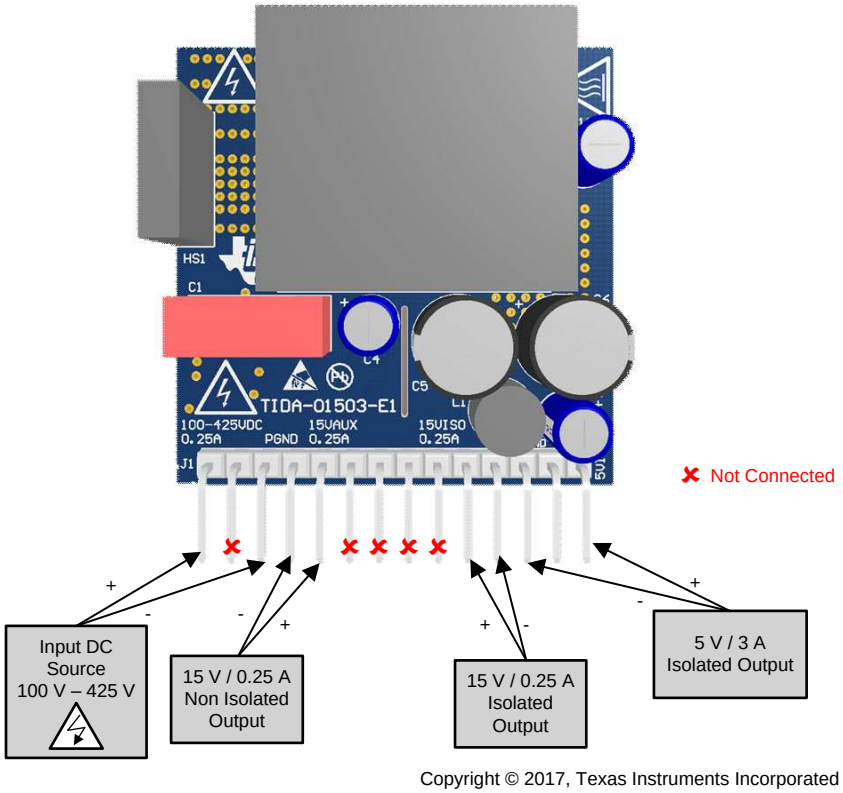


図 8. Test Setup for TIDA-01503

3.1.4 Test Equipment Needed to Validate the Board

- DC source: 0- to 600-V DC rated
- Digital oscilloscope
- 6 ½ digit multimeter
- Electronic or resistive load

3.1.5 Test Conditions

For the input voltage range, the DC source must be capable of varying between a V_{INDC} of 100- to 450-V DC. Set the input current limit to 0.5 A.

For the output voltage range, connect an electronic load capable of 20 V to all the three outputs. The load must be variable and capable of 3 A for V_{OUT}/5 V_ISO and 0.3 A for V_{OUT}/15 V_ISO and V_{OUT}/15 V_AUX. A rheostat or resistive decade box can also be used in place of an electronic load.

3.1.6 Test Procedure

1. Connect the DC source at the input terminal (Pin 1 and Pin 3 of connector J1) of the reference board with Pin 3 being the primary ground reference. Set the current limit to 0.5 A.
2. Connect the following output terminals:
   - Pin 12 and 13 for 5 V/3 A, with Pin 12 being the isolated secondary ground reference. This rail must be loaded up to 3 A at maximum.
   - Pin 10 and 11 for 15-V/0.25-A isolated output, with Pin 11 being the isolated secondary ground reference. This rail must be loaded maximum up to 0.25 A at maximum.
   - Pin 4 and 5 for 15-V/0/.25-A non-isolated output, with Pin 4 being the primary ground reference. This rail must be loaded maximum up to 0.25 A at maximum.
3. Gradually increase the input voltage from 0 V to a turnon voltage of 100 V.
4. Turn on the load to draw current from the output terminals of the converter.
5. Observe the startup conditions and smooth switching waveforms.

3.2 Testing and Results

This section shows the test results for this reference design. To see the test conditions and procedure, see 3.1.5.

3.2.1 Performance Data

3.2.1.1 Efficiency and Regulation With Load Variation

表 4 shows the efficiency and regulation performance data at 100-V DC.

表 4. Efficiency and Regulation at 100-V DC

LOAD	V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	Vout-5V-ISO (V)	Iout-5V-ISO (A)	Vout-15V-ISO (V)	Iout-15V-ISO (A)	Vout-15V-AUX (V)	Iout-15V-AUX (A)	P_{OUT} (W)	EFF	Reg-5V-ISO	Reg-15V-ISO	Reg-15V-AUX
8%	100.11	0.02	1.95	4.935	0.201	13.92	0.027	14.423	0.022	1.68	86.072%	–1.3%	–7.2%	–3.85%
11%	100.11	0.027	2.69	4.946	0.299	14.08	0.027	14.437	0.033	2.32	86.321%	–1.08%	–6.13%	–3.75%
21%	100.11	0.053	5.27	4.977	0.601	14.2	0.05	14.639	0.057	4.53	85.973%	–0.46%	–5.33%	–2.41%
32%	100.02	0.08	8.01	5.011	0.901	14.28	0.082	14.81	0.08	6.86	85.69%	0.22%	–4.8%	–1.27%
43%	100.01	0.107	10.68	5.038	1.205	14.38	0.104	14.938	0.103	9.1	85.173%	0.76%	–4.13%	–0.41%
54%	100	0.134	13.39	5.08	1.49	14.51	0.133	15.085	0.128	11.42	85.281%	1.6%	–3.27%	0.57%
65%	100	0.162	16.18	5.104	1.801	14.59	0.156	15.172	0.152	13.78	85.152%	2.08%	–2.73%	1.15%
76%	100	0.19	18.98	5.131	2.101	14.68	0.181	15.256	0.177	16.14	85.03%	2.62%	–2.13%	1.71%
88%	99.99	0.218	21.78	5.163	2.406	14.78	0.206	15.367	0.203	18.58	85.298%	3.26%	–1.47%	2.45%
100%	99.99	0.248	24.75	5.194	2.753	14.88	0.232	15.5	0.223	21.2	85.68%	3.88%	–0.8%	3.33%
107%	99.98	0.265	26.47	5.214	2.893	14.93	0.244	15.498	0.253	22.65	85.588%	4.28%	–0.47%	3.32%

表 5 shows the efficiency and regulation performance data at 165-V DC.

表 5. Efficiency and Regulation at 165-V DC

LOAD	V_{IN} (V)	I_{in} (A)	P_{IN} (W)	Vout-5V-ISO (V)	Iout-5V-ISO (A)	Vout-15V-ISO (V)	Iout-15V-ISO (A)	Vout-15V-AUX (V)	Iout-15V-AUX (A)	P_{OUT} (W)	EFF	Reg-5V-ISO	Reg-15V-ISO	Reg-15V-AUX
8%	165.01	0.012	1.96	4.938	0.2	13.92	0.027	14.419	0.022	1.68	85.517%	–1.24%	–7.20%	–3.87%
11%	165.04	0.016	2.71	4.944	0.3	14.06	0.027	14.43	0.033	2.33	86.014%	–1.12%	–6.27%	–3.8%
21%	165.07	0.032	5.22	4.978	0.601	14.2	0.049	14.632	0.057	4.52	86.635%	–0.44%	–5.33%	–2.45%
33%	165.04	0.048	7.92	5.015	0.902	14.29	0.082	14.814	0.08	6.88	86.808%	0.3%	–4.73%	–1.24%
43%	165.04	0.063	10.46	5.039	1.205	14.4	0.102	14.935	0.102	9.07	86.663%	0.78%	–4%	–0.43%
54%	165	0.08	13.18	5.07	1.502	14.52	0.122	15.056	0.127	11.3	85.702%	1.4%	–3.2%	0.37%
66%	165	0.097	16.07	5.104	1.804	14.59	0.156	15.158	0.152	13.8	85.839%	2.08%	–2.73%	1.05%
77%	165	0.114	18.81	5.133	2.103	14.68	0.18	15.252	0.177	16.13	85.771%	2.66%	–2.13%	1.68%
88%	165	0.131	21.6	5.166	2.406	14.77	0.205	15.36	0.202	18.56	85.948%	3.32%	–1.53%	2.40%
100%	164.99	0.148	24.47	5.195	2.708	14.87	0.23	15.463	0.228	21.03	85.938%	3.9%	–0.87%	3.09%
107%	164.99	0.159	26.15	5.217	2.873	14.93	0.243	15.49	0.253	22.53	86.168%	4.34%	–0.47%	3.27%

表 6 shows the efficiency and regulation performance data at 250-V DC.

表 6. Efficiency and Regulation at 250-V DC

LOAD	V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	Vout-5V-ISO (V)	Iout-5V-ISO (A)	Vout-15V-ISO (V)	Iout-15V-ISO (A)	Vout-15V-AUX (V)	Iout-15V-AUX (A)	P_{OUT} (W)	EFF	Reg-5V-ISO	Reg-15V-ISO	Reg-15V-AUX
8%	250.04	0.008	1.98	4.939	0.2	13.92	0.027	14.423	0.022	1.68	85.057%	–1.22%	–7.20%	–3.85%
11%	250.04	0.011	2.75	4.945	0.3	14.06	0.027	14.433	0.033	2.34	85.171%	–1.1%	–6.27%	–3.78%
22%	250.04	0.021	5.23	4.977	0.601	14.2	0.049	14.627	0.056	4.5	86.201%	–0.46%	–5.33%	–2.49%
33%	250.04	0.032	7.90	5.011	0.901	14.27	0.081	14.797	0.08	6.85	86.732%	0.22%	–4.87%	–1.35%
44%	250.06	0.043	10.65	5.045	1.206	14.41	0.104	14.94	0.102	9.11	85.518%	0.9%	–3.93%	–0.4%
56%	250.06	0.054	13.43	5.073	1.502	14.48	0.132	15.03	0.132	11.51	85.732%	1.46%	–3.47%	0.2%
66%	250.06	0.064	16.03	5.103	1.803	14.58	0.155	15.15	0.152	13.75	85.767%	2.06%	–2.8%	1%
78%	250.06	0.075	18.78	5.135	2.103	14.67	0.18	15.249	0.177	16.13	85.899%	2.7%	–2.2%	1.66%
89%	250.06	0.086	21.58	5.166	2.406	14.77	0.205	15.35	0.201	18.54	85.92%	3.32%	–1.53%	2.33%
100%	250.06	0.097	24.16	5.197	2.672	14.85	0.23	15.448	0.222	20.74	85.867%	3.94%	–1%	2.99%
109%	250.06	0.105	26.28	5.22	2.889	14.93	0.244	15.513	0.247	22.56	85.838%	4.4%	–0.47%	3.42%

表 7 shows the efficiency and regulation performance data at 350-V DC.

表 7. Efficiency and Regulation at 350-V DC

LOAD	V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	Vout-5V-ISO (V)	Iout-5V-ISO (A)	Vout-15V-ISO (V)	Iout-15V-ISO (A)	Vout-15V-AUX (V)	Iout-15V-AUX (A)	P_{OUT} (W)	EFF	Reg-5V-ISO	Reg-15V-ISO	Reg-15V-AUX
8%	349.95	0.006	2.1	4.936	0.201	13.91	0.028	14.392	0.024	1.72	82.255%	–1.28%	–7.27%	–4.05%
11%	349.95	0.008	2.72	4.943	0.301	14.04	0.028	14.61	0.025	2.25	82.651%	–1.14%	–6.4%	–2.6%
22%	349.95	0.015	5.27	4.97	0.602	14.16	0.051	14.642	0.054	4.51	85.500%	–0.6%	–5.61%	–2.39%
32%	349.95	0.022	7.8	5.005	0.903	14.29	0.072	14.787	0.077	6.69	85.765%	0.1%	–4.73%	–1.42%
44%	349.95	0.03	10.59	5.04	1.202	14.36	0.106	14.89	0.105	9.14	86.283%	0.8%	–4.27%	–0.73%
55%	349.95	0.038	13.34	5.07	1.511	14.47	0.133	15.013	0.129	11.53	86.394%	1.4%	–3.53%	0.09%
66%	349.95	0.046	16.1	5.109	1.795	14.58	0.156	15.149	0.155	13.79	85.638%	2.18%	–2.8%	0.99%
78%	349.95	0.054	18.97	5.137	2.109	14.67	0.181	15.227	0.179	16.22	85.535%	2.74%	–2.2%	1.51%
89%	349.95	0.062	21.7	5.165	2.405	14.76	0.206	15.324	0.205	18.59	85.686%	3.3%	–1.62%	2.16%
100%	349.95	0.07	24.39	5.196	2.685	14.84	0.231	15.433	0.225	20.85	85.472%	3.92%	–1.07%	2.89%
106%	349.95	0.074	25.76	5.214	2.828	14.90	0.242	15.477	0.244	22.12	85.891%	4.28%	–0.67%	3.18%

表 8 shows the efficiency and regulation performance data at 400-V DC.

表 8. Efficiency and Regulation at 400-V DC

LOAD	V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	Vout-5V-ISO (V)	Iout-5V-ISO (A)	Vout-15V-ISO (V)	Iout-15V-ISO (A)	Vout-15V-AUX (V)	Iout-15V-AUX (A)	P_{OUT} (W)	EFF	Reg-5V-ISO	Reg-15V-ISO	Reg-15V-AUX
9%	399.94	0.006	2.2	4.936	0.202	13.92	0.027	14.29	0.029	1.79	81.163%	–1.28%	–7.2%	–4.73%
11%	399.94	0.007	2.8	4.943	0.302	14.07	0.027	14.49	0.031	2.31	82.425%	–1.14%	–6.2%	–3.4%
21%	399.95	0.013	5.32	4.97	0.601	14.17	0.049	14.65	0.053	4.47	83.975%	–0.6%	–5.53%	–2.33%
33%	399.94	0.02	8.08	5.008	0.903	14.26	0.081	14.8	0.077	6.82	84.429%	0.16%	–4.93%	–1.33%
55%	399.94	0.034	13.4	5.07	1.502	14.47	0.132	15.041	0.124	11.38	84.97%	1.4%	–3.53%	0.27%
66%	399.94	0.041	16.2	5.101	1.803	14.56	0.154	15.11	0.154	13.77	85.017%	2.02%	–2.93%	0.73%
78%	399.94	0.047	18.96	5.134	2.104	14.66	0.181	15.222	0.18	16.18	85.366%	2.68%	–2.27%	1.48%
89%	399.94	0.054	21.6	5.165	2.402	14.76	0.205	15.345	0.2	18.49	85.601%	3.3%	–1.6%	2.30%
100%	399.94	0.061	24.36	5.196	2.692	14.85	0.23	15.438	0.225	20.87	85.67%	3.92%	–1%	2.92%
108%	399.94	0.066	26.2	5.218	2.891	14.92	0.243	15.509	0.244	22.49	85.861%	4.36%	–0.53%	3.39%

表 9 shows the efficiency and regulation performance data at 425-V DC.

表 9. Efficiency and Regulation at 425-V DC

LOAD	V_{IN} (V)	I_{IN} (A)	P_{IN} (W)	Vout-5V-ISO (V)	Iout-5V-ISO (A)	Vout-15V-ISO (V)	Iout-15V-ISO (A)	Vout-15V-AUX (V)	Iout-15V-AUX (A)	P_{OUT} (W)	EFF	Reg-5V-ISO	Reg-15V-ISO	Reg-15V-AUX
8%	425.04	0.005	2.08	4.937	0.2	13.93	0.027	14.443	0.022	1.67	80.41%	–1.26%	–7.13%	–3.71%
11%	425.1	0.007	2.85	4.943	0.301	14.06	0.027	14.453	0.033	2.34	82.08%	–1.14%	–6.27%	–3.65%
22%	425.04	0.013	5.36	4.975	0.601	14.18	0.049	14.635	0.056	4.5	84.09%	–0.5%	–5.47%	–2.43%
33%	425.05	0.019	8.12	5.009	0.901	14.26	0.081	14.78	0.079	6.84	84.31%	0.18%	–4.93%	–1.47%
44%	425.02	0.025	10.75	5.045	1.206	14.4	0.103	14.936	0.103	9.1	84.67%	0.9%	–4%	–0.43%
55%	425.01	0.032	13.47	5.076	1.505	14.48	0.132	15.044	0.127	11.45	85%	1.52%	–3.47%	0.29%
66%	425.01	0.038	16.19	5.103	1.81	14.57	0.156	15.134	0.151	13.79	85.19%	2.06%	–2.87%	0.89%
77%	425.01	0.045	18.91	5.135	2.106	14.66	0.180	15.237	0.177	16.15	85.41%	2.7%	–2.27%	1.58%
89%	425.01	0.051	21.76	5.167	2.408	14.76	0.205	15.343	0.202	18.57	85.35%	3.34%	–1.6%	2.29%
100%	425.01	0.058	24.44	5.195	2.698	14.85	0.23	15.448	0.222	20.86	85.35%	3.9%	–1%	2.99%
108%	425.01	0.062	26.22	5.217	2.837	14.88	0.253	15.469	0.252	22.46	85.65%	4.34%	–0.8%	3.13%

表 10 shows the line regulation of the outputs over the input voltage range for full load.

表 10. Line Regulation at Full Load

INPUT VOLTAGE	Vout-5V-ISO (V)	Vout-15V-ISO (V)	Vout-15V-AUX (V)	Reg-5V-ISO	Reg-15V-ISO	Reg-15V-AUX
99.987	5.194	14.88	15.5	3.88%	–0.8%	3.33%
164.99	5.195	14.87	15.463	3.90%	–0.87%	3.09%
250.06	5.197	14.85	15.448	3.94%	–1%	2.99%
349.95	5.196	14.84	15.433	3.92%	–1.07%	2.89%
399.94	5.196	14.85	15.438	3.92%	–1%	2.92%
425.01	5.195	14.85	15.448	3.90%	–1%	2.99%

表 11, 表 12, and 表 13 show the cross reference data for the 5-V_ISO/3-A rail, 15-V_ISO/0.25-A rail, and 15-V/0.25-A rail, respectively. The cross reference data for each rail is noted while the other output is at full load with a 400-V DC input voltage.

表 11. Cross Regulation for 5 V_ISO/3-A With Full Load on Other Outputs

V_{IN} (V)	Vout-5V-ISO (V)	Iout-5V-ISO (A)	Vout-15V-ISO (V)	Iout-15V-ISO (A)	Vout-15V-AUX (V)	Iout-15V-AUX (A)
400.01	5.176	0.0755	13.57	0.2416	13.954	0.24947
400.01	5.08	0.3016	13.65	0.2428	14.037	0.2509
400.01	5.053	0.6001	13.79	0.2445	14.187	0.2542
400.01	5.059	0.9011	13.955	0.2479	14.359	0.258
400.01	5.082	1.201	14.12	0.2504	14.572	0.2469
400.01	5.11	1.503	14.28	0.2532	14.757	0.24936
400.01	5.136	1.8018	14.43	0.25714	14.924	0.2527
400.01	5.156	2.106	14.57	0.2469	15.068	0.25568
400.01	5.175	2.402	14.69	0.2489	15.231	0.2473
400.01	5.201	2.7003	14.82	0.2506	15.382	0.2506
400.01	5.215	2.813	14.886	0.2521	15.47	0.2523

表 12. Cross Regulation for 15 V_ISO/0.25-A With Full Load on Other Outputs

V_{IN} (V)	Vout-5V-ISO (V)	Iout-5V-ISO (A)	Vout-15V-ISO (V)	Iout-15V-ISO (A)	Vout-15V-AUX (V)	Iout-15V-AUX (A)
400.01	5.16	2.678	17.4	0.0234	15.35	0.25008
400.01	5.169	2.681	15.64	0.05529	15.35	0.2498
400.01	5.17	2.683	15.35	0.07805	15.345	0.2495
400.01	5.176	2.6846	15.19	0.0987	15.35	0.2498
400.01	5.18	2.689	15.08	0.1257	15.356	0.2501
400.01	5.184	2.689	15.01	0.1481	15.36	0.25008
400.01	5.19	2.693	14.96	0.1715	15.368	0.2502
400.01	5.197	2.697	14.89	0.205	15.382	0.2512
400.01	5.2	2.699	14.86	0.2299	15.396	0.2505
400.01	5.207	2.702	14.835	0.2513	15.408	0.2511

表 13. Cross Regulation for 15-V/0.25-A With Full Load on Other Outputs

V_{IN} (V)	Vout-5V-ISO (V)	Iout-5V-ISO (A)	Vout-15V-ISO (V)	Iout-15V-ISO (A)	Vout-15V-AUX (V)	Iout-15V-AUX (A)
400.01	5.164	2.681	14.79	0.2508	19.39	0.0245
400.01	5.17	2.685	14.8	0.25032	17.522	0.0505
400.01	5.175	2.688	14.8	0.2505	16.612	0.0768
400.01	5.182	2.691	14.81	0.2506	16.176	0.103
400.01	5.186	2.692	14.81	0.2511	15.955	0.1245
400.01	5.19	2.694	14.82	0.2508	15.746	0.1536
400.01	5.195	2.696	14.824	0.2514	15.642	0.1758
400.01	5.201	2.699	14.83	0.2508	15.533	0.2052
400.01	5.204	2.701	14.835	0.2516	15.483	0.2223
400.01	5.21	2.704	14.84	0.2518	15.415	0.2509

3.2.1.2 Standby Power

The standby power is noted at multiple DC input voltages with a 2-mA load on a 15-V/0.25-A non-isolated output and no load on other outputs. The results are shown in 表 14.

注: For operating in no load condition, a minimum load of 2 mA is needed on the 15-V/0.25-A non-isolated output.

表 14. Standby Power

INPUT VOLTAGE (V)	INPUT CURRENT (mA)	POWER (mW)
100	0.4017	40.17
165	0.2783	45.9195
250	0.2308	57.7
350	0.2176	76.16
400	0.2184	87.36
425	0.2214	94.095

3.2.2 Performance Curves

3.2.2.1 Efficiency With Load Variation

図 9 shows the measured efficiency of the system with DC input voltage variation.

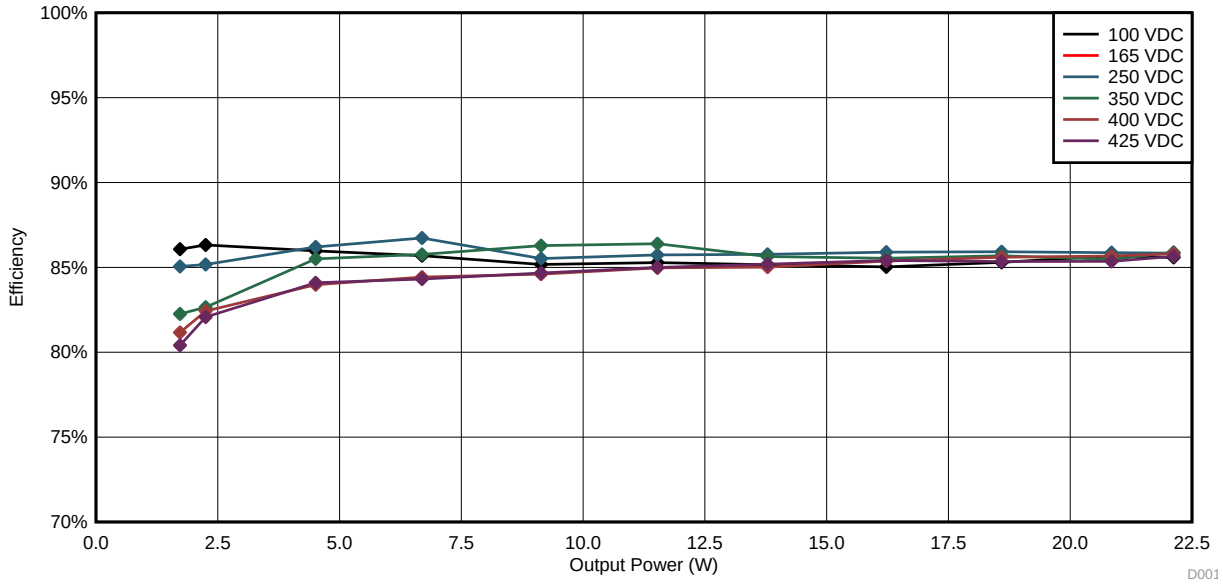


図 9. Efficiency versus Output Power

3.2.2.2 Load and Line Regulation in CV Mode

図 10 shows the measured load regulation of the 5-V_ISO/3-A output.

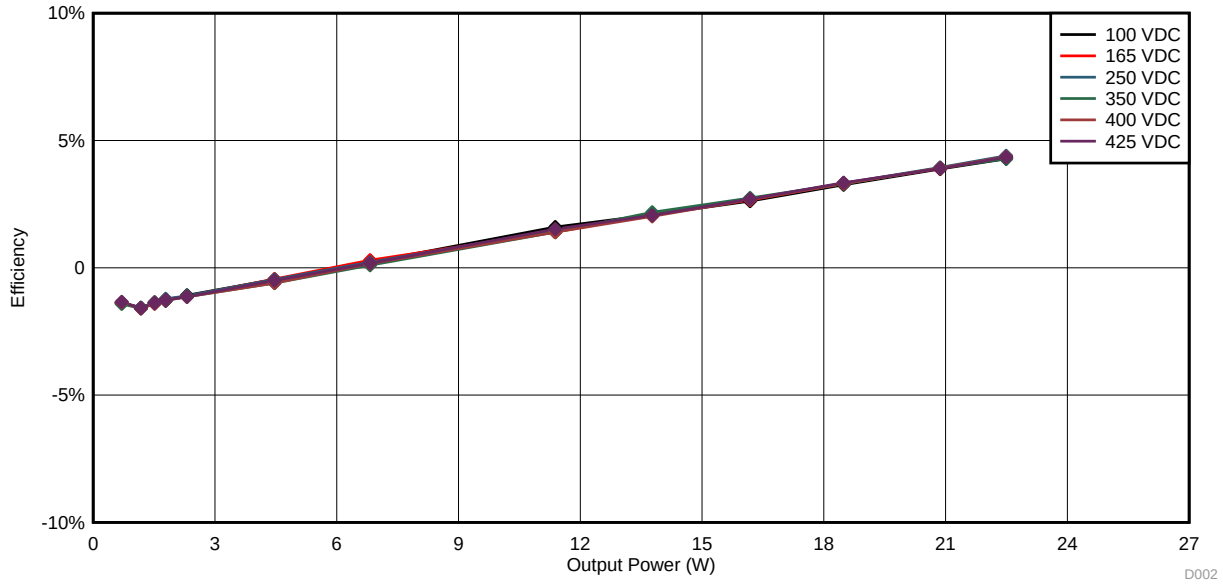


図 10. 5-V_ISO Output Voltage Regulation With Load Current in CV Mode

図 11 shows the measured load regulation of the 15-V_ISO/0.25-A output.

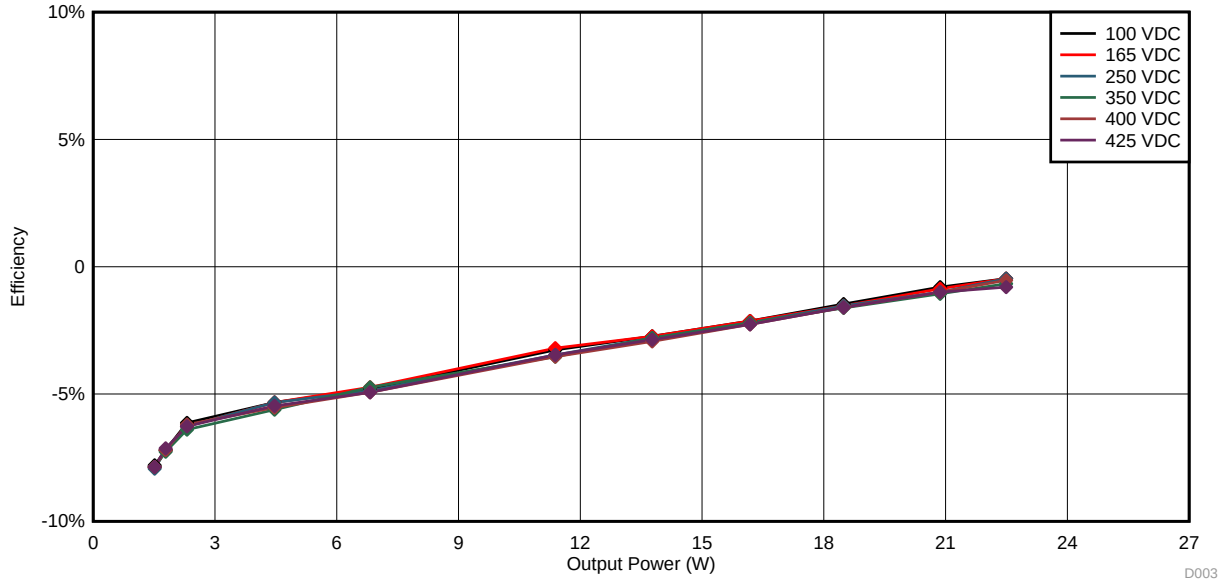


図 11. 15-V_ISO Output Voltage Regulation With Load Current in CV Mode

図 12 shows the measured load regulation of the 15-V/0.25-A output.

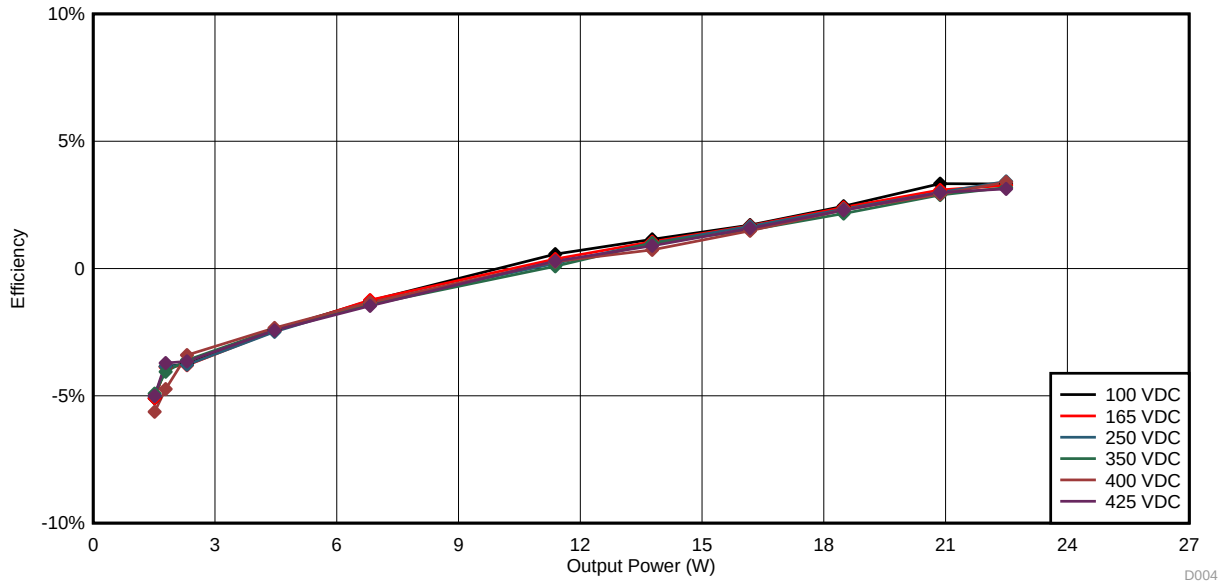


図 12. 15-V_Non-ISO Output Voltage Regulation With Load Current in CV Mode

図 13 shows the measured line regulation of all the outputs at full load.

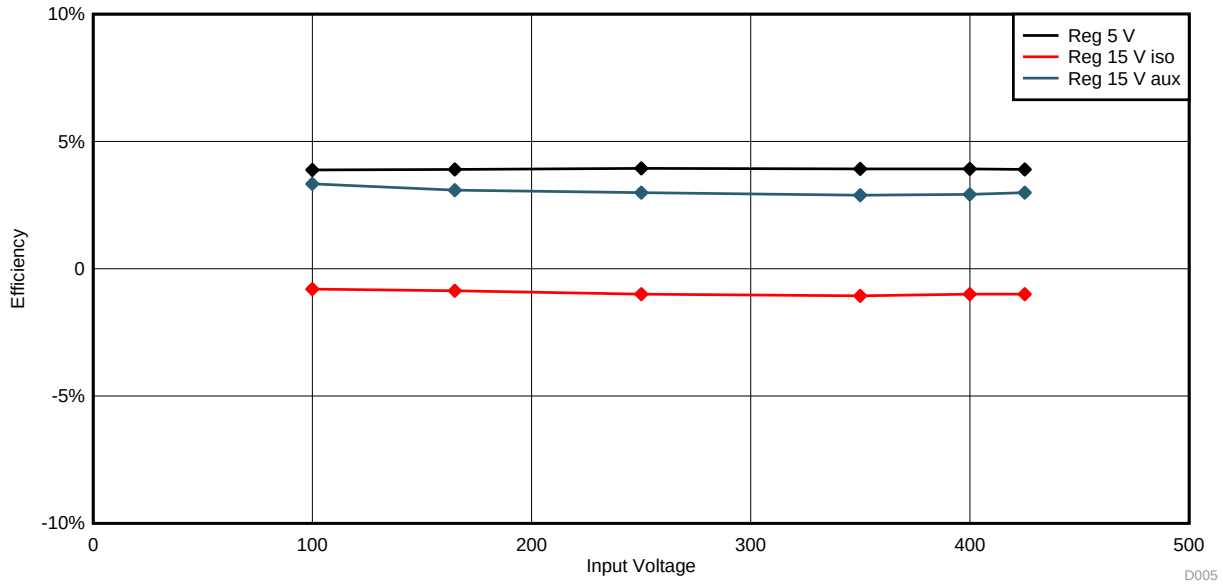


図 13. Line Regulation With Full Load

3.2.3 Functional Waveforms

3.2.3.1 Flyback MOSFET Switching Node Waveforms

Waveforms at the flyback switching (SW) node are observed along with the MOSFET current for 100-V DC and 400-V DC under full load condition.

図 14 and 図 15 show the SW node waveform along with MOSFET current for a 100-V DC input and a 400-V DC input, respectively, with all the rails loaded fully.

注: Yellow trace: Drain-to-source voltage; Red trace: Drain current, 1 A/div

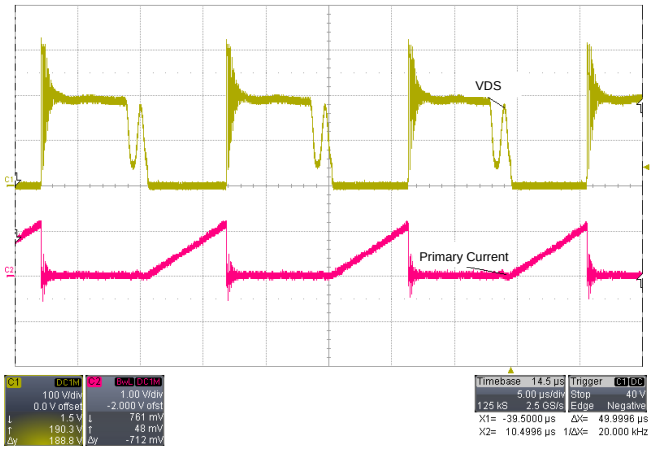


図 14. SW Node Waveform and MOSFET Current at V_{INDC} = 100 V at Full Load

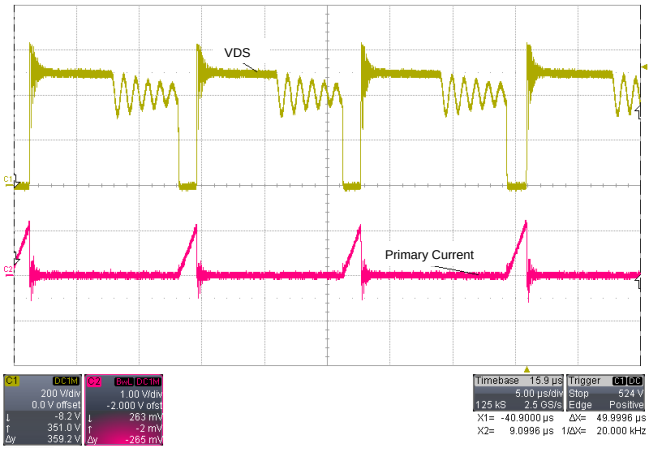


図 15. SW Node Waveform and MOSFET Current at V_{INDC} = 400 V at Full Load

図 16 and 図 17 show the VDS turnon and turnoff waveforms at 400-V DC input voltage and full load.

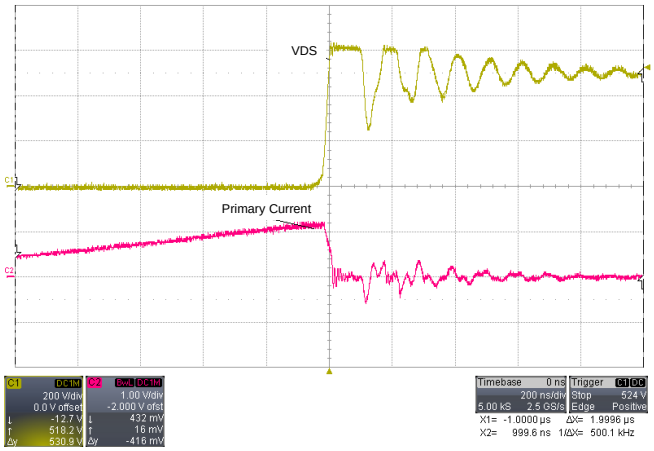


図 16. VDS Turnoff Waveform

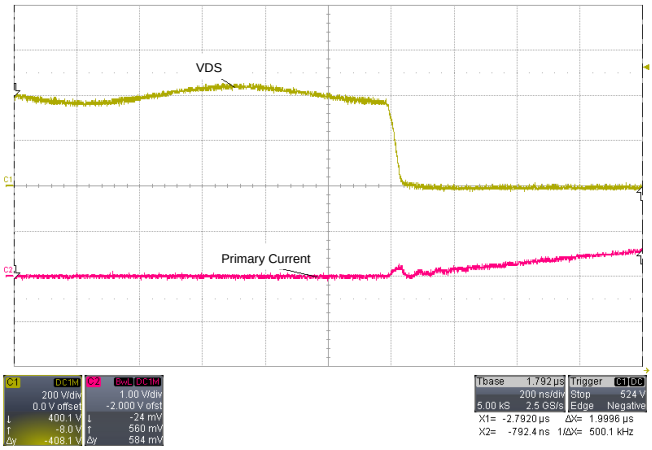


図 17. VDS Turnon Waveform

3.2.3.2 Rectifier Waveforms

Waveforms across all the rectifier diodes are observed at 400 V under full load conditions.

図 18 shows the voltage across diode D3 (for 5-V/3-A isolated output) at a 400-V input at full load.

注: Yellow trace: Diode voltage, 10 V/div

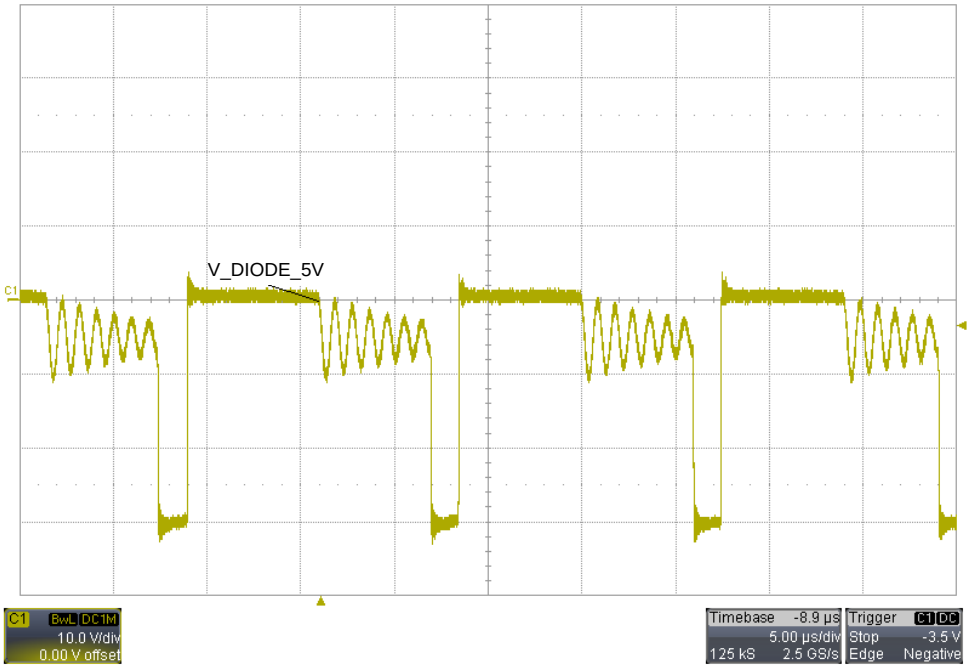


図 18. Voltage Across Diode D1 at 400-V Input at Full Load

図 19 shows the voltage across diode D8 (for a 15-V/0.25-A isolated output) at a 400-V input at full load.

注: Yellow trace: Diode Voltage, 50 V/div

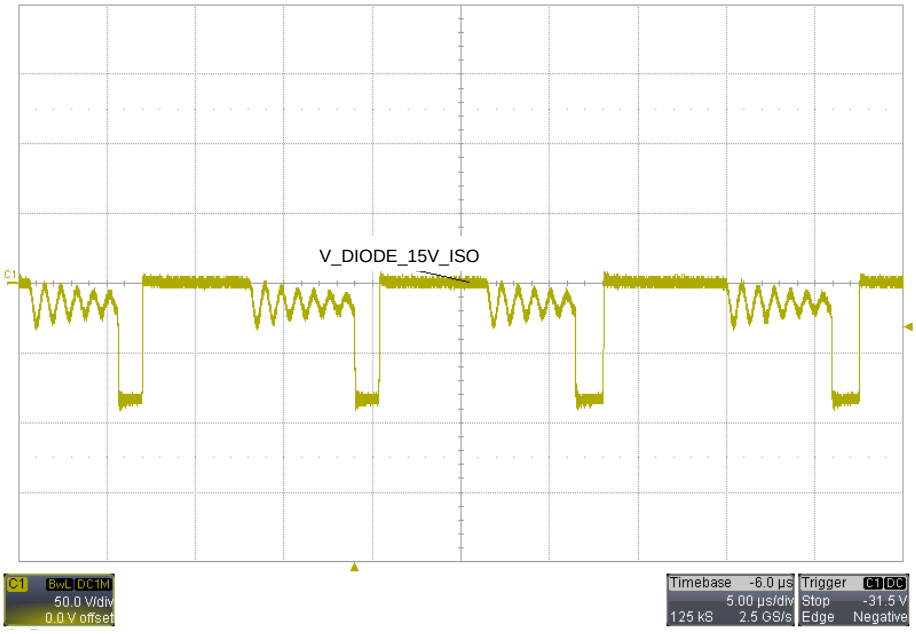


図 19. Voltage Across Diode D8 at 400-V Input at Full Load

図 20 shows the voltage across diode D4 (for 15-V/0.25-A non-isolated output) at a 400-V input at full load.

注: Yellow trace: Diode voltage, 50 V/div

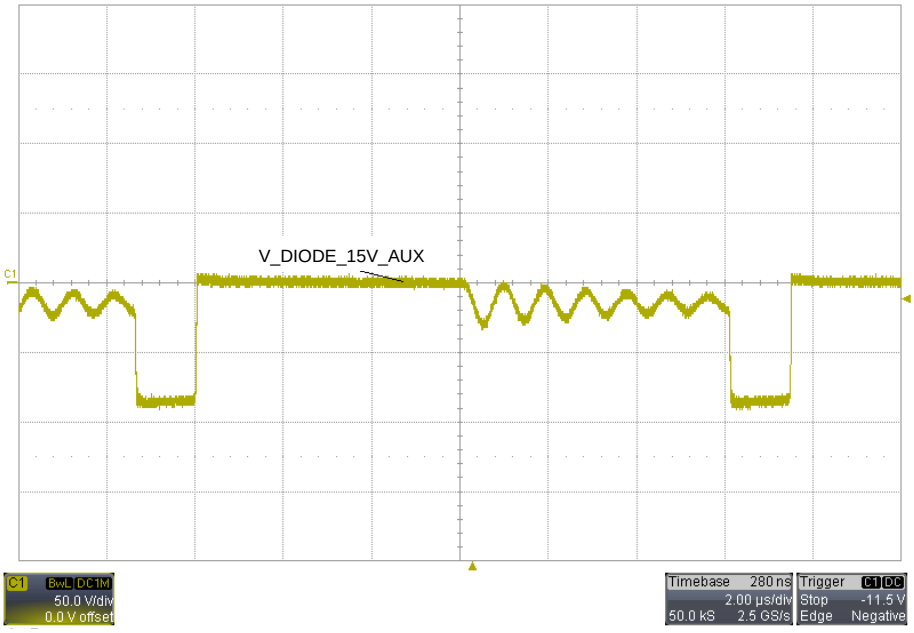


図 20. Voltage Across Diode D4 at 400-V Input at Full Load

3.2.3.3 Output Ripple

For the following figures, the ripple is observed at all the outputs at full load with a 400-V DC input voltage.

The peak-to-peak ripple voltage is around 75 mV for 5-V_ISO output, 500 mV for 15-V_ISO, and 500 mV for 15V-non isolated output.

図 21, 図 22, and 図 23 show the ripple for 5-V_ISO/3-A, 15-V_ISO/0.25-A rail, and 15-V/0.25-A rail, respectively.

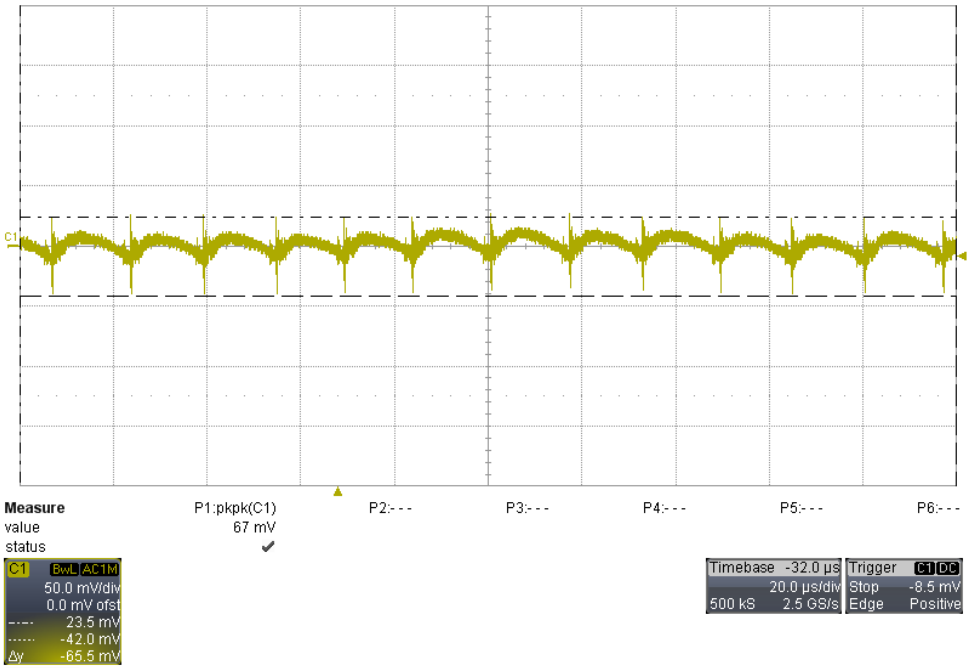


図 21. 5-V_ISO Output Ripple at V_{INDC} = 400 V at Full Load

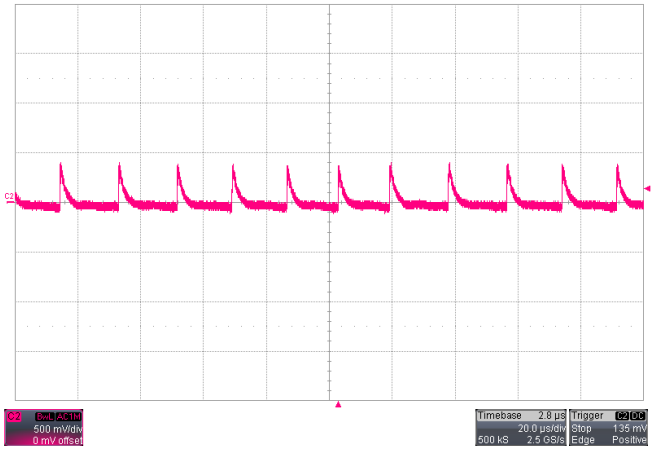


図 22. 15-V_ISO Output Ripple at V_{INDC} = 400 V at Full Load

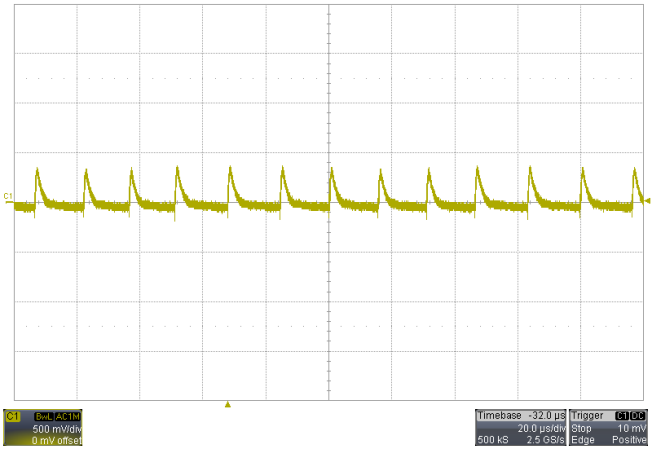


図 23. 15-V Non-Isolated Output Ripple at V_{INDC} = 400 V at Full Load

3.2.4 Transient Waveforms

3.2.4.1 Turnon and Turnoff Characteristics

The output turnon and turnoff waveforms are observed with a resistive load.

図 24 and 図 25 show the turnon and turnoff waveforms at the 5-V_ISO/3A output at a 400-V DC input voltage and full load, respectively.

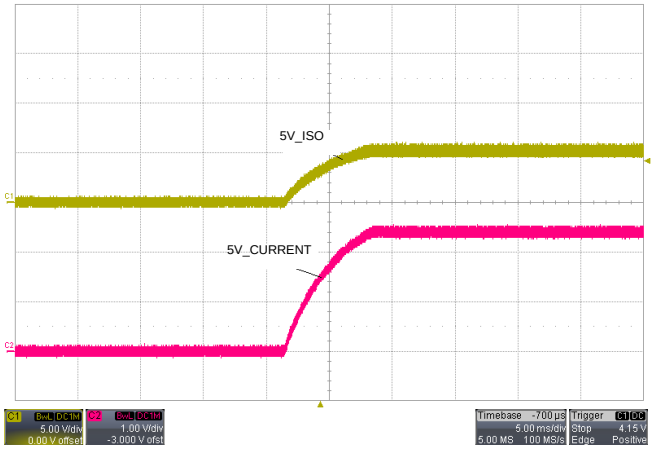


図 24. 5-V_ISO/3-A Output Turnon Waveform at 400-V DC

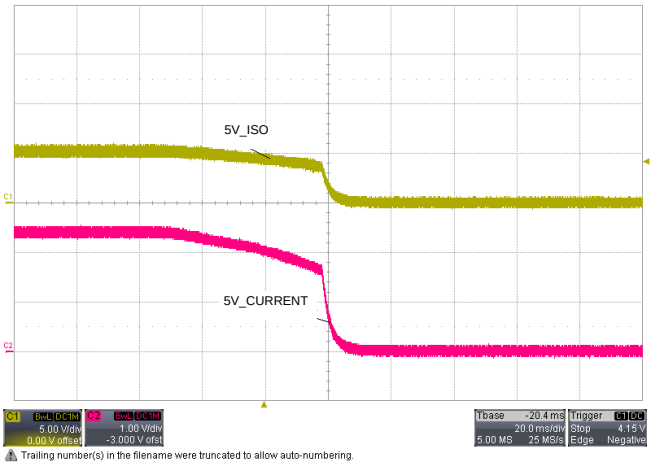


図 25. 5-V_ISO/3-A Output Turnoff Waveform at 400-V DC

図 26 and 図 27 show the turnon and turnoff waveforms at the 15-V_ISO/0.25-A output at a 400-V DC input voltage and full load, respectively.

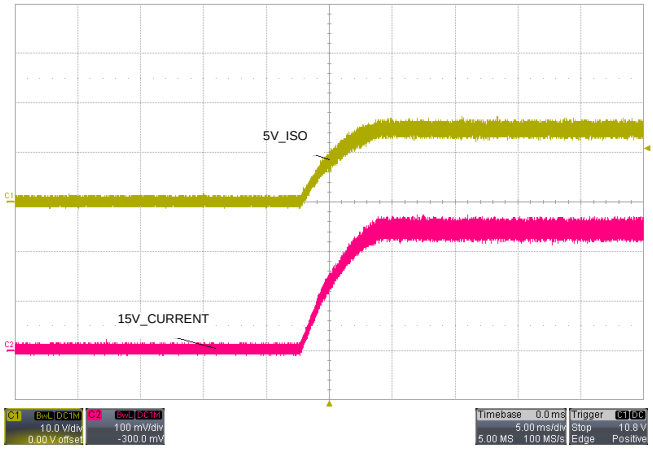


図 26. 15-V_ISO/0.25-A Output Turnon Waveform at 400-V DC

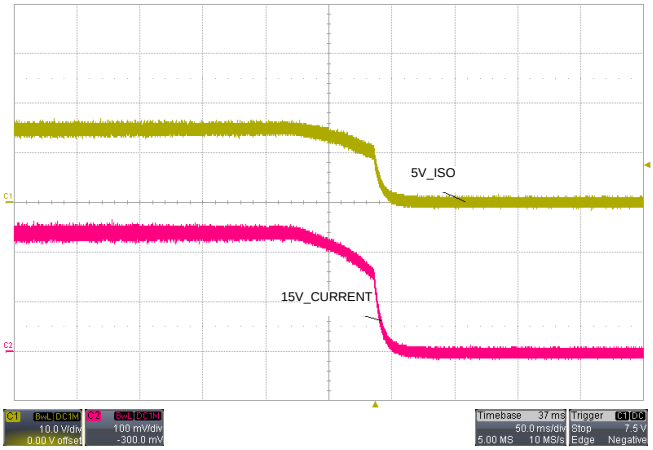


図 27. 15-V_ISO/0.25-A Output Turnoff Waveform at 400-V DC

図 28 and 図 29 show the turnon and turnoff waveforms at the 15-V_Non-ISO/0.25-A output at a 400-V DC input voltage and full load, respectively.

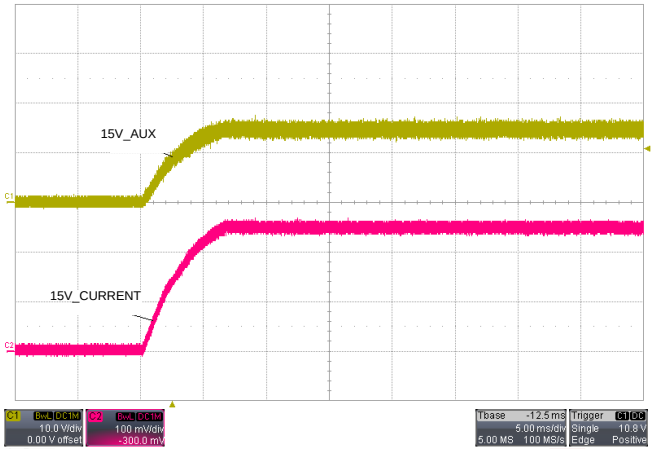


図 28. 15-V_Non-ISO/0.25-A Output Turnon Waveform at 400-V DC

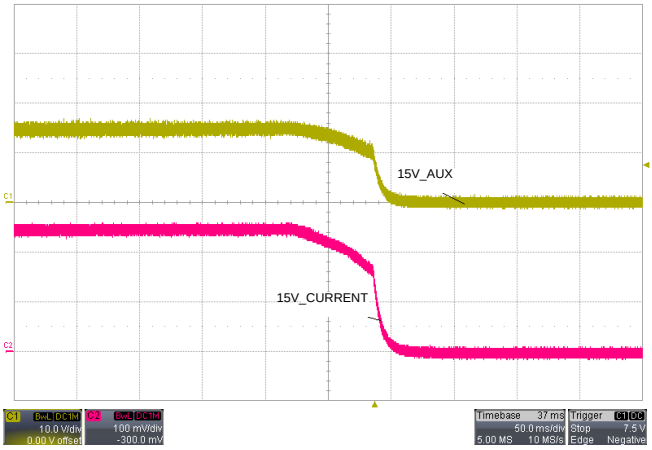


図 29. 15-V_Non-ISO/0.25-A Output Turnoff Waveform at 400-V DC

3.2.4.2 Transient Load Response

Load transient performance is observed for the 5-V/3-A ISO rail. The load transient is observed for output switched on from 10% to 100% and switched off back to 10% load.

図 30 and 図 31 depict the transient load response for the 5-V_ISO output at an input voltage of 400-V DC with a load transient from 0.275 to 2.75 A and vice versa.

注: Yellow trace: Output voltage, 500 mV/div; Red trace: Output current, 2 A/div

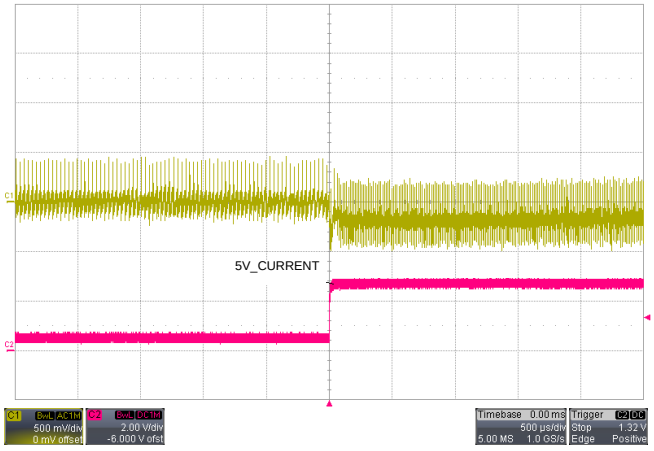


図 30. 5-V_ISO Output Waveform, Load Transient From 0.275 to 2.75 A

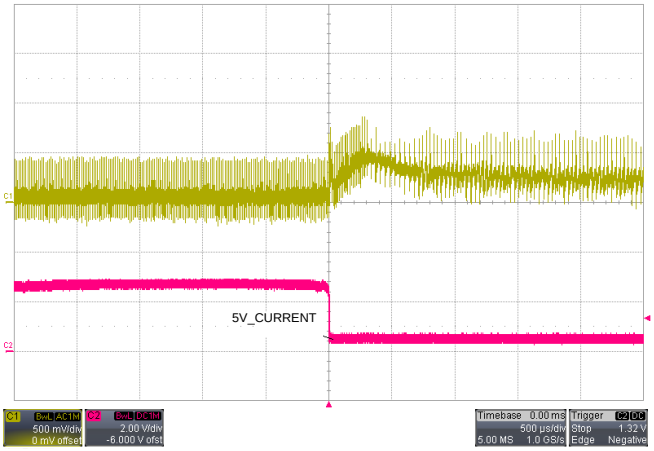


図 31. 5-V_ISO Output Waveform, Load Transient From 2.75 to 0.275 A

3.2.4.3 Short-Circuit Response

The short-circuit response is recorded by applying a short at the 5-V_ISO/3-A output during full load operation. 図 32 shows that during the interval when the short is present, the converter goes into hiccup mode; when the short is removed, the converter recovers back to the normal operation.

注: Yellow trace: Output voltage, 2 V/div; Red trace: Output current, 5 A/div

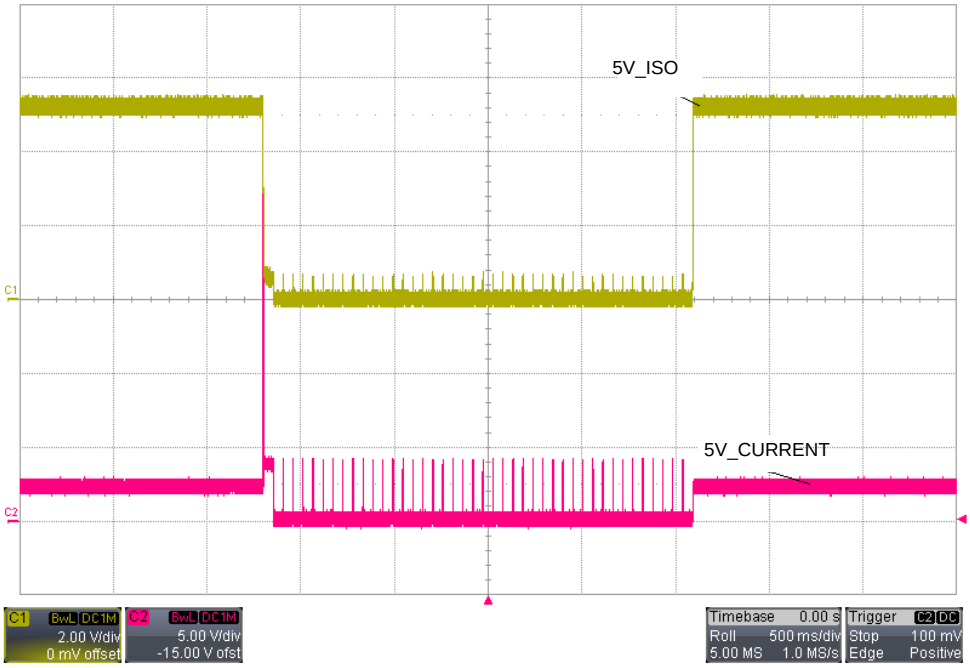


図 32. Response During Short-Circuit and Auto-Recovery After Removal of Short

3.2.5 Thermal Measurements

The thermal measurements are taken at room temperature (25°C) with a 400-V DC input voltage at full load after letting the board run for half an hour and without any external cooling.

図 33 and 図 34 show the top and bottom side thermal images of this reference design, respectively.

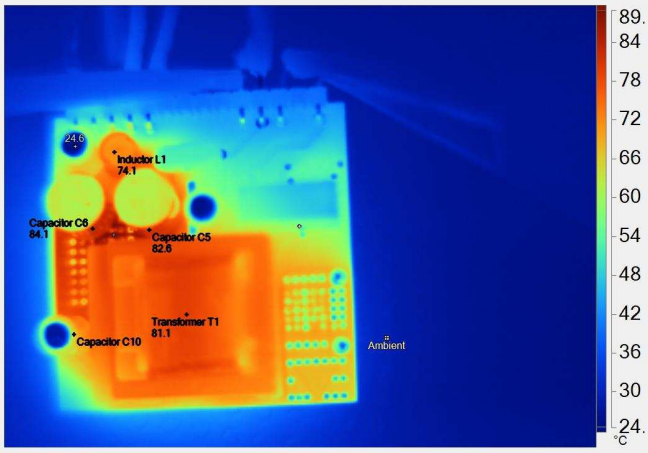


図 33. Top-Side Thermal Image at 400-V DC Input, Full Load, Without Fan

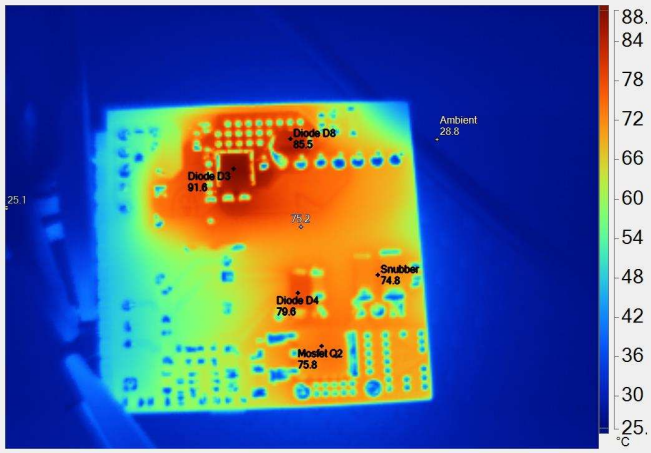


図 34. Bottom-Side Thermal Image at 400-V DC Input, Full Load, Without Fan

表 15. Highlighted Image Markers

NAME	TEMPERATURE
Diode D3	91.6°C
Diode D8	85.5°C
Diode D4	79.6°C
Mosfet Q2	75.8°C
Snubber	74.8°C
Transformer T1	81.1°C
Capacitor C8	84.1°C
Capacitor C5	82.8°C
Inductor L1	74.1°C

3.2.6 Conducted Emissions

This reference design is used as a bias power supply in the TIDA-01494 reference design, and the conducted EMI performance is tested.

図 35 shows the EMI test result.

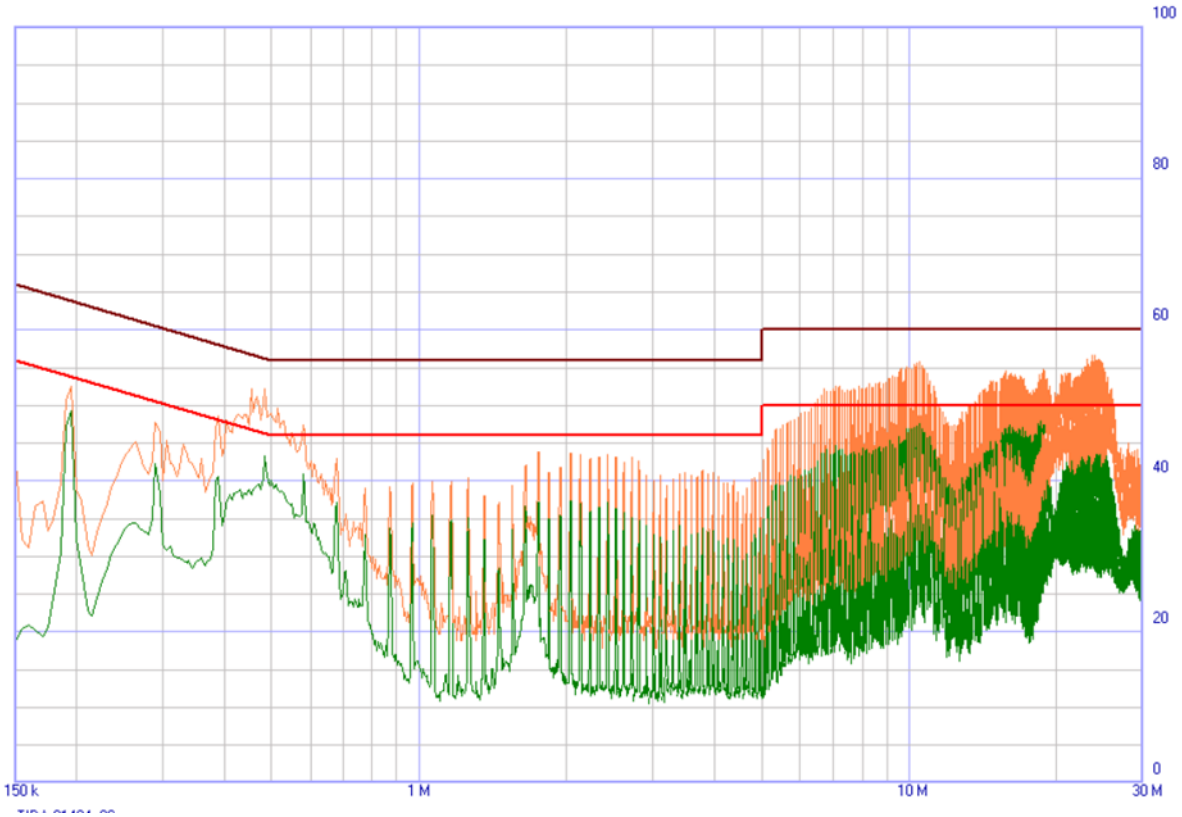


図 35. CE as per EN55022 Class B With TIDA-01494 Board

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01503.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01503.

4.3 PCB Layout Recommendations

Note that the design contains high voltages. The layout must be done with extreme care.

4.3.1 Power Stage Specific Guidelines

Follow these guidelines to route power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high-frequency switching currents. This helps to reduce EMI and improve converter overall performance.
- Keep the switch node as short as possible. A compact switch node reduces common mode noise associated with the high dV/dt.
- Keep traces with high dV/dt and high dI/dt away or shielded from sensitive signal traces with adequate clearance and/or ground shielding.
- Place protection devices such as TVS, snubbers, capacitors, or diodes physically close to the device they are intended to protect, and route them with short traces to reduce inductance.
- To improve thermal performance, increase the copper area connected to GND pins.

4.3.2 Controller Specific Guidelines

Follow the key guidelines for routing controller components and signal circuits:

- Minimize stray capacitance on the VS node. Place the voltage sense resistors close to the VS pin.
- Arrange the components to minimize the loop areas of the switching currents as much as possible. These areas include such loops as the transformer primary winding current loop, the MOSFET gate-drive loop, the primary snubber loop, the auxiliary winding loop, and the secondary output current loop. In practice, trade-offs may have to be made. Loops with higher current must be minimized with higher priority.
- See the placement and routing guidelines and layout examples presented in the UCC28704 datasheet (SLUSCA8).

4.3.3 Layout Prints

To download the layer plots, see the design files at TIDA-01503.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01503.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01503.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01503.

5 Related Documentation

1. Texas Instruments, *Under the Hood of Flyback SMPS Designs*, Power Supply Design Seminar SEM1900 (SLUP254)
2. Texas Instruments, *Control Challenges for Low Power AC/DC Converters*, Power Supply Design Seminar SEM2100 (SLUP325)
3. Texas Instruments, *Troubleshooting TI PSR Controllers*, Application Report (SLUA783)

5.1 商標

6 About the Authors

SALIL CHELLAPPAN is a system manager, member, and group technical staff at Texas Instruments, where he is responsible for developing customized power solutions as part of the power delivery, industrial segment. Salil brings to this role his extensive experience in power electronics, power conversion, EMI/EMC, power and signal integrity, and analog circuits design spanning many high-profile organizations. Salil holds a Bachelor of Technology degree from the University of Kerala.

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改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年9月発行のものから更新 **Page**

- Figure 35: *External EMI Filter Configuration* 削除 34
- Figure 36: *CE as per EN55022 Class A Without External EMI Filter* 削除..... 34
- Figure 37: *CE as per EN55022 Class A With External EMI Filter* 削除 34
- Figure 35: *CE as per EN55022 Class B With TIDA-01494 Board* 追加 34

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お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、もしくは、TIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。