参考資料

TI Designs: TIDA-00313
絶縁付きの-48Vテレコム用電流、電圧、電力検出のリファレンス・デザイン

概要

この検証済みのデザインは、-48Vを搬送するバスの電流、電圧、電力を正確に測定し、そのデータをI^2C互換のインターフェイスで提供できます。このデザインはテレコム・アプリケーションを対象としており、この負の電源電圧は、テレコム機器で最も一般的に使用されています。このデザインは、INA226およびISO1541デバイスを使用します。INA226は、I^2C互換インターフェイスを搭載した電流シャントおよび電力モニタです。このデバイスは、これらの正確な測定を行い、ISO1541デバイスを使用して、負の電圧をグランド基準の信号に変換できます。ISO1541は、低消費電力の双方向I^2C互換アイソレータです。

リソース

TIDA-00313	デザイン・フォルダ
INA226	プロダクト・フォルダ
INA226EVM	プロダクト・フォルダ
ISO1541	プロダクト・フォルダ
TINA-TI™	プロダクト・フォルダ

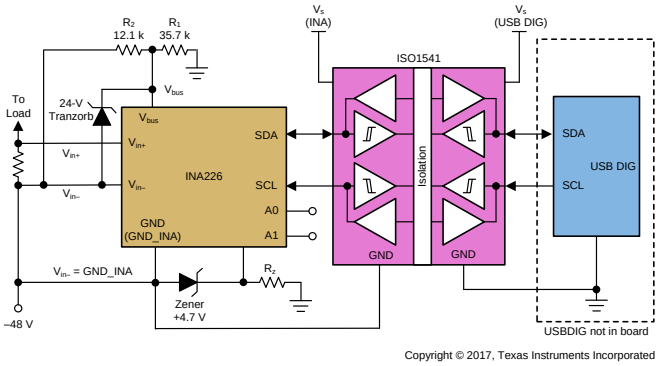
特長

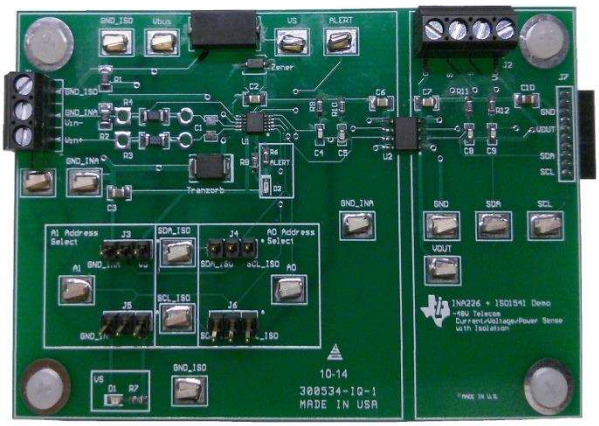
- 電流シャント監視用の-48V同相
- 最大±80mVの差動シャント電圧を測定
- 電流、バス電圧、シャント電圧、電力の測定値を報告
- 絶縁電力
- 低消費電力
- I^2Cとの互換性

アプリケーション

- 標準テレコム機器の電流シャント監視
- 通信インフラストラクチャ

E2Eエキスパートに質問
WEBENCH® デザイン・センター
TI Designs - 高精度ライブラリ





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1 System Description

The challenges that developers of telecom DC/DC power supplies face today include achieving high efficiency, high integration, low system cost, ease of development, and product differentiation. Customers demand additional features such as more sophisticated fault diagnosis, power measurement, and more extensive status reporting over the I^2C or CAN interface. Texas Instruments has digital current shunt monitors capable of reporting current, voltage, and power when a positive power supply is applied to the input; however, most common telecom equipment use a negative supply range of –48 V. The goal of this reference design is to provide these status and monitoring features for a negative voltage bus. This design offers a solution using TI products for telecom companies that wish to monitor current and power in their applications.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	DESCRIPTION	SPECIFICATIONS
Bus voltage	Bus voltage of the current sense resistor in common telecom equipment	–48 V
Measurable shunt voltage range	Range of differential shunt voltages that system can measure	±80 mV
Measurements	What the system can measure and report	Shunt voltage (and current), bus voltage (and power)
Communication	System communication protocol	I^2C compatible

表 2 summarizes the design goals and performance. 図 1 shows the measurement accuracy of the design.

表 2. Comparison of Design Goals and Measured Performance

RELATIVE ERROR	GOAL	MEASURED
I_{load} = 50 mA	0.510%	0.403%
I_{load} = –50 mA	0.51%	0.404%
I_{load} = 750 mA	0.114%	0.013%
I_{load} = –750 mA	0.114%	0.103%

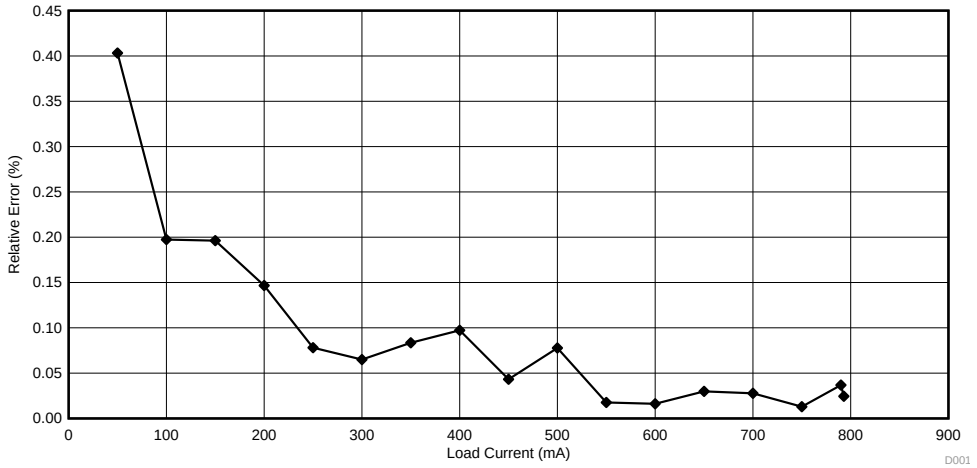

図 1. Measured Relative Error with R_{shunt} = 100 mΩ and I_{load} = 50 mA to 750 mA

2 System Overview

2.1 Block Diagram

図 2 shows the basic idea of the design, which comprises three stages. The first stage uses a TI INA226 current shunt monitor to measure the load current while the device is floating at the –48-V rail. The second stage incorporates a low-power bidirectional isolator (ISO1541) with I²C communication capabilities. This isolator translates these –48-V reference signals to ground reference signals. The third stage uses the TI SM-USB-DIG Platform and INA226EVM software to display the data collected by the INA226 device.

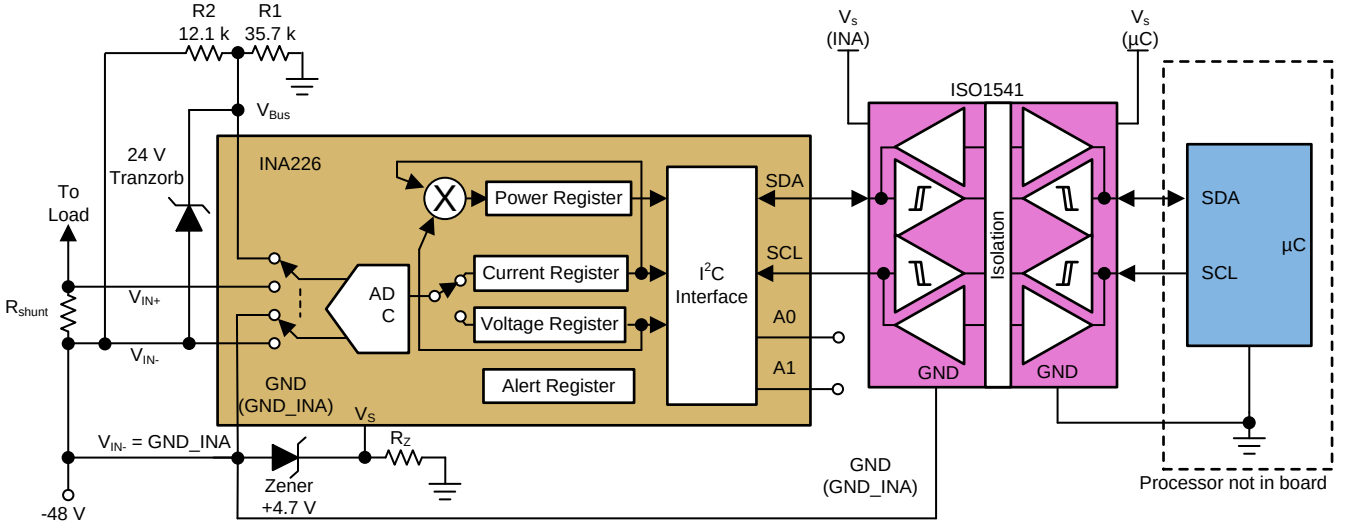

図 2. TIDA-00313 Basic Block Diagram

2.2 Design Considerations

2.2.1 First Stage—INA226 Connections and External Components

The first stage of the circuit uses the INA226 device to monitor the shunt voltage and the bus supply voltage. The INA226 is limited to a bus input voltage range of 0 V to 36 V. This design is intended for use at –48 V, outside the INA226 input voltage capabilities. The following changes are required to enable the INA226 device to monitor the shunt and the –48-V bus supply voltage:

1. Connect a 4.7-V Zener diode between the GND and the V_S pins of the INA226. The potential generated by the voltage drop across the Zener diode and referenced to the negative rail (–48 V) powers the INA226 device. This action provides the positive supply voltage (V_S) that the INA226 device requires to operate.
2. Incorporate a voltage divider on the V_{bus} pin input. Doing so helps to limit the input voltage of the V_{bus} to 36 V maximum, even though –48 V has been applied to the input.

2.2.2 INA226 Referenced to Negative Rail

A separate supply that can range from 2.7 V to 5.5 V typically powers the INA226 device. For this design, connect a 4.7-V Zener diode between the GND (GND_INA) and V_S pins of the INA226. Also, the INA226 ground pin (GND) is tied to the V_{in-} pin of the INA226 (see 図 3). This configuration powers the device using the potential generated by the voltage drop across the Zener diode and references the device to the –48-V rail.

注: This design refers the INA226 GND pin as "GND_INA".

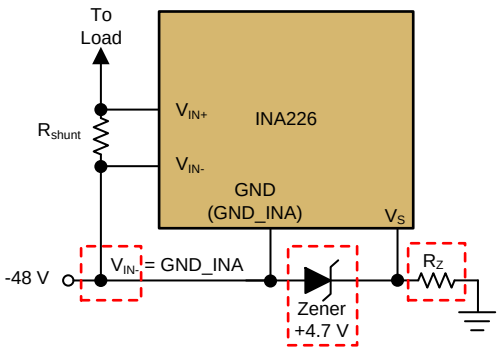

図 3. Connections for Negative Voltage Reference

A power resistor (R_Z) is required in series with the Zener diode. 式 1 calculates the resistor value and 図 4 shows a TINA-TI™ DC simulation with the circuit configuration, calculated values, and results. For this calculation, the designer must consider the Zener bias current and the INA226 quiescent current. From the INA226 data sheet specifications, the maximum quiescent current is 420 µA with V_S = 3.3 V. Because this design specifies to power the device with +4.7 V, estimate the INA226 quiescent current to be approximately 600 µA, maximum.

$$R_Z = \frac{|V_{in-} - V_{zener}|}{I_{zener} + I_{INA226}} = \frac{|48\ V - (-4.7\ V)|}{5\ mA + 600\ \mu A} = 7.73\ k\Omega \quad (1)$$

式 2 shows the power consumption calculation, which is required to determine the power rating of the R_Z resistor.

$$Power = \frac{V^2}{R} = \frac{|V_{in-} - V_{zener}|^2}{R_z} = \frac{|-48\ V - (-4.7\ V)|^2}{7.73\ k\Omega} = 0.2425\ W \quad (2)$$

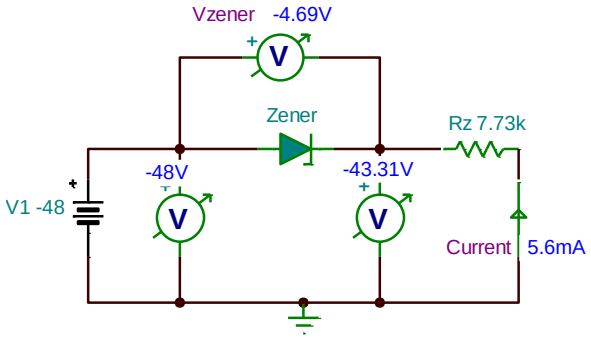

図 4. Power Resistor Selection Simulation

The INA226 has more devices connected to the V_S pin, such as the ISO1541 isolator and some light-emitting diodes (LEDs) which are included on this design. These other devices increase the current flowing through this resistor. For this reason, the R_Z resistor value requires modification. 図 5 shows all devices connected to the V_S pin.

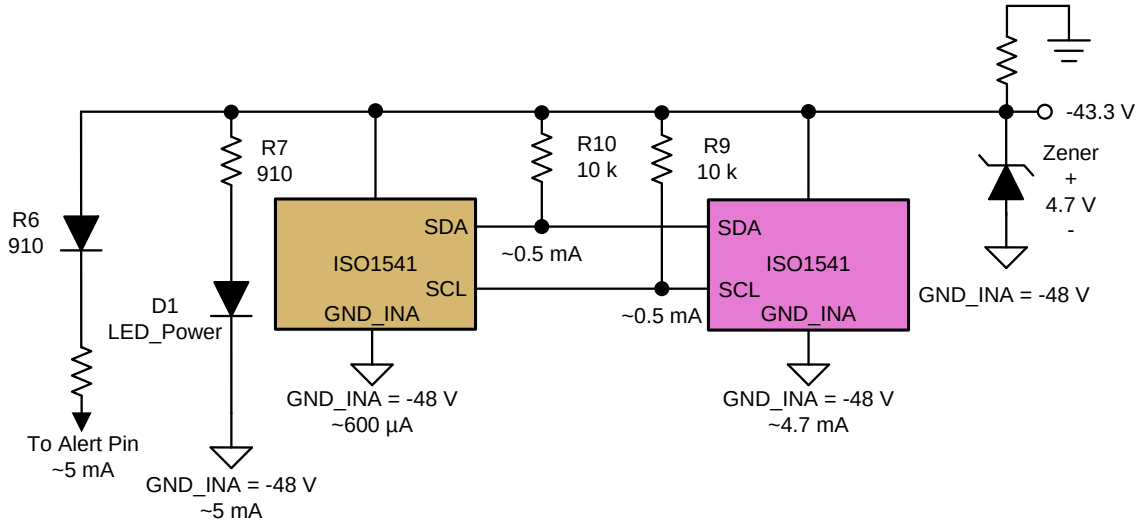

図 5. Devices Connected to INA226 V_s Pin

表 3 lists the current expected to flow through the R_Z resistor.

表 3. Expected Current to Flow Through R_Z

DEVICE	CURRENT
D2 (LED diode for the alert pin)	5.0 mA
D1 (LED diode for power, V_S pin)	5.0 mA
INA226	0.6 mA
ISO1541	4.7 mA
SDA pullup	0.5 mA
SCL pullup	0.5 mA
Zener diode	5.0 mA
	I_{TOTAL} = ≈21.3 mA

Approximating I_{TOTAL} to be 24 mA, calculate the new R_Z and its required power rating (see 式 3).

$$R_z = \frac{\left|V_{in} - V_{zener}\right|}{I_{TOTAL}} = \frac{\left|-48\ V - \left(-4.7\ V\right)\right|}{24\ mA} = 1.8\ k\Omega \tag{3}$$

$$\text{Power} = \frac{V^2}{R} = \frac{\left|V_{in-} - V_{zener}\right|^2}{R_z} = \frac{\left|-48\ V - \left(-4.7\ V\right)\right|^2}{1.8\ k\Omega} = 1.04\ W$$

2.2.3 Limiting Input Voltage of V_{bus}

The INA226 V_{bus} pin is limited to 36 V. This design uses voltages greater than 36 V; therefore, a voltage divider is required at the input of the bus voltage pin. Note that the INA226 device measures the bus voltage, V_{bus}, with respect to GND_INA. 図 6 shows the voltage divider and 式 4 shows the basic voltage divider equation.

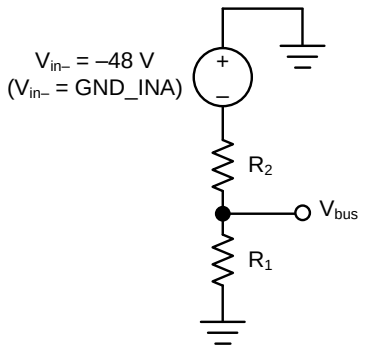

図 6. Voltage Divider

$$V_{bus} = \frac{R_2}{R_1 + R_2} \times V_{in-} \tag{4}$$

Target a voltage divider ratio of 4:1 (4 V_{bus} = V_{in-}), as 式 5 shows.

$$V_{bus} = \frac{1}{4} \times V_{in-} \tag{5}$$

Combine 図 6 and 式 5 to obtain 式 6.

$$\frac{R_2}{R_1 + R_2} = \frac{1}{4} \tag{6}$$

Rearrange 式 6 to define the relation for R_1 and R_2 in 式 7.

$$\frac{R_1}{R_2} = 3 \tag{7}$$

Another important detail to consider is that the V_{bus} pin has an input impedance of 830 kΩ. The 830-kΩ impedance, R_{Vbus}, is connected in reference to GND_INA, which means it will be in parallel with R_2. Now calculate 式 8 as:

$$\frac{R_1}{R_2 \,//\, R_{Vbus}} = 3 \tag{8}$$

For this design, choose R_1 = 35.7 kΩ and R_2 = 12.1 kΩ. With this combination of resistors and with V_{in-} at –48 V, the V_{bus} has 12.02 in reference to GND_INA (see 式 9). Also, just 1 mA of current will flow in that path. If the designer were to select lower resistor values, such as R_1 = 3 kΩ and R_2 = 1 kΩ, around 10 mA of current would be driven. The lower the resistor value, the larger the current that flows in that path.

$$V_{bus} = \frac{R_2}{R_1 + R_2} \times V_{in-} = \frac{12.1\text{k}}{35.7\text{k} + 12.1\text{k}} \times -48\ \text{V} = -12.02\ \text{V} \tag{9}$$

図 7 shows a simple simulation in TINA-TI™ that shows the position and value of the selected resistors, how V_{bus} is measured, and how much current to expect with these resistors values.

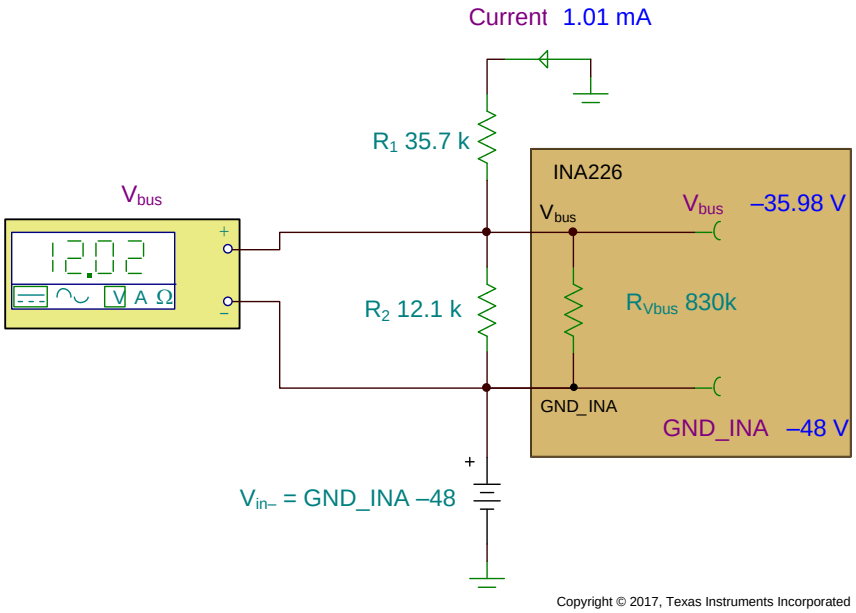

図 7. TINA-TI™ Simulation of Voltage Divider

A TVS (transient voltage suppressor) diode provides protection against surge at the V_{bus} input. TVS devices are ideal for the protection of I/O interfaces, the VCC bus, and other vulnerable circuits for use in telecom applications. With the bus voltage maximum specified as 36 V, the TVS diode must have a breakdown voltage slightly lower than 36 V. The SMBJ24A is selected to protect the INA226 device.

Note that with the V_{bus} connected to the V_{in-} pin (throught R_2), V_{bus} measurements will reflect the divided-down voltage of the bus line source. Thus, the power readings of the INA226 will be the power of the entire system. If knowing the power supplied to the load was desired, then V_{bus} should be connected to the V_{in+} pin (through R_2). In this case, V_{bus} measurements would reflect the divided-down voltage of the load.

Also, note that if the absolute bus voltage of the system is within the V_{bus} input operating voltage range (0 V to 36 V), then the resistor divider is not required and the user can connect the V_{bus} directly to the earth ground of the system.

2.2.4 INA226 Filtering and Input Considerations

The TIDA-00313 board has an optional input filter to remove high-frequency noise from the inputs V_{in+} and V_{in-}.The default values for R_3 and R_4 are 0-Ω resistors. 図 8 shows the recommended values for the filter. 図 9 shows the location of the filter in the board. The board comes populated with two 0-Ω resistors (R_3 and R_4). However, the filter capacitor does not come preinstalled. If a filter is required, use the lowest possible series resistance (typically 10 Ω or less) and a ceramic capacitor. The recommended values for this capacitor are 0.1 µF to 1.0 µF. In many cases, a filter is not necessary.

注: Make sure the 0-Ω resistors are populated on the board; otherwise, the input of the INA226 device remains open.

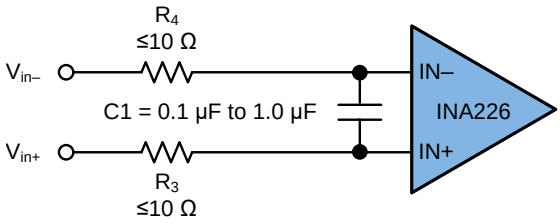

図 8. Input Filter Schematic

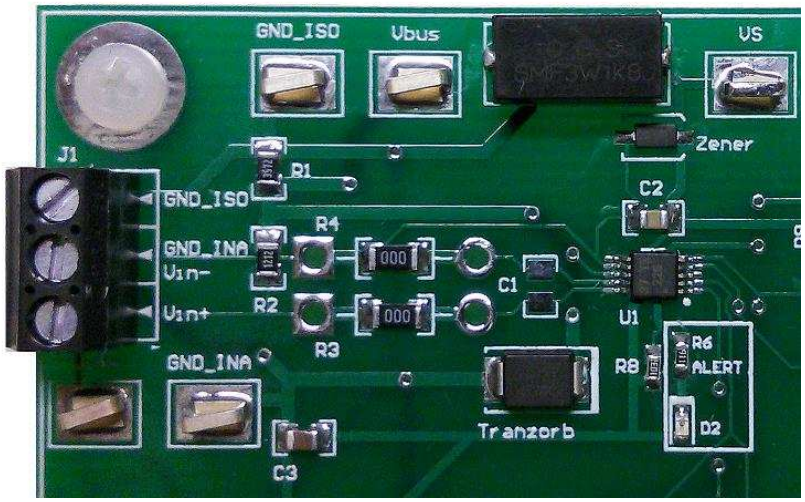

図 9. Location of Input Filter in TIDA-00313 Board

2.2.5 Second Stage—ISO1541 Connections and External Components

The second stage of the circuit uses the ISO1541. The ISO1541 is a low-power, bidirectional I^2C-compatible bus isolator. For more information about how the ISO1541 operates, see *ISO154x Low-Power Bidirectional I^2C Isolators* (SLLSEB6).

The ISO1541 device requires pullup resistors on the SCL and SDA pins. Pullup resistors of 10 kΩ are selected for this design. Capacitors (C_4, C_5, C_6, and C_7) have also been connected to match the test diagram shown in the ISO1541 data sheet, but these are *optional*. TI recommends a 0.01-µF bypass capacitor on the supply. 図 10 shows how the ISO1541 is incorporated in this design. The high-voltage side is connected to the INA226 V_s, GND, SCL, and SDA pins. The low-voltage side is connected to the I^2C master that functions to read the data collected by the INA226 device.

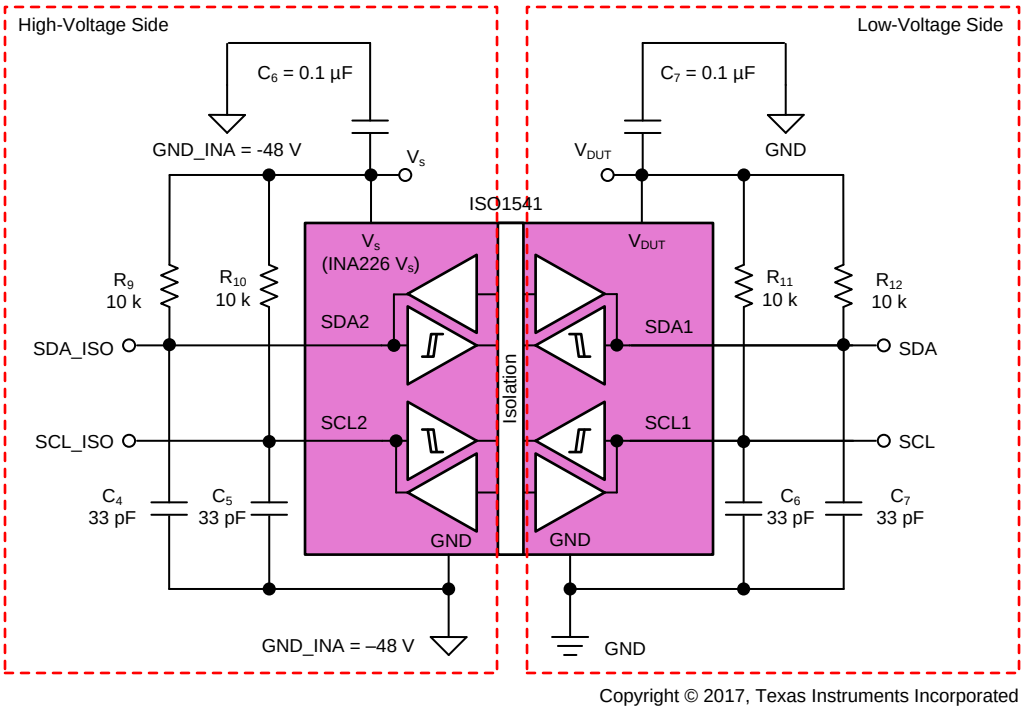

図 10. ISO1541 Connections

2.2.6 Third Stage—SM-USB-DIG Platform and INA226 Software

The third stage uses the TI SM-USB-DIG Platform and INA226EVM software to display the data collected by the INA226 device. 図 11 shows the overall system setup for the TIDA-00313 system. The PC runs software (INA226 Telecom Demo Software) that communicates with the SM-USB-DIG Platform. The SM-USB-DIG Platform provides the supply voltage for the low-voltage side of the ISO1541 device and generates digital signals used to communicate with the TIDA-00313 board. Connectors on the board allow the user to connect to the system under test and monitor the power, current, and voltage.

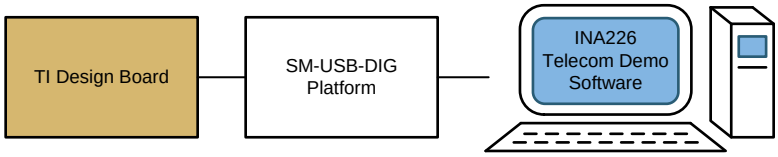

図 11. TIDA-00313 System Setup

For more information about the SM-USB-Dig Platform, see *SM-USB-DIG Platform* (SBOU098). For a quick tutorial on the INA226EVM software, see *INA226EVM Evaluation Board and Software Tutorial* (SBOU113).

2.3 Highlighted Products

2.3.1 INA226

The function of this design calls for a current shunt monitor with a wide common-mode range; high accuracy; the ability to report current, voltage, and power; and the capability to perform I^2C interface communications. The chosen current shunt monitor for this application is the INA226. This device not only has the resolution and accuracy required to achieve the design goals, but also features all the internal subsystems required to realize the current, voltage, and power calculations.

The INA226 is a digital current shunt monitor with an I^2C interface. The device takes two measurements: shunt voltage and bus voltage. 図 12 shows a basic block diagram of INA226. For more information about INA226 features, see *INA226 High-Side or Low-Side Measurement, Bi-Directional Current and Power Monitor with I^2C Compatible Interface* (SBOS547).

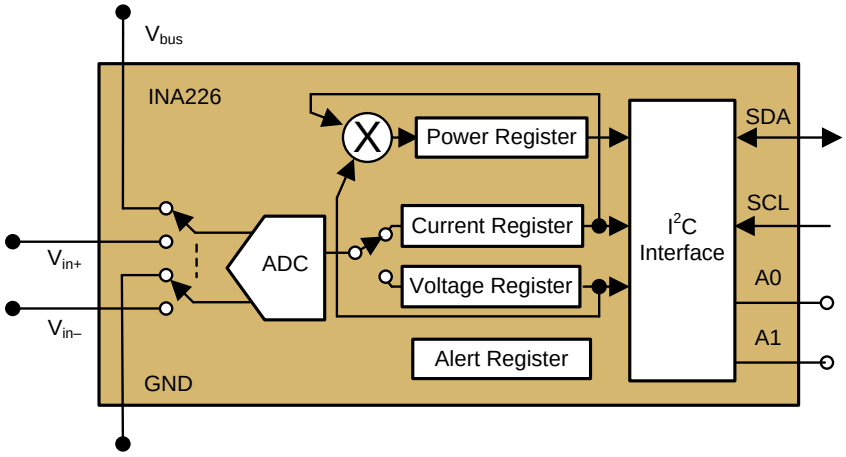

図 12. INA226 Basic Block Diagram

2.3.2 ISO1541

In this design the INA226 device is referenced to the –48-V rail. This task requires a device that is capable of translating a –48-V reference into ground referenced signals. Additional requirements consist of low power consumption, compatibility with I^2C interfaces, and a 3.3-V to 5-V supply voltage range. The device selected for this task is the ISO1541.

The ISO1541 is a low-power, bidirectional I^2C bus isolator. The ISO1541 has its logic input and output buffers separated by TI's capacitive isolation technology using a silicon dioxide (SiO_2) barrier. This isolation technology provides for function, performance, size, and power consumption advantages when compared to optocouplers. The ISO1541 has a bidirectional data and a unidirectional clock channel. The device is compatible with I^2C interfaces and its supply range, 3 V to 5.5 V, meets the supply requirements of this design. 図 13 shows a basic block diagram of ISO1541. For more information about the ISO1541, see *ISO154x Low-Power Bidirectional I^2C Isolators* (SLLSEB6).

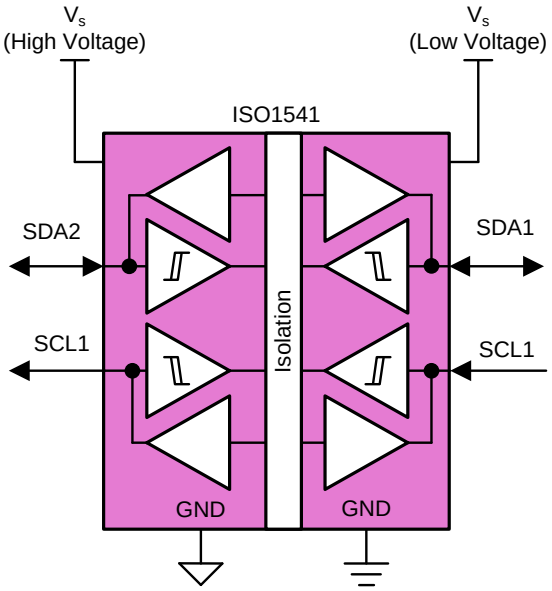

図 13. ISO1541 Block Diagram

3 Hardware, Software, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

The contents of the reference design kit are as follows:

- TIDA-00313 board
- USB SM-DIG Platform PCB
- USB extender cable
- SM-Dig connector ribbon cable

図 14 shows the included hardware.

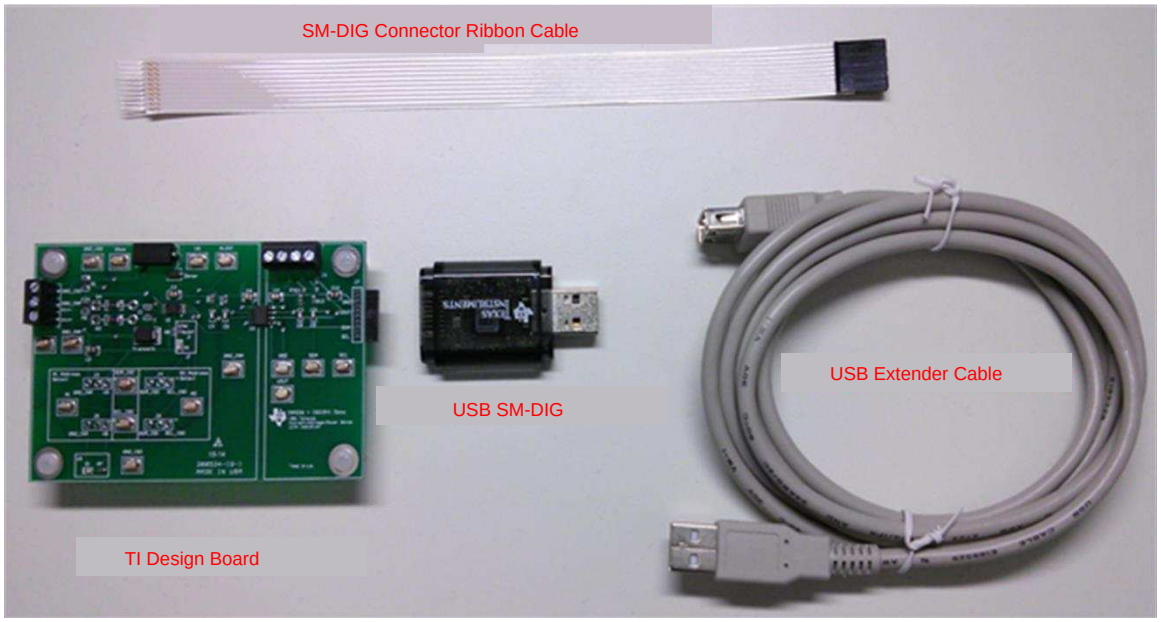

図 14. Required Hardware for TIDA-00313 Evaluation

3.1.1.1 INA226 Telecom Demo Hardware Setup

Connect the INA226 Telecom Demo and the USB SM-DIG Platform together. Make sure that the two connectors are completely pushed together; loose connections may cause intermittent operation. 図 15 shows the board connected to the platform (the Texas Instruments logo should be upside down).

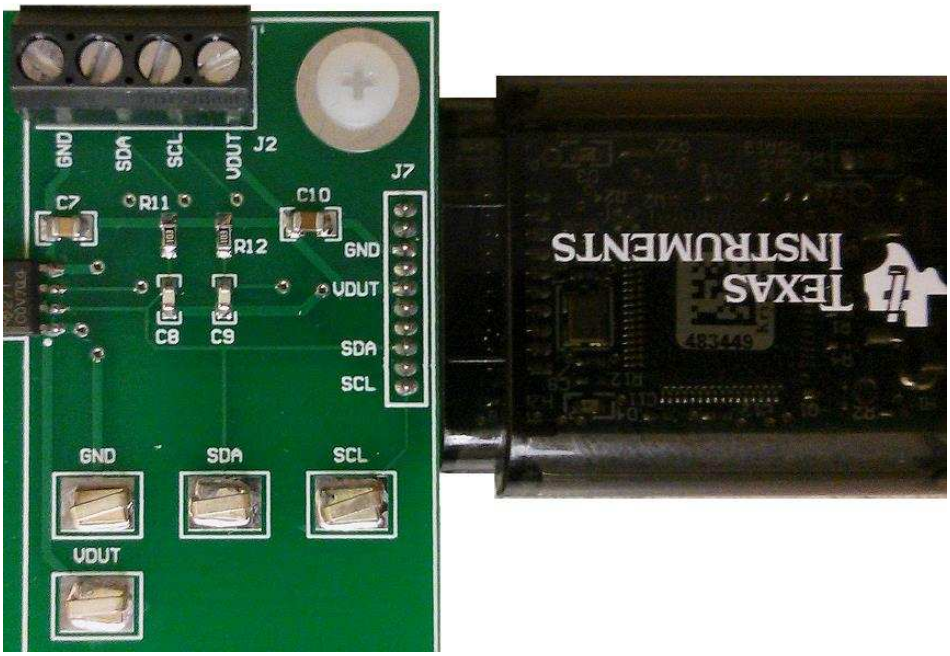

図 15. How to Connect TIDA-00313 Board and USB SM-DIG Platform

After the INA226 Telecom Demo board and SM-DIG are connected as shown in 図 15, connect the desired bus voltage and shunt configuration intended to be measured. For this, connect an external DC power supply of –48 V to the V_{in-} (GND_INA) pin referenced to the GND_ISO pin on terminal block J1. Also, connect a shunt resistor between the V_{in+} and V_{in-} terminals. When connecting a load, attach it to the V_{in+} pin at terminal block J1. See 図 24 for a layer reference.

3.1.1.2 INA226 Telecom Demo Jumper Settings

Jumpers 3 through 6 (J3-J6) control the I^2C address pin for the INA226; these jumpers can set the address for A0 and A1 to either high, low, SCL, or SDA. Make sure to only connect one jumper at a time for each address control; for example, connecting only J3 and not J4. Failure to properly connect jumpers can cause shorts or interruptions in the communication lines. For more information on the INA226 addressing, see *INA226 High-Side or Low-Side Measurement, Bi-Directional Current and Power Monitor with I^2C Compatible Interface* (SBOS547). 表 4 summarizes the function of the TIDA-00313 board jumpers.

表 4. TIDA-00313 Jumper Functions

JUMPER	DEFAULT	PURPOSE
J3/J4	GND	This jumper selects I^2C AO address selection for A0. The designer can select from four separate I^2C addresses depending on whether J3 has been set to high or low or if J4 has been set to SDA or SCL.
J5/J6	GND	This jumper selects I^2C AO address selection for A1. The designer can select from four separate I^2C addresses depending on whether J5 has been set to high or low or if J6 has been set to SDA or SCL.

3.1.1.3 INA226 Telecom Demo Features

This section describes some of the hardware features present on the TIDA-00313 board.

- J3 and J4 – I^2C address hardware setting (A0):

  Use jumper J3 and J4 to configure the hardware settings for the A0 I^2C address pin on the INA226. Using J3, the A0 address can be set to either a logic “1” or a logic “0”. Using J4, the A0 address can be set to either the SCL or SDA communication line. Make sure to only have either J3 or J4 connected individually; failure to keep these lines separate can lead to board shorts and problems with the I^2C communication lines. For more information on how to configure the INA226EVM software to match the J3 and J4 hardware setting, see the section regarding I^2C address selection in *INA226EVM Evaluation Board and Software Tutorial* (SBOU113).

- J5 and J6 – I^2C address hardware setting (A1):

  Use jumper J5 and J6 to configure the hardware settings for the A1 I^2C address pin on the INA226. Using J3, the A1 address can be set to either a logic “1” or a logic “0”. Using J4, the A1 address can be set to either the SCL or SDA communication line. Make sure to only have either J5 or J6 connected individually; failure to keep these lines separate can lead to board shorts and problems with the I^2C communication lines. For more information on how to configure the INA226EVM software to match the J5 and J6 hardware setting, see the section regarding I^2C address selection in *INA226EVM Evaluation Board and Software Tutorial* (SBOU113).

- External I^2C lines and terminal block J2:

  The I^2C communication lines on the TIDA-00313 board are tied to two sources: The internal I^2C communication lines from the SM-DIG (J7) and the terminal block J2. In the event the user wants to add an external signal separate from the SM-DIG, simply disconnect the SM-DIG from the TIDA-00313 board and hook up the required SDA, SCL, and GND lines. Also, remember to apply an external DVDD to the lines that are compatible with the I^2C communication device in use.

3.1.2 Software

A modified version of the INA226EVM software has been released which is only for this demonstration of this reference design. This new version is known as the INA226 Telecom Demo Software and it allows the user to modify the least significant bit (LSB) step size of the bus voltage, a feature not available in the INA226EVM software. The LSB step-size value requires modification due to dividing the bus voltage by 4 (with the voltage divider), which is done to meet the voltage specifications of the INA226 input bus.

Currently, the INA226EVM software uses 1.25 mV as the LSB step size for the bus voltage. The user must note the importance of taking this LSB number and multiplying it by the voltage divider ratio, 4. Failure to property set the LSB step size results in incorrect bus voltage readings.

The new LSB value is 5 mV (see 式 10). This 5-mV value has been set as the default in the INA226 Telecom Demo Software.

$$\text{New\_LSB} = (\text{Vbus\_Divider}) \times (\text{Old\_LSB}) = 4 \times 1.25\ \text{mV} = 5\ \text{mV} \quad (10)$$

where,

- New_LSB: New LSB step size (bus voltage),
- Old_LSB: Old LSB step size (bus voltage),
- Vbus_Divider: V_{bus} voltage divider ratio.

図 16 shows the graphical user interface (GUI) of the INA226 Telecom Demo. Note “Step 7” enclosed in the red-dotted box. This step is not included in the INA226EVM software GUI. Use Step 7 to set the step-size value for the bus voltage LSB. This exclusion is the only modification that has been made to the INA226EVM GUI. For software configuration and GUI instructions, see *INA226EVM Evaluation Board and Software Tutorial* (SBOU113).

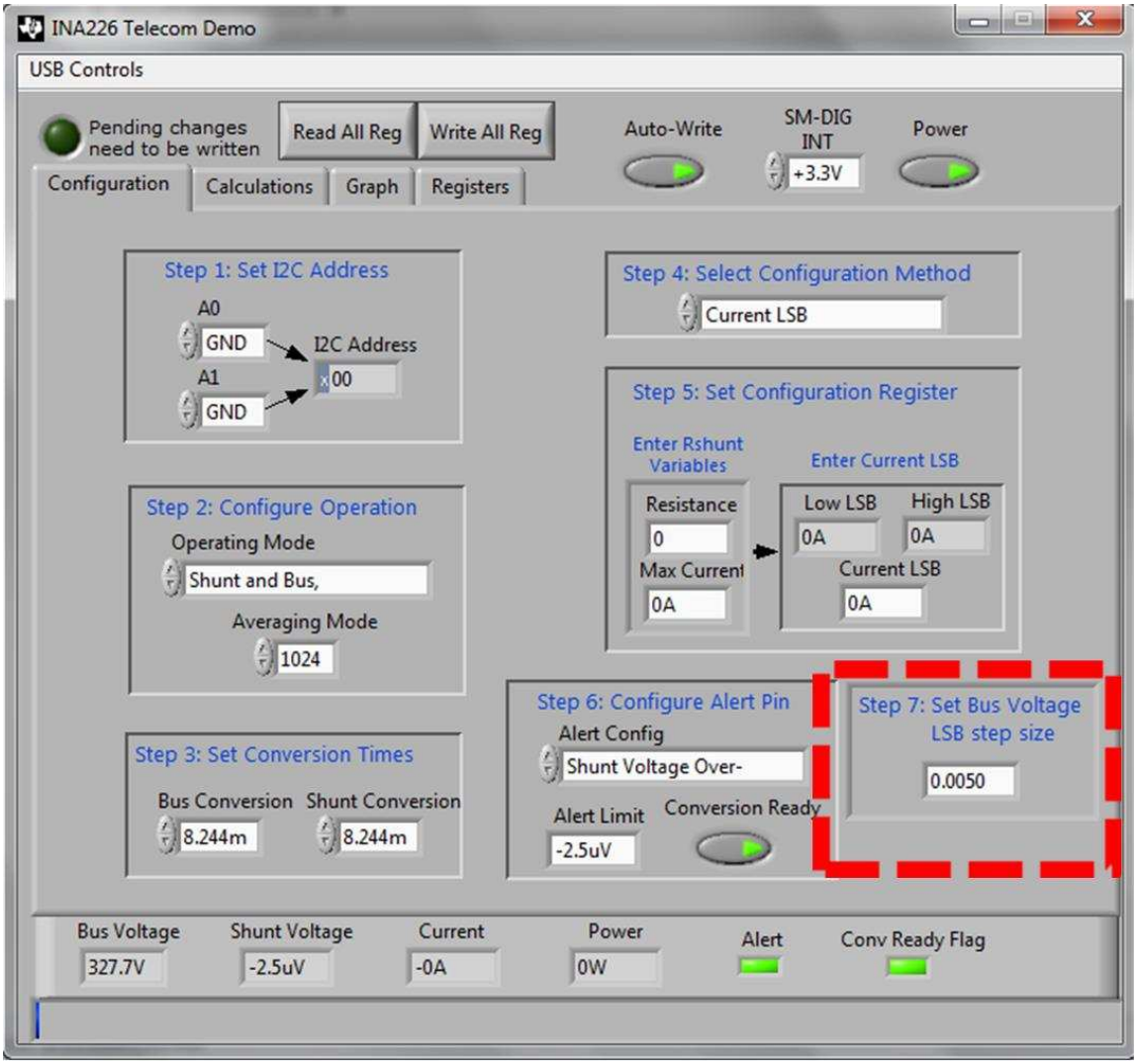

図 16. INA226 Telecom Demo GUI

No simulation models are available for the INA226 device, so it is currently not possible to simulate the full functionality of the system.

3.2 Testing and Results—Measuring System DC Transfer Function

3.2.1 Data Collected With R_{shunt} = 100 mΩ and I_{load} = 50 mA to 750 mA

Data was collected by sweeping the load current from *50 mA to 750 mA* and measuring the shunt voltage of the INA226 device across a 100-mΩ shunt resistor. 表 5 shows the collected data. $Vshunt_{REAL}$ is the actual differential voltage that is applied to the differential input and a precision voltmeter measures this voltage at the inputs of the INA226 device. $Vshunt_{INA226}$ is the V_{shunt} reported by the INA226 device.

The relative error has been calculated using 式 11.

$$\%\text{Reletive\_Error} = \frac{\text{Vshunt}_{\text{REAL}} - \text{Vshunt}_{\text{INA226}}}{\text{Vshunt}_{\text{REAL}}} \times 100 \quad (11)$$

表 5. Data Collected With R_{shunt} = 100 mΩ and I_{load} = 50 mA to 750 mA

R_{SHUNT} (mΩ)	LOAD CURRENT (mA)	$VSHUNT_{REAL}$ (mV)	$VSHUNT_{INA226}$ (mV)	% ERROR
100	50	4.96	4.94	0.403
100	100	10.13	10.11	0.197
100	150	15.29	15.26	0.196
100	200	20.45	20.42	0.147
100	250	25.61	25.59	0.078
100	300	30.78	30.76	0.065
100	350	35.94	35.91	0.083
100	400	41.11	41.07	0.097
100	450	46.27	46.25	0.043
100	500	51.43	51.39	0.078
100	550	56.6	56.59	0.018
100	600	61.78	61.77	0.016
100	650	66.97	66.95	0.030
100	700	72.13	72.11	0.028
100	750	77.29	77.3	0.013

図 17 shows the calculated relative error and 図 18 shows the transfer function.

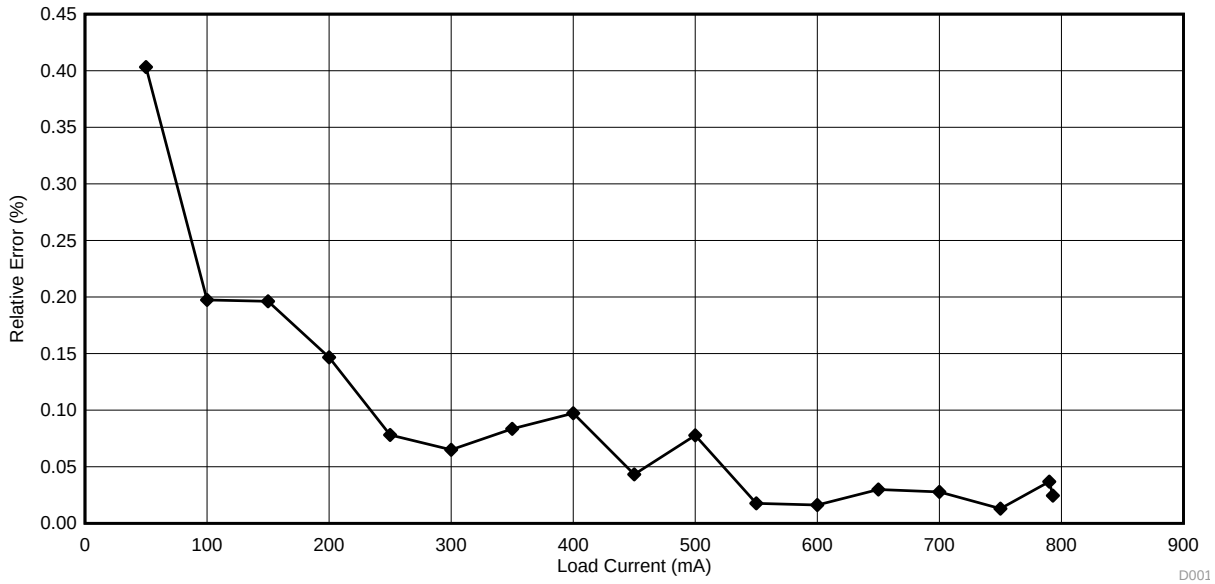

図 17. Measured Relative Error With R_{shunt} = 100 mΩ and I_{load} = 50 mA to 750 mA

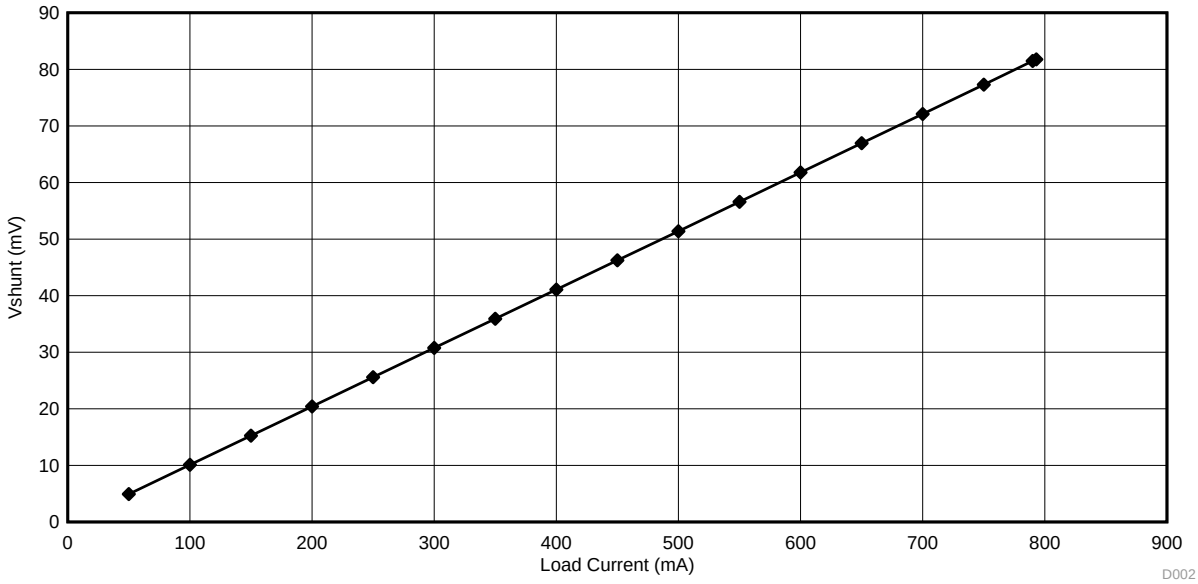

図 18. Measured DC Transfer Function (V_{shunt} vs I_{IN}) With R_{shunt} = 100 mΩ and I_{load} = 50 mA to 750 mA

3.2.2 Data Collected With R_{shunt} = 100 mΩ and I_{load} = –50 mA to –750 mA

A new set of data was collected by sweeping the load current from *–50 mA to –750 mA* and measuring the shunt voltage of the INA226 device across a 100-mΩ shunt resistor. 表 6 shows the collected data.

表 6. Data Collected With R_{shunt} = 100 mΩ and I_{load} = –50 mA to –750 mA

R_{SHUNT} (mΩ)	LOAD CURRENT (mA)	$VSHUNT_{REAL}$ (mV)	$VSHUNT_{INA226}$ (mV)	% ERROR
100	–50	–4.95	–4.93	0.404
100	–100	–10.53	–10.56	0.285
100	–150	–15.69	–15.73	0.255
100	–200	–20.84	–20.89	0.240
100	–250	–26.01	–26.07	0.231
100	–300	–31.17	–31.23	0.192
100	–350	–36.33	–36.4	0.193
100	–400	–41.5	–41.55	0.120
100	–450	–46.66	–46.73	0.150
100	–500	–51.83	–51.89	0.116
100	–550	–57.01	–57.05	0.070
100	–600	–62.17	–62.24	0.113
100	–650	–67.33	–67.42	0.134
100	–700	–72.51	–72.61	0.138
100	–750	–77.78	–77.86	0.103

図 19 shows the calculated relative error and 図 20 shows the transfer function.

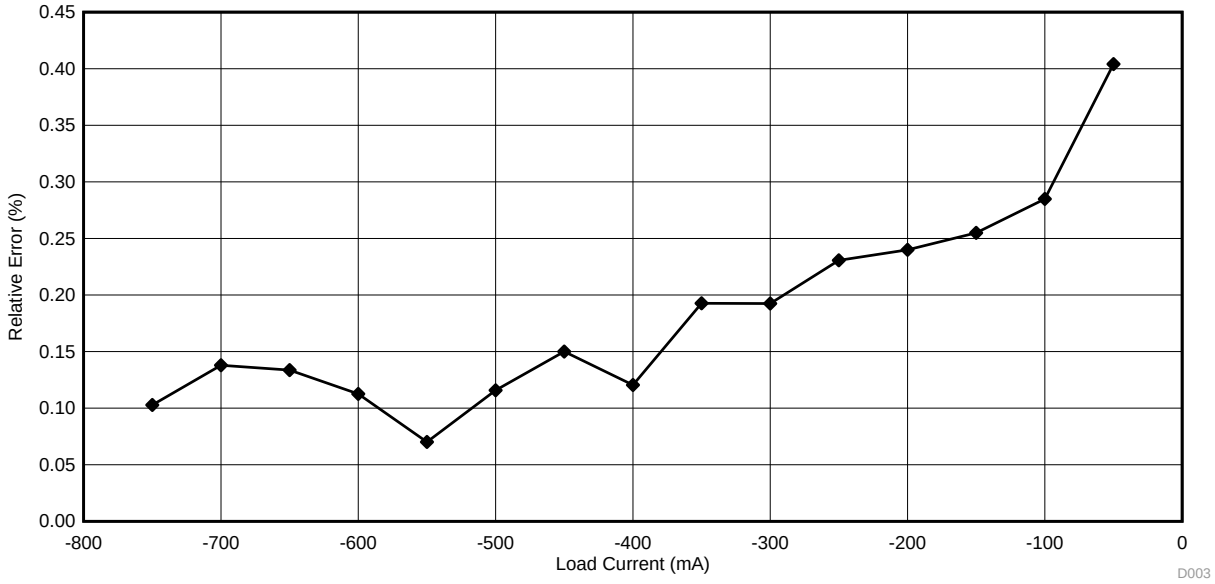

図 19. Measure Relative Error With R_{shunt} = 100 mΩ and I_{load} = –50 mA to –750 mA

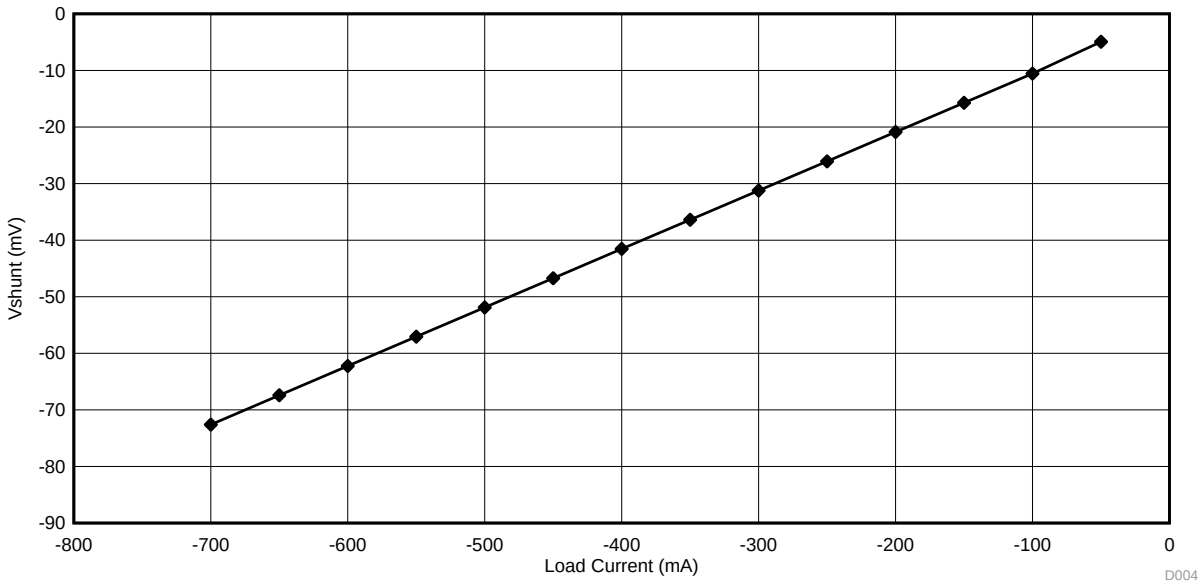

図 20. Measured DC Transfer Function (V_{shunt} vs I_{IN}) With R_{shunt} = 100 mΩ and I_{load} = –50 mA to –750 mA

3.3 Maximum Shunt Voltage Error Analysis

To set the design goals, the main influences of maximum shunt voltage errors are identified as follows:

- Input offset voltage (V_{os}) of the INA226
- Shunt voltage gain error
- Common-mode rejection (CMR) of the INA226
- Power supply rejection (PSR) of the INA226
- Input offset current (I_{os})
- Shunt resistor tolerance

3.3.1 Errors at Small Values of Load Current

When the load current is small, there is a corresponding small input voltage to the INA226. Thus, errors will be dominated primarily by the input-offset-related errors. Determining the errors associated with each parameter is straightforward and the following subsections address this process.

3.3.2 Initial Offset Voltage Error

Take the maximum error due to input offset voltage directly from the INA226 device specification. The maximum input offset voltage is given as 10 µV at 25°C. This error is calculated with respect to the ideal voltage across the shunt (V_{shunt}). The ideal shunt voltage is the product of the load current and ideal shunt resistor value. The system nominal current is 50 mA and the ideal shunt resistor value is 100 mΩ (see 式 12).

$$e_{V_{os}} = \frac{V_{os(max)}}{V_{shunt}} \times 100 = \frac{V_{os(max)}}{I_{load} \times R_{shunt}} \times 100 = \frac{10\ \mu V}{50\ mA \times 100\ m\Omega} \times 100 = 0.20\% \quad (12)$$

3.3.3 Initial CMR Error

Calculate the maximum input offset error due to the common-mode rejection of the INA226 by determining the actual common-mode voltage as applied to the INA226 with a reference to the ground pin of the INA226. The INA226 device specification gives the common-mode rejection ratio minimum as 126 dB (0.501 µV/V). The offset voltage in the data sheet is specified with a common-mode voltage that is 12 V higher than what is known as GND_INA, –48 V. This means that the datasheet specification of 12-V bus voltage is the same as –36 V in this application, $V_{cm\text{-}pds}$ = –36 V. The resulting common-mode error is determined as calculated in 式 13:

$$e_{CMRR} = \frac{\left(\left|V_{cm-pds} - V_{cm-sys}\right|\right) \times CMRR_{INA226}}{V_{shunt}} \times 100 = \frac{\left(\left|-36\ V - (-48\ V)\right|\right) \times 0.501 \frac{\mu V}{V}}{50\ mA \times 100\ m\Omega} \times 100 = 0.120\% \quad (13)$$

3.3.4 Initial PSR Error

Error due to power supply rejection ratio (PSRR) can be calculated in a manner similar to common-mode rejection ratio (CMRR). The INA226 device specification gives the specified power supply voltage for the input offset voltage specification as 3.3 V. Any deviation from 3.3 V applied between the INA226 V+ pin and ground pin results in an additional error. The INA226 device specification gives the PSRR minimum as 2.5 µV/V. 式 14 calculates the PSR error:

$$e_{PSRR} = \frac{\left(\left|V_{s-pds} - V_{s-sys}\right|\right) \times PSRR_{INA226}}{V_{shunt}} \times 100 = \frac{\left(\left|3.3\ V - (-4.7\ V)\right|\right) \times 2.5 \frac{\mu V}{V}}{50\ mA \times 100\ m\Omega} \times 100 = 0.07\% \quad (14)$$

3.3.5 Input Bias Current Error

The input bias current is given as 10 µA at 25°C. This error is calculated with respect to the ideal voltage across the shunt (V_{shunt}). The ideal shunt voltage is the product of the load current and ideal shunt resistor value. The system nominal current is 50 mA and the ideal shunt resistor value is 100 mΩ.

$$e_{I_B} = \frac{I_B \times R_{shunt}}{V_{shunt}} \times 100 = \frac{10\,\mu A \times 100\,m\Omega}{50\,mA \times 100\,m\Omega} \times 100 = \frac{1\,\mu V}{5\,mV} \times 100 = 0.02\% \quad (15)$$

3.3.6 Shunt Voltage Gain Error

The INA226 device specification gives the shunt voltage gain error as 0.1%.

3.3.7 Total Error at Small Currents

式 16 calculates the worst-case total error at small load currents.

$$e_{total-worst-case}(\%) = \sum_1^n e_n = 0.20 + 0.120 + 0.07 + 0.02 + 0.1 = 0.510\% \quad (16)$$

3.3.8 Errors at Large Values of Load Current

At large load currents, the input voltage that develops across the shunt resistor will be at its maximum. This condition minimizes the percentage contribution of the errors from the previously-described initial error sources. The dominant errors sources for large inputs are:

- Shunt voltage gain error from the INA226
- Shunt resistor accuracy

3.3.9 INA226 Shunt Voltage Gain Error

The INA226 device specification gives the shunt voltage gain error as 0.1%.

3.3.10 Shunt Resistor Error

The assumption in this design is that the shunt resistor tolerance (accuracy) is 1.0%; however, disregard this value because the differential voltage that is reported in the previous results has been measured at the inputs of the INA226 with a precision voltmeter. Measuring at the inputs of the INA226 eliminates the shunt resistor error contribution in these results.

3.3.11 CMR, PSR, and V_{os} Errors

The total error at a large load current also include the errors due to CMR, PSR, V_{os}, and input bias current with respect to the maximum load current (750 mA). 式 17, 式 18, and 式 19 calculate the errors as follows:

$$e_{CMRR} = \frac{\left(\left|V_{cm-pds} - V_{cm-sys}\right|\right) \times CMRR_{INA226}}{V_{shunt}} \times 100 = \frac{\left(\left|-36\ V - (-48\ V)\right|\right) \times 0.501\frac{\mu V}{V}}{750\ mA \times 100\ m\Omega} \times 100 = 0.0080\% \quad (17)$$

$$e_{PSRR} = \frac{\left(\left|V_{s-pds} - V_{s-sys}\right|\right) \times PSRR_{INA226}}{V_{shunt}} \times 100 = \frac{\left(\left|3.3\ V - 4.7\ V\right|\right) \times 2.5\frac{\mu V}{V}}{750\ mA \times 100\ m\Omega} \times 100 = 0.0047\% \quad (18)$$

$$e_{I_B} = \frac{I_B \times R_{shunt}}{V_{shunt}} \times 100 = \frac{10\,\mu A \times 100\,m\Omega}{I_{load} \times R_{shunt}} \times 100 = \frac{1\,\mu V}{750\,mA \times 100\,m\Omega} \times 100 = 0.0013\% \quad (19)$$

3.3.12 Total Error at High Currents

式 20 calculates the worst-case total error at high load currents.

$$e_{total-worst-case}(\%) = \sum_{1}^{n} e_n = 0.1 + 0.0080 + 0.0047 + 0.0013 = 0.1140\% \quad (20)$$

3.4 Measured Results Summary

表 7 summarizes the measured performance results.

表 7. Measured Performance Results

RELATIVE ERROR	GOAL	MEASURED
I_{load} = 50 mA	0.510%	0.403%
I_{load} = –50 mA	0.510%	0.404%
I_{load} = 750 mA	0.114%	0.013%
I_{load} = –750 mA	0.114%	0.103%

3.5 V_{bus} Range

The targeted bus voltage for this reference design was –48 V. The results shown in 表 5 and 表 6 prove that, while using this TIDA-00313 board, the INA226 device is able to collect data at the –48-V rail. The V_{bus} range was verified by sweeping the bus voltage from 0 V to –50 V. Results showed that the INA226 is not able to collect data with V_{bus} values from 0 V to –7 V. At this voltage range, the potential generated by the voltage drop across the Zener diode is not enough to power the device. Using this TIDA-00313 board the INA226 device is able to measure bus voltage and shunt voltage when the V_{bus} is –8 V to –50 V, which 図 21 shows.

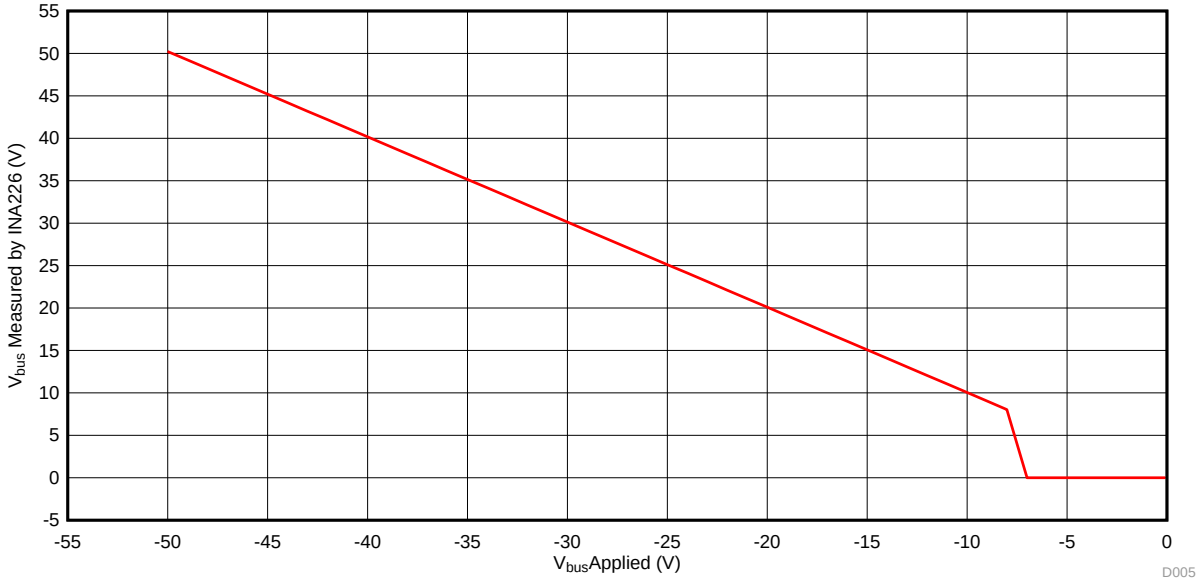

図 21. V_{bus} Range Accepted by TIDA-00313 Board

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00313.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00313.

4.3 PCB Layout Prints

The two-layer printed circuit board (PCB) used in this design measures 3.54 in × 2.33 in. The PCB layout adheres to the following guidelines:

1. The input signal has a simple and clean path to the INA226, V_{in+}, and V_{in-} pins (see 図 22). The terminal block J1 for the input current and power supply share a common ground (GND_ISO) connection at the left side of the board. This shared connection shortens the path of the load current on the PCB.

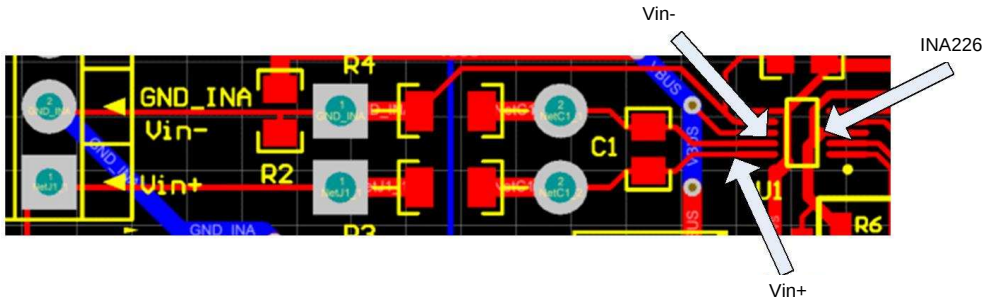

図 22. INA226 Path for Input Pins

2. The power supply bypass capacitors are placed close to the supply pins of the device (see 図 23).

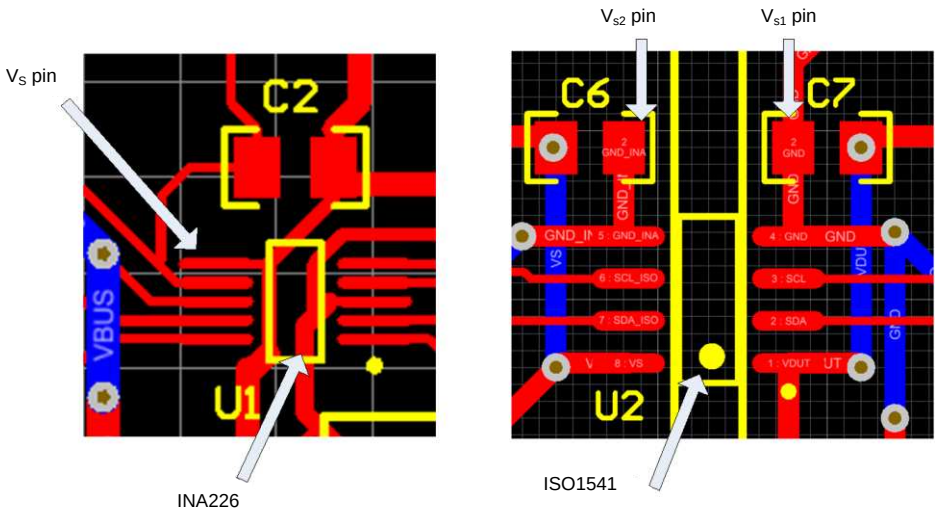

図 23. Bypass Capacitors

3. The terminal block J7 has all the connections required for the SM-USB-DIG device and is located in close proximity to the ISO1541 SDA, SCL, V_s, and GND low-voltage side pins. Some users may desire to use an alternate I^2C interface communication and supply voltage. For this purpose, another block terminal, J2, has been placed near the ISO1541 low-voltage side pins.

4. The board should have two ground sides: one ground side for the high-voltage connections (–48 V) and the other side for the USB DIG low-voltage connections. The board has been divided in two sections and marked with silkscreen boundaries (see 図 24).

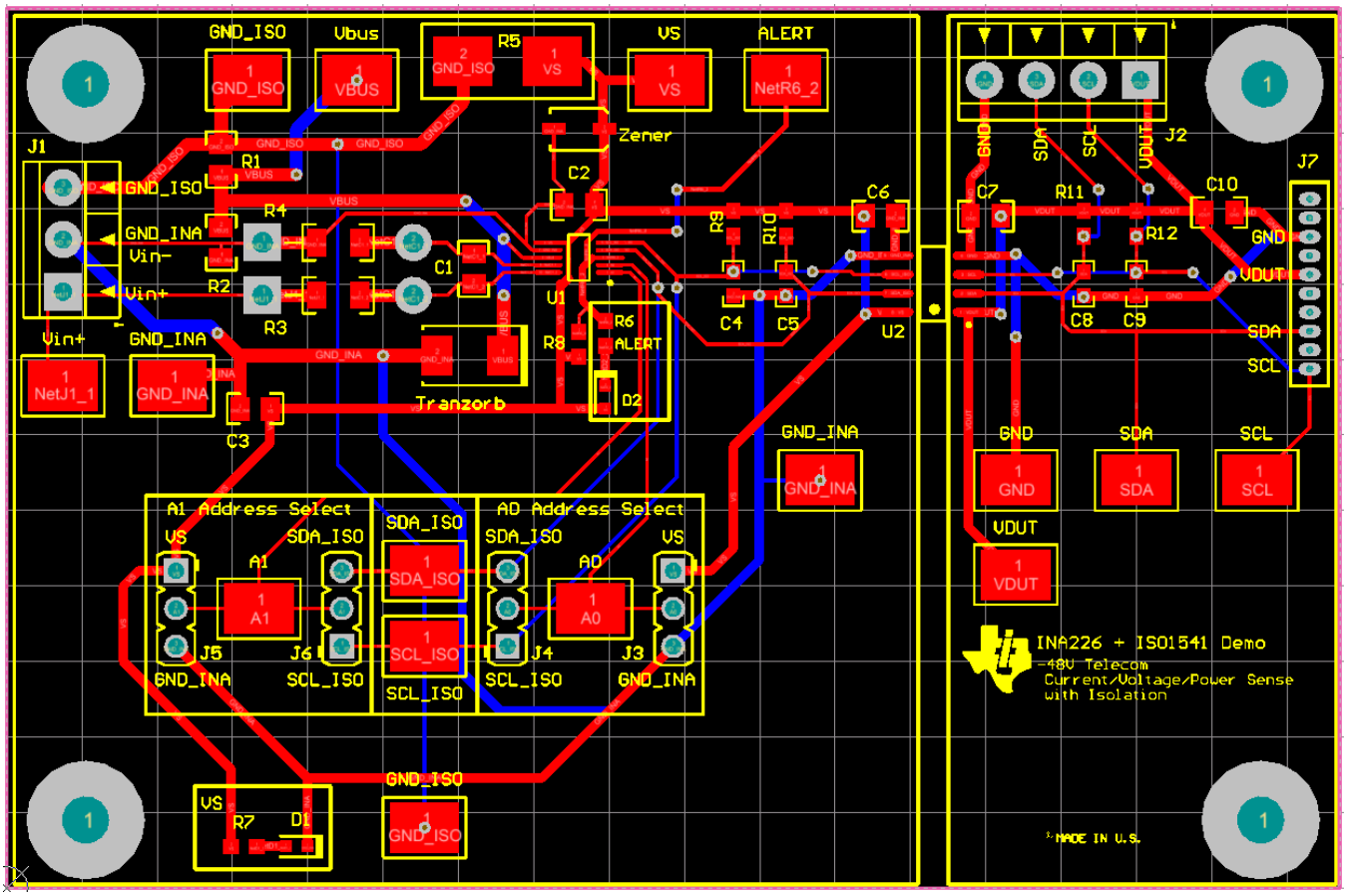

図 24. PCB Layout

To download the layer plots, see the design files at TIDA-00313.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-00313.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00313.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00313.

5 Related Documentation

1. EETimes.com, Semig, Peter; Wells, Collin; *A Current Sensing Tutorial* Parts 1-4, Design How-To (http://www.eetimes.com/design/industrial-control)
2. Texas Instruments, *INA226 High-Side or Low-Side Measurement, Bi-Directional Current and Power Monitor with I²C Compatible Interface*, INA226 Data Sheet (SBOS547)
3. Texas Instruments, *SM-USB-DIG-Platform*, User's Guide (SBOU098)
4. Texas Instruments, *INA226EVM Evaluation Board and Software Tutorial*, INA226EVM User's Guide (SBOU113)
5. Texas Instruments, *ISO154x Low-Power Bidirectional I²C Isolators*, ISO154x Data Sheet (SLLSEB6)
6. Texas Instruments, *Power: Telecom DC/DC Module: Analog*, TI Applications Page
7. Texas Instruments, *Getting Started with Current Sense Amplifiers*, TI Current Sense Amplifier Video Training Series

5.1 商標

6 About the Author

MAYRIM VERDEJO is an applications engineer at Texas Instruments where she supports current shunt monitors and temperature sensors. Mayrim graduated from the University of Puerto Rico, Mayagüez where she earned a Bachelor of Science in Electrical Engineering with emphasis on Digital Signal Processing.

7 Acknowledgments

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改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2014年9月発行のものから更新 **Page**

- タイトルを「*絶縁付きの-48Vテレコム用電流/電圧/電力検出*」から「*絶縁付きの-48Vテレコム用電流、電圧、電力検出のリファレンス・デザイン*」に更新 1
- 表紙のブロック図を更新(技術的な変更なし) 1
- 表紙の「*TI Designs - 高精度*」セクションを「*概要*」セクションに置き換え 1
- *特長* 追加 1
- *アプリケーション* セクション 追加 1
- Reorganized content into updated document flow 2
- *Key System Specifications* table 追加 2
- Updated 図 2 3
- Updated 図 3 4
- Updated 図 10 10
- Updated 図 11 10
- Updated 図 12 11
- Updated 図 13 12
- title of *Input Offset Current Error* section to *Input Bias Current Error* 変更 22
- Item 3 to *Related Documentation* 追加 26
- Item 7 to *Related Documentation* 追加 26

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お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

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TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。