参考資料

TI Designs: TIDA-01002
YUV422出力フォーマットでFPD-Link IIIとPoC (Power over Coax)を使用する車載用1MPカメラ・モジュールのリファレンス・デザイン

概要

このリファレンス・デザインでは、ADAS (先進運転支援システム)およびインフォテインメント・システムで使用するための、非圧縮1MP、HDR (High Dynamic Range) YUV422ビデオを提供します。このデザインは、TIのFPD-Link III SerDesテクノロジと、ON Semiconductor®のAS0140AT CMOS (相補型金属酸化膜半導体)イメージャを使用して、ビデオ・データ、双方向の制御信号、および電力のすべてを、1本の同軸ケーブルで伝送します。このデザインは、サラウンド・ビュー・システム、後方視野カメラ、またはアナログやイーサネット・カメラの代替品として使用できます。

リソース

TIDA-01002	デザイン・フォルダ
DS90UB913A-Q1	プロダクト・フォルダ
TPS62170-Q1	プロダクト・フォルダ
TPS62171-Q1	プロダクト・フォルダ

TI E2E™ Community

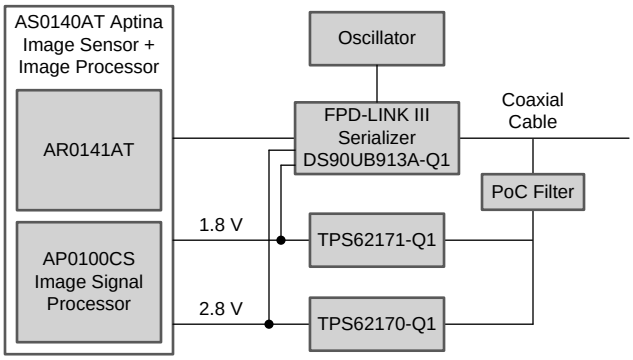
E2E™エキスパートに質問

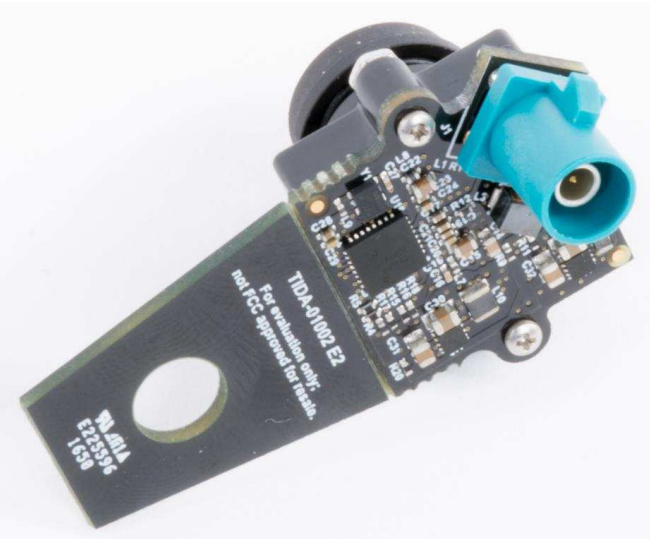
特長

- 1枚の20×20mmのPCBに搭載された省スペースのデザイン
- スイッチ・モード電源のみを使用した高効率電源
- YUV422 720pを最大30fpsで出力するモジュール
- 単一のRosenberger Fakra製の同軸コネクタで、デジタル・ビデオ、電力、制御、診断信号を伝送
- 設計上の考慮事項と部品表(BOM)分析が付属

アプリケーション

- サラウンド・ビュー・システム
- ADASビジョン・システム
- 後方視野カメラ
- スマート・ミラー





1 System Description

For many automotive safety systems, small camera modules that provide low-latency, uncompressed video are required. This reference design addresses these requirements by combining a 1-MP imager with an integrated image signal processor, a 1.4 Gbit/s serializer, and a necessary power supply for the two to provide uncompressed, displayable 720-p resolution at up to 30-fps video data. This functionality is contained on a 20-mm × 20-mm circuit card. The only connection required by the system is a single 50-Ω coaxial cable.

This camera module is intended to be used as either a rearview camera, a camera in a surround view system, or as a replacement for an analog camera module. An added feature to this design is that the integrated image signal processor performs the color-space conversion and distortion correction necessary to display video. In short, the output is an uncompressed, readily-displayed video feed, which frees up processing of an onboard processor. Analog and Ethernet cameras cannot provide uncompressed, low-latency displayable video without extra processing. 図 1 shows the block diagram of the design.

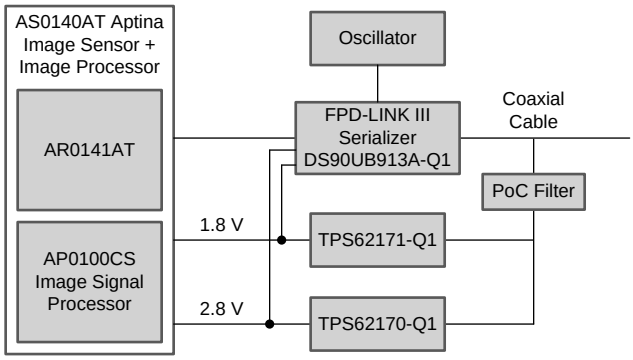


図 1. Camera Block Diagram

As shown in 図 1, the combined signal, which contains the FPD-Link front and back channels and DC power, enters the board from a coaxial cable through the FAKRA coax connector. The PoC filter shown in 図 2 blocks all of the high-speed content of the signal, without significant attenuation, while allowing the DC portion of the signal to pass through inductor L3.

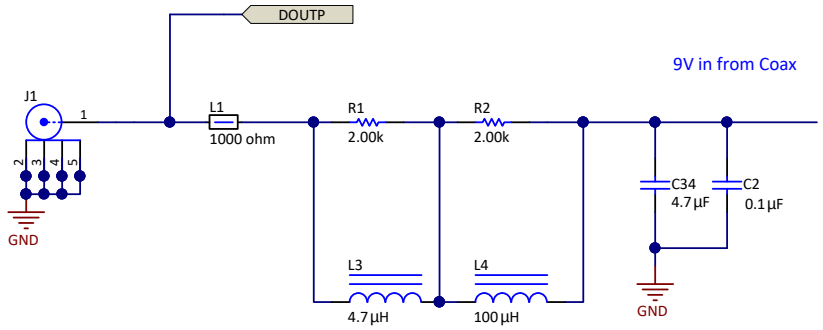


図 2. FPD-Link III Signal Path

The DC portion connects to the input of the TPS62170-Q1 and TPS62171-Q1 buck converters to output 2.8 V and 1.8 V. The high-frequency portion of the signal connects to the serializer through an AC coupling capacitor to block out any DC. The video data and control back channel transmits through the AC coupling capacitors and coaxial cable between the serializer and deserializer. The output of the CMOS imager connects to the serializer through a parallel digital video interface. The serializer converts the video data to a single, high-speed serial stream that is transmitted over a single low-voltage differential signaling (LVDS) pair to a deserializer located on the other end of the coax cable. On the same coax cable, there is separate low-latency, bidirectional control channel that transmits control information from an I^2C port. This control channel is independent of video blanking period and is used by the system microprocessor to configure and control both the imager and serializer.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage	Power over coax	5	9	14.5	V
P_{TOTAL}	Total power consumption	VPOC = 12 V		0.7	1.1	W
F_{sw}	Switching frequency	AM avoidance	1.8			MHz
F_{PCLK}	Pixel clock frequency		25		100	MHz

2 System Overview

2.1 Block Diagram

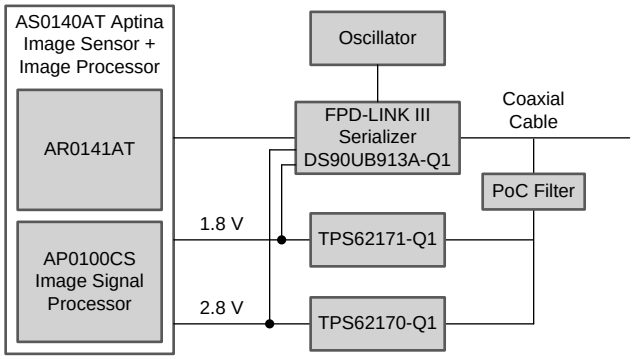


図 3. Block Diagram of TIDA-01002

2.2 Highlighted Products

This design uses the following TI products:

- The *DS90UB913A-Q1* is the serializer portion of a chipset that offers a FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coaxial cable or differential pair. This chipset incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer and deserializer pair is targeted for connections between imagers and video processors in an electronic control unit (ECU).
- The *TPS62170-Q1* is an automotive-qualified step-down DC converter optimized for applications with high-power density. A typical switching frequency of 2.25 MHz allows the use of small inductors and provides fast transient response.
- The *TPS62171-Q1* is the 1.8-V fixed-output version of the TPS62170-Q1.

The ON Semiconductor AS0140AT ¼-inch CMOS image sensor and signal processor is the sensor and processor used in this design.

More information on each device and why they were chosen for this application follow in the next sections.

2.2.1 AS0140AT Imager Plus ISP

Available from ON Semiconductor, this device has both the AR0140AT imager and AP0100AT image signal processor conveniently available in one single package. It contains a ¼-inch 1-MP CMOS imager with high dynamic range (HDR) and YUV422 8-bit, 10-bit, or 10- to 12-bit tone-mapped Bayer output data formats. There is also a fully programmable spatial transform engine (STE) which can perform spatial transforms and eliminate the requirement for an expensive digital signal processor (DSP) for lens distortion correction. This sensor-processor combination package is suitable for automotive viewing systems. Some additional features of the imager are:

- Supports image sizes 1280 × 800 and 720-p (16:9) images
- 45 fps at 1 MP, 60 fps at 720 p
- 50-Hz and 60-Hz auto-flicker detection and avoidance
- Superior low-light performance

- Configured using I^2C

2.2.2 DS90UB913A-Q1

Using a serializer to combine video data with a bidirectional control signal onto one coax or a twisted pair greatly simplifies system complexity, cost, and cabling requirements. The parallel video input of the DS90UB913A-Q1 combines with the 12-bit parallel output of the AS0140AT imager. When combined with the power over coax (PoC) filter, video, I^2C control, diagnostics, and power can all be transmitted up to 15 meters on a single, inexpensive coax cable. For more information on the cable itself, see the cable requirements in the *Cable Requirements for the DS90UB913A & DS90UB914A Application Report*[4].

2.2.3 TPS62170-Q1

To keep the camera small, the power supply must be small. The power supply must also be power efficient while not adding measurable noise to the video from the imager. Often, these two requirements stand in opposition. A switching power supply is more efficient than a linear regulator, but a switching power supply can add noise to the system and size to the discrete components in the solution.

It is important to avoid interfering with the AM radio band and camera sensor circuits, which are usually sensitive to noise at frequencies below 1 MHz. To avoid interference with the AM radio band and camera sensor circuits, staying above 1.8 MHz is desirable. The TPS62170-Q1 switching regulator operating at 2.25 MHz will meet both requirements, switching above 1.8 MHz. This high-switching frequency also helps reduce the size of the discrete components in the circuit.

The image sensor and serializer have a few power sequencing requirements. Fortunately, both the imager and serializer require that the 2.8-V rail must be on before the 1.8-V rail, and finally the serializer will require an active-high signal on its power down bar (PDB) pin to come out of reset once the 1.8-V rail has stabilized. The power good (PG) signals from the switchers will provide the proper power sequencing for both the imager and serializer.

2.2.4 TPS62171-Q1

This device is the 1.8-V fixed-output version of the TPS62170-Q1. Because the device is fixed output, there is no resistor feedback network. The external component count is reduced and total solution size decreases, which is desirable with such tight board size requirements.

To meet the sequencing requirement, the enable pin of the TPS62171-Q1 will receive the PG signal from the TPS62170-Q1 once the 2.8-V rail has stabilized. The device will then transmit a PG signal to the serializer to pull it out of reset once the 1.8-V rail is stable.

2.3 System Design Theory

2.3.1 PCB and Form Factor

This design was not intended to fit any particular form factor. The only goal of the design with regards to the PCB was to make as compact a solution as possible. The square portion of the board is 20 mm × 20 mm. The area near the board is used for attaching the optics housing that holds the lens with screws.

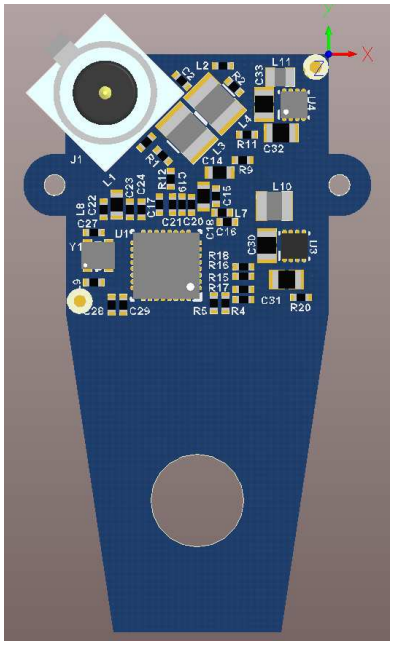


図 4. PCB Top View

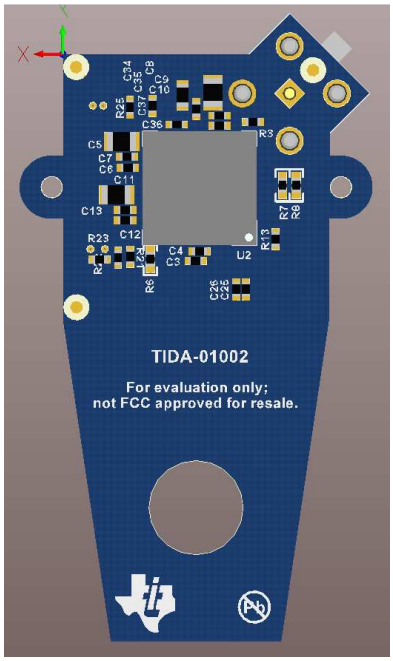


図 5. PCB Bottom View

The mounting tab on the bottom of the board allows for easy mounting to tripods through the ¼-inch screw hole. This tab has no circuitry and is only intended to be used for mounting. It can be removed if desired. 図 6 shows the mounting of the board to a tripod.

図 6. Mounted Board

2.3.2 Power Supply Design

Because this design is targeted at automotive applications, there are few considerations that constrict the design choices. In addition, there are systems-level specifications which shaped the design.

- The total solution size must be minimized to meet the size requirement, which is less than 20 mm × 20 mm. Parts that integrate FETs, diodes, compensation networks, and feedback resistor dividers to eliminate external circuitry should be chosen.
- The input voltage range is 5 V to 14.5 V (9 V nominal).
- To avoid interference with the AM radio band, all switching frequencies must be greater than 1800 kHz or lower than 540 kHz. Lower switching frequencies are less desirable in this case because they require large inductors and can still produce harmonics in the AM band. For this reason higher frequency switchers, above 1.8 MHz, are desirable.
- All devices must be advanced embedded control (AEC) Q100 (-Q1) rated.
- Efficiency is important insofar as to keep the total power budget below 1 W. Efficiency can be balanced with size and cost, but 1 W is a good number stay below. Though the system will be quite low-power, it is also an extremely small board in a hot environment.

Before choosing parts, the input voltage range, required rails, and current required by each rail must be known. The input voltage is a pre-regulated 9-V supply coming in over coax. The range is discussed later, but this is the nominal value. The system has only two main integrated circuits (ICs), which will consume the majority of the power. 表 2 shows requirements for each supply on these devices.

表 2. Power Budget

PARAMETER	VOLTAGE (V)	CURRENT (TYP) (A)	CURRENT (MAX) (A)	POWER (TYP) (W)	POWER (MAX) (W)
DS90UB913A-Q1					
VDDT	1.8	0.061	0.08	0.1098	0.144
VDDIO	2.8	0.005	0.008	0.0027	0.0054
ON AS0140AT					
VDD_1V8	1.8	0.2313	0.46	0.41634	0.828
VDDA_DAC	2.8	0.0001	0.0003	0.00028	0.00084
VDDIO_2V8	2.8	0.0329	0.06	0.09212	0.168
VAA_2V8	2.8	0.0405	0.07	0.1134	0.196
RAIL TOTAL					
	1.8	0.2923	0.548	0.52884	0.9864
	2.8	0.0785	0.1383	0.2085	0.38724
TOTAL POWER					
				0.73734	1.37364

Summing these values, the 1.8-V rail requires 292 mA and the 2.8-V rail requires 78.5 mA. If later chosen to cascade these power supplies, the 2.8-V regulator must source the current for the 1.8-V rail as well. These calculations neglect the consumption of passive components, oscillators, IC quiescent currents, but is a good ballpark number.

With the input and output voltages, output current requirements, and typical total power consumption, nominal input currents can be calculated as 式 1.

$$P_{out} = P_{in} = I_{in} \times V_{in} \rightarrow 737\ mW = I_{in} \times 9\ V \rightarrow I_{in} = 81.88\ mA\ (Typ) \quad (1)$$

These numbers give a good starting point for selecting the parts and topology for the regulators, as well as the inductor selections later on. However, this calculation does not take into account the efficiencies of the power supplies.

As previously mentioned, the parts in the power supply must be Q100 rated, switch above the AM band, and satisfy the voltage and current requirements listed above. Because the input voltage is a regulated voltage that will always be greater than any of the power rail requirements, choose from step down converters and low-dropout regulators (LDOs) only. However, keep in mind that in some situations a designer may sacrifice the efficiency in order to avoid the inherent noise and electromagnetic interference (EMI) issues associated with switching power supplies.

The key feature of the system is the small size so integration of external circuitry is a high priority. Integrating FETs, compensation networks, and sometimes feedback can significantly reduce total solution size. Many of the buck regulators integrate everything but the input and output caps and the inductor into very small packages. With high integration, efficiency loss across different operating points can occur. However for this design, some efficiency was sacrificed for size and simplicity. Ultimately this design uses two device families: the TPS621x0 and the TPS6223x. Both of these device families have high integration of external circuitry and high efficiency.

2.3.2.1 TPS62170-Q1

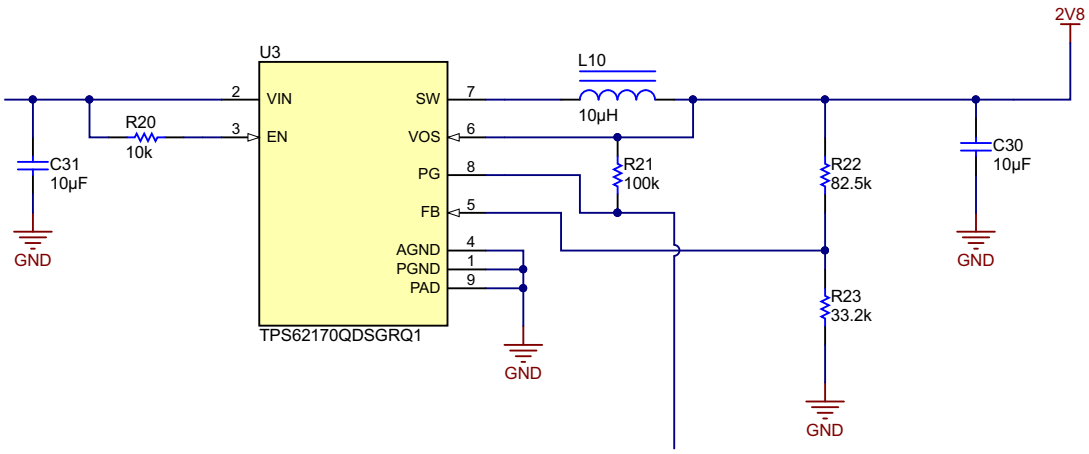


図 7. 2.8-V Supply Schematic

More component selection and design theory can be found in the application section of the *TPS6217x-Q1 3-V to17-V 0.5-A Step-Down Converters with DCS-Control™ Data Sheet*[2].

2.3.2.1.1 Calculating the Output Inductance

As mentioned above, it is required in this design that the switching frequency of the converter remains above 1.8 MHz to stay outside the AM band. The design will stay above the AM band if the converter operates in pulse width modulation (PWM) mode. The nominal switching frequency of this mode is 2.25 MHz, and the frequency variation depends on the input and output voltage and inductance. To stay in PWM mode, the output current must be greater than half the inductor ripple current and the inductor must be in continuous current mode. First, calculate the minimum inductance required for continuous inductor current.

Because the input voltage and output voltage are fixed and the output current is almost constant and can be predicted easily, the minimum inductance, L, for the converter to operate with continuous inductor current can be calculated using 式 2.

$$L = \frac{V_{out}\left(V_{in} - V_{out}\right)}{2 \times V_{in} \times I_{out} \times f} = \frac{2.8\ V\left(14.5\ V - 2.8\ V\right)}{2 \times 14.5\ V \times 0.08\ A \times 2.25\ mHz} = 6.28\ \mu H \quad (2)$$

Note in the equation above, the larger the output current, the lower the minimum inductance required to conduct continuously. Therefore, the typical current draw value of 80 mA instead of the transient maximum value of 150 mA is used. A light load and wide delta between input and output voltage is the worst case here. Because 6.28 µH is between standard inductor values, the next standard value of 10 µH is used because this value provides considerable headroom, and there are inductors with the same footprint as the 6.8 µH inductor (more inductance in the same amount of space). For more information on calculating the inductance for continuous current mode, see the end of Section 2 of *Low-Noise CMOS Camera Supply Application Report*[6].

With the inductance value chosen, inductor with a proper saturation current is required. The proper saturation will be the combination of the steady state supply current as well as the inductor ripple current. The current rating must be sufficiently high but minimized as much as possible to reduce the physical size of the inductor. 式 3 is used to calculate the inductor ripple current (from *TPS6217x-Q1 3-V to17-V 0.5-A Step-Down Converters with DCS-Control™ Data Sheet*[2]).

$$\Delta I_L = V_{out} \times \left(\frac{\left(1 - \frac{V_{out}}{V_{in}}\right)}{L \times f_{SW}} \right) \quad (3)$$

Where the parameters for the design using the TPS62170-Q1:

- V_{out} = 2.8 V
- V_{in} = 14.5 V
- L = µH
- f_{SW} = 2.25 MHz

This equation yields an inductor ripple current of ΔI_L = 100 mA. To stay in PWM mode, the load current must be greater than 50 mA. Because the estimated load current is 80 mA, there is a fair amount of headroom to work with because an inductor with an inductance of 10 µH as opposed to 6.8 µH was used.

The maximum current draw of this rail is conservatively estimated to be 150 mA. Finally, 式 4 gives the minimum saturation.

$$L_{sat} \geq \left(I_{max} + \frac{\Delta I_L}{2} \right) \times 1.2 = \left(150\ mA + \frac{100\ mA}{2} \right) \times 1.2 = 240\ mA \quad (4)$$

The 10-µH Wurth Elektronik 744798893310, which has a saturation current of 500 mA, was used. This part comes in a very small 2.0 mm × 2.5 mm package. It is important to note that with smaller inductors with high inductances there is a DC resistance. If efficiency is of a greater concern, a lower DCR should be given more priority when selecting inductors. This inductor has a data capture record (DCR) of 300 mΩ. With a load current of roughly 80 mA, an estimated 24 mW will be dissipated in this inductor.

2.3.2.1.2 Choosing the Output Capacitor

Because the device is internally compensated, it is stable for certain LC filter component values. From *Optimizing the TPS62130/40/50/60/70 Output Filter Application Report*[5], the stable values shown in 表 3 is used. With 10 µH, anything in between 4.7 to 22 µF can be used. A 10-µF output capacitor is used, which puts the corner frequency near the center of this region and provides considerable headroom for harsh transients and operating conditions.

表 3. Stability Versus Effective LC Corner Frequency

NOMINAL INDUCTANCE VALUE	NOMINAL CERAMIC CAPACITANCE VALUE (EFFECTIVE = ½ NOMINAL)								
	4.7 µF	10.0 µF	22 µF	47 µF	100 µF	200 µF	400 µF	800 µF	1600 µF
	EFFECTIVE CORNER FREQUENCIES								
0.47 µF	151.4 kHz	103.8 kHz	70.0 kHz	47.9 kHz	32.8 kHz	23.2 kHz	16.4 kHz	11.6 kHz	8.2 kHz
1.00 µF	103.8 kHz	71.2 kHz	48.0 kHz	32.8 kHz	22.5 kHz	15.9 kHz	11.3 kHz	8.0 kHz	5.6 kHz
2.2 µF	70.0 kHz	48.0 kHz	32.4 kHz	22.1 kHz	15.2 kHz	10.7 kHz	7.6 kHz	5.4 kHz	3.8 kHz
3.3 µF	57.2 kHz	39.2 kHz	26.4 kHz	18.1 kHz	12.4 kHz	8.8 kHz	6.2 kHz	4.4 kHz	3.1 kHz
4.7 µF	47.9 kHz	32.8 kHz	22.1 kHz	15.1 kHz	10.4 kHz	7.3 kHz	5.2 kHz	3.7 kHz	2.6 kHz
10.0 µF	32.8 kHz	22.5 kHz	15.2 kHz	10.4 kHz	7.1 kHz	5.0 kHz	3.6 kHz	2.5 kHz	1.8 kHz
	Recommended for TPS6213x, TPS6214x, TPS6215x, TPS6216x, and TPS6217x								
	Recommended for TPS6213x, TPS6214x, and TPS6215x only								
	Stable without Cff (within recommended LC corner frequency range)								
	Stable without Cff (outside recommended LC corner frequency range)								
	Unstable								

2.3.2.1.3 Choosing the Feedback Resistor Values

The output voltage is determined by the resistor divider to the feedback pin. 式 5 is the calculation for the output voltage. The goal is 2.8-V out but with the ability to work with readily available resistor values.

$$R_1 = R_2 \times \left(\frac{V_{out}}{V_{ref}} - 1 \right) \rightarrow V_{out} = \left(\frac{R1}{R2} + 1 \right) \times V_{ref} = \left(\frac{82.5\ k\Omega}{33.2\ k\Omega} + 1 \right) \times\ 0.8\ V = 2.84\ V \quad (5)$$

式 5 gives a close enough output voltage to the desired 2.8 V. For improved accuracy, all FB resistor dividers should use components with 1% or better tolerance.

2.3.2.1.4 Sequencing

The PG signal of the device is used for sequencing. The PG is an open-drain output. Because the open-drain output must be driven high, the PG signal is pulled-up through a 100-kΩ resistor and connected to the enable pin of the TPS62171-Q1. The system sequencing requirement is that the 2.8-V rail must come up and stabilize before the 1.8-V rail does.

2.3.2.2 TPS62171-Q1

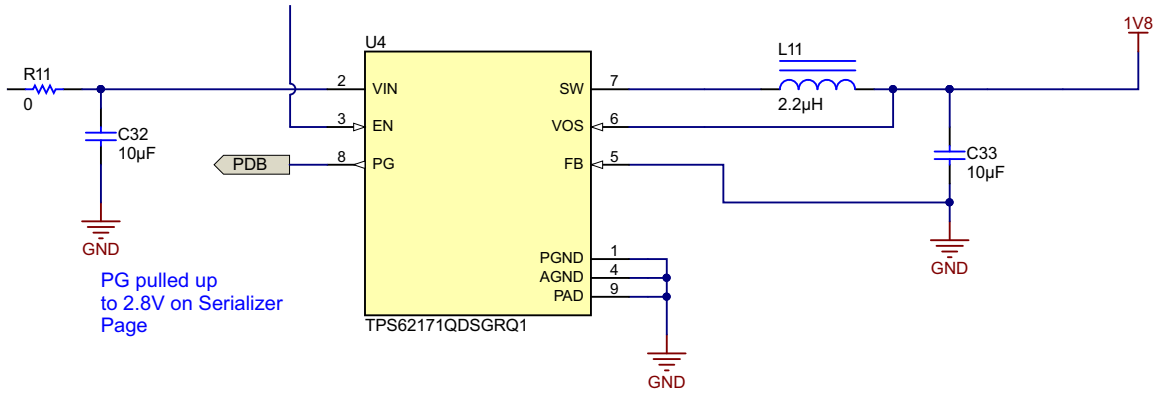


図 8. 1.8-V Supply Schematic

This device is a bit simpler than the TPS62170-Q1 because it is a fixed voltage device. The considerations are nearly identical and the process to select components will be the same as selecting components for the TPS62170-Q1.

Following the same procedure as for the TPS62170, the output LC filter for this supply was selected. The equations from 2.3.2.1 are used to find the design values here. To remain in continuous current mode, an inductance of at least 1.2 µH is required. The next larger standard inductance value of 2.2 µH was chosen to provide more headroom to maintain continuous current mode operation. Referring again to 表 3 in the previous section, this converter is stable with a 1- or 2.2-µH inductor and a 10-µF capacitor. The minimum LSAT is 318 mA required for the inductor. The Würth Elektronik is ultimately selected.

The PG signal from this device is connected to the PDB of the serializer for proper sequencing. This PG signal is set high once the output voltage has stabilized. The serializer is brought up out of reset once the 1.8-V rail is stable, and the PDB pin is set high by the PG signal. The output of PG must be pulled-up to 2.8 V for proper activation of the serializer.

2.3.3 FPD-Link III Interface

The FPD-Link III interface allows for proper power and high-throughput data transmission and is made up of a PoC filter and the DS90UB913A-Q1. This section discusses the PoC filter followed by a discussion of key parameters when designing with the serializer.

2.3.3.1 Power Over Coax (PoC) Filter

One of the most critical portions of a design with PoC is the filter circuitry. The goal of the PoC filter is twofold:

1. Deliver a clean DC supply to the input of the switching regulators.
2. Protect the FPD-Link communication channels from noise coupled backwards from the rest of the system.

The DS90UB913A/DS90UB914 SerDes devices used in this system communicate over two carrier frequencies: 700 MHz at full speed ("forward channel") and 2.5 MHz ("backchannel") determined by the deserializer device. The filter should attenuate this rather large band spanning both carriers, only passing DC. This DC portion is connected to the input of the LM53600-Q1 buck converter to output 3.3 V. By filtering out the backchannel frequency, the PoC filter can also filter the switching frequencies from the upstream power supplies. In 図 9, L2 represents the full PoC filter in this reference design:

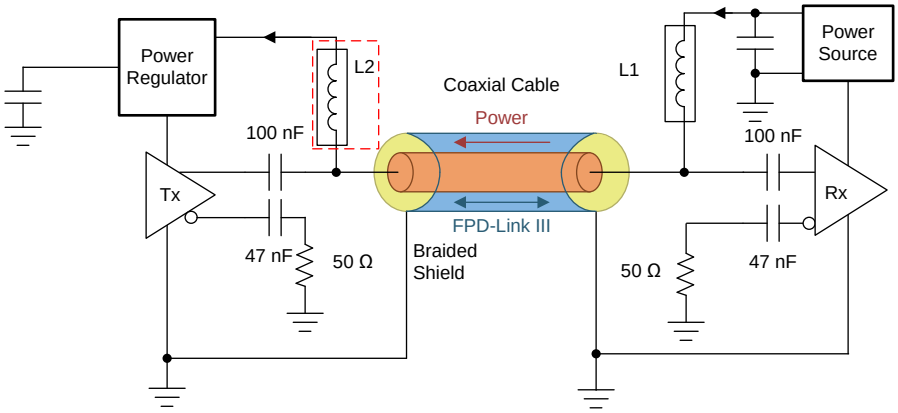


図 9. Power Over Coax

The nominal backchannel speed is 2.5 MHz but can vary from 1 MHz to 4 MHz when taking into account process variation, temperature, and power supply. To achieve the 1-kΩ impedance for the POC network across the full frequency range of 1 MHz to 700 MHz, it is recommended to use two inductors: a 4.7-µH inductor for high frequency forward channel filtering, and a 100-µH inductor for low-frequency backchannel filtering. See the PoC application note for more details[1].

図 10 shows the schematic of the PoC filter for this system:

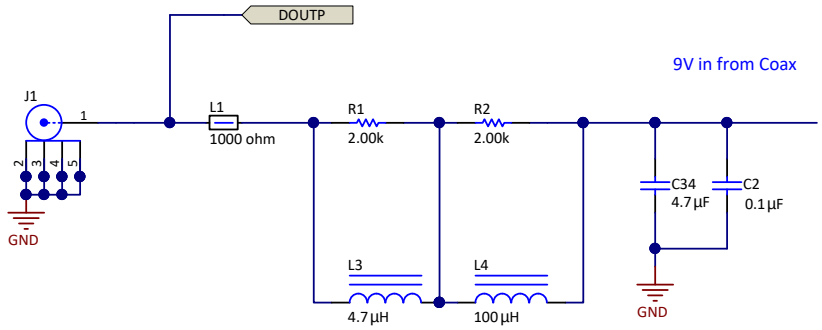


図 10. Power Over Coax Schematic

Ferrite bead L1 increases conducted immunity tested in bulk current injection (BCI) tests. The resistor parallel to the inductors prevents the impedance from spiking above 2-kΩ across the band of interest.

2.3.3.2 DS90UB913A-Q1

図 11 closely resembles the FPD-Link III interface of this reference design and is shown to demonstrate important components and sub-blocks of this system.

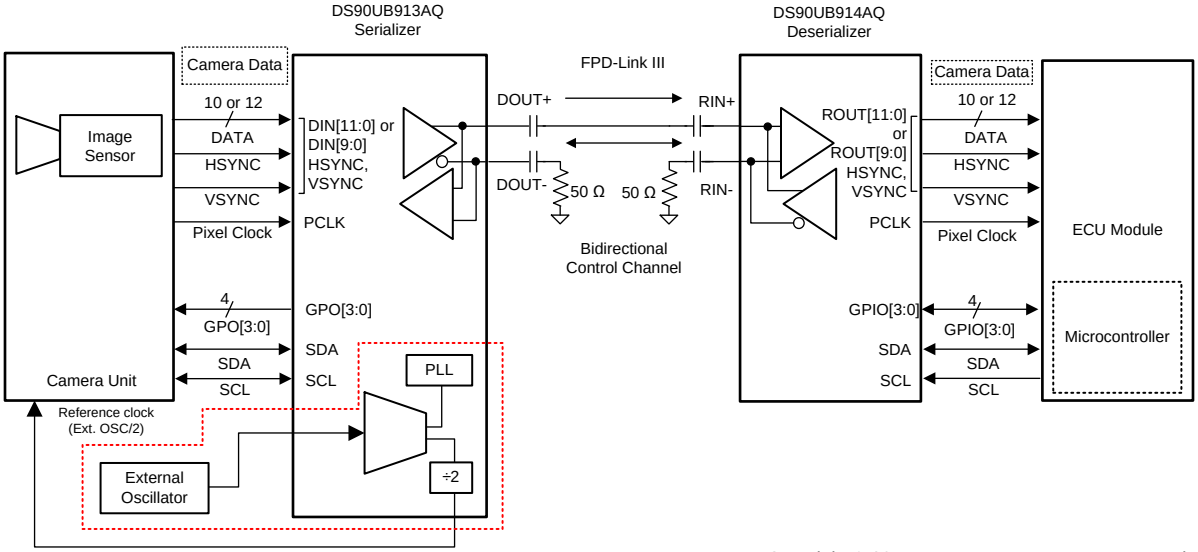


図 11. Typical Operation in External Oscillator Mode

Aside from the passives used in this configuration circuitry, an oscillator must be selected. The TIDA-01002 uses a non-automotive grade 48-MHz oscillator for the serializer to operate in external oscillator mode and 12-bit high frequency mode to achieve 720 p at 30 fps (see 2.3.3.2.1 for more details on why this was selected). This camera module supports outputs from the ISP in 8- and 10-bit YUV422. Note that the data output of the AS0140AT is LSB aligned. LSB aligned was ultimately selected for compatibility across multiple test platforms that use a parallel or CSI-2 interface.

The following critical design parameters are covered in the following subsections:

- Modes of Operation
- PCLK Frequency
- Synchronizing Multiple Cameras
- GPIO Pins
- Power-up and PDB Pin
- ID[X] Pin

Find more details on component selection and design theory in *DS90UB913A-Q1 25-MHz to 100-MHz 10/12-Bit FPD-Link III Serializer*[1].

2.3.3.2.1 Modes of Operation

This reference design uses the serializer in a 12-bit high-frequency mode with an external 48-MHz oscillator as the reference clock. There is an important distinction to note between these two types of modes: the 10- or 12-bit mode relates to the number of data bits input to the serializer, and the other relates to the way the serializer-deserializer pair gets its reference clock. These modes are set in hardware but can be overridden over I^2C. For the oscillator mode, this is set in hardware on the serializer side of the channel. For the bit mode, this is set in hardware on the deserializer side of the channel.

Some systems may require using the pixel clock (PCLK) as the reference clock source for the system. This can be done to achieve higher frame rates or simply for flexibility of the timing signals, such as PCLK and VSYNC. However, the PCLK from an imager can have jitter that exceeds the serializer jitter tolerance in the PCLK mode compared to when the serializer is in external oscillator mode. It is recommended to use an external clock source for the reference clock of the serializer. In this mode, the serializer has a higher jitter tolerance than when operating with pixel clock from imager as the reference clock. This reference design follows this recommendation.

When the serializer operates in external oscillator mode, the reference clock signal that is fed to the ISP from the serializer will be half the external oscillator frequency. The output from the external oscillator goes into the serializer through GPO pin 3, and through a divide-by-2 circuit before being outputted at GPO pin 2. The 30-fps requirement drives the reference clock requirement and, in turn, resonant frequency requirement of the external oscillator to be within 48 MHz to 60 MHz. The ISP requires a reference clock to be within 6 MHz and 30 MHz.

The following values were derived from the data sheets of both serializer and imager. Here are the requirements for the external oscillator:

- Resonant frequency of 48 to 60 MHz
- Supply voltage rated for V_{DDIO} or 2.8 V
- Small footprint

The TIDA-01002 design uses a 48-MHz crystal oscillator from Pericom. The oscillator has a small footprint (2.5 mm × 2.0 mm), a jitter of ±10 ppm over temperatures of –40°C to +105°C, and supports a supply voltage range of 1.8 V to 3.3 V.

See the device data sheet for details on the required circuitry to implement the clocking scheme described in this section.

2.3.3.2.2 Pixel Clock (PCLK) Frequency

Because the serializer will be operating in 12-bit high frequency mode using an external oscillator as its reference clock, PCLK and external oscillator ratio must be fixed. In 12-bit high frequency mode, the device divides the incoming pixel clock internally by 1.5. Therefore, the pixel clock frequency must be 1.5 times the external oscillator frequency. In this reference design, the external oscillator frequency is 48 MHz. This means the PCLK frequency from the AS0140AT to the serializer must be 72 MHz.

2.3.3.2.3 Synchronizing Multiple Cameras

For surround view systems, synchronizing multiple cameras is required. To achieve this with this serializer, the GPIO pins transmit the control signals for syncing multiple cameras. The system controller must provide a field sync output, such as a vertical sync or frame sync signal, and the imager must be set to accept an auxiliary sync input. 図 12 shows an example of the synchronization.

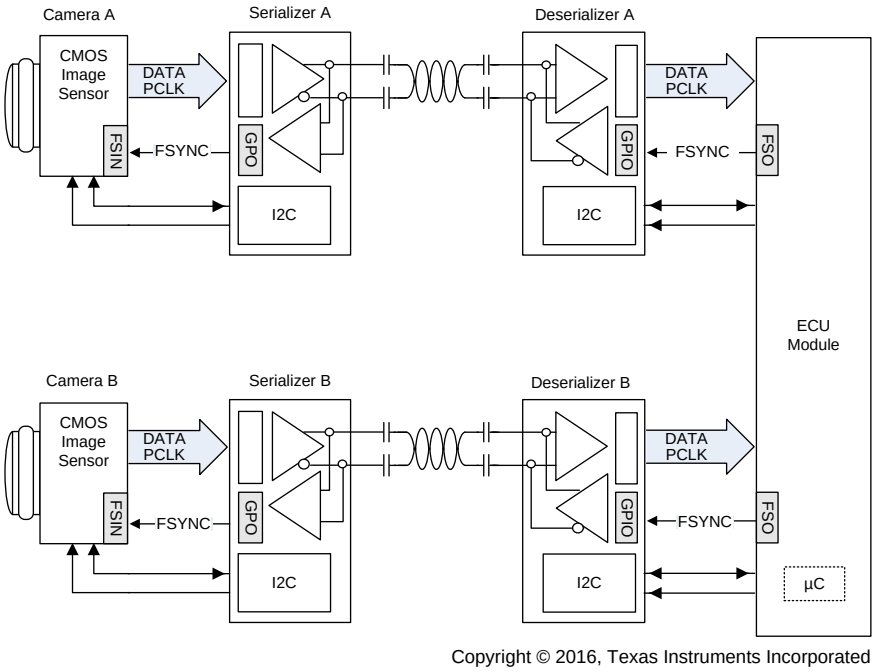


図 12. Synchronizing Multiple Cameras

When control data is reconstructed from the bidirectional control channel, there is a time variation of GPIO signals arriving at different target devices between the parallel links (camera A and B). For synchronization, the maximum latency delta, T1, of the GPIO data transmitted across multiple links is 25 µs. This 25 µs is the maximum time between the rising edge of GPIO and the time the signal arrives at the camera. Note the timing variations between the different links must always be verified to system and timing specifications. 図 13 shows an example of what this maximum latency looks like.

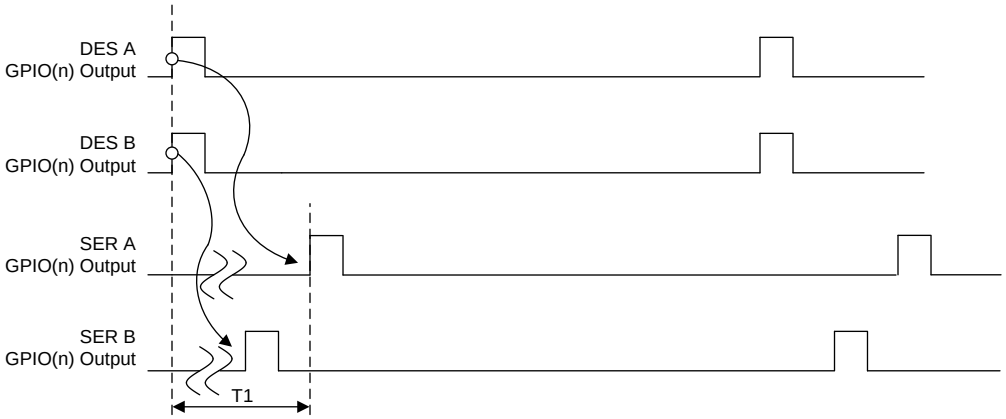


図 13. GPIO Maximum Latency

2.3.3.2.4 GPO Pins

There are four GPO pins available on the serializer. However, because this reference design is running in External Oscillator mode, GPO3 is automatically configured to be the input for the external clock, and GPO2 is configured to be the output of the divide-by-2 clock, which is fed to the imager as its reference clock. This leaves two GPO pins for use.

Because this reference design also must be able to use this camera in a synchronized multi-camera system, one of these GPO pins will be used as the frame sync signal transmitter, and the last GPO pin serves as the reset for the imager.

2.3.3.2.5 Power Up and PDB

The Power Down Bar input pin, or PDB pin, enables or disables the serializer. The purpose of PDB is to ensure the serializer turns on when system voltages have stabilized. When PDB is low and it is powered down, the internal PLL is shut off and current draw is minimized. The PDB pin must be ramped after the VDDIO and VDD_n supplies reach final voltage levels. In this case, 2.8 V must come up before 1.8 V then finally PDB. 図 14 shows how the sequence should look.

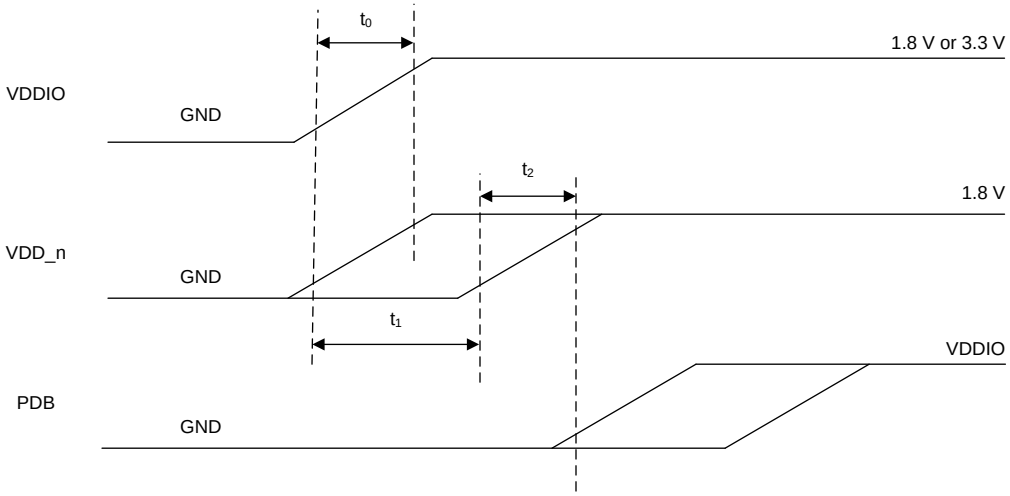


図 14. Target Power Up Sequence

The PG output from the 1.8-V switcher is used to enable the serializer. The main constraint is that V_{DD_n} does not lead in ramping before the V_{DDIO} system supply. In this system, PDB is pulled-up to V_{DDIO}.

2.3.3.2.6 ID[x]

The ID[x] pin is used to assign the device I²C address. The pin is used to decode and set the physical slave address of the serializer to allow up to five devices on the bus connected to the serializer. There are six possible addresses for each serializer device.

In this design's serializer, address 0x58 will be set with a 0-Ω resistor as R_{ID}, or the ID setting resistor. The recommended maximum resistor tolerance is 1%. 図 15 shows the resistor divider which sets the ID.

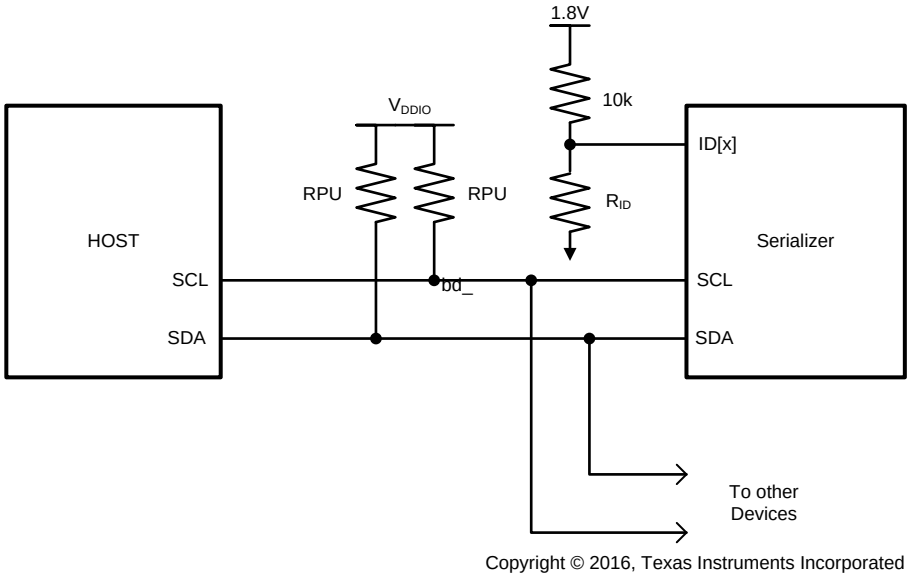


図 15. ID[x] Address Decoder of Serializer

In the following section, there will be more details about the I²C communication of the system.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

The TIDA-01002 only requires one connection to a system with a compatible deserializer. Simply connect the FAKRA connector of the coax cable to the coax connector of deserializer board and TIDA-01002.

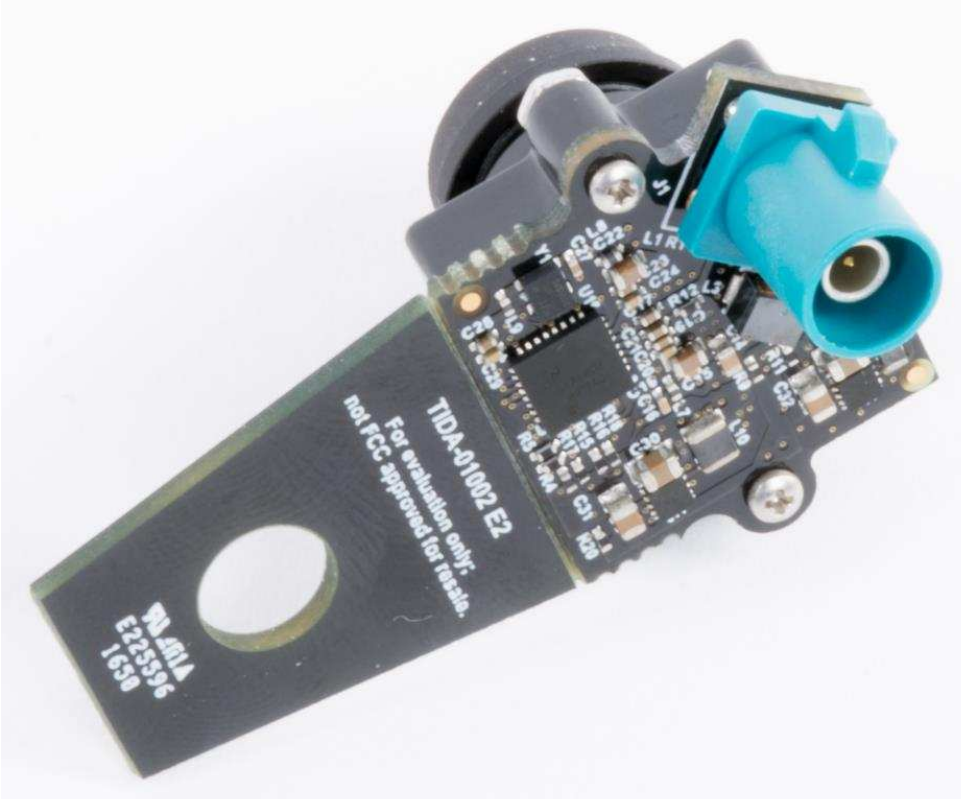


図 16. Getting Started With Board

When the TIDA-01002 is connected to a deserializer board, the LOCK signal on the deserializer should be high. This signifies that the PLL is locked and forward channel communication is possible. The deserializers have a LOCK and PASS pin to monitor the state of the link. On some EVMs, the LOCK status is reported by turning on an LED. Whenever the forward channel link is lost, LOCK will go low. Whenever there is an error detected in the transmission of data, the PASS pin goes low. These two pins used in conjunction are a way to determine the reliability of the link. Triggering on an event such as a loss of LOCK while monitoring other signals, such as the pixel clock or other I^2C commands, can yield very useful information about the system and the link quality. For more details on troubleshooting and diagnostic features of the deserializer, see the corresponding device data sheet.

3.1.1.1 I²C FPD-Link III Initialization

In order to stream video from the imager, the serializer-deserializer pair must be properly initialized. This is done in a few simple steps over the backchannel using I²C. As discussed in previous sections, the default addresses of both the serializer and deserializer are selected by voltage dividers on the ID[x] pins. In this reference design, the default addresses are 0xB0 (0x58 7-bit) for the serializer, and 0xC0 (0x60 in 7-bit) for the '914A-Q1 deserializer and 0x60 (0x30 in 7-bit) for the '934-Q1.

The deserializer must be initialized first as it is the first "stop" in the communication chain. The first step is to write the serializer address to the serializer ID register of the deserializer. This is not always mandatory because ser-des is designed to do this automatically once the pair is locked; this step is included for thoroughness. The second step is to write the ISP address to the slave ID register and the slave alias ID register of the deserializer. Now the deserializer and serializer are initialized. To bring the imager out of reset, the serializer GPO that controls the imager reset must be set high. Once it is set, the TIDA-01002 design is ready to talk to the ISP. The last thing to ensure is that the deserializer is in 12-bit high frequency mode.

The writes to initialize the 913-914 pair are as follows:

- Deserializer I²C address 0xC0 (8-bit) or 0x60 (7-bit):
  - Register 0x07 with 0xB0: Sets serializer ID to 0xB0
  - Register 0x08 with 0x90: Sets slave ID for imager to 0x90
  - Register 0x10 with 0x90: Sets slave alias for imager to 0x90
  - Register 0x1F with 0x12: Overrides mode set by pin, enables 12-bit HF mode
- Serializer I²C address 0xB0 (8-bit) or 0x58 (7-bit):
  - Register 0x0D with 0x99: Sets GPO0 and 1 on serializer, disables remote deserializer GPO control

For the 913-934 pair, see the following writes:

- Deserializer I²C address 0x60 (8-bit) or 0x30 (7-bit):
  - Register 0x4c with 0x01: Enables register writes for Port 0
  - Register 0x58 with 0x58: I²C passthrough enabled
  - Register 0x5C with 0xB0: Sets serializer alias to 0xB0
  - Register 0x65 with 0x90: Sets slave ID for imager to 0x90
  - Register 0x6D with 0x7E: Configures port to coax mode and FPD III to RAW 12 HF mode
- Serializer I²C address 0xB0 (8-bit) or 0x58 (7-bit):
  - Register 0x0D with 0x99: Sets GPO0 and 1 on serializer, disables remote deserializer GPO control

3.1.1.1.1 Software

The software used to verify and display video is DevWareX, from ON Semiconductor.

3.2 Testing and Results

For the following tests, the camera was connected to a single camera system. The DS90UB914A-Q1 EVM was used to connect to the camera module, and a Demo3 was connected to the EVM through two adapter boards.

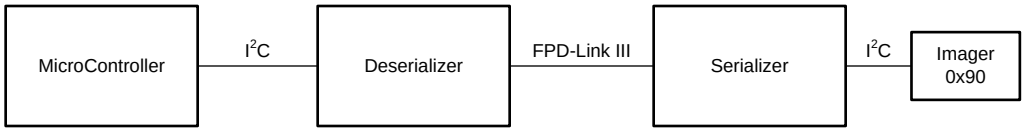


図 17. Simplified Block Diagram

3.2.1 Test Setup

3.2.1.1 Setup for Verifying Power Supply Requirements

The following sections go over the test set up for verification of the design. The power-up sequence, switching frequencies of the DC/DC converters, and system efficiency will be tested. For the switching frequencies and efficiency tests, the camera will be transmitting video.

3.2.1.1.1 Power-up Sequence

The sequencing requirement is that 2.8-V rail turns on before the 1.8-V rail, which turns on the serializer.

1. V_{IN} ON
2. 2.8-V ON
3. 1.8-V ON
4. PDB ON

図 18 shows where the test leads are connected.

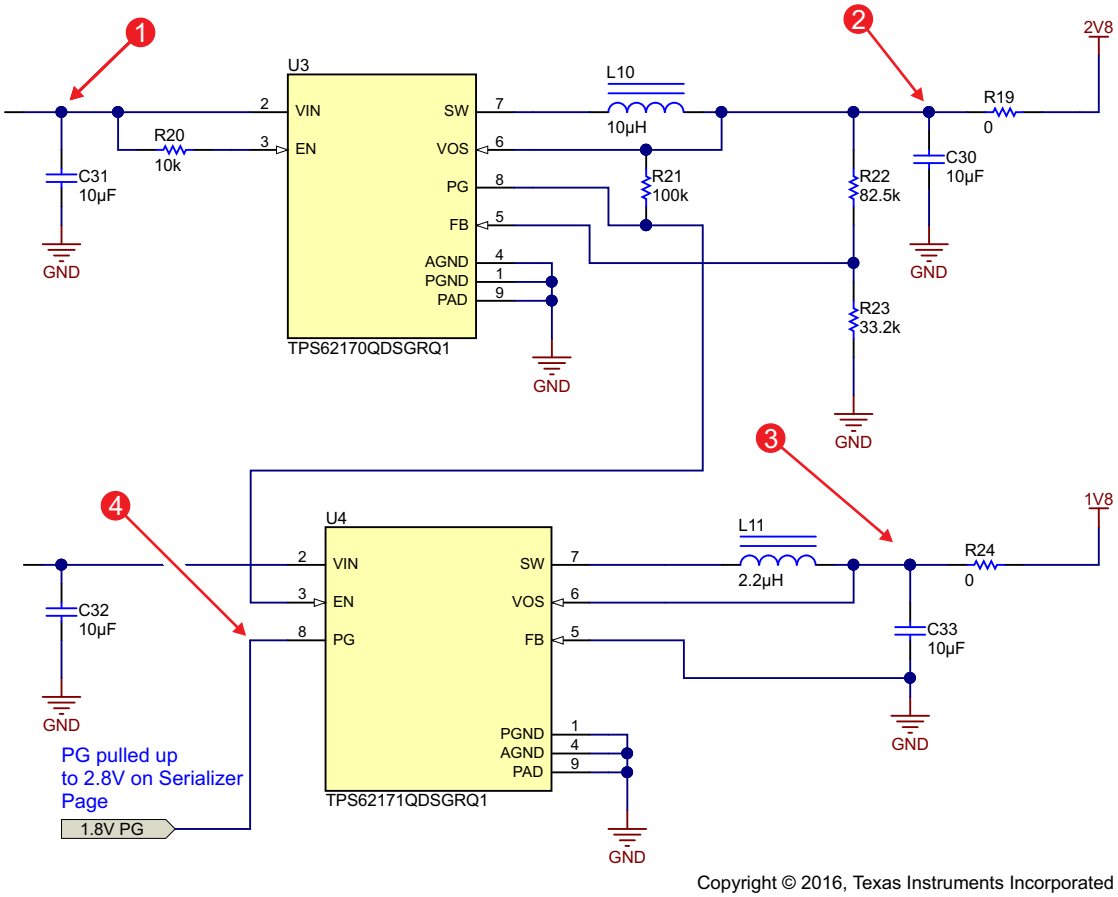


図 18. Power-up Sequence Test Lead Connections

3.2.1.1.2 Switching Frequencies

One of the system requirements is to keep switching frequencies of the DC/DC converters outside of the AM band (530 kHz to 1.8 MHz). To test this, the side of L10 is tapped, which connects to the SW pin 7 of U3, TPS62170, and the same for L11 of U4. Tapping the wrong side of the inductor will show a filtered version without the frequency content. 図 19 shows the probe points to get the scope shots.

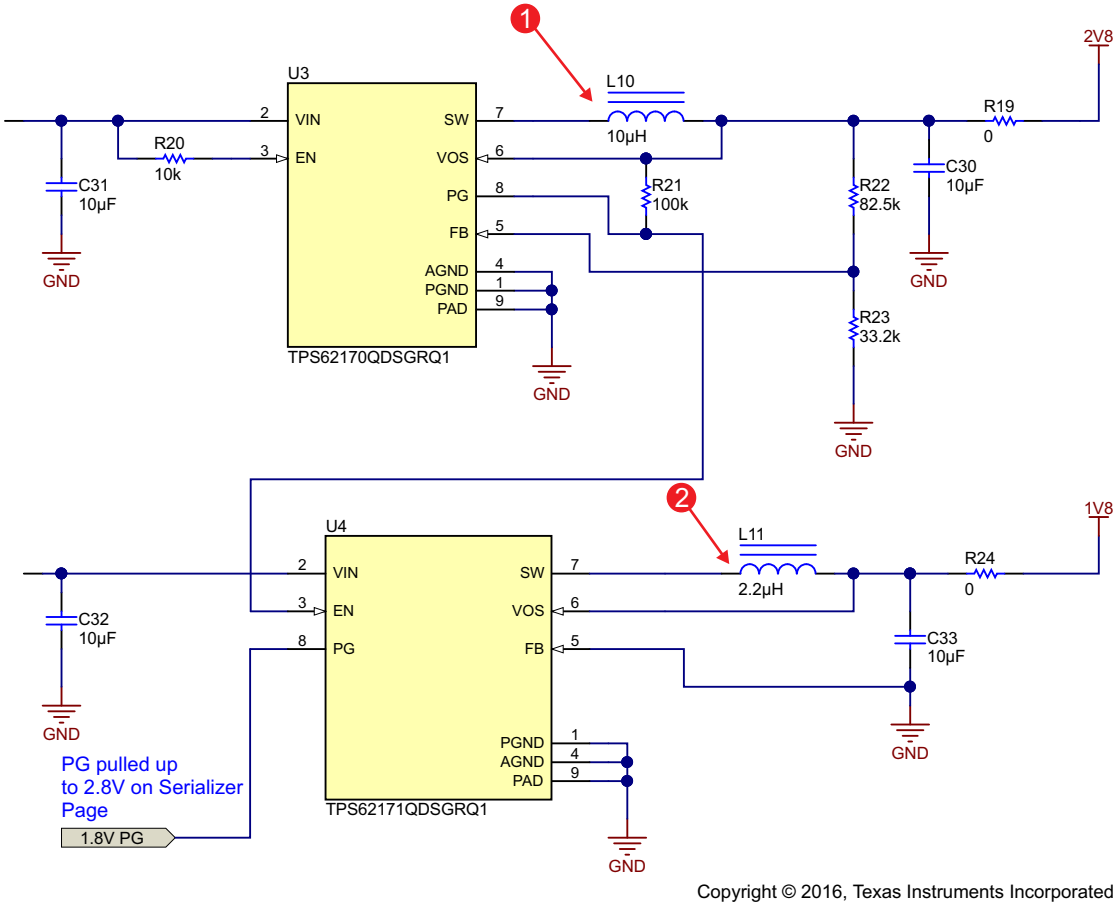


図 19. Switching Frequency Test Setup

3.2.1.1.3 Power Supply Efficiency

A total efficiency of 77% was estimated for a 9-V input. However, the available test platform provides a 5-V input. The efficiency estimation for 5-V input to the switchers is roughly 89.1%.

To test the system efficiency, the current will be measured directly out of the output inductors of the switchers and out of the PoC input inductor. This measurement will be done by placing a current probe on each loop to measure the RMS DC current draw of the board and output currents for both switchers during video transmission. The input voltage for the test setup will be 5 V (the output voltage of the switchers). This is enough information to yield a good measure of system efficiency.

3.2.1.2 Setup for Verifying Video

The main requirement of this system is of course a clear video feed. In this section, the video feed will be tested by showing a screenshot of the video transmission from the software tool, DevwareX. Some screenshots of the video feed are required as captured by the software associated with the imager and ISP in the following output formats:

- 8-bit YUV422
- 10-bit YUV422
- RAW 12-bit Bayer

Results are shown in 3.2.2.2.

3.2.1.3 Setup for Verifying I²C Communications

For this test, a logic analyzer with I²C decode is used to monitor the I²C traffic on the buses. The two buses of interest are:

1. I²C connection from serializer to imager
2. I²C connection from microprocessor to deserializer

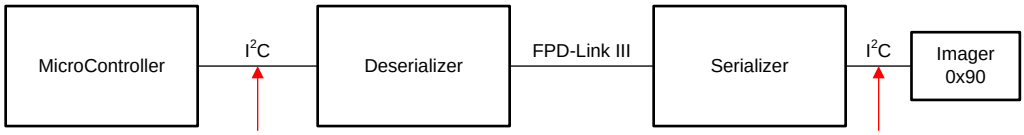


図 20. Setup for Monitoring I²C Transactions

When I²C communication is working properly, transactions meant for addresses on the remote end of the FPD-Link III can be detected.

3.2.2 Test Results

This section contains not only test data to verify the design of the system but also some of the problems encountered and what was implemented to move past them. One should always be extremely careful and thorough when designing, especially with signal processors. For those times when extra caution could have been exercised, the following may help with debug.

3.2.2.1 Power Supply Requirements Testing and Modification

Examine the power supply to ensure it meets the requirements outlined in 3.2.1.1.

3.2.2.1.1 Power-up Sequence

The power-up sequence requires the 2.8-V rail to come up before 1.8-V rail and for PDB to come out of reset once the 1.8-V rail is stabilized. This sequencing is achieved through cascading power good signals and an RC circuit to delay the turn on of the serializer and ISP. The values used are a 0.1-µF capacitor and 100-k pullup resistor.

図 21 shows the target waveform.

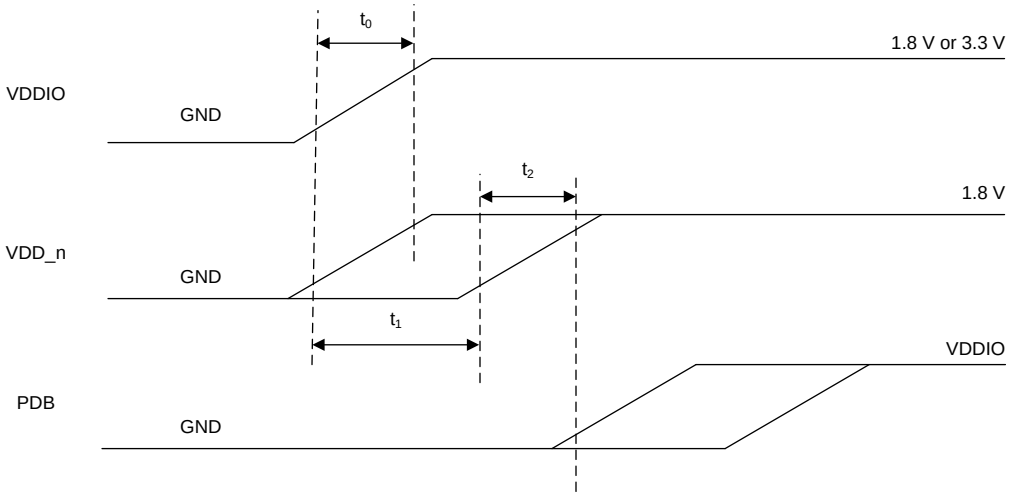


図 21. Target Power-up Sequence

図 22 shows a screen shot of the actual power-up sequence.

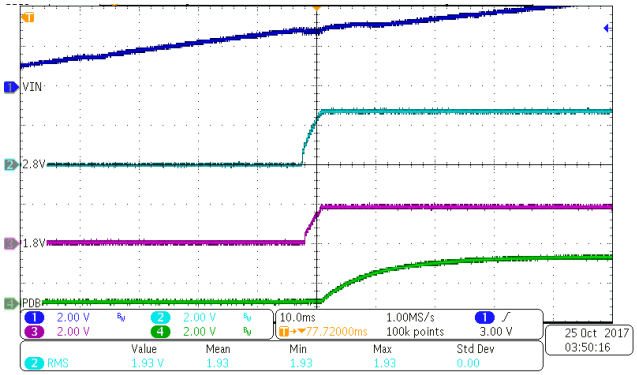


図 22. Power-up Sequence

3.2.2.1.2 Switching Frequencies

The switching frequencies of both DC/DC converters are well above the required 1.8 MHz for a good margin from the AM band. 図 23 and 図 24 show the oscilloscope images of the waveforms at the switching node of each DC/DC converter.

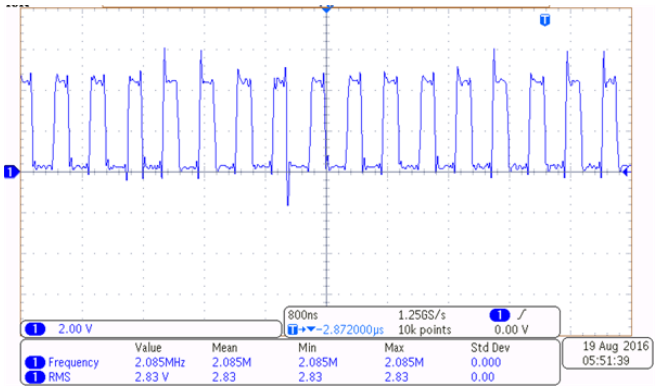


図 23. 2.8-V Switching Node

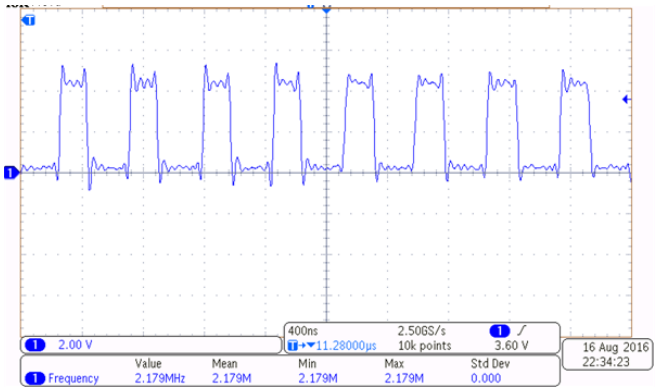


図 24. 1.8-V Switching Node

3.2.2.1.3 Power Supply Efficiency

Before discussing the results, note that input voltage of the tested system was 5 V. With a 5-V input, the power supply efficiency is estimated to be 89.1%. The total measured efficiency was 88.5%, which is only slightly lower than the estimate.

図 25 and 図 26 show the current waveforms measured through each inductor.

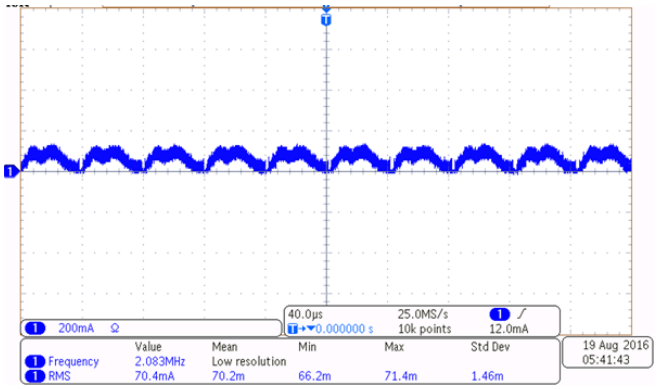


図 25. Loading on 2.8-V Rail

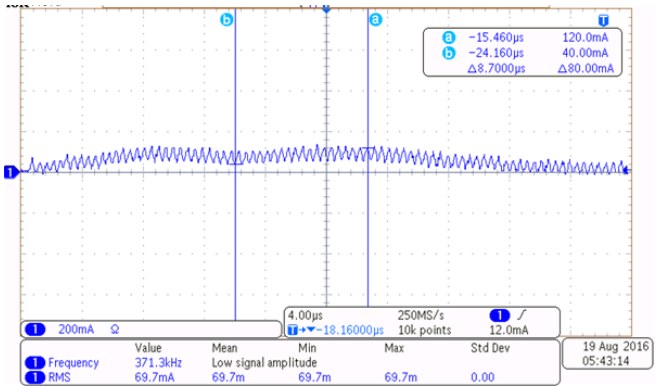


図 26. 2.8-V Ripple Current

As shown in 図 25 and 図 26, the RMS current of the 2.8-V rail was found to be 70.4 mA. This result was quite close to the estimated 80 mA. Using the RMS current as a good representation of the current consumed by the system, the output power of this rail is 197.12 mW.

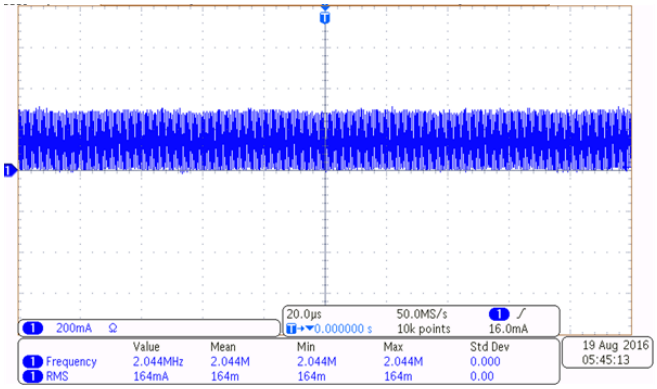


図 27. Loading on 1.8-V Rail

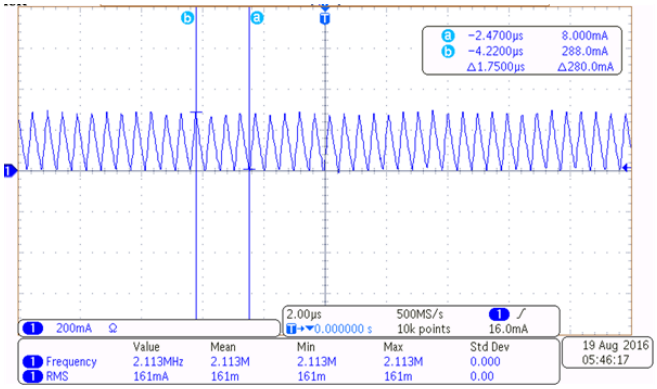


図 28. 1.8-V Ripple Current

The RMS current for the 1.8-V rail is roughly 160 mA, much lower than the original estimate of 230 mA. The 1.8-V rail power consumption is therefore roughly 290 mW.

図 29 shows the input current through inductor L3.

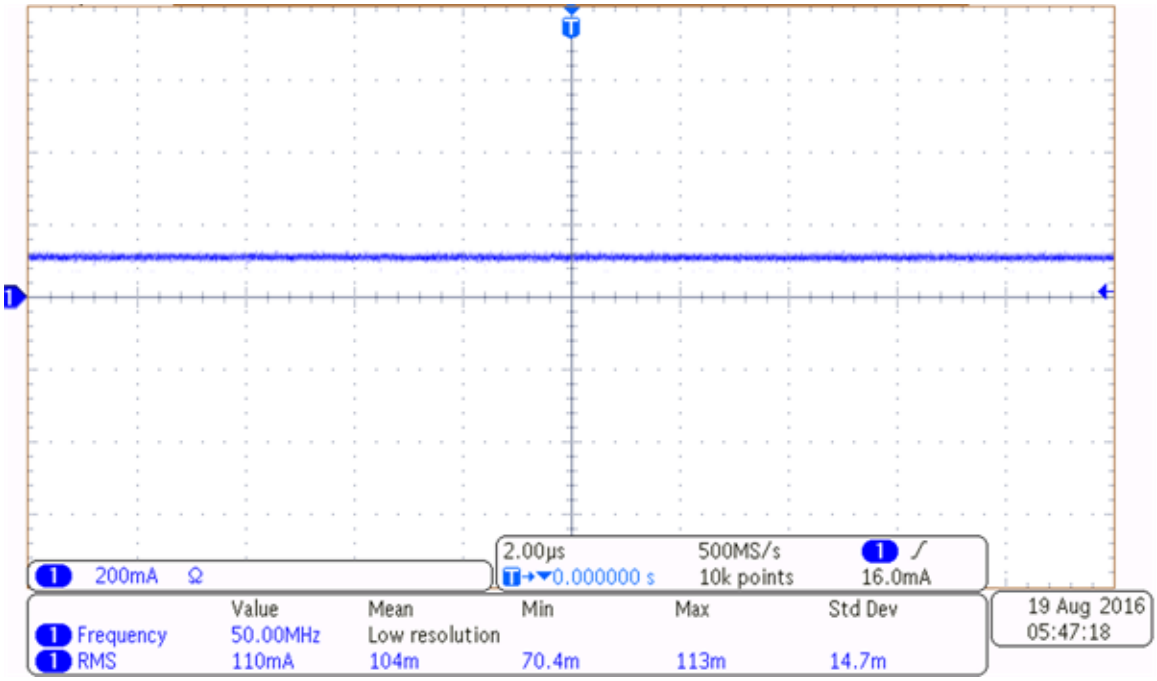


図 29. Input Current Through L3

式 6 is used to calculate a good estimate of the system efficiency and does not include power dissipation through DC resistances of external components:

$$\text{Efficiency} = \frac{P_{1.8\,V} + P_{2.8\,V}}{P_{in}} = \frac{1.8 \times 0.161 + 2.8 \times 0.0704}{5 \times 0.110} = 88.5\% \quad (6)$$

Because the current of the 1.8-V rail was roughly 161 mA, the current on the 2.8-V rail was roughly 70.4 mA, and the input current was 110 mA, the total efficiency is calculated to be 88.5%.

3.2.2.2 Video Verification

図 30 was taken of the live video feed. DevWareX runs at 720 p at 30 fps with 8-bit YUV422 output format. Video streamed for five and half minutes when this frame was captured. The number of frames captured is stored in the mon_heartbeat register shown in the upper-right corner of the capture.

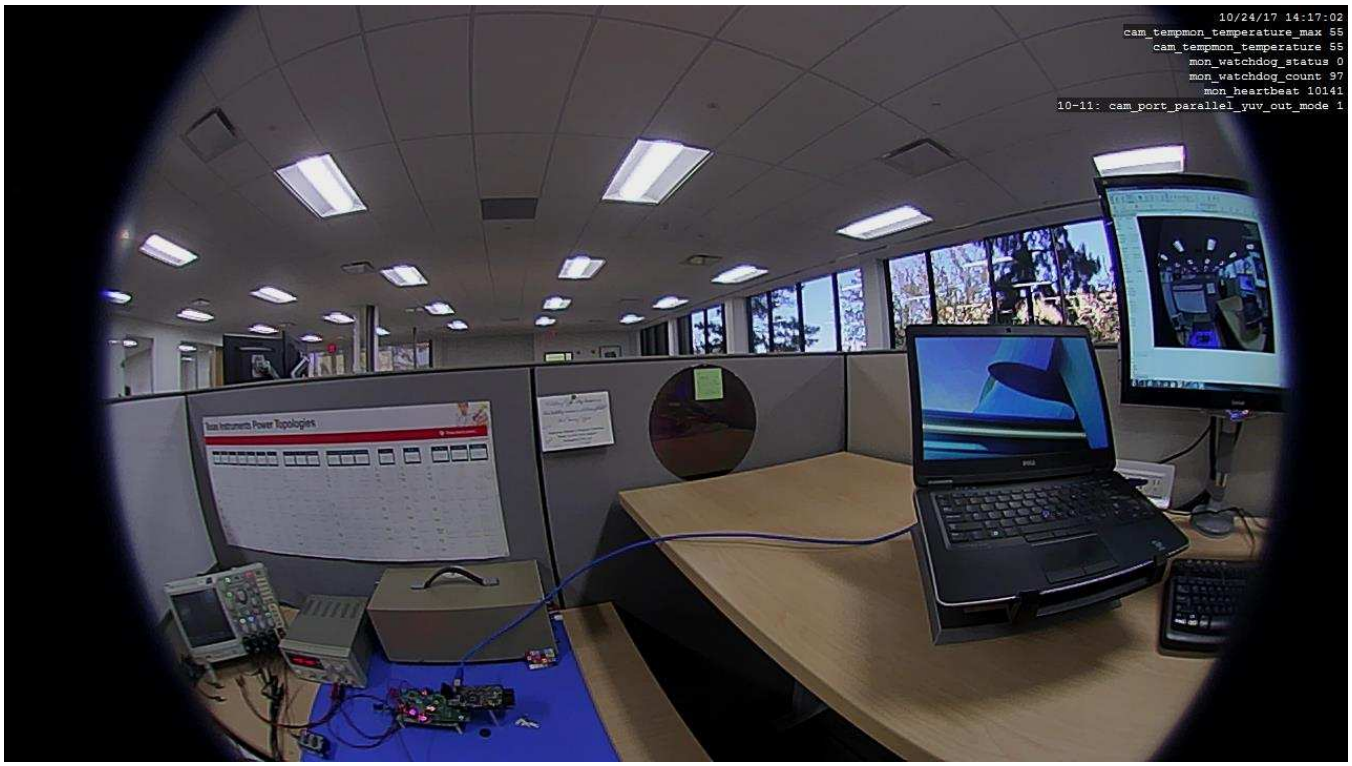


図 30. 720 p at 30 fps

図 31 shows the 10-bit YUV422 video output. Video streamed for three and a half minutes when this frame was captured.

図 31. 10-bit YUV422

3.2.2.3 I²C Communications

図 32 shows that the I²C communication through the FPD-Link III is working. The I²C master on the deserializer end successfully reading a register in the ISP is demonstrated in 図 32.

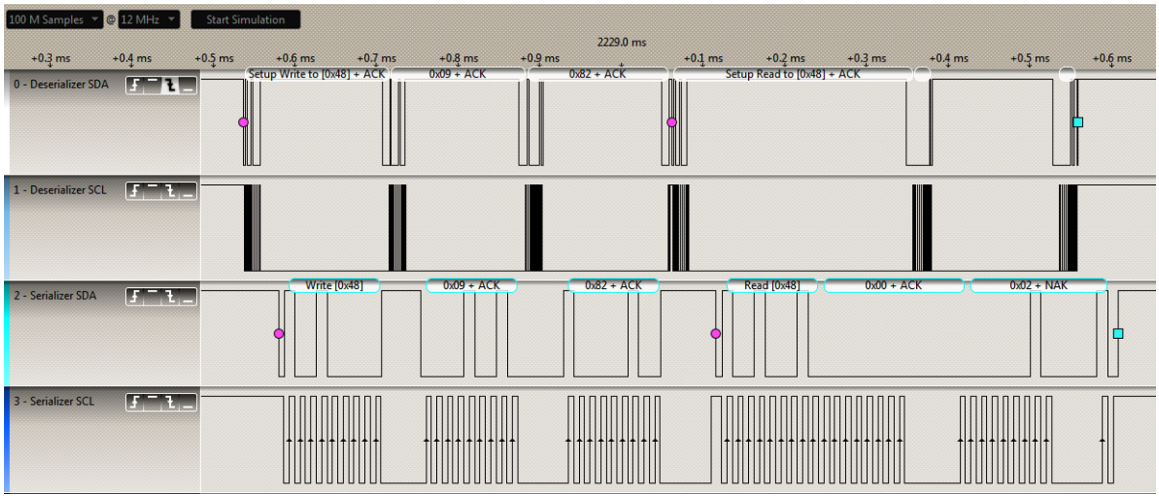


図 32. I²C ISP Transaction

This transaction only occurs if the deserializer is properly initialized, as described in 3.1.1.1. By acknowledging the I^2C write, the ISP has confirmed that it is present and active. Reading the status registers can confirm the status of the imager as well as verify that the correct imager was installed during assembly.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01002.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01002.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01002.

4.3.2 Power Supply Layout

During part placement and routing, it is critical to consider all current paths in the circuit, especially fast-changing currents. Careful placement is especially important for this case where both a sensor and ISP are loading each rail. Proper and strategic use of power planes and vias enables maximum performance of the power supplies to respond to dynamic loading and sensitivity of the imager and ISP rails to avoid video defects and FPD-Link communication disruption.

For this reference design, the top priority is the placement and orientation of the sensor. After the imager placement is locked in, the placement of the PoC filter and power supplies are designed to minimize noise. The distance between the rails of the ISP and the supplies are kept short, and the high di/dt current paths are kept as far away as possible from sensitive circuitry and high-speed video signals. After mapping out critical power paths, the required escaped vias are spaced to minimize voids in the power and ground planes. There are many different ways to prioritize component placement, but for this type of system, prioritizing power paths is the most critical for a high quality system output: clear video.

The layout for the 1.8-V supply did not require any special technique besides what the data sheet recommends. As the 1.8-V switcher is a fixed output device, the FB pin was tied to GND on the thermal pad. 図 33 shows the component placement of the 1.8-V supply.

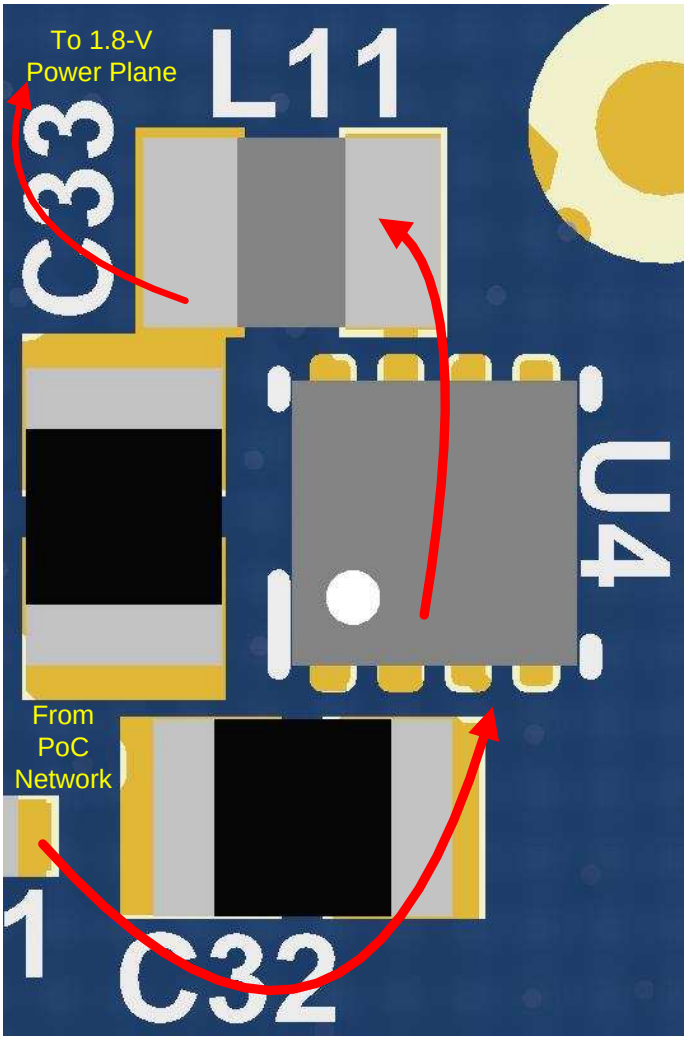


図 33. 1.8-V Supply Component Placement

The red arrows designate current flow. Current flows in from the PoC network through R11, and the output is 1.8 V at the L11-C33 node. This 1.8-V output is distributed to the serializer and ISP through power planes on the top layer, inner Layer 4, and the bottom layer, as shown in 図 34.

図 34 shows the power planes on the top layer, Layer 4, and the bottom layer. The yellow boxes appear where the corresponding chips are placed.

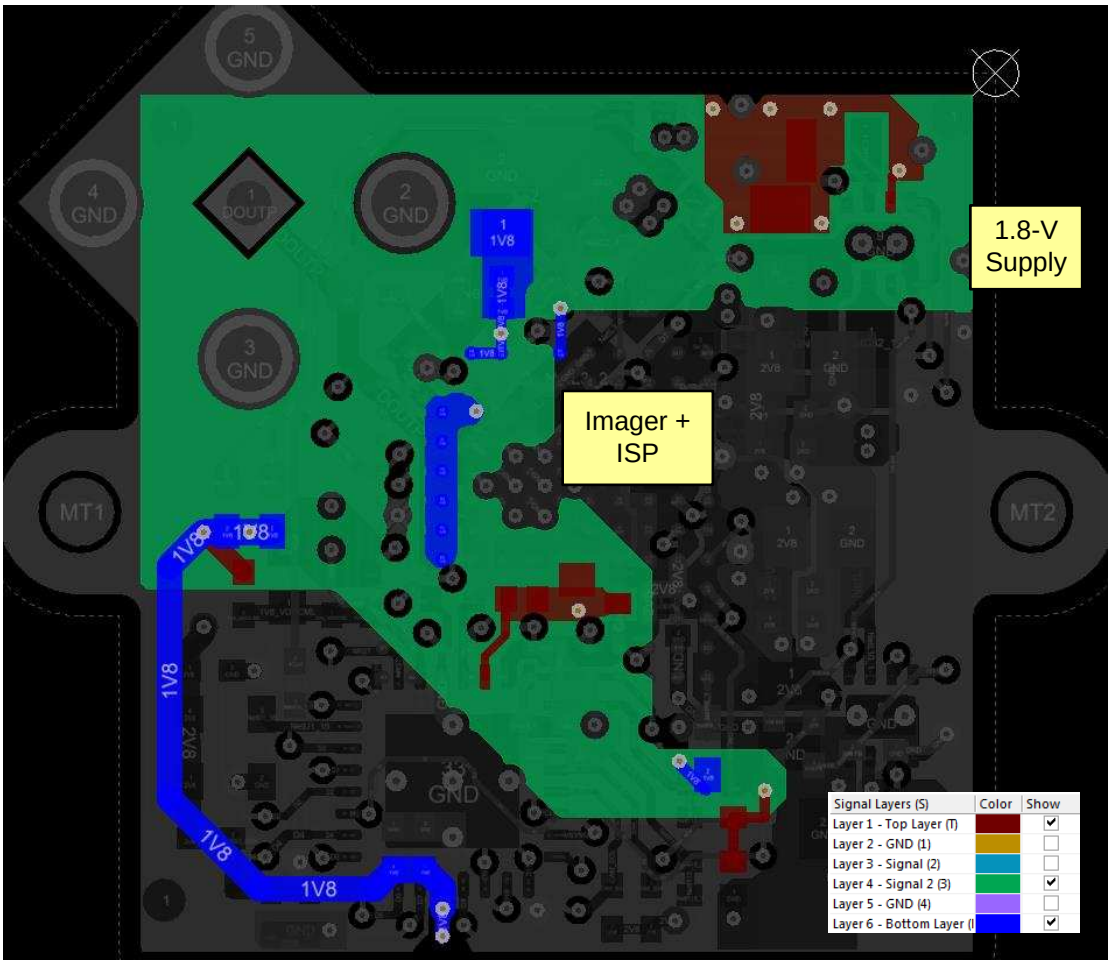


図 34. 1.8-V Power Plane

図 35 shows the 2.8-V supply component placement. Similar to the 1.8-V supply component placement, the data sheet recommendations are followed very closely, with all passive components on the same layer (top layer) as the device. One difference to note between the 1.8- and 2.8-V supply layout is that the input to the 2.8-V supply comes from the 9-V IN plane on Layer 3, as opposed to on the top layer like for the 1.8-V supply. This change is done to keep the 9-V IN plane away from the 2.8-V switch node on the top layer.

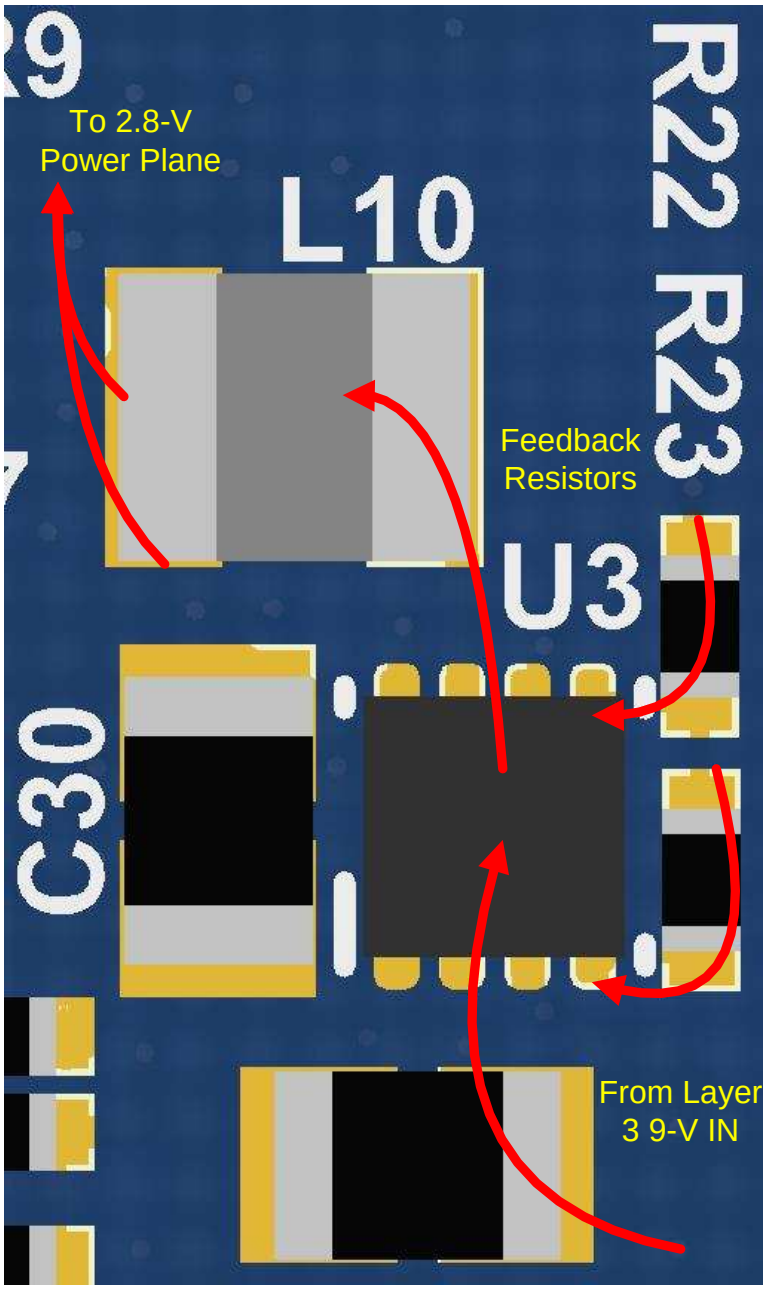


図 35. 2.8-V Supply Component Placement

The red arrows show current flow.

図 36 shows the 2.8-V power plane, which is on the top layer, Layer 4, and the bottom layer.

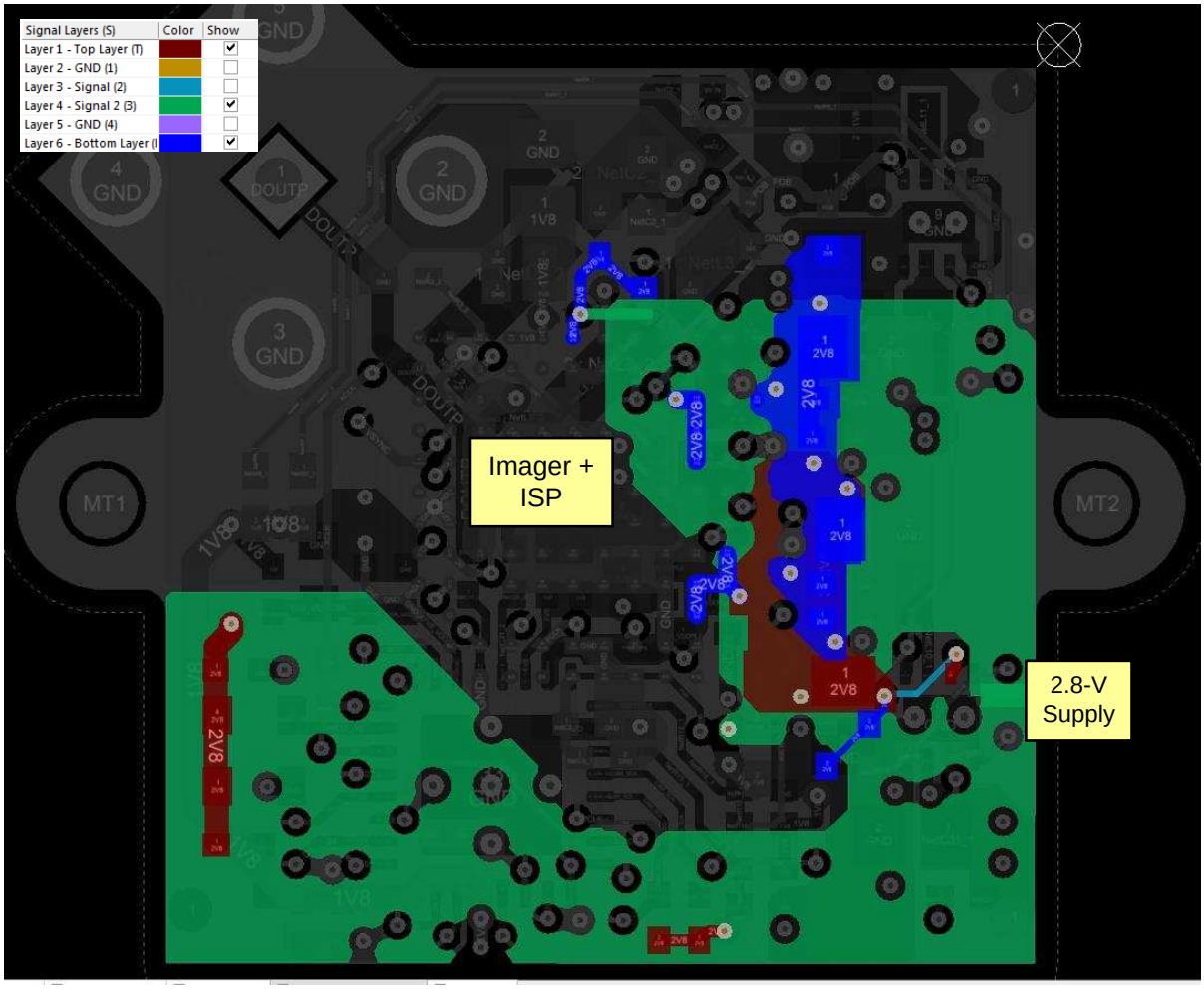


図 36. 2.8-V Power Plane

4.3.3 High-Speed Trace and PoC Layout

The layout for the PoC filter is critical for reliable FPD-Link communication. Because the PoC filter is required to provide clean power to the system and enable reliable communication, small mistakes can cause big problems in performance. First, the layout of the high-speed, 50-Ω trace which will carry both power and signal is discussed, followed by a look at the power over coax filter network.

For this application, a single-ended impedance of 50 Ω is required for the coax interconnect between DOUTP and the AC coupling cap C17. Whenever possible, this trace should also be kept short to reduce system susceptibility to noise, and minimize EMI and parasitics. The routing of the high speed serial line is shown in 図 37. The total length of the trace is 9.74 mm or 383 mils.

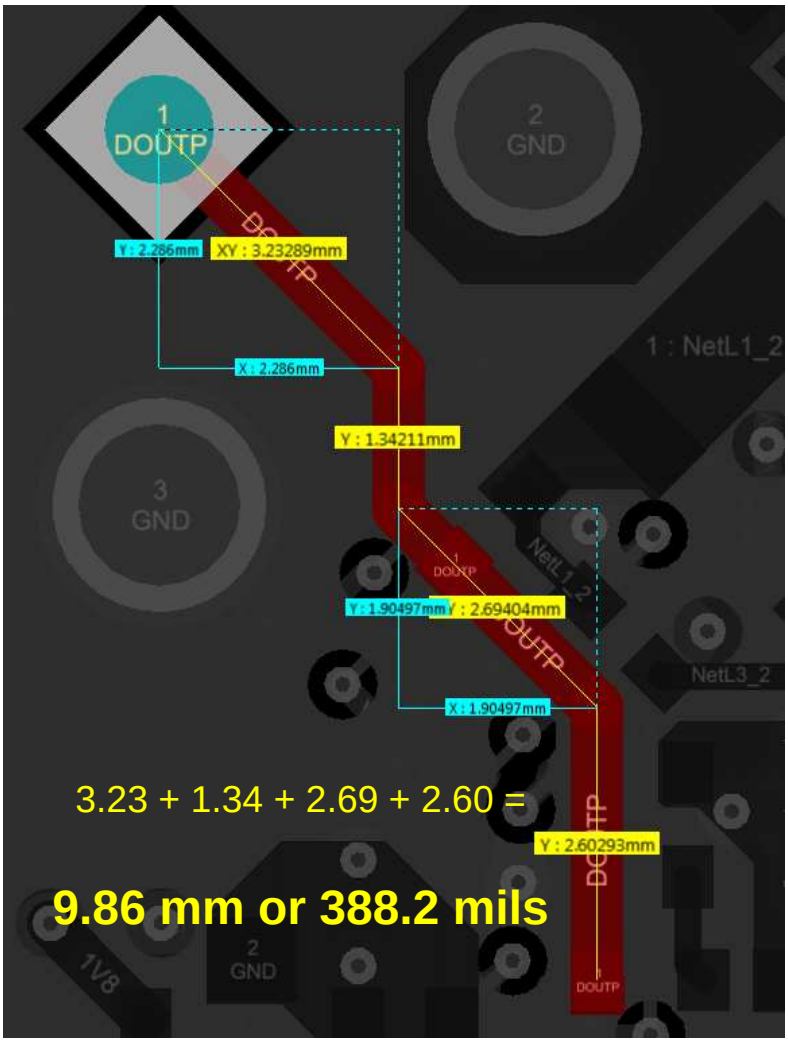


図 37. High Speed Data Line Trace

図 38 shows the path that DC and filter out AC will take through the power over coax filter to the system supplies.

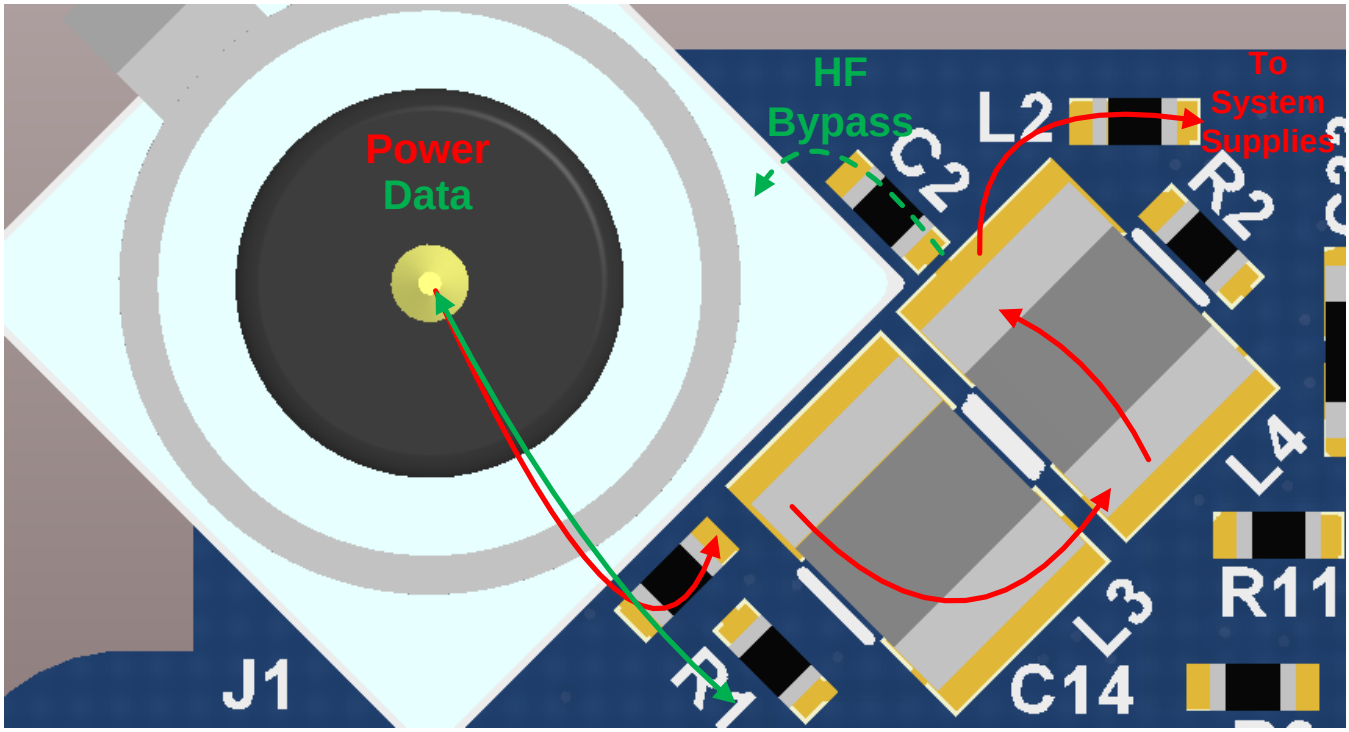


図 38. Input Current Path Through PoC

The red arrows follow DC to the system supplies, and the bidirectional green arrow that travels along the same trace as the red arrow represents the FPD-Link communication. The dashed green arrow shows the path through C2 that unfiltered high frequency noise takes. Placement of this high-frequency filter capacitor is critical and can have a direct effect on link performance. This capacitor (or capacitors) should always be placed in such a way as to minimize the current loop through the PoC network and isolate the filtered high frequency noise from the rest of the system. Here, the current loop is kept within the top corner of board, near the coax connector.

図 39 shows the actual traces of the PoC network, which are on the top layer, along with solid yellow lines to represent DC and dashed yellow to represent bypassed high frequency noise.

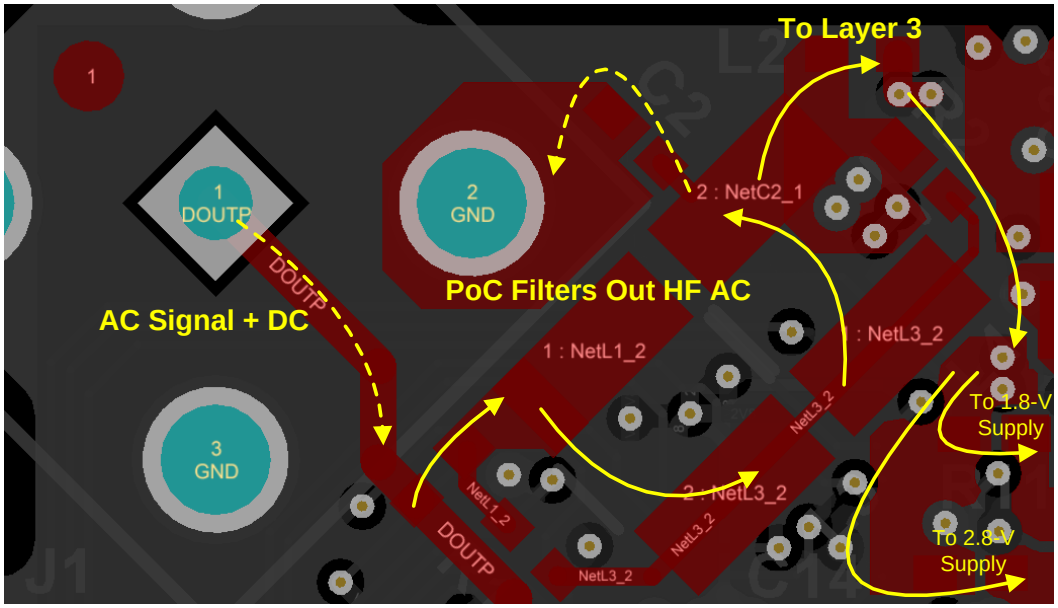
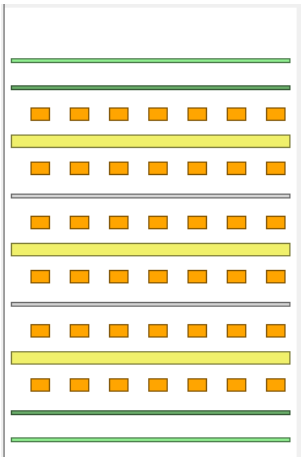


図 39. PoC Layout to Supplies

4.3.4 PCB Layer Stackup Recommendations

The following are PCB layer stackup recommendations. Because automotive is the target space, there are a few extra measures and considerations to take when dealing with high speed signals and small PCBs.

- Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines.
- If using a four layer board, layer two should be a ground plane. Because most of the components and switching currents are on the top layer, this middle ground layer reduces the inductive effect of the vias when currents are returned through the plane.
- An additional two layers were used in this board to simplify BGA and serializer fan out and routing. 図 40 shows the stack up used in this board.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
Top Overlay	Overlay				
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Layer 1 - Top Lay...	Signal	Copper	1.4		
Dielectric 1	Dielectric	Core	10.6	370HR	4.2
Layer 2 - GND	Signal	Copper	1.417		
Dielectric 6	Dielectric	Prepreg	8	370HR	4.2
Layer 3 - Signal	Signal	Copper	1.417		
Dielectric 3	Dielectric	Core	15.6	370HR	4.2
Layer 4 - Signal 2	Signal	Copper	1.417		
Dielectric 4	Dielectric	Prepreg	8	370HR	4.2
Layer 5 - GND	Signal	Copper	1.417		
Dielectric 5	Dielectric	Core	10.6	370HR	4.2
Layer 6 - Bottom...	Signal	Copper	1.4		
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Bottom Overlay	Overlay				

図 40. Layer Stackup

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01002.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01002.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01002.

5 Software Files

To download the software files, see the design files at TIDA-01002.

6 Related Documentation

1. Texas Instruments, *DS90UB913A-Q1 25-MHz to 100-MHz 10/12-Bit FPD-Link III Serializer Data Sheet*
2. Texas Instruments, *TPS6217x-Q1 3-V to17-V 0.5-A Step-Down Converters with DCS-Control™ Data Sheet*
3. Texas Instruments, *Sending Power Over Coax in DS90UB913A Designs Application Report*
4. Texas Instruments, *Cable Requirements for the DS90UB913A & DS90UB914A Application Report*
5. Texas Instruments, *Optimizing the TPS62130/40/50/60/70 Output Filter Application Report*
6. Texas Instruments, *Low-Noise CMOS Camera Supply Application Report*

6.1 商標

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (November 2017) から Revision C に変更 **Page**

- Figure 2: *FPD-Link III Signal Path* 変更 3
- Figure 4: *PCB Top View* 変更 6
- Figure 5: *PCB Bottom View* 変更 6
- Figure 10: *Power Over Coax Schematic* 変更 12
- layout guidelines in Section 4.3.2: *Power Supply Layout* 追加 30
- Figure 33: *1.8-V Supply Component Placement* 変更 31
- Figure 34: *1.8-V Power Plane* 変更 32
- Figure 36: *2.8-V Power Plane* 変更 34
- Figure 37: *High Speed Data Line Trace* 変更 35
- Figure 38: *Input Current Path Through PoC* 変更 36
- Figure 39: *PoC Layout to Supplies* 変更 37
- Figure 40: *Layer Stackup* 変更 37

Revision A (December 2016) から Revision B に変更 **Page**

- 右側の基板の画像 変更 1
- 現行のテンプレートと作成ガイドラインに合わせてデザイン・ガイドを 変更 1
- *The other 1.8-V rail required by the serializer and the imager is provided by the TPS62171-Q1 buck converter.* 削除 3
- *and TPS62171-Q1*, *and 1.8 V*, *through a parallel digital video interface*, and *The serializer converts the*. 追加 3
- Section 2.2.1 Power Supply Topology Evaluation 削除 8
- image and caption for 図 7 変更 8
- image and caption for 図 8 変更 11
- The FPD-Link III interface allows for proper power and high-throughput data transmission and is made up of a PoC filter and the DS90UB913A-Q1. This section discusses the PoC filter followed by a discussion of key parameters when designing with the serializer. 追加 11
- The FPD-Link III interface allows for proper power, high-throughput data transmission, and video data. The interface is made up of a power over coax filter and the DS90UB913A-Q1 device. First the power over coax filter is described, which uses a special new inductor, followed by a discussion of key parameters when designing with the serializer. 削除 11
- 2.3.3.2 変更 13
- 2.3.3.2.1 追加 14
- 2.3.3.2.2 追加 14
- 2.3.3.2.4 変更 16
- 2.3.3.2.5 変更 16
- Section 2.4 I2C Addressing, Section 2.4.1 I2C FPD-Link III Initialization, and Section 2.4.2 Multiple Device Addressing 削除 17
- 3.1.1.1 追加 19
- Section 4.1.4 System Operating Temperature 削除 23
- 3.2.2.1.1 変更 23
- 図 22 追加 24
- Section 4.4.1.4 System Operating Temperature 削除 27
- 3.2.2.2 変更 28
- 図 30 変更 28
- 図 31 変更 29
- title of 4.3.2 from *PoC Filter and Power Supplies* to *Power Supply Layout* 変更 30
- 4.3.2 変更 30
- 図 33 追加 31
- 図 34 追加 32
- 図 35 追加 33

- 図 36 追加 34
- title of 4.3.3 from *Serializer Layout Recommendations* to *High-Speed Trace and PoC Layout* 変更 35
- 4.3.3 変更 35
- 図 37 追加 35
- 図 38 追加 36
- 図 39 追加 37

2016年9月発行のものから更新 **Page**

- Figure 6: *Power Over Coax Schematic* 変更 12
- and replaced 図 32. 削除 29

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