参考資料

TI Designs: TIDA-01492
統合された2MHzのパワー・フロント・エンドおよびマルチフェーズ・プロセッサ電源のリファレンス・デザイン

概要

このプロセッサ電源のリファレンス・デザインは、先進運転支援システム(ADAS)の高性能、単一コア電圧のアプリケーション・プロセッサで使用される、車載用電源ソリューションです。このデザインは、0.9Vで最大10Aのコア電源電流をサポートできます。また、このデザインは広い入力電圧範囲で動作でき、バッテリが逆に接続されても耐えられ、始動-停止および3.5V入力までのコールド・クランクに対応し、出力が中断しません。このソリューションに使用されるすべてのスイッチング周波数は、2MHz以上です。このデザインは、マルチフェーズ構成と電源の内蔵から、本質的に電磁気干渉(EMI)が低く、高い効率を実現します。また、このリファレンス・デザインはCISPR 25 Class 5の伝導性エミッション・テストに準拠した結果を提供します。

リソース

TIDA-01492	デザイン・フォルダ
LP87561-Q1	プロダクト・フォルダ
LM73605-Q1	プロダクト・フォルダ
LM26420-Q1	プロダクト・フォルダ
LM74700-Q1	プロダクト・フォルダ
LM2775	プロダクト・フォルダ
TIDA-00530	プロダクト・フォルダ
TIDA-00699	プロダクト・フォルダ
PMP7233	プロダクト・フォルダ
AutoCrankSim-EVM	ツール・フォルダ

TI E2E™ Community

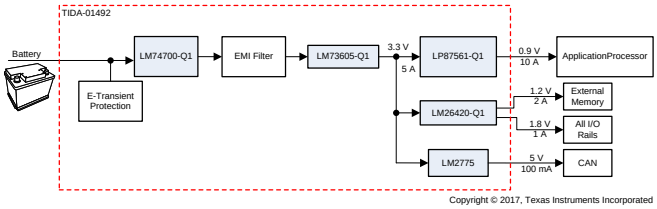
E2Eエキスパートに質問

特長

- 5Aの統合された2.2MHz同期、広い入力電圧範囲の降圧DC/DCコンバータ
- アプリケーション・プロセッサのコア電圧レールに0.9Vで10Aを供給
- スマート・ダイオードのバッテリ逆極性保護により電圧降下が最小限
- 動作範囲3.5V～36Vで、始動-停止およびコールド・クランクをサポート
- インターリーブされた4相のコア電圧電源により、リップル、EMI、インダクタのサイズを最小化
- CISPR 25 Class 5で伝導性エミッションをテスト済み
- 5V CAN電源用の小さな昇圧スイッチト・キャパシタにより、ソリューションのサイズとBOMコストが低減

アプリケーション

- フロント・カメラ
- ドライバー監視システム
- カメラ監視システム
- サラウンド・ビュー
- ADASドメイン・コントローラ



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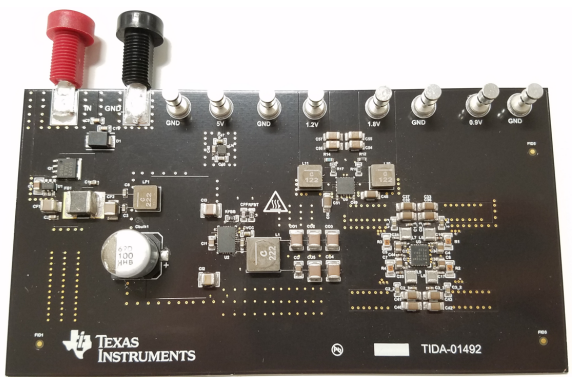

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1 System Description

Camera-based ADAS systems process and analyze video feeds from local or distributed cameras and either output video or use machine-vision algorithms to perceive the environment in and around the car. Such functions are made possible by application processors which typically have specific power requirements. Application processors are used in automotive camera systems such as front camera, mirror replacement, driver monitoring, surround view systems, and to some extent, sensor fusion systems. This design focuses on applications up to 15 W and application processors with single-core voltage domains. This design has been created with the following features in mind:

- Provide 10 A at 0.9 V to single core voltage rail for video application processors
- Minimize electromagnetic interference (EMI) and solution size with a multiphase configuration for the single-core-voltage rail supply
- Limit conducted emissions below CISPR 25 Class 5 conducted emissions limits
- Withstand reverse battery condition
- Operate through start-stop and cold-crank down to 3.5 V
- Optimize the individual blocks for smallest possible solution size
- Provide power for CAN PHY and external DDRx memory

図 1 shows an example of a front camera system.

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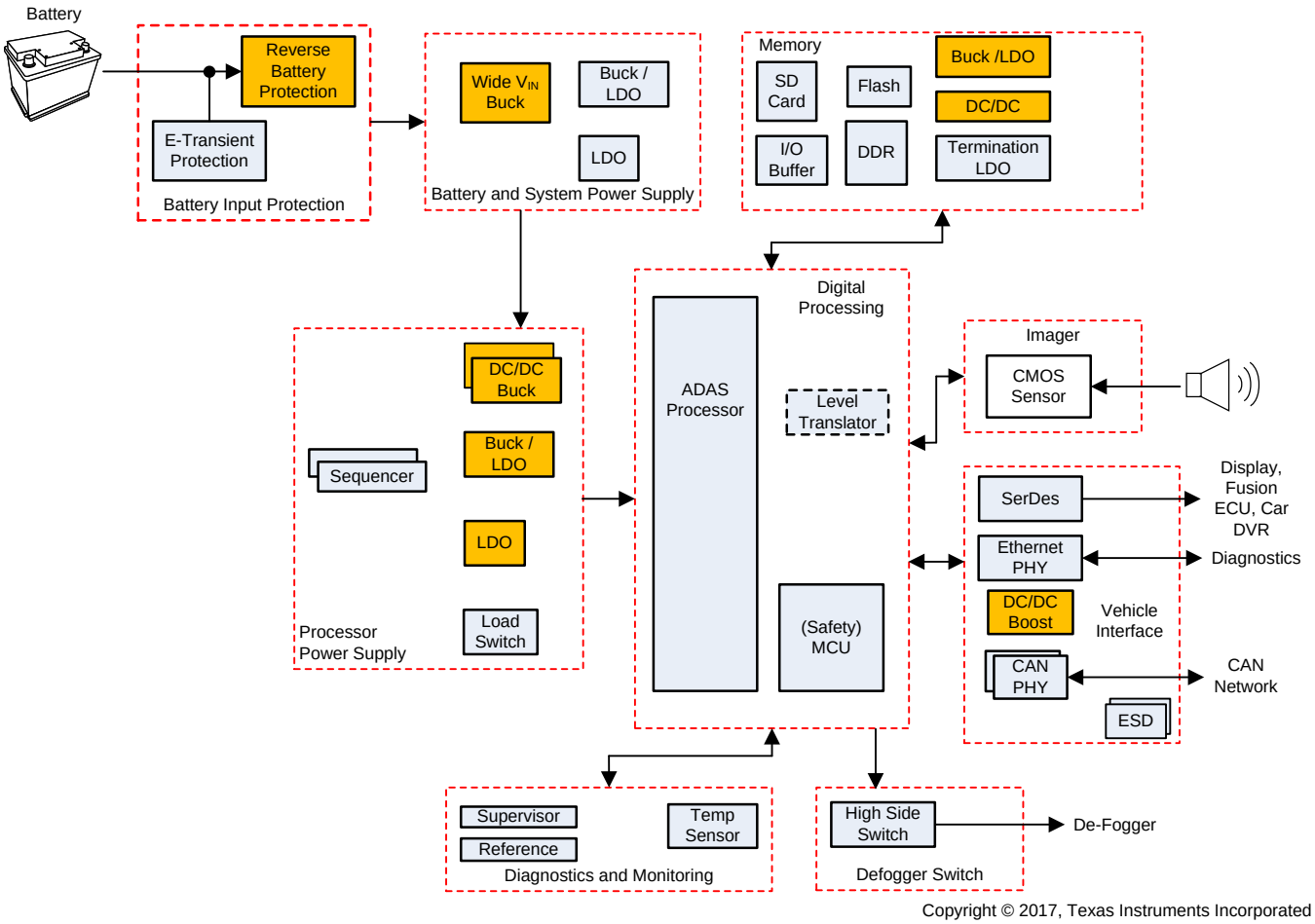

図 1. Example of Front Camera Block Diagram

These camera systems vary in the location of cameras and the number of cameras and processors. The red blocks are all components located on the TIDA-01492 board and which cover the power requirements for an application processor. Functionality, such as voltage supervision and sequencing, are partially integrated into the integrated circuits (ICs). 図 2 shows each subsystem and block on the actual TIDA-01492 board.

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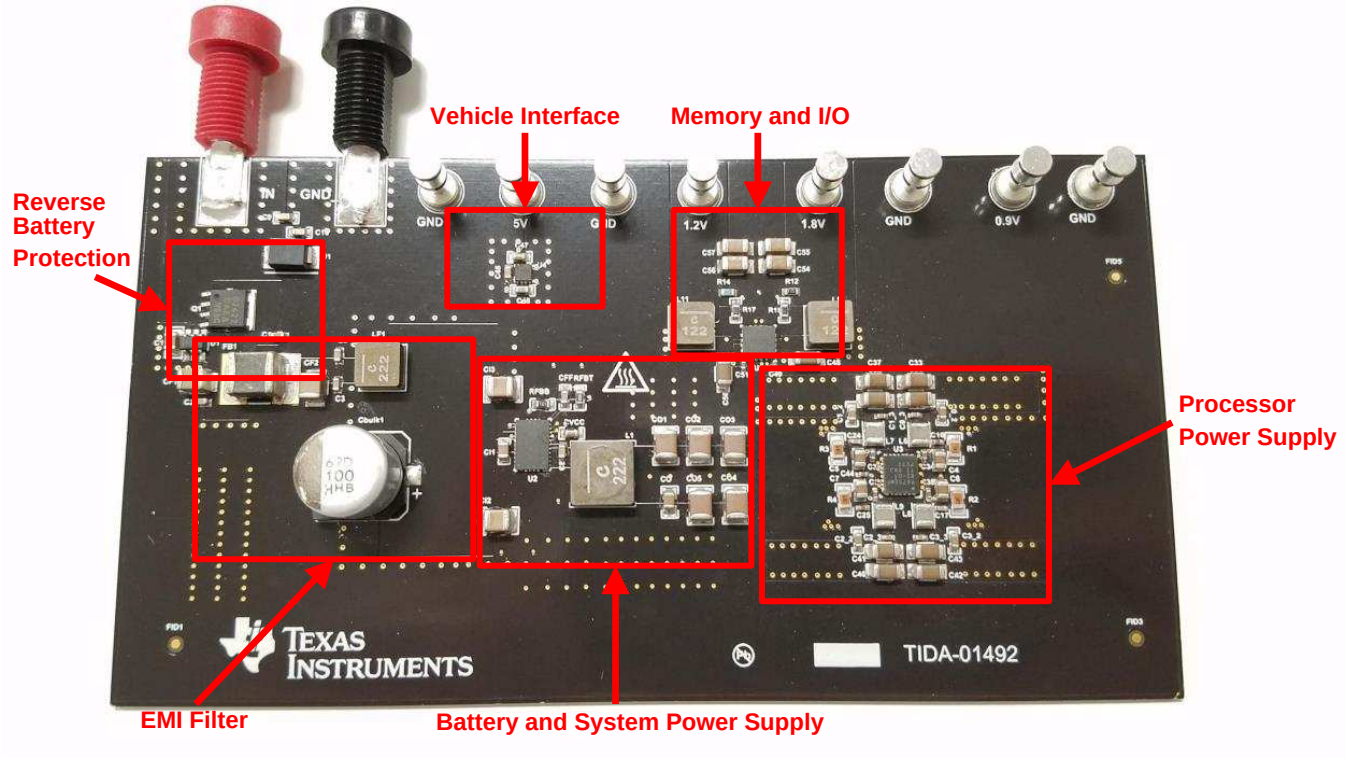

図 2. TIDA-01492 Subsystems Highlight

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
SYSTEM INPUT						
V_{IN}	Input voltage	Battery voltage range (DC)	3.5	13.5	36.0	V
V_{CORE}	Core-voltage supply output voltage	—	—	0.9	—	V
I_{CORE}	Core-voltage supply output current	—	—	—	10.0	A
$V_{I/O}$	I/O supply voltage	—	—	1.8	—	V
$I_{I/O}$	I/O supply output current	—	—	—	1.0	A
V_{MEMORY}	Memory supply voltage	—	—	1.2	—	V
I_{MEMORY}	Memory supply output current	—	—	—	2.0	A
V_{CAN}	CAN supply voltage	—	—	5.0	—	V
I_{CAN}	CAN supply output current	—	—	—	0.1	A
F_{SYS_SW}	Switching frequency	Switching frequency of all supplies in system	2.0	—	—	MHz

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2 System Overview

2.1 Block Diagram

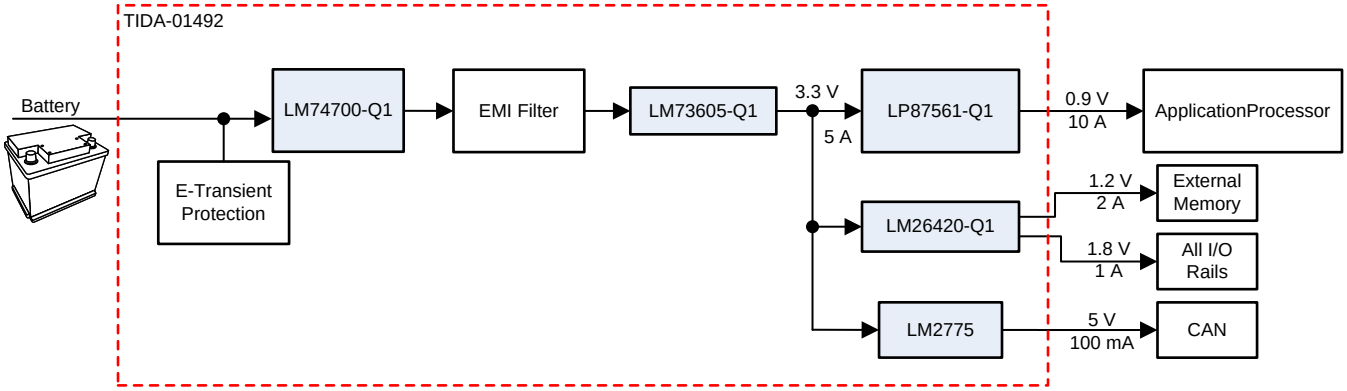

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図 3. Power Solution for Single-Core-Voltage Application Processors

2.2 Highlighted Products

This reference design uses the following TI products:

- LM73605-Q1: 5-A synchronous buck converter with a wide input voltage range from 3.5 V to 36 V (42-V transients), enabling the device to work directly from an automotive battery
- LP87561-Q1: Four-phase, 16-A buck converter with I^2C compatible serial interface designed to meet power management requirements for the latest automotive processor applications
- LM26420-Q1: Highly-efficient, dual, 2-A synchronous buck converter with independent power good and precision enable for each output
- LM2775: Highly-compact, switched-capacitor 5-V boost converter
- LM74700-Q1: The "Always On Smart Diode Controller" is a high-side N-channel field-effect transistor (N-FET) controller with ultra-low forward voltage drop intended for reverse-battery protection

The following subsections detail each device and explain their selection for this application.

2.2.1 LM73605-Q1

The LM73605-Q1 is the main system supply in this reference design. The wide input voltage range, high integration, and fast switching at 5-A make this device a top choice for the wide input, voltage power front end. The switching frequency of the device is adjustable between 350 kHz to 2.2 MHz. The switching frequency is selected to be 2.2 MHz because there should be minimal interference in the AM band (530 kHz to 1.8 MHz) for all automotive applications. The benefit to switching above the AM band rather than below is that the faster switching frequency reduces the physical size of the output inductor and decreases the total solution size.

Though not used in this reference design, this switcher supports external clock synchronization to avoid beat frequencies between multiple converters or to allow a master to dither the clock signal. This feature can be very useful for optimizing systems for EMI performance.

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2.2.2 LP87561-Q1

The LP87561-Q1 contains four step-down DC-DC converter cores configured to a four-phase single output configuration to power a single-core voltage rail of an automotive video applications processor with 10 A at 0.9 V. The designer can control and configure the device over the I^2C interface. The maximum output current of the device is actually 16 A (4 A per phase); however, the designer must consider thermal limitations.

For application processor power delivery, a multiphase synchronous buck converter offers several advantages over a single power stage converter. The load current in a multiphase converter is shared evenly among interleaved phases, which eases the inductance and saturation current requirements for each output inductor. Less inductance allows for higher dynamic current, which improves transient response and recovery times. An added benefit is that the heat generated is greatly reduced for each channel due to the fact that current is shared between phases.

The buck regulators switch at 2 MHz, which meets the requirement to stay above the AM band.

Although this device is not used in this reference design, it does have internal sequencing, which allows for some systems to eliminate the requirement for external sequencer ICs, further reducing the solution footprint. This device also supports remote differential voltage sensing, programmable start-up and shutdown delays, using an external clock input for switching, spread-spectrum, and phase interleaving.

2.2.3 LM26420-Q1

The LM26420-Q1 is a dual, 2-A integrated buck regulator providing 2 A at 1.2 V to memory and 1 A at 1.8 V to the I/O voltage in this design. The switching frequency of this device is 2.2 MHz, which is above the AM band. Each output has independent power good and precision enable signals. This design does not have a sequencing requirement, so these signals remain unused.

The 2-A, 1.2-V supply is intended for 1GB of DDR3 memory, which is sufficient for the targeted low-end processing applications and the 1-A, 1.8-V supply provides sufficient headroom for the I/O.

2.2.4 LM2775

The LM2775 is a fixed, 5-V switched capacitor boost converter for CAN PHY. Compared to an inductor-based solution, the switched capacitor approach reduces the total solution size. The device switches above the AM band at 2.0 MHz. Because 5 V at 200 mA is required for a single CAN PHY, this device is optimized for single CAN PHY applications. The package is a very small 2×2-mm WSON. The only required external components are the I/O capacitors and switched capacitor.

The LM2775 has output disable control. When the device is in shutdown, setting the OUTDIS pin high or low pulls the output voltage to GND or leaves the output in a high impedance state.

2.2.5 LM74700-Q1

The LM74700-Q1 is used for low-loss reverse polarity protection. Using a charge pump, this device controls an external N-FET in series with the battery supply input to act as an ideal diode, with a very-low voltage drop and power loss as opposed to a discrete diode solution. This controller is "Always On" to avoid periodic voltage drops at the input. After detecting a reverse-battery condition, the device quickly turns off the field-effect transistor (FET) that isolates and protects the downstream circuitry.

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The voltage drop across the FET is negligibly small, which allows for more input voltage headroom for the wide input voltage buck converter, permitting it to operate at even lower battery input voltages. For example, a cold-crank condition occurs when the battery tries to energize the starter of the engine and the battery voltage drops as low as 3.5 V. With a diode solution, the voltage at the input of the buck converter will be 3.5 V minus the typical diode drop of 0.7 V or 2.8 V. This input voltage is too low for the converter to regulate the 3.3-V system voltage. With the smart diode solution, input voltage at the buck will be close to 3.5 V during this condition and will continue to regulate.

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2.3 System Design Theory

2.3.1 Printed-Circuit Board (PCB) and Form Factor

This design does not have any specific requirements for the board geometry. The main objective is to have as small of a solution size as possible for each supply. 図 4 shows a three-dimensional (3-D) rendering of the PCB, followed by a labeled photograph of the actual board in 図 5.

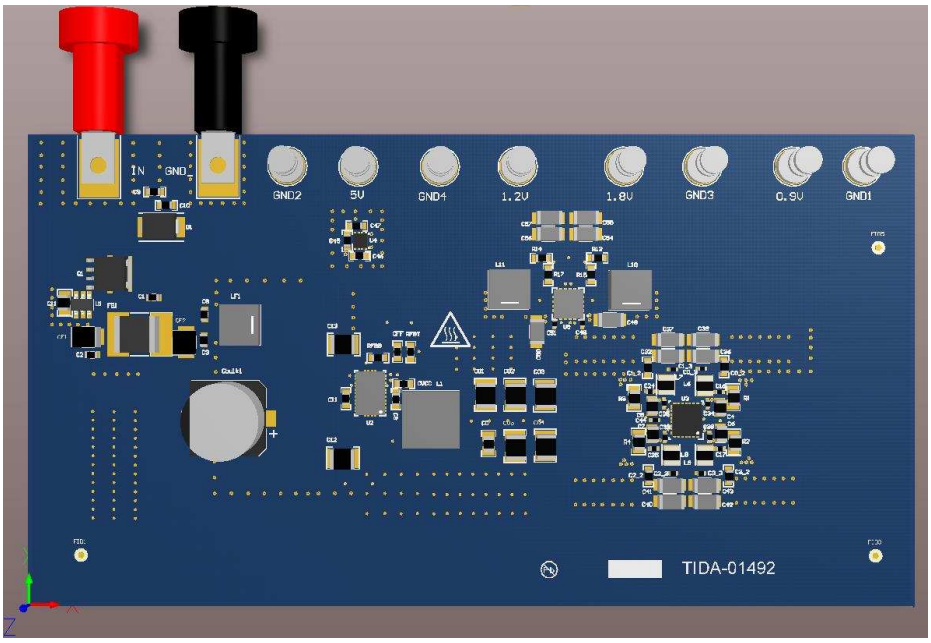

図 4. TIDA-01492 PCB Render

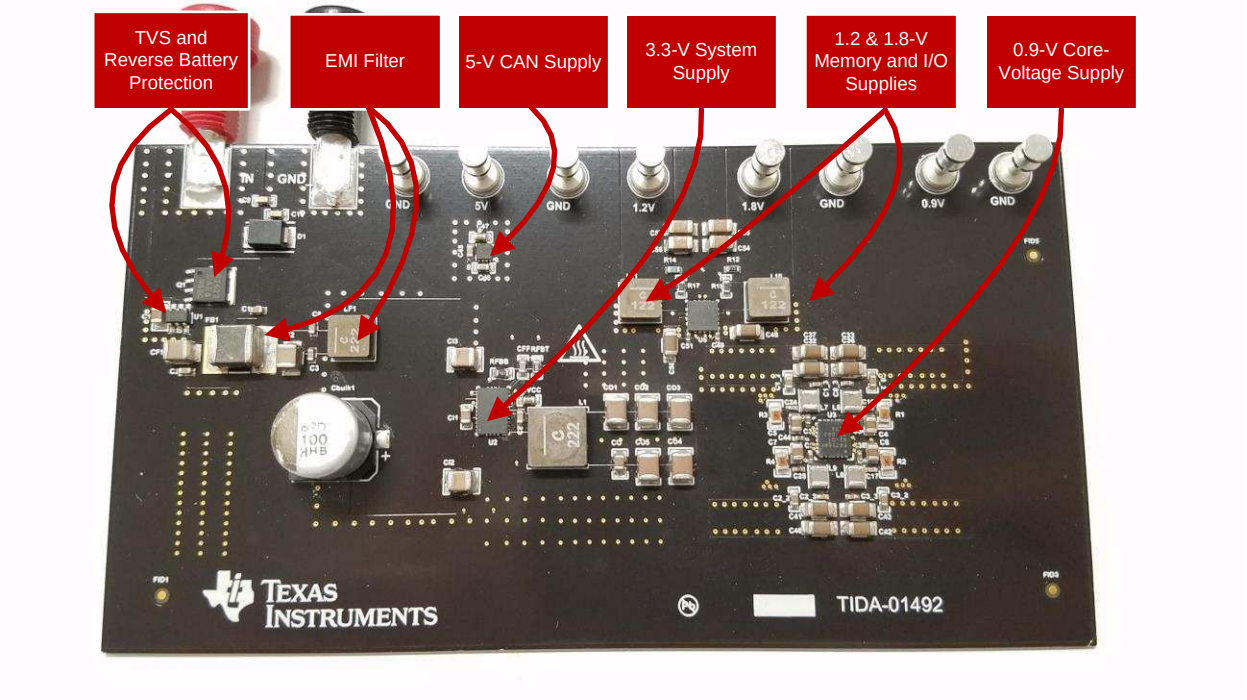

図 5. TIDA-01492 Labeled Supplies and Components

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2.3.2 Input Protection and Wide-V_{IN} DC-DC

2.3.2.1 TVS Diodes

Transient voltage suppression (TVS) diodes are required on the supply input of the system to protect against both positive and negative going transients. The transients of concern are detailed in ISO 7637-2:2004, pulses 1 and 2a. Many systems in a car can simply shut down during these transients until the condition passes; alternatively, many ADAS applications require continuous operation. For this reason, the transients must be shunted instead of using an overvoltage shutdown scheme.

図 6 shows a schematic of the input transient protection.

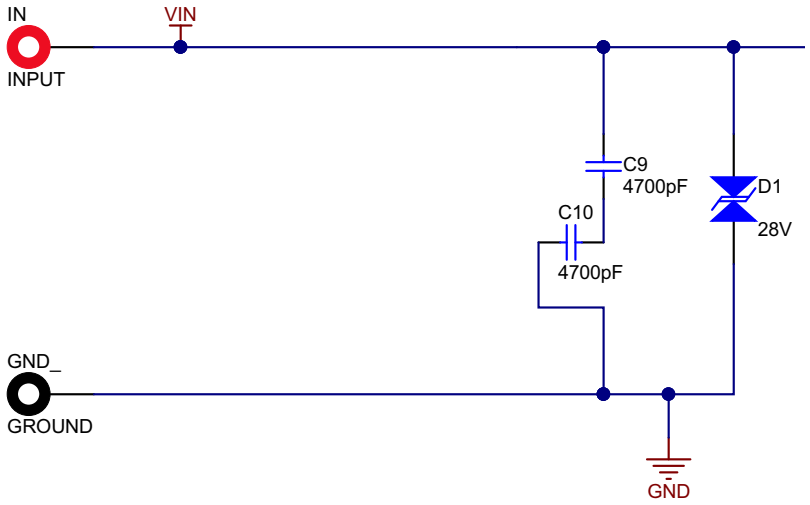

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図 6. Input Transient Protection

The diode breakdown voltages have been chosen such that transients are clamped at voltages that protect the MOSFET and the rest of the system. The positive clamping device must clamp above a double-battery (jump-start) and clamped load dump voltages, but lower than the maximum operating voltage of the downstream devices. In this case, the requirement is to clamp around 28 V but have a maximum clamping voltage below 40 V. Ideally, the best choice is to specify 36 V as the approximate maximum clamping voltage.

The reverse clamping device must clamp all negative voltages greater than the battery voltage so that it does not short out during a reverse-battery condition.

Due to the energy of the pulses, SMD-sized TVS diodes with 600-W instantaneous peak power ratings are the required minimum specification. This design uses a 600-W, 28-V bidirectional TVS diode.

2.3.2.2 Reverse Battery Protection

Reverse battery protection is a requirement in nearly every electronic subsystem of a vehicle, both by original equipment manufacturer (OEM) standards as well as ISO 16750-2, an international standard that pertains to supply quality.

図 7 shows a schematic of the reverse battery input protection.

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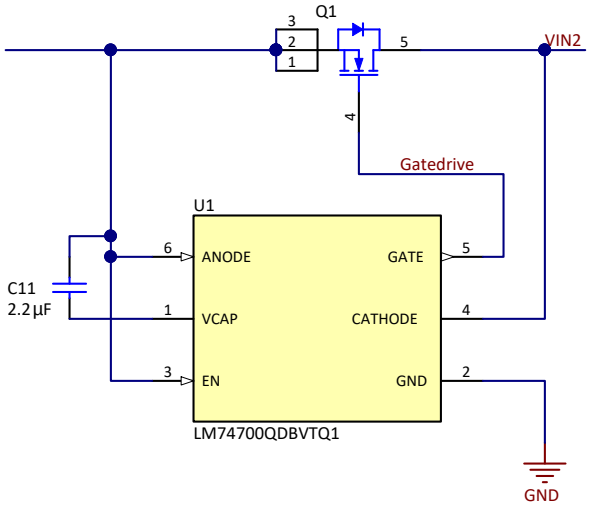

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図 7. Reverse Battery Input Protection

Rather than use the traditional diode rectifier solution for reverse battery protection, this implementation uses an N-channel MOSFET driven by the LM74700-Q1 device. The power dissipation of a discrete diode solution is significantly higher due to the typical 600-mV to 700-mV forward drop. A very-low forward voltage drop can be achieved using low $R_{DS(ON)}$ external N-channel MOSFETs. This low forward voltage drop from the supply to the system yields much higher efficiency, less heat, and a lower input voltage operating range while protecting the system from a reverse polarity condition.

The FET must have a rating which is at least as high as the clamped input voltage. This reference design uses a 40-V N-FET with a 2-V gate-source threshold voltage.

2.3.2.3 Input Capacitors Exposed to Battery Inputs

The final consideration for the front-end protection is the input capacitors. This design uses two, 100-V rated capacitors in series between the battery line and ground, which effectively makes a 200-V rated capacitor of half the nominal capacitance value, to suppress voltage transients detected at the input to protect downstream devices.

2.3.2.4 Input EMI Filter

The schematic in 図 8 shows the EMI filter at the system supply input, after the reverse battery protection.

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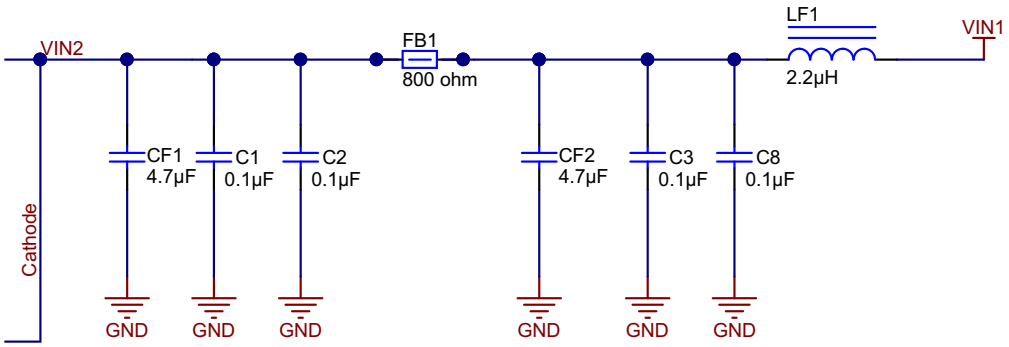

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図 8. Input EMI Filter Schematic

Because the switching frequency of the main supply is 2.2 MHz, this EMI filter inductor requirement can be eased. Filtering out frequencies below the AM band typically requires larger inductors with more inductance, usually 10 µH or more, as more inductance provides more impedance at lower frequencies. Decoupling capacitors C3 and C8 filter out the high-frequency noise that the inductor LF1 cannot attenuate.

The ferrite bead FB1 has a higher resonant frequency than inductor LF1, around 100 MHz. The impedance due to the higher resonant frequency attenuates any unfiltered noise around this 100-MHz band that has been conducted upstream from the LF1-CF2 node to VIN2 and acts as a high-frequency current choke by increasing the impedance for higher-frequency currents from the larger upstream loop, from VIN2 to downstream components after VIN1. Similar to capacitors C3 and C8 after LF1, the decoupling capacitors C1 and C2 provide a low impedance path for high-frequency currents to ground.

When selecting and adding decoupling capacitors, it may seem attractive to simply add more capacitors. No matter how much decoupling is used, designers must take careful consideration to avoid parallel resonances resulting from the unseen parasitics of the passives. Parallel resonances can cause EMI problems that may be difficult to pinpoint and address.

While it is critical to select the right components for the EMI filter, strategically laying out these components is equally critical for an effective EMI filter.

2.3.2.5 Wide Input Voltage Buck Converter

The LM73605-Q1 is an AECQ100-qualified, wide-input voltage buck regulator used as a front-end supply to provide a 3.3-V system voltage. With a nominal input voltage range of 3.5 V to 36 V and transients up to 42 V, the device can continue operation through most battery conditions such as start-stop, cold-crank, and load dump.

図 9 shows a schematic of the wide input voltage buck.

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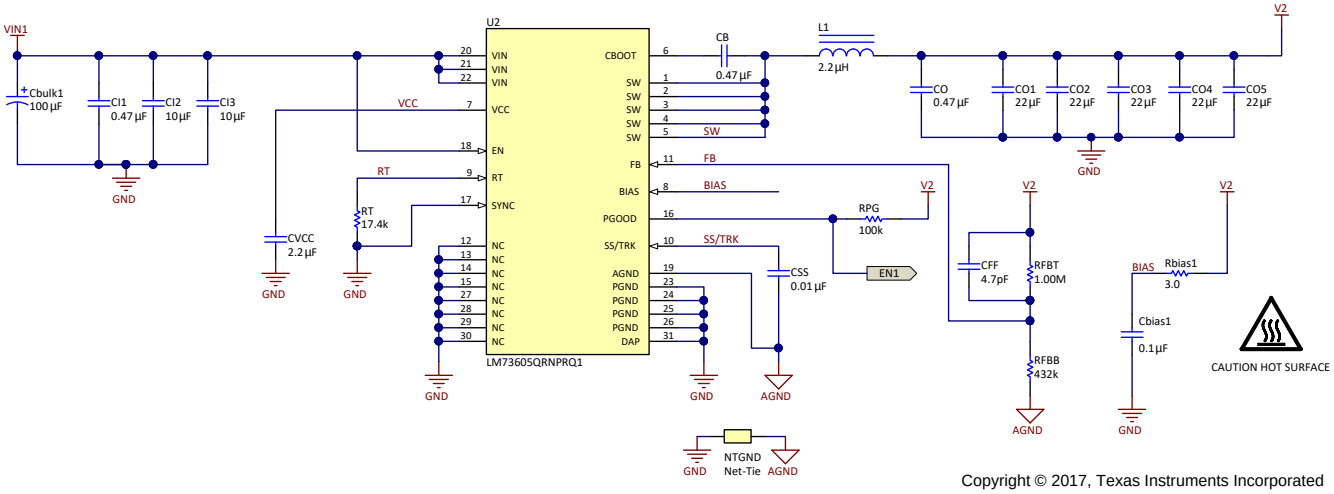

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図 9. Wide Input Voltage Buck

The LM73605-Q1 delivers 5 A at a 2.2-MHz switching frequency in the above configuration. The previous 図 9 shows both RT and SYNC pulled to ground. This setup configures the device for a 2.2-MHz switching frequency and a light load architecture (PFM), which means that the device lowers its switching frequency for lower current loads.

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2.3.3 Power Supply Design Considerations

For this power supply, choose inductors such that:

- The ripple current is between 20% to 40% of the load current I_{LOAD} with the given switching frequency, input voltage, and output voltage. This reference design uses 40%.
- The temperature ratings are appropriate for automotive applications, typically –40°C to 125°C for ADAS applications.
- Saturation current is chosen per 式 1 for peak current, plus additional margin.

$$I_{SAT} \left(I_{LOAD} + 0.5 \times I_{RIPPLE}\right) \times 1.2 \quad (1)$$

An important recommendation for ADAS applications is selecting ceramic capacitors that use X7R dielectric material, which ensures minimum capacitance variation over the full temperature range. The voltage rating of the capacitors must be greater than the maximum voltage and twice the typical voltage across its terminals to avoid DC bias effects. The amount of output capacitance used depends on output ripple and transient response requirements, for which there are many equations and tools available online to help estimate. The supplies in this solution have been designed for a ±2.5% total transient response. Low equivalent series resistance (ESR) ceramic capacitors have been used exclusively for the purpose of reducing ripple. For internally-compensated supplies, see the device-specific data sheets, as they may have limitations on acceptable LC output filter values.

ICs must always be qualified per AECQ100. TI parts that are qualified typically have part numbers ending in "-Q1".

For improved accuracy, all feedback resistor dividers must use components with 1% tolerance.

2.3.3.1 LP87561-Q1 Core-Voltage Supply

The LP87561-Q1 is a four-phase single output device. Rather than using external resistor dividers to set core configurations, operating modes, slew rates, and status signal delays, the device is configurable through an I^2C interface. In this design, the I^2C lines are unused and the device runs in the default state. The default values of key device parameters are defined as follows:

- V_{OUT} = 0.9 V
- Forced pulsed width modulation (PWM) mode
- Automatic phase adding and shedding
- Switch current limit = 5 A
- Output voltage slew rate = 10 mV/µs
- Start-up delay = 0 ms
- Shutdown delay = 0 ms

図 10 shows the schematic for the device.

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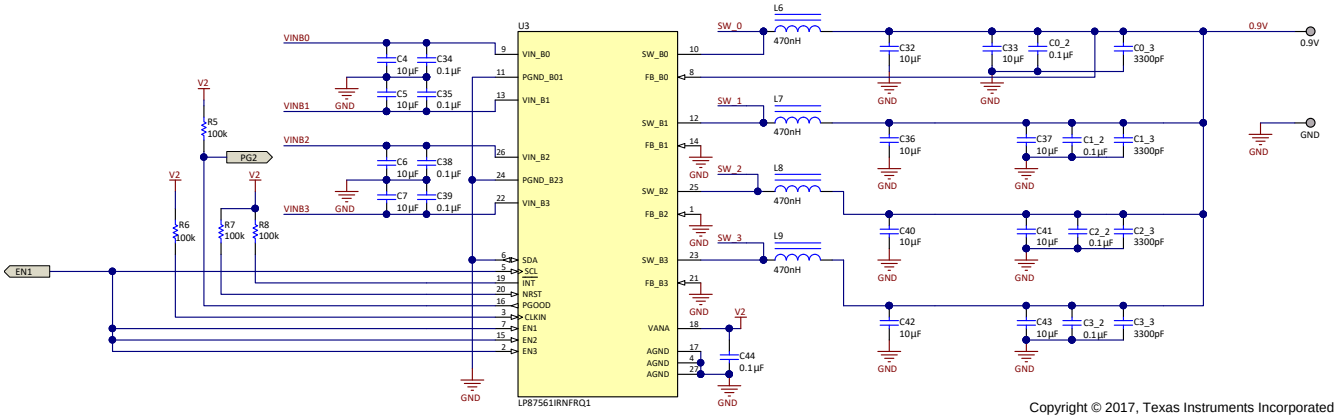

図 10. Core-Voltage Supply Schematic

For more detail on the design procedure and component selection, see *LP87561F-Q1 Four-Phase 16-A Buck Converter With Integrated Switches* (SNVSAS3). The following subsections describe the input EMI filters and snubber circuits for each phase.

2.3.3.1.1 LP87561-Q1 Input EMI Filter

図 11 shows the schematic for the EMI filter for each phase input.

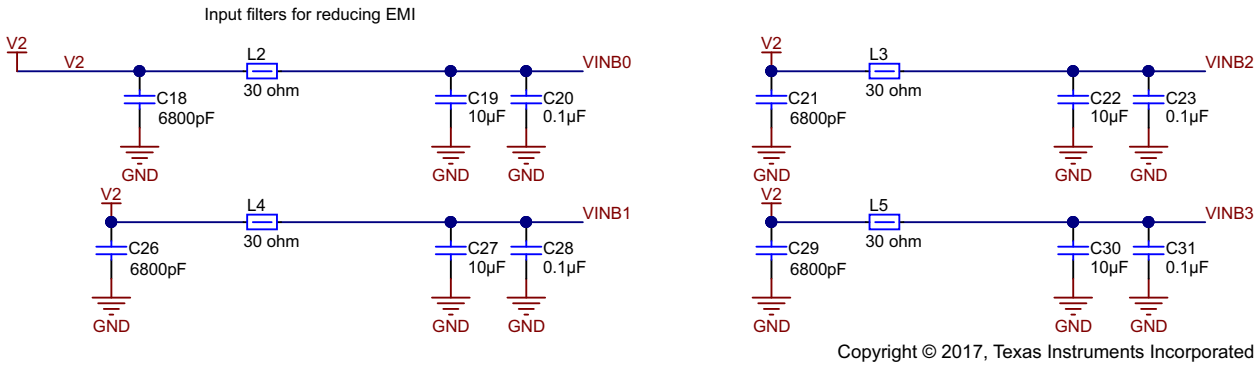

図 11. Input EMI Filter for Each Phase

These input EMI filters are pi filters. Similar to the system input EMI filter that addresses, the ferrite bead acts as both an AC current-loop choke from a larger upstream loop and an attenuator of high-frequency noise conducted back into the system. A 30-Ω ferrite bead has been selected for low DCR, and 30 Ω at 100 MHz is a good starting point for increasing or decreasing the impedance of the larger loop upstream. This impedance is not required to be very high, but just high enough for high-frequency currents to flow through lower impedance paths through the decoupling capacitors, which form a tight loop with the supply input and output. The 6800-µF capacitor provides a low-impedance path to ground for the very-high-frequency noise conducted back into the system that has not been suppressed by the ferrite bead.

Component values have been selected based on commonly-used and suggested values and are simply intended to serve as a starting point. Component value optimization is empirical. Note that the layout of these components is just as important as the component values. A bad layout can make a thoroughly-designed filter schematic useless or even introduce problems into the circuit.

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2.3.3.1.2 LP87561-Q1 Snubber Circuits

Switch node ringing can cause problems for a device or system. Here, the main concern is that the switch node does not create EMI problems, which is addressed by using a snubber circuit. 図 12 shows the schematic of the snubber circuit for each phase output.

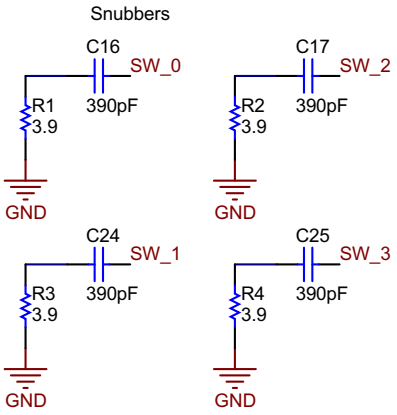

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図 12. Output Snubber Circuit for Each Phase

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The snubber circuit reduces switch node ringing at an efficiency cost by filtering out the higher frequencies (> 100 MHz) due to the high dv/dt at the switch node.

Component values have been selected based on commonly-used and suggested values and are simply intended to serve as a starting point. Component value optimization is empirical. The layout of these components is just as important as the component values. A bad layout can make a thoroughly-designed filter schematic useless or even introduce problems into the circuit.

2.3.3.2 LM26420-Q1 Memory and I/O Supply

The switching frequency of the LM26420-Q1 is preset to 2.2 MHz, which reduces the size of output inductors and maintains a small total solution size. The current mode architecture of the IC simplifies the regulator compensation, reducing design time and requiring fewer external components than voltage mode regulators. The device output voltage regulation uses current-mode control, which provides fast transient response. The device is internally compensated, which further reduces the total solution size.

図 13 shows the memory and I/O supply schematic.

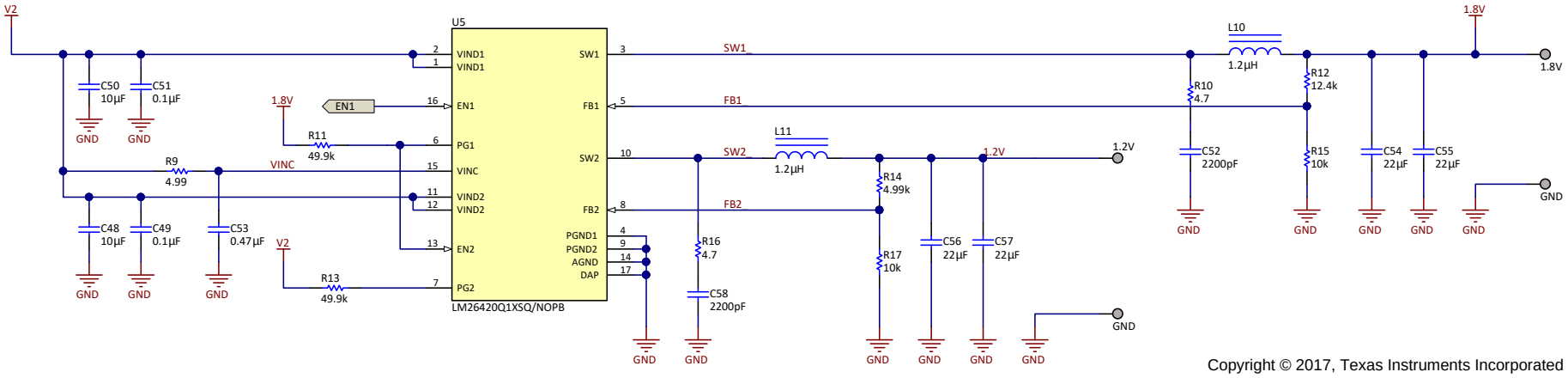

図 13. Memory and I/O Supply Schematic

For more detail on the design procedure and component selection, see *LM26420/LM26420-Q0/Q1 Dual 2-A Automotive-Qualified, High-Efficiency Synchronous DC-DC Converter*.

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2.3.3.3 LM2775 5-V CAN Supply

The LM2775 device provides the 5-V output voltage required for a CAN bus (see 図 14).

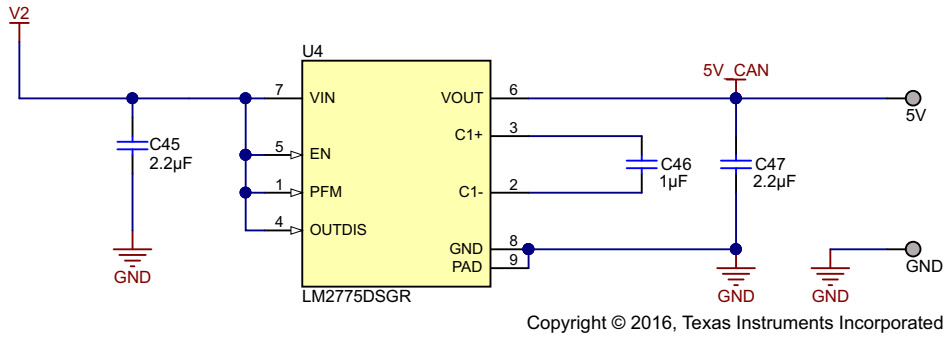

図 14. 5-V CAN Supply Schematic

For more details on the device, see *LM2775 Switched Capacitor 5-V Boost Converter*.

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3 Getting Started Hardware

3.1 Hardware

To get started with the TIDA-01492 board, simply connect the leads to the banana jack on the top-left corner of the board. The screw terminals are labeled IN and GND to indicate the correct polarity of the supply (see 図 15).

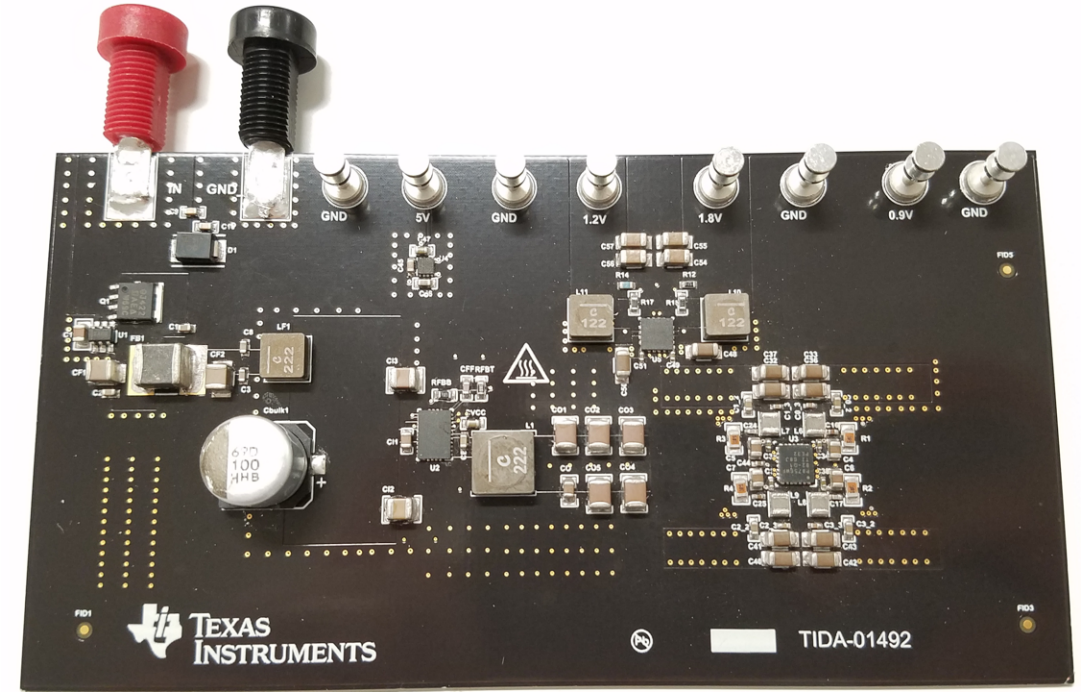

図 15. Board Input Terminals

Connect a power supply that is capable of at least 13.5 V and 2 A to the leads to supply power.

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4 Testing and Results

The following information shows how to set up for the various tests performed on this design.

To perform pulse testing, this design used the AutoCrankSim-EVM: Simulator for Automotive Cranking Pulses Evaluation Module Board. This board is available for purchase at: AUTOCRANKSIM_EVM: Simulator for Automotive Cranking Pulses Evaluation Module Board. If the designer wishes to build the board or simply view the design files, use the power design files from: PMP7233 Cranking Simulator Reference Design for Automotive Applications.

4.1 Test Data

The following subsections show the test data from characterizing the switching power supplies in the system.

4.1.1 Load Regulation and Efficiency

This section presents and discusses the core-voltage supply load regulation and two-stage efficiency test results. 図 16 shows the output voltage variation of the 0.9-V core-voltage supply with varying load current, from no load to full load.

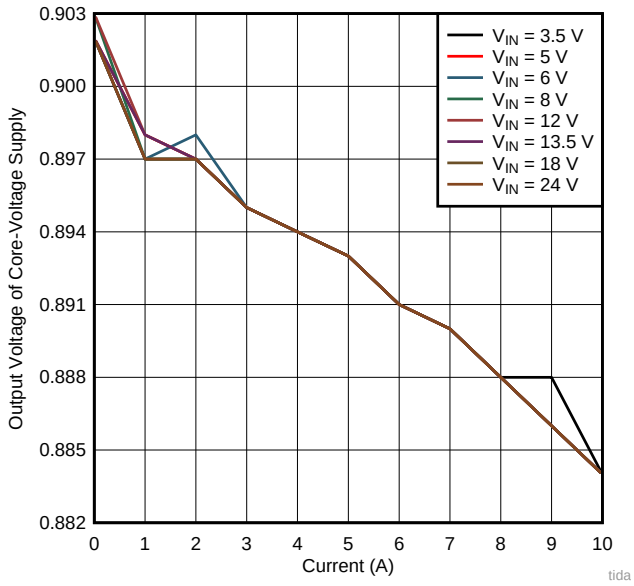

図 16. Load Regulation of Core-Voltage Supply

A close examination of the previous 図 16 shows that the maximum measured deviation from the nominal output of the 0.9-V supply is 1.778%. This value comes from estimating the measured output voltage to be 0.884 V at the full load and nominal input voltage.

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The following 図 17 shows the efficiency of the two-stage approach used in this design. The two-stage approach consists of the LM73605-Q1 main 3.3-V system supply feeding the LP87561-Q1 core-voltage supply for the application processor. Output voltage and current measurements were taken across an input voltage range of 3.5 V to 24 V.

図 17 plots the data linearly for both x- and y-axes.

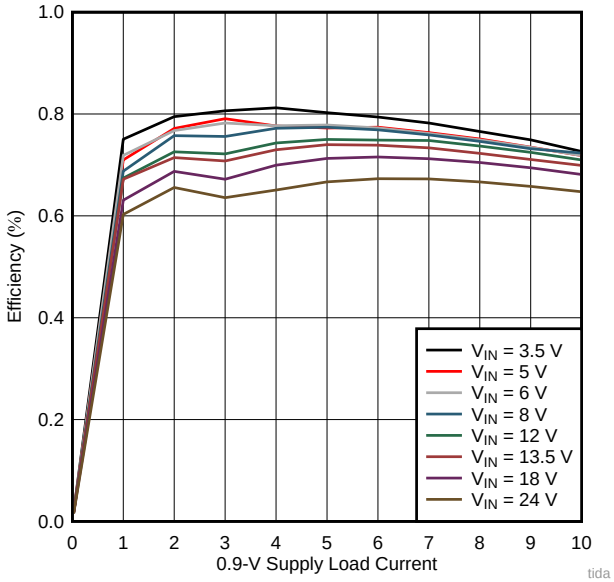

図 17. Two-Stage Efficiency, Linear Plot

図 18 shows the efficiency with varying input voltage and the full 10-A load.

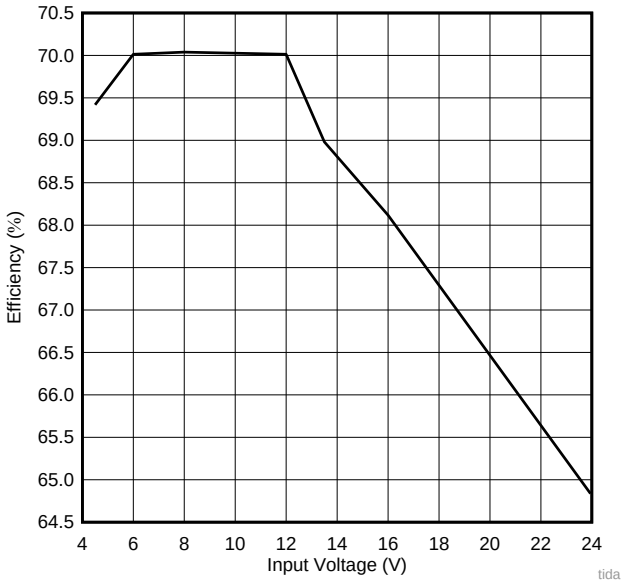

図 18. Full Load Efficiency for Varying Input Voltage

As expected, the measured peak efficiency appears to be around 8 V, with the efficiency dropping off as the input voltage increases.

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4.1.2 Switch Node Waveforms and Output Voltage Ripple

The following 図 19, 図 20, and 図 21 show the switch node and output voltage ripple at the full load of each DC-DC converter. The first set of scope shots show the switch node for the main 3.3-V system supply, LM73605-Q1, with a 4.5-V, 13.5-V, and 20-V input voltage. Channel 1 (yellow) shows the switch node waveform and channel 2 (pink) shows the output voltage ripple. The output voltage ripple measurements were AC coupled. Note that all switching frequencies are above 2 MHz.

The scope shots show that the switching frequency of the supply sits around 2.1 MHz, except with a 4.5-V input voltage.

図 19. LM73605-Q1 Switch Node and Output Voltage Ripple, 13.5-V Input at Full Load

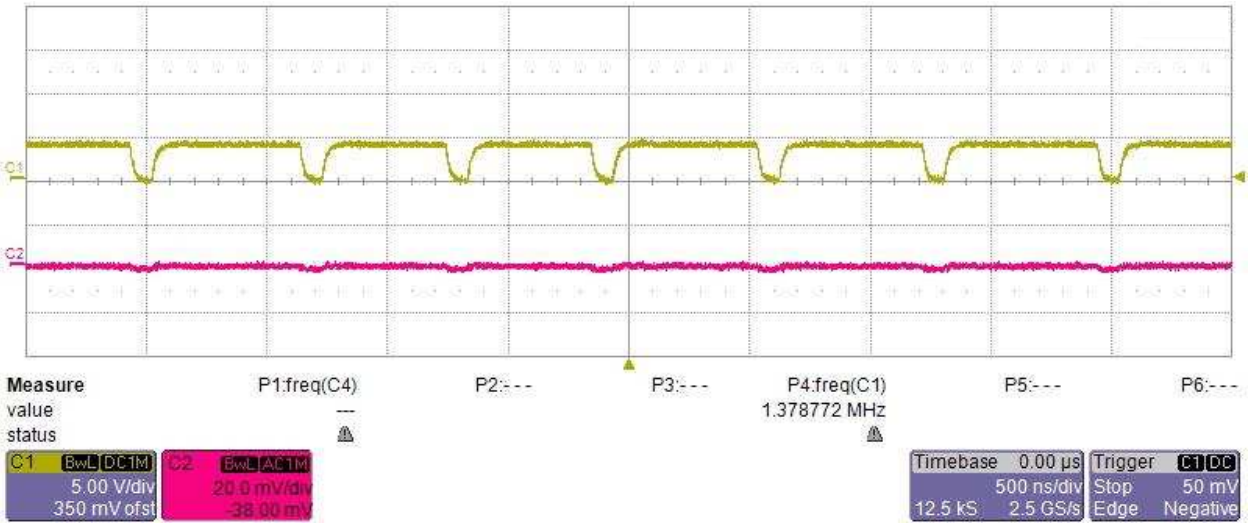

図 20. LM73605-Q1 Switch Node and Output Voltage Ripple, 4.5-V Input at Full Load

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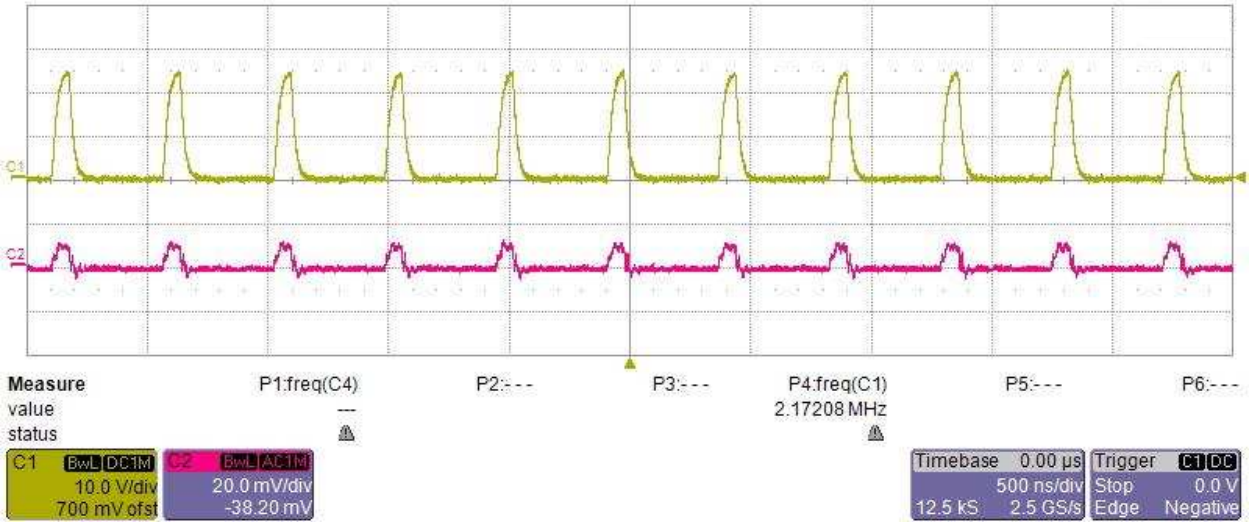

図 21. LM73605-Q1 Switch Node and Output Voltage Ripple, 20-V Input at Full Load

図 22 and 図 23 show the switch node and output voltage ripple for the memory and I/O supply, LM26420-Q1. The first scope shot shows the 1.2-V output, followed by the 1.8-V output.

The screen shots show the switching frequency to be around 2.25 MHz for both switcher outputs.

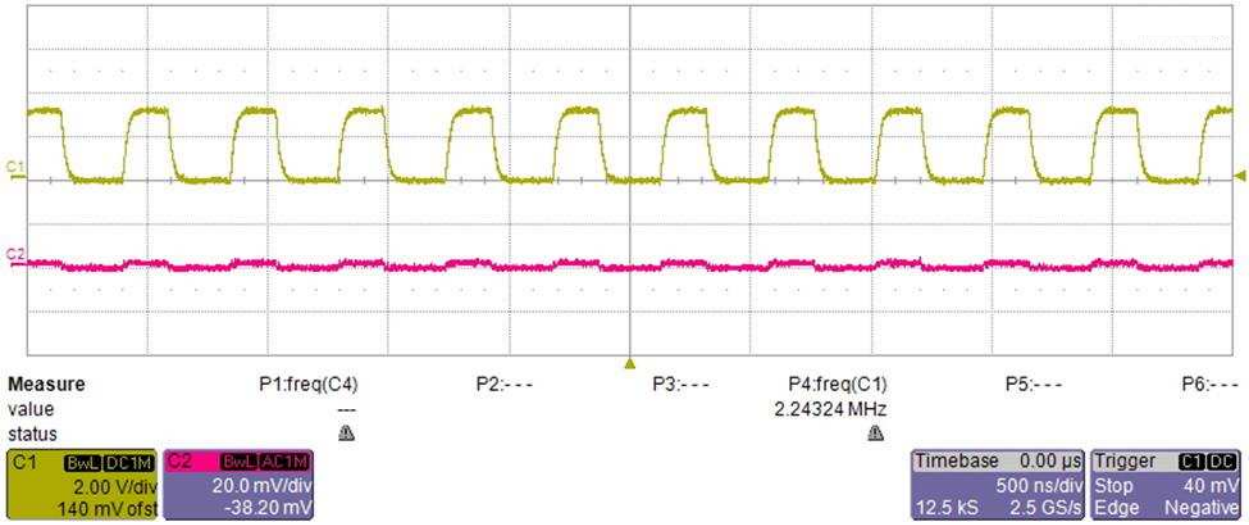

図 22. LM26420-Q1 Switch Node and Output Voltage Ripple, 1.2-V Output at Full Load

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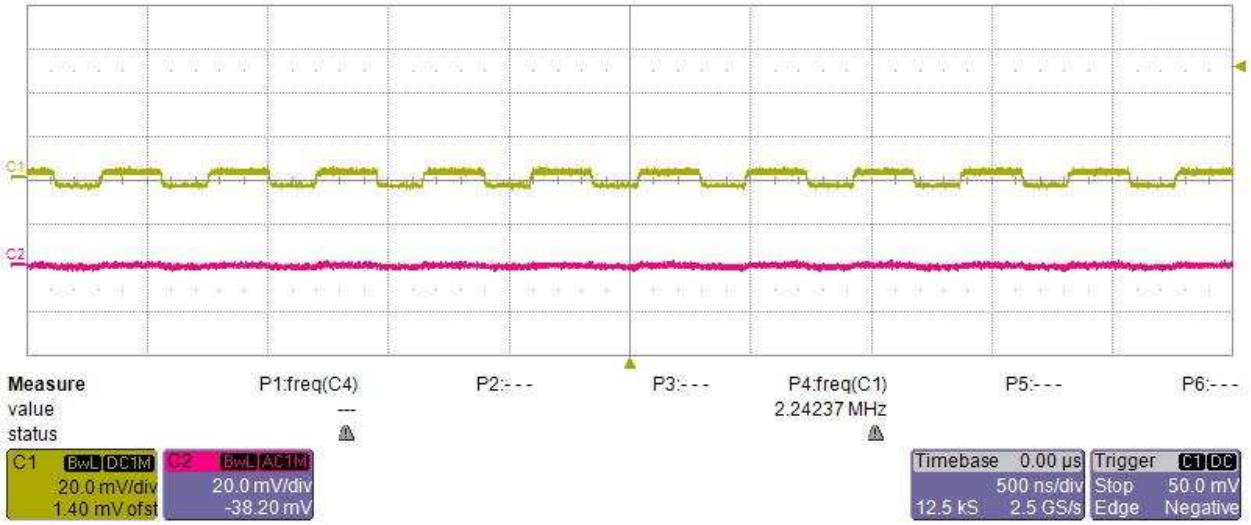

図 23. LM26420-Q1 Switch Node and Output Voltage Ripple, 1.8-V Output at Full Load

図 24 shows the 5-V CAN supply switch node and output voltage ripple. The switching frequency for the CAN supply is 2 MHz.

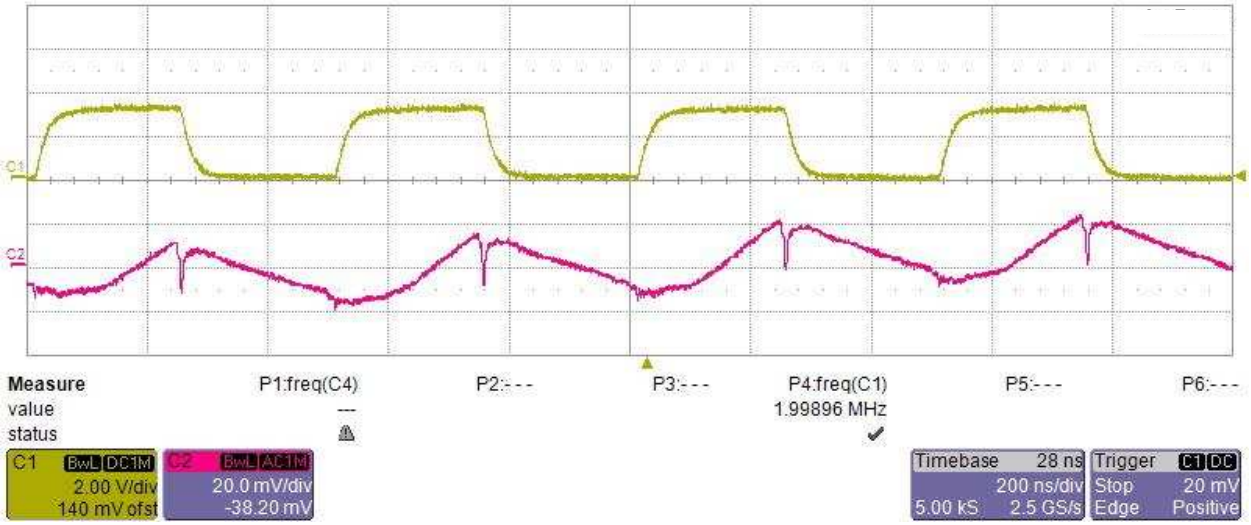

図 24. LM2775 Switch Node and Output Voltage Ripple, 5-V Output and Full Load

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図 25 shows the switch node and output voltage ripple for the 0.9-V core-voltage supply. The switching frequency for the core-voltage supply is 1.9 MHz and the output voltage ripple is less than 5 mV.

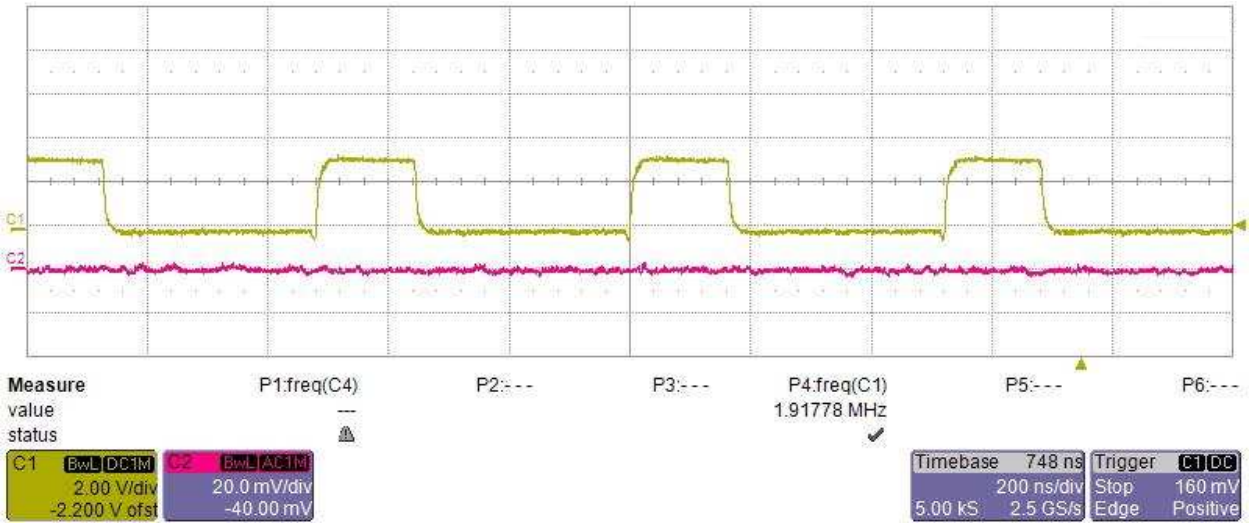

図 25. LP87561-Q1 Switch Node and Output Voltage Ripple, 0.9-V Output and Full Load

4.1.3 Load Transients

図 26 through 図 29 shows the transient responses to 50-100% load steps for memory, I/O supplies, CAN supplies, and a 0-100% load step for the core-voltage supply. Channel 2 (pink) measures current and channel 3 (blue) takes an AC-coupled measurement of the output voltage ripple.

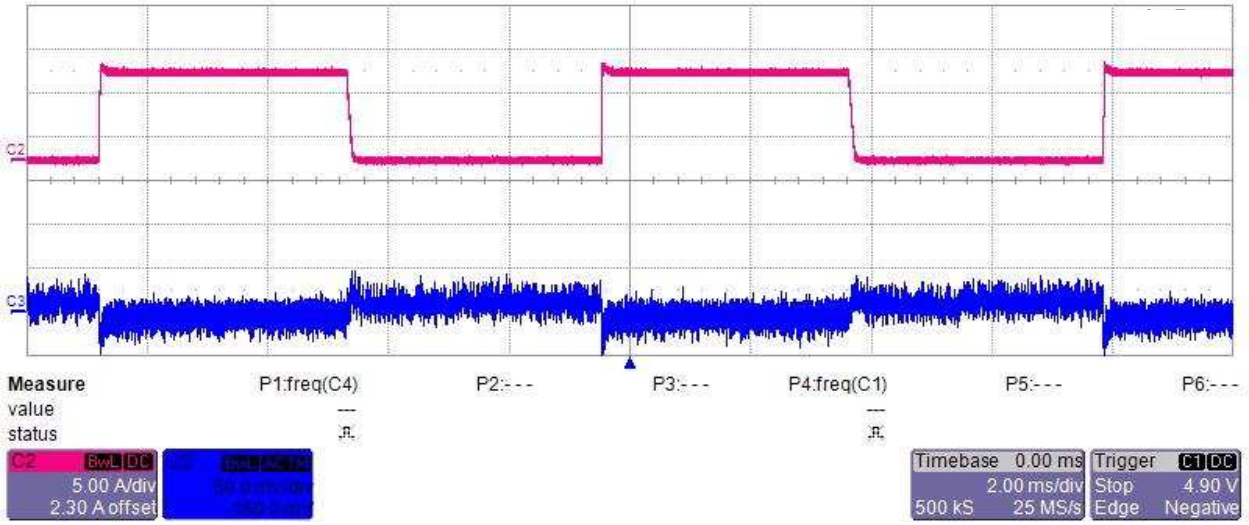

図 26. LP87561-Q1 0-100% Load Transient

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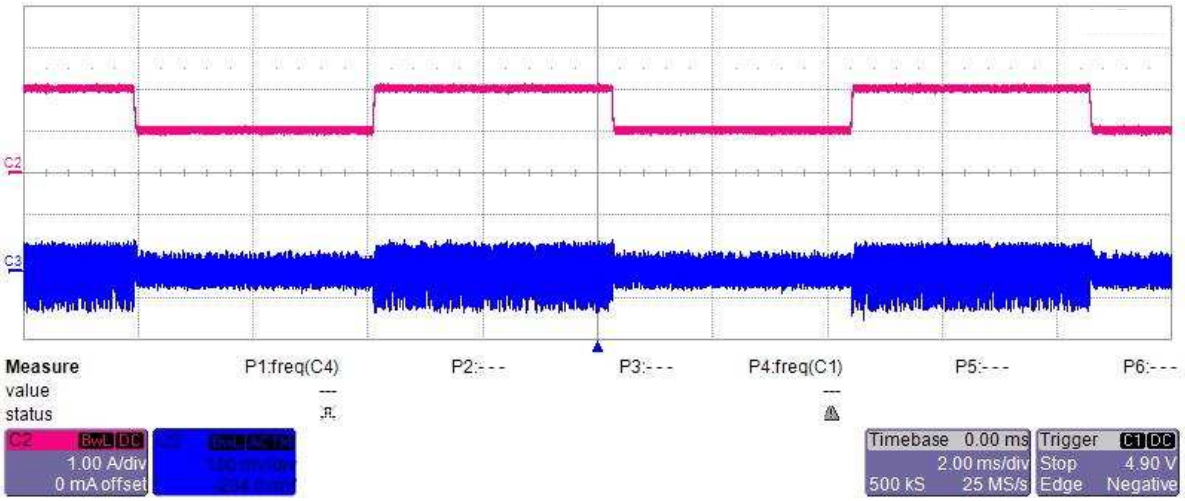

図 27. LM26420-Q1 50-100% Load Transient, 1.8 V

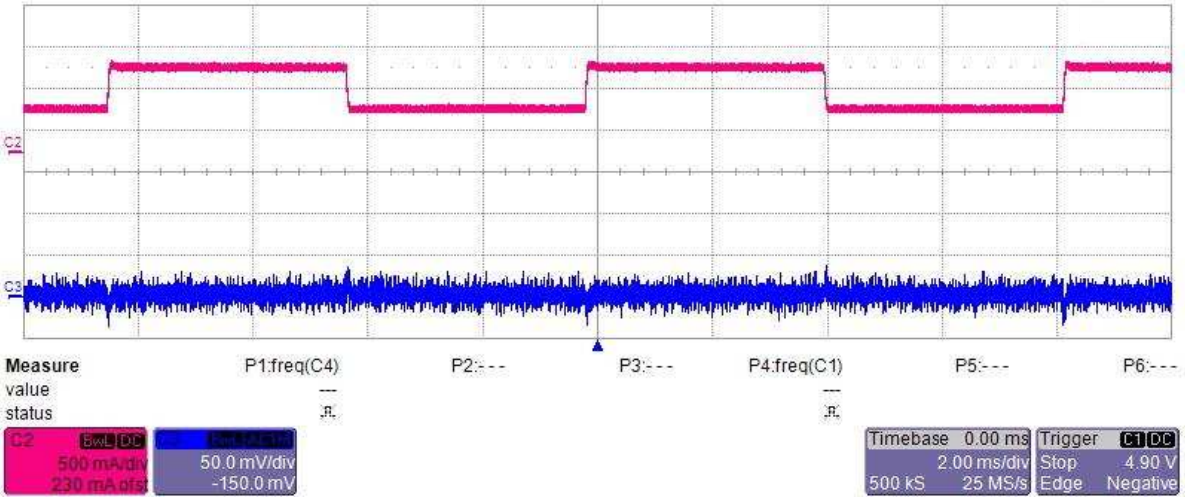

図 28. LM26420-Q1 50-100% Load Transient, 1.2 V

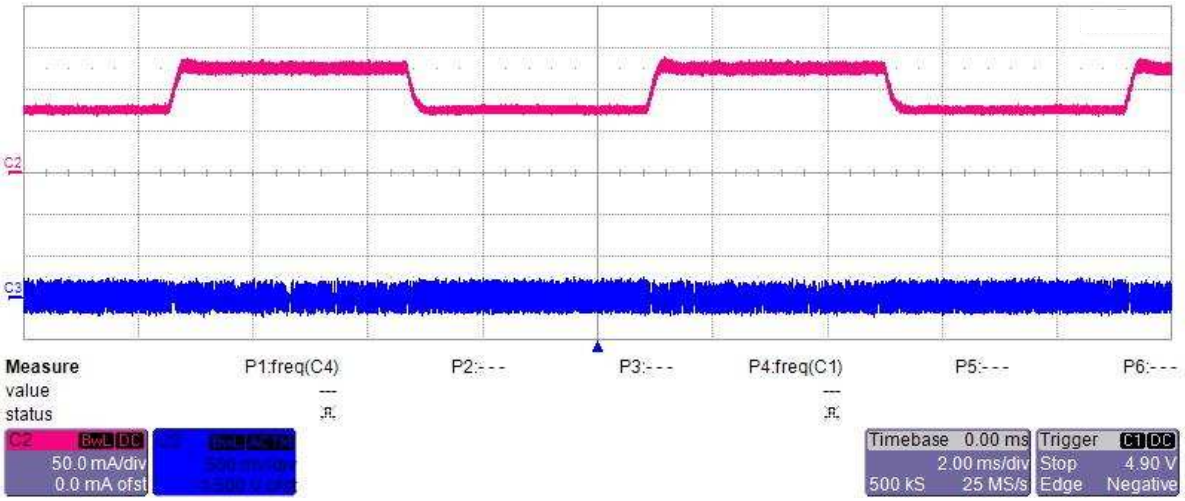

図 29. LM2775 50-100% Load Transient

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4.1.4 Thermal Images

図 30 through 図 33 shows the temperature rise of each supply on the board under full load conditions and with a 13.5-V input voltage after 10 minutes.

注: Board temperatures can exceed 55°C during operation.

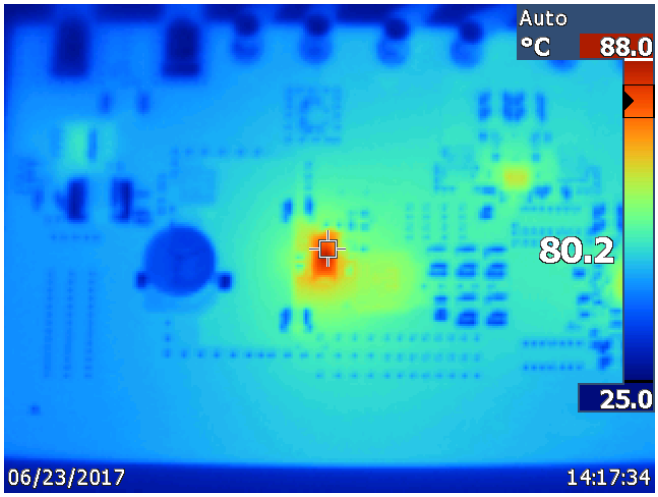

図 30. Thermal of LM73605-Q1 at 5-A Load

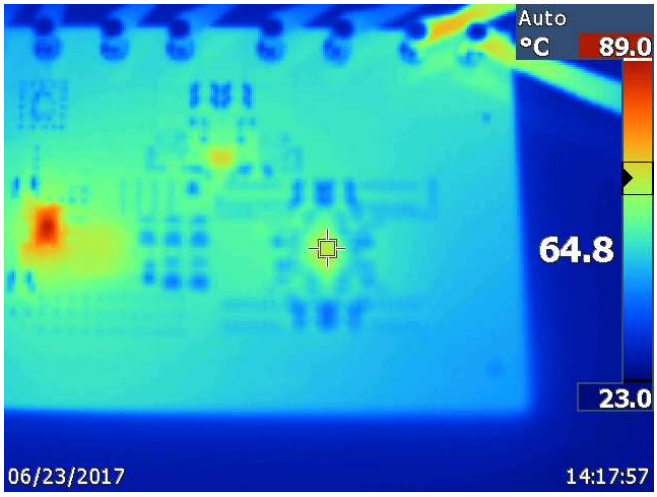

図 31. Thermal of LP87561-Q1 at 10-A Load

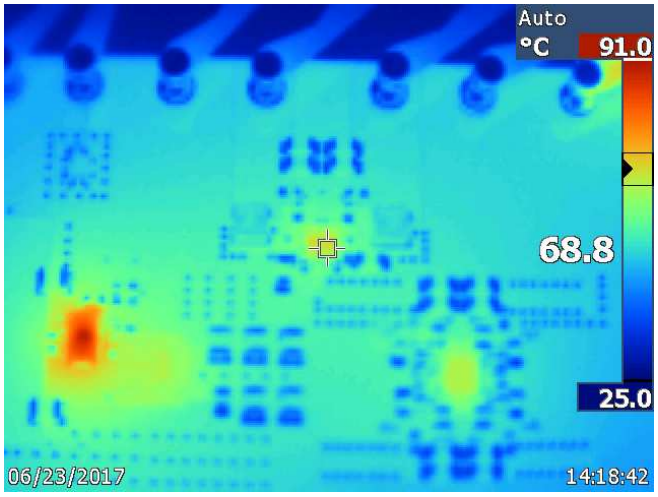

図 32. Thermal of LM26420-Q1 at 1 A for 1.8-V Rail and 2 A for 1.2-V Rail

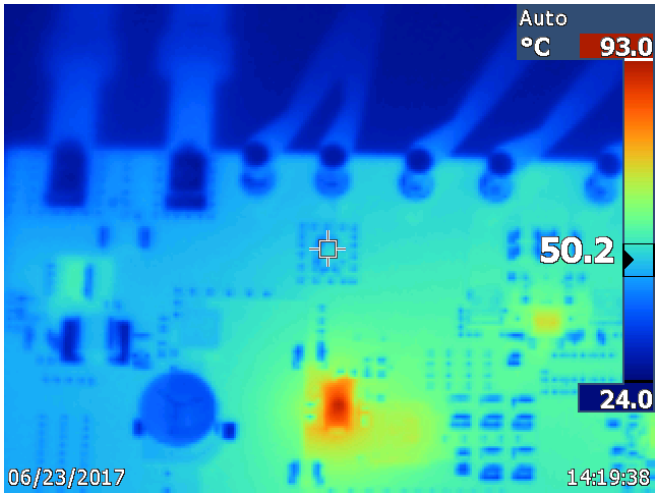

図 33. Thermal of LM2775 at 100-mA Load

4.1.5 Electrical Transient Testing

The following transients were tested:

- Reverse battery
- Cold crank
- Warm crank
- Start-stop

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- Start-up and shutdown

The following subsections show the waveforms of each rail during each condition.

4.1.5.1 Reverse Battery

The following 図 34 shows that the input is disconnected during the reverse battery input voltage condition. Channel 4 is the input voltage and channel 1 is the input voltage after the LM74700-Q1 device.

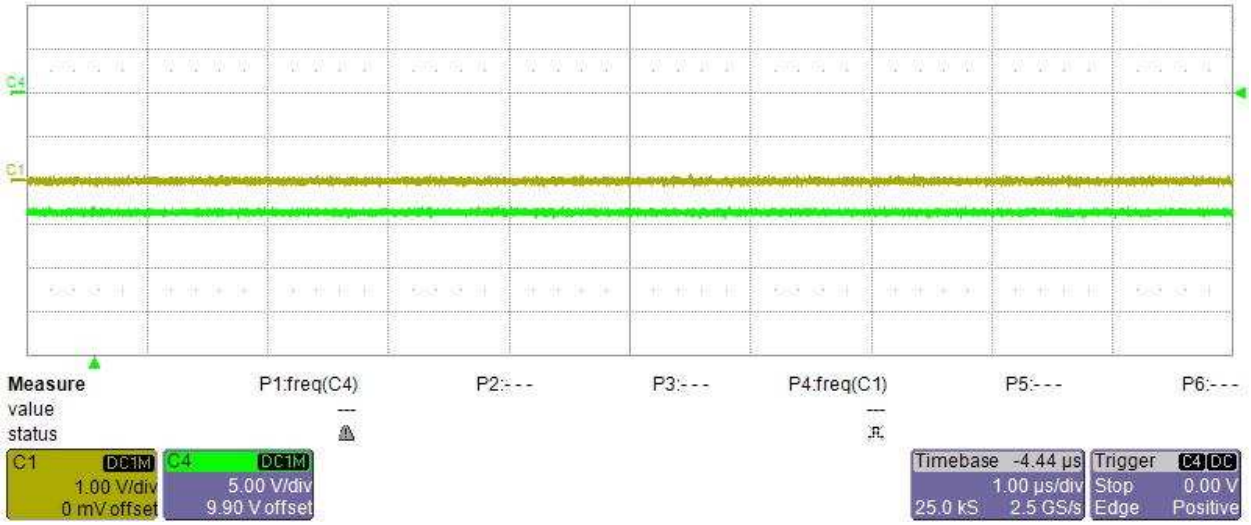

図 34. Continuous Reverse Voltage at Input

This behavior is expected from the LM74700-Q1 smart diode, where, upon a reverse voltage condition, the smart diode disconnects the system from the input. 図 35 shows the transition to reverse input voltage.

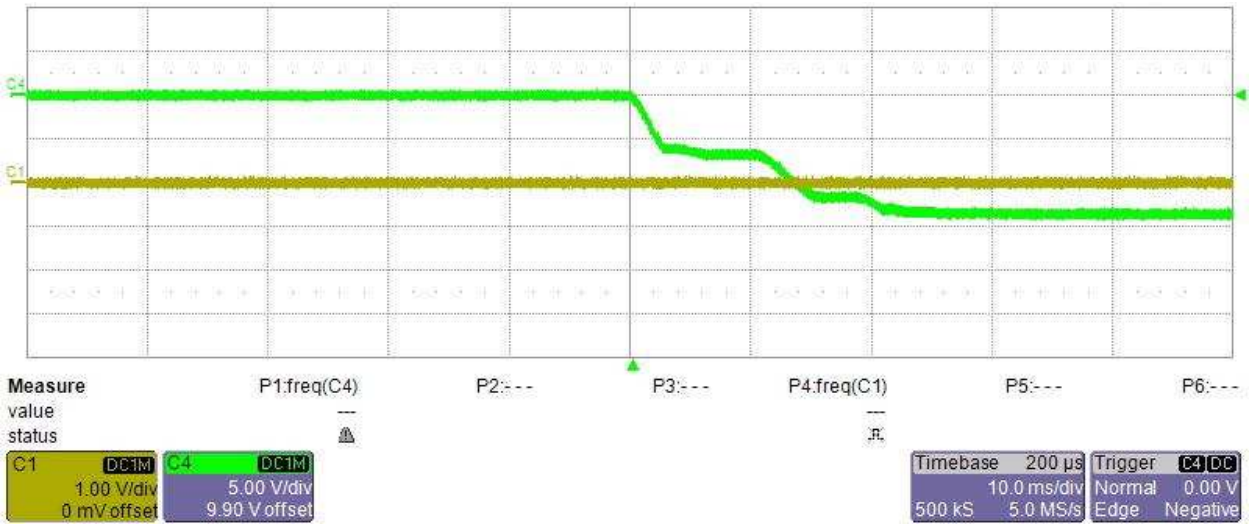

図 35. Transition to Reverse Voltage at Input

The input voltage after the smart diode remains undisturbed as the voltage at the input becomes increasingly negative.

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4.1.5.2 Cold Crank

Testing this design for a severe cold-crank condition was a key objective. This test was accomplished without using a pre-boost.

For the cold-crank test, the input voltage was allowed to fall to 3.5 V from the nominal 13.5 V. 図 36 shows the cold-crank waveform.

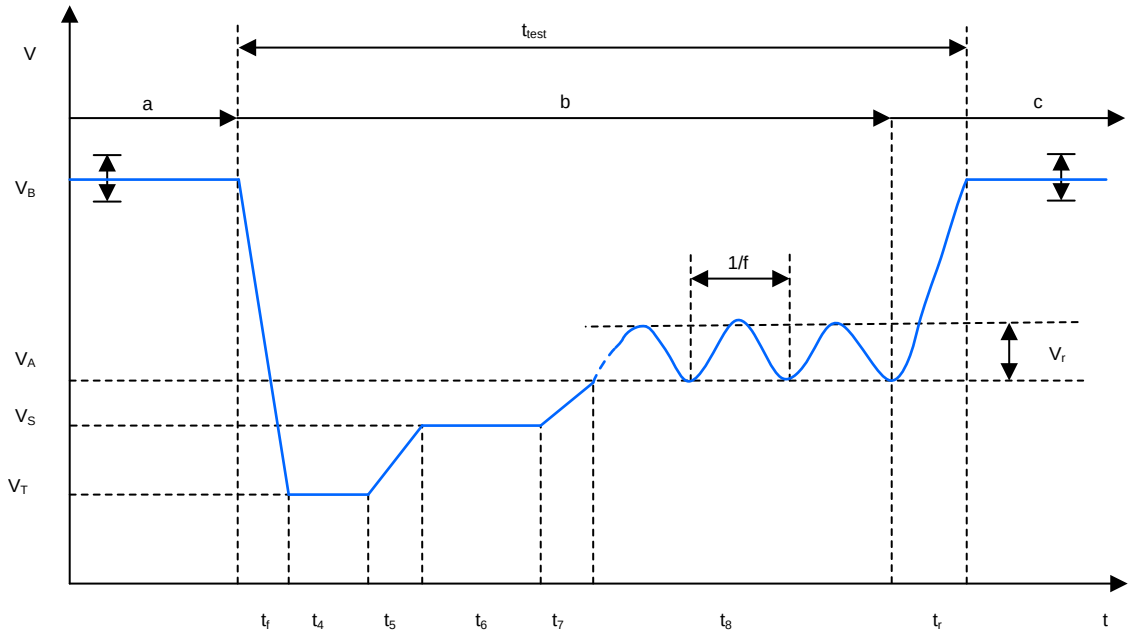

図 36. Cold-Crank Waveform and Parameters

表 2 list the cold-crank test pulse parameters.

表 2. Cold-Crank Test Pulse Parameters

PARAMETER	"NORMAL" TEST PULSE	"SEVERE" TEST PULSE
V_B	11.0 V	11.0 V
V_T	4.5 (0%, –4%)	3.2 V (0%, –4%)
V_S	4.5 (0%, –4%)	5.0 V (0%, –4%)
V_A	6.5 V (0%, –4%)	6.0 V (0%, –4%)
V_R	2 V	2 V
t_f	≤ 1 ms	≤ 1 ms
t_4	0 ms	19 ms
t_5	0 ms	≤ 1 ms
t_6	19 ms	329 ms
t_7	50 ms	50 ms
t_8	10 s	10 s
t_r	100 ms	100 ms
f	2 Hz	2 Hz

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Only the severe test pulse was tested. The cold-crank condition lasts roughly 3.5 s, after which it repeats. In 図 37, channel 1 (yellow) shows the cold-crank input voltage waveform, channel 2 (pink) shows the 3.3-V output, and channel 3 (blue) shows the 0.9-V core-voltage supply output.

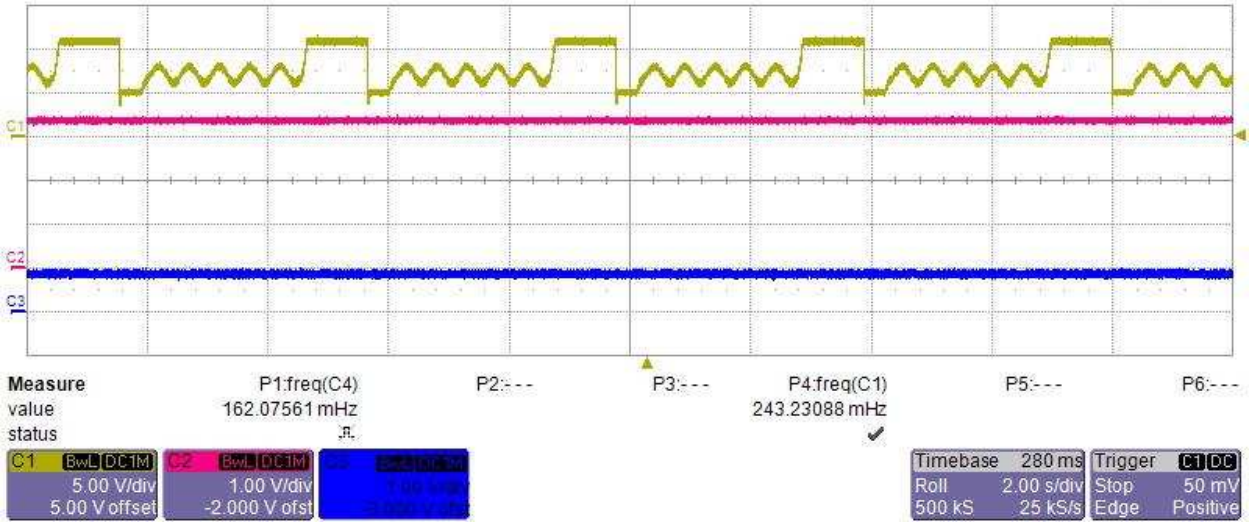

図 37. Cold Crank LP87561–Q1: 0.9 V at 10-A Output

Note that, in the previous 図 37, the output voltages are undisturbed by the cold-crank condition. 図 38 shows the initial drop from 13.5 V to 3.5 V in a shorter timescale.

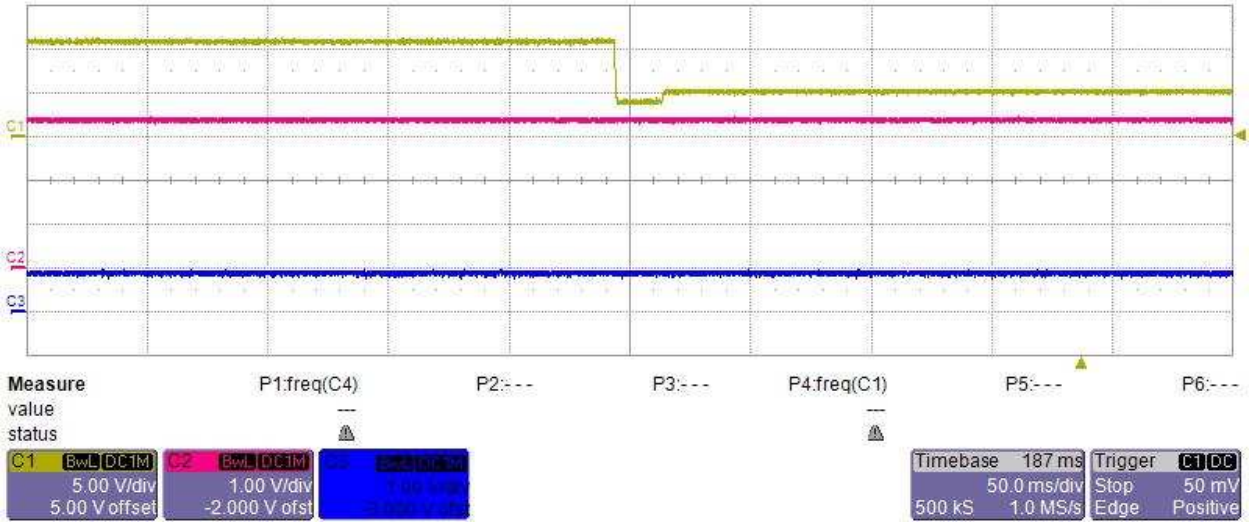

図 38. Cold Crank Down to 3.5 V, LP87561–Q1: 0.9 V at 10-A Output

The initial drop on a shorter timescale still shows no disturbance to the output of the supplies.

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4.1.5.3 Warm Crank

This subsection provides test data for the main system supply and core-voltage rails during warm-crank conditions. In 図 39 and 図 40, channel 1 (yellow) measures the warm-crank input voltage waveform, channel 2 (pink) measures the 3.3-V main system supply, and channel 3 (blue) measures the 0.9-V core-voltage supply.

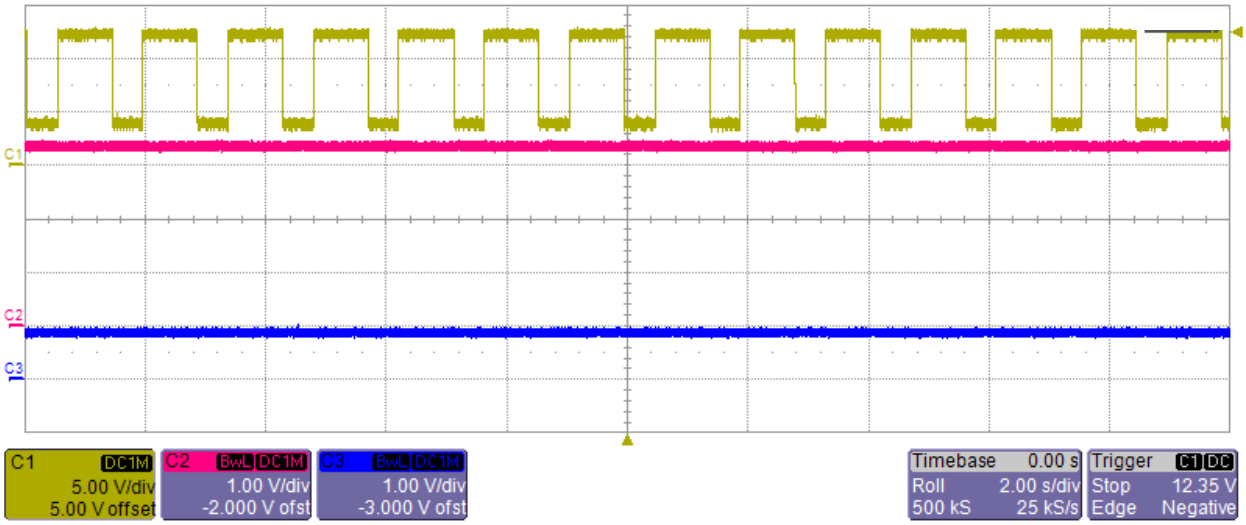

図 39. Warm Crank LP87561-Q1: 0.9 V at 10-A Output

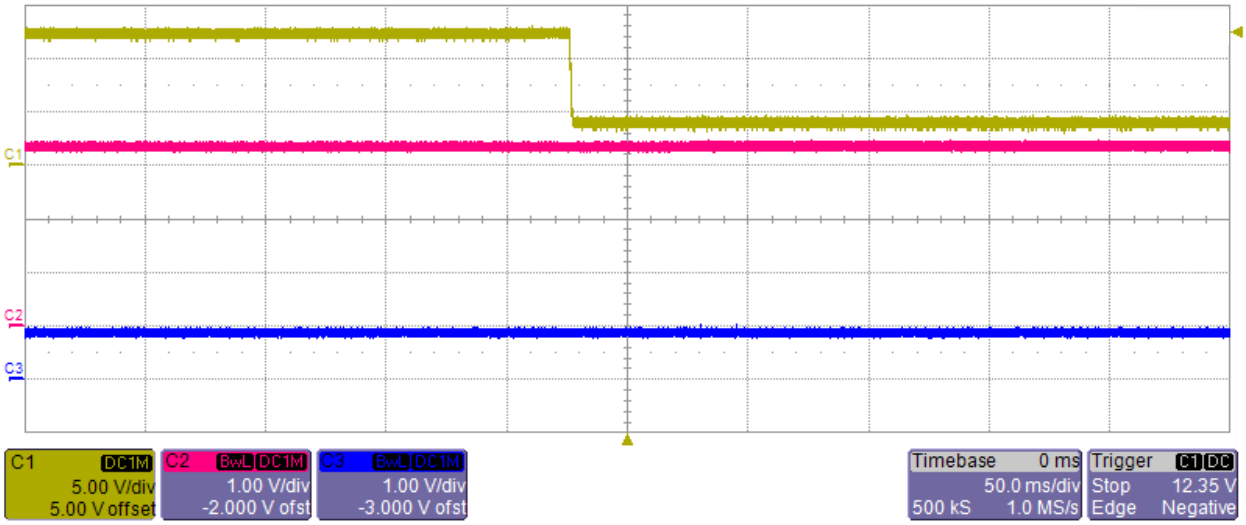

図 40. Warm Crank 50-ms Timescale

Both figures show the output of the supplies to be undisturbed during the warm-crank condition.

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4.1.5.4 Start-Stop

This subsection provides test data for the main system supply and core-voltage rails during start-stop conditions. In 図 41 and 図 42, channel 1 (yellow) measures the start-stop input voltage waveform, channel 2 (pink) measures the 3.3-V main system supply, and channel 3 (blue) measures the 0.9-V core-voltage supply.

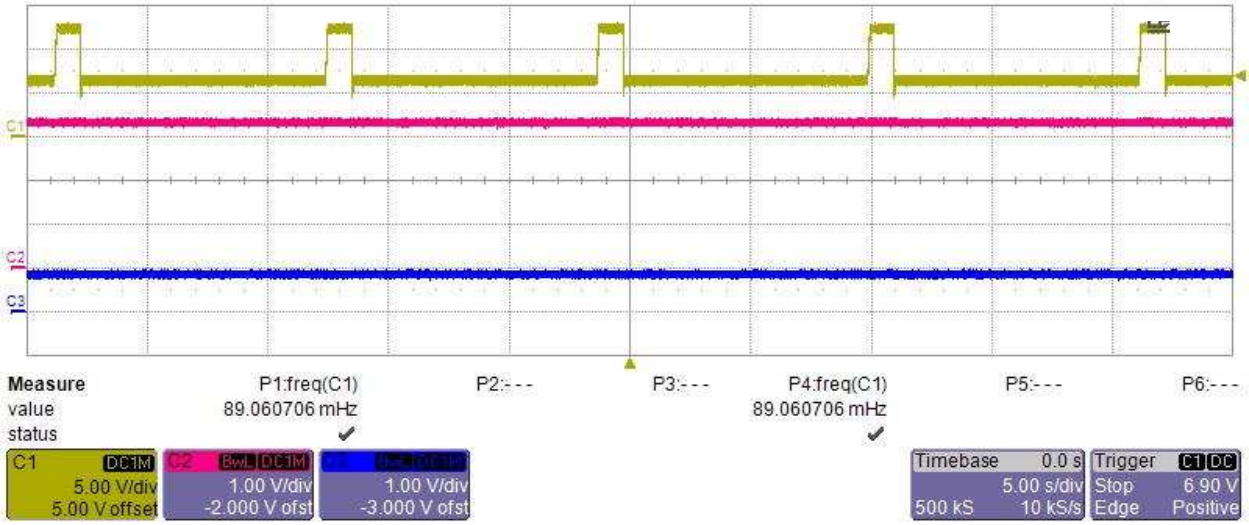

図 41. Start-Stop 5-s Timescale, 0.9 V at 10-A Output

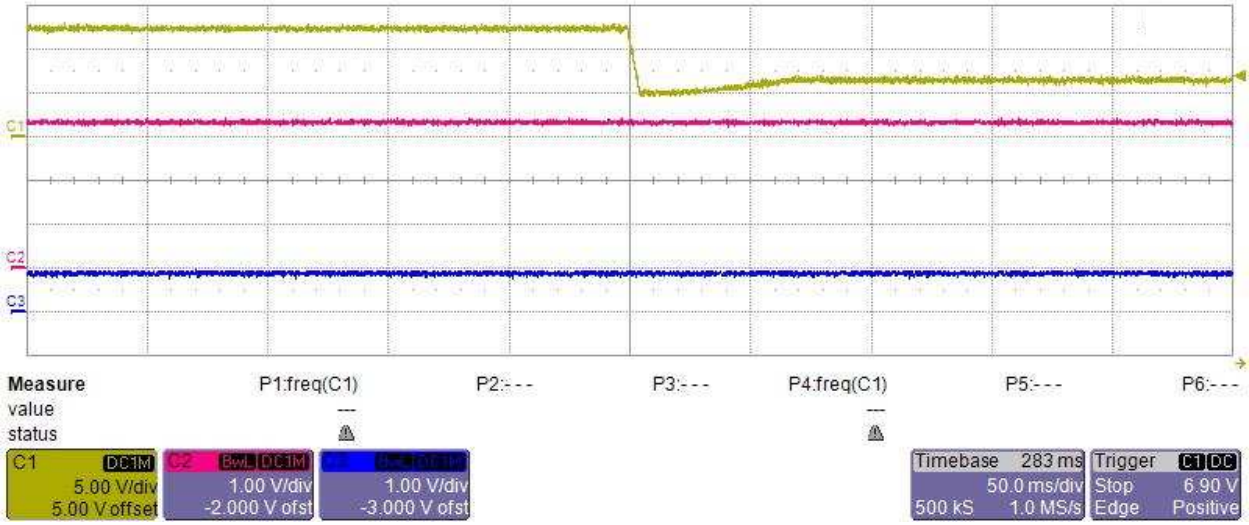

図 42. Start-Stop 50-ms Timescale, 0.9 V at 10-A Output

Both figures show the output of the supplies to be undisturbed during the start-stop condition.

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4.1.5.5 Start-Up and Shutdown

This subsection provides test data for the core-voltage, CAN, and I/O supplies during system start-up and shutdown. Measurements were taken at full and no loads for each supply. The waveforms in 図 43 and 図 44 are labeled on the left side. In 図 45 through 図 46, channel 1 (yellow) measures the input voltage waveform, channel 2 (pink) measures the 0.9-V core-voltage supply, channel 3 (blue) measures the 1.8-V I/O supply, and channel 4 (green) measures the 5-V CAN supply.

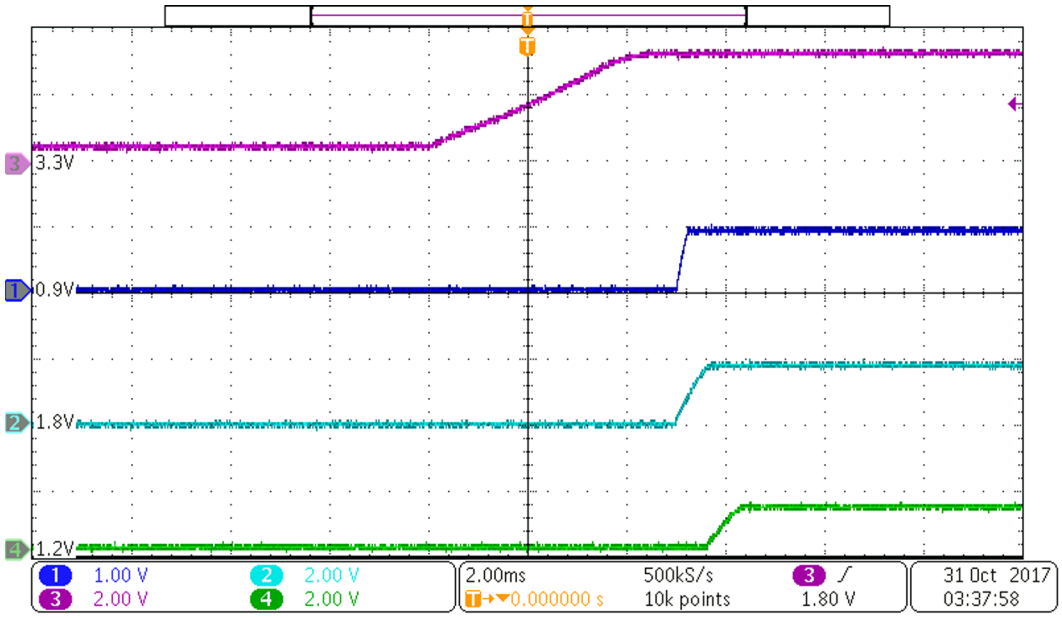

図 43. No Load Start-Up

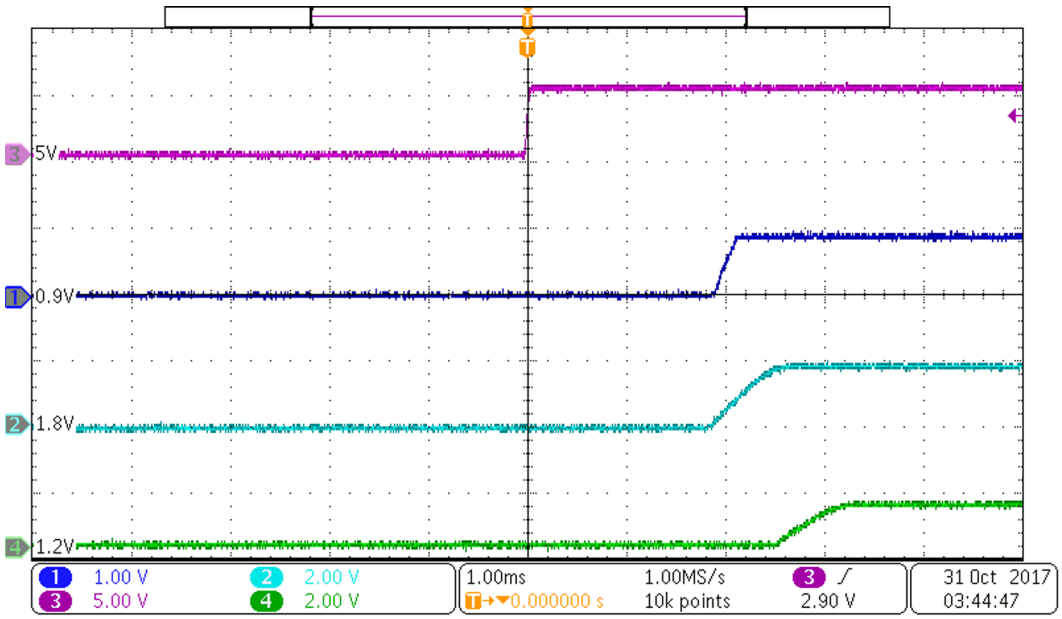

図 44. Full Load Start-Up

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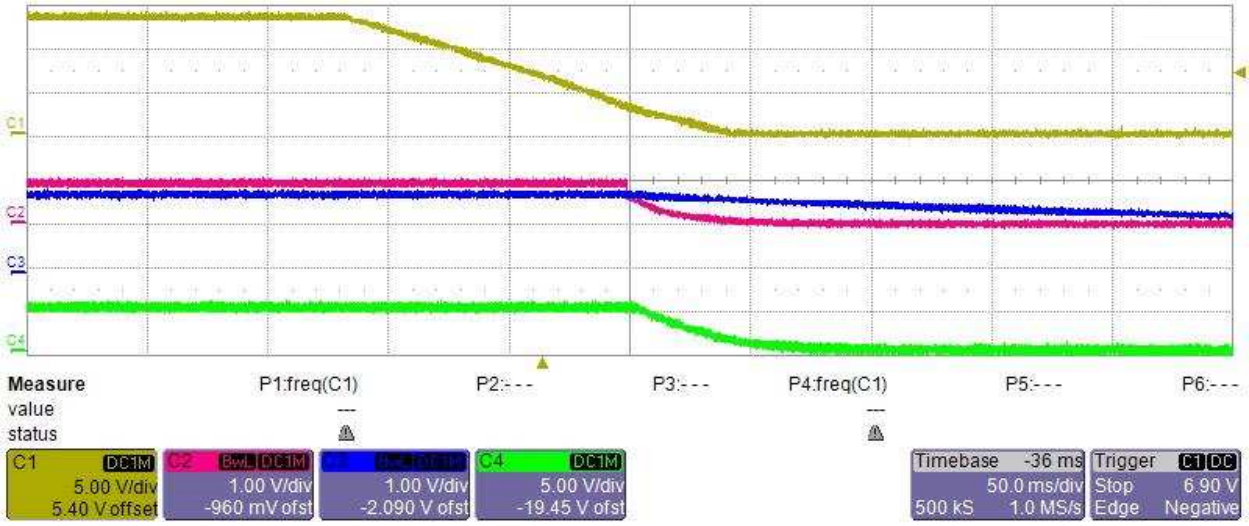

図 45. No Load Shutdown

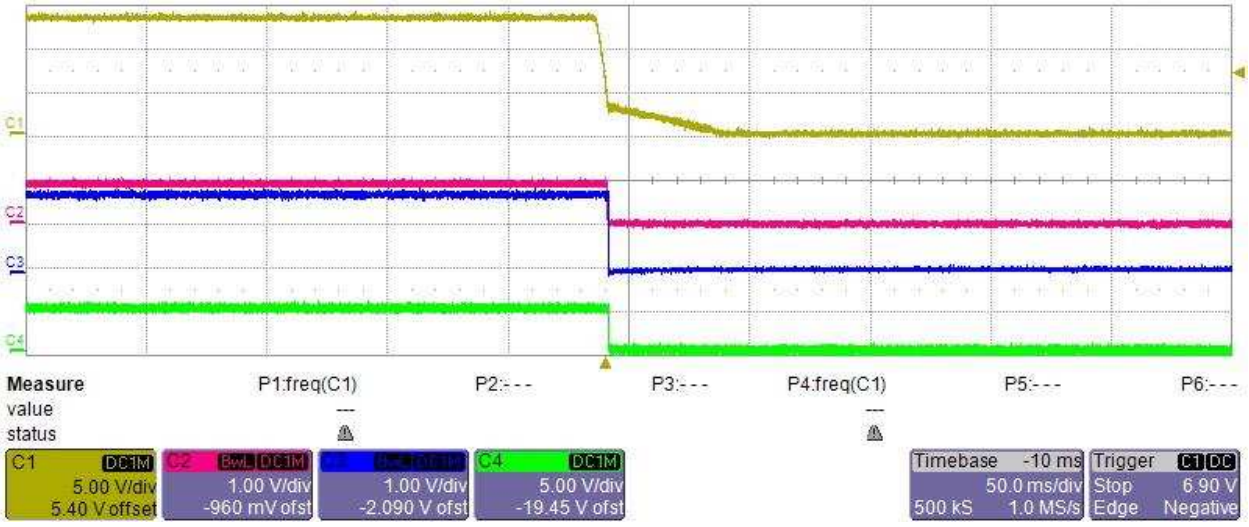

図 46. Full Load Shutdown

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4.1.6 Conducted Emissions

The conducted emissions of the TIDA-01492 have been tested against CISPR 25 Class 5 limit lines. The examined frequency band spans from 150 kHz to 108 MHz covering the AM-FM radio bands, very-high-frequency (VHF) band, and TV band specified in CISPR 25.

図 47 and 図 48 show the test results. 図 47 shows the test results using peak detector and average detector measurements, respectively, up to 30 MHz. 図 48 shows the test results using average detector and peak detector measurements from 30 MHz to 108 MHz. The limit lines (shown in red) are the Class 5 limits for conducted disturbances specified in the CISPR 25. The yellow trace (peak detector measurement) and blue trace (average detector measurement) are the measured results.

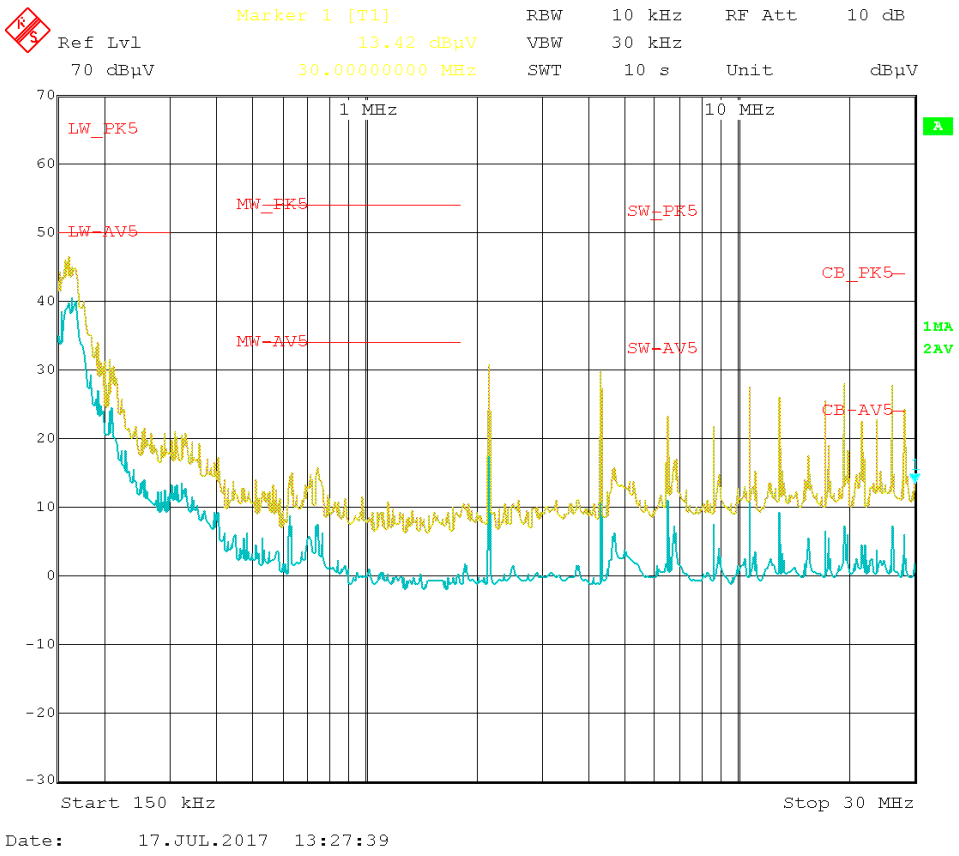

図 47. 150-kHz to 30-MHz Conducted Emissions—Peak and Average Detection

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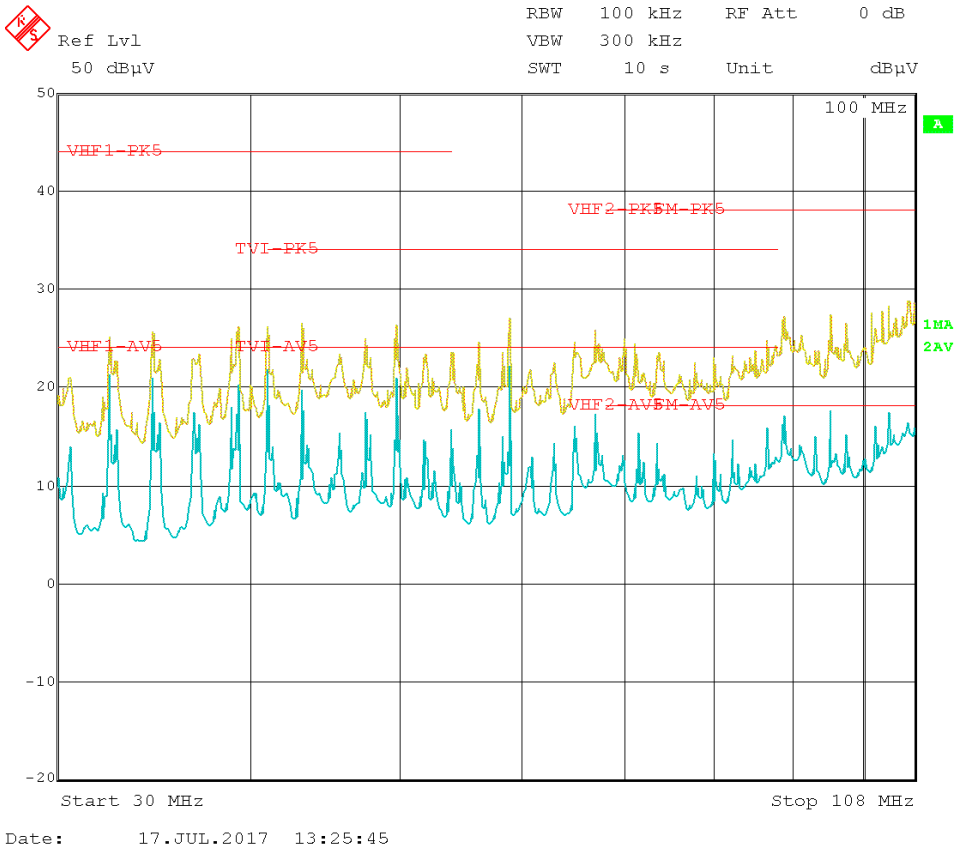

図 48. 30-MHz to 108-MHz Conducted Emissions—Peak and Average Detection

The conducted emissions were tested using the setup shown in 図 49, where a 0.1-Ω load was added directly on the output capacitors of the LP87561-Q1 device. The load is attached to a heat shield facing in the direction of the LP87561-Q1 device.

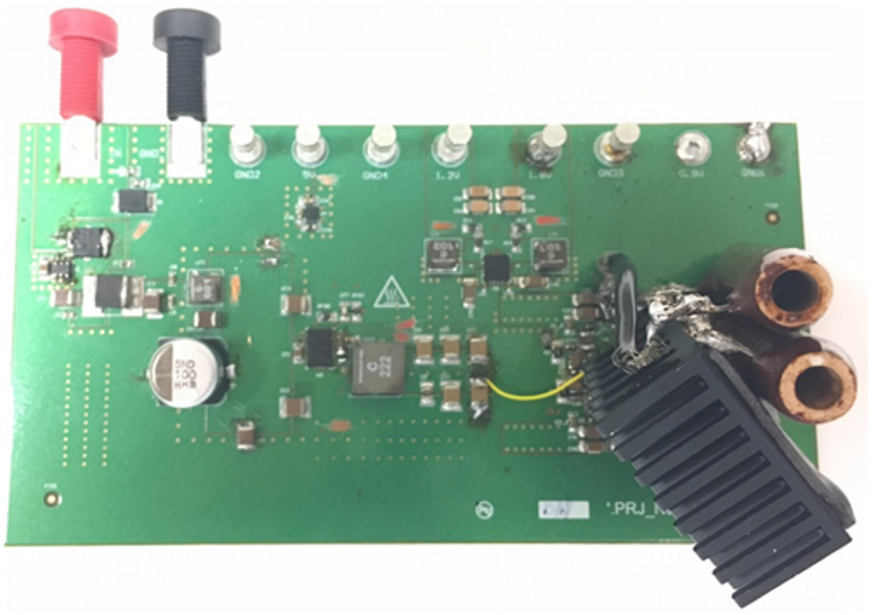

図 49. Setup for EMI Testing

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5 Design Files

To download the design files for this TI Design including the schematic, bill of materials, layer plots, Gerber files, and Altium files, see the design files at TIDA-01492.

5.1 PCB Layout Recommendations

5.1.1 Input Protection Circuitry

Place input protection circuitry as close to the battery terminal inputs as possible, rather than close to the downstream circuit it is protecting, to reduce the inductance of the path. This placement allows the TVS diodes to react as quick as possible to any transients. Close placement provides a tight loop for the return path back to the battery terminals while the TVS diodes shunt a transient event. In the event of a reverse polarity event, the FET Q1 quickly shuts off, possibly causing inductive kicks due to the interrupted current flow. The severity of this kick is a function of the inductance and, therefore, the length and width of the power path.

5.1.2 Input EMI Filter Considerations

The goal of the EMI filter is to minimize emissions, especially conducted emissions. The key to minimizing emissions is providing low impedance paths to quickly ground high-frequency noise, which is typically accomplished by containing high-frequency current loops. 図 50 shows the current flow through the EMI filter. The DC is outlined in red and the high-frequency AC paths are outlined in green.

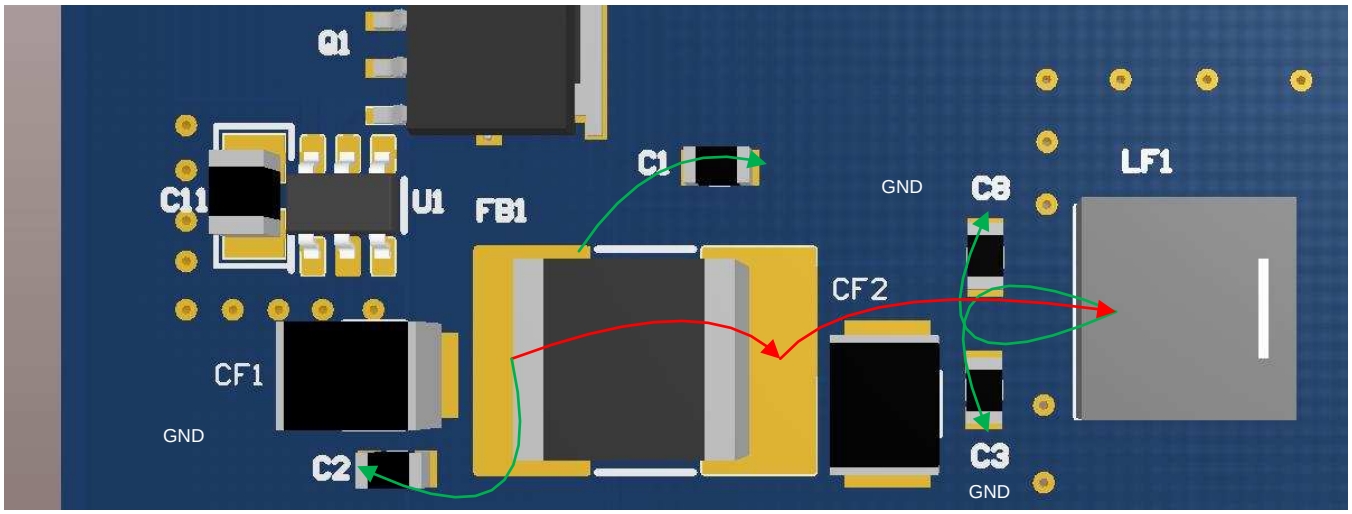

図 50. Input EMI Filter

Conducted emissions are mainly due to high-frequency noise that input capacitors cannot bypass. This noise is conducted onto the input leads of the supply, which drives the convention that the higher-frequency AC flows away from the 3.3-V supply back toward the system supply.

The previous 図 50 shows the smaller 0.1-µF capacitors C3 and C8 close to the 2.2-µH inductor LF1 to filter out the high-frequency noise not attenuated by the inductor. Capacitors C3 and C8 are placed across from each other instead of next to each other to minimize the possibility of inductive coupling during operation due to their close proximity.

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Inductors behave capacitively above their resonant frequency; therefore, any frequencies above this are not attenuated. The amount of noise that is injected back onto the supply line directly depends on how much has been filtered out; therefore, the smallest path to ground for high-frequency noise is required.

5.1.3 Noise-Sensitive Traces and Components

The feedback (FB) and compensation (COMP) nodes of power supplies are especially high impedance and thus susceptible to picking up noise. These nodes are critical to operate the control loop of the device; therefore, poor placement and routing of these components or traces can affect the performance of the device and system by introducing unwanted parasitic inductances and capacitances.

The switch node of DC-DC converters are typically very noisy. The switch node can radiate a significant amount of energy and can couple noise into sensitive lines. Traces for the switch node must be wide enough for the maximum current but small enough to minimize radiation. Signals like output voltage FB traces for power supplies are high-impedance lines. These signals are quite sensitive to disturbances, especially to noise from switch nodes and high-bandwidth I^2C lines. Placing sensitive traces apart from noisy traces, ideally on the opposite sides of the board or separate layers (with ground planes between them), mitigates such negative effects. The FB loop itself, from output voltage to FB pin and analog ground, must be small enough to minimize parasitics and noise susceptibility. Place all analog and control loop components such that their trace lengths back to the IC are minimized.

The TIDA-01492 layout in 図 51 shows the current flow and FB for the main 3.3-V supply at the PCB level. As in the previous 5.1.2, the red arrows outline the DC and the green arrow shows the high-frequency AC path, which filters out high-frequency noise from the output. The 3.3-V output voltage is sensed and fed back to the supply far enough from the switch node and high-frequency noise path to avoid noise coupling.

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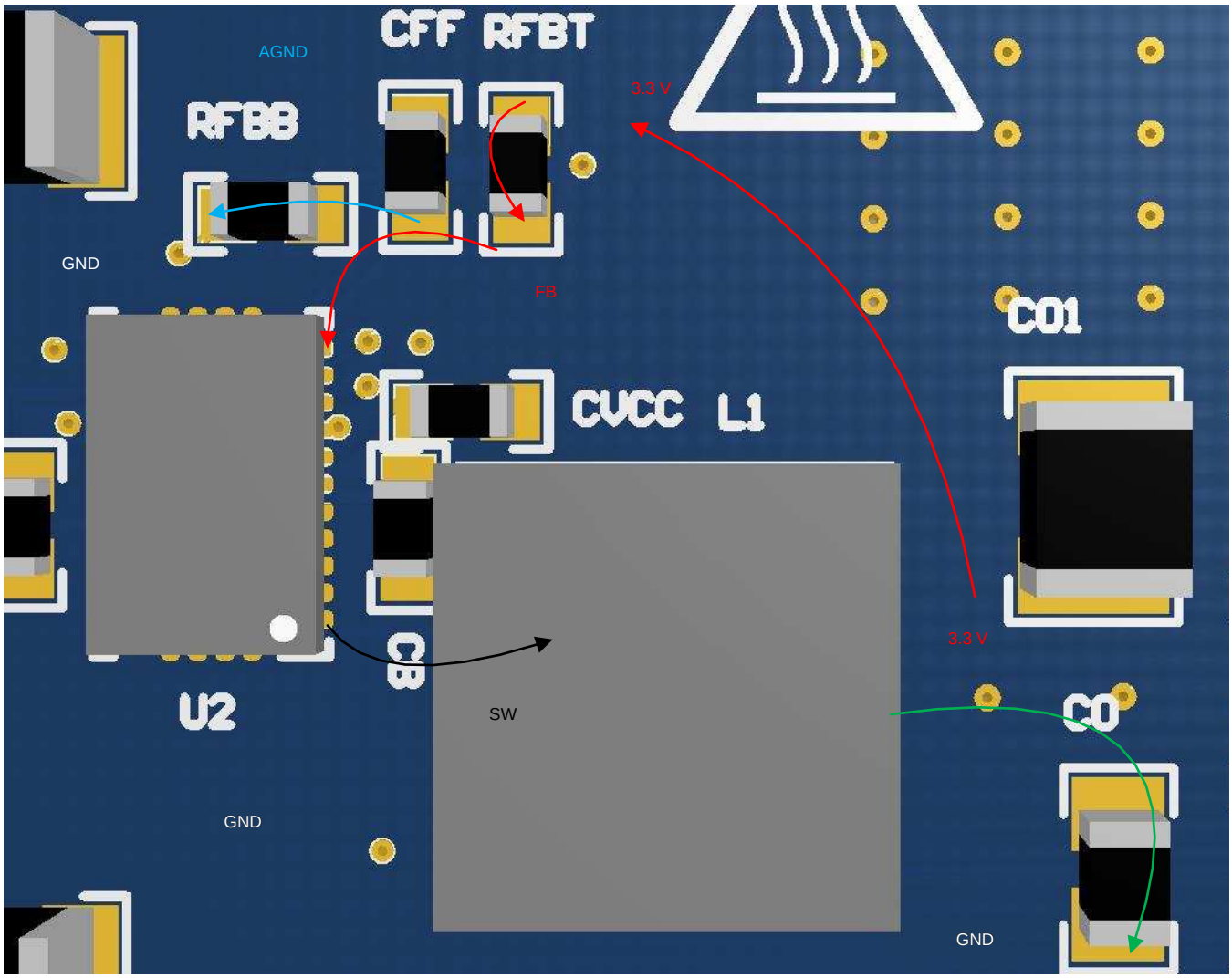

図 51. 3.3-V Supply Component and Node Placement

図 52 shows the current flow and FB for the main 3.3-V supply along with layer and trace details.

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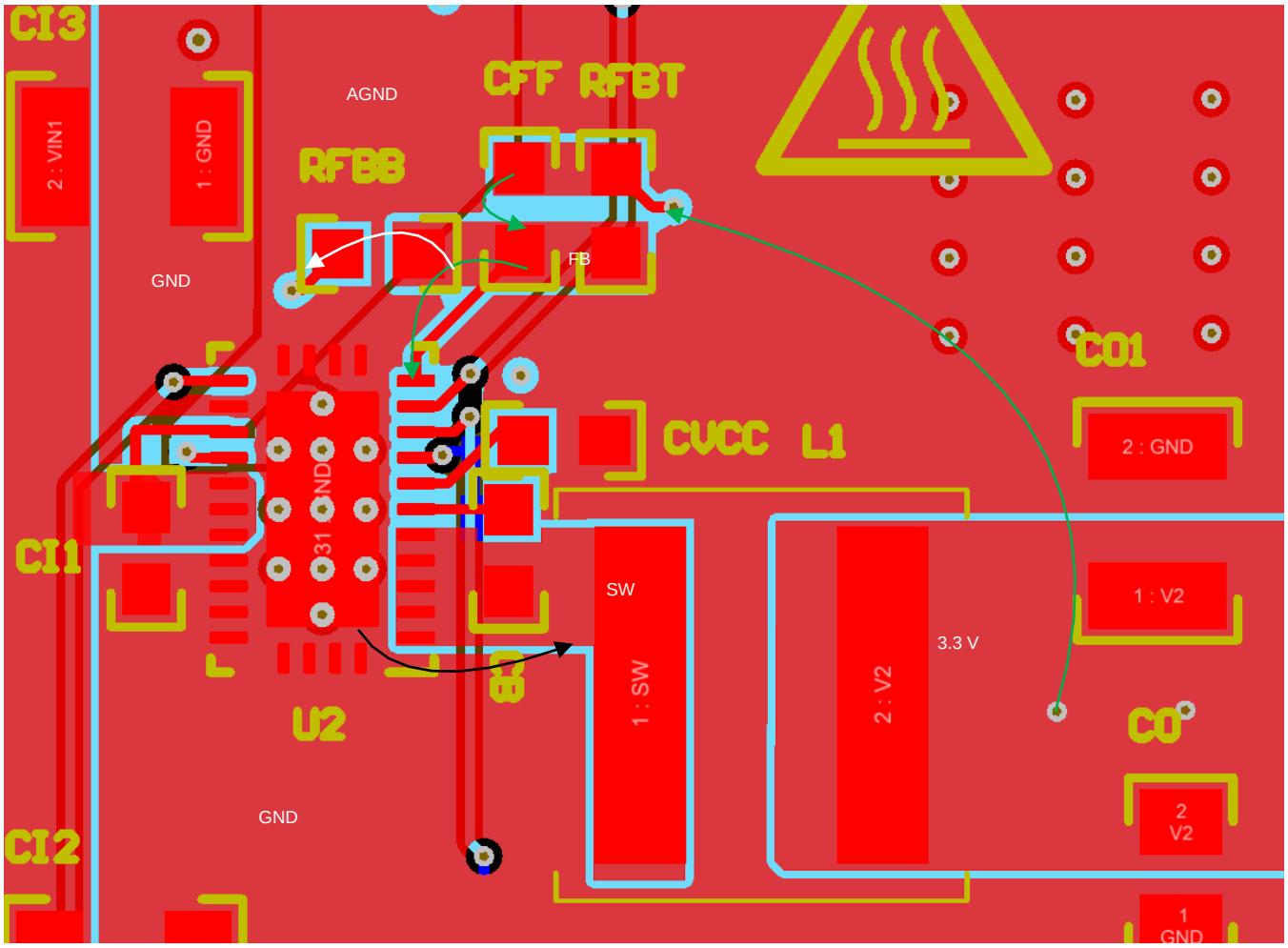

図 52. 3.3-V Output and Feedback Network

In 図 52, the red layer is the top layer and the light blue is the third layer, which contains the 3.3-V plane, analog ground plane, and several other signals and nodes. Each respective node is labeled accordingly. Arrows show the current flow from the output through the feedback network. The 3.3-V output voltage is sensed in the third layer of the board where the 3.3-V rail is quiet and distributed to the rest of the system. Note that the voltage feedback path is small and away from the switch node and switching currents, with a dedicated analog ground plane (labeled with yellow text) running along the 3.3-V plane and feedback network.

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Similar layout considerations have been made for the 0.9-V core-voltage supply. 図 53 shows the FB trace of the core-voltage supply output routed on layer 3, which is several millimeters from the switch node.

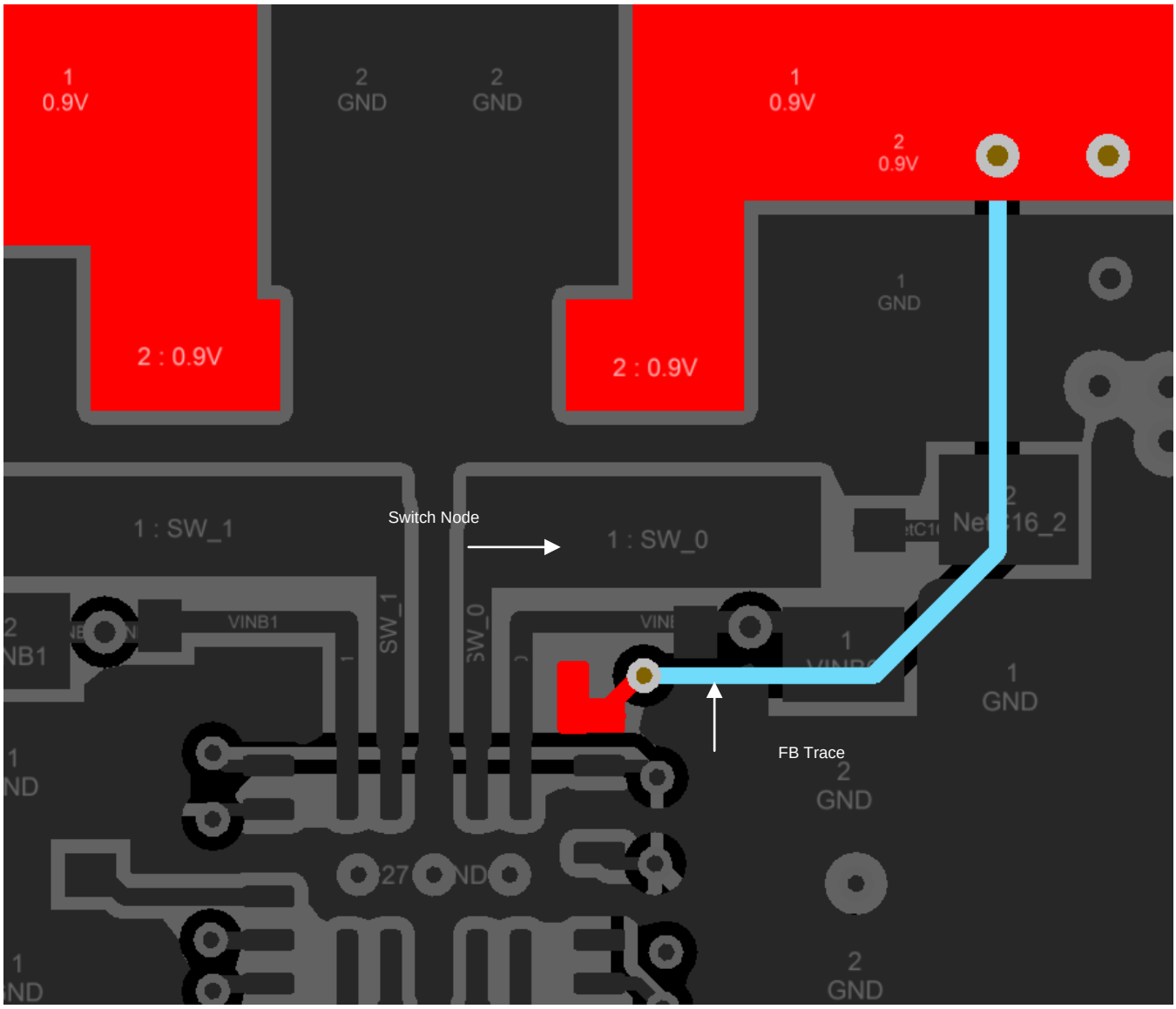

図 53. Routing Feedback Traces Around Switch Nodes

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5.1.4 EMI Mitigation for Core-Voltage Supply

This subsection covers the layout for the filtering circuitry for the 0.9-V core-voltage supply. Because this supply provides the most current, more considerations have been made to mitigate EMI, which includes both the snubber circuits and input EMI filters for each phase. For more theory on EMI reduction for DC-DC converters, see *AN-2155 Layout Tips for EMI Reduction in DC/DC Converters*. The following 図 54 and 図 55 show the external component placement for the 0.9-V core-voltage supply.

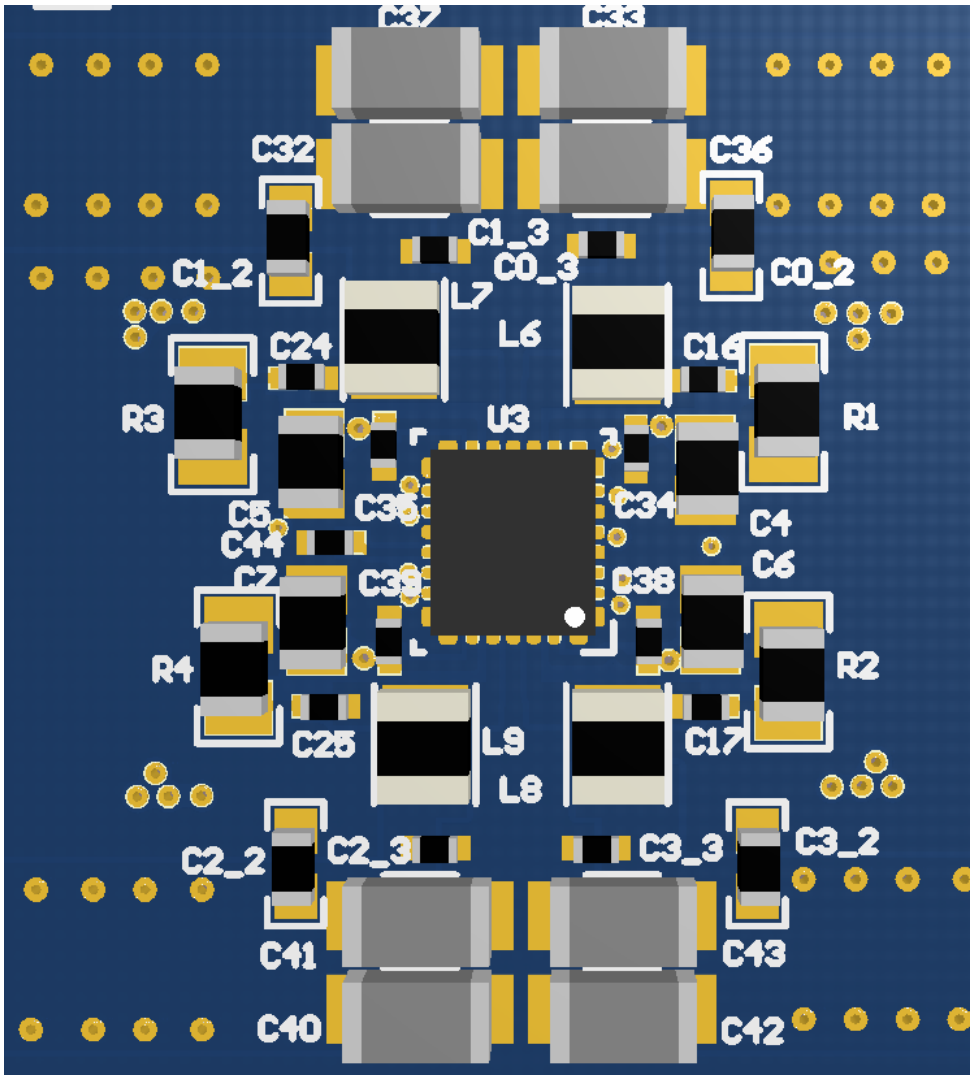

図 54. Core-Voltage Supply Component Placement—Top View

Note that, on the top layer, the 0.9-V output voltage plane encircles the entire solution and each buck has its own quadrant with high-frequency filter circuitry in close proximity with the IC.

The same rule for high-frequency filtering has been followed on the bottom layer. The main goal is to ensure that high-frequency current loops (high di/dt) are as small as possible. High-frequency decoupling caps are located on both sides of the board by the device input to minimize the current loop area by providing a low impedance path for high-frequency input currents. For example, observe in 図 55 that buck 0 uses C20 (top-center left) and C34 in 図 54 (top-center right) for high-frequency decoupling.

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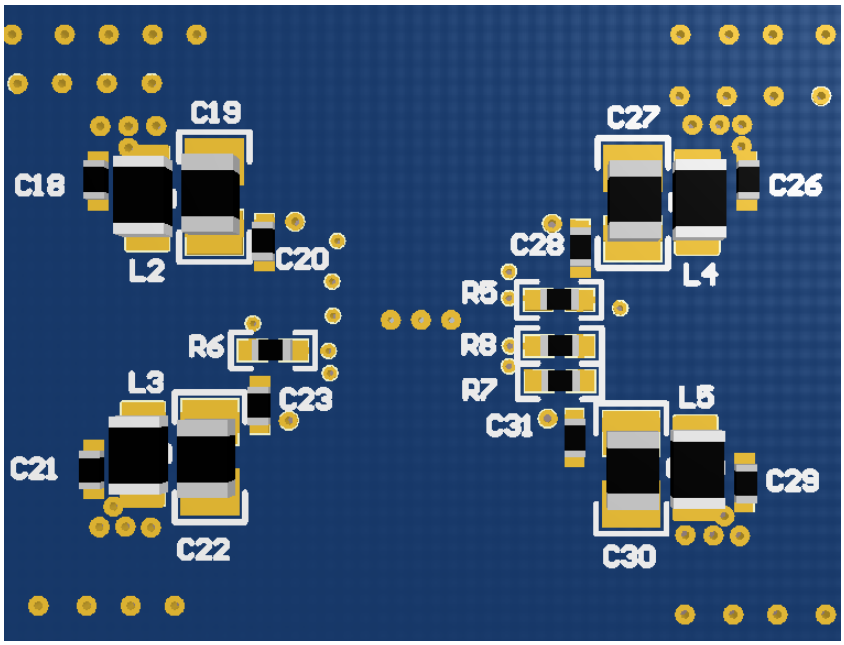

図 55. Core-Voltage Supply Passives Placement—Bottom View

The layout screen shot shown in 図 56 focuses on the components for buck 0 and the arrows to show current flow. The dashed arrows represent switching current. The green dashed arrow shows the switching current flow through the snubber circuit (C16 to R1) to ground.

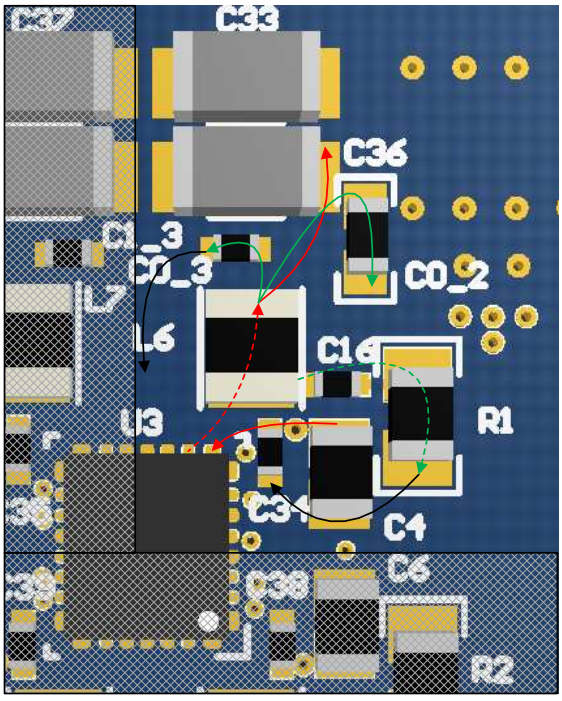

図 56. AC and DC Flow Through Snubber Circuit and Output Filter

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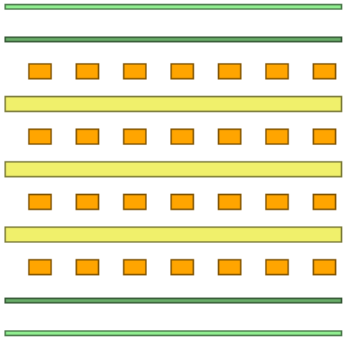
Note that the snubber circuit is closest to the input of buck 0 instead of the output. This placement is intended to minimize the current loop of the high-frequency currents that flow from the input capacitors, to the switch node, and back to the input capacitors. For example, if the snubber is placed above inductor L6 near C0_3, the high-frequency current loop is much larger to return to input capacitors C34 and C4. This larger current loop can interfere with other nearby circuits and current loops and introduce other EMI problems.

5.1.5 PCB Layering Recommendations

If using a six-layer board, make layers 2 and 5 ground planes to shield the internal signal layers from outside noise sources as well as the switch nodes found on the top layer. If using a four-layer board (as in this reference design), layer 2 must be a ground plane. 図 57 details the stack-up used in this reference design.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant
Top Overlay	Overlay				
Top Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Top Layer	Signal	Copper	2.8		
Dielectric 2	Dielectric	Core	10	FR-4	4.2
Signal Layer 1	Signal	Copper	1.4		
Dielectric 3	Dielectric	Core	10	FR-4	4.2
Signal Layer 2	Signal	Copper	1.4		
Dielectric1	Dielectric	Core	10	FR-4	4.2
Bottom Layer	Signal	Copper	2.8		
Bottom Solder	Solder Mask/Co...	Surface Material	0.4	Solder Resist	3.5
Bottom Overlay	Overlay				

図 57. Layer Stack-Up With GND Planes Separating Signal Layers

Keep power traces and pours on the same layer as much as routing requirements allow. This grouping minimizes the inductance of the path and reduces noise coupling between planes. Unfortunately, due to the high number of rails in this reference design and the routing requirements required to get signals to the EVM connectors, sticking to this rule is not totally possible.

6 Related Documentation

1. Texas Instruments, *LM73605/LM73606 3.5-V to 36-V, 5-A or 6-A Synchronous Step-Down Voltage Converter*
2. Texas Instruments, *Four-Phase 16-A Buck Converter With Integrated Switches*
3. Texas Instruments, *LM26420/LM26420-Q0/Q1 Dual 2-A Automotive-Qualified, High-Efficiency Synchronous DC-DC Converter*
4. Texas Instruments, *LM2775 Switched Capacitor 5-V Boost Converter*
5. Texas Instruments, *LM74700-Q1 Low I_Q Always ON Smart Diode Controller*
6. Texas Instruments, *AN-2155 Layout Tips for EMI Reduction in DC/DC Converters*

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