参考資料

TI Designs: TIDA-01508
サブ1W、16チャネルの絶縁デジタル入力モジュールのリファレンス・デザイン

概要

このリファレンス・デザインでは、TIのISO121xデバイスを使用した16の絶縁デジタル入力チャネルのコンパクトな実装を紹介します。このデザインは絶縁電源なしに動作し、チャネルごとに最高100kHzの入力信号(200kbit)をサポートします。16のチャネルをすべて合計しても入力電力は1W未満で、小型のレイアウトが可能になり、熱発散も最小限となります。すべての入力チャネルは、IEC 61000-4-2に従い、ESD、EFT、およびサージ・イベントに耐えられるよう設計されています。さらに、これらのチャネルは最高±60Vの入力電圧に耐えられます。

リソース

TIDA-01508	デザイン・フォルダ
ISO1211	プロダクト・フォルダ
ISO1212	プロダクト・フォルダ
SN74LV165A	プロダクト・フォルダ
SN74LVC1GU04	プロダクト・フォルダ
TVS3300	プロダクト・フォルダ

TI E2E™ Community

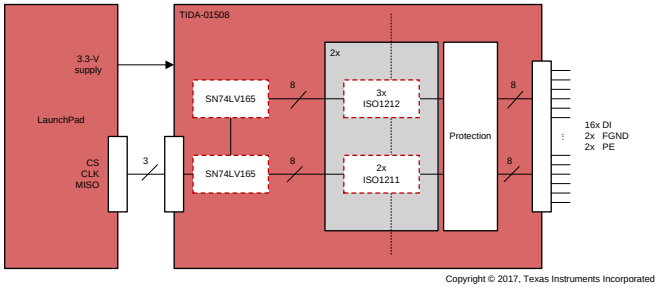
E2E™エキスパートに質問

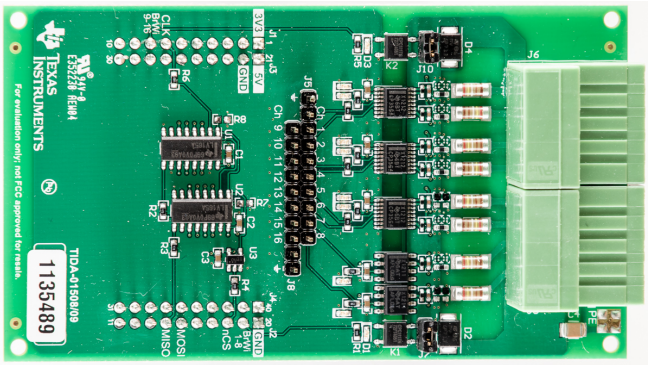
特長

- 最高±60Vの入力電圧を許容する16のデジタル入力チャネル
- 主電源のみで動作し、絶縁電源が不要
- パラレルおよびシリアル出力のオプション
- ±6kVのIEC 61000-4-2 ESD性能
- ±2kVのサージに耐えられ、EFTバースト許容の設計
- LaunchPad™ヘッダーによる迅速で簡単な評価

アプリケーション

- デジタル入力モジュール
- 産業用ロボットのIOモジュール





1 System Description

This reference design shows a compact implementation of 16 isolated digital input channels using TI's new ISO121x devices, a single (ISO1211) and dual (ISO1212) channel, isolated, 24-V digital input receiver. The ISO121x device provides an accurate current limit for digital inputs, enabling a power dissipation of less than 1 W for 16 inputs channels. The 16 channels are divided into two groups of eight channels, each consisting out of three dual-channel ISO1212 and two single-channel ISO1211 devices.

ISO121x devices can be configured for IEC 61131-2 Type 1, 2, 3 compliant characteristics with only two external resistors, which are at the same time protecting the device itself against ESD, EFT, and surge events. In this design, all inputs are configured for Type 1.

Every channel is designed to withstand ESD, EFT, and surge events according to IEC 6100-4-2, IEC 6100-4-4, and IEC 6100-4-5, respectively. This protection is achieved by using pulse resistant resistors to configure ISO121x for Type 1. Furthermore, every input can withstand input voltages of up to ±60 V. For additional protection, every channel is either protected with a varistor or with two of TI's TVS3300 TVS diodes.

To read the output states of the 16 channels, each group of eight outputs is connected to a parallel-in serial-out register (SN74LV165A). The serial outputs of the two registers can be read out using the SPI of a microcontroller. Therefore, this reference design can be plugged onto the MSP430FR5969 LaunchPad or any other TI LaunchPad with the same SPI pinout. The LaunchPad also supplies power to the system.

For serial readout of the output states, the board is designed to support up to input signals of up to 100 kHz (200 kbit) per channel. However, ISO121x devices support data rates of up to 4 Mbps. For parallel readout, an additional 16-pin connector is mounted on the board.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Number of channels	16 (in groups of 8)	2.3.1
Low level threshold = 0	12.5 V	2.3.1
High level threshold = 1	13.65 V	2.3.1
Typical threshold voltage hysteresis	1.2 V	2.3.1
$I_{(INx+SENSEx),\ typ}$ Typical sum of current drawn from IN and SENSE pins across temperature	2.2 mA per 2.47 mA per channel	3.2.2.1
$I_{(INx+SENSEx),\ max}$ Maximum sum of current drawn from IN and SENSE pins across temperature	2.1 mA to 2.83 mA per channel; 30 V < V_{SENSE} < 36 V	3.2.2.1
Power consumption	859 mW for 16 channels, 24 V_{IN}	3.2.2.1
Maximum sampling speed, serial	100 kHz (200 kbps) per channel	3.2.2.3
Maximum sampling speed, parallel	2 MHz (4 Mbps) per channel	3.2.2.3
Thermal dissipation	43°C max after 1 hour of continuous operation, 24 V_{IN}, 25°C ambient temperature	3.2.2.1
ISO121x CHARACTERISTICS		
Propagation delay	125 ns	
Isolation rating	3 kV_{RMS}	
Working voltage	500 V_{RMS} for 1 minute	
Common-mode transient immunity	25 kV/µs	
Maximum standoff voltage at input pins	±60 V	

2 System Overview

2.1 Block Diagram

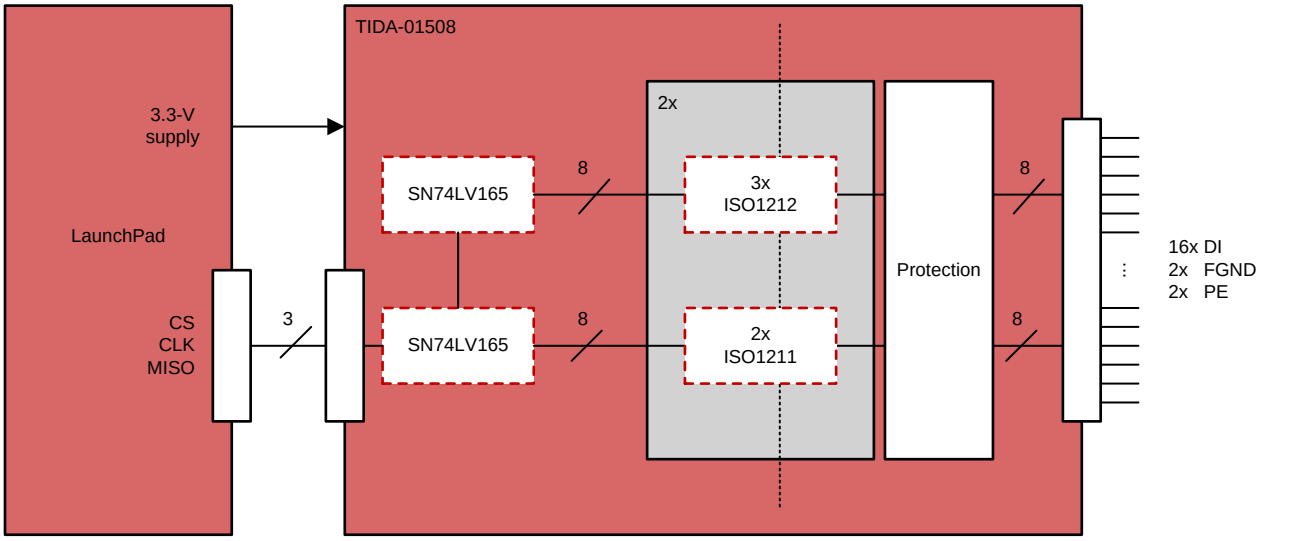


図 1. Block Diagram of TIDA-01508

2.2 Highlighted Products

2.2.1 ISO121x

The ISO1211 and ISO1212 are isolated 24-V digital input receivers, compliant to IEC 61131-2 Type 1, 2, and 3 characteristics, and suitable for programmable logic controllers (PLCs) and motor-control digital input modules. Unlike traditional optocoupler solutions with discrete, imprecise current limiting circuitry, the ISO121x devices provide a simple, low-power solution with an accurate current limit to enable the design of compact and high-density I/O modules. These devices do not require field-side power supply and are compatible with high-side or low-side switches. The ISO121x devices operate over the supply range of 2.25 V to 5.5 V, supporting 2.5-V, 3.3-V, and 5-V controllers. A ±60-V input tolerance with reverse polarity protection helps ensure the input pins are protected in case of faults with negligible reverse current. These devices support up to 4-Mbps data rates passing a minimum pulse width of 150 ns for high-speed operation. The ISO1211 device is ideal for designs that require channel-to-channel isolation and the ISO1212 device is ideal for multichannel space-constrained designs.

図 2 shows the functional block diagram of one channel of the ISO121x family.

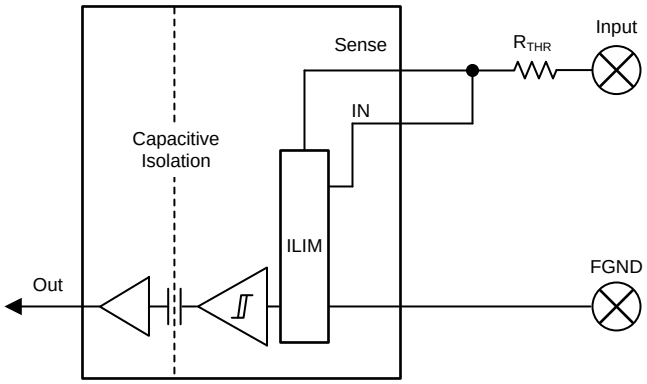


図 2. Functional Block Diagram of ISO121x

2.2.2 SN74LV165A

The SN74LV165A devices are parallel-load, 8-bit shift registers designed for 2-V to 5.5-V VCC operation. When the devices are clocked, data is shifted toward the serial output QH. Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the shift/load (SH/LD) input. The SN74LV165A devices feature a clock-inhibit function and a complemented serial output, QH.

図 3 shows a functional block diagram of SN74LV165A.

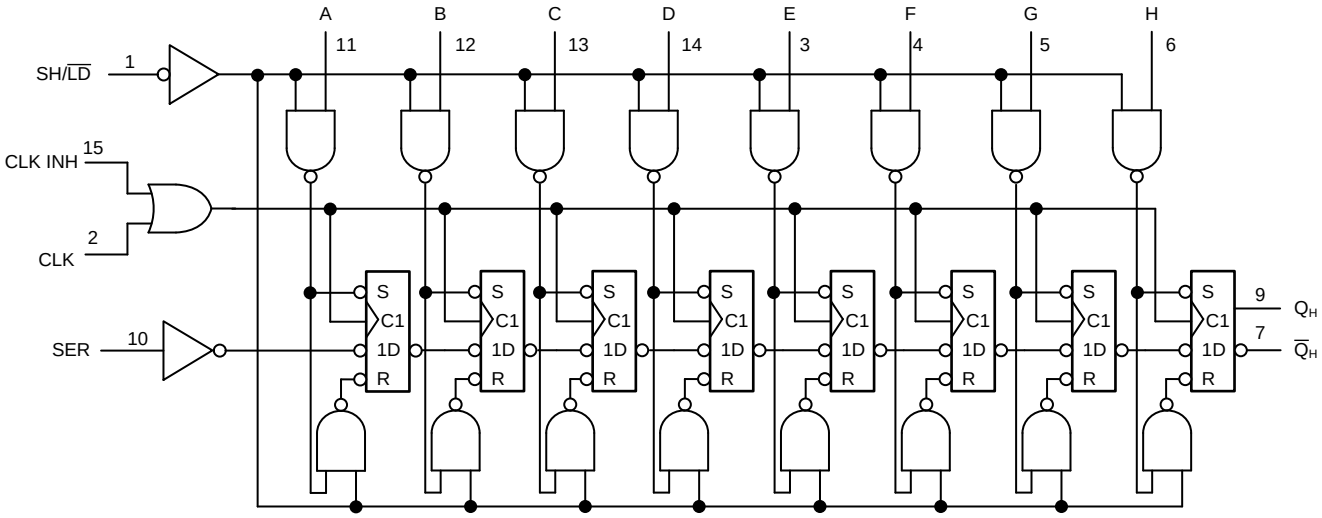


図 3. Functional Block Diagram of SN74LV165A

2.2.3 SN74LVC1GU04

This single inverter gate is designed for 1.65-V to 5.5-V VCC operation. The SN74LVC1GU04 device contains one inverter with an unbuffered output and performs the boolean function Y = $\overline{A}$.

2.2.4 TVS3300

The TVS3300 is a transient voltage suppressor that provides robust protection for electronic circuits exposed to high transient voltage events. Unlike a traditional TVS diode, the TVS3300 precision clamp triggers at a lower breakdown voltage and regulates to maintain a flat clamping voltage throughout a transient overvoltage event. The lower clamping voltage combined with a low dynamic resistance enables a unique TVS protection solution that can lower the voltage a system is exposed during a surge event by up to 30% in unidirectional configuration and up to 20% in bidirectional configuration when compared to traditional TVS diodes.

2.3 System Design Theory

This section explains the digital input stage and readout functionality of the design.

2.3.1 Digital Input Stage

The 16 inputs of this reference design are built up in two groups of eight channels. Three dual-channel ISO1212 and two single-channel ISO1211 are used per group so that maximum flexibility is provided to the user. 図 4 and 図 5 show the input stages of one ISO1212 and one ISO1211, respectively. Although not visible in these figures, pin FGND of the ISO1211 as well as pins FGND1 and FGND2 of the ISO1212 are all connected to input port FGND, which is the common field ground of all digital inputs.

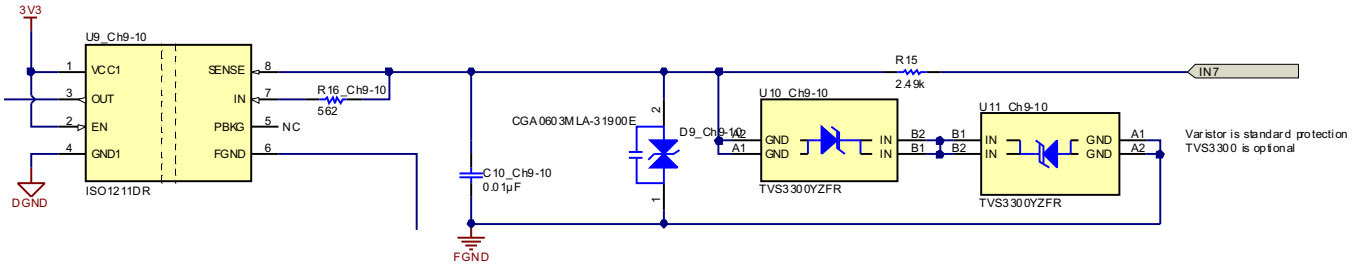


図 4. ISO1211 Input Stage Schematic

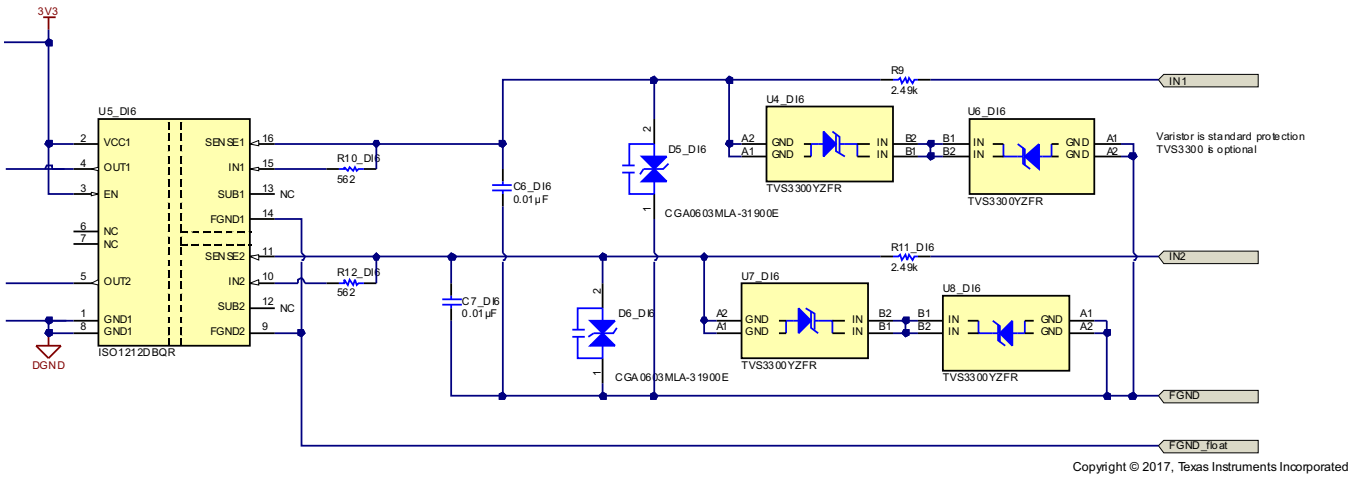


図 5. ISO1212 Input Stage Schematic

Every input of the ISO1211 can be configured for Type 1, 2, 3 characteristics according to IEC 61131-2 with resistors R_{THR} and R_{SENSE}. In addition, an input capacitor C_{IN} is connected after R_{THR} to GND creating an RC filter with R_{THR} for further protection against ESD, EFT, and surge events. To withstand high pulse voltages, R_{THR} is selected as a pulse proof resistor. 表 2 shows the configuration for Type 1 and 3 digital inputs as well as the resulting voltage ratings according to IEC 61002-4-2, IEC 61002-4-4, and IEC 61002-4-5 for specific values of R_{THR}, R_{SENSE}, and C_{IN}, respectively.

表 2. Surge, ESD, and EFT

IEC 61131-2 TYPE	R_{SENSE}	R_{THR}	C_{IN}	SURGE			ESD	IEC EFT
				LINE-TO-PE	LINE-TO-LINE	LINE-TO-FGND		
Type 1	562	3 kΩ	10 nF	±1 kV	±1 kV	±1 kV	±6 kV	±4 kV
Type 3	562	1 kΩ	10 nF	±1 kV	±1 kV	±500 kV	±6 kV	±4 kV
			330 nF	±1 kV	±1 kV	±1 kV	±6 kV	±4 kV

To protect the inputs against surge events with even higher ratings, all inputs are as well protected with either a varistor or two TVS3300 TVS diodes. Those devices are placed in parallel to C_{IN}.

In this design, all channels as configured for Type 1 inputs with R_{THR} = 2.4 kΩ and R_{SENSE} = 562 Ω. The typical high-level threshold V_{IH} and minimum low-level threshold V_{IL} at the ISO121x input (include R_{THR}) for output high and low are given by 式 1 and 式 2.

$$V_{IH}\left(typ\right) = 8.25\ V + R_{THR} \times \frac{2.25\ mA \times 562\ \Omega}{R_{SENSE}} = 13.65\ V \quad (1)$$

$$V_{IL}\left(min\right) = 7.1\ V + R_{THR} \times \frac{2.25\ mA \times 562\ \Omega}{R_{SENSE}} = 12.5\ V \quad (2)$$

2.3.2 Readout of Digital Outputs

To readout the 16 digital output signals, there exist two options:

1. Parallel readout of output signals at connectors J5 (channels 1–8) and J8 (channels 9–16)
2. Serial readout of output signals from parallel-in serial-out registers U1 and U2

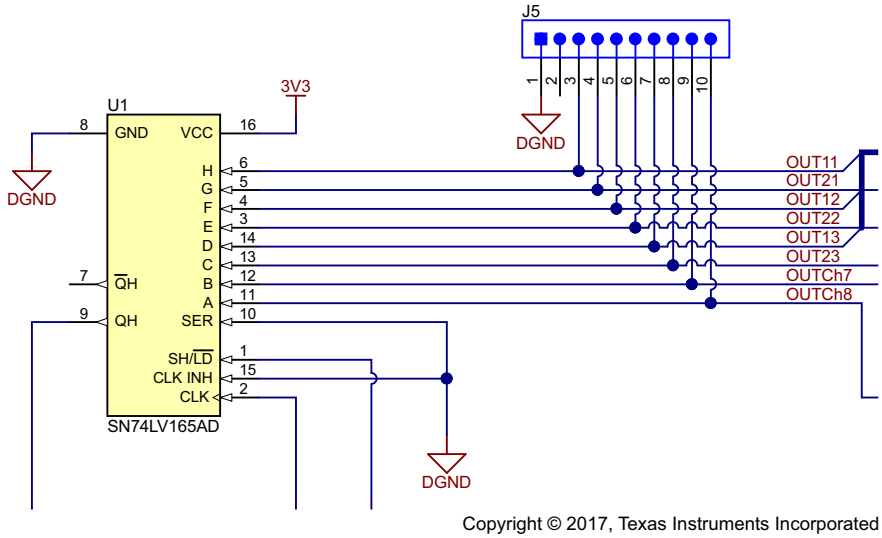


図 6. Schematic of Parallel and Serial Readout Options for Output Signals

For serial readout, all eight output signals per group are connected to the parallel-in serial-out register SN74LV165A. The output QH of register U1 is connected to input pin SER of register U2. To readout the register, the SPI of the LaunchPad is used. For this, the LaunchPad SPI is connected to the SN74LV165A registers as shown in 表 3:

表 3. Electrical Connections Between SPI and U1, U2

LAUNCHPAD	U1 (CHANNELS 1–8)	U2 (CHANNELS 9–16)
SPI_MOSI	Not used	Not used
SPI_MISO	Not connected	QH
SPI_nCS	SH/$\overline{LD}$	SH/$\overline{LD}$
SPI_CLK	CLK	CLK
	QH	SER

注: The SPI_nCS signal of the LaunchPad is inverted using a logic gate SN74LVC1GU04 with function Y = $\overline{A}$.

→ SPI_nCS logic '0' / low = logic '1' / high at SH/$\overline{LD}$ pin of SN74LV165A

The readout of the 16 output states works as follows:

1. SPI_nCS is high → both SN74LV165A continuously load input states
2. SPI_nCS pulled low → both SN74LV165A store current status of their respective eight inputs
3. SPI_CLK is clocked 16 times → output QH of register U2 first gives out outputs states of inputs H–A (channel 9–16) of U2, second gives out output states H–A (channel 1–8) of U1.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

The board can be powered and interfaced over connectors J1–J4. 図 7 shows a snapshot of the interface. To simplify the evaluation, it is recommended to use a LaunchPad like the MSP430FR5969 or the CC3220 to power and interface the board.

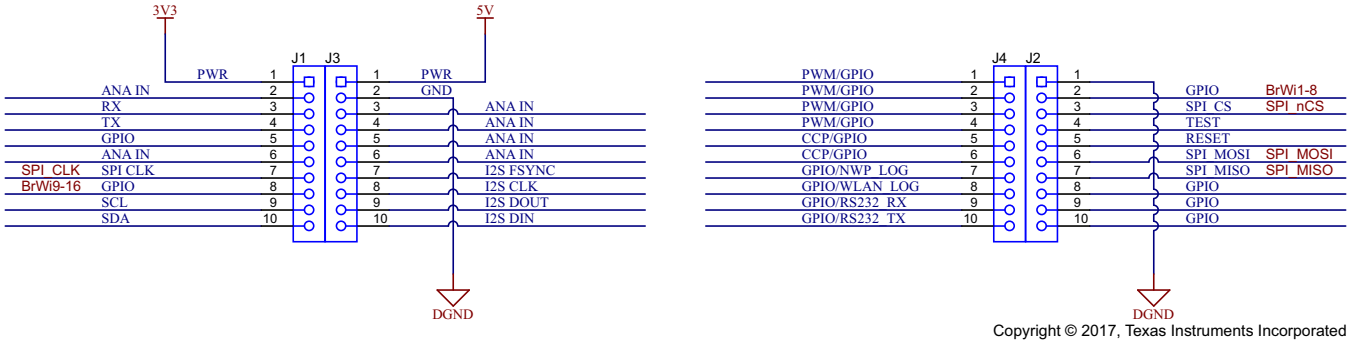


図 7. BoosterPack Interface of TIDA-01508

3.1.1 Hardware

- Laptop
- MSP430FR5969 LaunchPad
- Signal generator and scope: National Instruments Virtual Bench
- Precision source measure unit (SMU): Keysight B2912A

3.1.2 Software

For parallel readout of the output signals of the ISO121x devices, no special hardware is required. For serial readout using registers U1 and U2, program an SPI routine as described in 2.3.2.

3.2 Testing and Results

3.2.1 Test Setup

This reference design is plugged onto an MSP430™ LaunchPad, which is connected over USB to a laptop. The laptop is used to readout these stored values. Registers U1 and U2 are read out using the SPI of the LaunchPad. The LaunchPad performs multiple readout and stores the data in its memory. Afterwards, the information is sent to the laptop using the USB interface of the LaunchPad. To generate the digital input signals, test the voltage thresholds, and to measure the power consumption, the SMU is used.

図 8 shows a simple picture of the test setup.

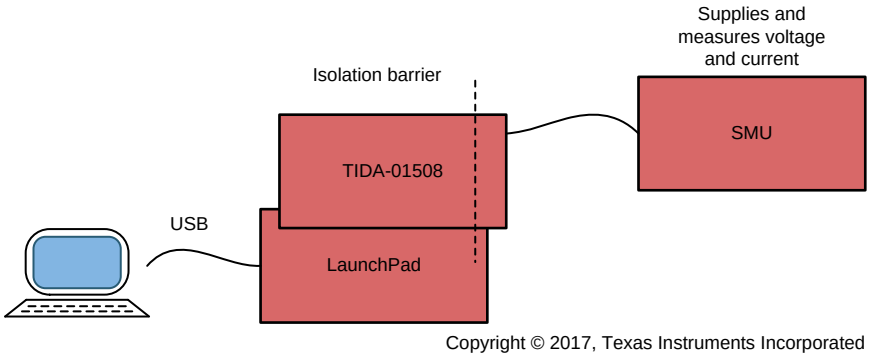


図 8. Test Setup of TIDA-01508

3.2.2 Test Results

3.2.2.1 Power Dissipation and Thermal Images

To test the power dissipation of the 16 inputs, a 24-V signal is connected from the SMU to each input. The current that is drawn from the inputs is measured by the same SMU. The setup is left running for one hour, then the current measured and a thermal image is taken.

All 16 inputs together draw a current of 35.8 mA. Therefore, the power dissipation of all 16 channels together is 24 V × 35.8 mA = 859.2 mW. This means that every channel is only drawing 2.2375 mA in average.

The thermal images show that the two channel devices (ISO1212) heat up to 43°C (see 図 9). The ambient temperature is around 25.8°C, which is a difference of 17.2°C. Furthermore, this difference shows that the devices only dissipate a small amount of energy, which enables to use them also in applications with high ambient temperatures.

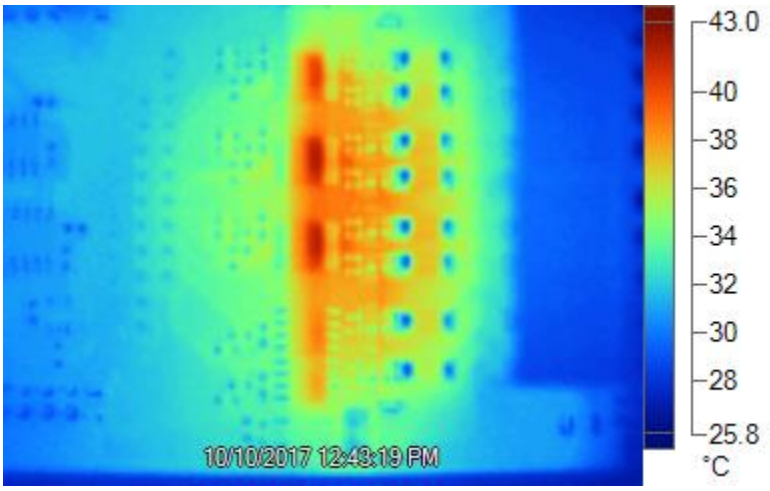


図 9. Thermal Image of TIDA-01508 After 1 Hour With 24-V Input Connected to Every Channel

Next, the input signals are changed to 30 V and the test is repeated. The resulting input current is now 36.3 mA, which results in a power dissipation of 1089 mW. Hence, every channel is only drawing 2.26875 mA in average. Furthermore, this value shows that even for input voltages, the input current stays low.

The power dissipation of the rest of the board is also measured. For an input voltage of 3.3 V, the board consumes 41 mA, which results in an additional 135-mW power dissipation, dominated by the LED power dissipation. This value is the same for 24-V inputs and 30-V inputs.

3.2.2.2 Serial Readout of Output States

図 10 shows the CLK and MISO signal lines of the SPI for the readout of 16 channels. The output states of the channels are 0-0-1-1-1-1-0-1 and 1-1-0-1-1-0-1-0 (channels 9–16 and channels 1–8, respectively). The SPI is running at a frequency of 8 MHz. The overall readout procedure takes around 6 µs. This results in a readout frequency of around 167 kHz.

There is a delay between the readout of the first eight channels and the second eight channels. In a final application, this delay can be optimized to achieve higher readout frequencies.

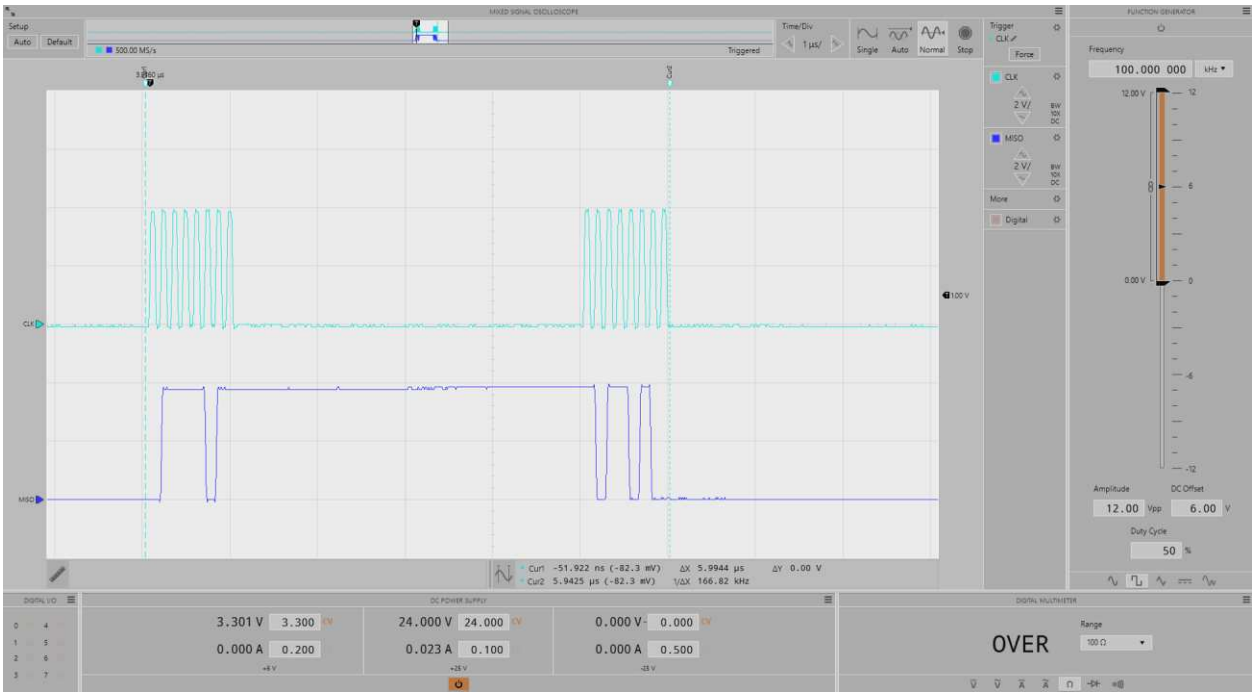


図 10. Readout Procedure With SPI Running at 8 MHz

図 11 shows the readout procedure for the first eight channels when the SPI is running at 16 MHz. This results in a readout time for eight output states of only 600 ns. Also for this higher speed, the readout works fine.

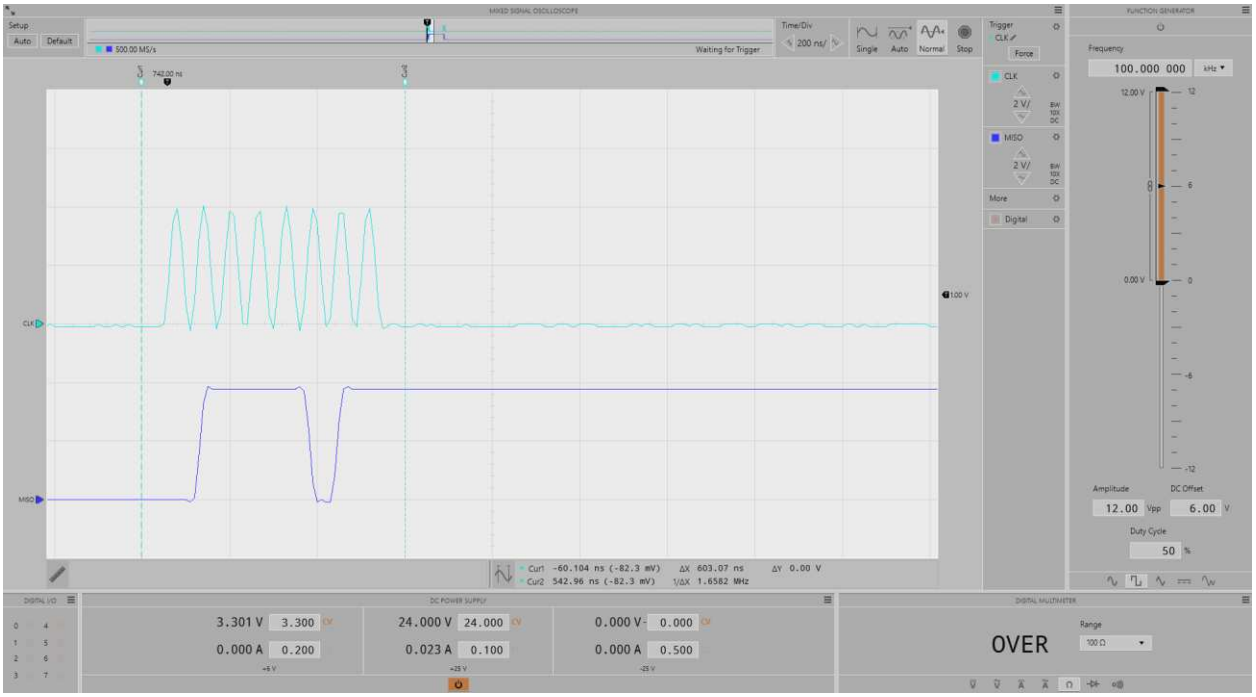


図 11. Readout Procedure With SPI Running at 16 MHz

3.2.2.3 Input Switching Frequency

Both TVS3300 and varistor inputs are tested up to 100 kHz by using the signal generator of the SMU. Because the signal generator only supports signals up to 12 V peak to peak, the voltage threshold resistor R_{THR} has been removed for this test so that the voltage thresholds of the ISO121x are low enough. The signal is set to 12 V peak to peak, rectangular waveform, 100 kHz.

The outputs of the ISO121x are measured with a scope. Furthermore, a 150-mΩ resistor is placed between the GND of this reference design and the actual GND of the power supply to observe peak currents with a scope. 図 12 shows an input protected with the TVS3300, and 図 13 shows an input protected with the varistor.

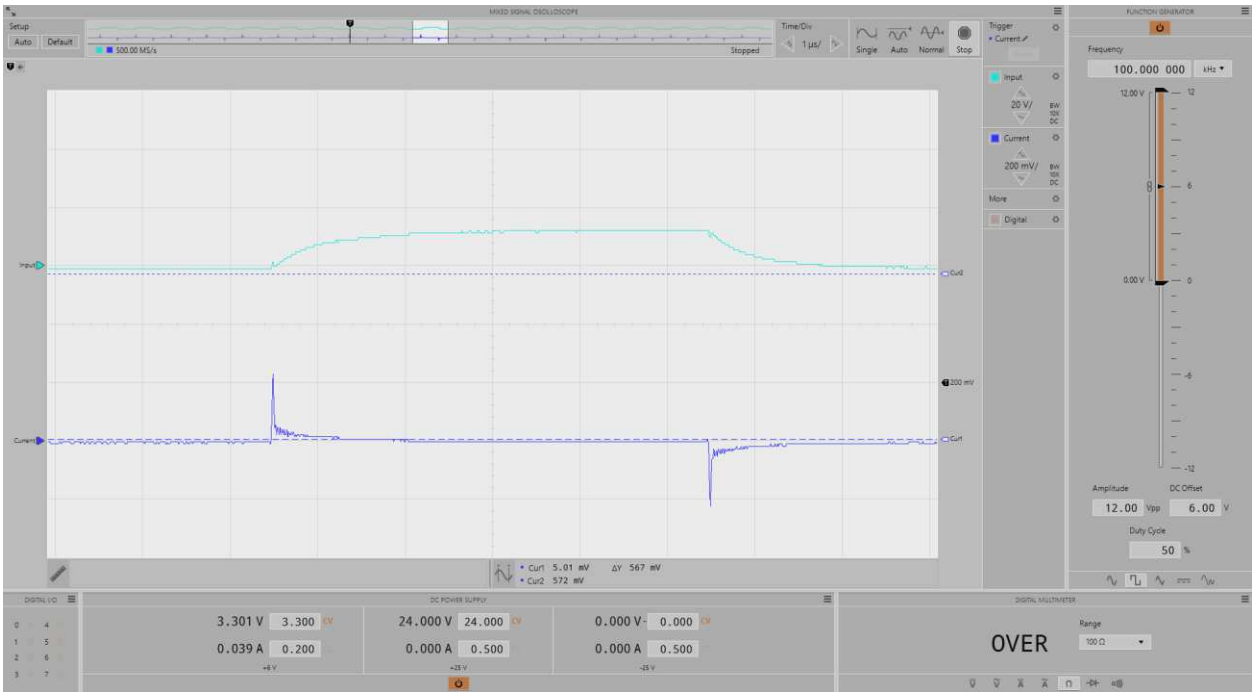


図 12. Switching of Outputs and Peak Currents With TVS Protection

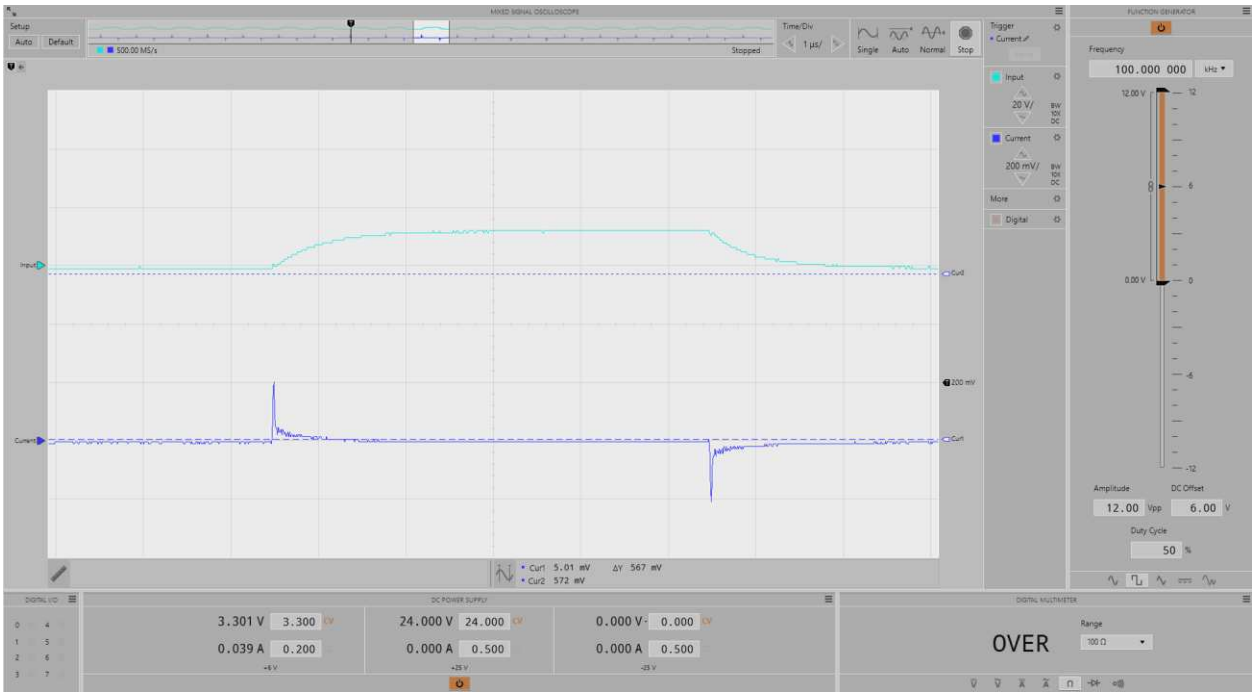


図 13. Switching of Outputs and Peak Currents With Varistor Protection

For both protection schemes, the switching can go up to 100 kHz without any problem. Furthermore, when the 12-V signal is switching, a peak current of 200 mV/150 mΩ = 1.3 A is flowing for a very short time. This is due to the input capacitor in front of the ISO121x.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01508.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01508.

4.3 PCB Layout Recommendations

For layout guidelines regarding the digital input stage, refer to the Layout section of *ISO121x Isolated 24-V to 60-V Digital Input Receivers for Digital Input Modules* .

4.3.1 Protection Circuit Input Stage

図 14 shows the two input stages of one ISO1212 from left to right. In this case, the protection circuit consists of the resistor R_{THR} and a varistor. Depending on the channel, the varistor can also be replaced by two TVS3300 devices. The two smaller components next to the ISO1211 input pins are the input capacitor C_{IN} and the sense resistor R_{SENSE}.

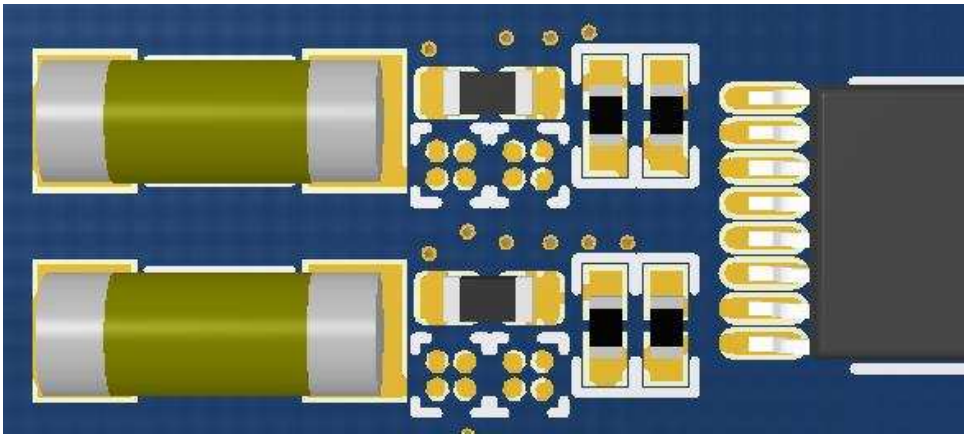


図 14. Input Protection Stage of ISO1212

As described in 2.3.1, R_{THR} is a pulse proof resistor in a 0207 footprint. After R_{THR} is passed, the signal line is first routed through the pads of the TVS3300, and varistors before it are connected to the pads of C_{IN} and R_{SENSE}. This connection ensures that in case of ESD, EFT, or surge events, the protection stage is always passed first before any possibly damaging voltage or current strikes reach the ISO121x. Furthermore, this results in a distance around 8 mm between the high-voltage side or left pad of R_{THR}, where the ESD, EFT, or surge event hits first, and the pad of C_{IN}. This distance results in additional protection against voltage spikes.

In general, do not place the resistor pad connected to external high voltage within 4 mm of the ISO121x device pins or the C_{IN} and R_{SENSE} pins to avoid flashovers during EMC tests (refer to the Layout section of *ISO121x Isolated 24-V to 60-V Digital Input Receivers for Digital Input Modules*).

4.3.2 Layout Prints

To download the layer plots, see the design files at TIDA-01508.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01508.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01508.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01508.

5 Software Files

To download the software files, see the design files at TIDA-01508.

6 Related Documentation

1. Texas Instruments, *ISO121x Isolated 24-V to 60-V Digital Input Receivers for Digital Input Modules Data Sheet*
2. Texas Instruments, *SNx4LV165A Parallel-Load 8-Bit Shift Registers Data Sheet*
3. Texas Instruments, *SN74LVC1GU04 Single Inverter Gate Data Sheet*
4. Texas Instruments, *TVS3300 33-V Precision Surge Protection Clamp Data Sheet*

6.1 商標

7 About the Author

TOBIAS PUETZ is a systems engineer in the Texas Instruments Factory Automation and Control team, where he is focusing on PLC and robotics. Tobias brings to this role his expertise in various sensing technologies as well as power design. Tobias earned his master's degree in electrical engineering and information technology at the Karlsruhe Institute of Technology (KIT), Germany in 2014.

7.1 Acknowledgments

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TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関係する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、あるいはTIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。