参考資料

TI Designs: TIDA-01558
DC UPS用の98%効率、全アナログ、24V～36V、500Wバックアップおよび50W充電器のリファレンス・デザイン

概要

このアナログ、双方向電力変換のリファレンス・デザインには、500Wの放電または昇圧段と、50Wの充電または降圧段があります。このリファレンス・デザインは24Vバッテリ・パックと、30V～38Vのバス電圧用に作成されており、DC-UPS、バッテリ・バックアップ・ユニット(BBU)、ローカル・エネルギー・ストレージ(LES)、DC/DCブリック・モジュールに使用できます。このデザインは放電が98%超、充電が95%超の高効率であるため、熱管理が最適化され、バッテリ・バックアップの時間が延長されます。

リソース

TIDA-01558	デザイン・フォルダ
TPS43060	プロダクト・フォルダ
LMR14020	プロダクト・フォルダ
CSD18532KCS	プロダクト・フォルダ
LM358A	プロダクト・フォルダ
LM293A	プロダクト・フォルダ
TLV704	プロダクト・フォルダ

TI E2E™ Community

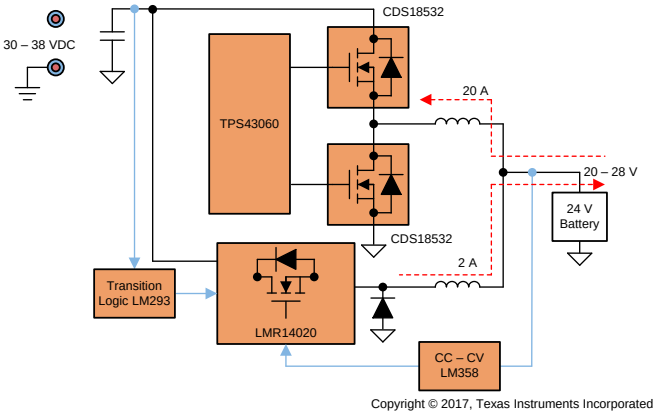
E2Eエキスパートに質問

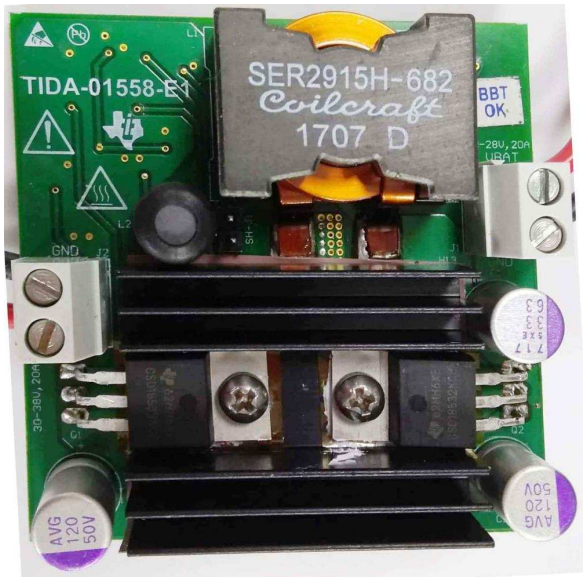
特長

- ピーク約98.3%、全負荷で約97.4%の高効率のバックアップ・バッテリ電源
- バックアップ電源として20A、30Vの大電力出力を実現し、通常動作時に2Aでバッテリを充電
- 充電中からバックアップ電源モードに500µs以内で切り替わる高速チェンジオーバーにより、電源障害時に高速な電力供給が可能
- ヒートシンク内蔵のコンパクトなソリューション(65mm×60mm×25mm)
- モード切り替え用の完全な組み込みアナログ・ソリューションと、CC-CVロジックの実装により、ソリューションの総コストを低減

アプリケーション

- DC-UPSバッテリ
- バックアップ・ユニット(BBU)
- ローカル・エネルギー・ストレージ(LES)
- DC/DCブリック・モジュール





1 System Description

There is a demand for a bidirectional power supply for the battery backup units (BBUs) used in industrial DC UPS and single-phase UPS with solar panel input to convert 24 V_{BATT} (battery voltage) to 36 V_{BUS} (line voltage). These battery backup and power storage systems also find a role in many other industrial applications like BBU, local energy storage (LES), and DC/DC brick modules. The main function of these DC/DC battery backup systems is to provide reliable power during power failure and ensure uninterrupted plant operation. The most common DC voltages in use are 48 V, 24 V, and 12 V. 図 1 shows the typical power flow for a 24-V system.

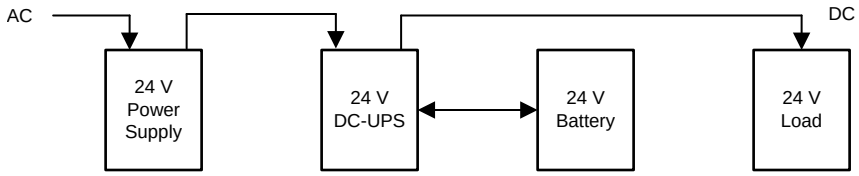


図 1. 24-V System Block Diagram

A typical battery backup or energy storage bank has the following subsystems:

1. A battery charger subsystem to charge the battery from a power source
2. A battery discharge subsystem to power a load from the battery
3. A battery management solution (BMS) system to monitor and protect the battery

Under normal operating conditions, the battery backup system draws power from the DC bus to charge the battery bank and the battery discharge system remains inactive. Upon power failure of the DC bus input, the battery discharge system takes over and begins to immediately feed power into the DC bus. During this time the battery charger system remains inactive. 図 2 shows a typical functional diagram of DC-UPS and where this reference design fits in the system.

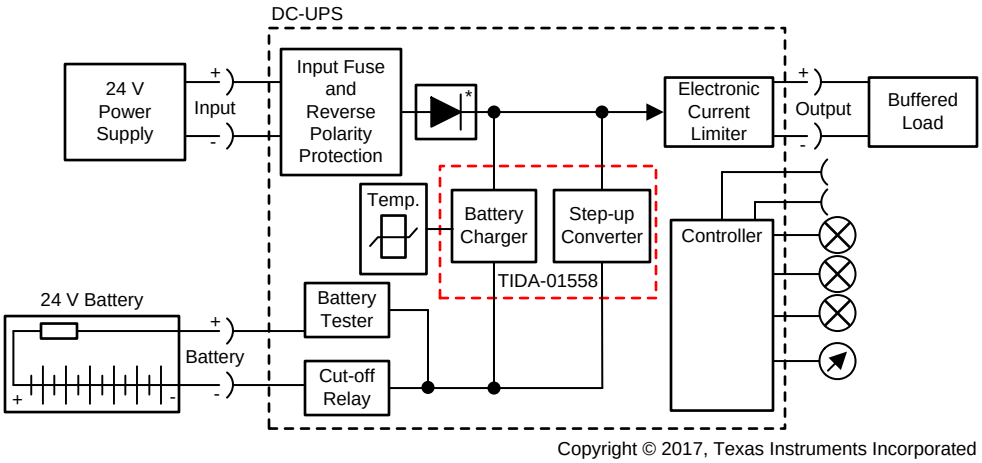


図 2. Functional Diagram of DC-UPS

The key features for these bidirectional power supplies are simplicity and solution cost. The conventional approach involves going for a digitally-controlled power supply, which tends to make the solution complex and relatively expensive. Another approach for these systems is to implement a four-switch buck-boost bidirectional converter, which also tend to be relatively expensive. This design takes an simpler alternative and cost-effective analog approach that uses basic buck and boost controllers to achieve the same functionality with very high efficiency and fast transition from charging to backup supply.

This two stage design uses synchronous boost topology with the TPS43060 controller for discharge state and buck topology implemented with the LMR14020 for battery charging state. The design is capable of delivering 500 W as the backup power and 50 W as battery charger. The transition logic for changeover from discharge to charge state is implemented with comparator LM293, and the CC-CV profile for battery charging is implemented with a basic LM358 dual op amp by TI.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SYMBOL	TEST CONDITION	MINIMUM	NOMINAL	MAXIMUM	UNIT
BACKUP SUPPLY MODE (BOOST STAGE)						
Input voltage (battery voltage)	V_{BAT}	—	20	24	28	v
Output voltage (bus voltage)	V_{BUS}	—	29.7	30	30.3	V
Output current (bus current)	I_{BUS}	—	—	—	16.5	A
Line regulation (20 V – 28V_INDC)	—	At full load	—	—	±1	%
Load regulation (20 V – 28V_INDC)	—	10 to 100% load	—	—	±1	%
Output voltage ripple	—	At full load	—	—	300	mV
Input voltage ripple	—	At full load	—	—	240	mV
Efficiency	Throughout Input Voltage, V_{BAT}	At 100% load	96.06	—	98.10	%
		At 50% load	97.65		98.79	
		At 20% load	97.25		97.41	
Output power	—	—	—	—	500	W
BATTERY CHARGER MODE (BUCK STAGE)						
Input voltage (bus voltage)	V_{BUS}	—	32	36	38	V
Output voltage (battery voltage)	V_{BAT}	—	—	—	24	V
Output current (battery current)	I_{BAT}	—	—	—	2	A
Output voltage ripple	—	At full load	—	—	300	mV
Efficiency	—	10 to 100% load	89.15	—	95.75	%
Output power	—	—	—	—	50	W
Operating ambient	—	—	–20	25	55	°C
Dimension	—	Length × breadth × height	60 × 60 × 16 , two layer, 2-oz copper			mm

2 System Overview

2.1 Block Diagram

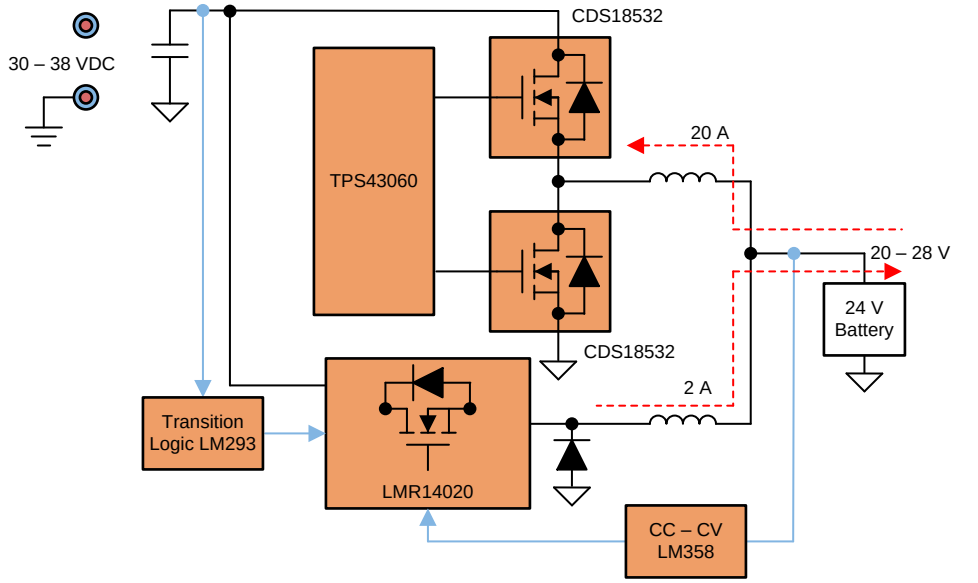


図 3. TIDA-01558 Block Diagram

2.2 Highlighted Products

The following are the highlighted products used in this reference design. Key features for selecting the devices for this reference design are described. Complete details of the highlighted devices can be found in respective product data sheets.

2.2.1 TPS43060

In order to achieve the desired cost and performance of the design for the given voltage levels, a low-quiescent current synchronous boost DC-DC controller TPS43060 is a preferred choice.

The TPS43060 is a low-IQ current mode synchronous boost controller with wide-input voltage range from 4.5 V to 38 V (40 V absolute maximum) and boosted output range up to 58 V. Synchronous rectification enables high-efficiency for high-current applications. A 3-mm × 3-mm WQFN-16 package with PowerPAD™ integrated circuit package of TPS43060 supports high-power density. The TPS43060 includes a 7.5-V gate drive supply, which is suitable to drive a broad range of MOSFETs. Voltage regulation is achieved by employing constant frequency current mode pulse-duration modulation (PWM) control. The switching frequency is set either by an external timing resistor or by synchronizing to an external clock signal.

Some of the key features include:

- 58-V maximum output voltage
- 4.5 V to 38 V (40-V absolute maximum) VIN range
- Adjustable frequency from 50 kHz to 1 MHz
- Adjustable soft-start time
- Inductor DCR or resistor current sensing

- Output voltage power-good indicator
- Cycle-by-cycle current limit and thermal shutdown

2.2.2 LMR14020

In order to make the solution compact, a simple integrated buck controller is preferred.

The LMR14020 SIMPLE SWITCHER® power converter regulator is an easy-to-use, step-down DC/DC converter that operates from 4-V to 40-V supply voltage. The device integrates a 90-mΩ (typical) high-side MOSFET and is capable of delivering up to 2-A DC load current with exceptional efficiency and thermal performance in a very small solution size. The operating current is typically 40 μA under no load condition (not switching). When the device is disabled, the supply current is typically 1 μA.

The LMR14020 implements constant frequency peak current mode control with sleep-mode at light load to achieve high efficiency. The device is internally compensated, which reduces design time, and requires fewer external components. The switching frequency is programmable from 200 kHz to 2.5 MHz by an external resistor RT. For other features and more information, refer to the *LMR14020 SIMPLE SWITCHER® 40 V 2 A, 2.2 MHz Step-Down Converter with 40 μA I_Q Data Sheet*[1]

2.2.3 CSD18532KCS

For effective thermal management in small form-factor, high-power density designs, it is vital to have high-efficiency devices and the capability to extract heat effectively.

CSD18532KCS is a 60-V TO-220 N-Channel MOSFET with ultra low Q_g and Q_{gd}. A low R_{dson} of around 5 mΩ at 60°C and 7.5-V gate drive voltage helps keep the power dissipation low. More details on this FET can be obtained from the *CSD18532KCS 60-V N-Channel NexFET™ Power MOSFET Data Sheet*[2].

2.3 System Design Theory

This reference design is a 500-W boost, 50-W buck DC/DC bidirectional power converter. The aim of this design is to develop a high-efficiency, cost-competitive, and compact non-isolated bidirectional power converter that can deliver 500 W of load power from a 24-V battery bank when V_{BUS} is not present and charge the battery at 2 A when V_{BUS} is present. The design is realized with a two-switch synchronous boost stage and an integrated buck stage with boost converter operating at 100 kHz while buck converter operating at 500 kHz.

2.3.1 Operating Principle

Because this is a backup power supply design, the power transfer to load happens when V_{BUS} falls below the acceptable level, and the battery is charged when V_{BUS} comes back to a stable value. For this design, the synchronous boost stage takes over when the V_{BUS} drops. The synchronous boost stage transfers power from the 24-V battery bank to the load. Once the V_{BUS} comes back, the boost stage is disabled, and the buck stage is enabled, which charges the 24-V battery.

This reference design is designed for the following voltage levels for enabling and disabling of the two stages:

1. Buck stage or the battery charging is disabled when the V_{BUS} falls below 31 V.
2. Boost stage is enabled when the V_{BUS} falls below 30 V, which is the regulated output voltage of the converter.
3. Boost stage is disabled when V_{BUS} is maintained at a voltage higher than the regulated output, that is, 30 V.

4. Buck stage is enabled when V_{BUS} goes above 32 V and starts to charge the battery pack again.

The power flow of the buck and boost stage is shown in 図 4 for charge mode (buck) and in 図 5 for discharge mode (boost).

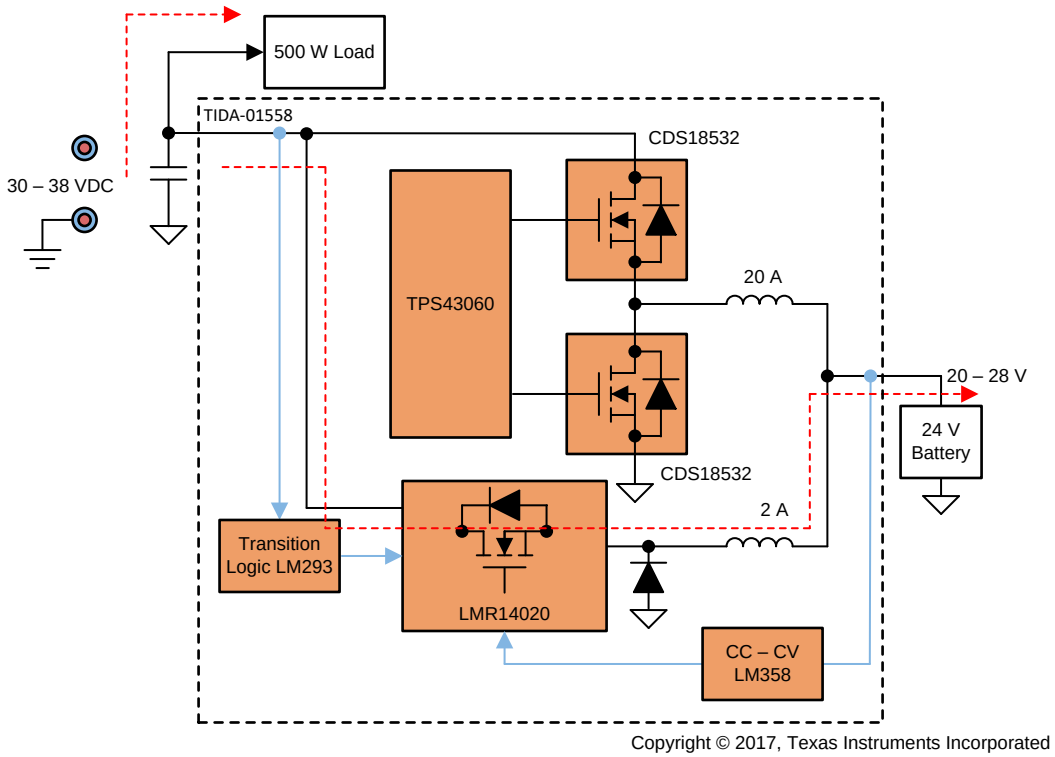


図 4. Power Flow in Charge (Buck) Mode

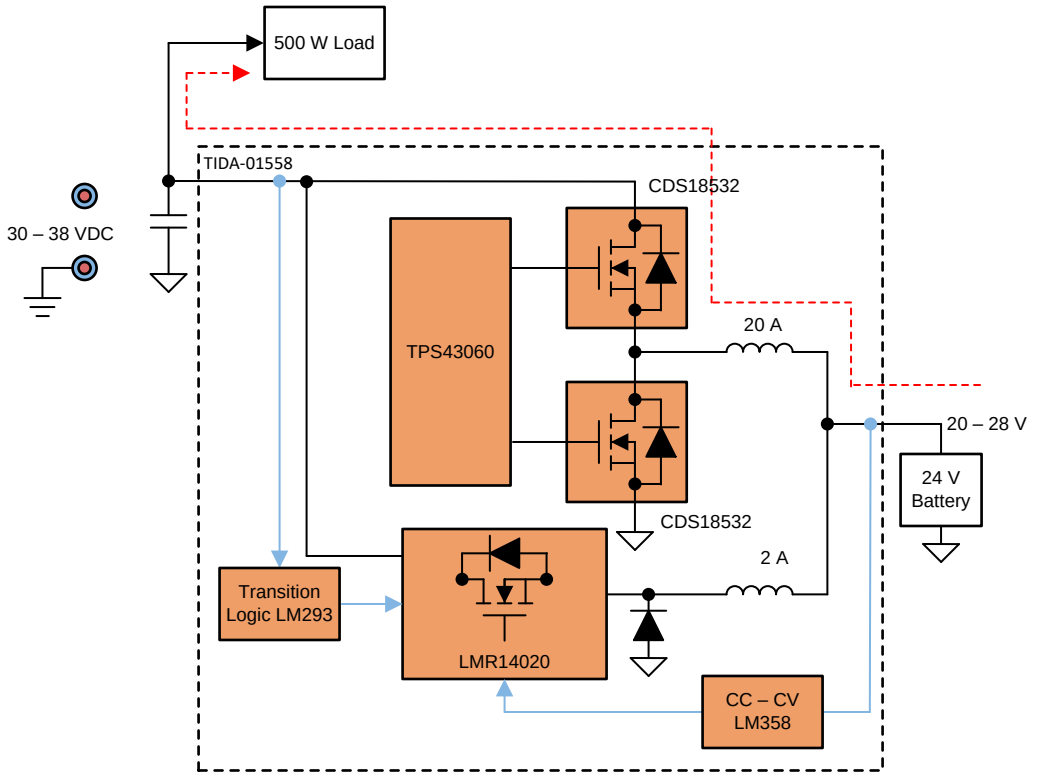


図 5. Power Flow in Discharge (Boost) Mode

2.3.2 Boost Stage Calculations

In the following sections calculations for the power stage are shown along with approximate loss estimation on the major components.

2.3.2.1 Selection of Switching Frequency

First determine the switching frequency of the power converter. There are a certain tradeoffs to consider when selecting switching frequency. A higher switching frequency allows for lower-value inductors and smaller-output capacitors compared to a power converter that switches at a lower frequency. A lower switching frequency produces a larger solution size but typically has better efficiency. Setting the frequency for the minimum tolerable efficiency produces the optimum solution size for the application. For this design, a switching frequency of 100 kHz was chosen as a compromise between efficiency and small solution size. For the boost controller used in this design, TPS43060, the switching frequency is determined by the timing resistor RT as per 式 1.

$$\mathrm{RT}\left(\mathrm{k\Omega}\right) = \frac{57500}{\mathrm{fsw}\left(\mathrm{kHz}\right)} = \frac{57500}{100\left(\mathrm{kHz}\right)} = 575\ \mathrm{k\Omega} \tag{1}$$

2.3.2.2 Inductor Selection

In a boost topology, the average inductor current is equal to the input current. The current delivered to the output is the input current modulated at the duty cycle of the PWM.

The maximum inductance required can be calculated from the maximum input voltage and the inductor ripple current that can be allowed. In order to get high efficiency and the dimension of the design in control, the inductor ripple current is taken to be around 60% of the average output current.

The maximum duty cycle operation at full output load is obtained when the input battery voltage is at its minimum. This is calculated by 式 2.

$$D_{MAX} = \frac{V_{OUT} - V_{IN\_MIN}}{V_{OUT}} = \frac{30 - 20}{30} = \frac{1}{3} \tag{2}$$

For calculating inductor ripple current, the average input current must be known. Considering the efficiency of 97%, the input current can be calculated as 式 3.

$$I_{IN\_AVG} = \frac{I_{OUT}}{1 - D} = \frac{\frac{P_{OUT}}{\eta \times V_{OUT}}}{1 - D_{MAX}} = \frac{\frac{500}{0.97 \times 30}}{1 - \frac{1}{3}} = 25.7732 \text{ A} \tag{3}$$

Now the desired ripple current is:

$$I_{RIPPLE} = 0.6 \times I_{IN} = 0.6 \times 25.7732 = 15.464 \tag{4}$$

The minimum boost inductor can then be calculated with 式 5.

$$L_{MIN\_BOOST} = \frac{V_{IN_{MIN}} \times D_{MAX}}{I_{RIPPLE} \times f\ sw} = \frac{20 \times \frac{1}{3}}{15.464 \times 100\ kHz} = 4.311\,\mu H \tag{5}$$

This design uses an inductor with 6.8-µH inductance. Ripple current with the selected inductor value can be calculated as 式 6.

$$I_{RIPPLE} = \frac{V_{IN\_MIN} \times D_{MAX}}{L_{SELECTED} \times f\ sw} = \frac{20 \times \frac{1}{3}}{6.8\ \mu H \times 100\ kHz} = 9.804 \text{ A} \tag{6}$$

While selecting the inductor, note the maximum current through inductor. The saturation current of the chosen inductor must be higher than the calculated peak inductor current. The peak current though the inductor can be calculated as 式 7.

$$I_{LPEAK} = I_{IN\_AVG} + \frac{I_{RIPPLE}}{2} = 25.7732 + \frac{9.804}{2} = 30.675 \text{ A} \tag{7}$$

Because the boost converter works in continuous conduction mode (CCM) at full load, the RMS current through the inductor can be calculated as 式 8.

$$I_{L_{RMS}} = \sqrt{I_{IN\_AVG}{}^2 + \left(\frac{I_{RIPPLE}}{\sqrt{12}}\right)^2} = \sqrt{25.7732^2 + \left(\frac{9.804}{\sqrt{12}}\right)^2} = 25.93 \text{ A} \tag{8}$$

The maximum loss on the inductor occurs at the maximum input voltage. The loss on the inductor can be divided into the core losses and the root mean square (RMS) current induced losses. The core loss depends on the switching frequency and flux swing. The RMS current induced losses are dictated by the DC resistance (DCR) of the inductor.

$$Pl_{LOSS} = Pl_{CORE_{LOSS}} + Pl\_DCR\_loss \tag{9}$$

The losses can be analyzed by using the graph given in the inductor selection sheet at http://www.coilcraft.com/coreloss. In this design the SER2915H-682KL inductor has been selected.

2.3.2.3 MOSFET Selection

In hard-switched synchronous boost topology, the switching MOSFET undergoes losses at turnon, conduction, and turnoff. However, the synchronous FET does not suffer turnon or turnoff losses but only MOSFET and internal body diode conduction losses.

The compact nature of the design and requirement for using TO-220 FET pose another significant challenge in terms of thermal management. Because the majority of losses in this design are going to be on the switching FET, the chosen FET must allow for an easy way to remove heat from the FET.

One of the major challenges in this design is choosing a FET that can help in minimizing the switching and conduction losses, which also allows for efficient heat removal.

The CSD18532KCS FET was chosen as it has low Rdson and very low Qg and Qgd, which can help decrease the conduction and switching losses.

In the following sections, the loss estimation of each of the FETs is calculated under nominal operating condition with Vin =24 V and full load of 500 W. Duty cycle at nominal operating condition shown in 式 10.

$$D_{NOM} = \frac{30 - 24}{30} = 0.2 \tag{10}$$

2.3.2.3.1 Losses in Synchronous FET

In hard-switched CCM synchronous boost converter, the turnon of the high-side MOSFET happens under the zero voltage switching (ZVS) condition as the voltage across the MOSFET is clamped by the current flowing through its internal body diode, which is around 1 V. The turnoff also occurs under ZVS condition if the current through the MOSFET is greater than zero at turnoff. Thus for this design, the switching loss of the MOSFET can be safely neglected. The conduction loss is calculated as 式 11.

$$P_{sync\_cond\_loss} = I_{sync\_FET(RMS)}^{2} \times R_{DSON}(60^{\circ}C) \tag{11}$$

The RMS current through sync FET can be calculated as 式 12.

$$I_{sync_{FET(RMS)}} = \sqrt{(1 - D_{NOM}) \times IL_{RMS}^{2}} = \sqrt{(1 - 0.2) \times 25.93^{2}} = 23.1925 \text{ A} \tag{12}$$

The conduction loss can now be calculated as $P_{SYNC_{COND_{LOSS}}} = 23.1925^{2} \times 5\,m\Omega = 2.69$ W.

The body diode loss during the dead time can be given by 式 13.

$$P_{body\_diode\_loss} = Vf \times \left(\left(I_{INAVG} + \frac{I_{RIPPLE}}{2} \right) \times DT_{on} + \left(I_{INAVG} - \frac{I_{RIPPLE}}{2} \right) \times DT_{off} \right) \times fsw \quad (13)$$

Where:

- Vf is the forward voltage drop of the body diode (0.8V typically)
- DTon is the dead time at turnon of the FET (65 ns, set by the controller)
- DToff is the dead time as turnoff of the FET (65 ns, set by the controller)

$$P_{body\_diode\_loss} = 0.8 \times \left(\left(25.7732 + \frac{9.804}{2} \right) \times 65\,ns + \left(25.7732 - \frac{9.804}{2} \right) \times 65\,ns \right) \times 100\,kHz = 0.268\,W$$

2.3.2.3.2 Losses in Main Switching FET

The losses in the switching FET can be divided into conduction loss and switching loss. The switching loss can be further divided into turnon and turnoff loss.

The turnon and turnoff losses can be calculated with 式 14 and 式 15 respectively.

$$P_{loss\_Turn\_on} = \frac{1}{2} \times V_{DS} \times I_{ds_{on}} \times t_{on} \times f_{sw} \quad (14)$$

$$P_{loss\_Turn\_off} = \frac{1}{2} \times V_{DS} \times I_{ds_{off}} \times t_{off} \times f_{sw} \quad (15)$$

Because the layout has a major role to play in switching losses, the switching losses theoretically cannot be accurately calculated—instead relying upon the practical results obtained. The turnon time of the main switching FET is observed to be around 35 ns while the turnoff time to be around 20 ns.

For the boost converter, the low-side FET turns on when the inductor current is minimum and turns off when the inductor current is maximum.

The switching loss can now be calculated as

$$P_{loss\_Turn\_on} = \frac{1}{2} \times 24 \times \left(25.7732 - \frac{9.804}{2} \right) \times 35\,ns \times 100\,kHz = 0.88\,W$$ and

$$P_{loss\_Turn\_off} = \frac{1}{2} \times 24 \times \left(25.7732 - \frac{9.804}{2} \right) \times 20\,ns \times 100\,kHz = 0.74\,W$$.

The total switching loss would be: P_(loss_Turn_on) + P_(loss_Turn_off) = 1.613 W

The reverse recovery loss from the body diode of the low-side MOSFET can be estimated using 式 16.

$$P_{RR\_DIODE} = Q_{RR} \times V_{IN} \times fsw \quad (16)$$

Here Qrr is the reverse recovery charge of the body diode and can be obtained from the *CSD18532KCS 60-V N-Channel NexFET™ Power MOSFET Data Sheet*[2].

For this design, $P_{RR\_DIODE} = 127\,nC \times 24 \times 100\,kHz = 0.305\,W$

The loss in the output capacitance, Coss, of the FET can be calculated as 式 17.

$$P_{COSS} = \frac{Coss \times fsw \times V_{IN}^2}{2} = \frac{470\,pF \times 100\,kHz \times 24^2}{2} = 13.54\,mW \quad (17)$$

The conduction loss of the main switching FET can be calculated as 式 18.

$$P_{main\_cond\_loss} = I_{main\_FET(RMS)}^2 \times R_{DSON}(60^{\circ}C) \quad (18)$$

The RMS current through the main switching FET can be calculated as 式 19.

$$I_{MAIN_{FET(RMS)}} = \sqrt{D_{NOM} \times IL_{RMS}{}^2} = \sqrt{0.2 \times 25.93^2} = 11.6 \text{ A} \quad (19)$$

The conduction loss can now be calculated as $Pmain\_cond\_loss = 11.6^2 \times 5\,m\Omega = 0.672\ W$.

2.3.2.4 Current Sense Resistor Selection

The external current sense resistor sets the cycle-by-cycle peak current limit. The peak current limit must be set to assure the maximum load current can be supported at the minimum input voltage.

At minimum input voltage, the duty cycle is 0.33 as calculated in 式 2. From the controller's datasheet, the current sense voltage threshold (Vcs) for 0.33 duty cycle is 72 mV. After keeping a 20% margin, the current sense resistor (Rcs) can now be calculated as 式 20.

$$R_{CS} = \frac{V_{CS}}{1.2 \times IL_{PEAK}} = \frac{72\ mV}{1.2 \times 30.675\ A} = 1.96\ m\Omega \quad (20)$$

This design uses a 2-mΩ sense resistor.

The power loss in the sense resistor can be estimated as 式 21.

$$P_{CS} = IL_{RMS}^{2} \times R_{CS} = 25.93\ A^{2} \times 2\ m\Omega = 1.345\ W \quad (21)$$

For proper sensing and filtering out noise, an RC filter of 4.7 Ω and 47 nF and ferrite bead of 600 Ω at 100 MHz is used at ISNS pins.

2.3.2.5 Output Capacitor Selection

The desired ripple voltage is 1% of output voltage: Vripple = 0.01 × 30 = 0.3 V

The worst case output ripple current occurs when the duty cycle is maximum. Thus for the operating frequency of 100 kHz, the required output capacitance is calculated as 式 22.

$$C_{OUT} > \frac{I_{OUT} \times D_{MAX}}{V_{RIPPLE} \times fsw} = \frac{16.67 \times \left(\frac{1}{3}\right)}{0.3 \times 100\ kHz} = 185\ \mu F \quad (22)$$

For this design, 2 × 120-µF, 50-V electrolytic and 4 × 10-µF, 50-V ceramic capacitors have been used with a combined ESR of 0.5 mΩ.

2.3.2.6 Bootstrap Capacitor Selection

A capacitor must be connected between the BOOT and SW pins for proper operation. This capacitor provides the instantaneous charge and gate drive voltage needed to turn on the high-side FET. Use 式 23 to limit the BOOT capacitor ripple voltage to 250 mV.

$$C_{BOOT} = \frac{Qg\left(\text{of selected FET}\right)}{\Delta V_{BOOT}} = \frac{44\ nC}{0.25} = 176\ nF \quad (23)$$

This design uses a 220-nF, 0603 ceramic capacitor for bootstrap.

2.3.2.7 Input Capacitor

For the desired 1% input voltage ripple and earlier calculated ripple current, the required input capacitor for 100 kHz switching can be calculated as 式 24.

$$C_{IN} > \frac{I_{RIPPLE}}{4 \times fsw \times V_{INRIPPLE}} = \frac{9.804}{4 \times 100\ kHz \times 0.24\ V} = 102\ \mu F \quad (24)$$

A 120-µF, 50-V electrolytic and a 10-µF, 50-V ceramic capacitor at the input.

2.3.2.8 Feedback Resistors Selection

The voltage divider at FB pin sets the output voltage. The FB pin threshold, VFB, is 1.22 V. With a 10-kΩ low-side resistor, the high-side resistor can be calculated as 式 25.

$$R_{HS} = R_{LS} \times \frac{V_{OUT} - VFB}{V_{OUT}} = 10\ k\Omega \times \frac{30\ V - 1.22\ V}{1.22\ V} = 236\ k\Omega \quad (25)$$

This design uses a 0603, 237-kΩ resistor.

2.3.2.9 Soft-Start Time

The soft-start capacitor determines the amount of time allowed for the output voltage to reach its nominal programmed value during power up. A controlled start-up time is necessary with large output capacitance to limit the current into the capacitor during start-up. Large input currents charging the output capacitors during start up can trigger the current limit. Excessive current drawn from the input power supply may also cause the input voltage rail to sag. The soft-start capacitor can be sized to limit in-rush current or output voltage overshoot during start up.

For a desired soft-start time of 100 µs, the soft-start capacitor can be calculated as 式 26.

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{REF}} \quad (26)$$

Here, Iss is the soft-start bias current (5 µA) set by controller: $C_{SS} = \frac{100\ \mu s \times 5\ \mu A}{1.22\ V} = 409.84\ pF$.

This design uses the nearest 390-pF capacitor.

2.3.2.10 Control Loop Compensation

The calculation of the control loop compensation components are done as per the *TPS4306x Low Quiescent Current Synchronous Boost DC-DC Controller With Wide V_{IN} Range Data Sheet*[3]. For a cut off frequency of 4.7 kHz, the calculated type-II compensation components are: Rcomp = 6.9 kΩ, Ccomp = 0.047 µF, and CHF = 470 pF.

2.3.3 Buck Stage Calculations

2.3.3.1 Output Voltage Set-Point and Feedback Resistors

The output voltage of LMR14020 is externally adjustable using a resistor divider network. The divider network is comprised of top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. 式 27 is used to determine the output voltage.

$$R_{FBT} = \frac{V_{OUT} - 0.75}{0.75} R_{FBB} \quad (27)$$

Let R_{FBB} be 10 kΩ, which results in the calculated value of R_{FBT} = 310 kΩ.

2.3.3.2 Switching Frequency

For desired frequency, use 式 28 to calculate the required value for R_T.

$$R_T\,(k\Omega) = 32537 \times f_{SW}\,(kHz)^{-1.045} \quad (28)$$

With a compromise between solution size and efficiency, the switching frequency of 500 kHz is chosen for this design. Thus, the calculated value of R_T = 49.2 kΩ.

2.3.3.3 Output Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the RMS current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Because the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use 式 29 to calculate the minimum value of the output inductor.

$$L_{MIN} = \frac{\left(V_{IN\_MAX} - V_O\right) \times \frac{V_O}{V_{IN\_MAX}}}{I_{RIPPLE} \times fsw} \tag{29}$$

Considering a ripple of 50%, I_{ripple} for buck can be calculated as 式 30.

$$I_{RIPPLE} = 0.5 \times \frac{P_{OUT}}{V_{OUT}} = 0.5 \times \frac{50}{24} = 1.041\,A \tag{30}$$

With this, the minimum value of inductor can be calculated as $L_{MIN} = \frac{(38-24) \times \frac{24}{38}}{1.041\,A \times 500\,kHz} = 16.99\,\mu H$.

A standard available inductor of inductance 18 µH is used for this design. The actual I_{ripple} with 18-µH inductance can be calculated with 式 29 as well: $I_{RIPPLE} = \frac{\left(V_{IN\_MAX} - V_O\right) \times \frac{V_O}{V_{IN\_MAX}}}{L_{MIN} \times fsw} = 0.982\ A$.

Because the buck converter will be working in CCM, the peak current through the inductor can be calculated as 式 31.

$$I_{PEAK} = \frac{P_{OUT}}{V_{OUT}} + \frac{I_{RIPPLE}}{2} = \frac{50}{24} + \frac{0.982}{2} = 2.575\ A \tag{31}$$

2.3.3.4 Output Capacitor Selection

The output voltage ripple is essentially composed of two parts: one is caused by the inductor current ripple going through the equivalent series resistance (ESR) of the output capacitors, and the other is caused by the inductor current ripple charging and discharging the output capacitors. For a desired V_{ripple} of 50 mV, the minimum value of C_{out} required is calculated as 式 32.

$$C_{OUT} = \frac{I_{RIPPLE}}{8 \times fsw \times V_{RIPPLE}} = \frac{0.982}{8 \times 500\,kHz \times 0.05\,V} = 4.91\,\mu F \tag{32}$$

Because for this design, the input capacitor for boost stage will work as output capacitors for buck stage, it is not necessary to put any extra capacitor there as the value of C_{in} for boost stage is much higher than the C_{out} required for buck stage.

2.3.3.5 Soft-Start Capacitor Selection

式 33 is used in order to calculate the soft-start capacitor value for a desired soft-start time of 1 ms.

$$C_{SS}(nF) = \frac{t_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)} \tag{33}$$

Where:

- C_{SS} = soft-start capacitor value
- I_{SS} = soft-start charging current (3 µA)
- t_{SS} = desired soft-start time (1 ms)

With these, the calculated soft-start capacitor value is C_{ss} = 4 nF. A 4.7-nF ceramic capacitor is used in this design.

2.3.4 CC-CV Circuit Design for Charger

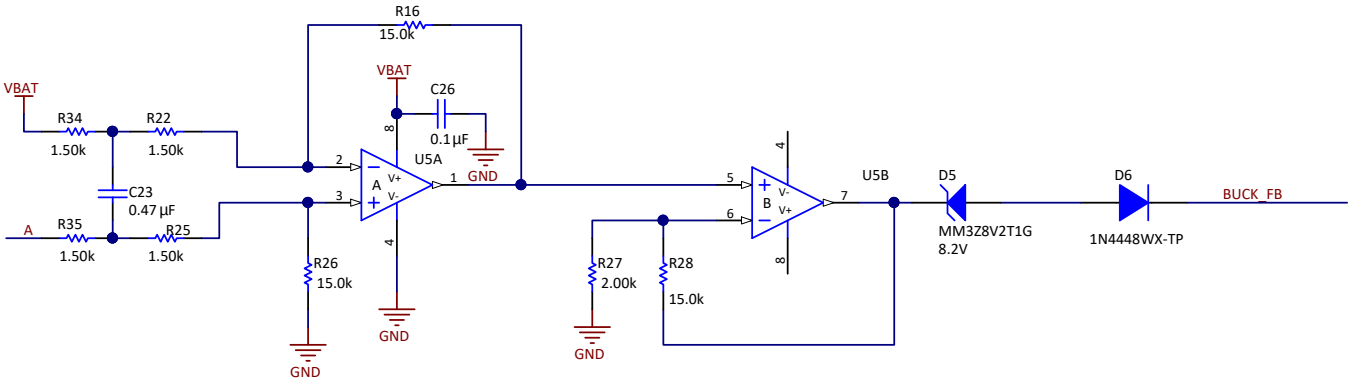


図 6. CC-CV Circuit

In order to achieve CC-CV profile for battery charging, a basic dual operational amplifier LM358 capable of single supply range up to 32 V is used. The CC-CV circuit consists of two stages: one for the differential sensing of the charging current and another as a non-inverting amplifier.

Because the buck controller has the provision only for voltage feedback loop with VFB threshold set to 0.75 V, the current loop must be interfaced parallel to the buck controller.

The output voltage of the amplifier can be calculated as 式 34.

$$V_{OUT\_AMP} = \left(1 + \frac{R28}{R27}\right) \times \left((Ich \times Rsense) \times \frac{R16}{R34 + R22}\right) \quad (34)$$

The relation between output voltage of the amplifier, break-down voltage of the zener diode and the feedback voltage is 式 35.

$$V_{OUT\_AMP} - V_Z - V_f + VFB = 0 \quad (35)$$

Where:

- Vz is the break down voltage of the zener diode
- Vf is the forward voltage drop of the D6 (approximately 1 V)
- VFB is the threshold voltage of the FB pin (0.75 V set by controller)

Thus Vout_amp for an 8.2-V zener can be calculated as $V_{OUT_{AMP}} = 8.2 + 1 - 0.75\ V = 8.45\ V$.

For the charger, the full load current, Ich = (50 W / 24 V) = 2.08 3 A

Thus, the desired value for current regulation is taken as 2.1 A.

In order to have the power dissipation in the sense resistor under control, a 0.1-Ω resistor is chosen.

For the previously mentioned values, the total gain of the amplifier stage should be

$$\left(1 + \frac{R28}{R27}\right) \times \frac{R16}{R34 + R22} = \frac{V_{OUT_{AMP}}}{(Ich \times Rsense)} = \frac{8.45\ V}{2.1\ A \times 0.1\Omega} = 40.24$$

In order to accommodate for the input offset voltage of the op amp and other irregularities, the total gain chosen for the amplifier is slightly higher than the calculated value. TIDA-01558 is designed for a gain of 5 for the differential amplifier and a gain of 8.5 for the non-inverting amplifier.

The CC set point can be changed by adjusting the gain of the amplifier accordingly.

2.3.5 Transition Logic Circuit for Buck

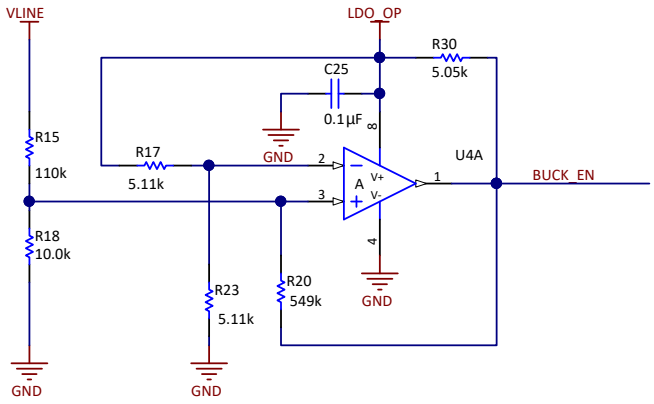


図 7. Buck Transition Circuit

For this design, the regulated output voltage for boost is 30 V. Thus, until VBUS is maintained above this voltage level, the boost stage remains disabled. A transition logic circuit for the buck stage is all that is required.

This reference desighn uses a non-inverting hysteresis comparator for enabling and disabling of buck controller where the enable threshold is VBUS ≥32 V and disable threshold of ≤31 V. The boost stage is disabled when the VBUS goes higher than the regulated output voltage of the converter. There are no chances of cross conduction of both buck and boost stage at any point of time.

When V_{buck_en} = 0 V and V_{ref} = 2.5 V, the voltage requirement at the positive pin of the comparator for the output voltage to go high is given by 式 36.

$$\frac{V_{BUS} \times (R18 \| R20)}{R15 + (R18 \| R20)} = 2.5\ V \tag{36}$$

Once the output of the comparator is pulled high, that is, 5 V, the voltage requirement at the positive pin to pull the output low is given by 式 37.

$$\frac{V_{BUS} \times (R18 \| R20)}{R15 + (R18 \| R20)} + \frac{5\ V \times (R15 \| R18)}{R20 + (R15 \| R18)} = 2.5\ V \tag{37}$$

The values chosen for the three resistors satisfying both 式 36 and 式 37 are:

- R15: 110 kΩ
- R18: 10 kΩ
- R20: 550 kΩ

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

3.1.1.1 Conditions

To test this reference design, two power supplies are used: one emulating the 24-V battery and the other emulating the 30-V to 38-V bus. Electronic loads are used for applying load.

3.1.1.2 Equipment

1. Two DC power supplies, each capable of supplying up to 30-A current
2. Digital oscilloscope
3. At least two multimeters with greater than four-and-a-half digit accuracy for measuring efficiency
4. Precision current shunt resistors for measuring current
5. Electronic loads or resistive loads

3.2 Testing and Results

3.2.1 Test Setup

図 8 shows the setup recommendations for testing the reference design. The setup does not show the connections to the multimeters for measuring various voltages and currents. These can be connected by the user accordingly for testing efficiency.

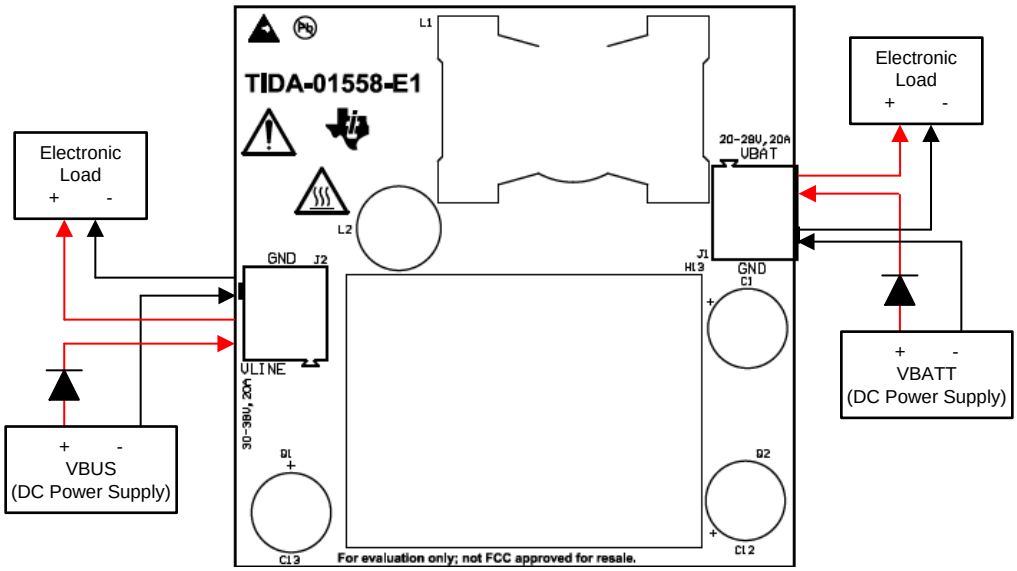


図 8. Recommended Test Setup for Testing TIDA-01558

The procedure to test TIDA-01558 is as follows:

1. Connect the set of wires from the power supplies to the board and from the board to the load as shown in 図 8. Do not forget to connect the diodes as shown 図 8.
2. Set the buck power supply between 32 V and 38 V with a current limit of 100 mA.
3. Set the boost power supply between 20 V and 28 V with a current limit of 100 mA.

4. Set the electronic loads in resistive mode. Resistor banks can also be used as load.
5. Connect a DC fan and position it so that the board is perpendicular to the fan and the airflow passes through the heat-sink fins.
6. Any of the DC power supplies can be turned on first. If the input power supply (V_{BATT}) to boost is turned on, the output line voltage gets regulated to 30 V. If the buck power supply(V_{BUS}) is turned on, the output battery voltage gets regulated to 24 V.
7. Increase the current limit of the power supplies: 26 A for the boost mode power supply and 2.5 A for the buck mode power supply.
8. The boost stage (backup power supply mode) can be loaded up to 300 W without any airflow and up to 500 W with 500 LFM to 550 LFM airflow, and the buck stage (charger mode) can be loaded up to 50 W without any airflow.
9. The buck stage (charger) has the CC point set to 2.1 A. Until the load is less than 2.1 A, the converter works in CV mode, and once the load crosses 2.1 A, the converter will work in CC mode until the output voltage drops to 11 V.
10. If the V_{BUS} supply is switched on first with voltage set >32 V, the system works as a charger. The 500-W load will also be supplied by V_{BUS} directly.
11. Reduce the V_{BUS} voltage below 30 V while the V_{BATT} is switched on and set anywhere between 20 V to 28V. When V_{BUS} reaches 30 V, the transition from charger mode to backup power supply mode will happen. Increase back the V_{BUS} voltage slowly. When V_{BUS} goes higher than 30 V, the boost stage (backup power supply) stops working. When V_{BUS} goes higher than 32 V, the charger is enabled.
12. The necessary functional performance characteristics can be measured for both buck and boost now.

3.2.2 Test Results

The test results are divided into multiple sections that cover the stead state performance, efficiency data, functional waveforms, and thermal performance.

3.2.2.1 Performance Data

3.2.2.1.1 Efficiency, Load and Line Regulation in Discharge (Boost) Mode

This test is conducted when the system is operating as a backup power supply. The system transfers power from the 24-V battery pack to the 30-V bus. The steady state performance and efficiency results are captured for different battery voltage and load conditions.

表 2. Test Results in Boost Mode at 28-V Battery Voltage

VBAT (V)	IBAT (A)	PIN (W)	VBUS (V)	IBUS (A)	POUT (W)	EFF
28	2.223928815	62.27000682	30.28	2	60.56	97.25%
28	3.87355414	108.4595159	30.28	3.514	106.40392	98.10%
28	5.473480979	153.2574674	30.28	4.986	150.97608	98.51%
28	7.633533634	213.7389418	30.28	6.961	210.77908	98.62%
28	9.261610499	259.325094	30.29	8.445	255.79905	98.64%
28	10.84054247	303.5351891	30.29	9.877	299.17433	98.56%
28	12.99668608	363.9072104	30.29	11.822	358.08838	98.40%
28	14.56764893	407.89417	30.29	13.232	400.79728	98.26%
28	16.17576616	452.9214524	30.28	14.677	444.41956	98.12%
28	18.07301512	506.0444234	30.28	16.369	495.65332	97.95%

表 3. Test Results in Boost Mode at 24-V Battery Voltage

VBAT (V)	IBAT (A)	PIN (W)	VBUS (V)	IBUS (A)	POUT (W)	EFF
23.94	2.597861679	62.19280859	30.27	1.995	60.38865	97.10%
23.94	4.53506166	108.5693761	30.28	3.513	106.37364	97.98%
23.94	6.43616882	154.0818816	30.28	4.995	151.2486	98.16%
23.94	8.964616772	214.6129255	30.28	6.967	210.96076	98.30%
23.94	10.88483832	260.5830294	30.28	8.455	256.0174	98.25%
23.94	12.74688894	305.1605213	30.28	9.888	299.40864	98.12%
23.94	15.29258221	366.1044181	30.28	11.836	358.39408	97.89%
23.94	17.14463562	410.4425768	30.28	13.253	401.30084	97.77%
23.94	19.07315368	456.6112991	30.28	14.693	444.90404	97.44%
23.94	21.310805	510.1806717	30.28	16.382	496.04696	97.23%

表 4. Test Results in Boost Mode at 20-V Battery Voltage

VBAT (V)	IBAT (A)	PIN (W)	VBUS (V)	IBUS (A)	POUT (W)	EFF
20	3.10444769	62.0889538	30.27	1.995	60.38865	97.26%
20	5.458656948	109.173139	30.27	3.513	106.33851	97.40%
20	7.74021106	154.8042212	30.27	4.995	151.19865	97.67%
20	10.78970177	215.7940355	30.27	6.966	210.86082	97.71%
20	13.10956225	262.191245	30.27	8.445	255.63015	97.50%
20	15.36515429	307.3030858	30.27	9.887	299.27949	97.39%
20	18.44504519	368.9009039	30.27	11.829	358.06383	97.06%
20	20.74908255	414.981651	30.27	13.258	401.31966	96.71%
20	23.0350013	460.700026	30.27	14.684	444.48468	96.48%
20	25.83927538	516.7855077	30.27	16.375	495.67125	95.91%

3.2.2.1.2 Efficiency in Charge (Buck) Mode

This test is conducted when the system is operating as charger (buck mode). The system charges 24-V battery pack from a 32 V to 38 V VBUS. The steady state performance and efficiency results are captured for different VBUS voltage and load conditions.

表 5. Test Results in Buck Mode at 38-V Bus Voltage

VBUS (V)	IBUS (A)	PIN (W)	VBAT (V)	IBAT (A)	POUT (W)	EFF
37.99	0.15	5.6985	24.14	0.2154	5.199756	91.248%
37.98	0.292	11.09016	24.13	0.4258	10.274554	92.646%
37.98	0.429	16.29342	24.12	0.6363	15.347556	94.195%
37.97	0.567	21.52899	24.12	0.847	20.42964	94.894%
37.96	0.699	26.53404	24.12	1.0473	25.260876	95.202%
37.95	0.838	31.8021	24.12	1.258	30.34296	95.412%
37.95	0.978	37.1151	24.12	1.4682	35.412984	95.414%
37.94	1.119	42.45486	24.12	1.6788	40.492656	95.378%
37.93	1.253	47.52629	24.12	1.8792	45.326304	95.371%
37.92	1.381	52.36752	24.11	2.0698	49.902878	95.294%

表 6. Test Results in Buck Mode at 32-V Bus Voltage

VBUS (V)	IBUS (A)	PIN (W)	VBAT (V)	IBAT (A)	POUT (W)	EFF
31.99	0.179	5.72621	24.13	0.2157	5.204841	90.895%
31.99	0.343	10.97257	24.14	0.4266	10.298124	93.853%
31.98	0.506	16.18188	24.14	0.6375	15.38925	95.102%
31.97	0.669	21.38793	24.14	0.8481	20.473134	95.723%
31.96	0.825	26.367	24.13	1.0483	25.295479	95.936%
31.95	0.99	31.6305	24.14	1.2588	30.387432	96.070%
31.94	1.157	36.95458	24.14	1.4696	35.476144	95.999%
31.93	1.316	42.01988	24.14	1.6697	40.306558	95.923%
31.92	1.483	47.33736	24.14	1.88	45.3832	95.872%
31.91	1.641	52.36431	24.12	2.077	50.09724	95.671%

3.2.2.1.3 Charger CC-CV Profile

表 7 and 表 8 summarize the efficiency reading of the charger in CC mode at different input voltages:

表 7. Charger Efficiency in CC Mode at 38 VBUS

VBUS (V)	IBUS (A)	PIN (W)	VBAT (V)	IBAT (A)	POUT (W)	EFF
37.92	1.381	52.36752	24.11	2.0698	49.902878	95.294%
37.92	1.405	53.2776	23.99	2.1135	50.702865	95.167%
37.92	1.392	52.78464	23.51	2.1367	50.233817	95.167%
37.93	1.372	52.03996	23.02	2.146	49.40092	94.929%
37.93	1.324	50.21932	22.01	2.159	47.51959	94.624%
37.93	1.209	45.85737	20.01	2.1687	43.395687	94.632%
37.94	1.105	41.9237	18.01	2.1756	39.182556	93.462%
37.95	0.995	37.76025	16.01	2.1867	35.009067	92.714%
37.95	0.883	33.50985	14.01	2.1948	30.749148	91.762%
37.96	0.77	29.2292	12.02	2.2021	26.469242	90.558%
37.96	0.688	26.11648	10.61	2.2016	23.358976	89.442%

表 8. Charger Efficiency in CC Mode at 32 VBUS

VBUS (V)	IBUS (A)	PIN (W)	VBAT (V)	IBAT (A)	POUT (W)	EFF
31.91	1.641	52.36431	24.12	2.077	50.09724	95.671%
31.91	1.67	53.2897	23.95	2.128	50.9656	95.639%
31.91	1.636	52.20476	23.45	2.131	49.97195	95.723%
31.91	1.618	51.63038	23.02	2.1444	49.364088	95.611%
31.92	1.569	50.08248	22.06	2.146	47.34076	94.526%
31.92	1.43	45.6456	20.06	2.155	43.2293	94.706%
31.93	1.31	41.8283	18.06	2.1814	39.396084	94.185%
31.94	1.176	37.56144	16.06	2.1893	35.160158	93.607%
31.95	1.046	33.4197	14.06	2.1977	30.899662	92.459%
31.95	0.91	29.0745	12.07	2.2044	26.607108	91.514%
31.96	0.811	25.91956	10.57	2.22	23.4654	90.532%

3.2.2.2 Performance Curves

3.2.2.2.1 Boost (Discharge) Mode Efficiency

The boost mode or discharge mode efficiency varies as a function of load and battery voltage. 図 9 shows the efficiency plotted for three different battery voltages.

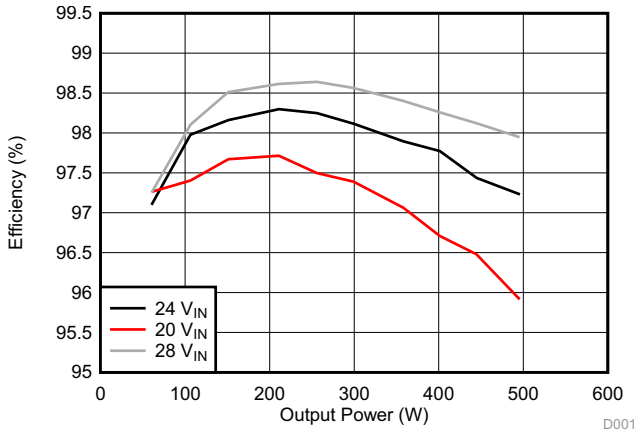


図 9. Boost Efficiency vs Output Load in Backup Power Supply Mode

3.2.2.2.2 Buck (Charge) Mode Efficiency

図 10 shows the efficiency of buck or charger stage at various VBUS voltage levels as a function of load.

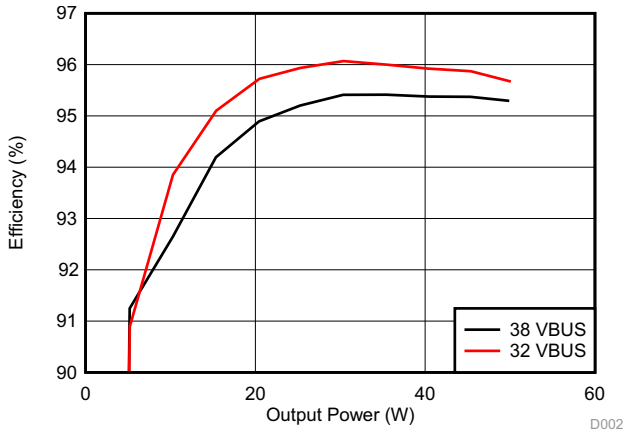


図 10. Buck Efficiency vs Output Load in Battery Charging Mode

3.2.2.2.3 CC-CV Performance of Charger

図 11 shows the CC-CV characteristics of the charger where the output current is limited at 2.1A

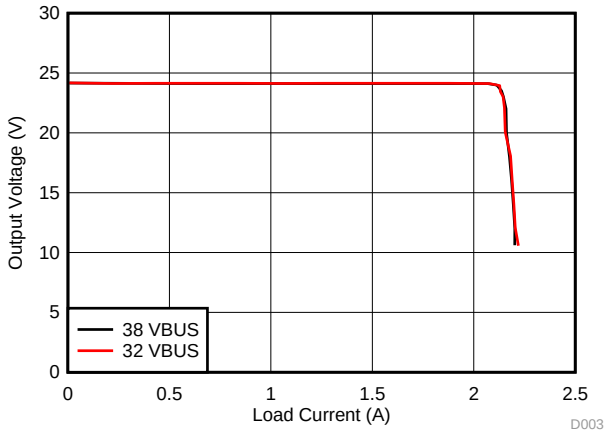


図 11. CC-CV Characteristic of Charger

図 12 shows the efficiency of the charger in CC mode.

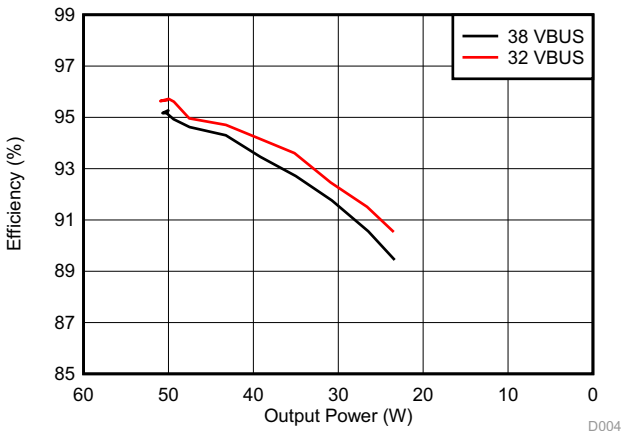


図 12. Efficiency of Charger in CC Mode

3.2.2.3 Functional Waveforms

3.2.2.3.1 Boost Stage Switching Waveforms

図 13 shows the switching waveform of the boost stage with V_{GS} of both low-side and high-side FET, switch node waveform, and inductor current. 図 14 and 図 15 show the turnon and turnoff waveform of the low-side FET of the boost stage. These waveforms were captured at 24-V battery voltage input and full output load.

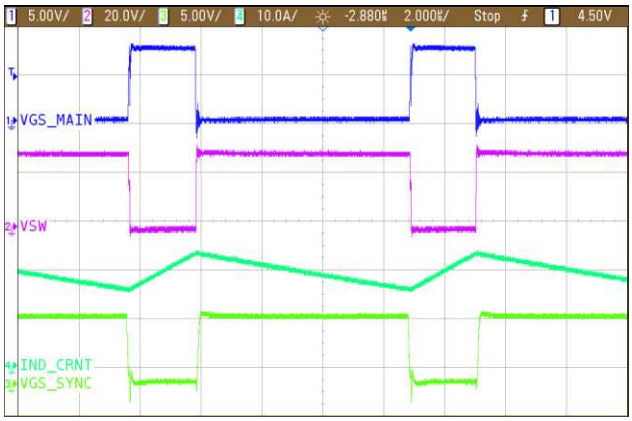


図 13. Switching Waveform of Boost Stage

図 14. Turn on of Low-side FET

図 15. Turn off of Low-Side FET

Due to the usage of TO-220 package FET, the high-side FET's diode reverse recovery effect on the switch node waveform and V_{GS} waveform of low-side FET can be seen.

3.2.2.3.2 Buck Stage Switching Waveforms

図 16 shows the switch node waveform and inductor current waveform of the buck stage. 図 17 and 図 18 show the zoomed in turnon and turnoff waveform of the buck converter respectively. The waveforms are captured at 34 VBUS input and 50-W output load.

図 16. Buck Stage Switching Waveform

図 17. Zoomed-in Turnon Waveform

図 18. Zoomed-in Turnoff Waveform

3.2.2.3.3 Ripple Voltage

図 19 shows the output ripple voltage of the boost stage. The actual ripple voltage is around 300-mV peak to peak. The high-frequency LC oscillations in the waveform can be avoided with a small LC filter at the output.

図 19. Boost Converter Output Ripple

図 20 shows the output ripple voltage of the buck stage. The peak-to-peak ripple voltage is around 300 mV.

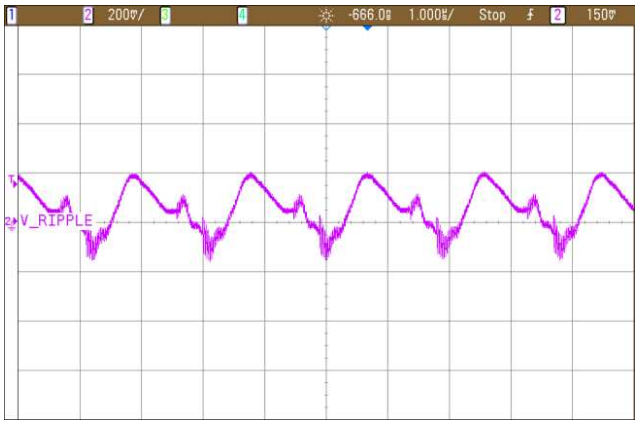


図 20. Buck Converter Output Ripple

3.2.2.3.4 Transition Waveform

For this design, the transition from charging mode to back-up power supply mode is measured with the 240-µF bulk capacitor. 図 21 shows the time from when the boost stage (back-up power supply) is enabled and when the controller starts switching. This time, as measured, is around 240 µs. 図 22 shows the response time of the control loop where the time between the start of switching and voltage coming back to regulated output is shown. This waveform is captured when VBUS changes from 34 V to 0 V, and the load to the system is 500 W. During the transition, the maximum voltage drop at VBUS is around 900 mV. Thus the load connected to the system must be capable of running at an input voltage of around 29 V.

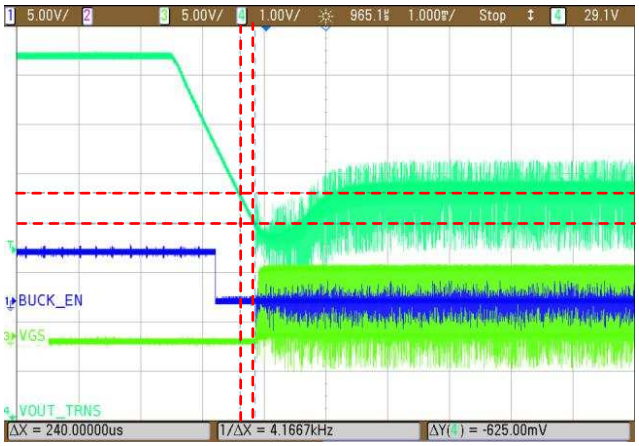


図 21. Transition Time Between Boost Enable and Start of Switching

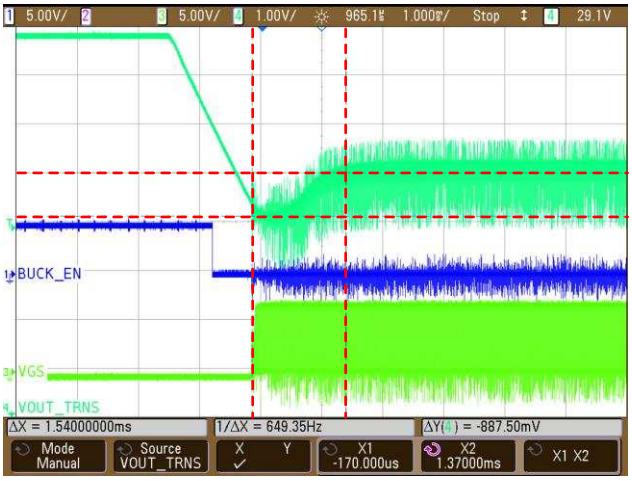


図 22. Response Time of Control Loop

3.2.2.3.5 Boost Stage Load Transient

図 23 shows the load transient response of the boost stage with load varying from 10% to 100% at 24 Vin.

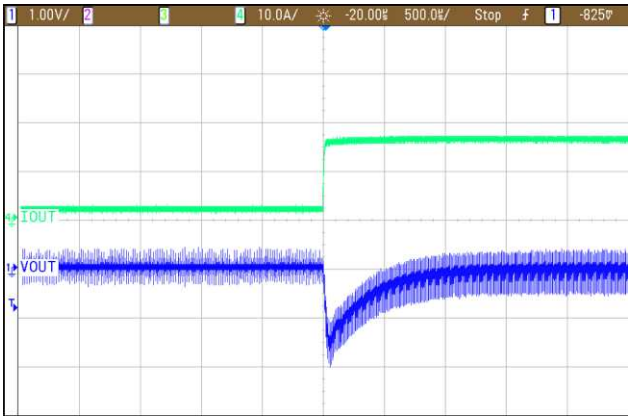


図 23. Load Transient Waveform of Boost Stage

3.2.2.3.6 Thermal Data

This design can be loaded up to 500 W as back-up power supply and 50W as charger. The continuous power rating is 300 W without any forced cooling and 500 W with 400 LFM to 600 LFM fan. 表 9 and 図 24 give the output load capability of the power stage with time as the temperature on the board reaches 80°C with no forced cooling.

表 9. Load Capability of Design Without Forced Cooling

OUTPUT POWER (W)	TIME TO REACH 80°C (minutes) WITH NO FORCED COOLING
500	1.5
450	2.5
400	3.67
350	6
300	15.5

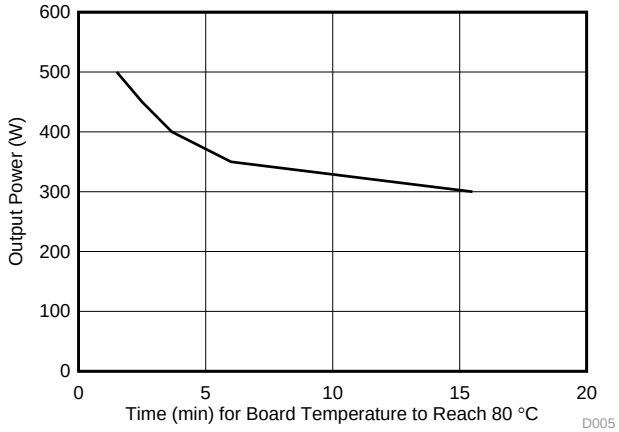


図 24. Load Capability of Design Without Forced Cooling

図 25 and 図 26 show the thermal images of the top side and bottom side respectively with the system loaded for 500 W for 15 minutes, 24-V input, and about 500 LFM to 550 LFM airflow.

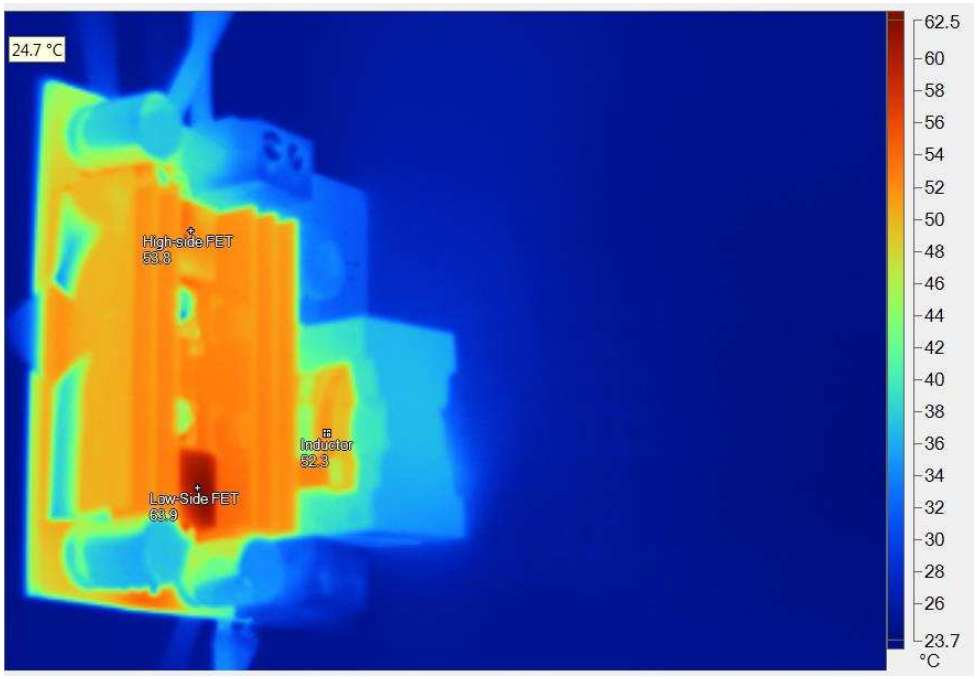


図 25. Top Side Thermal Image

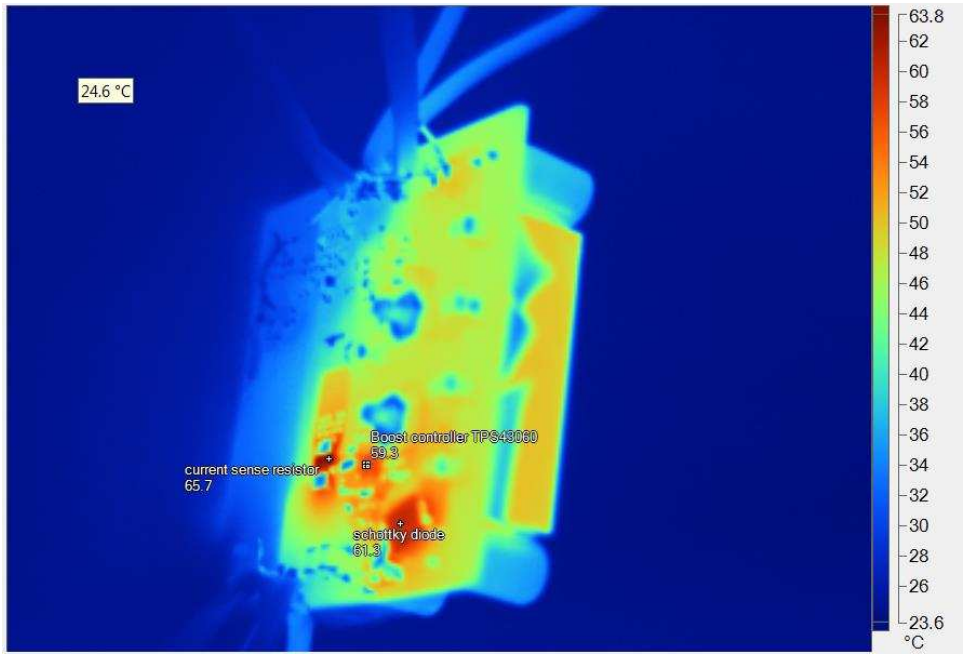


図 26. Bottom Side Thermal Image

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01558.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01558.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01558.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01558.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01558.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01558.

5 Software Files

To download the software files, see the design files at TIDA-01558.

6 Related Documentation

1. Texas Instruments, *LMR14020 SIMPLE SWITCHER® 40 V 2 A, 2.2 MHz Step-Down Converter with 40 μA I_Q Data Sheet*
2. Texas Instruments, *CSD18532KCS 60-V N-Channel NexFET™ Power MOSFET Data Sheet*
3. Texas Instruments, *TPS4306x Low Quiescent Current Synchronous Boost DC-DC Controller With Wide V_{IN} Range Data Sheet*

6.1 商標

7 About the Author

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