参考資料

TI Designs: TIDA-01504
高精度、ループ駆動、4～20mA、HARTモデム搭載のフィールド・トランスミッタのリファレンス・デザイン

概要

このリファレンス・デザインは、ループ駆動でHARTモデムを搭載した高精度フィールド(センサ)トランスミッタ用のソリューションです。このデザインは、部分的に独立した4～20mA電流トランスミッタ、HARTモデム、マイクロコントローラ、および電力コンディショニング・ブロックを使用し、SMARTフィールド・トランスミッタのデザインを実現します。このデザインはHART FSK物理層の要件に準拠しており、FieldComm Group™に登録されています。

リソース

TIDA-01504	デザイン・フォルダ
DAC8740H	プロダクト・フォルダ
DAC8830	プロダクト・フォルダ
OPA335	プロダクト・フォルダ
OPA333	プロダクト・フォルダ
MSP430FR5969	プロダクト・フォルダ
TPS7A4101	プロダクト・フォルダ
TPS7B69-Q1	プロダクト・フォルダ
LM4132	プロダクト・フォルダ

TI E2E™ Community

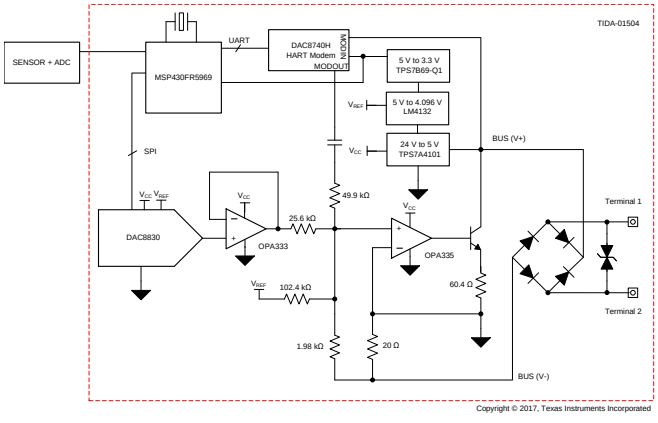
E2E™エキスパートに質問

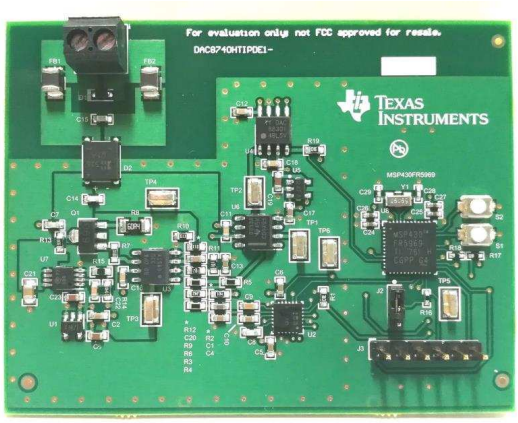
特長

- DAC8740H HARTモデムとオンボードの電力コンディショニング・ブロックによるループ駆動、4～20mAの電流トランスミッタ
- 室温で0.1%未満のFSR合計未調整誤差
- 逆極性保護機能付きの外部保護回路
- HART FSK物理層の要件に準拠した、登録済みHARTデバイス

アプリケーション

- ファクトリ・オートメーションとプロセス制御
- 流量トランスミッタ
- レベル・トランスミッタ
- 圧力トランスミッタ
- 温度トランスミッタ





1 System Description

This reference design provides a complete SMART field transmitter, essentially creating a HART enabled, loop-powered, highly accurate, 4- to 20-mA field transmitter, along with the microcontroller (MCU). The design includes several circuit elements in creating a modular design that can support many two-wire current loop applications. This design accepts a wide input loop supply voltage range from 14 V to 36 V, while regulating the loop current with a total unadjusted error accuracy of less than 0.1% full-scale range (FSR) of total error at room temperature. The design also demonstrates a total system power budget less than 2.6 mA, which is well below the NAMUR NE43 standard of 3.5 mA.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input voltage	14-V to 36-V DC
Outputs	4 mA to 20 mA DC current, HART FSK data
Total unadjusted error (TUE)	<0.1% FSR
HART signal amplitude	400 mVpp to 600 mVpp
HART FSK rise and fall time	75 μs to 200 μs while transmitting a mark symbol, 75 μs to 100 μs while transmitting a space symbol
HART FSK frequencies	1200 Hz ±1% while transmitting a mark symbol, 2200 Hz ±1% while transmitting a space symbol
Output noise during silence	< 2.2 mV RMS within the extended frequency band with no active HART FSK
System input impedance	< 5000 pF equivalent capacitance, > 100 kΩ equivalent resistance
HART FSK compliance	Registered as compliant with FieldComm Group
Operating temperature range	–40°C to +85°C
Debug communication port	Spy-Bi-Wire (two-wire JTAG)

2 System Overview

2.1 Block Diagram

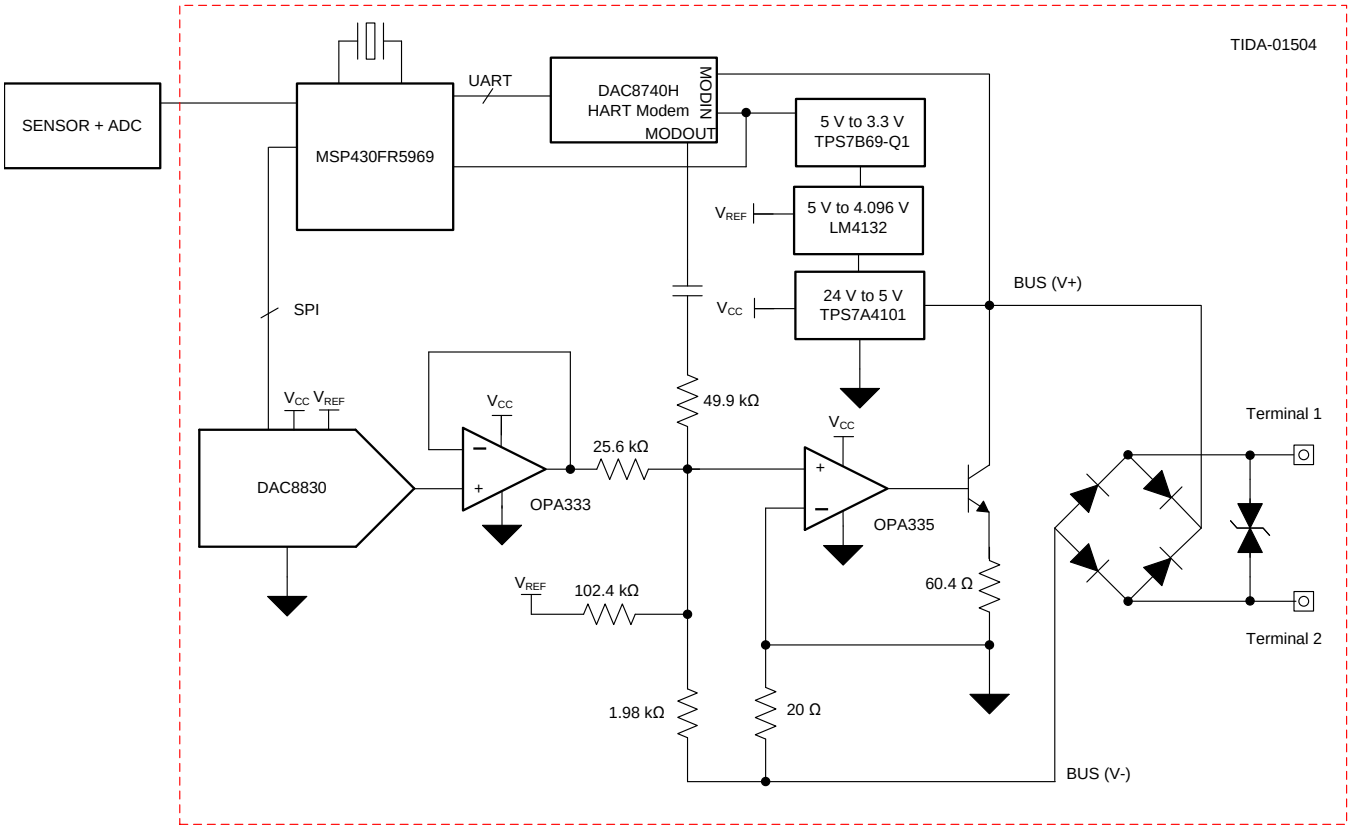


図 1. Detailed Circuit Diagram of TIDA-01504

2.2 Highlighted Products

2.2.1 HART Modem—DAC8740H

The Highway Addressable Remote Transducer (HART) FSK is generated by the DAC8740H device, which is a HART-compliant physical layer modem. The device has an operational supply voltage range of 2.7 V to 5.5 V while consuming only 265 µA when using an internal reference or oscillator, making it an excellent choice for loop-powered or two-wire applications. Additionally, the device operates from –55°C to +125°C and is available in a small 24-pin (4-mm × 4-mm) VQFN package.

2.2.2 DAC8830

The high accuracy of the 4- to 20-mA span is realized by the DAC8830 device, which is a single-channel, 16-bit, serial-input, voltage-output digital-to-analog converter (DAC) operating from a single 3-V to 5-V power supply. The excellent linearity (1 LSB INL), low noise and glitch, and fast settling make the DAC an ideal candidate when designing industrial applications that require high levels of measurement accuracy.

2.2.3 OPA335

The primary operational amplifier (OPA) error sources that may impact the transmitter's accuracy include input offset voltage and input bias current. The gain of the discrete (Voltage-to-Current) V/I circuit amplifies this error source and translates it as an offset current value. This error source is addressed with the OPA335 CMOS OPA. This OPA uses auto-zeroing techniques to simultaneously provide very low offset voltage (5 µV max), and near-zero drift over time and temperature. Additionally, this OPA is optimized for low-voltage, single-supply operation and consume only a typical value of 285 µA of quiescent current during operation.

The large bandwidth of the device, a 2-MHz gain bandwidth product, also ensures that the loop is well regulated in the event of HART communication or any programmed current changes.

2.2.4 OPA333

The output impedance of the DAC8830 and input of the V/I circuit is separated with the buffered configuration of the OPA333 device. The high-impedance input of the OPA successfully buffers the output of the DAC creating a low-impedance voltage output that drives the input of the V/I circuit. As with the OPA335 device, the biggest error source associated with the OPA333 is the offset voltage. The OPA333 uses a proprietary auto-calibration technique to simultaneously provide very low offset voltage (10 µV max) and near-zero drift over time and temperature. Furthermore, this OPA also accepts single-supply operation and only exhibits a typical value of 17 µA of quiescent current during operation.

2.2.5 MSP430FR5969

The intelligence of the transmitter comes directly from the MSP430FR5969 device. The MSP430™ ultra-low-power (ULP) FRAM platform combines a uniquely embedded FRAM and a holistic ultra-low-power system architecture, allowing innovators to increase performance at lowered energy budgets. FRAM technology combines the speed, flexibility, and endurance of SRAM with the stability and reliability of flash at much lower power.

The MSP430 ULP FRAM portfolio consists of a diverse set of devices featuring FRAM, the ULP 16-bit MSP430 CPU, and intelligent peripherals targeted for various applications. The ULP architecture showcases seven low-power modes, optimized to achieve extended battery life in energy-challenged applications.

2.2.6 TPS7A4101

The TPS7A4101 device is a very high voltage-tolerant linear regulator that offers the benefits of a thermally enhanced package (MSOP-8), and is able to withstand continuous DC or transient input of up to 50 V. In this reference design, the TPS7A4101 converts the loop supply applied across the field transmitter and lowers this voltage to a 5-V output that is used by various active components and other regulators such as the OPA333, OPA335, DAC8830, TPS76933, and so on.

2.2.7 TPS7B69-Q1

The TPS7B69-Q1 device is a low-dropout linear (LDO) regulator designed for up to 40-V VI operations. With only a 15-µA (typical) quiescent current at light load, the device is suitable for standby microcontroller unit systems. This LDO provides 3.3 V of power for the DAC8740H and MSP430FR5969 devices.

2.2.8 LM4132

The LM4132 family of precision voltage references performs comparable to the best laser-trimmed bipolar references, but in cost-effective CMOS technology. Unlike other LDO references, the LM4132 can deliver up to 20 mA and does not require an output capacitor or buffer amplifier. These advantages along with the SOT-23 packaging are important for space-critical applications. The precision reference provides a stable 4.096 V to the VREF pin of the DAC8830 device.

2.3 System Design Theory

2.3.1 Brief Overview of Transmitters

Field instruments such as sensor transmitters are typically located out in a field or factory floor and are responsible for monitoring process control variables. These variables can include temperature, pressure, flow rates, level measurements, and axis motion. Often described as transducers, sensor transmitters convert the sensor output to a standardized transmitted analog value, which typically ranges from 4 mA to 20 mA in industrial applications. The entire span of the analog signal is essentially a function of the measured process variable. Transducers that provide only the analog representation of the measured process value are described as simple transmitters because they do not provide any other means of communicating other sensor-related information through the current loop.

Evolving the simple transmitter hardware to include a HART modem, which provides the capability of superimposing a FSK signal onto the analog waveform, enables the transducer to become a single modular auto-ranging remote transducer (SMART). The transmitter's HART modem and MCU, provide a way of communicating digital data through the analog current-loop enabling the transmitter to communicate vital sensor information such as diagnostic data, invoking calibration routines, or changing sensor configurations.

Transmitters are generally biased with an external power supply in series with a typical 250-Ω load. These elements, power supply, and load are generally included in another module—the analog input module—which is typically coupled with an analog-front-end, including the ADC, MCU, and optional HART for intelligent current loops. The ADC records the resulting potential developed across the load resistor and reports this process value to the MCU for data processing and action, as shown in 図 2. An addition of a HART modem turns the two-wire loop into an intelligent loop, as the master is able to query for health, calibration, and status of the connected sensor transmitter.

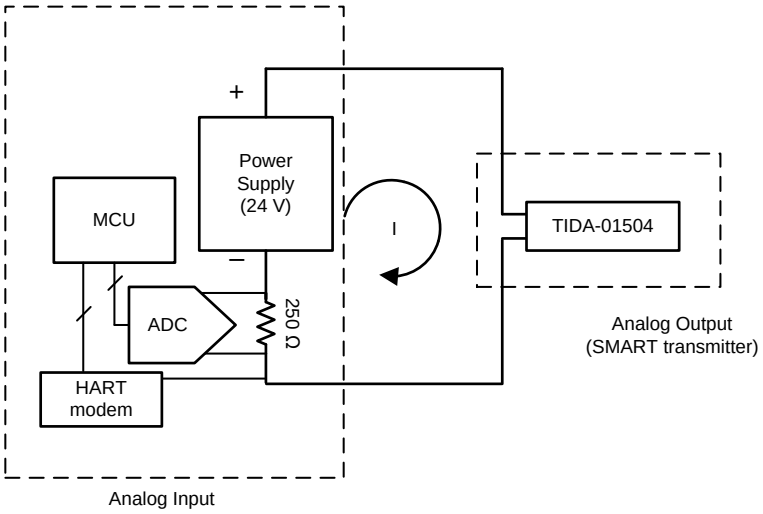


図 2. Example of Two-Wire Current Loop

図 3 shows a simplified schematic of the 4- to 20-mA two-wire transmitter, which is often referred to as a V-I converter. The designed transmitter has two external input terminals of no fixed polarity; a positive or negative lead can connect to either terminal. This reverse polarity protection is accomplished through diode-bridge rectification. The positive lead provides the supply voltage that the transmitter requires for power-up and operation, while the negative lead provides the path for return current.

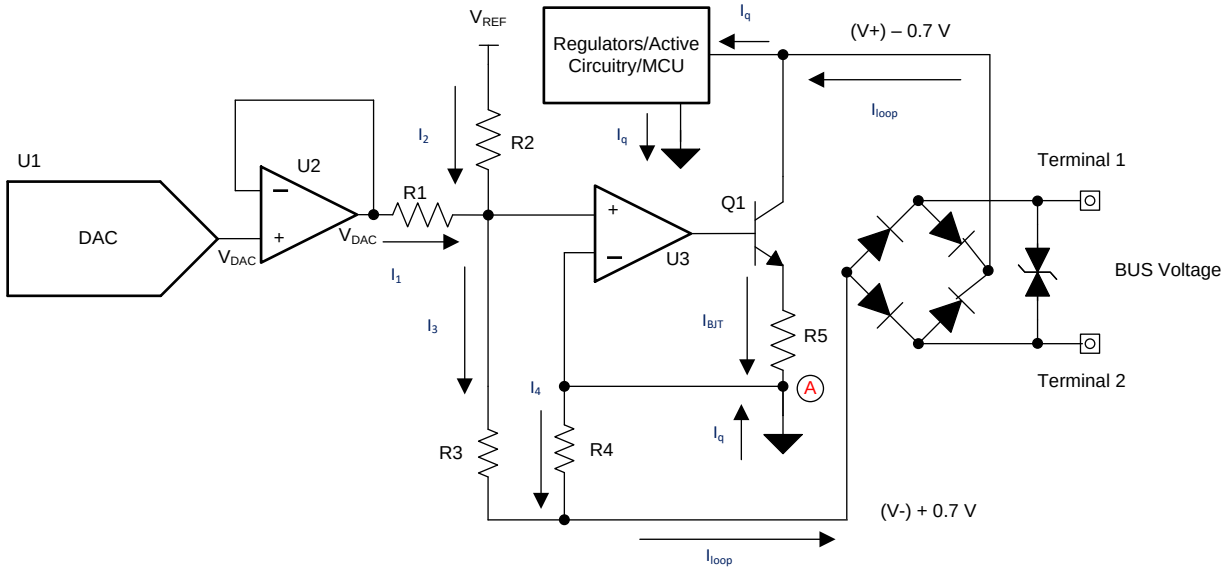


図 3. Simplified V/I Converter Circuit

Replacing all components with their ideal counterparts such as ideal OPAs reveal a starting point when deriving the simplified transfer function. Through the properties of an ideal OPA, both input terminals of U3 have the same potential. In this reference design, the negative input terminal is driven to local ground. Ideally, no input bias current flows into the input terminals of U3; therefore, the current through R2 and R1 must be equivalent to the current through R3, shown as I3. This KCL equation is shown in 式 1.

$$I_3 = \frac{V_{REF}}{R_3} + \frac{V_{DAC}}{R_1} \quad (1)$$

An important concept to iterate is the return path of quiescent current in the current loop. The bus voltage supplies the LDO that provides power to the analog sections of the transmitter. These sections are responsible for programming the current level and maintaining local ground. The quiescent current, Iq, of all active components eventually returns from node A, which combines with the current through R5 and returns to BUS voltage (V-) through resistor R4. Negative feedback of U3 ensures that the two input terminals of the OPA are driven to the same voltage by biasing the base of the Q1 NPN BJT. The BJT conducts current through R5, matching the voltages across R3 and R4, producing 式 2.

$$I_3 \times R_3 = I_4 \times R_4$$

$$\therefore I_4 = \frac{I_3 \times R_3}{R_4} \quad (2)$$

The currents, I3 and I4, then combine to form the output loop current, which is shown in 式 3.

$$I_{LOOP} = I_3 + I_4 = I_3 + \frac{I_3 \times R_3}{R_4} = I_3 \times \left(1 + \frac{R_3}{R_4}\right)$$
$$= \left(\frac{V_{REF}}{R_2} + \frac{V_{DAC}}{R_1}\right) \times \left(1 + \frac{R_3}{R_4}\right) \quad (3)$$

This output current can also be expressed as a function of DAC input code, as shown in 式 4.

$$I_{LOOP} = \left(\frac{V_{REF}}{R_2} + \frac{V_{REF} \times Code}{R_1 \times 2^N} \right) \times \left(1 + \frac{R_3}{R_4} \right) \quad (4)$$

From 式 4, the gain is directly proportional to R3/R4. To design for minimal power dissipation among active components (DAC, LDO, reference, and so on), the R3 and R4 resistors must be chosen such that a majority of the loop current flows through the BJT. In this reference design, the R3/R4 gain is chosen as 99.

For a V_{REF} value of 4.096 V, the zero-scale portion of the transfer function, [VREF / (102.4k)] × (100), translates to 4 mA, while the span, [V_{DAC} / (25.6k)] × 100, encompasses 16 mA. This final design is a system capable of sourcing 4 to 20 mA, which is dependent on DAC output voltage.

2.3.2 Loop Voltage Regulator

With two-wire transmitters, the most common loop supply voltage is 24-V DC; however, supply voltages can range from 12 V to 36 V. During full-scale operation, the transmitter is sourcing 20 mA through the load resistor, which creates a potential drop that is equivalent to this resistor value multiplied by the full-scale current, 20 mA. Therefore, it is important to remember that this voltage sets the maximum BUS voltage that the transmitter requires for proper operation.

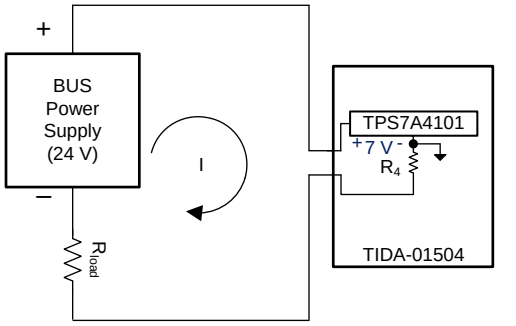


図 4. TPS7A4101 Minimum Voltage

The TPS7A4101 requires a minimum input voltage of 7 V for proper operation. Because the transmitter creates its own local ground, the voltage drop across resistor R4 must be calculated in determining the delta from local ground to BUS (V-). Assuming that all the full-scale current is conducted through the BJT, this resistance experiences a voltage drop that is equivalent to the full-scale current multiplied by the resistance, which in this reference design produces 0.4 V (20 Ω × 20 mA). This delta is added to the 7-V input voltage in creating the minimum transmitter voltage of 7.4 V. The two forward-biased diodes in the bridge rectifier circuit must also be taken into account, as each diode adds 0.7 V to the previous estimate. Therefore, in this reference design, a minimum transmitter voltage of 8.8 V (potential drop across transmitter terminals) is required to successfully power the TPS7A4101 device.

Using this voltage, along with the known load resistor value, the necessary loop voltage can be calculated as:

$$\begin{aligned} \text{BUS voltage} &= 7.4\ \text{V} + 2 \times 0.7\ \text{V} + \left(R_{load} \times \text{full-scale current} \right) \\ &= 8.8\ \text{V} + \left(R_{load} \times 20\ \text{mA} \right) \end{aligned} \quad (5)$$

A 250-Ω load results in a necessary minimum BUS voltage of 13.8 V for proper operation.

In this reference design, the TPS7A4101 converts the external supply to a 5-V rail that is used by the DAC8830, LM4132, and OPA333 or OPA335. The 200-Ω resistor that separates the loop supply from the LDO acts as a current limiting resistor at startup and additionally improves the overall receiver impedance of the design.

2.3.3 Q1 Compliance Voltage

During normal operation, the Q1 transistor operates in the forward-active region and regulates loop current through negative feedback by U3. To remain in this mode, the voltage drop across the collector-emitter must be greater than the drop across the base-emitter. Increasing resistance at the BJT's emitter can cut into the headroom of the BJT. Therefore, consider when choosing values for R4 and R5. The compliance voltage of this circuit is mostly dependent on creating a stable V_{CE} for forward-active operation. To clarify this concept, the BJT regulation branch of the transmitter has been simplified to the one shown in 図 5.

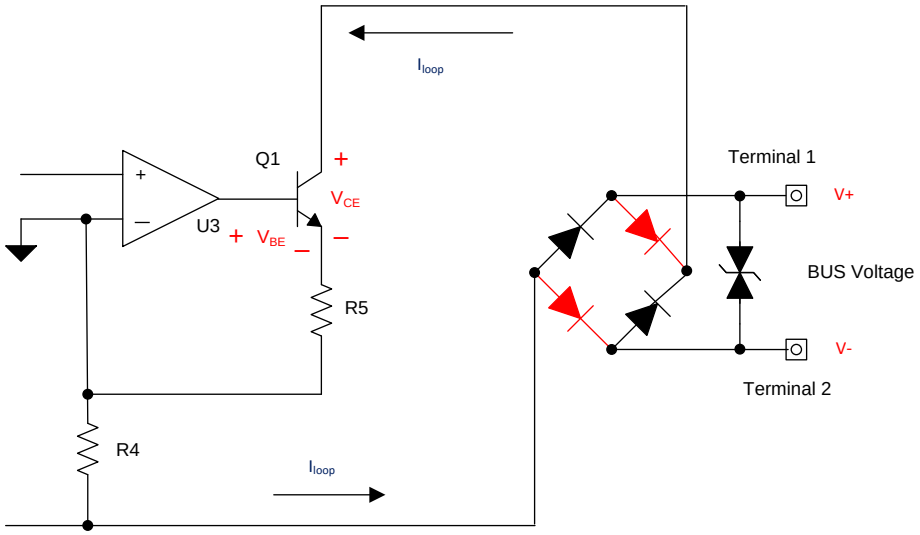


図 5. Q1 BJT Regulation Branch

In this reference design, the U3 is a rail-to-rail amplifier, which produces a possible maximum base voltage of 5 V, with respect to local ground. Using this constraint can show that the emitter resistor, R5, must have a value less than [(5 – 0.7 / 20 mA] Ω to maintain 0.7 V V_{BE} during maximum regulation.

In addition to this, the loop supply must be capable of maintaining a forward-active V_{CE} potential while providing all necessary voltages across the resistor path during full-scale regulation. This relationship is expressed in 式 6.

$$\text{BUS voltage} = V_{CE} + \left(R_4 + R_5 + R_{load}\right) \times 20\ \text{mA} + 2 \times 0.7\ \text{V} \quad (6)$$

In this design, the R4 and R5 resistor values are chosen for minimal potential drop while fixed for an R3/R4 gain of 99. Using a V_{CE} value of 2 V and the values specified in the schematic results in a required BUS supply of 10.008 V. Notice that this voltage is significantly lower than the BUS voltage required to correctly bias the TPS7A4101 for a 5-V operation. The chosen passive values ensure that the BUS supply is only limited by the input voltage required to operate the TPS7A4101 device as opposed to limiting headroom for compliance.

2.3.4 Loop Current Error Sources—Designing for Minimal Error

Transmitter accuracy is mostly affected by the gain stage of the transmitter's V/I circuit; this gain stage consists of several active and passive components. The active components included in the reference design consist of two OPAs and precision DAC, while passives relate to the resistors. 図 6 displays most error sources produced by these components and highlights the most significant in red.

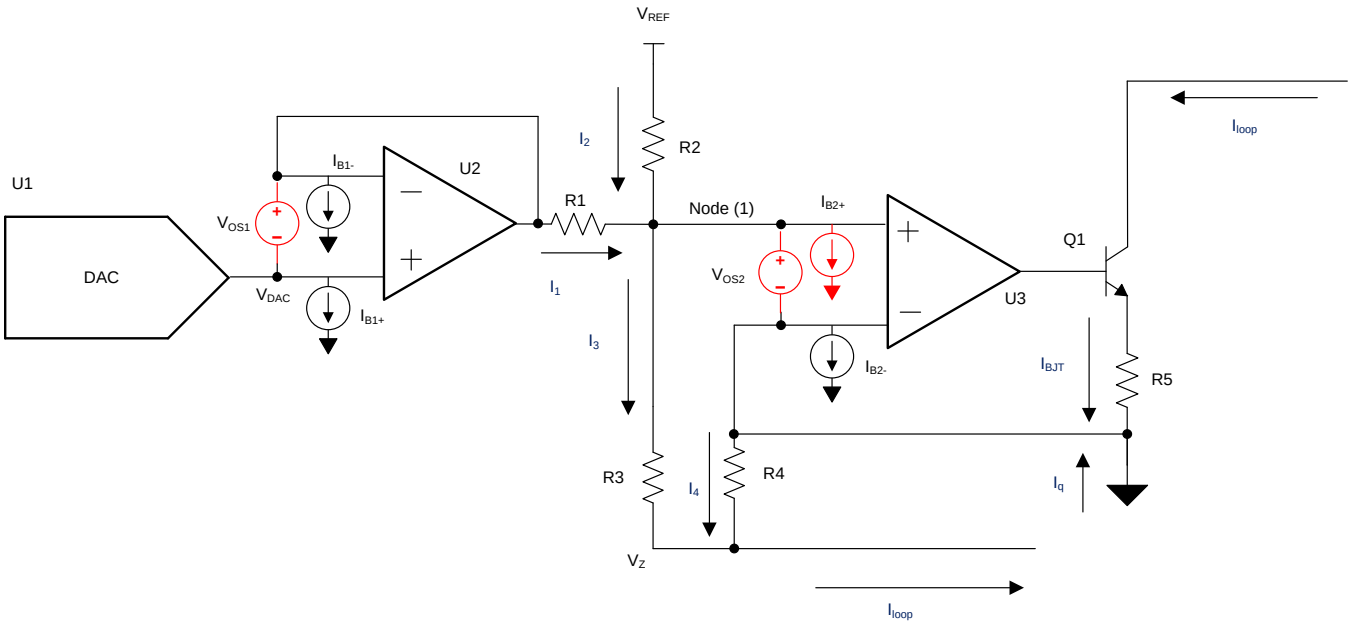


図 6. Transmitter V/I With Error Sources

KCL is performed to include these error sources and yields the equations written below. The KCL equation derived from inspecting Node (1) is shown in 式 7.

$$\frac{V_{OPA2+} - (V_{OS1} + V_{DAC})}{R_1} + \frac{V_{OPA2+} - V_{REF}}{R_2} + I_{B2+} + I_3 = 0$$

$$\therefore I_3 = \frac{(V_{OS1} + V_{DAC}) - V_{OPA2+}}{R_1} + \frac{V_{REF} - V_{OPA2+}}{R_2} - I_{B2+} \quad (7)$$

Applying the input offset error, associated with U3, into this analysis produces the following set of equations when deriving the voltage drop across R3 and R4.

$$(V_{OPA2+}) - (V_{OPA2-}) = V_{OS2}$$

$$I_3 \times R_3 = (V_{OPA2+}) - (V_Z)$$

$$I_4 \times R_4 = (V_{OPA2-}) - (V_Z)$$

$$\therefore I_4 = \frac{I_3 \times R_3 - V_{OS2}}{R_4} \quad (8)$$

To reduce nodal voltages from the previous equations, the negative input node of U3 can be substituted to zero, (V_{OPA2-}) = 0, which reduces the calculation of the loop current to the one expressed in 式 9.

$$\left(V_{OPA2+}\right) = V_{OS2}$$

$$I_3 = \frac{\left(V_{OS1} + V_{DAC}\right) - V_{OS2}}{R_1} + \frac{V_{REF} - V_{OS2}}{R_2} - I_{B2+}$$

$$I_4 = \frac{I_3 \times R_3 - V_{OS2}}{R_4}$$

$$I_{LOOP} = I_3 + I_4 \tag{9}$$

Because all error sources are treated as linearly independent, the total unadjusted error of the entire system can be calculated by performing the root sum squared (RSS) method across all component error sources. The superposition theorem can be applied to 式 9 in verifying individual total unadjusted error percentages. 表 2 provides these calculations.

表 2. Error Source Calculations

COMPONENT	TUE % (MID-SCALE)
REF	0.05
R1	–0.033316675
R2	–0.016658337
R3	0.0495
R4	–0.049475262
VOS1 (OPA333)	0.000325521
VOS2 (OPA335)	–0.002286784
VDAC	0.005571722
IB2+	–0.000166667
RSS TUE (Total) %FSR	0.093925289

2.3.5 HART Modem Circuit

The DAC8740H MODOUT pin of the HART modem connects to the transmitter through an AC coupled capacitor, C1. This capacitor along with R6 creates a high-pass filter that attenuates frequencies lower than the chosen cutoff frequency, 1 / (2 × π × R6 × C1).

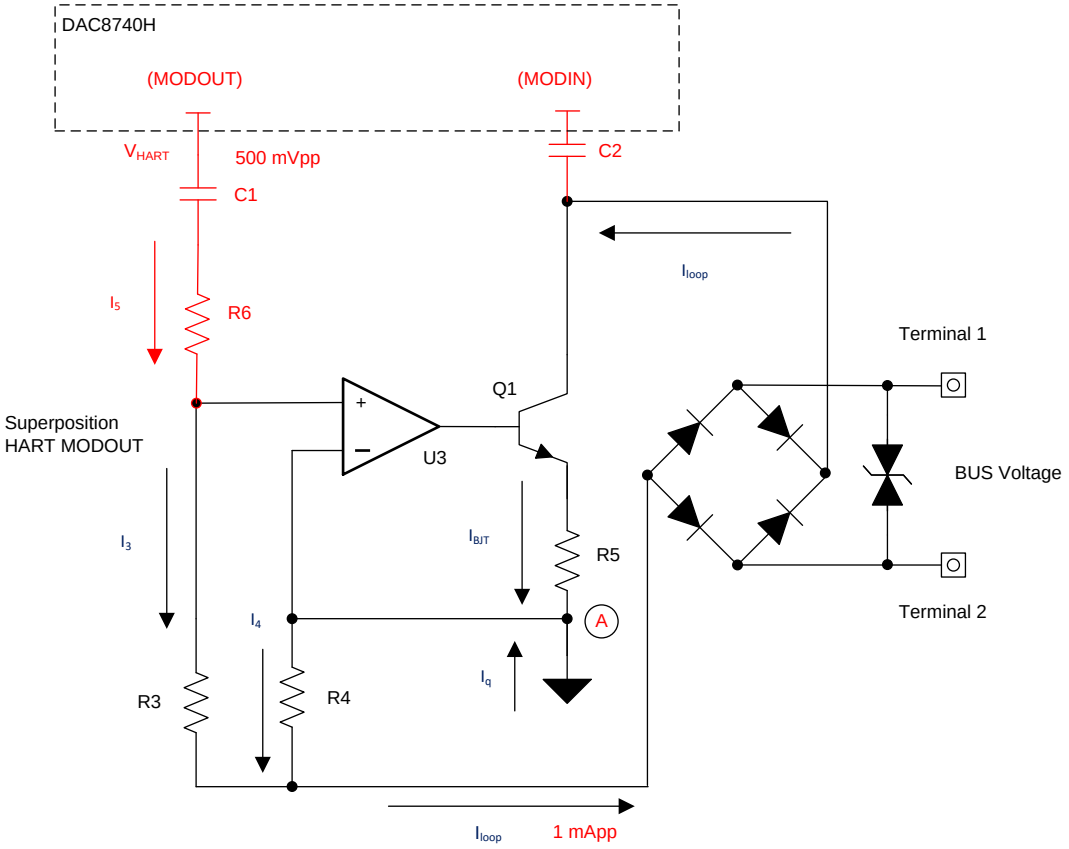


図 7. Superposition of HART Waveform

In 2.3.1, the HART modem is not included in loop current calculations because it essentially outputs 0 V when inactive. However, when the device is active, it must superimpose the loop current analog value with a FSK of 1 mApp. This value is accomplished by connecting R6 to the non-inverting terminal of U3. Through superposition, the AC component of the current loop can be calculated as:

$$I_{OUTpp} = \frac{V_{HART}}{R_6} \times \left(1 + \frac{R_3}{R_4}\right)$$

$$\therefore R_6 = \frac{V_{HART}}{I_{OUTpp}} \times \left(1 + \frac{R_3}{R_4}\right) \quad (10)$$

Substituting schematic values for R3, R4, and the peak-to-peak voltage of MODOUT reveals a required resistance value of 49.9 kΩ. Once R6 is chosen, C1 can be calculated in choosing the cutoff frequency of the high-pass filter. In this reference design, the cutoff frequency is chosen as 679 Hz, ensuring noise and frequencies lower than 1200 Hz and 2200 Hz are effectively attenuated without significantly impacting the HART band frequency range.

The DAC8740H MOD_IN pin connects to the positive BUS supply net of the transmitter circuit through an AC coupled capacitor, C2, and into an internal band-pass filter. The internal band-pass consists of the passives shown in 図 8 and requires 2200 pF for C2 to operate the correct filter, creating cut-off frequencies at 602.4 Hz and 10.4 kHz.

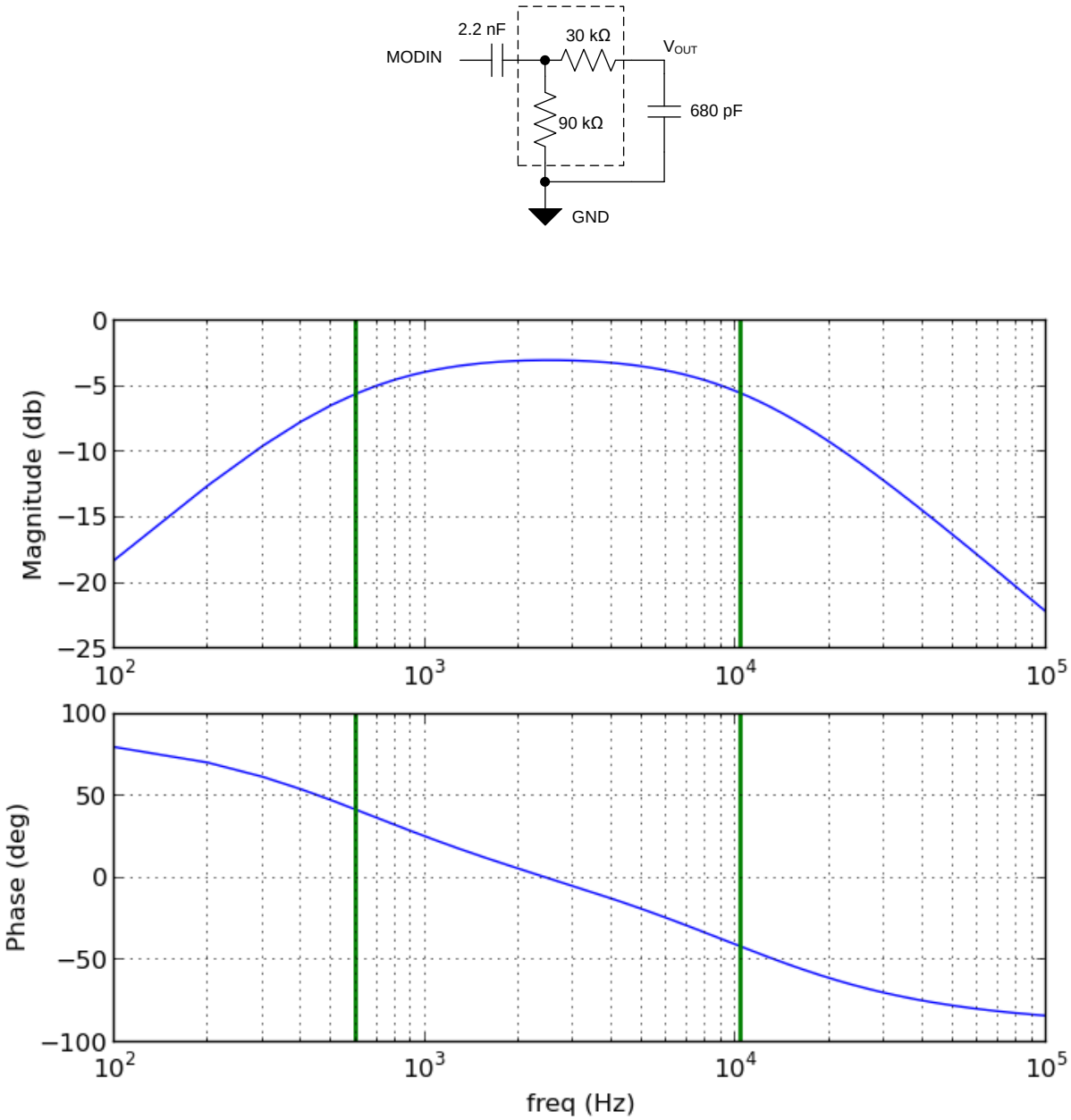


図 8. Band-Pass Filter and Frequency Response

Upon receiving HART communication, the DAC8740H asserts the Carrier Detect pin and directly streams bit data from UART_OUT to the MCU at 1200 baud following the 8O1 UART character format.

注: In this reference design, the internal band-pass filter and internal reference are enabled by connecting their respective enable pin (REF_EN, BPF_EN) to IOVDD.

2.3.6 System Power Budget

When designing two-wire transmitters, consider power consumption. Power supplied from the loop must power all circuitry related to the transmitter and sensor. Because the minimum loop current in two-wire applications is typically 4 mA, the power budget of all transducer circuitry must be well below a maximum allowable system power budget of 3.5 mA. 表 3 lists the specified maximum quiescent current of all included active components, which are provided from their respective data sheet.

表 3. Component Quiescent Currents

DEVICE	QUIESCENT CURRENT
TPS7B69-Q1 (typ)	15 µA
LM4132 (typ)	60 µA
TPS7A4101 (typ)	25 µA
OPA333 (typ)	17 µA
OPA335 (typ)	285 µA
DAC8830	0.475 mA
DAC8740H (typ) internal ref/internal osc	265 µA
MSP430FR5969	Dependent of firmware

The measured combined quiescent current draw of all active components is displayed in 表 4. These measurements are taken across five boards while the MCU is idle.

表 4. Quiescent Current Across Five Boards

BOARD NUMBER	QUIESCENT CURRENT (A)
1	0.002348696
2	0.00259922
3	0.002404303
4	0.002399448
5	0.002387305

2.3.7 Input Protection and Diode Bridge Rectification

Industrial factories sometimes create harsh environments where exposure to dangerous electrical transients is commonplace. To reduce the destructive effects of these environmental hazards, the protection scheme shown in 図 9 is implemented. The protection circuitry consists of a diode bridge rectifier, TVS diode, and ferrite beads.

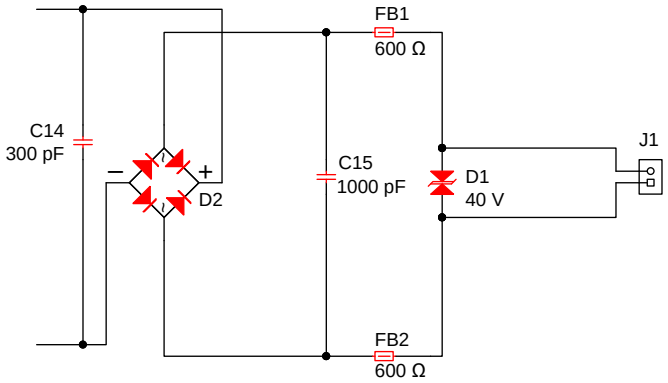


図 9. Diode Bridge Rectifier With TVS Protection Circuit

The first line of defense is the transient voltage suppressor (TVS) diode. This diode is responsible for diverting energies associated with large input voltage transients such as ESD events away from the sensitive inputs of the transmitter circuitry and back to the return path or ground. TVS diodes protect by conducting excess current when the voltage across the diode exceeds the avalanche breakdown voltage. TVS diodes are also very helpful to protect against transients because they break down very quickly and often feature high power ratings, which are critical to survive multiple transient strikes.

Attenuation of transient events is accomplished by implementing passive components. Passive components, primarily resistors, and capacitors are employed to attenuate high-frequency transients and additionally limit the large current produced by these transients. This reference design uses ferrite beads to limit the currents associated with high-frequency transients while maintaining DC accuracy during normal operation. In addition to ferrite beads, a capacitor, C15, is placed across the input terminals to help reduce high-frequency noise.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 Default Hardware Settings

This reference design uses a single jumper to determine the supply for the MCU, which can either be sourced from the loop or connected externally through a header pin. This jumper allows the MCU to be flashed without the need for the design to connect to BUS supply.

3.1.2 Programming Header and MCU Debug Button

This reference design features two push-buttons connected to the MCU. These buttons can invoke certain subroutines or test modes during HART FSK testing and debugging. J3 also provides an interface for the two-wire Spy-Bi-Wire JTAG interface.

表 5. MSP430FR5969 Digital Pin Header and Shunt Connections

HEADER	DESCRIPTION
J3-1	RX_TARGETIN
J3-2	V_DEBUGGER
J3-3	TEST
J3-4	RST
J3-5	GND
J3-6	TX_TARGETOUT
J2 (1-2)	Connect AVDD to IOVDD
J2 (2-3)	Connect to J3-2 pin

表 6. S1 and S2 Push-Button Descriptions

PUSH-BUTTON	DESCRIPTION
S1	Connects to P4.5 on MSP430FR5969
S2	Connects to P4.6 on MSP430FR5969

3.1.3 MSP430FR5969 Firmware With Included HART Stack

The firmware flashed onto the MCU uses a functioning HART FSK stack developed with the assistance of Smart Embedded Systems.

3.2 Transmitter Test Setup and Results

3.2.1 Total Unadjusted Error (TUE) Test Setup

図 10 displays the test setup when measuring the transmitter's output current. The 24-V BUS supply is created with the HP E3631A and current through the loop is recorded with the HP3458A digital multimeter.

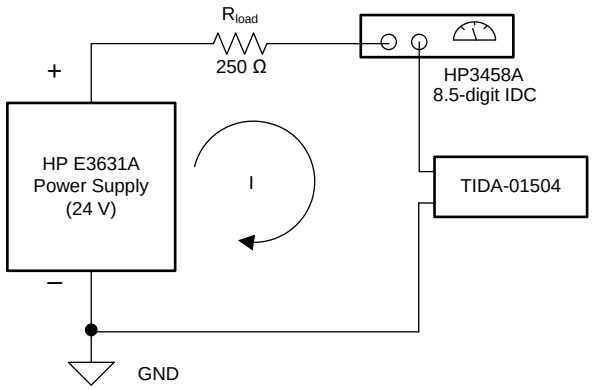


図 10. Test Setup of TUE

Measurement data is taken on five different boards, producing the 4- to 20-mA transfer function shown in 図 11.

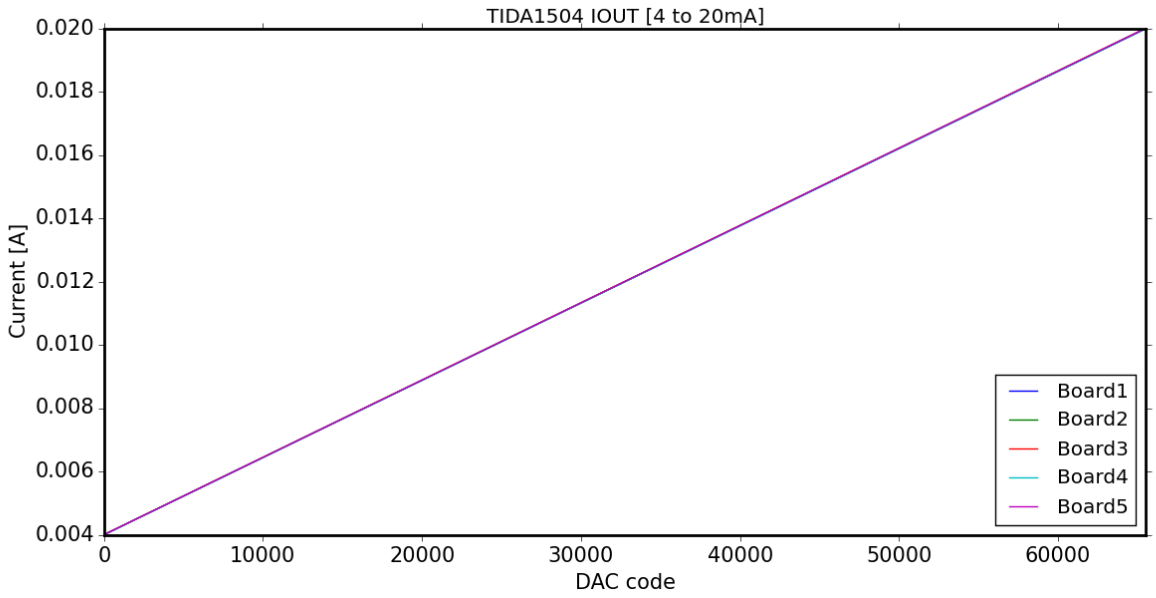


図 11. Measured Transfer Function

The TUE of the transmitters is displayed in 図 12.

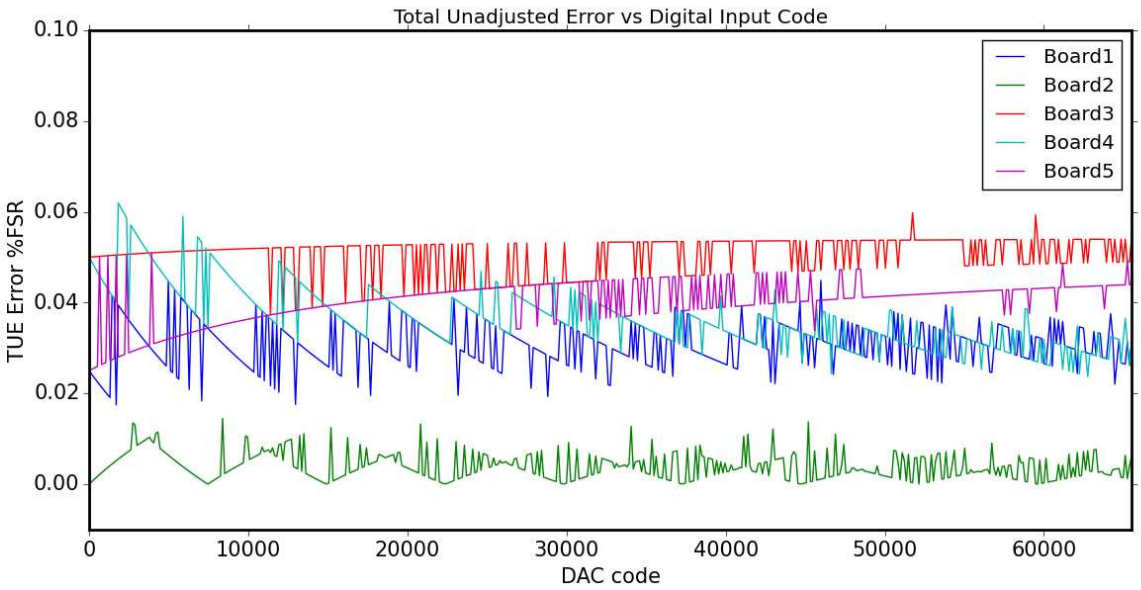


図 12. Measured TUE

3.2.2 HART Protocol Definitions and Certification Tests

Three different definitions are used when describing the HART communication protocol. These definitions or layer specifications are referred to as the FSK Physical Layer, Data Link Layer, and Application/Command Summary Layer.

All three specifications are tested during HART Certification; however, this design guide only focuses on the FSK Physical Layer portion, which relates to the design of the transmitter. Direct all inquiries related to the software stack that encompasses the Data Link Layer and Application Layer to Smart Embedded Systems (SES).

3.2.2.1 outlines several key tests, procedures, and equipment necessary to determine HART conformance of the transmitter.

3.2.2.1 HART Waveform Test Setup

図 13 shows the setup for the HART waveform test. A 500-Ω, 1% resistor is connected in series with the power supply and transmitter. An oscilloscope with AC coupled probes captures and records the HART signal measured across the terminals of the transmitter.

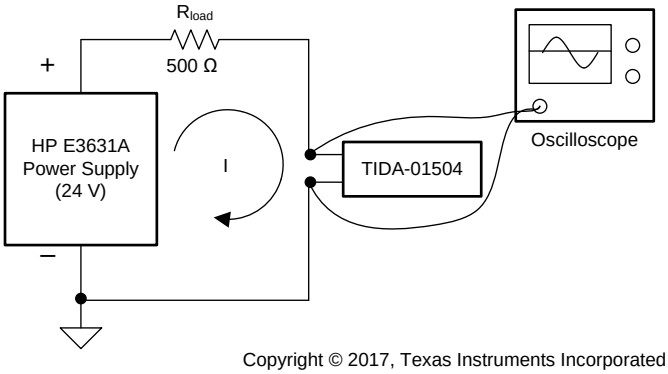


図 13. Test Setup of HART Waveform

Because the resolution of the oscilloscope can impact the captured measurements of the signal, it is recommended to only capture one waveform cycle, with the vertical and horizontal scales adjusted to ensure that the entire signal covers most of the screen.

Using the aforementioned setup, the following waveform characteristics are captured and verified for the 1200-Hz and 2200-Hz components of the HART waveform.

The measured waveforms are shown in 図 14 and 図 15.

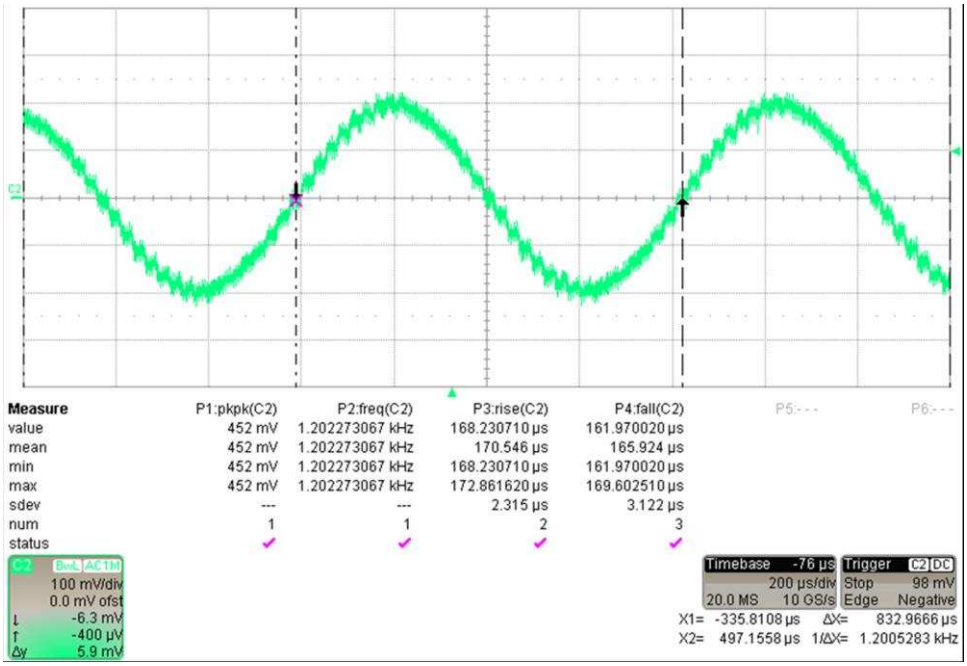


図 14. 1.2-kHz HART Wave Signal

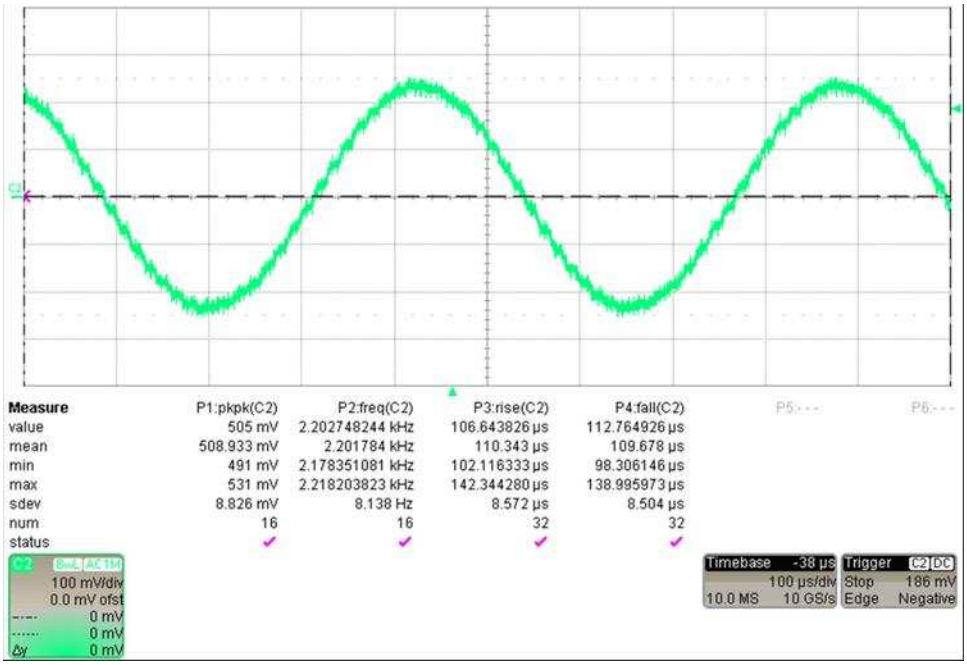


図 15. 2.2-kHz HART Wave Signal

3.2.2.2 HART Amplitude

HART amplitude requirements specify that the amplitude levels must fall within the 400-mVpp to 600-mVpp range. 表 7 shows the amplitude levels recorded on this reference design.

表 7. Recorded HART Amplitude Levels

TEST	MEASURED	PASS CRITERIA
1200-Hz measured amplitude	452 mVpp	(400 to 600 mVpp: Hi Z)
2200-Hz measured amplitude	505 mVpp	(400 to 600 mVpp: Hi Z)

3.2.2.3 HART Frequency

表 8 shows the HART frequency requirements along with the measured results of this reference design.

表 8. HART Frequency Requirements and Results

TEST	MEASURED	PASS CRITERIA
1200-Hz measured frequency	1202 Hz	1188 to 1212 Hz
2200-Hz measured frequency	2202 Hz	2179 to 2222 Hz

3.2.2.4 HART Rise and Fall Times

HART rise and fall times associated with the HART waveform of this reference design are reported in 表 9, along with HART timing requirements for conformance.

表 9. HART Rise and Fall Time Requirements and Results

TEST	MEASURED	PASS CRITERIA
1200-Hz rise time	168 µs	75 to 200 ms
1200-Hz fall time	161 µs	75 to 200 ms
2200-Hz rise time	106 µs	75 to 200 ms
2200-Hz fall time	112 µs	75 to 200 ms

3.2.2.5 Output Noise During Silence

When the device is idle and not transmitting HART information, the output of the transmitter must not couple noise onto the loop Any excess can disrupt communication between other devices on the network or interfere with the reception of HART signal to the transmitter.

The setup involves a low-noise power supply, which can be created from several batteries in series. In this setup, three (3) 9-V batteries are connected in series to create a 27-V supply. The measurement setup is similar to the one described in 3.2.2.1 with the addition of a digital filter that connects across the transmitter's terminals. The digital filter, HCF_TOOL-31, is a band-pass filter with a pass band of 500 Hz to 10 kHz with a gain of 10X.

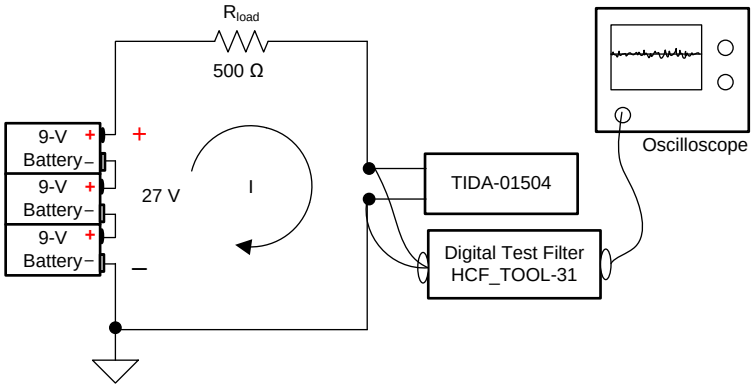


図 16. Test Setup of Output Noise During Silence

This test requires two measurements: Broadband noise and in-band noise:

1. The passing criterion for broadband noise is an RMS reading of less than 138 mV RMS.
2. The passing criterion for in-band noise is a noise level less than 2.2 mV RMS. If the digital filters are used, then the output of the filter must be less than 22 mV RMS because the filter includes a gain of 10X.

Both RMS measurements are shown in 図 17 with results in 表 10.

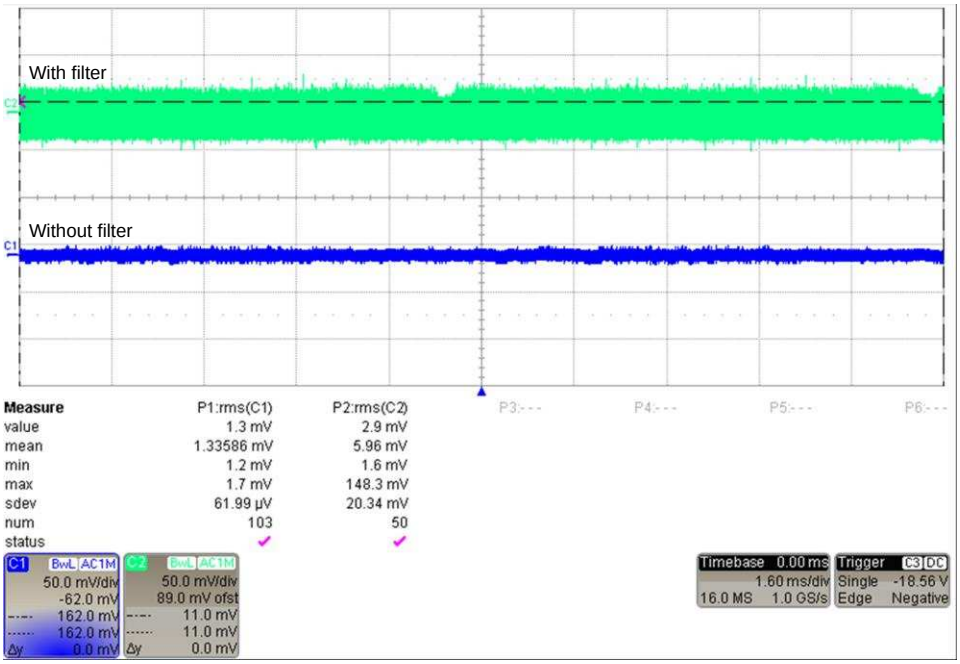


図 17. Output Noise During Silence Measurement

表 10. Output Noise During Silence Results

TEST	MEASURED	PASS CRITERIA
Broadband noise w/o filter	1.3 mV RMS	138 mV max
In-band (500 Hz to 10 kHz) using HART digital test filter (10X gain)	2.9 mV RMS	22 mV RMS max

3.2.2.6 Receive Impedance

Receive impedance is an electrical characteristic that has the ability to impact performance in HART point-to-point and multi-drop operation. In point-to-point, receive impedance directly impacts the distance required to maintain correct HART signaling. In multi-drop, the impedance relates to the number of multi-dropped devices that can operate over the network.

In this measurement, receive impedance is represented as two different components: the equivalent device capacitance Cx, and equivalent device resistance Rx. The setup displayed in 図 18 measures the input impedance of the transmitter. A waveform generator or power supply, which is capable of superimposing AC signals on a DC level, provides loop voltage to the transmitter and 5-kΩ test resistor. A sinusoidal waveform is sourced from the waveform generator, and the amplitude is set so that a 1-Vpp drop develops across the transmitter terminals when set at 200 Hz. A True RMS Digital Voltmeter records the voltages Va and Vb, while performing a frequency sweep from 200 Hz to 10 kHz.

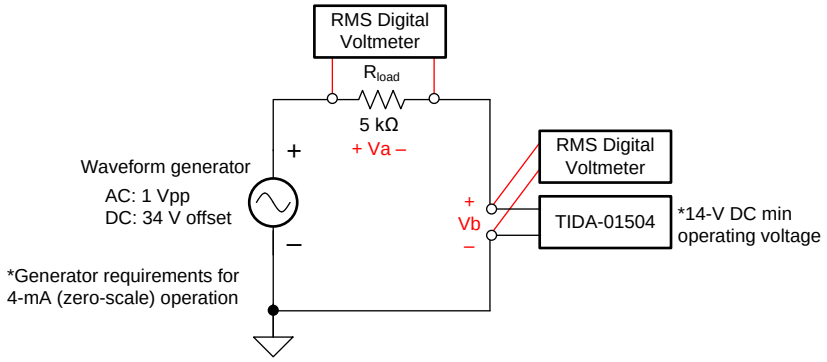


図 18. Test Setup of Transmitter Input Impedance

When needed, adjust the power supply so that the voltage developed across the transmitter's terminals is well within the device's normal operating input voltage range. Using a minimum transmitter voltage of 14 V and zero-scale current of 4 mA produces a required DC supply value of 34 V.

If the power supply or waveform generator does not provide adequate supply levels, use the difference amplifier circuit shown in 図 19 in conjunction with an AC and DC supply to reach the levels required for testing.

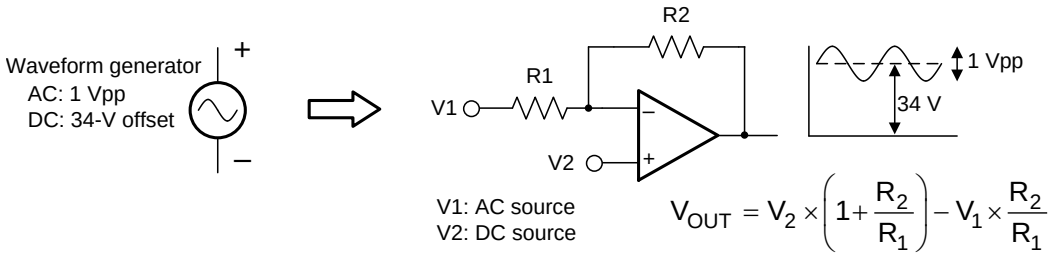


図 19. Difference Amplifier Circuit

Data is measured from 200 Hz to 10 kHz, with the frequency increments shown in 表 11.

The transmitter impedance magnitude, Zm, is calculated at every frequency increment using 式 11.

$$Z_m = R_{Va} \cdot V_b \quad (11)$$

Where:

- Va is the measured RMS value across the 5 kΩ resistor
- Vb is the drop across the transmitter

表 11 shows the impedance of this reference design across frequency.

表 11. Impedance Measurements of Design versus Frequency

FREQUENCY (Hz)	Vb (VRMS)	Va (VRMS)	Zm
200	0.353	0.0051	353456.8
500	0.355	0.0113	160428.6
950	0.36	0.0256	71811.56
1600	0.362	0.0504	36678.36
2500	0.359	0.0843	21746.97
5000	0.331	0.16	10564.28
10000	0.26	0.248	5353.694
20000	0.165	0.308	2735.679
50000	0.0744	0.355	1134.123

The equivalent impedance is then plotted on a logarithmic graph to estimate Cx and Rx, as shown in 図 20.

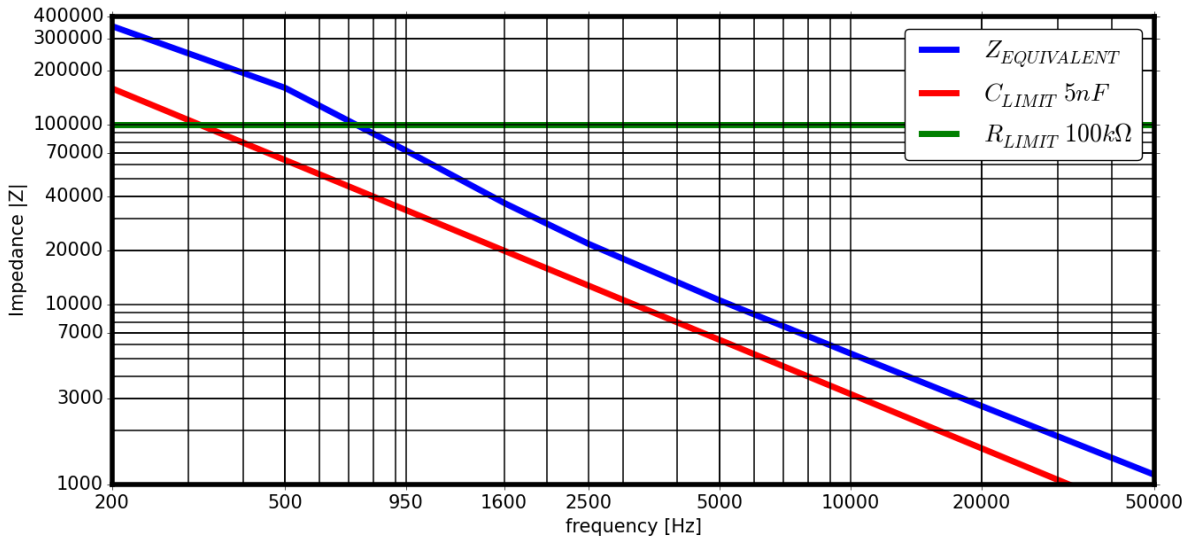


図 20. Impedance of Design versus Frequency

Test conditions and results are as follows:

- RX: 350000
- CX: 3000 pF
- Loop current: 4 mA
- Resistors value: 5.1 kΩ

3.2.2.7 FieldComm Group Certification Results

This reference design is verified to be compliant with HART FSK Physical Layer Specification (HCF_SPEC-54) using the HART Physical Layer Test Specification (HCF_TEST-2). Through this design, the DAC8740H has been validated and registered by the FieldComm Group as a compliant HART enabled device. 図 21 shows the registration certificate, and the registered device can be found on the FieldComm group website.


HART® REGISTERED

Certificate of Registration
FieldComm Group Verified

Texas Instruments Manufacturer	DAC8740H Product Name
60B0 Manufacturer ID (Hex)	E3AC Expanded Device Type (Hex)
7 HART Protocol Revision	01 Device Revision (Hex)
00 Hardware Revision (Hex)	01 Software Revision (Hex)
8/25/2017 Test Date	FieldComm Group Verification Method

The above product has successfully completed the validation process and meets the requirements to be "HART REGISTERED".

"HART REGISTERED" products conform to GB/T 29910.1-6-2013 and IEC 61158 standards.

Registration Number: L2-06-1000-692 Registration Issue Date: September 26, 2017 Approval:

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HART® is a registered trademark of FieldComm Group

図 21. HART Registration Certificate

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01504.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01504.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01504.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01504.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01504.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01504.

5 Related Documentation

1. FieldComm Group, *HART Protocol Test Specifications (HART Protocol Revision 7.5)*

5.1 商標

6 Terminology

DAC— Digital-to-analog converter

V/I— Voltage to current

HART— Highway addressable remote transducer

MCU— Microcontroller

FSK— Frequency shift keying

OPA— Operational amplifier

TVS— Transient voltage suppressor

7 About the Author

MATTHEW SAUCEDA is an applications engineer in the Precision Digital-to-Analog Converters group at Texas Instruments, where he supports industrial and catalog products. Matthew received his MSEE from Texas A&M University in 2009.

7.1 Acknowledgments

Special thanks to fellow colleagues **SHREENIDHI PATIL**, **COLLIN WELLS**, and **KEVIN DUKE** for their valuable inputs in this reference design.

Additionally, TI wishes to acknowledge Smart Embedded Systems (SES) in Fremont, California for their participation in this project concerning the development of the HART stack used for achieving device registration with the FieldComm Group. To reach out to SES, go to http://www.smartembeddedsystems.com/

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