参考資料

TI Designs: TIDA-01555
複数のADCを使用する同時コヒーレントDAQ用の柔軟なインターフェイス(PRU-ICSS)のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインでは、6つの高電圧バイポーラ入力、8チャネル、マルチプレクサ入力のSAR ADCを、Sitara™ Arm®プロセッサと接続し、プログラム可能なリアルタイム・ユニット(PRU-ICSS)を使用して入力チャネルの数を増やす、インターフェイスの実装を紹介します。ADCは、すべてのADC間にわたって同じチャネルを同時にサンプリングするよう構成されます。この設計では、PRU-ICSSがライン・サイクルごとに640サンプルをサンプリングし、1536ksps (各サンプル = 16ビット)のデータレートを処理できることが注目点です。50Hz サイクルの場合、これは 6 つの ADC が同時に動作したときチャネルごとに 32ksps に対応します (640 サンプル/サイクル × 50Hz × 6 ADC × 8 チャネル = 1536ksps)。また、2番目のPRUはデータを後処理し、コヒーレントなサンプリングを達成するため使用されます。

リソース

TIDA-01555	デザイン・フォルダ
ADS8688	プロダクト・フォルダ
BEAGLEBK	ツール・フォルダ
OPA4197	プロダクト・フォルダ
TPS22914	プロダクト・フォルダ
TPS65131	プロダクト・フォルダ
TPS7A6533	プロダクト・フォルダ
TPS7A39	プロダクト・フォルダ
LP2992	プロダクト・フォルダ
CDCLVC1106	プロダクト・フォルダ

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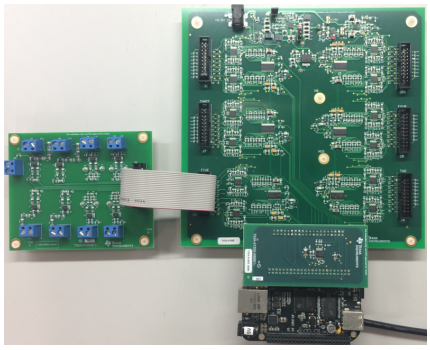
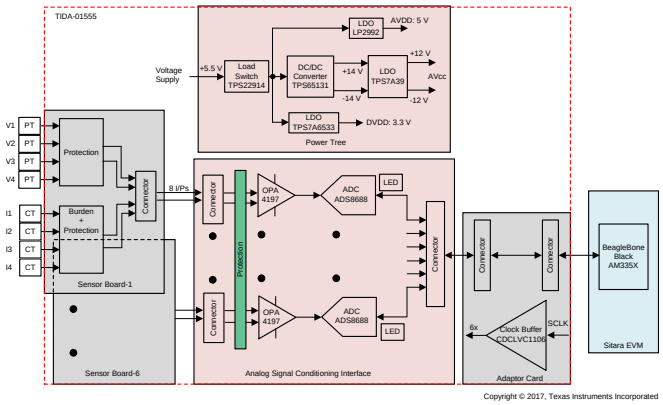


特長

- PRU-ICSS (Sitaraプロセッサ)を使用して複数のSAR ADCと通信する柔軟なインターフェイス
- AC電圧および電流の測定精度
  - AC電圧: 2.5V～120Vについて±0.2%未満
  - AC電流: 2.5A～70Aについて±0.2%未満
  - 6つのADCにわたる同時サンプリング (16ビット、500ksps/ADC)
- PRU-ICSSインターフェイス
  - PRU-ICSSはチャネル拡張のため柔軟なデータのキャプチャを提供
  - ファームウェア・ベースの手法により、別のSitaraプロセッサでも再利用可能
  - ライン・サイクルをソフトウェアで計算し、CS信号を調整することで、コヒーレントなサンプリングを実現

アプリケーション

- 保護リレー、IED
- 端末装置
- マージング・ユニット
- プログラマブル・ロジック・コントロール(PLC)
- 航空
- 計測機器



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1 System Description

In sectors such as grid infrastructure, factory automation, test and measurements , and so on, there are various applications in which multiple analog signals from sensors need to be captured on a single processor for monitoring and protection of critical equipment. In these scenarios, multiple analog-to-digital converters (ADCs) convert the analog signals from transducers to digital domain for further processing or to communicate through the network. Choosing a converter with good performance with very high resolution and parametric data is only one half of the equation. When more than two ADCs need to be interfaced with a single processor, choosing the right processor becomes challenging due to limited peripherals. The choice becomes narrower if more ADCs need to be interfaced with higher throughput. Controlling the timing of the interface and control signals along with the jitter is equally as important as it helps in accurate data representation with minimal spectral leakages.

One of the ways to interface multiple data converters is to select a processor that can support multiple SPI peripherals as shown in 図 1. Depending on the architecture, the interaction between the CPU, the direct memory access (DMA), and the system and data bus poses certain restrictions. Even though the processor can support multiple SPI peripherals, the path in which the data flows is shared. This path limits not only the rate at which data can be accessed from two or more ADCs, but also requires the CPU to be constantly interrupted.

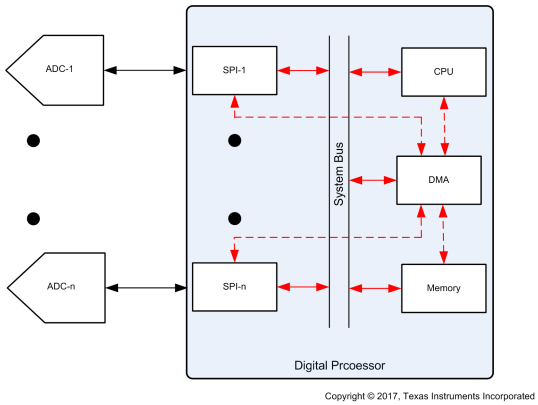

図 1. Interface Between Multiple ADCs With a Processor Using SPI

Furthermore, the delays introduced in the SDI, SDO, and SCLK paths could be different when multiple ADCs are used in a system. The round-loop delay becomes a bigger issue at high speeds or if digital isolators are used as shown in 図 2. Compensation methodologies can be used to overcome path dependent delay but are difficult to implement when using SPI peripherals for communication.

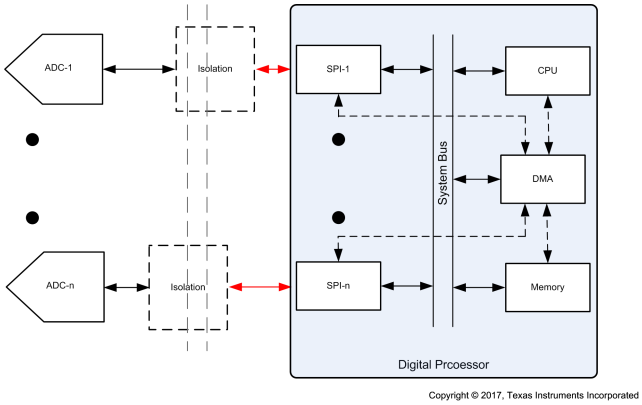

図 2. Data Acquisition System With Digital Isolation

FPGAs are used as an intermediate interface element to overcome these issues. This reference design showcases how to implement a flexible interface that can simultaneously connect with six ADCs using the Sitara processor. The PRU-ICSS subsystem integrated in the processor are used for both data acquisition and for data computation. This frees up the bandwidth of the Arm core as the interface and processing can now be handled independent of the core CPU.

This reference design:

- Provides data acquisition from 48 analog input channels using six ADCs
- Does the analog signal conditioning for improved signal chain performance
- Uses PRU-ICSS to adjust the time base for the communication interface to achieve coherent sampling thereby reducing the spectral leakages

1.1 Protection Relay

Protection Relays are used to improve the reliability and efficiency of the power systems in various stages. These stages include power generation to transmission and distribution by detecting defective transmission lines, apparatus or other abnormal power system conditions. These relays are placed to monitor electrical parameters in the power systems or in the vicinity of primary equipment to detect any abnormal conditions to prevent any damages. Protection relay consists of an AC analog input module, which acquires data from voltage and current sensors from different phases. In digital protection relays, data acquisition system consists of measurement of voltages and currents along with analog signal conditioning, data converters, and host interface to capture digital values providing post processing of the acquired data. In this application, flexible data acquisition shown in this reference design can be used to achieve required AC and DC performance.

1.2 Grid Automation

In substation automation, terminal units and merging units collect and forward sensor data to intelligent electronic devices (IEDs). These units collect the data from conventional or non-conventional instrument transformers and send the sampled current and voltage signals over the network. This reference design can be used to interface and process the data using a single processor for very high speeds.

1.3 Other Applications

In programmable logic controllers (PLCs) and other instrumentation systems in avionics and test and measurement, this reference design can be customized for different number of input channels to realize high-speed data acquisition system for simultaneous sampling.

1.4 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
ADC	16-bit, 8-channel, 500 ksps	ADS8688 500-ksps, 8-Channel, 16-Bit, SAR ADC with Bipolar Input Ranges 2.2.1
Number of channels	48 channels	
Input voltage range at transducer	120-V AC RMS	2.3.2
Input current range at transducer	70-A AC RMS	2.3.2
Input voltage range at ADC	±10.24 V	±20-V overvoltage protection
AC voltage accuracy	< ±0.2%	2.5 to 120 V RMS
AC current accuracy	< ±0.2%	2.5 to 70 A RMS
Interface	4-wire SPI (ADC)	
	PRU-ICSS (processor)	
SPI clock frequency	10 MHz (for six ADCs)	2.3.1.2
	17 MHz (ADC max)	
	25 MHz (PRU-ICSS max)	
DC performance	Code spread of ≤ 4	3.2.2.2
	Sigma ≤ 0.58	
AC performance	SFDR = 110 dB	Fin = 64 Hz, number of points = 65536
Sampling frequency per input channel	32 ksps per channel across six ADCs	Total throughput of 1536 ksps
Coherent sampling	CS adjustment for input frequency 50 Hz ± 10%	2.3.1.3.1
Power supply	5-V analog supply for ADS8688	
	3.3-V digital supply	
	±12-V analog signal conditioning of input signals	

2 System Overview

2.1 Block Diagram

This reference design consists of the following subsystems:

- Sensor boards connect outputs of current transformers (CTs) and potential transformers (PTs) to the data acquisition board.
- The data acquisition board has six ADS8688 for supporting 48 channels taking inputs from sensor boards. In addition, high voltage drivers (±10 V) are used to gain the signal.
- A 5.5-V supply is used to derive all the voltage rails including ±12 V, +5 V, +3.3 V.
- The adapter card acts as an intermediate interface to match the pin signals between the ADC and the Sitara processor. A clock buffer is added to clean up the clock before fanning out to six ADCs.
- The BeagleBone Black EVM is used as the host to demonstrate the working of PRU-ICSS.

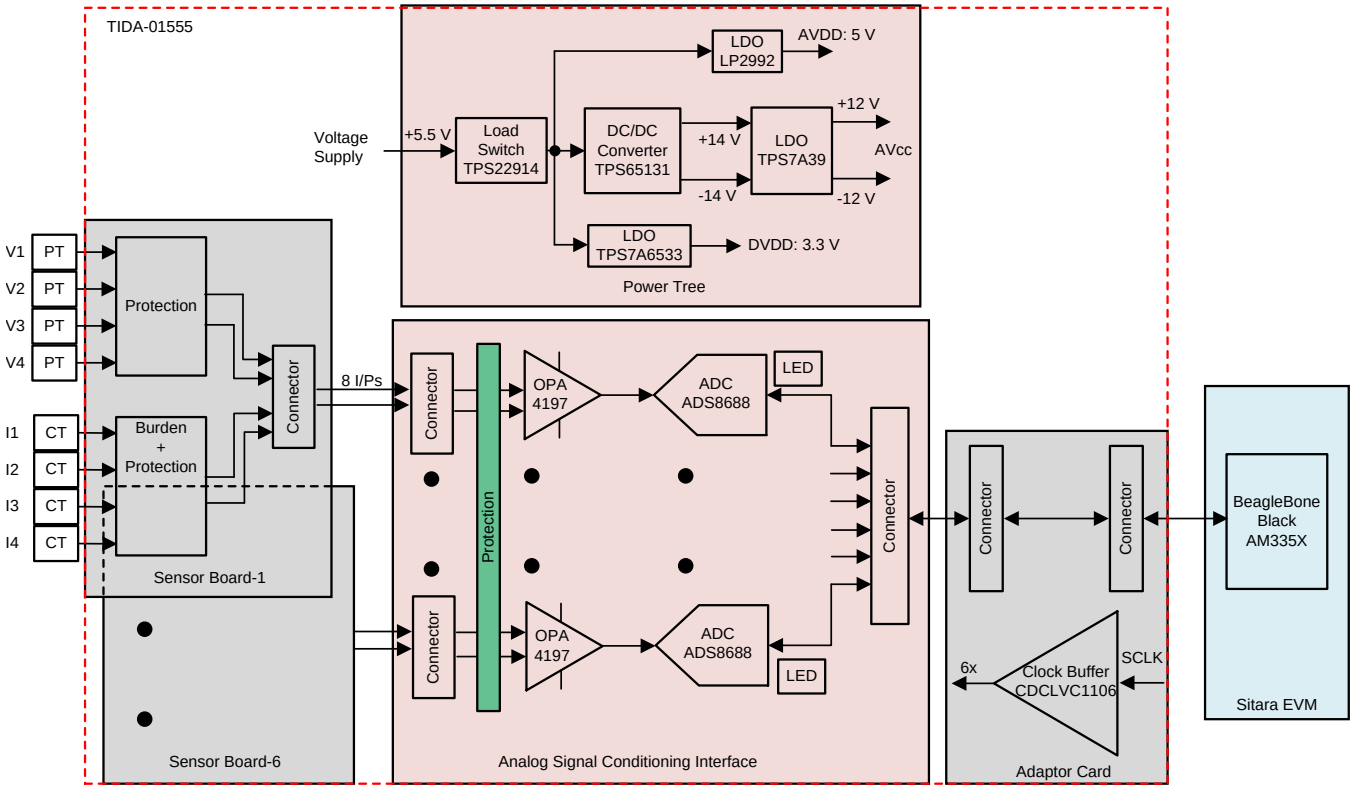

図 3. Block Diagram of TIDA-01555

図 4 shows the interconnection between the ADCs and the Sitara processor. SDI and SDO pins are all connected to individual GPO, GPI pins in PRU. All CS pins are tied to a single GPO pin for simultaneous sampling across ADCs. Each clock pin is driven by separate output lines from the clock buffer, which takes input from a single GPO pin of PRU.

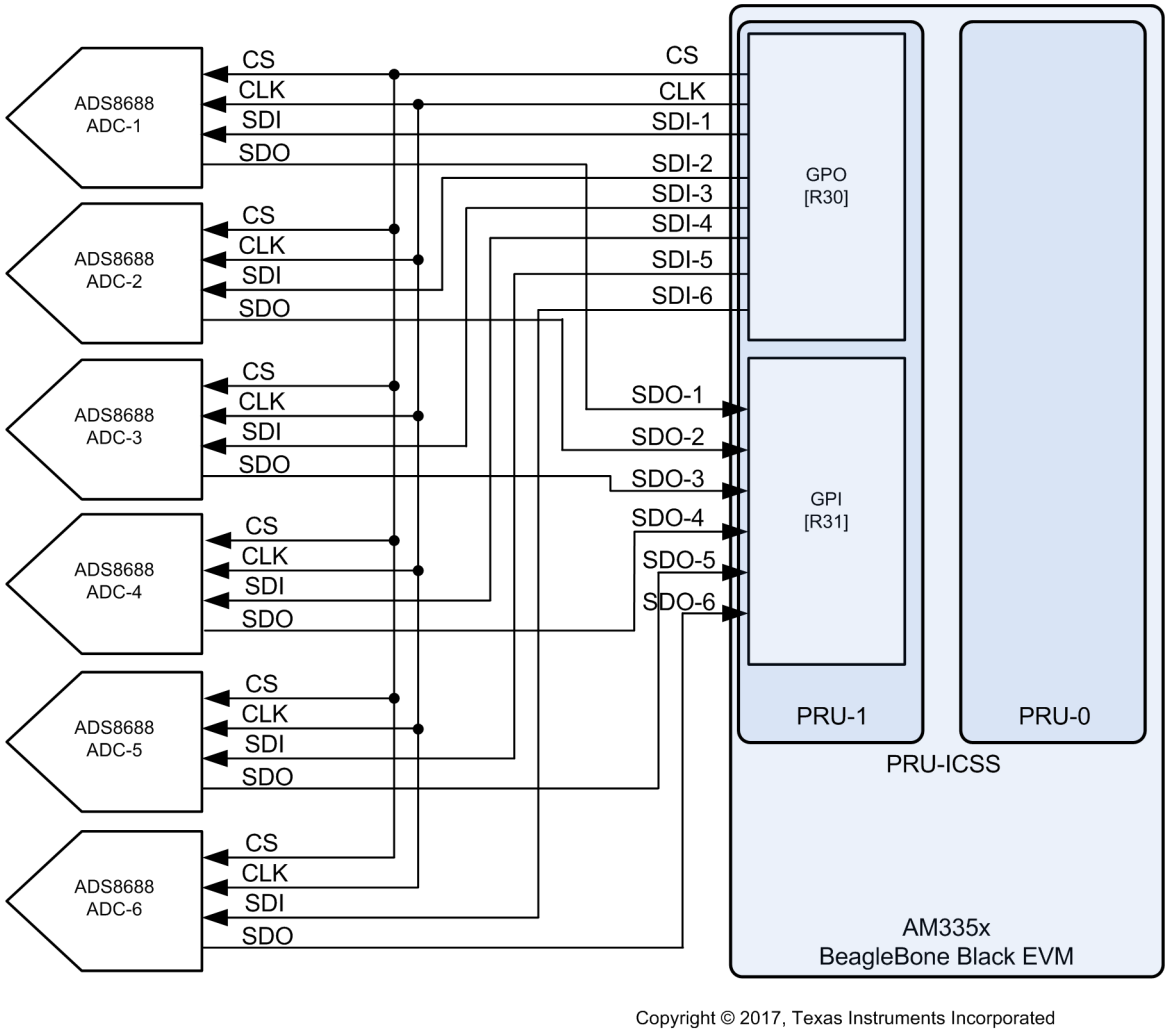

図 4. Interconnection Between Six ADS8688s and PRU-ICSS

2.2 Highlighted Products

2.2.1 ADS8688: 500-kSPS, 8-Channel, SAR ADC With Bipolar Input Ranges

The ADS8688 is an 8-channel, 16-bit successive approximation register (SAR) ADC capable of running at 500 ksps. The ADC has an integrated front-end mux with automatic and manual scanning modes, an on-chip precision low drift reference, and ±20-V overvoltage protection. Each input channel on the device can support true bipolar input ranges of ±10.24 V, ±5.12 V, and ±2.56 V as well as unipolar input ranges of 0 V to 10.24 V and 0 V to 5.12 V while operating on a 5-V unipolar supply. The gain of the analog front end (AFE) for all input ranges is accurately trimmed to ensure a high DC precision. The input range selection is software-programmable and independently controlled for each channel. The device offers a 1-MΩ constant resistive input impedance irrespective of the selected input range.

The ADS8688 offers a simple SPI-compatible serial interface to the digital host and also support daisy-chaining of multiple devices. The digital supply operates from 1.65 V to 5.25 V, enabling direct interface to a wide range of host controllers. For more details on the features of the ADS8688, see *ADS868xA 16-Bit, 500-kSPS, 4- and 8-Channel, Single-Supply, SAR ADCs with Bipolar Input Ranges*.

2.2.2 AM3358

The AM3358 device belongs to family of AM335x processors, based on the Arm Cortex®-A8 core that is enhanced with image, graphics processing, peripherals, and industrial interfaces. This device supports high-level operating systems (HLOS) such as Linux, which is available free of charge from TI. 図 5 provides more details on the subsystems inside the AM335x processor.

- The microprocessor unit (MPU) subsystem is based on the Arm Cortex-A8 core.
- The PRU-ICSS is separate from the Arm core, which allows independent operation and clocking for greater efficiency and flexibility. The PRU-ICSS enables additional peripheral interfaces and real-time protocols. Along with its access to pins, events, and all system-on-chip (SoC) resources, the programmable nature of the PRU-ICSS provides flexibility in implementing fast, real-time responses, specialized data handling operations, custom peripheral interfaces, and in offloading tasks from the other processor cores of the SoC.

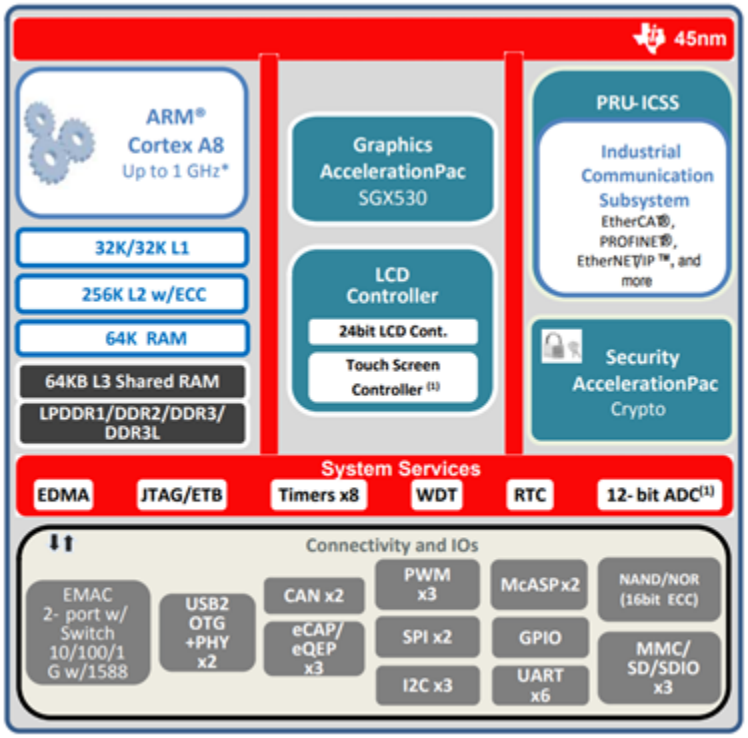

Figure 3. AM335x Block Diagram

図 5. Block Diagram of AM335X

This reference design showcases the PRU-ICSS's ability to implement a custom simultaneous SPI to connect to multiple high-speed ADCs.

2.2.3 OPA4197: Precision, Rail-to-Rail I/O Operational Amplifier

The 36-V op amp OPA4197 drives ±10.24 V of voltage at the input of the ADS8688. The OPA4197 offers outstanding DC precision and AC performance, including rail-to-rail input/output, low offset (±25 μV, typ), low offset drift (±0.25 μV/°C, typ) with a 10-MHz bandwidth.

2.2.4 TPS22914: 37-mΩ On-Resistance Load Switch

The TPS22914 is a small, low RON, single-channel load switch with controlled slew rate. The device contains a N-channel MOSFET that can operate over an input voltage range of 1.05 V to 5.5 V and can support a maximum continuous current of 2 A. The switch is controlled by an on and off input, which is capable of interfacing directly with low-voltage control signals. The small size and low RON makes this device ideal for monitoring the system current and for controlling the power-on sequence.

2.2.5 TPS65131: Positive and Negative Output DC/DC Converter

The TPS65131 is dual-output DC/DC converter that generates a positive output voltage up to 15 V and a negative output voltage down to –15 V with output currents in a 200-mA range in typical applications, depending on input voltage to output voltage ratio.

The device operates with only a 500-μA device quiescent current. Independent enable pins allow power-up and power-down sequencing for both outputs. The device has an internal current limit overvoltage protection and a thermal shutdown for highest reliability under fault conditions.

2.2.6 TPS7A39: 150-mA, Positive and Negative LDO Voltage Regulator

The TPS7A39 device is a dual, monolithic, high-PSRR, positive and negative low-dropout (LDO) voltage regulator capable of sourcing (and sinking) up to 150 mA of current. The regulated outputs can be independently and externally adjusted to symmetrical or asymmetrical voltages, making this device an ideal dual, bipolar power supply for signal conditioning. The TPS7A39 also features high PSRR to eliminate power-supply noise, such as switching noise, that can compromise signal integrity.

2.2.7 TPS7A6533-Q1: 300-mA, Low-Dropout Regulator

The TPS7A6533-Q1 is a 3.3-V LDO from a family of low-dropout linear voltage regulators designed for low power consumption and quiescent current less than 25 μA in light-load applications. This device features integrated overcurrent protection and a design to achieve stable operation even with low-ESR ceramic output capacitors. A low-voltage tracking feature allows for a smaller input capacitor and can possibly eliminate the need of using a boost converter during cold crank conditions. Because of these features, this device is well-suited in power supplies for various automotive and industrial applications.

2.2.8 LP2992: Micropower, 250-mA, Ultra-Low-Dropout Regulator

The LP2992 is a 250-mA, fixed-output voltage regulator designed to provide ultra-low dropout and low noise with enhanced stability and precise output.

2.2.9 CDCLVC1106: LVCMOS High-Performance Clock Buffer

The CDCLVC1106 is a modular, high-performance, low-skew, general-purpose clock buffer family with low pin-to-pin skew of < 50 ps and low additive jitter of < 100 fs.

2.3 System Design Theory

2.3.1 Interfacing With Multiple ADCs

The GPIO pins from PRU-ICSS transfer data between all ADCs and the processor. While PRU-1 handles the external data communication, PRU-0 performs low-level filtering and zero cross detection. The Arm core running RT Linux can be used for further processing of data and HMI control.

2.3.1.1 PRU-ICSS

The PRU-ICSS consists of dual 32-bit RISC cores, shared data, instruction memories, internal peripheral modules, and an interrupt controller (INTC). Along with its access to pins, events, and all SoC resources, the programmable nature of the PRU provides flexibility in implementing fast real-time responses, custom peripheral interfaces, and in offloading tasks from the other processor cores of the SoC.

The execution path of the PRU core is not pipelined, and nearly every instruction (outside of memory loads) completes in a single cycle. This allows the PRU cores to operate in a 100% deterministic fashion that is ideal for interfacing to real world events and devices in applications such as a data acquisition system.

図 6 shows the functional block diagram of the PRU-ICSS.

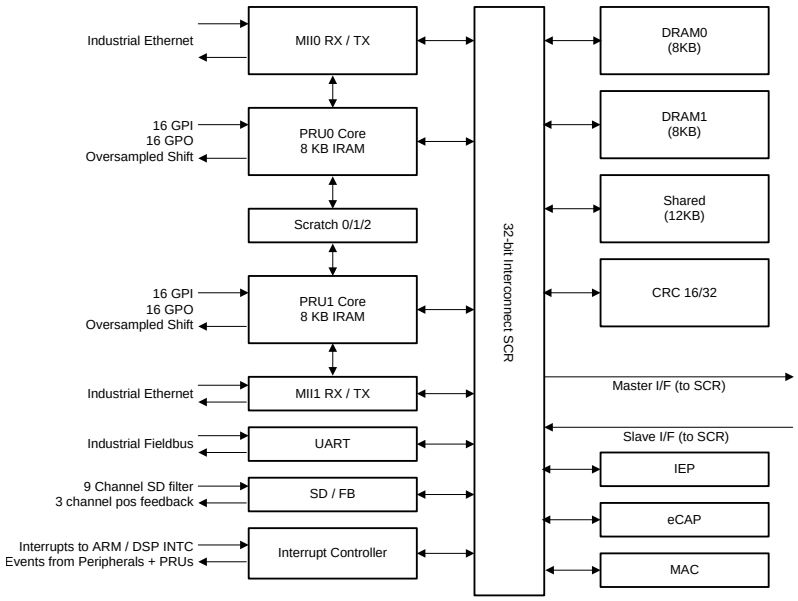

図 6. Functional Block Diagram of PRU-ICSS

2.3.1.2 PRU-ADC Interface (Implemented in PRU-1)

The PRU-ICSS subsystem runs on a 200-MHz internal clock. However, the ADC data rate (SCLK) is limited by the number of instructions that needs to be executed by the PRU for reading and writing data, which in turn depends on the number of devices connected. 表 2 shows the maximum data rate that can be achieved when using multiple ADCs.

表 2. Maximum Clock Speed for Interfacing Multiple ADCs

NUMBER OF ADCs	MAXIMUM CLOCK SPEED
1	25 MHz
2	20 MHz
3	16.67 MHz
4	14.29 MHz
5	12.25 MHz
6	11.11 MHz

The sampling speed (Fs) of the ADC is also limited by the number ADCs that can be connected to the PRU-ICSS. The ADS8688 can support clock speeds of up to 17 MHz while running at full throughput (500 ksps). Because this reference design uses six ADCs, according to 表 2, the maximum clock speed that can be used is 11.11 MHz. This design uses a 10-MHz data rate, which translates to a sampling speed of 256 ksps (32 ksps per channel) per ADC. For higher sampling speeds, compute the required clock rate from the data sheet of the ADC and use 表 2 to decide the number of ADCs that can be connected with the AM335x processor.

The PRU-ICSS implements an enhanced General-Purpose Input/Output (GPIO) module that supports direct input and direct output modes. PRU core register R30 serves as the interface for the general purpose outputs and register R31 for inputs. Any value written into register R30 of the PRU core will be output to the PRU's external pins a single cycle later. (R30 bit 0 corresponds to pin 0, bit 1 to pin 1, and so on.) Inversely, whenever the PRU core reads register R31, the values on the PRU core's external pins are stored a single cycle later. The value of pin 0 is stored in R31 bit 0, pin 1 into bit 1, and so on. Along with the direct input and output modes, the PRU's determinism allow it to be an ideal solution for implementing the simultaneous SPI for communicating with multiple ADCs in this use case.

図 7 shows the simultaneous SPI that has been configured in the PRU software. Shared chip select and SPI clock allow ADCs to acquire data simultaneously and at the same instance. Each ADC device has its own MISO and MOSI pins so that the ADC configurations and data can be sent and received in parallel.

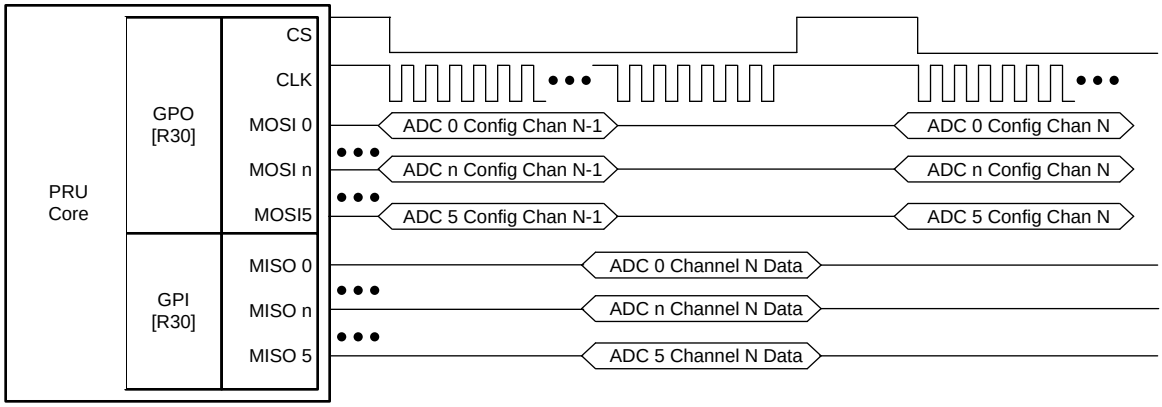

図 7. Interfacing Between ADC and PRU

2.3.1.2.1 Advantages of Using PRU-ICSS

This subsection showcases the benefits of using bit-banging in PRU-ICSS over dedicated hardware SPI peripheral.

表 3. Advantages of PRU-ICSS

PARAMETER	SPI	PRU-ICSS
Connections to slave	Fixed (1, 2, 4); depends on the product family SPI offering	Variable (1, 2, 3..n); depends on the configurations on the PRU GPIO
Flexibility with controlling the CS	If each SPI port has a dedicated CS then the phase delay between different SPI ports could introduce error in simultaneous sampling.	CS is an independent timing signal and hence can control all ADCs simultaneously with one common signal.
System bandwidth	More frequent CPU core interrupt as it needs to manage the DMA allocation and data transfer between SPI ports, memory, CPU due to shared resources.	CPU core interrupt is no longer required as both PRUs can run independently.
	This limits the overall sampling speed of ADCs when multiple SPI ports are used.	ADCs can run at higher sampling speed as the data is now transferred at much faster rate between multiple ADCs and PRU.
	The CPU core cannot do any data computation in parallel when being used for supervisory function.	The CPU core is now idle as second PRU is used for ZCD. The core can be used for post processing of data or for implementing other functionalities.

表 3. Advantages of PRU-ICSS (continued)

PARAMETER	SPI	PRU-ICSS
Timing compensation	In SPI peripherals, the relationship between clock edge and the arrival of data has to be tightly controlled (less than half CLK cycle). At higher speeds or with digital isolators, signal path delays could be significant to affect the timing criteria. This results in corrupted data that requires expensive hardware fixes or reduced throughput.	The PRU-ICSS subsystem is more relaxed as the delays in arrival of data beyond the CLK edge can be compensated due to a higher resolution internal time base (5 ns) for data capture.

2.3.1.3 Digital Filtering and Feedback (Implemented in PRU-0)

The simultaneous SPI interface is accomplished in only one of the two PRU cores in the PRU-ICSS. This frees up the other PRU core to provide a feedback loop for the incoming signal frequency (to adjust the ADC sampling rate for achieving coherent sampling) as well as perform low-level filtering on the incoming ADC data. Because the timing requirements on this PRU core is not as tight, the firmware is implemented in C code.

2.3.1.3.1 Coherent Sampling (Sample Rate Adjustment)

When measuring periodic signals, such as voltage and current in an AC system, it is important to acquire a fixed number of samples per cycle. When the frequency of the line cycle changes, sampling rate of the ADC is adjusted to maintain a fixed number of samples per cycle using a phase-locked loop circuit. In grid, methodology and admissible error that occur while measuring harmonic component is captured in IEC 61000-4-7. There are many ways of implementing PLL that could be done in either analog domain or digital domain. Non-coherent sampling results in spectral leakages leading to loss of data and reduction in accuracy as shown in 図 27.

In this reference design, the second PRU core performs frequency estimation by using a zero cross detection (ZCD) algorithm. Once the incoming frequency has been determined, the PRU can update the sampling rate of the acquisition PRU to achieve a precise number of samples per cycle across the full range of expected incoming frequencies (45 to 55 Hz). The ADC channel to be used for frequency estimation, as well as the number of cycles are both configurable in the PRU firmware.

In 図 27, a 45-Hz sine wave is provided to the ADC input. The top data is acquired at a fixed rate of 32000 samples per second (assuming a 50-Hz input signal and 640 samples per cycle). For the bottom data, the PRU is allowed to estimate the incoming signal frequency and then alter the sampling rate to achieve 640 samples per cycle. Notice that 1280 samples are exactly 2 periods of the signal and the FFT leakage rolls off very quickly in the bottom data.

2.3.1.3.2 Achievable Sampling Frequencies

Each PRU core in the PRU-ICSS runs at 200 MHz giving a cycle time of 5 ns. As mentioned before, the absolute determinism of the PRU cores allows the developer to control what happens on each and every cycle. Knowing this, the ADC sampling frequency can be determined which the PRU can achieve for each channel.

Before digging into the frequencies, a discussion on the use case requirements and techniques used to accomplish those requirements will be useful. This reference design has the following requirements:

- 45- to 55-Hz incoming frequency: Assumed frequency is 50 Hz with a worst case variation of ±10%
- 640 samples per cycle: Sampling rate must vary from 28.8 ksps to 35.2 ksps based on incoming

frequency

- 10-MHz SPI clock
- 48 ADC channels: Six ADCs are sampled in parallel, each with eight channels sampled sequentially

The ADCs that are chosen for this design trigger data acquisition when the Chip Select (CS) line is taken low. To change the sampling frequency of a channel, the time between CS falling edges must be increased or reduced. 図 8 shows an example of the SPI clock (SCLK) and CS lines that are shared between the six ADC devices. 図 8 shows the amount of time that CS remains low is fixed for each sample and the amount of time that CS remains high is varied to alter the sampling rate.

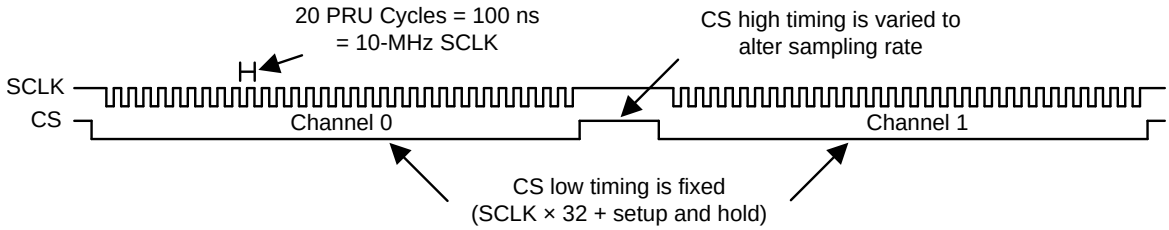

図 8. Timing Diagram Showing CS and CLK

Zooming out a bit, achieving a consistent sampling rate for a given channel is slightly complicated by the fact that each ADC provides data from eight channels sequentially. 図 9 shows that the period of channel 0 is actually determined by the first and eight falling edge of CS, and channel 7's period is determined by the 7th and 15th falling edge.

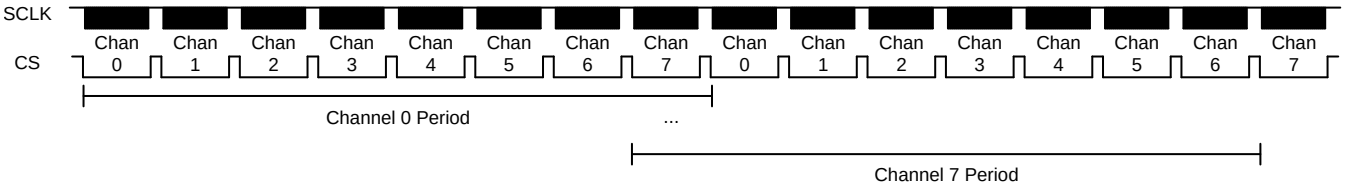

図 9. Overall Functioning of Timing Adjustments

This means that if a fixed delay is chosen between each CS, then any error is magnified by a factor of 8 for each channel. For instance, to achieve 640 samples per cycle per channel at a 50-Hz incoming frequency, it would theoretically require 781.25 PRU cycles between each falling CS:

- 50 Hz × 640 samples per cycle = 32 ksps per channel
- 32 ksps per channel × 8 channels = 256 ksps per device
- 1/256 ksps = 3906.25 ns between each sample
- 3906.25 ns / 5 ns = 781.25 PRU cycles (1 PRU cycle is 5 ns)

Because the PRU can only delay by an integer number of cycles, 781 cycles would be chosen and the actually sampling frequency would be ≈ 256,082 samples per device per second (≈ 32,010 samples per second for each channel). This error amount doubles if exactly 781.5 PRU cycles are needed for a different incoming frequency.

To overcome this error, and to improve the granularity of achievable sampling rates, a single PRU cycle of compensation delay can be added to a variable number of delay values (from 0 to 7 compensation cycles are available). 図 10 shows where the optional compensation would occur.

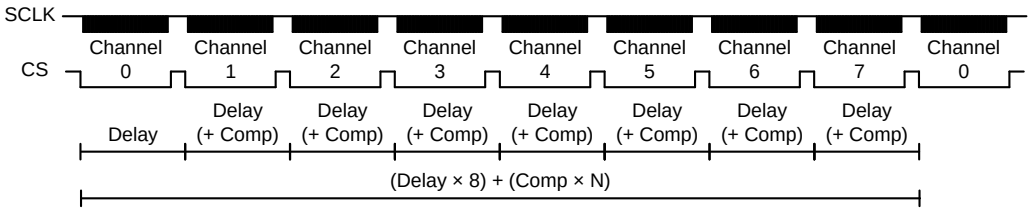

図 10. Timing of CS Across Multiple Channels of ADCs

Returning to the previous example where an exact 32 ksps per channel needs to be achieved, it is possible to introduce base delay of 781 PRU cycles and then add 1 cycle of compensation, which captures two of the six channels. This averages out to exactly 781.25 PRU cycles at each channel:

- 781 + 782 + 782 + 781 + 781 + 781 + 781 + 781 = 6250 PRU cycles
- 6250 / 8 = 781.25 PRU cycles
- 1 / (781.25 cycles × 5 ns) = 256 ksps
- 256 ksps / 8 channels = 32 ksps per channel

These compensation cycles allow the user to increase the frequency granularity by a factor of 8. Because the period of each channel encompasses eight samples, these compensation methods work across all eight channels. The only caveat introduced by having asymmetric delay samples between individual channels is that the delay between each individual channel's sample is no longer fixed. In this example, the delay between channel 0 and channel 1 is 781 cycles; however, the delay between channel 1 and channel 2 is 782 cycles.

After discussing the requirements and the techniques, the achievable sampling rates using the aforementioned methods can be shown. 表 4 covers the extremes of the input frequency range as well as the expected middle. This is meant to show the best, worst, and average cases. Notice that the resolution between the ideal input frequency at each sampling rate never exceeds 0.01 Hz.

表 4. Achievable Sampling Rates

DELAY CYCLES (5 ns)	COMPENSATION CYCLES (5 ns)	SAMPLING RATE PER CHANNEL (sps)	SAMPLING RATE PER DEVICE (sps)	IDEAL FREQUENCY AT SAMPLING RATE (Hz)	RESOLUTION FROM NEXT FREQUENCY (Hz)
710	0	35211.2676	281690.1408	55.0176	0.00968
710	1	35205.0695	281640.5562	55.0079	0.00968
710	2	35198.8736	281590.9891	54.9982	0.00968
710	3	35192.6799	281541.4394	54.9886	0.00967
710	4	35186.4884	281491.9071	54.9789	0.00967
710	5	35180.2990	281442.3923	54.9692	0.00967
710	6	35174.1119	281392.8948	54.9595	0.00966
710	7	35167.9269	281343.4148	54.9499	0.00966
…	…	…	…	…	…
781	0	32010.2433	256081.9462	50.0160	0.00800
781	1	32005.1208	256040.9666	50.0080	0.00800
781	2	32000.0000	256000.0000	50.0000	0.00800
781	3	31994.8808	255959.0466	49.9920	0.00800
781	4	31989.7633	255918.1062	49.9840	0.00799
781	5	31984.6474	255877.1790	49.9760	0.00799
781	6	31979.5331	255836.2648	49.9680	0.00799
781	7	31974.4205	255795.3637	49.9600	0.00799
…	…	…	…	…	…
868	0	28801.8433	230414.7465	45.0029	0.00648
868	1	28797.6962	230381.5695	44.9964	0.00648
868	2	28793.5502	230348.4020	44.9899	0.00648
868	3	28789.4055	230315.2440	44.9834	0.00647
868	4	28785.2619	230282.0956	44.9770	0.00647
868	5	28781.1196	230248.9567	44.9705	0.00647
868	6	28776.9784	230215.8273	44.9640	0.00647
868	7	28772.8384	230182.7075	44.9576	0.00647

2.3.1.3.3 Oversampling

Digital domain filtering is also performed by the second PRU in the form of an averaging filter. This filter achieves the same results as the oversampling function on more expensive ADCs. Oversampling the incoming data performs a low-pass filter and removes high-frequency noise before passing the data on to the next stop in the processing pipeline. The PRU core accumulates the samples from each channel as the data is coming in and then once the configurable oversampling factor is reached the division is performed to get the average value.

2.3.1.4 High-Level Data Processing (Implemented in Arm Core)

All of the data acquisition and low-level processing happens completely in the PRU-ICSS without requiring a single cycle from the Arm core. This allows the Arm core to focus on higher level processing and communications. In this reference design, the Arm core is running Texas Instrument's Processor SDK RT Linux distribution. This distribution of Linux comes with the PREEMPT_RT patch applied and allows for user space threads to be assigned priorities that can allow them to get (nearly) uninterrupted CPU cycles for short periods of time.

The user space application that is provided with this reference design creates two threads: one for processing the ADC data, and one for displaying the results from the processing. The thread that is responsible for processing the ADC data is assigned to the highest priority possible (99) so that it can get through its assigned tasks (and then sleep until the next set of data is ready) without missing a cycle of data. This processing thread iterates through each sample for each of the 48 channels, finds the minimum and maximum values, and calculates the RMS value for each cycle. At the end of the cycle, the thread converts the ADC codes into their respective voltages and then stores the values for each channel into a global array. This gives the other thread access to the minimum voltage, the maximum voltage, and the RMS value for each cycle from each of the 48 channels.

The other user space thread is created with the default (lower) priority and it is responsible for displaying the results to the console. Once every 250 ms, this thread wakes up, prints the latest calculated minimum, maximum, and RMS values for each channel to the console, and then goes back to sleep. Because this thread is a lower priority, it never blocks the processing thread from getting through its tasks. 図 11 shows a mockup of the console output.

```
Ch00 Vpp:[-5.345,5.354]     RMS:3.594  | Ch24 Vpp:[-5.345,5.354]     RMS:3.594
Ch01 Vpp:[-5.345,5.354]     RMS:3.594  | Ch25 Vpp:[-5.345,5.354]     RMS:3.594
Ch02 Vpp:[-5.345,5.354]     RMS:3.594  | Ch26 Vpp:[-5.345,5.354]     RMS:3.594
Ch03 Vpp:[-5.345,5.354]     RMS:3.594  | Ch27 Vpp:[-5.345,5.354]     RMS:3.594
Ch04 Vpp:[-5.345,5.354]     RMS:3.594  | Ch28 Vpp:[-5.345,5.354]     RMS:3.594
Ch05 Vpp:[-5.345,5.354]     RMS:3.594  | Ch29 Vpp:[-5.345,5.354]     RMS:3.594
Ch06 Vpp:[-5.345,5.354]     RMS:3.594  | Ch30 Vpp:[-5.345,5.354]     RMS:3.594
Ch07 Vpp:[-5.345,5.354]     RMS:3.594  | Ch31 Vpp:[-5.345,5.354]     RMS:3.594
Ch08 Vpp:[-5.345,5.354]     RMS:3.594  | Ch32 Vpp:[-5.345,5.354]     RMS:3.594
Ch09 Vpp:[-5.345,5.354]     RMS:3.594  | Ch33 Vpp:[-5.345,5.354]     RMS:3.594
Ch10 Vpp:[-5.345,5.354]     RMS:3.594  | Ch34 Vpp:[-5.345,5.354]     RMS:3.594
Ch11 Vpp:[-5.345,5.354]     RMS:3.594  | Ch35 Vpp:[-5.345,5.354]     RMS:3.594
Ch12 Vpp:[-5.345,5.354]     RMS:3.594  | Ch36 Vpp:[-5.345,5.354]     RMS:3.594
Ch13 Vpp:[-5.345,5.354]     RMS:3.594  | Ch37 Vpp:[-5.345,5.354]     RMS:3.594
Ch14 Vpp:[-5.345,5.354]     RMS:3.594  | Ch38 Vpp:[-5.345,5.354]     RMS:3.594
Ch15 Vpp:[-5.345,5.354]     RMS:3.594  | Ch39 Vpp:[-5.345,5.354]     RMS:3.594
Ch16 Vpp:[-5.345,5.354]     RMS:3.594  | Ch40 Vpp:[-5.345,5.354]     RMS:3.594
Ch17 Vpp:[-5.345,5.354]     RMS:3.594  | Ch41 Vpp:[-5.345,5.354]     RMS:3.594
Ch18 Vpp:[-5.345,5.354]     RMS:3.594  | Ch42 Vpp:[-5.345,5.354]     RMS:3.594
Ch19 Vpp:[-5.345,5.354]     RMS:3.594  | Ch43 Vpp:[-5.345,5.354]     RMS:3.594
Ch20 Vpp:[-5.345,5.354]     RMS:3.594  | Ch44 Vpp:[-5.345,5.354]     RMS:3.594
Ch21 Vpp:[-5.345,5.354]     RMS:3.594  | Ch45 Vpp:[-5.345,5.354]     RMS:3.594
Ch22 Vpp:[-5.345,5.354]     RMS:3.594  | Ch46 Vpp:[-5.345,5.354]     RMS:3.594
Ch23 Vpp:[-5.345,5.354]     RMS:3.594  | Ch47 Vpp:[-5.345,5.354]     RMS:3.594


Estimated Frequency:50.000 Hz

Press any key to exit
```

図 11. Typical Output on Console

2.3.1.5 Software Data Flow

図 12 illustrates each of the functions mentioned in the previous sections. Keep in mind that the AM335x SoC is:

- Implementing a simultaneous SPI to six eight-channel ADCs (which are generating ≈ 1,536 ksps)
- Performing oversampling on the data if requested
- Detecting zero crossing to estimate the frequency and fine-tune the sampling rate
- Storing the samples in DDR memory
- Retrieving each sample and calculating the minimum, maximum, and RMS values for every single cycle for each of the 48 ADC channels
- Displaying the data for each channel with a 250-ms update rate

All of this processing is happening continuously and the Arm CPU usage reported by the "top" utility is only at ≈ 40%.

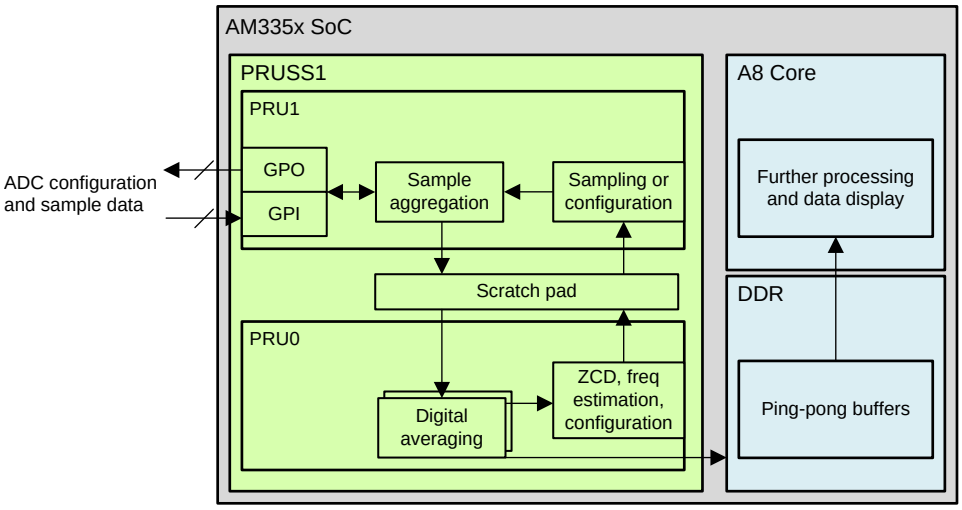

図 12. Software Data Flow Diagram

2.3.2 Analog Signal Conditioning

To meet the performance of a 16-bit SAR ADC at the maximum sampling rate (500 kSPS), the sample and hold capacitors at the input of the ADC must be successfully charged and discharged during the acquisition-time window. This drive requirement at the inputs of the ADC requires the use of a high bandwidth, low-noise, and stable amplifier buffer. Such an input driver is integrated in the front-end signal path of each analog input channel of the device. During transition from one channel of the multiplexer to another channel, the fast integrated driver ensures that the multiplexer output settles to 16-bit accuracy within the acquisition time of the ADC regardless of the input levels on the respective channels. The OPA4197 drives the analog input signals to the ADS8688 which provides wide bandwidth (GBW: 10 MHz) and low noise (5.5 nV/√Hz).

Any higher frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum. To avoid this, an antialiasing filter is realized using a second-order Sallen-Key Filter with unity gain removing any high-frequency components from the input signal.

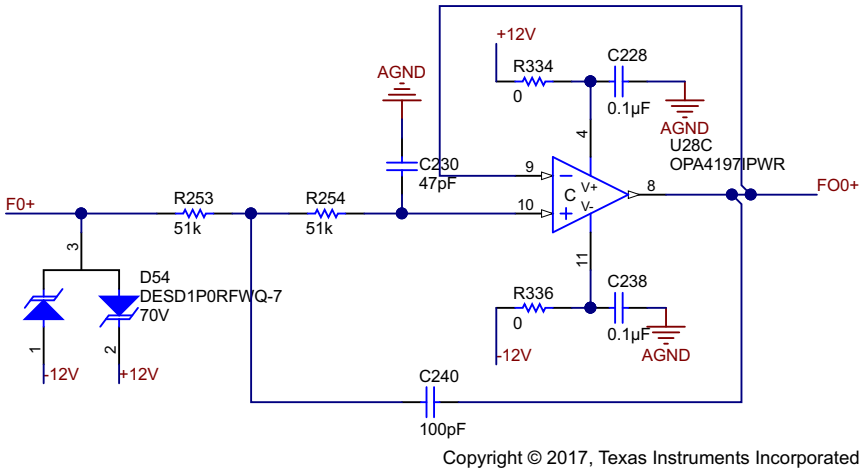

図 13. Schematic of Interfacing With Sensor Boards

2.3.3 ADC

The ADC is configured to use an internal reference of 4.096 V with a ±10.24-V input range for each channel while the analog supply is set for 5 V and digital supply for 3.3 V. A RC filter of 20 kHz is used for all the input channels.

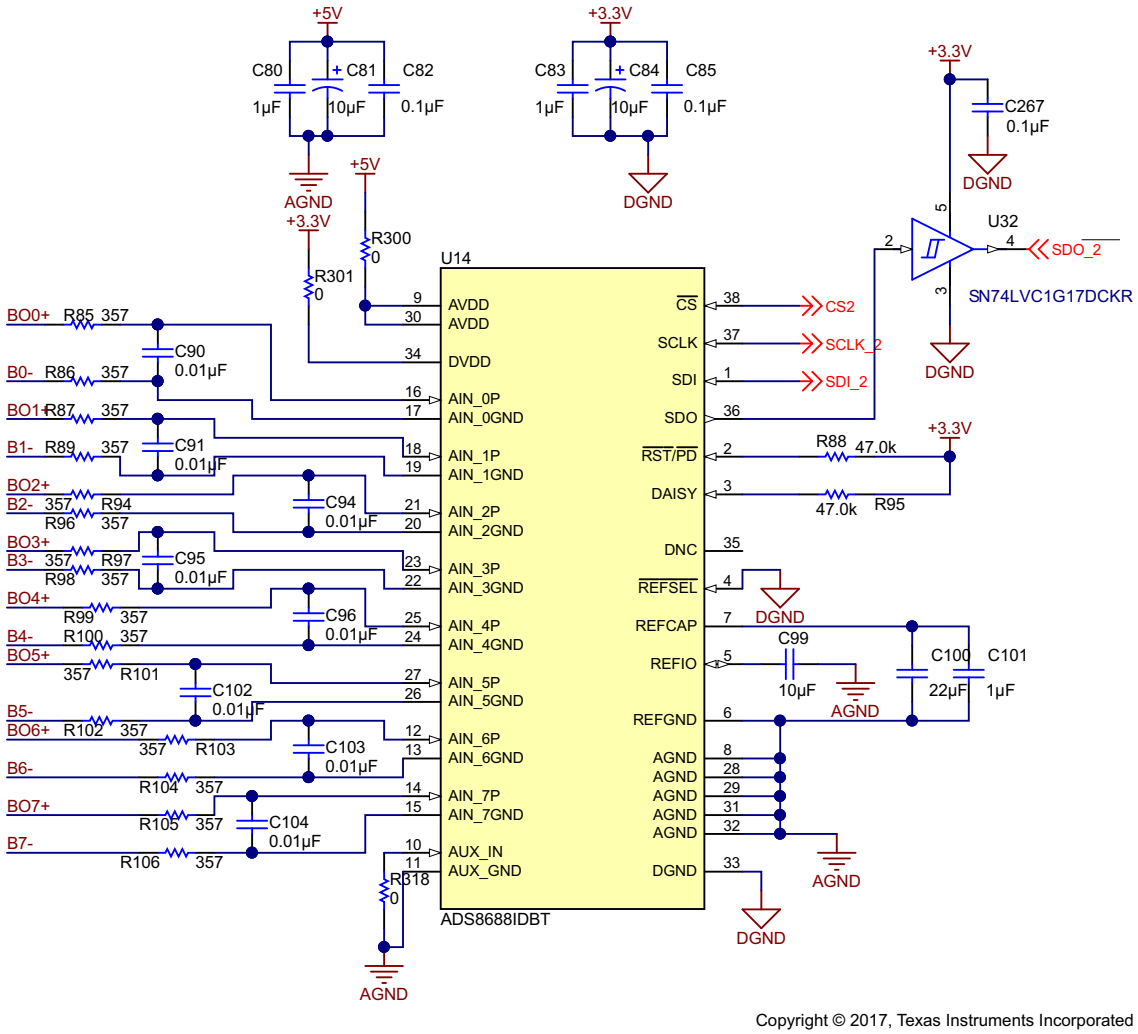

図 14. Schematic of Configurations for ADS8688

In this reference design, the CS for all the six ADCs are tied together to acquire data simultaneously across all the devices. A non-inverting buffer is used as shown in 図 15.

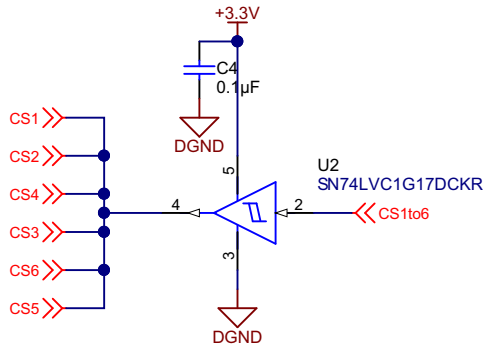

図 15. Schematic of Buffering Common Chip Select Across Multiple ADCs

For highest AC performance from the data acquisition, it is very critical to provide clock to each and every ADCs with low additive litter and low skew. The CDCLVC1106 is compatible with a 3.3-V supply and operates up to 250 MHz of clock. A pin-to-pin skew of less than 50 ps and additive jitter of less than 100 fs make the CDCLVC1106 good candidate for fanning out clock to all of the six ADS8688 devices. 図 16 shows the typical schematic for the interface of the clock buffer.

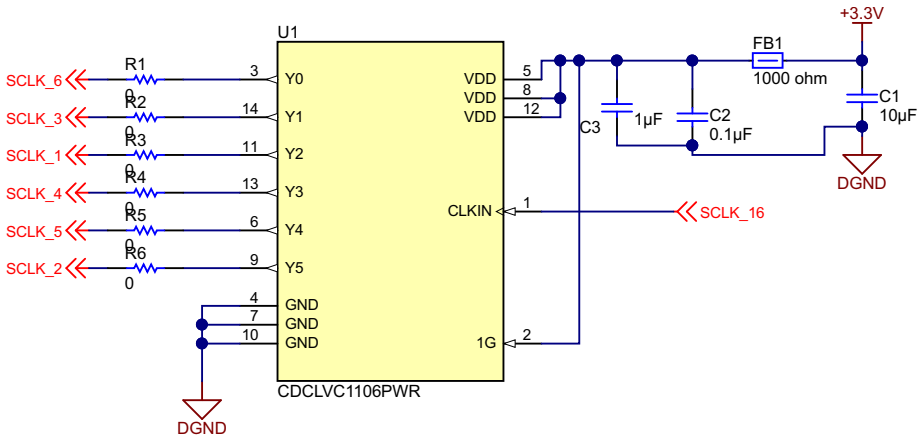

図 16. Schematic of Clock Buffer

2.3.4 Power Supply

Analog signal conditioning and data conversion require a power supply with multiple voltage levels. The ADS8688 requires a 5-V supply at the AVDD and uses 3.3 V for the digital interface at DVDD pin.

- 5-V AVDD: The ADS8688 requires a maximum of 16 mA at the 5-V supply and for maximum data throughput. For six ADCs, the total current requirement is approximately 96 mA.
- 3.3-V DVDD: Dynamic digital requirement for the current supply is typically 0.5 mA for one ADS8688 device. Including the digital buffer and LED indicators, the overall supply current required is around 50 mA.
- ±12-V AVcc: This is required to power up the AFE to condition the input signals feeding to ADCs. The OPA4197 drive the input signals and needs up to 1.5 mA per amplifier summing up to 72 mA for all the 48 channels.

  Based on these power requirements, the power tree for the system is designed as shown in 図 17.
- Load switch: This is used at the front end of the power supply to disable power supply to the whole board when OE is deactivated. OE is a GPIO connected to the Sitara processor to enable and power up the data acquisition board. This connection helps prevent any GPIO from getting pulled high or low when Sitara is not powered up providing fail-safe operation.

A single supply of 5.5 V is used to derive multiple voltage levels using power converters and LDOs as shown in 図 17. The TPS65131 generates both positive and negative voltage outputs from a single supply. This converter has internal boost converter control to step up the input voltage and an inverting converter control to derive negative voltage. External passives are designed to obtain ±14 V from the input.

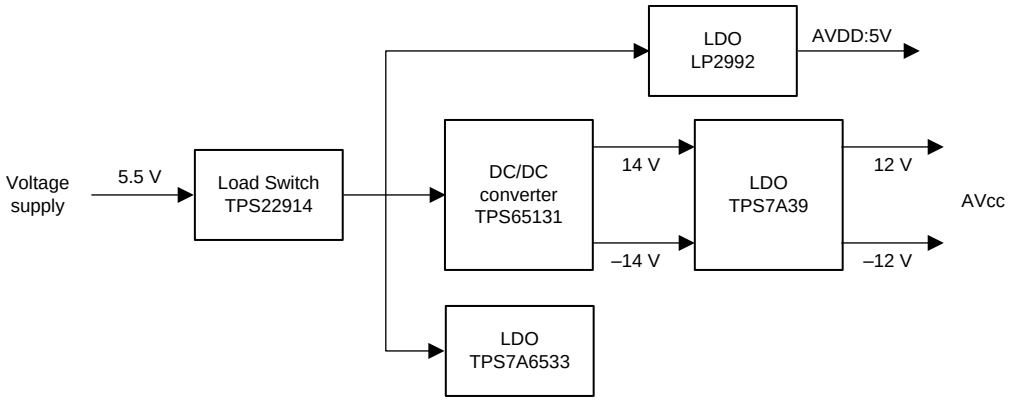

図 17. Power Tree for Data Acquisition

This converter is followed by a dual-channel LDO, the TPS7A39, consisting of a positive and negative LDO in a single package to simplify the system design. Regulator outputs can be independently adjusted and externally adjusted to obtain ±12 V as shown in 図 19.

The LP2992 LDO voltage regulator provides a fixed 5-V analog voltage supply required by the ADCs. Benefits of this device include ultra-low-dropout and low-noise regulators. For digital power supply of 3.3 V, the TPS7A6533 LDO regulator has been used.

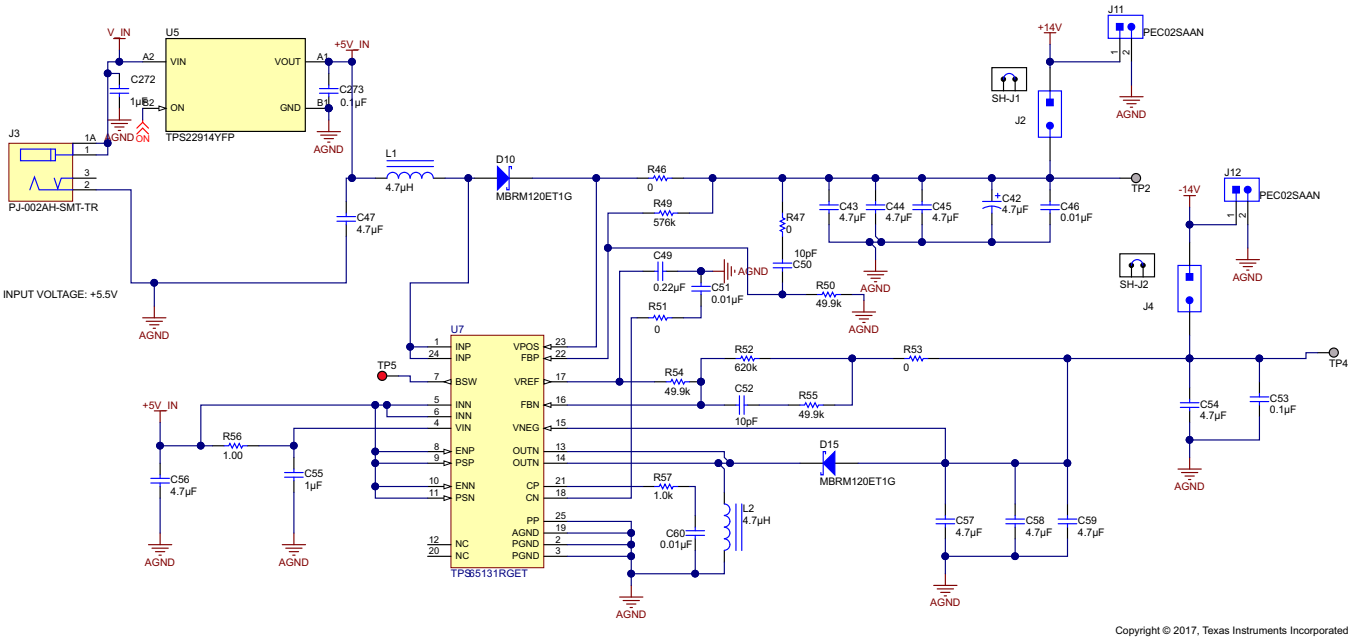

図 18. Schematic of Front-End DC/DC Converter Using TPS65131

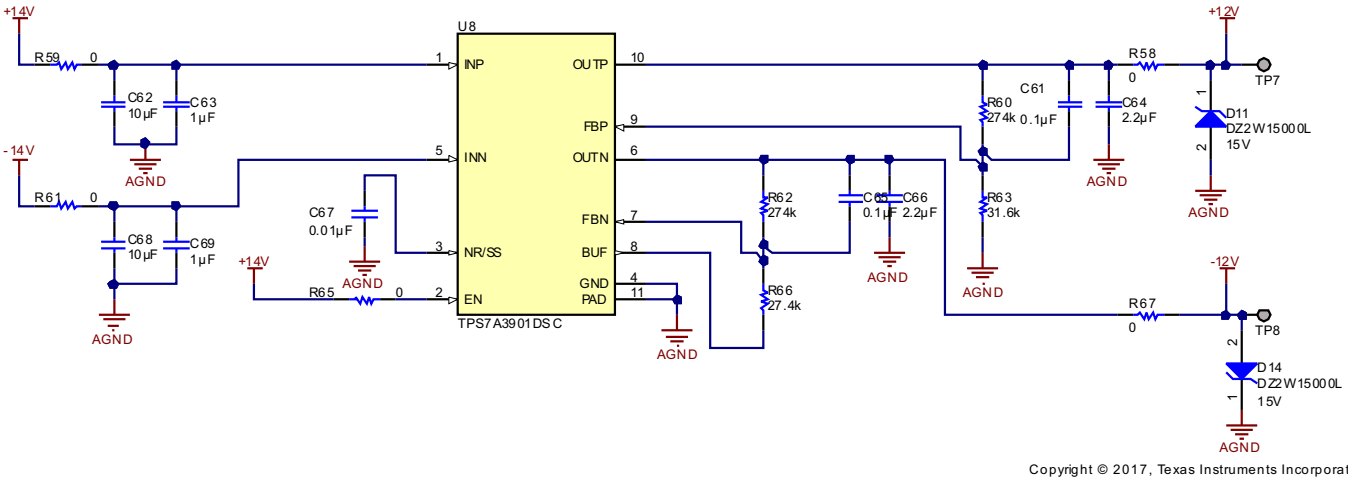

図 19. Schematic of Configuration for Dual-Channel LDO

2.3.5 Voltage and Current Sensing

PTs measures voltage and provide isolation. In this reference design, the PT120CF transformer measures up to 120-V AC RMS with 4 kV of isolation. Similarly, for high current measurement, the CR8450-1000 transformer measures the peak current measurement of 70-A AC RMS with linearity.

3 Hardware, Software, Testing Requirements, and Test Results

This section provides information on connecting this reference design for functional and performance testing.

3.1 Required Hardware and Software

3.1.1 Hardware

The hardware setup for this reference design consists of four boards, including the BeagleBone Black board. Analog signals can be either directly connected at the connectors on the data acquisition interface or through the sensor board where external voltage and current sensors can be connected. External PTs and CTs are connected on the sensor board feeding outputs for measuring higher voltages and currents with isolation. The interface connector on the AFE board is connected to the BeagleBone Black EVM through the adaptor card. 図 20 shows an overall setup for the interconnection.

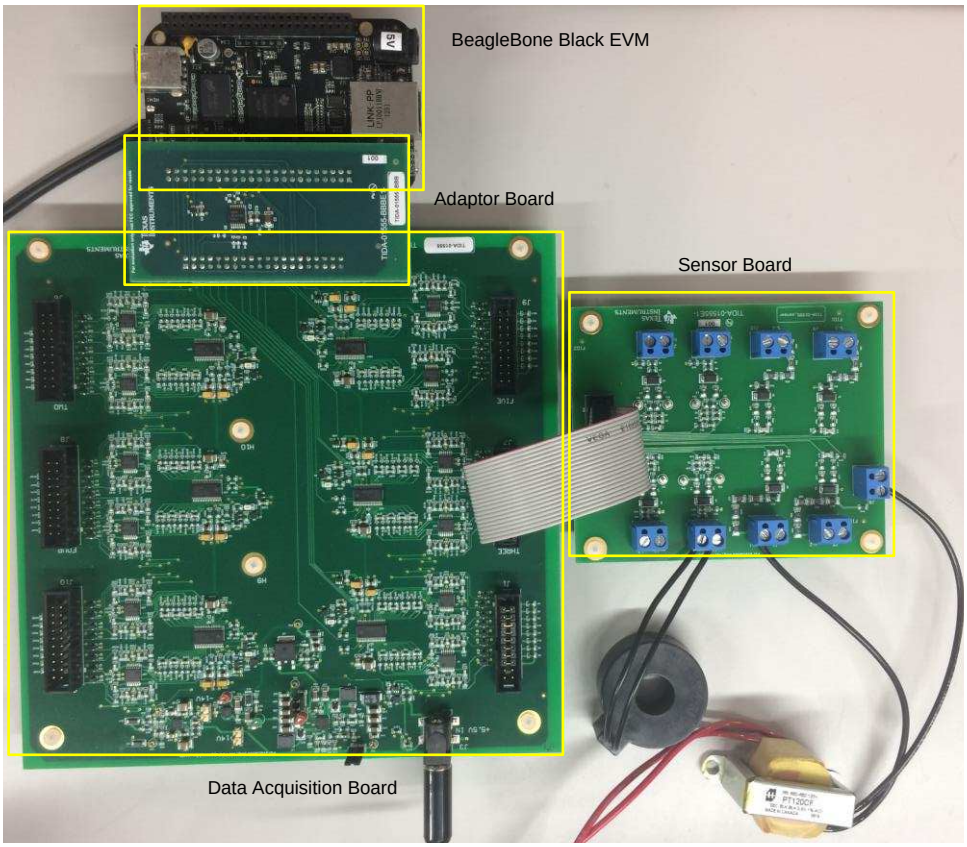

図 20. PCB Interconnection for TIDA-01555

This reference design can capture data from 48 analog channels by feeding signals to the six connectors on the AFE board. Each of these connectors can be fed from the sensor board, which can connect to four voltage and four current inputs through external PTs and CTs. 表 5 details the connectors on the sensor board.

表 5. Details of Connectors on Sensor Board

CONNECTOR	DESCRIPTION	CONNECTOR	DESCRIPTION
J8	Voltage reference (N)	J5	Connector to data acquisition interface
J6	Phase-1 voltage (V1)	J1	Phase-1 current (I1)
J7	Phase-2 voltage (V2)	J2	Phase-2 current (I2)
J9	Phase-3 voltage (V3)	J3	Phase-3 current (I3)
J10	Phase-4 voltage (V4)	J4	Phase-4 current (I4)

表 6 details the connectors on the AFE board where analog inputs for all the 48 channels can be given. This board can be operated from a single power supply of 5.5 V at the connector J3. There is a provision to supply an external ±14 V for the data acquisition card.

表 6. Connector Details for Data Acquisition Board

CONNECTOR	DESCRIPTION	CONNECTOR	DESCRIPTION
J1	Signals from Sensor Board-1	J3	Power supply input
J6	Signals from Sensor Board-2	J5	Connector to adaptor board
J7	Signals from Sensor Board-3	J11	Option for external 14-V supply
J8	Signals from Sensor Board-4	J12	Option for external –14-V supply
J9	Signals from Sensor Board-5	J10	Signals from Sensor Board-6

This reference design provides multiple test points for probing the voltages at different stages for debugging purposes. 表 7 lists the different available test points.

表 7. Test Points on Data Acquisition Board

TEST POINTS	DESCRIPTION	TEST POINTS	DESCRIPTION
TP1	5-V AVDD	TP5	Pin for external battery switch
TP2	14 V	TP6	3.3-V DVDD
TP3	AGND	TP7	12 V
TP4	–14 V	TP8	–12 V

Analog inputs for an individual ADS8688 is mapped onto separate connectors with a provision for feeding differential analog signal for all the eight inputs of the ADC as given in 表 8.

表 8. Connector Interfacing Sensor Board and AFE Board

PIN NO	DESCRIPTION	PIN NO	DESCRIPTION
1	AIN5+	2	AIN5-
3	AIN4+	4	AIN4-
5	AIN3+	6	AIN3-
7	AIN2+	8	AIN2-
9	AIN1+	10	AIN1-
11	AIN0+	12	AIN0-
13	AIN7+	14	AIN7-
15	AIN6+	16	AIN6-
17	AGND	18	AGND
19	12 V	20	–12 V

All the digital interfaces to the ADS8688 through serial communication are available at a single connector, which is connected to the Sitara processor through an adaptor board in between. 表 9 details the connector pins that interfaces the AFE board and the adaptor board.

表 9. Connector Interfacing AFE Board and Adaptor Board

PIN NO	DESCRIPTION	PIN NO	DESCRIPTION
1	SDI-1	2	SDI-2
3	CS-1	4	CS-2
5	SCLK-1	6	SCLK-2
7	SDO-1	8	SDO-2
9	DGND	10	DGND
11	SDI-3	12	SDI-4
13	CS-3	14	CS-4
15	SCLK-3	16	SCLK-4
17	SDO-3	18	SDO-4
19	DGND	20	DGND
21	SDI-5	22	SDI-6
23	CS-5	24	CS-6
25	SCLK-5	26	SCLK-6
27	SDO-5	28	SDO-6
29	DGND	30	DGND
31	DGND	32	DGND
33	OUTPUT ENABLE	34	+3.3V
35	AGND	36	AGND
37	AGND	38	AGND
39	12 V	40	–12 V

When connecting the AFE to the BeagleBone Black EVM, CS and CLK for all the six ADS8688 devices are tied together, and the intermediate buffer is provided on the adaptor board. The connector on the adaptor board is configured to connect with P8 on the BeagleBone Black EVM and the corresponding pin details are provided in 表 10.

表 10. Connector Interfacing Adaptor Board With BeagleBone Black

PIN NO	SIGNAL	PIN NO	SIGNAL
P8.40	SDI-1	P8.45	SDO-1
P8.46	SDI-2	P8.46	SDO-2
P8.27	SDI-3	P8.43	SDO-3
P8.29	SDI-4	P8.44	SDO-4
P8.30	SDI-5	P8.41	SDO-5
P8.21	SDI-6	P8.42	SDO-6
P8.39	CS	P8.20	SCLK
P8.16	Output enable		

3.1.2 Software

3.1.2.1 Software Requirements

To use the demo software provided with this reference design, the user must have the RT Linux Processor SDK for the AM335x device.

- AM335x RT Linux Processor SDK v05.01.00.11 or newer

3.1.2.2 AM335x RT Linux Processor SDK Installation

This reference design is written using a 64-bit version of an Ubuntu 14.04 LTS host machine.

- Linux Processor SDK download page: Processor SDK Download Page
- Installation instructions: Processor SDK Linux Installer
- Processor SDK Linux Getting Started Guide

3.1.2.3 TIDA-01555 PRU ADC Demo Software

The demo software for this reference design can be found in the 'example-applications/pru-adc-x.y/' directory of the Processor SDK Linux installation. This directory contains the source files for the PRU firmwares, the user space application, and the device tree file.

3.1.2.4 Running the Demo

All software and binaries needed to run the demo are included out of the box in the RT Linux Processor SDK filesystem. When the board is booted with the default kernel and filesystem, the following steps can be used to run the demo:

1. Change to the pre-built PRU ADC device tree to configure the required pin muxing.

```
# cd /boot
# cp am335x-boneblack.dtb am335x-boneblack.dtb.orig
# cp am335x-boneblack-pru-adc.dtb am335x-boneblack.dtb
```

2. Link the PRU ADC firmware binaries to the symbolic links, so they are loaded when the PRU starts up.

```
# cd /lib/firmware
# ln -sf /lib/firmware/pru/PRU_ADS8688_Controller.out am335x-pru0-fw
# ln -sf /lib/firmware/pru/PRU_ADS8688_Interface.out am335x-pru1-fw
```

3. Reboot the EVM to let the updated device tree take affect.

```
# reboot
```

4. Execute the provided script to load the PRUs and start the Arm binary.

```
# run-pru-adc.sh
```

These steps are also documented online on the Linux Processor SDK Application Demos page here: PRU-ADC Demo.

3.1.2.5 Rebuilding from Source

The source files and utilities to build them are provided in the Linux Processor SDK installation package. The following sections have instructions on how to rebuild the demo from source.

3.1.2.5.1 Compile the Device Tree to Configure Pin Muxing

A device tree include file that configures the demo pin muxing and reserves a block of DDR memory is provided in the Linux Processor SDK kernel source files at: ${RT Linux Processor SDK Install Path}/board-support/linux-xx.xx.xx/arch/arm/boot/dts/am335x-pru-adc-dtsi. To change the PRU pin muxing or the location of the reserved memory, open this file and make the desired changes. When the changes are complete, the top-level SDK Makefile can be used to rebuild the device tree.

```
# cd ${RT Linux Processor SDK Install Path}
# make linux-dtbs
```

The newly rebuilt device tree is located in the kernel source at: ${RT Linux Processor SDK Install Path}/board-support/linux-xx.xx.xx/arch/arm/boot/dts/am335x-boneblack-pru-adc.dtb.

3.1.2.5.2 Compiling the Arm User Space Binary and PRU-ICSS Firmwares

To compile the Arm binary and the two PRU firmwares required to run the demo, use the SDK top-level Makefile. The source files for the demo are found in the example-applications/pru-adc-x.y/ directory of the Linux Processor SDK installation folder. Make any desired changes to the source files, then rebuild with the top-level Makefile.

```
# cd ${RT Linux Processor SDK Install Path}
# make pru-adc
```

注: This top-level file Makefile calls Makefiles in each project folder, which can be called directly to rebuild each binary separately.

If nothing is missing, the binaries are located in the newly created gen folder inside each of the three project folders:

- Arm user space application binary: example-applications/pru-adc-x.y/ARM_User_Space_App/gen/Arm_User_Space_App.out
- PRU-ICSS core 0 firmware binary: example-applications/pru-adc-x.y/PRU_ADS8688_Controller/gen/PRU_ADS8688_Controller.out
- PRU-ICSS core 1 firmware binary: example-applications/pru-adc-x.y/PRU_ADS8688_Interface/gen/PRU_ADS8688_Interface.out

3.1.2.5.3 Copying Files to the File System of the Board

When all device trees, binaries, and firmwares have been built, move them to the file system of the BeagleBone Black running the RT Linux Processor SDK Linux distribution.

- Device Tree – The device tree (am335x-boneblack-pru-adc.dtb) created in 3.1.2.5.1 must be placed in the /boot/ directory of the BeagleBone Black's file system.
- Arm Binary – The Arm binary (Arm_User_Space_App.out) created in 3.1.2.5.2 must be renamed to 'pru-adc-arm-app.out' and placed in the /usr/bin/ directory of the BeagleBone Black's file system.
- PRU Firmwares – The PRU firmwares (PRU_ADS8688_Controller.out and PRU_ADS8688_Interface.out) created in 3.1.2.5.2 must be copied to the /lib/firmware/pru/ directory of the BeagleBone Black's file system.

When these updated files have been moved to the file system, the steps in 3.1.2.4 can be followed to run the demo.

3.2 Testing and Results

3.2.1 Functional Tests

- Power tree: Before testing for performance, the data acquisition board is powered up by giving the 5.5-V supply at the input. Voltage at different test points are measured to validate the ±12 V, +5 V and +3.3 V rails.
- Analog driver: Using a function generator, AFE of the board is tested by giving AC voltage of less than a ±10-V peak at the analog input pins. This is to verify voltages going at the input of ADS8688 and functioning of analog driver for the same.
- Sensor board: Functioning of the sensor board is verified by connecting CTs and PTs at the corresponding connectors. Voltage at the input of PT is swung up to 120-V AC RMS to make sure output of the sensor board is within the input voltage range of ±10.24 V. Similarly, on the CT, input current is given up to 70 A RMS to validate the output of the board is limited within the range of the ADC.
- ADS8688: To verify how the AFE and ADS8688 boards function, the test setup shown in 図 21 is used where the ADS8688EVM along with a simple capture card (SDCC) evaluate the performance of an individual ADC.
  - DC performance: By shorting the input signal connector on the AFE board, DC performance of the ADC is captured using the graphical user interface (GUI) through a USB interface. The histogram analysis provides a mean ADC value, code spread, sigma (standard deviation), and the peak value for zero input.
  - AC performance: For an FFT analysis using GUI, an external function generator is used to generate a sine wave of fixed frequency and amplitude less than the input voltage range of the ADS8688 that is being set on the GUI configuration. The GUI provides AC performance of the analog signal chain and the ADS8688 by providing key dynamic parameters such as signal-to-noise ratio (SNR), total harmonic distortion (THD), signal-to-noise and distortion ratio (SINAD), and spurious-free dynamic range (SFCR).

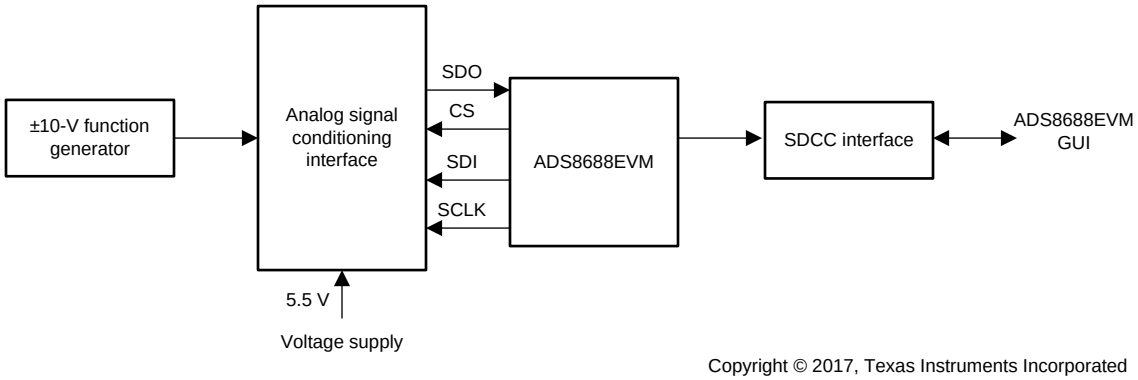

図 21. Test Setup for Functional Testing of Data Acquisition Board

3.2.2 Performance Tests

3.2.2.1 Test Setup

To evaluate the performance of this reference design as shown in 図 22, use the following:

- AC voltage and current source (120-V AC RMS and 70-A AC RMS)
- External CTs (CR8450-1000) and PTs (PT120CF)
- Sensor board (TIDA-01555)
- Data acquisition board (TIDA-01555)
- Interface adaptor board (TIDA-01555)
- BeagleBone Black EVM
- 5.5-V power supply (up to 500 mA)

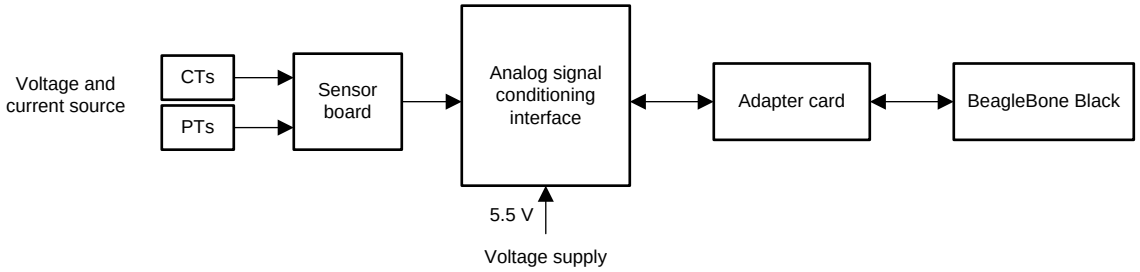

図 22. Test Setup for Performance Testing

3.2.2.2 DC Performance

To evaluate the DC performance of this reference design, instead of connecting inputs from the sensor boards, short the analog input terminals for all the 48 channels. The AFE board is connected to the BeagleBone Black EVM through the interface adaptor. The PRU on the AM335x is programmed to interface with all the six ADS8688 devices to capture data from all the channels. The input voltage range for the ADC is set to ±2.5 × V_{REF}, which is ±10.24 V. Each ADC is configured to sample at 256 ksps, which corresponds to 32 ksps per channel. Data across all 48 channels are being collected for 1 second and analyzed. Parameters such as minimum, maximum, code spread, and mean code are calculated for all the channels to show the DC performance of the entire data acquisition system as given in 表 11. Most of the channels have code spread of less than 4 with standard deviation of 0.5 to 0.58 across the channels. 図 23 shows a DC histogram for one of the channels.

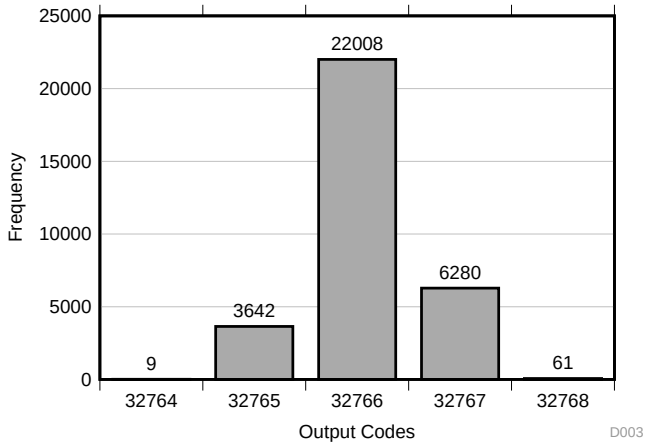

図 23. DC Histogram for One Channel: Sigma = 0.55, Code Peak = 32766

表 11. DC Performance of Data Acquisition

CH. NO.	MINIMUM CODE	MAXIMUM CODE	CODE SPREAD	MEAN CODE	CH. NO.	MINIMUM CODE	MAXIMUM CODE	CODE SPREAD	MEAN CODE
0	32764	32768	4	32766	24	32765	32769	4	32766
1	32764	32768	4	32766	25	32765	32769	4	32766
2	32764	32768	4	32765	26	32766	32770	4	32767
3	32764	32768	4	32765	27	32767	32771	4	32768
4	32764	32768	4	32766	28	32766	32770	4	32767
5	32764	32768	4	32766	29	32766	32770	4	32768
6	32765	32769	4	32766	30	32765	32768	3	32766
7	32766	32769	3	32767	31	32766	32769	3	32767
8	32766	32770	4	32768	32	32764	32768	4	32765
9	32766	32769	3	32767	33	32764	32768	4	32766
10	32765	32769	4	32766	34	32766	32770	4	32767
11	32766	32770	4	32767	35	32765	32769	4	32766
12	32766	32769	3	32767	36	32763	32767	4	32764
13	32765	32769	4	32766	37	32763	32767	4	32765
14	32764	32768	4	32766	38	32766	32770	4	32767
15	32764	32768	4	32766	39	32765	32769	4	32767
16	32764	32767	3	32765	40	32766	32769	3	32767
17	32766	32770	4	32767	41	32763	32767	4	32764
18	32765	32769	4	32767	42	32767	32771	4	32769
19	32764	32768	4	32765	43	32766	32769	3	32767
20	32764	32768	4	32766	44	32763	32767	4	32765
21	32764	32768	4	32766	45	32764	32769	5	32766
22	32765	32769	4	32766	46	32765	32768	3	32766
23	32764	32767	3	32765	47	32764	32768	4	32766

3.2.2.3 AC Performance

To test the board for accuracy of AC signals, a variable voltage and current source are connected at the input of the PTs and CTs. 図 22 shows the setup used to sweep the input voltage and current signals. The frequency of the input voltage and current is set to 50 Hz. For every line cycle, 640 samples are collected for each channel through SPI. The ping-pong buffer stores the data corresponding to one cycle from all the 48 channels. RMS value is being calculated for using this data for every cycle and stored in a buffer. Input AC voltage is varied from 2.5-V to 120-V RMS and the measurement accuracy has been captured in 図 24 and 表 12. This error includes total error of the system including non-linearity of the PTs.

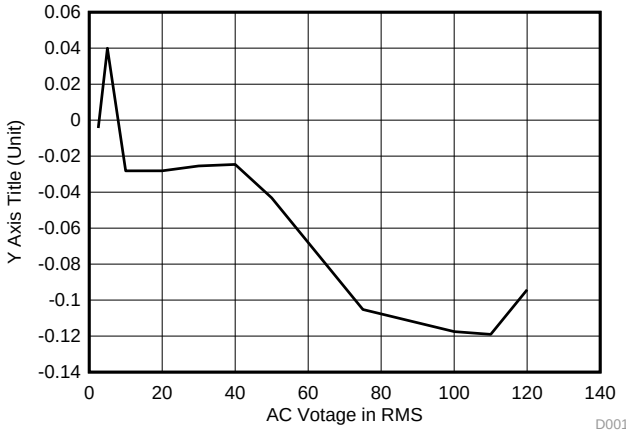

図 24. Performance of DAQ for AC Voltage Measurement

表 12. Accuracy of AC Voltage Measurement

VOLTAGE (V_{RMS})	APPLIED VOLTAGE (V_{RMS})	MEASURED VOLTAGE AT ADC (V_{RMS})	MEASURED VOLTAGE AFTER CALIBRATION (V_{RMS})	% ERROR
2.5	2.477	0.1028	2.4771	–0.0044
5	5.002	0.2075	5.0000	0.0400
10	10.002	0.4152	10.0048	–0.0282
20	20.0016	0.8303	20.0072	–0.0281
30	30.002	1.2454	30.0096	–0.0255
40	40.0022	1.6605	40.0120	–0.0246
50	50.0025	2.076	50.0241	–0.0432
75	75.003	3.1159	75.0819	–0.1052
100	100.003	4.155	100.1205	–0.1175
110	110.004	4.5706	110.1349	–0.1190
120	120.005	4.9849	120.1181	–0.0942

Similarly, measurement accuracy for current is captured by varying the input current from 2.5 A to 70 A RMS. 図 25 and 表 13 show the overall accuracy measurement, which is found to be less than ±0.11%.

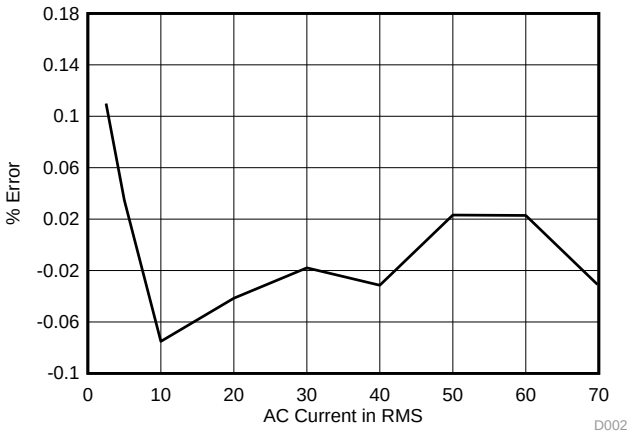

図 25. Performance for Capturing AC Current

表 13. Accuracy of AC Current Measurement

CURRENT (A_{RMS})	APPLIED CURRENT (A_{RMS})	MEASURED CURRENT AT ADC (A_{RMS})	MEASURED CURRENT AFTER CALIBRATION (A_{RMS})	% ERROR
2.5	2.50072	0.2463	2.4980	0.1099
5	5.00072	0.4929	4.9990	0.0347
10	10.0006	0.9868	10.0081	–0.0751
20	20.0069	1.9735	20.0152	–0.0416
30	30.0078	2.9593	30.0132	–0.0179
40	40.0077	3.946	40.0203	–0.0315
50	50.0055	4.9294	49.9939	0.0232
60	60.0056	5.9152	59.9919	0.0229
70	70.002	6.9044	70.0243	–0.0319

3.2.2.4 Simultaneous Sampling Between ADCs

In this design, all the six ADCs have a common CS signal. Sampling delay between n^{th} channel of all the ADCs will be minimal. For example, CH0 of ADC1, CH0 of ADC2, and CH0 of ADC6 must have a very small delay between sampling. This delay is verified by performing the following test:

- Configure all the ADCs to sample only first channel of its input (that is, CH0). This results in higher throughput and smaller conversion time.
- Apply an input signal of 50 Hz to CH0 of all the ADCs.
- Configure the ADCs to capture at full speed of 256 ksps for each ADS8688.
- Capture the data from each ADC for 1 second, which results in 256k samples for each input channel.
- Compare the ADC sample number corresponding to maximum value and minimum value in two ADCs.

表 14 shows the output value from two ADCs near the minimum and maximum values captured along with the sample number. From both of these values, there is a delay of one sample and half sample cycle in these two cases. From the experiment, the maximum delay between two channels is no more than 1 sample cycle, which is 3.9 µs.

表 14. Sample Numbers Around Peak Values for Two ADCs

SAMPLE NUMBER	OUTPUT FROM CH-0 OF ADC-1	OUTPUT FROM CH-0 OF ADC-2	SAMPLE NUMBER	OUTPUT FROM CH-0 OF ADC-1	OUTPUT FROM CH-0 OF ADC-2
525	1893	1897	3087	63595	63593
526	1893	1897	3088	**63596**	63593
527	1893	1896	3089	**63596**	**63594**
528	**1892**	1896	3090	**63596**	**63594**
529	**1892**	1896	3091	**63596**	**63594**
530	**1892**	**1895**	3092	63595	63593
531	1893	1896	3093	63594	63592

3.2.2.5 Coherent Sampling

In this reference design, input frequency is estimated by detecting zero crossing of the input signal. This detection is implemented on the second PRU core, which counts the number of zero crossings of the signal captured at a user specified channel. In this example, the core captures time taken for 10 zero crossings, which corresponds to five line cycles. Based on this computation, the PCU can update the sampling rate of acquisition on the first PRU to precisely adjust the CS to achieve fixed number of samples in spite of variations in the line cycle.

To validate the functioning of coherent sampling, logic analyzer is plugged on to the CS pin and voltage is fed from a function generator to the corresponding channel, which is programmed to detect frequency and zero crossing. Initially, the input signal is set to 50 Hz, which results in an overall conversion time of 3.91 µs, or 255.8 kHz (50 Hz × 640 samples × 8 channels). When the input signal frequency is changed to 45 Hz, the frequency of the CS signal also changes accordingly to 4.34 µs, or 230.4 kHz (45 Hz × 640 samples × 8 channels). 図 26 shows the transition between two situations.

図 26. Adjusting CS for Coherent Sampling

図 27 demonstrates the improvement in the AC performance of data acquisition due to coherent sampling. In the initial setup, coherent sampling is disabled and the sampling rate is fixed to 256 ksps, which results in 640 samples per cycle when the input frequency is 50 Hz. A sampling window of 1920 samples is used to analyze FFT. In this analysis, an input voltage of 45 Hz is given to one of the analog channels and the data is being captured. Time samples of the ADC output is plotted on the left side and FFT plot on the right-hand side of 図 27.

When the coherent sampling is disabled, fewer than three cycles are captured on the given sampling window as shown in the right-top plot, and the corresponding FFT plot is shown next to it. With the coherent sampling enabled, PRU can able estimate the input frequency by looking at the zero crossings. This adjusts the CS to achieve a fixed 640 samples per cycle in spite of any variations in the input frequency, which is evident in the bottom plot of 図 27. Exactly two cycles are captured in a sampling window of 1920 samples, which results in an improved FFT plot with reduced spectral leakage.

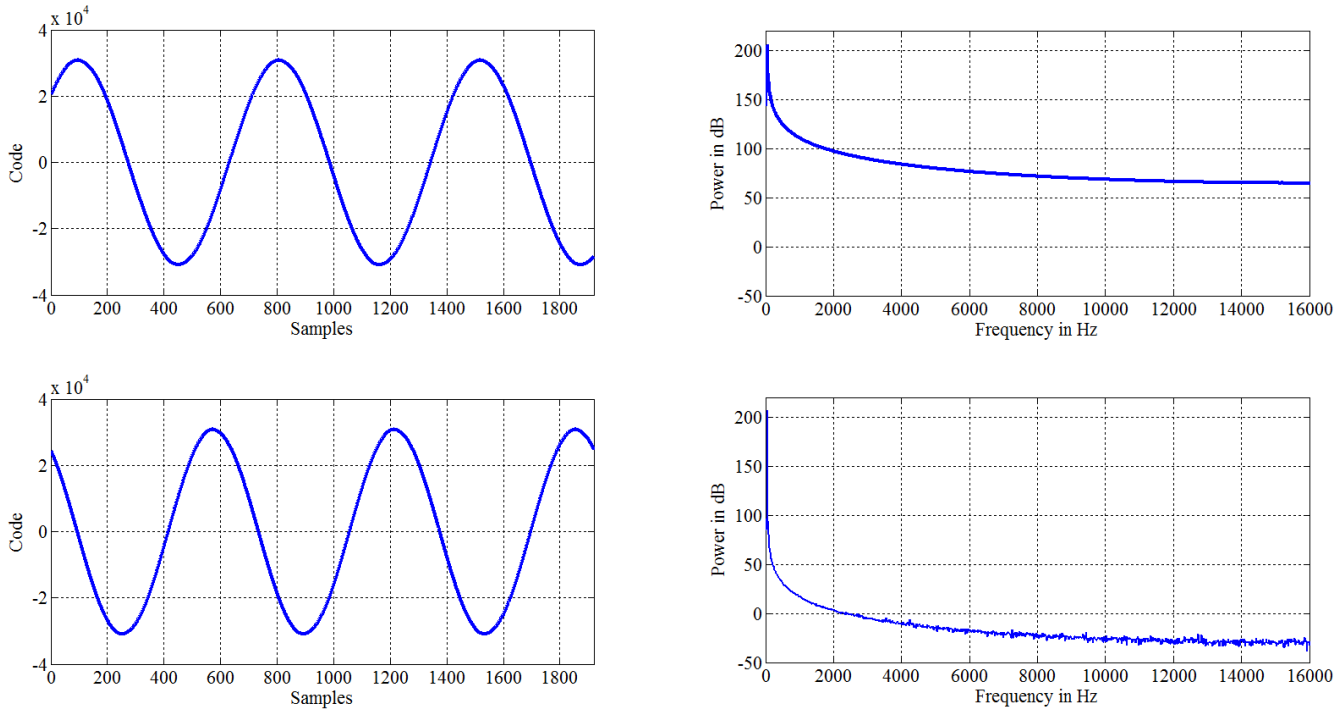

図 27. Comparison of AC Performance for Non-Coherent and Coherent Sampling

3.2.2.6 FFT Analysis

図 28 shows the frequency plot for a 64-Hz input signal with a voltage range setting of ±10.24 V and for 65536 samples. An SFDR of 110 dB is obtained, and 表 15 lists the harmonic amplitude.

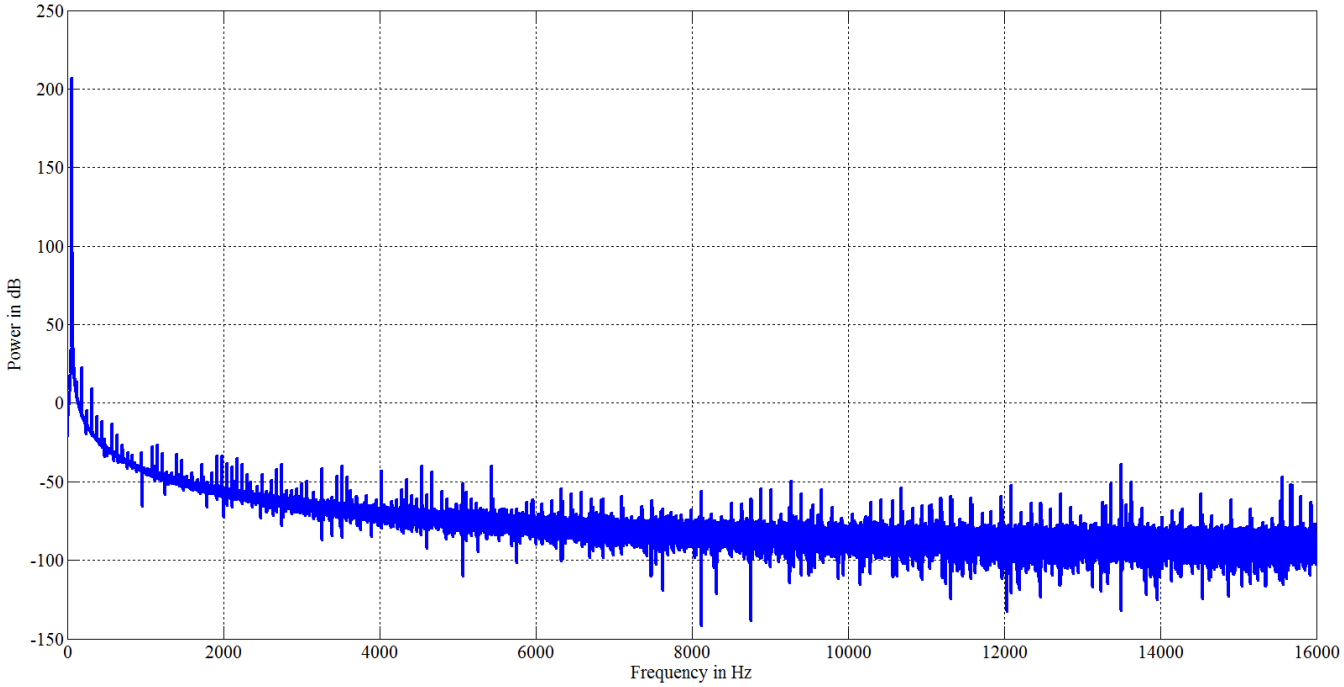

図 28. FFT Plot for AC Input Signal: Number of Points = 65536, f_{IN} = 64 Hz, SFDR = 110 dB

表 15. Harmonic Amplitude

PEAK	POWER (dB)
First peak	206.7394
Second peak	96.7118
Third peak	96.66346
Fourth peak	82.90698
Fifth peak	82.73659

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01555.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01555.

4.3 PCB Layout Recommendations

Performance of data acquisition is highly dependent on the design and layout of PCB in both analog and digital sides. Addressing the details of PCB design is critical to ensure the best performance out of the ADC. For more details, see *ADS868x 16-Bit, 500-kSPS, 4- and 8-Channel, Single-Supply, SAR ADCs with Bipolar Input Ranges*.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01555.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01555.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01555.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01555.

5 Software Files

To download the software files for this reference design, see the link at TIDA-01555.

6 Related Documentation

1. Texas Instruments, *TIDA-00307 High-Accuracy AC Voltage and Current Measurement AFE for Feeder Terminal Unit Reference Design*
2. Texas Instruments, *ADS8688EVM-PDK Evaluation Module User's Guide*
3. Texas Instruments, *TIDA-01214 Isolated, High-Accuracy Analog Input Module Reference Design Using 16-Bit ADC and Digital Isolator*

6.1 商標

7 Terminology

ADC— Analog-to-digital converter

AFE— Analog front end

CT— Current transformer

FFT— Fast Fourier transform

GUI— Graphic user interface

LPF— Low-pass filter

PRU— Programmable real-time unit

PT— Potential transformer

SFDR— Spurious-free dynamic range

SINAD— Signal-to-noise and distortion ratio

SNR— Signal-to-noise ratio

THD— Total harmonic distortion

8 About the Authors

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改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年12月発行のものから更新 **Page**

- position of Figure 10: *Overall Functioning of Timing Adjustments* to Figure 9 変更 15
- position of Figure 9: *Timing of CS Across Multiple Channels of ADCs* to Figure 10 変更 15
- Updated Software Requirements section. 27
- Updated links in AM335x RT Linux Processor SDK Installation section. 28
- Updated TIDA-01555 PRU ADC Demo Software section. 28
- Removed Compile the Device Tree to Configure Pin Muxing section. 28
- Added Running the Demo section. 28
- Removed Compiling the Arm User Space Binary and PRU-ICSS Firmwares section. 28
- Added Rebuilding from Source section. 28
- Removed Copying Files to the File System of the Board section. 30
- Removed Booting and Running the Demo section. 30
- Removed Software Disclaimer section. 30
- sample window size from 1280 to 1920 変更 37
- number of cycles captured from two to three 変更 37

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