参考資料

TI Designs: TIDA-01434
24ビットADC用の絶縁された、変圧器なしのバイポーラ電源のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

3.65mmと薄型のこの絶縁型リファレンス・デザインは、24ビット・デルタ-シグマ・アナログ/デジタル・コンバータ(ADC)により高集積のバイポーラ入力高性能ソリューションを実現します。今日のアナログ入力モジュールは同容積でのチャネル密度の向上など、さまざまな面で高い性能が要求されます。その対応には、消費電力の低減と同時に動作温度範囲の拡大が必要です。

このリファレンス・デザインでは、DC/DCコンバータと内蔵チャージ・ポンプを使用する単純な電力ツリーにより、これらの要求に対処しています。1チャネルの設計から、絶縁電源の再定義なしに、複数のチャネルへ簡単に拡張できます。

特長

- 内蔵の絶縁電源を高精度のデルタ-シグマADCと組み合わせて性能を評価
- バイポーラのアナログ電源と反転チャージ・ポンプ
- アクティブなアナログ・フロントエンド・コンポーネントを必要とせずにバイポーラ信号の入力が可能
- 高性能LDOと比較するためのリファレンス・セットアップ
- インダクタなしで、合計高さ3.65mmの高集積設計
- 外部基準電圧のオプション

アプリケーション

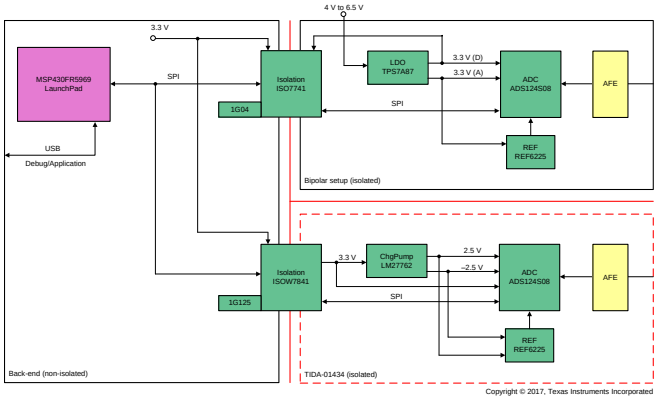
- アナログ入力モジュール

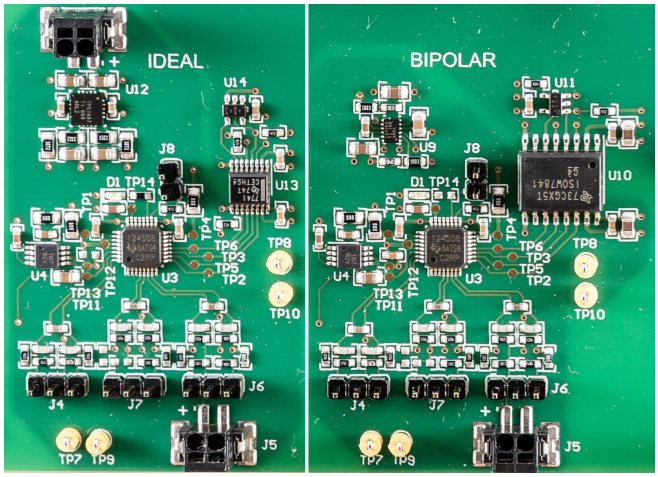
リソース

TIDA-01434	デザイン・フォルダ
ADS124S08	プロダクト・フォルダ
LM27762	プロダクト・フォルダ
TPS7A87	プロダクト・フォルダ
REF6225	プロダクト・フォルダ
ISOW7841	プロダクト・フォルダ
ISO7741	プロダクト・フォルダ

TI E2E™ Community

E2E™ エキスパートに質問





1 System Description

Modern analog input modules commonly add a separate low-dropout regulator (LDO) to analog-to-digital converter (ADC) analog power supply rails to clean up the supply rails and enable the highest ADC performance. Dedicated, low-noise LDOs with a high power supply rejection ratio (PSRR) serve this purpose.

Two kinds of PSRR exists, $PSRR_{DC}$ and $PSRR_{AC}$. $PSRR_{DC}$ describes the change of the digital output in respect of power supply shifts. $PSRR_{AC}$ specifies the impact of high-frequency interferences at the power supply to the digital output. This reference design investigates $PSRR_{AC}$.

The high-precision delta-sigma (ΔΣ) ADC ADS124S08 has an analog supply $PSRR_{DC}$ of 105 dB and a digital supply $PSRR_{DC}$ of 115 dB. The internal reference has a $PSRR_{DC}$ of 85 dB. A frequency rejection of 50 Hz or 60 Hz is particularly important to suppress the mains frequencies. The $PSRR_{AC}$ rejection of these frequencies at the analog supply is specified to 115 dB. This reference design focuses on the impact of high-frequency DC/DC converter or charge pumps added to the supply rails.

This design is isolated and space-optimized for bipolar input signals with only three components. No additional effort is taken to clean the power supply rails, such as an RC or LC filter in the power path. The DC/DC converter integrated in the ISOW7841 isolates the power from the backplane side. The LM27762 is a low-noise positive and negative output power device with an integrated charge pump and following LDOs and generates the analog bipolar voltage for the ADS124S08.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input power source	Backplane power supply	2.1
Input power voltage	3 V to 5.5 V	2.1
Average active-state input current	17 mA	2.1.1.1
Output voltages	3.3 V, –2.5 V, and 2.5 V	2.1
Average active-state efficiency	≈ 12%	2.1.1.1
Operating temperature	–40°C to +124°C	2.1.2
Form factor	35 mm × 35 mm × 3.65 mm	2.1.1.4

2 System Overview

The evaluated circuit focuses on a single- or multi-channel analog input module with bipolar analog input signals for programmable logic controllers (PLCs), but is not limited to this application. With its total solution height of 3.65 mm, the circuit is stackable, which can further increase the channel count per module.

It is suitable for both channel-to-channel or group-isolated input topologies. In a channel-to-channel isolated design, every input channel has its own ground. This topology enables the measurement of input signals with large ground potential differences. The other option is the group-isolated analog input where all input signals share the same ground. As only limited common-mode voltages are allowed, this topology is suitable for environments with well-controlled ground. The circuit in this reference design conforms to a channel-to-channel isolated input as it has one ADC at the isolated island.

As the channel count increases, so does power consumption. It is essential to take care of the power consumption of the parts and its efficiency to keep the generated heat to a minimum.

The bipolar input option supports industry standard ranges like ±50 mV to ±10 V and ±20 mA. An ADC with bipolar input range can convert these signals directly with a passive attenuation where if the input voltage can go beyond the analog rails (±2.5 V). An ADC with unipolar input range requires a shift to a unipolar voltage with an active component like an operation amplifier (op amp). An op amp can contribute additional noise to the signal-chain and add board and space and cost.

The power for the isolated part is provided either from a field power supply (24-V DC) or from the non-isolated back-end using an isolated power supply. This design does not need a 24-V DC field power supply as the energy is provided over the isolation barrier, which saves a separate power supply and protection at the isolated side.

The design splits into two parts: the bipolar setup and the reference setup. The bipolar setup is evaluated in this design while the reference setup is used as a benchmark. Both setups have identical schematics and layout, where possible.

2.1 Block Diagram

図 1 shows the block diagram of this reference design.

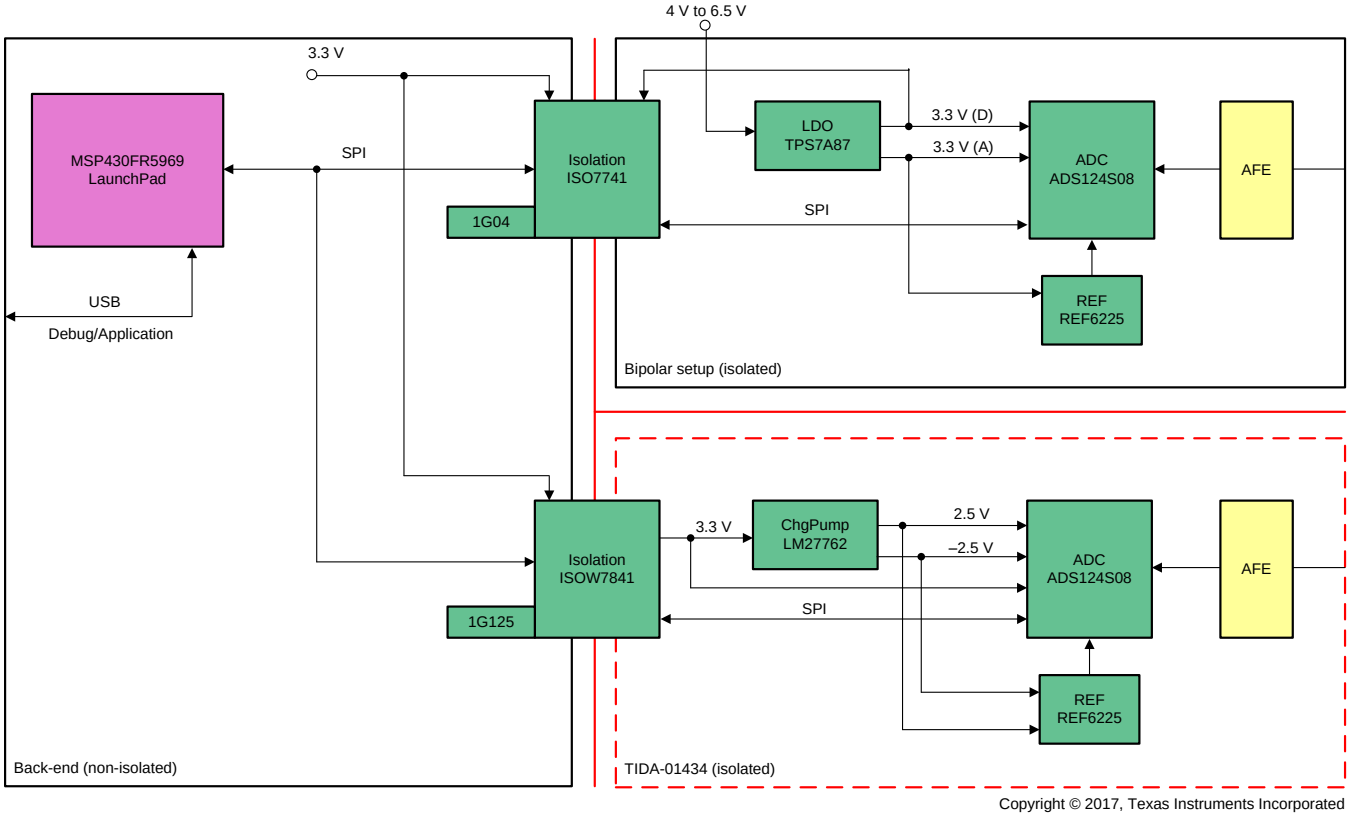


図 1. TIDA-001434 Block Diagram

2.1.1 Design Considerations

2.1.1.1 Bipolar Setup

The bipolar setup powers from a 3-V to 5.5-V supply from the back-end side. Usually, a voltage of 3.3 V already exists to power the digital part of the back-end. The ISOW7841, a member of the ISOW78xx family, isolates the four serial peripheral interface (SPI) data lines and the power. The integrated transformer removes the need for a bulky external transformer. As a result, a total solution height of 3.65 mm is possible. The ISOW7841 drives the isolated SPI bus with the generated 3.3-V isolated voltage. Therefore, the digital interface power (IOVDD) of the ADS124S08 connects to this voltage.

The digital core power of the ADS124S08 and the LM27662 connect to the same voltage. The LM27762 generates the positive analog voltage (2.5 V) by an LDO. The negative analog voltage (–2.5 V) is generated by an inverting charge pump and an succeeding negative LDO. This ±2.5-V bipolar voltage connects to the analog power supply rails of the ADS124S08 and the optional external reference REF6225.

The bipolar setup draws about 17 mA from the backplane power supply. The overall power consumption P_{TOTAL} is 3.3 V × 17 mA = 56 mW. However, the LM27762 and the ADS124S08 together draw about 2 mA from the ISOW7841. Therefore, overall efficiency is only about P_{EFF} = (2 mA / 17 mA) × 100% ≈ 12%. The reason for the lower efficiency is the low output current. A group-isolated multichannel design with multiple ADS124S08 devices connected to the ISOW7841 increases the efficiency. For example, if a resistor of 55 Ω is added to the ISOW7841 output, a total current of 62 mA is drawn. In this case, the bipolar setup draws about 132 mA from the backplane power supply. The efficiency raises up to 47%.

2.1.1.2 Reference Setup

The reference setup runs from a 4×AA battery pack and is not isolated. The low-noise, dual-output LDO TPS7A8701 generates two 3.3-V rails. One rail drives the digital part of the ADS124S08 and the isolated side of the data isolator ISO7741. The second rail drives the analog part of the ADS1224S08 and the external reference. The reference setup runs the ADS124S08 in unipolar mode to avoid a switching negative power rail.

2.1.1.3 Control Unit

The MSP430FR5969 LaunchPad™ controls both setups and plugs to the test board. The MSP430FR5969 microcontroller provides a single SPI bus (SCLK, MISO, and MOSI signals). The microcontroller selects one setup at a time by two general purpose input/output pins (GPIO), which act as SPI chip select (CS) signals. A low level at CS selects the particular setup and enables the MISO line at the same time using a little-logic gate. The MISO line of the other setup is in tri-state, which avoids over stress of two MISO outputs connected together.

2.1.1.4 Design Board Space

The board space of the bipolar setup is 35 mm × 35 mm × 3.65 mm (1.4 in × 1.4 in × 0.14 in). The test points, jumper, and the external reference can be removed, further shrinking the design to about 50% of its original dimensions.

2.1.2 Operating Temperature Considerations

The ADS124S08 and the ISOW7841 have an operating temperature range of at least –40ºC to +125ºC. The LM27762 data sheet specifies an maximum ambient temperature T_A of 85ºC and a junction temperature T_J of 125ºC. The junction-to-ambient thermal resistance R_{JA} is 62.2ºC. Calculate the absolute power dissipation P_{DMAX} using 式 1:

$$P_{DMAX} = \frac{(T_J - T_A)}{R_{JA}} = \frac{(125°C - 85°C)}{62.2°C/W} = 0.64\ W \quad (1)$$

The LM27762 can dissipate a maximum power of 0.64 W at an ambient temperature of 85ºC. However, the quiescent power consumption of the LM27762 and the additional power dissipation from the inverting charge pump and LDOs is less than 5 mW. Solving for T_A leads to 式 2:

$$T_{Anew} = T_J - R_{JA} \times P_{DMAXnew} = 125°C - 62.2°C/W \times 5\ mW = 124.6°C \quad (2)$$

According to 式 2, T_A can rise up to 124.6ºC in this condition. A significantly rise in ambient temperature is tolerated due to the low-output power requirements.

2.2 Highlighted Products

2.2.1 ADS124S08

The ADS124S08 is a precision, 24-bit, ΔΣ, ADC that offers low power consumption and many integrated features to reduce system cost and component count in applications measuring small-signal sensors.

This device features configurable digital filters that offer low-latency conversion results and 50-Hz or 60-Hz rejection for noisy industrial environments. A low-noise, programmable gain amplifier (PGA) provides gains ranging from 1 to 128 to amplify low-level signals for resistive bridge or thermocouple applications. Additionally, this device integrates a low-drift, 2.5-V reference that reduces printed circuit board (PCB) area. Finally, two programmable excitation current sources (IDACs) allow for easy and accurate RTD biasing.

An input multiplexer supports 12 analog inputs that can be connected to the ADC in any combination for design flexibility. In addition, this device includes features such as sensor burn-out detection, voltage bias for thermocouples, system monitoring, and four general-purpose I/Os.

2.2.2 LM27762

The LM27762 delivers very low-noise positive and negative outputs that are adjustable between ±1.5 V and ±5 V. Input-voltage range is from 2.7 V to 5.5 V, and output current goes up to ±250 mA.

Negative voltage is generated by a regulated inverting charge pump followed by a low-noise negative LDO. The inverting charge pump of the LM27762 device operates at a 2-MHz (typical) switching frequency to reduce output resistance and voltage ripple. Positive voltage is generated from the input by a low-noise positive LDO.

2.2.3 TPS7A87

The TPS7A87 is a dual, low-noise (3.8 μV_{RMS}) LDO voltage regulator capable of sourcing 500 mA per channel with only 100 mV of maximum dropout.

The TPS7A87 provides the flexibility of two independent LDOs and approximately 30% smaller solution size than two single-channel LDOs. Each output is adjustable with external resistors from 0.8 V to 5.2 V. The wide input-voltage range of the TPS7A87 supports operation as low as 1.4 V and up to 6.5 V.

The TPS7A87 is designed to power noise-sensitive components such as those found in instrumentation, medical, video, professional audio, test and measurement, and high-speed communication applications. The very low 3.8-μV_{RMS} output noise and wideband PSRR (40 dB at 1 MHz) minimizes phase noise and clock jitter. These features maximize the performance of clocking devices, ADCs, and DACs.

2.2.4 REF6225

The voltage references in the REF6000 family have an integrated low output impedance buffer that enables the user to directly drive the reference (REF) pin of precision data converters, while preserving linearity, distortion, and noise performance. Most precision SAR and ΔΣ ADCs switch binary-weighted capacitors onto the REF pin during the conversion process. To support this dynamic load, the output of the voltage reference must be buffered with a low-output impedance, high-bandwidth buffer.

The REF6225 specifies a maximum temperature drift of just 3 ppm/°C and initial accuracy of 0.05% for both the voltage reference and the low output impedance buffer combined.

2.2.5 ISOW7841

The ISOW7841 is a high-performance, quad-channel reinforced digital isolator with an integrated high-efficiency power converter. The integrated DC/DC converter provides up to 650 mW of isolated power at high efficiency and can be configured for various input and output voltage configurations. Therefore, this device eliminates the need for a separate isolated power supply in space-constrained isolated designs.

2.2.6 ISO7741

The ISO7741 device is a high-performance, quad-channel digital isolator with 5000-V_{RMS} (DW package) and 2500-V_{RMS} (DBQ package) isolation ratings per UL 1577. This device has reinforced insulation ratings according to VDE, CSA, TUV, and CQC.

2.2.7 SN74AHC1G04

The SN74AHC1G04 contains one inverter gate.

2.2.8 SN74AHC1G125

The SN74AHC1G125 device is a single bus buffer gate and line driver with a three-state output.

2.3 System Design Theory

The delta-sigma architecture shows the best performance for DC or near-DC analog input signals. The noise-shaping feature of a delta-sigma converter pushes noise towards higher frequencies. This feature allows precise and accurate measurements in the low-frequency region. Temperature or 4- to 20-mA loop inputs measurements are common applications that use the strengths of the precision delta-sigma ADC topology. For this reason, all setups in this design use a DC input signal. The effective resolution, expressed in bits, is the performance metric for DC input signals. To measure the effective resolution at DC for a given hardware, a series of consecutive samples is taken. The standard deviation is calculated and applied to 式 3. Constant *N* is the bit width of the converter. For the ADS124S08, N = 24.

$$\text{Effective Resolution} = \log_2\left(\frac{2^N}{\text{stddev}(\text{samples})}\right) \quad (3)$$

The measured effective resolution is compared against the effective resolution from the data sheet. If the used configuration matches the data sheet configuration the values are directly taken from it. If the reference differs (for example, set up *RTD1000* with random reference voltage), the effective resolution is calculated with 式 4:

$$\text{Effective Resolution} = \log_2\left(\frac{\frac{2 \times V_{REF}}{GAIN}}{V_{N,RMS}}\right) \quad (4)$$

2.3.1 Expected Results

The measurements of the *ideal* setup and the *bipolar* setup are similar and are in the region of the data sheet values. This result proves that the interferences caused by the DC/DC converter (ISOW7841) and the inverting charge pump (LM27762) are sufficiently filtered by the LDOs (LM27762) and the ADS124S08 itself.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

The MSP430FR5969 microcontroller embedded in the MSP430FR5969 LaunchPad connects to the reference design hardware with two 1×10 pin headers. Power to the LaunchPad provides the USB connection. An LDO on the LaunchPad generates 3.3 V for the MSP430™ MCU. A lab power supply (Keysight E3631A) delivers 3.3 V for the primary side of the ISOW7841 (bipolar setup) and of the ISO7741 (reference setup). The low-noise dual LDO of the reference setup requires an extra 4-V to 6.6-V power source, which is delivered by a 4×AA battery pack. The small signal test configuration needs a constant current supplied by an SMU (Keysight B2912A).

The MSP430 MCU connects upwards to a standard Windows® host machine. 図 2 shows the hardware setup for the board test.

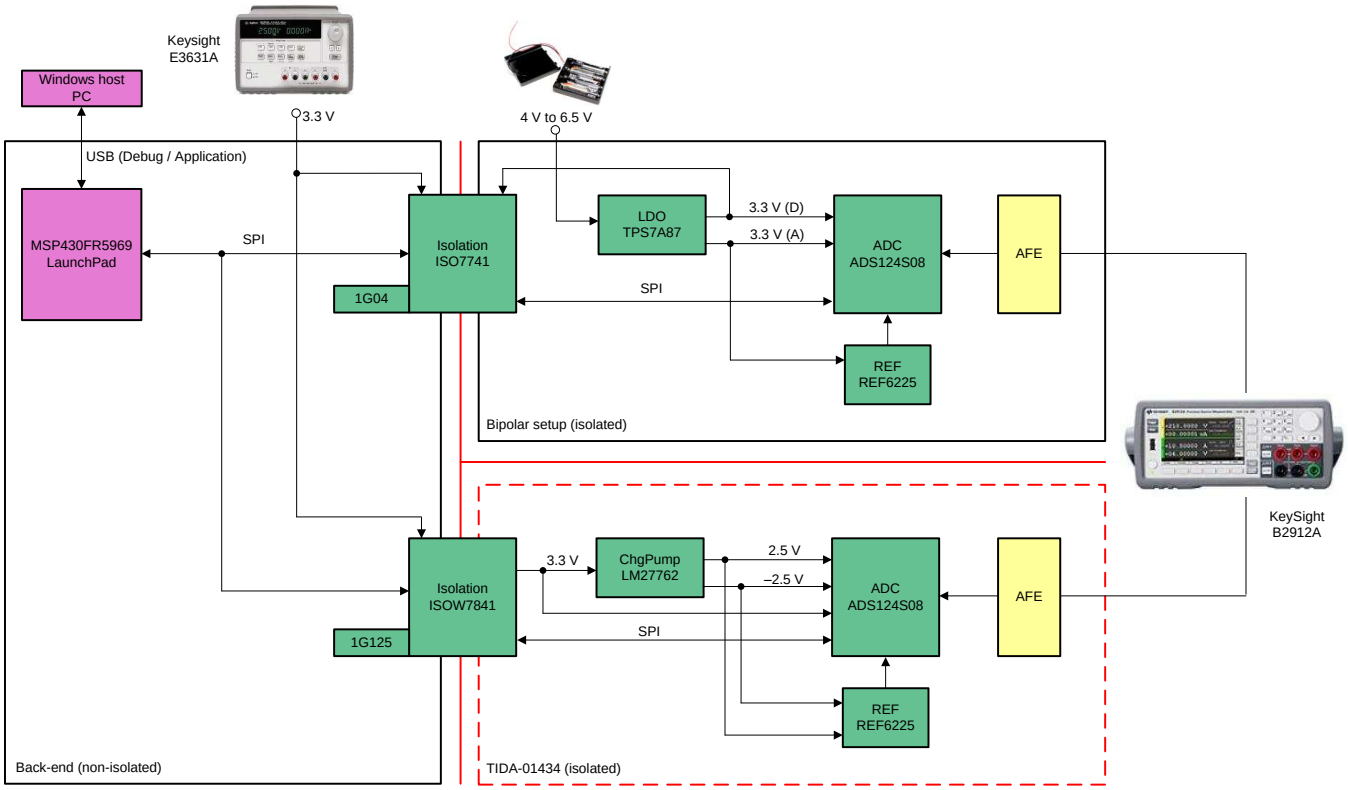


図 2. Lab Hardware Setup

3.1.1.1 Power Supply

The power supply path includes a DC/DC converter and an integrated transformer for the power isolation in the ISOW7841. The output voltage of 3.3 V maintains through a hysteresis window of about 100 mV. When the output voltage falls below the lower threshold, the DC/DC converter charges the output capacitor up to the upper threshold. The converter switches off until the output is discharged to the lower threshold again. The DC/DC switching frequency is 60 MHz. 図 3 shows the output of the ISOW7841 when the DC/DC converter operates.

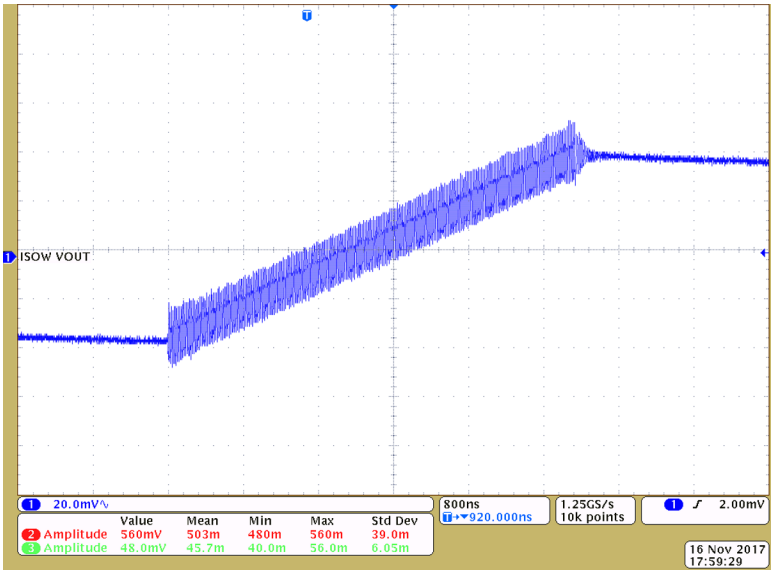


図 3. DC/DC Converter Charges Output Capacitor With 60 MHz

The frequency of the 100-mVpp charge and discharge curve depends on the output load. 図 4 shows that the output current of about 2 mA generates two frequencies: 25 kHz and 31.25 kHz. A resistor of 55 Ω is added to the 3.3-V rail to observe the behavior under a load of 62 mA total (see 図 5). The triangle frequency increases to 65 kHz and 77 kHz.

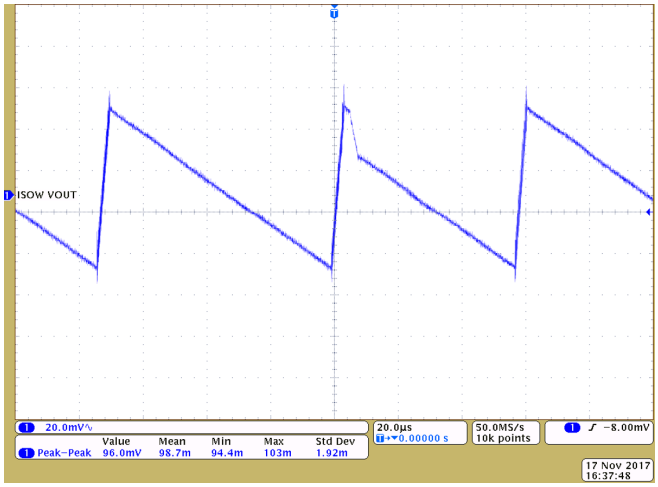


図 4. ISOW7841 Output Voltage at 2-mA Load Current

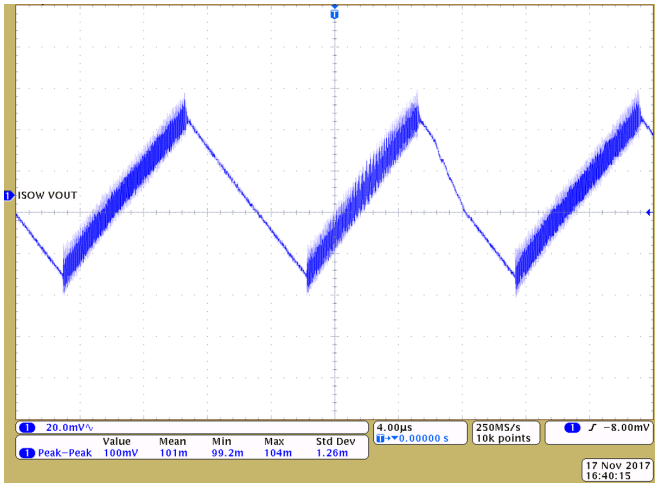


図 5. ISOW7841 Output Voltage at 62-mA Load Current

The other switching part of the power path is the inverting charge pump of the LM27762, which operates at 2 MHz. During light-load conditions, the charge pump enters the PFM or pulse-skipping mode to minimize quiescent current. As the load current required for the negative rail is very low (< 1 mA) compared to the maximum output current (250 mA), the LM27762 is in PFM mode at all times. 図 6 shows the 2-MHz burst of the inverting charge pump and its impact on the triangle of the ISOW7841 output. With a 2-mA load, every second triangle the LM27762 draws current for the charge pump, which causes a faster discharge of the ISOW7841 output capacitor. This increases the triangle frequency from 25 kHz to 31.25 kHz every other period.

図 7 shows the measured voltage at the analog power supply (AVSS, AVDD) of the ADS124S08). The differential voltage is around 9 mVpp.

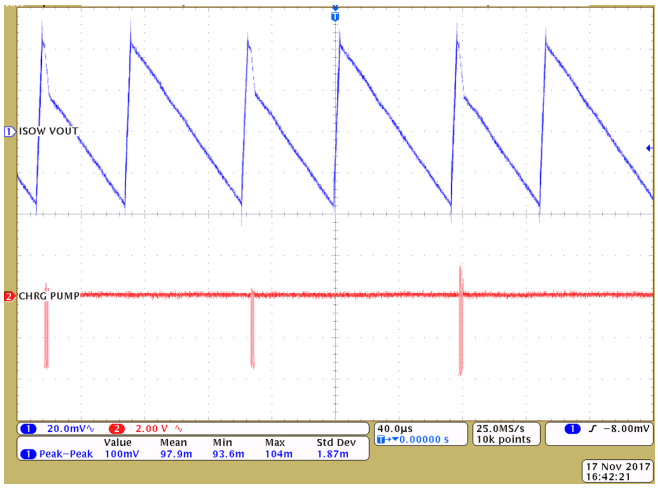


図 6. ISOW7841 Output Waveform and Inverting Charge Pump Relationship at 2-mA Load

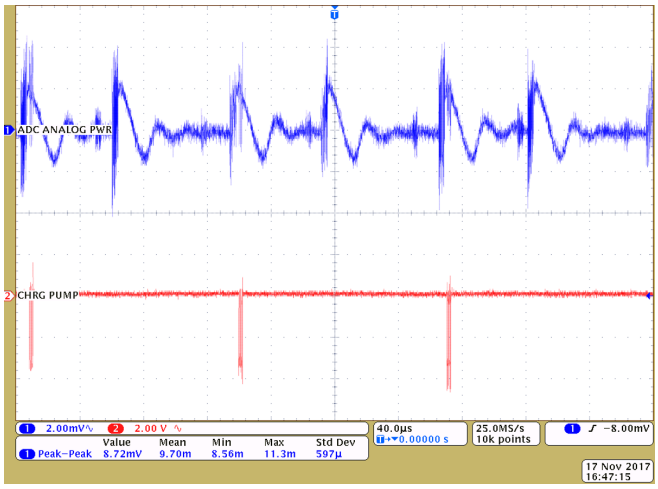


図 7. Power Supply Waveform Analog Section (AVSS-AVDD)

3.1.2 Software

All test cases are performed by automatic test equipment (ATE). Both the reference setup and the bipolar setup are controlled by an MSP430FR5969 LaunchPad board. The MSP430FR5969 accepts high-level commands from the host over USB. The host controls the MSP430FR5969 by a python script.

Script sequence:

1. Create an Excel® sheet for measurements and write column headers.
2. Select hardware (select CS# line for all further SPI communication).
3. For each test setup:
   a. Reset ADS124S08 (using software reset command).
   b. Program AI+/AIN-, IDAC, reference source, gain, system monitor, data rate, filter, and chopper.
   c. Start the conversion (ADS124S08 runs in continuous mode only) with the number of samples as an argument.
   d. The MSP430 MCU reads the requested number of conversion results and stores it in the MSP430 FRAM.
   e. Once finished, all samples are transferred to the host through UART (57600 baud) and stored in the Excel sheet.

Data are read with polling mode. After a predefined period of time, the CS# line is pulled low. If the MISO line drives low, new data is available and is read by the MSP430FR5969. The other option is to use the dedicated DRDY# line. However, this option adds a costly fifth isolated signal.

The performance of the ADS124S08 for both setups is tested with different data rates, filter settings, and optional chop feature. The internal reference in the ADS124S08 and an external high-performance REF6225 are also compared.

3.2 Testing and Results

Three configurations are used to the test the performance of the ideal and bipolar setups. Furthermore, two options to configure the ADS124S08 are introduced: *performance* and *speed*.

The performance option uses the SINC3 filter with the chopper feature enabled. This option provides highest effective resolution as the SINC3 filter has better noise performance than the low-latency filter at the cost of latency. The chopper averages two samples with opposite polarity, which removes system offset voltage at the cost of data throughput.

The speed option uses the low-latency filter with the chopper feature disabled. This option provides the highest data throughput with low latency at the cost of a lower effective resolution. This option is useful when switching through multiple input channels is required.

All configuration and option measurements use the internal reference of the ADS124S08.

3.2.1 Small Signal Configuration

3.2.1.1 Description

The small signal test configuration uses the analog front end (AFE) shown in 図 8. This configuration consists of two parallel resistor ladders (R21/R28 and R22/R29) with an equal resistance of 5.27 kΩ. This setup results in a total resistance of 2.635 kΩ between the two terminal pins of header J5. A constant current of 1 mA is injected through J5 to the AFE. The voltage at AIN1 (positive input) is always –2.5 V + 2.635 kΩ × 1 mA = 0.135 V. Jumper J6 selects one of the two resistor ladder mid-points, which provides the negative input voltage to AIN0. Note that AVSS = –2.5 V.

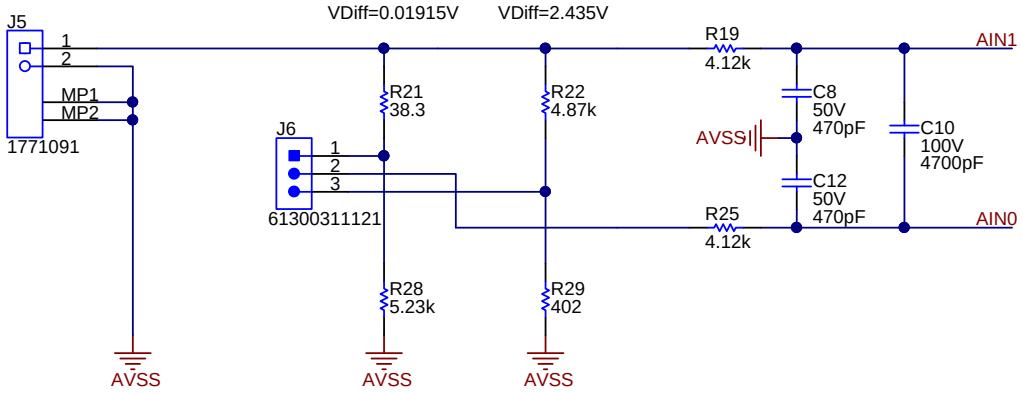


図 8. Schematic of AFE for Small Signal Test Configuration

表 2 shows the generated voltages.

表 2. Analog Input Voltages

JUMPER J6	CONFIGURATION	AIN–	AIN+	VDIFF
1-2	Small signal	0.116 V	0.135 V	0.019 V
2-3	Large signal	–2.299 V	0.136 V	2.435 V

Jumper position 1-2 selects the small signal configuration. This configuration generates a differential voltage of 19.15 mV. The common-mode voltage is (AIN– + AIN+) / 2 = 0.125 V, which is in the middle of the analog input range of 0 V. This is of benefit as the common-mode voltage window narrows with increasing PGA gains. 図 9 shows a screen shot of the ADS124S08 design calculator (available for download at the ADS124S08 product page) for the small signal configuration and a PGA gain of 128 V/V.

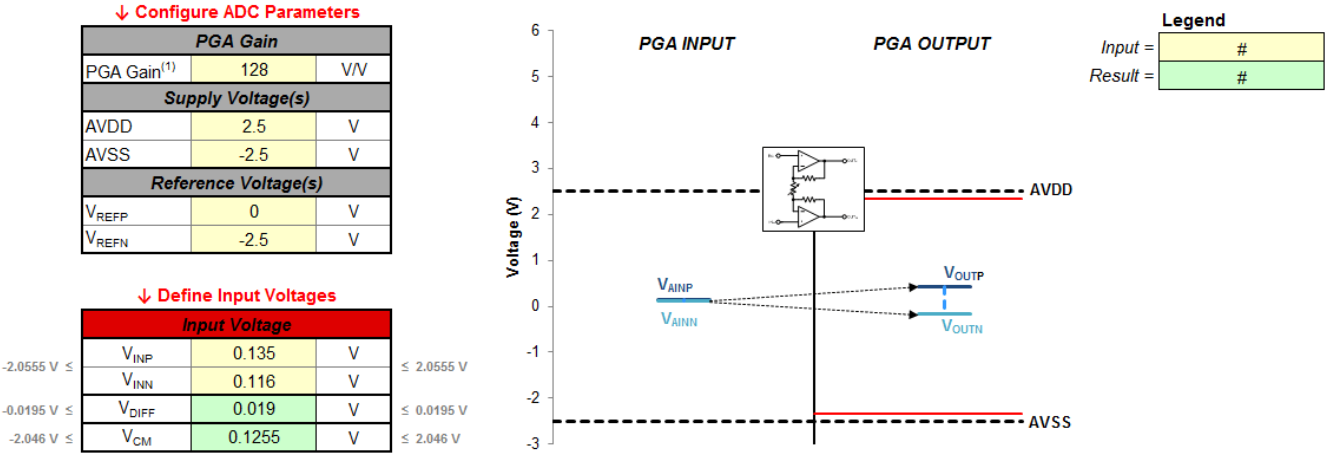


図 9. Small Signal Input Voltages for PGA Gain = 128 V/V

Note that the PGA output is 32 V/V of the differential input voltage as the two highest gain steps (64 V/V and 128 V/V) are performed digitally.

Jumper position 2-3 selects the large signal configuration. It generates a differential voltage of 2.435 V, which is close to the reference voltage of 2.5 V. This configuration is not considered here because the performance limits of the circuit are expected at lowest input-referred noise at highest gain values and lowest data rates.

The small signal configuration is tested with all data rates, all gains, internal reference and the high-performance option.

3.2.1.2 Results

図 10 shows the effective resolution with a PGA gain of 1 V/V and performance option for all data rates and compares it with the measurement results from the ideal and bipolar setups.

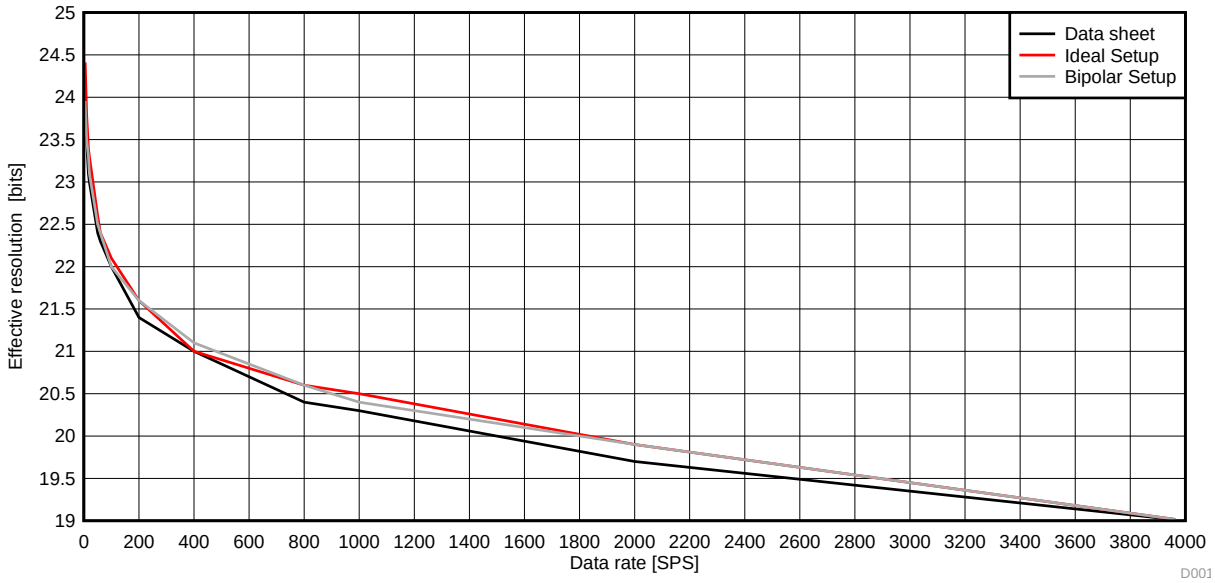


図 10. Effective Resolution Results of Small Signal (All Data Rates, PGA 1 V/V)

The ADS124S08 data sheet values match the measured values while the ideal setup even exceeds the data sheet values at low data rates.

図 11 shows the effective resolution with a PGA gain of 128 V/V and performance option for all data rates and compares it with the measurement results from the ideal and bipolar setups.

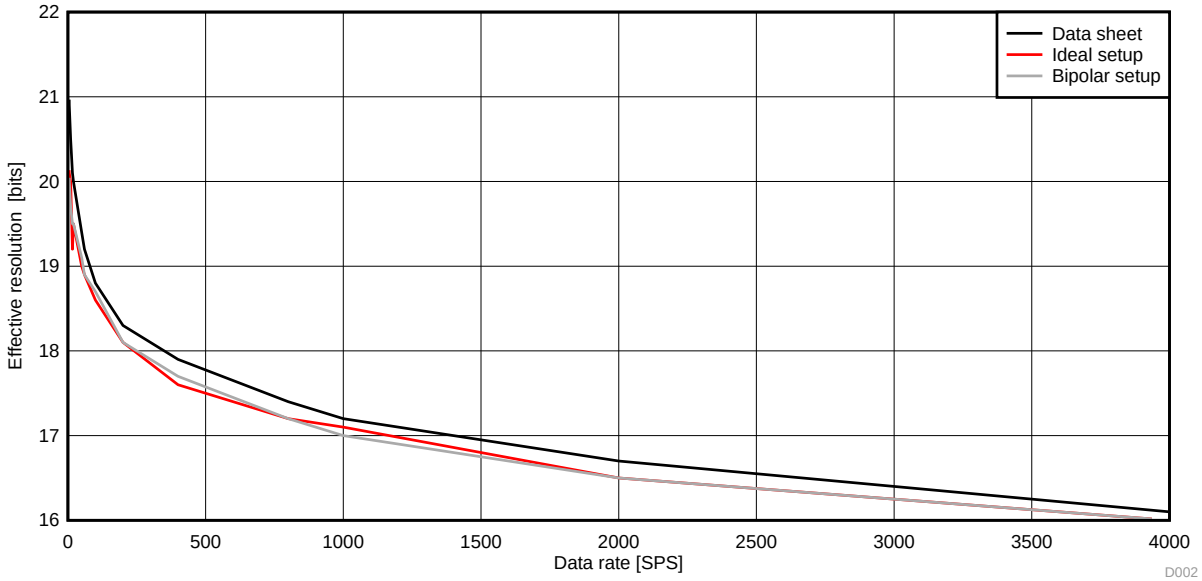


図 11. Effective Resolution Results of Small Signal (All Data Rates, PGA 128 V/V)

The ADS124S08 has the lowest input-referred noise at a data rate of 2.5 SPS and a PGA gain of 128 V/V and the performance option. The data sheet input-referred noise is 70 nVpp. The SMU drives the current of 1 mA into the AFE and has a noise performance of 6 nApp in this current range. As the current is split between the two resistor ladders, noise is also cut in half. The expected signal noise is $V_{N,SIGNAL}$ = 63 nApp / 2 × 38.3 Ω = 114.9 nVpp. As the noise of the input signal is higher than the input-referred noise, some degradation is observed in the data rate range of 2.5 to 20 SPS for both setups.

All small signal configurations are tested with the ADS124S08 internal reference and the REF6225 external reference. The external reference does not increase performance significantly.

3.2.2 Configuration RTD1000

3.2.2.1 Description

The schematic includes a simple two-wire RTD setup, which is a common application for analog input modules. The ADS124S08 built-in current source (IDAC1) drives a constant current of 50 µA through a standard 1-kΩ resistor (R24), which emulates the RTD. The voltage drop is V_{RTD} = 1 kΩ × 50 µA = 50 mV.

The same 50 µA flows through the reference resistor R17. The voltage drop of R17 is used as reference for the ADC (ratiometric measurement). The resistance of 17.4 kΩ generates a reference voltage of V_{REF} = 17.4 kΩ × 50 µA = 870 mV. 図 12 shows the AFE.

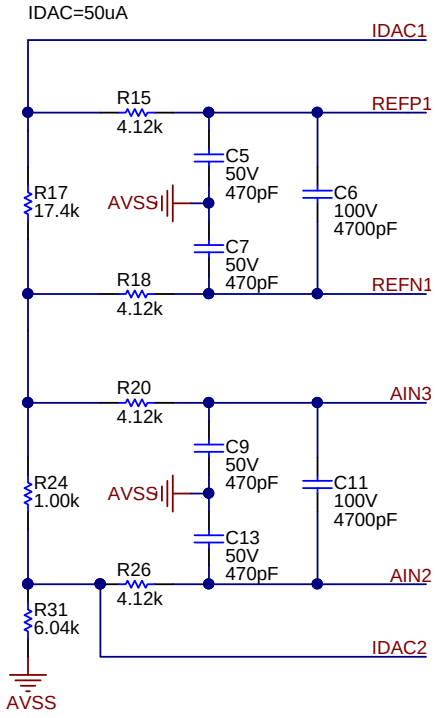


図 12. RTD1000 AFE Schematic

The RTD1000 test configuration uses PGA gains from 1 V/V to 16 V/V. The data rate is fixed to 20 SPS. More data rate is usually not needed for a slowly changing temperature. The ADS124S08 offers simultaneous 50- and 60-Hz mains frequency rejection at 20 SPS.

3.2.2.2 Results

The reference voltage of 870 mV leads to a full-scale range (FSR) of 2 × 870 mV/gain. The effective resolution is calculated with 式 4. The measurements from both setups are compared to the calculated value. 図 13 shows the results of the performance option.

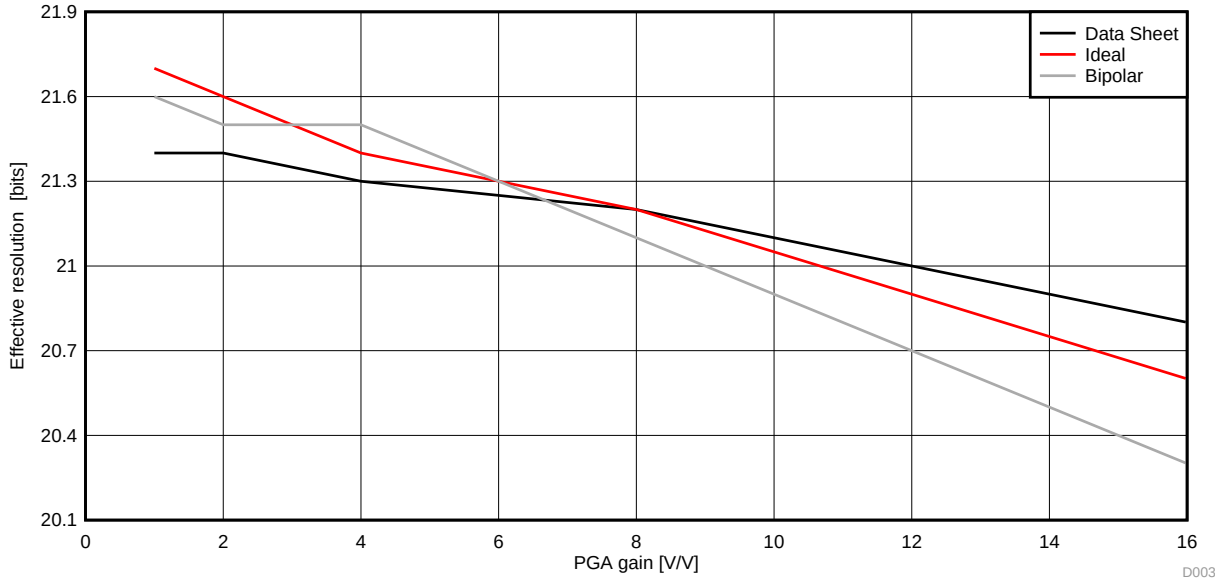


図 13. Performance Option Results for RTD1000

図 14 shows the measurements results of the speed option.

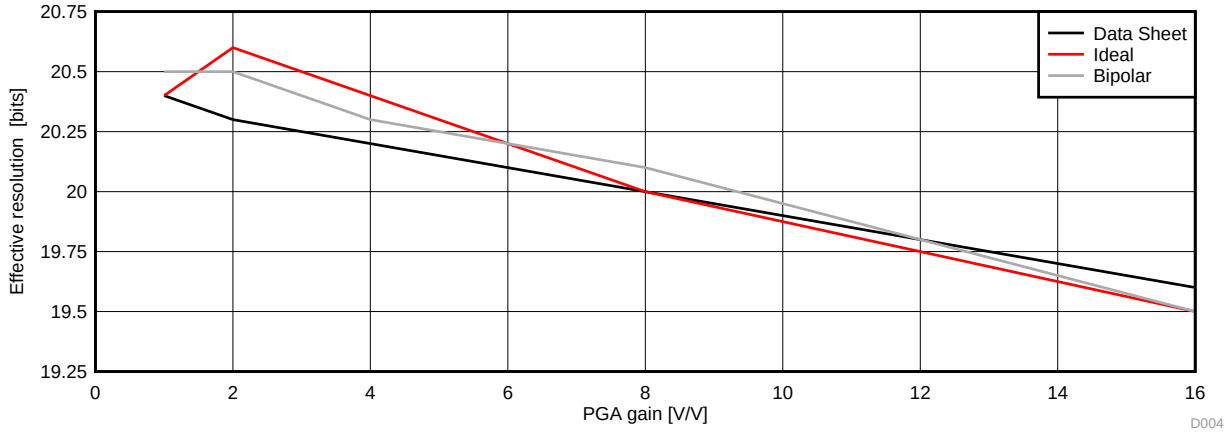


図 14. Speed Option Results for RTD1000

For both options, the measurement results are in the expected range. Note that the best effective resolution is reached with lower PGA gain values. It is not beneficial to use the full analog input range.

The performance option uses the SINC3 filter and the chopper feature. This option leads to an overall performance increase of 1 bit. If data rate and latency is not a concern, this is the preferred option.

3.2.3 Configuration Shorted Inputs

3.2.3.1 Description

Both analog inputs are internally shorted in this test configuration. The PGA is enabled with a gain of 1 V/V and 128 V/V. This configuration tests the output-referred noise of the ADS124S08 and is included to compare the ADS124S08 data sheet values with the ideal and bipolar hardware setups.

3.2.3.2 Results

図 15 shows the results of the ideal and bipolar setups compared to the data sheet values. The performance option is used with a PGA gain of 1V/V and an internal reference. The deviation is ±0.3 bits (max). Both setups perform similar to the data sheet values.

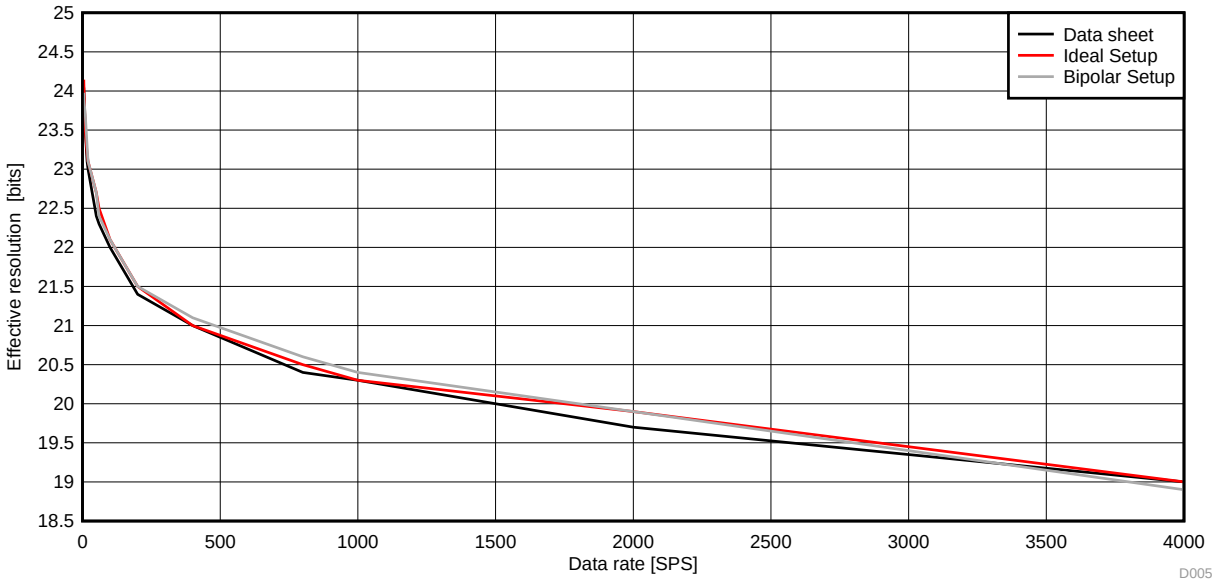


図 15. Measurement Results Effective Resolution With Shorted Inputs and PGA Gain = 1 V/V

図 16 shows the results of the ideal and bipolar setups compared to the data sheet values. The performance option is used with a PGA gain of 128 V/V and an internal reference. The deviation is ±0.3 bits (max). Both setups perform similar to the data sheet values.

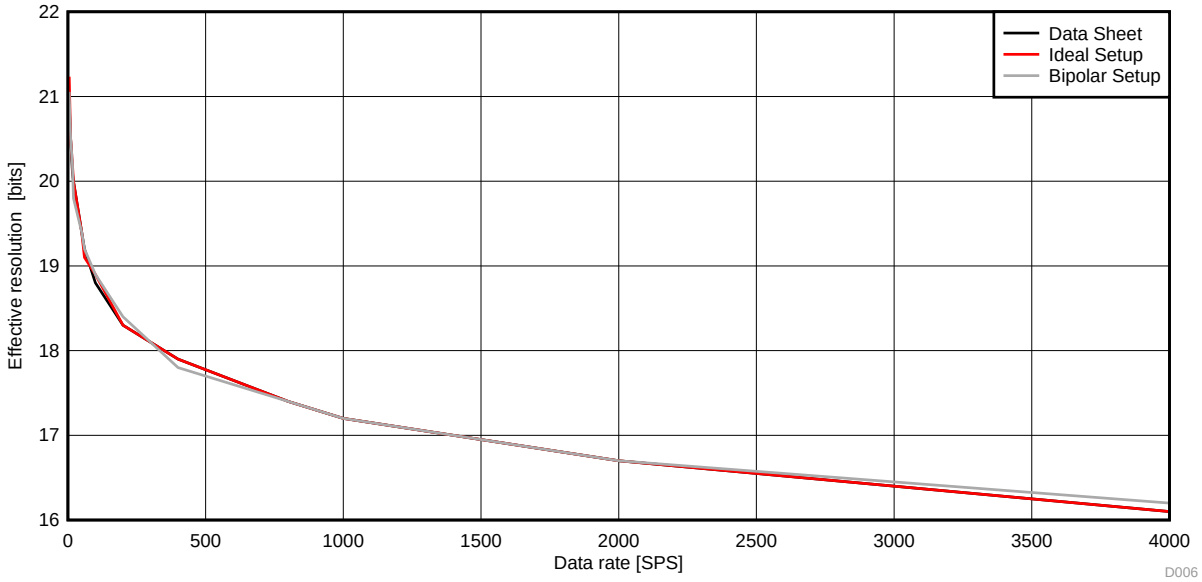


図 16. Measurement Results Effective Resolution With Shorted Inputs and PGA Gain = 128 V/V

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01434.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01434.

4.3 PCB Layout Recommendations

Please follow the layout recommendation of each device as descried in the data sheet.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01434.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01434.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01434.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01434.

5 Related Documentation

1. Texas Instruments, *ADS124S0x Low-Power, Low-Noise, Highly Integrated, 6- and 12-Channel, 4-kSPS, 24-Bit, Delta-Sigma ADC with PGA and Voltage Reference Data Sheet*
2. Texas Instruments, *LM27762 Low-Noise Positive and Negative Output Integrated Charge Pump Plus LDO Data Sheet*

5.1 商標

6 About the Author

LARS LOTZENBURGER is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Lars brings to this role his extensive experience in analog/digital circuit development, PCB design, and embedded programming. Lars earned his diploma in electrical engineering from the University of Applied Science in Mittweida, Saxony, Germany.

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2017年12月発行のものから更新 **Page**

- 「特長」から社内用語を 削除 1
- internal term to *ISOW78xx* 変更 4

重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件（www.tij.co.jp/ja-jp/legal/termsofsale.html）、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用されるTI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションが適用される各種規格や、その他のあらゆる安全性、セキュリティ、またはその他の要件を満たしていることを確実にする責任を、お客様のみが単独で負うものとします。上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件（www.tij.co.jp/ja-jp/legal/termsofsale.html）、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用されるTI の保証または他の保証の放棄の拡大や変更を意味するものではありません。