参考資料

TI Designs: TIDA-01024
レーダーおよび5Gワイヤレス・テスター用の、チャネル数の多いJESD204Bデイジー・チェーン・クロックのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

高速でマルチチャネルのアプリケーションには、チャネル間スキューを正確に調整して最適なシステムの信号対雑音比(SNR)、スプリアス・フリー・ダイナミック・レンジ(SFDR)、有効ビット数(ENOB)を実現できる、低ノイズでスケーラブルなクロック・ソリューションが必要です。このリファレンス・デザインは、JESD204Bに同期したクロックをデイジー・チェーン構成でスケーリングできます。このデザインは、TIのLMK04828クロック・ジッタ・クリーナ、およびVCOを内蔵したLMX2594ワイドバンド・フェーズロック・ループ(PLL)を使用して、マルチチャネルのJESD204Bクロックを実現し、10ps未満のクロック間スキューを達成しています。このデザインは、TIのADC12DJ3200 EVMを使用して3GSPSでテスト済みで、SRN性能の向上とともに50ps未満のチャネル間スキューが確認されています。すべての主要な設計理論が記載され、部品選択プロセスや設計の最適化の手引きとなります。

リソース

TIDA-01024	デザイン・フォルダ
ADC12DJ3200EVM	ツール・フォルダ
ADC12DJ3200	プロダクト・フォルダ
LMX2594	プロダクト・フォルダ
LMK04828	プロダクト・フォルダ
TSW14J56EVM	ツール・フォルダ

TI E2E™ Community

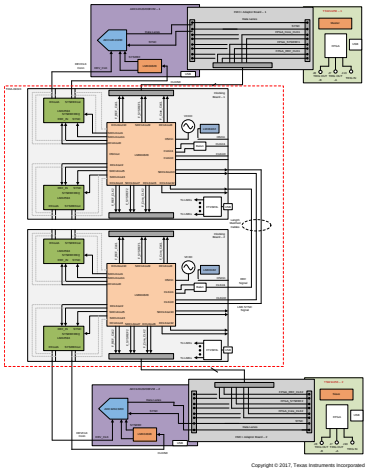
E2E™エキスパートに質問

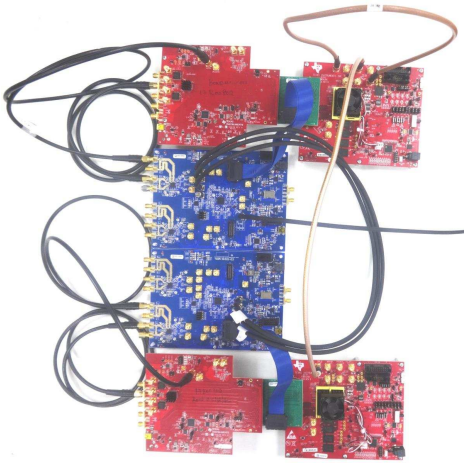
特長

- 高周波数(GSPS)のサンプル・クロック生成
- スケーラブルなJESD204B準拠のクロック・ソリューション
- RFサンプリングのADCおよびDAC向けの低位相ノイズのクロック生成
- 位相同期を構成し、マルチチャネル・システムで低スキューを実現
- TIの高速コンバータおよびキャプチャ・カード(ADC12DJ3200EVM、TSW14J56、TSW14J57)に対応

アプリケーション

- ワイヤレス通信テスター
- フェーズ・アレイ・レーダー





1 System Description

Clocking solutions for high-speed GSPS direct RF sampling signal chains are critical to achieve a high signal-to-noise ratio (SNR), low channel-to-channel skew, and to scale up the synchronized clocks for several end equipments. The tool folder for the TIDA-01021 shows the multichannel phase-synchronized JESD204B clock generation: *The Multichannel JESD204B 15-GHz Clocking Reference Design for DSO, Radar, and 5G Wireless Testers*. This reference design is an enhancement of the TIDA-01021 reference design to scale up the synchronized clocks in a daisy-chain configuration (multiboard synchronization) that can be used in applications such as a 5G wireless tester, phased array radars, and so forth.

Various topologies are available for synchronizing the multiple devices or boards, such as the tree topology and daisy chain topology. This design uses a daisy-chain topology to synchronize the multiple clocking boards. In this configuration, first the clocking board receives a high-frequency reference signal from an external clock source and generates the synchronized high-frequency clocks; it then distributes the same reference signal to the next clocking board, along with the sync signals, to synchronize the two clocking boards.

In this solution, clocking boards LMK04828 are in distribution mode; thus, they do not add PLL noise. LMX2594 frequency synthesizers receive a reference signal through the LMK04828s and generate high-performance phase-synchronized device clocks (sampling clocks) and SYSREF for multichannel high-speed signal chains. The clocking board LMK04828s also generates the field-programmable gate array (FPGA) device clocks and SYSREFs to each channel.

Wireless tester equipment uses multichannel receivers for testing cellular and multiple-input and multiple-output (MIMO) devices. Wireless testers require multiple synchronized analog channels, high dynamic range, and wideband receivers to test 3G and later wireless standards-compliant equipment. The ADC12DJ3200 is well suited for the multichannel receiver requirements of the wireless testers. The clocking solution that this reference design describes supplements a high-performance signal chain solution based on multiple ADC12DJ3200 analog-to-digital converters (ADCs) to achieve a low time skew between channels that provide both high dynamic range and a wide receiver bandwidth.

Phased array radar applications require multiple synchronized channels, high dynamic range, wide receiver bandwidth, and low latency. The signal chain solution based on the LMX2594, ADC12DJ3200, and LMK04828 devices can achieve optimum performance and high channel counts for phased array-radar applications.

1.1 Key System Specifications

The objective of this design is to demonstrate a scaling up the high-speed clocking solution for multichannel signal chains. This design focuses on measuring the configurable phase delay to align board-to-board multichannel clocks, the SNR at ADC12DJ3200 multiple signal chains, and the time skew between them. The TSW14J56 EVM performs the data capture, which is interfaced with the ADC12DJ3200EVM using an FMC adapter card. 表 1 lists the key system level specifications for the signal chain from the clocking solution perspective.

表 1. Key Specifications

PARAMETER	SPECIFICATIONS	CONDITIONS
SNR (dBFS) (dual-channel mode)	55.2	997-MHz ADC input signal
	52.7	2482-MHz ADC input signal
Board-to-board clock time skew	< 10 ps	3-GHz clock output
Analog channel-to-channel time skew	< 50 ps	997-MHz ADC input signal
		2482-MHz ADC input signal

2 System Overview

2.1 Block Diagram

図 1 shows the block diagram of the proposed, scalable, multichannel phase-synchronized clock solution. Each clocking board has two, high-speed synchronized JESD204B clocks. These boards synchronize to each other using the daisy-chain configuration, where the first clocking board synchronizes to the next clocking board by providing the same reference input signals and sync signals, then having the chain follow the same process. The clocking board uses length-matched cables to provide the reference and sync signals.

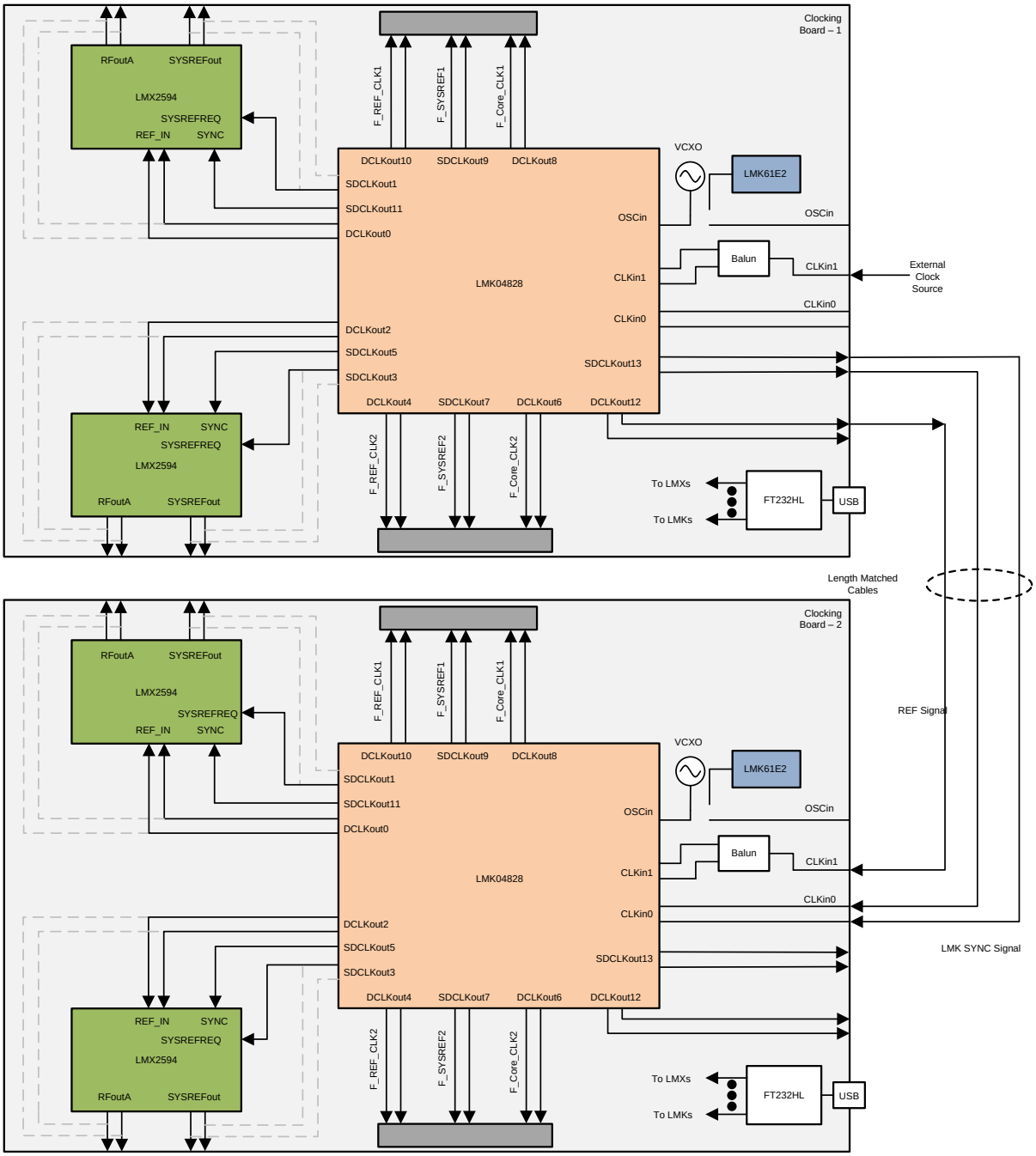


図 1. Daisy-Chain Configuration for Synchronizing Multiple Clocking Boards

2.2 Highlighted Products

2.2.1 LMX2594

The LMX2594 is a high-performance, wideband RF PLL with integrated VCO that supports a frequency range from 10 MHz to 15 GHz without using an internal doubler. The device supports both fractional-N and integer-N modes with a 32-bit fractional divider allowing fine frequency selection. The high-performance PLL with a figure of merit of –236 dBc/Hz and high-phase detector frequency can attain very-low in-band noise and integrated jitter. The integrated noise of 45 fs for a 7.5-GHz output makes the device an ideal low-noise source. The device accepts input reference frequency up to 1.4 GHz, which, when combined with frequency dividers and a programmable low-noise multiplier, allows flexible frequency planning. The high-speed N-divider has no pre-divider, thus significantly reduces the amplitude and number of spurs. The additional programmable low-noise multiplier allows users to mitigate the impact of integer boundary spurs. In fractional-N mode, the device can adjust the output phase by a 32-bit resolution. For applications that require fast frequency changes, the device supports a fast calibration option, which takes less than 20 μs. The LMX2594 adds support for generating or repeating SYSREF (compliant to JESD204B standard), which makes this device an ideal low-noise clock source for high-speed data converters. This configuration provides fine delay adjustment (9-ps resolution) to account for delay differences of board traces. This device uses a single 3.3-V supply and has integrated low-dropout linear regulators (LDOs) that eliminate the need for onboard low-noise LDOs.

2.2.2 ADC12DJ3200

The ADC12DJ3200 is an RF-sampling GSPS ADC with a –3-dB input bandwidth up to 8 GHz. The 12-bit ADC12DJ3200 can sample up to 3200 MSPS in dual-channel mode and up to 6400 MSPS in single-channel mode. The ADC12DJ3200 can sample signals in the 1st, 2nd, and higher Nyquist zones. The ADC12DJ3200 uses a high-speed JESD204B output interface with up to 16 serialized lanes and supports subclass-1 for deterministic latency and multi-device synchronization. The serial output lanes support up to 12.8 Gbps and can be configured to trade off bit rate versus the number of lanes. In dual-channel mode, optional digital down converters can tune and decimate a band from RF to a complex baseband signal to reduce the interface data rate in bandwidth-limited applications.

2.2.3 LMK04828

The LMK04828 is a dual-PLL jitter cleaner and clock generator for JESD204B systems. LMK04828 has 14 clock outputs from PLL2 that the user can configure to drive seven JESD204B converters or other logic devices using device and SYSREF clocks. The LMK04828 supports two ranges of VCOs: 2370 MHz to 2630 MHz and 2920 MHz to 3080 MHz. The LMK04828 also supports a distribution mode where the device accepts the high-frequency reference signal and distributes the signal to all 14 clock outputs without adding a PLL noise.

2.3 System Design Theory

Increasing the channel count in JESD204B clock generation is based on synchronization of board-to-board clocks, with a provision for phase alignment trimming and high-performance clock generation using the external clock source. This section describes the design details of the multiboard synchronization approach to achieve synchronized high-frequency JESD204B-complaint clocks.

2.3.1 Board-to-Board Clock Synchronization

To demonstrate the board-to-board synchronization, multiple boards are connected in a daisy-chain configuration, which requires the first clock source to provide the reference and sync signals to the next clocking device and chain to go further. A clock distribution device (LMK04828) can work in PLL mode or in distribution mode.

PLL mode requires a low-frequency reference signal and uses the internal VCO of the device to generate the clock signals. In PLL mode, the device adds the PLL noise, which can affect the overall performance of the generated clock signals. In distribution mode, the first device receives a high-frequency reference signal from the external clock source and distributes it to the next devices. This mode requires the least number of devices to obtain synchronized multiple clock boards; however, it increases the noise floor at each level of the daisy chain.

図 2 shows the daisy-chain configuration of multiple LMK04828 devices. In this design, the first clocking board receives the high-frequency external clock at the CLKin1 port of the LMK04828 and is configured in distribution mode. The next clocking board LMK04828 is synchronized with the previous LMK04828 using the reference signal at CLKin1 and the sync signal at CLKin0. Initially, the clocking board-1 LMK04828 device synchronizes its own internal dividers after receiving the external reference signal, so it has all-in phase DCLK and SDCLK. Then, the clocking board-2 LMK04828 device receives the bypass-delayed reference signal at CLKin1 from the previous board to synchronize the reference signals at both boards, after which it synchronizes the LMK04828 dividers using the SYNC signals at CLKin0. The end result is both clocking boards with synchronized LMK04828 outputs.

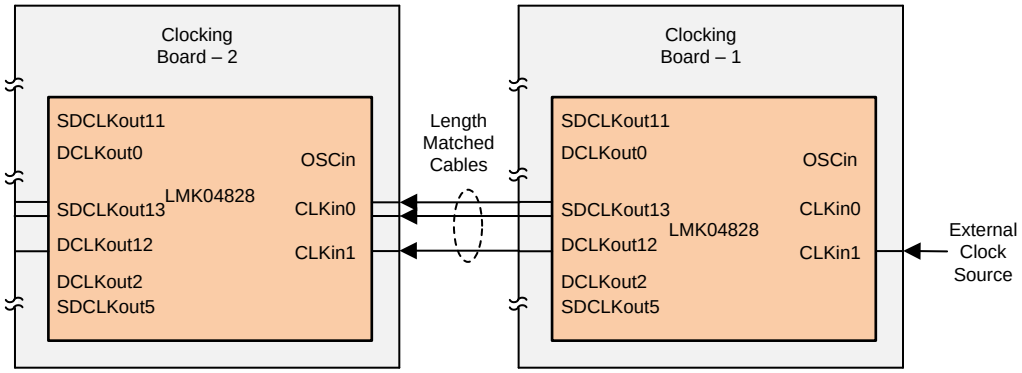


図 2. Daisy-Chain Configuration of Multiple LMK04828 Devices

In this design, the clocking board-1 LMK04828 receives a 1.2-GHz reference signal from an external source and bypasses the delayed 1.2-GHz DCLK to the next clocking board, divided the 37.5-MHz DCLKs to onboard LMX2594s, 300-MHz DCLK to FPGA, and 37.5-MHz SYSREF/SYNC signals after divider synchronization. The LMK04828 DCLKout12 output signal is fed to the next clocking board LMK04828 at CLKin1 and then sends the DC-coupled delayed-sync pulses through SDCLKout13 to synchronize the dividers and in-phase clocks with its own clocks. Then, the next board LMK04828 can generate the synchronized reference, SysRefReq, and SYNC signals to LMX2594 of the clocking boards and FPGA clocks to the capture cards. After synchronizing both boards, measure the clock skew; for which the results are available in 3.2.

The clocking boards LMK04828 must receive in-phase reference signals at the CLKin1 port to synchronize both devices in a daisy-chain configuration. The length of the cables from the clocking board 1 to clocking board 2 must be in the range of eq – 1, as the DCLK of LMK04828 has an analog delay range from 0 ps to 575 ps after enabling the analog delay, which adds a nominal 500 ps in addition to the programmed value.

$$\text{Cable length delay}: \left(\left(\frac{N}{F_{REF}}\right) - 500\right) \text{ to } \left(\left(\frac{N}{F_{REF}}\right) - 1075\right) \quad (1)$$

where,

- F_{REF} is the reference signal frequency (1.2 GHz) and N is an integer.

On clocking board 2, the CLKin0 path of the LMK04828 device must be modified for DC-coupled sync input signals. Remove the circled resistors R69 and R204 and replace capacitors C24 and C25 with 0201 0-Ω resistors, as 図 3 shows.

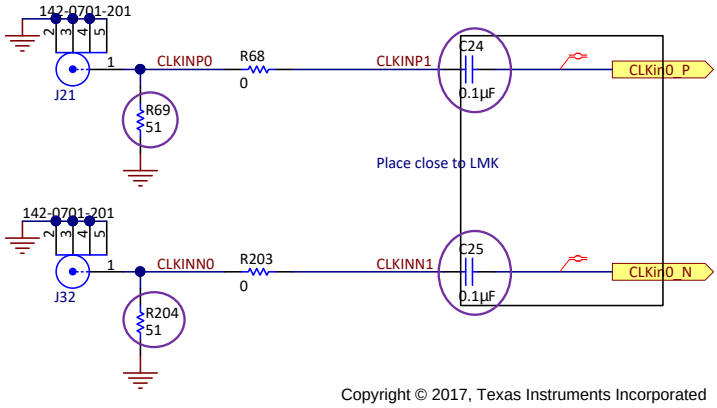


図 3. Clocking Board 2—LMK04828 CLKin0 Path Modification for DC-Coupled SYNC Inputs

2.3.2 LMX2594 Synchronized Clocks Output

図 4 shows the block diagram of the multichannel clocking board. In this design, the LMK04828 operates in distribution mode, which receives the 1.2-GHz reference clocks at the CLKin1 input and distributes 37.5 MHz at DCLKout1 and DCLKout2 as the reference input to both LMX2594 devices, 300 MHz as the FPGA clocks, and 37.5 MHz as the SYSREF output. To achieve phase synchronization, assign a common reference frequency input to the two LMX2594 synthesizers, the SYNC and SYSREFREQ signals from the LMK04828. To adjust slight mismatches in phase of the generated clocks, the LMX2594 provides a clock phase programming feature to program the clock phase using the MASH_SEED value. Each LMX2594 device may require tuning for the MASH_SEED and SYSREF delays to achieve in-phase generated clocks and the setup and hold time of the SYSREFs when interfaced with data converters. The operation and performance of both LMX2594s devices is equivalent to the device performance in the TIDA-01021 reference design; however, in this design, the devices receive the reference signal through DCLKout of the LMK04828 to maintain the synchronized reference signals in multiple boards.

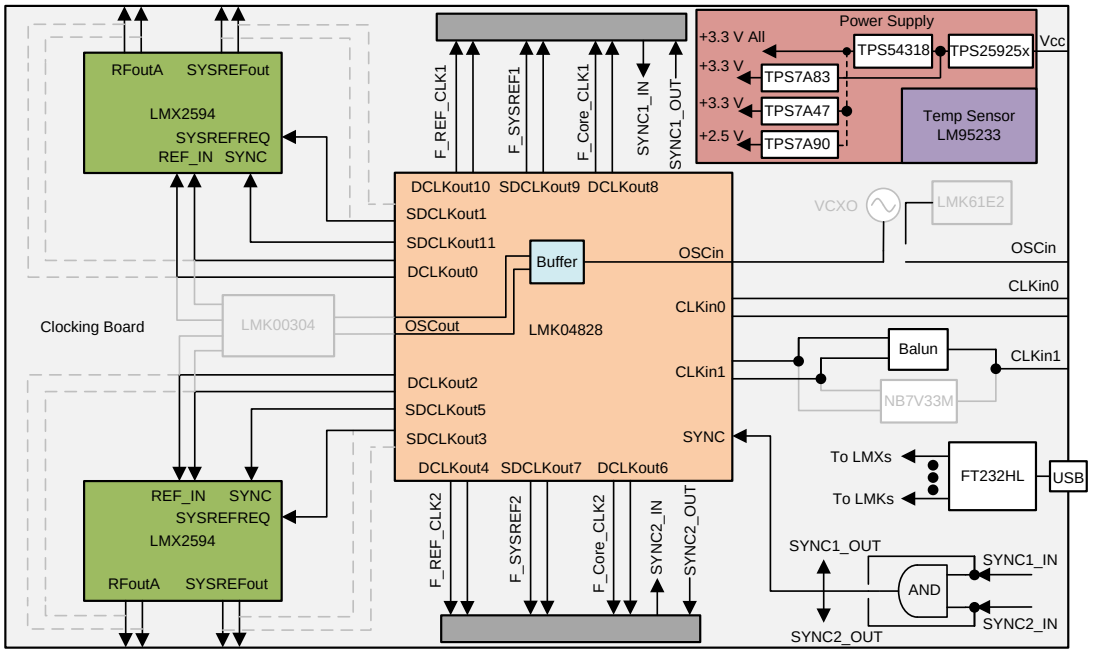


図 4. Block Diagram of Multichannel Clocking Board

In this design, the reference input path of the LMX2594 on the clocking boards must be modified. Remove the 0-Ω resistors R103, R165, R137, and R168 and mount 0402 0-Ω resistors at R274, R275, R108, R110, R278, R279, R141, and R143.

An input reference frequency of 37.5 MHz is provided to the clocking board LMX2594 devices by the LMK04828. The phase detector frequency also changes to 37.5 MHz. 表 2 lists the new loop filter configuration.

表 2. LMX2594 Loop Filter Component

COMPONENTS	VALUES
C62, C95	1.5 nF
C60, C93	56 nF
C59, C92	Open
C58, C91	1.8 nF
R96, R129	120 Ω
R95, R128	0 Ω
R94, R127	270 Ω

2.3.3 ADC12DJ3200 EVM Configuration

The design is validated with two channels of the ADC12DJ3200 EVM in a setup that uses two sets of ADC12DJ3200 EVMs to measure the impact of the scalable, multichannel clocking solution. The ADC12DJ3200 can reach up to a 3.2-GHz clock frequency, but the TSW14J56 capture card is limited at a 12-Gsps data rate, which limits the clocking frequency of the ADC. For these reasons, the ADC clock frequency is set to 3 GHz. The ADC12DJ3200 operates in dual-channel mode (JMODE2) where the input for only one channel is provided and output from the corresponding ADC core is captured.

The clocking board LMK04828 is used in this design to provide the reference signals to the LMX2594, FPGA reference clock, a core clock, and SYSREF to the TSW14J56 capture card through the FMC+ adapter board. The reference and core clock frequency of the FPGA are 300 MHz and the SYSREF frequency is 37.5 MHz. The adapter board also provides the interface between the ADC EVM and the capture card because it connects the ADC lanes to the FPGA. Various input signals are provided at the ADC input for SNR measurement. 3.2 shows these results.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

3.1.1.1 Clocking Boards Setup

図 5 shows an image of the multichannel clocking board with the hardware configuration for each clocking board.

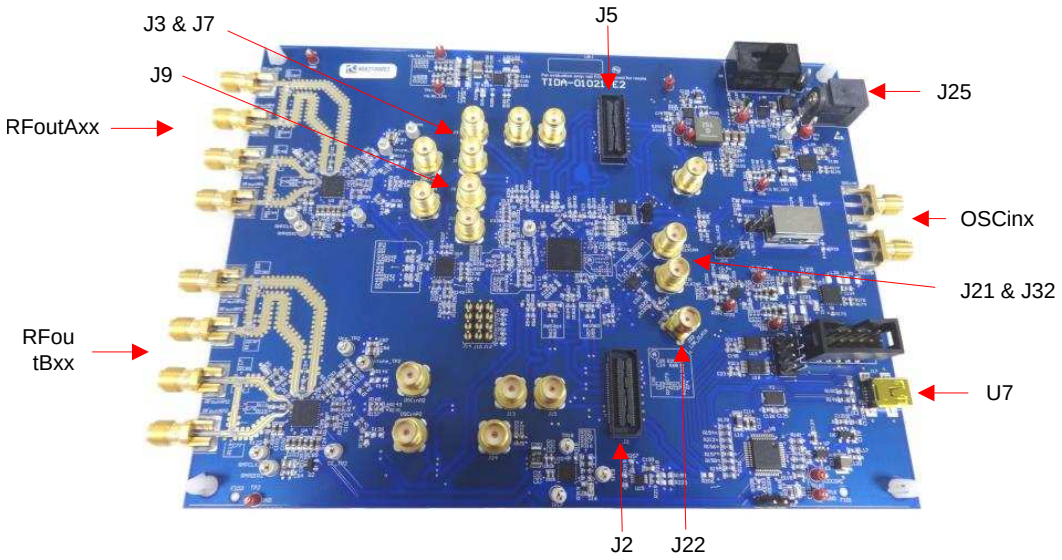


図 5. Multichannel Clocking Board Hardware

Power:

- Power supply connector J25: This connector is used to connect the power supply. Set the power supply to 5 V with a 2-A current limit.

Input reference signals:

- Option 1: The onboard VCXO Y1 is powered on using the jumper J8 and outputs a 100-MHz signal to the LMK04828 OSCin* pin input. While using Y1, disconnect the clock inputs from LMK61E2 (U2) and external reference by removing R36 and R38. At the same time, isolate the power supply to U2 by removing the jumper J16.
- Option 2: The onboard reference LMK61E2 (U2) is powered on using the jumper J16 and factory programmed to generate a 156-MHz LVDS output. U2 can be programmed to generate different clock frequencies using the I²C interface. While using U2, disconnect the clock inputs from Y1 and the external reference by removing C179, R37, and R39 then place R36 and R38. Isolate the power supply to Y1 by removing J8.
- Option 3: Connect the external reference to external OSCinP and OSCinN connectors. While connecting the external reference, disconnect the Y1 and U2 connection by removing C179, R45, and R46 and place R36 and R38. Disconnect the power supply of Y1 and U2 by removing jumpers J8 and J16.

- Option 4: One of the previous options are used when LMK04828 works in PLL mode. When LMK04828 is operating in distribution mode, connect the external reference to external connector J22. While operating in distribution mode, power down Y1 and Y2 by removing jumpers J8 and J16.

Input sync signal:

- Connect the external sync signal at external J21 and J32 connectors to reset the LMK04828 dividers.

Output signals:

- RFoutAP1, RFoutAM1, RFoutAP2, and RFoutAM2 connectors generate the DCLK and are connected to ADC EVMs to measure the SNR.
- RFoutBP1, RFoutBM1, RFoutBP2, and RFoutBM2 connectors generate the low-frequency SYSREF signals.
- Connectors J2 and J5 generate the FPGA CLKs and SYSREFs for two channels.

Programming interface:

- Connect the USB mini cable to the onboard USB connector U7 and test PC to program the clocking board devices using the High Speed Data Converter (HSDC) TID GUI.

3.1.1.2 FMC+ to FMC Adapter Board Setup

The FMC+ to FMC adapter board has connections to take FPGA clocks from the clocking or ADC12DJ3200 EVM. Follow the schematic in *4.1* to connect the FPGA clocks and SYSREFs from the clocking board.

3.1.1.3 ADC12DJ3200 EVM Setup

See *ADC12DJ3200 Evaluation Module User's Guide* for the ADC12DJ3200 EVM hardware setup procedure. The ADC12DJ3200 EVM has both internal and external options for clocking the ADC. Select the DEVCLK based on the placement of capacitors on the shared pads. Connect C49 and C50 for the external DEVCLK. Connect the external SYSREF for the ADC at connector J38 from the clocking board.

3.1.1.4 TSW14J56 Setup

See *TSW14J56 JESD204B High-Speed Data Capture and Pattern Generator Card User's Guide* for the TSW14J56 EVM hardware setup procedure.

3.1.2 Software Configuration

After connecting and modifying the boards, configure all the devices in multiple boards.

3.1.2.1 Board to Board Synchronization Programming Sequence

1. Download the HSDC TID GUI software from TI.com and install the program on two different test PCs to program the clocking board devices. 図 6 shows the HSDC TID GUI.
2. To synchronize the multiple board clocks:
   - Clocking board 1
     - Feed the external reference signal at J22 (CLKin1).
     - Load the *1024_BRD1_LMK04828_1200MREF_300MFCLK_37.5MSYSREF_Master.cfg* configuration file in HSDC TID GUI to program the LMK04828 device in distribution mode.
     - Load the *1024_BRD1_LMK04828_Divider_Sync.cfg* configuration file in HSDC TID GUI to synchronize the LMK04828 dividers.
   - Clocking board 2
     - Load the *1024_BRD2_LMK04828_1200MREF_300MFCLK_37.5MSYSREF_Slave.cfg* configuration file in HSDC TID GUI to program the LMK04828 device in distribution mode.
   - Clocking board 1

– Press the *Write Register* button for address 0x13E in LMK04828 to send sync pulses to the next clocking board LMK04828 device to reset the dividers, as 図 6 shows.

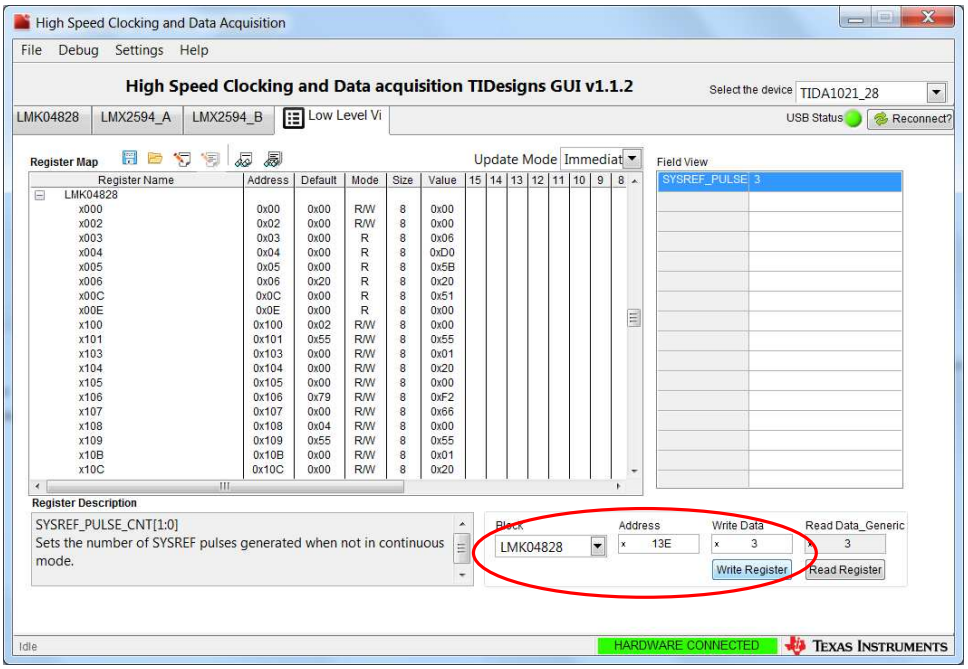


図 6. HSDC TID GUI

- Clocking board 2
  - Load the *1024_BRD2_LMK04828_SYNC_OFF_SYSREF_Conti.cfg* configuration file in HSDC TID GUI to “Disable SYNC on all Dividers” and place the LMK04828 SYSREF outputs in continuous mode.
- Clocking board 1
  - Load the *1024_BRD1_LMX2594_A_B_3GCLK_37.5MREF_37.5MPFD.cfg* configuration file in HSDC TID GUI to “Disable SYNC on all Dividers” of the LMK04828 and configure the LMX2594 devices.
- Clocking board 2
  - Load the *1024_BRD2_LMX2594_A_B_3GCLK_37.5MREF_37.5MPFD.cfg* configuration file in HSDC TID GUI to configure the LMX2594 devices.
- Clocking board 1 and 2
  - After configuring ADC EVMs, load the *LMX2594_A_B_SYSREF_OFF.cfg* configuration file in both HSDC TID GUI for SYSREF section OFF of the LMX2594 device.

3.1.2.2 ADC12DJ3200 EVM Programming

Download the ADC12DJxx00 GUI from TI.com to program the ADC12DJ3200 EVM. The ADC12DJ3200 and LMK04828 devices are configured for SNR measurement in the ADC12DJ3200 EVM, as shown in 図 7. The LMK04828 is programmed in distribution mode for the CLKin0 drive to configure SYSREF directly. The ADC12DJ3200 EVM is put into JMODE2 mode to use in dual-channel mode at the full Nyquist zone of the device. The EVM is set up in external clock source selection mode with a sampling frequency of 3000 Msps. Load the configuration files in the low-level view page of the ADC12DJ3200 GUI.

The programming sequence for the ADC12DJ3200 EVM is as follows:

1. Load the configuration file *1024_ADC_EVM_LMK04828_SYSREF_Bypass.cfg* for LMK04828 and bypass the ADC SYSREF signal.
2. Load the ADC configuration file *1024_ADC12DJxx00_JMODE2_SRC_EN.cfg* for ADC programming

and SYSREF auto calibration.

3. Load the ADC configuration file *1024_ADC12DJxx00_JMODE2_SRC_clear.cfg* for ADC SYSREF auto calibration OFF.

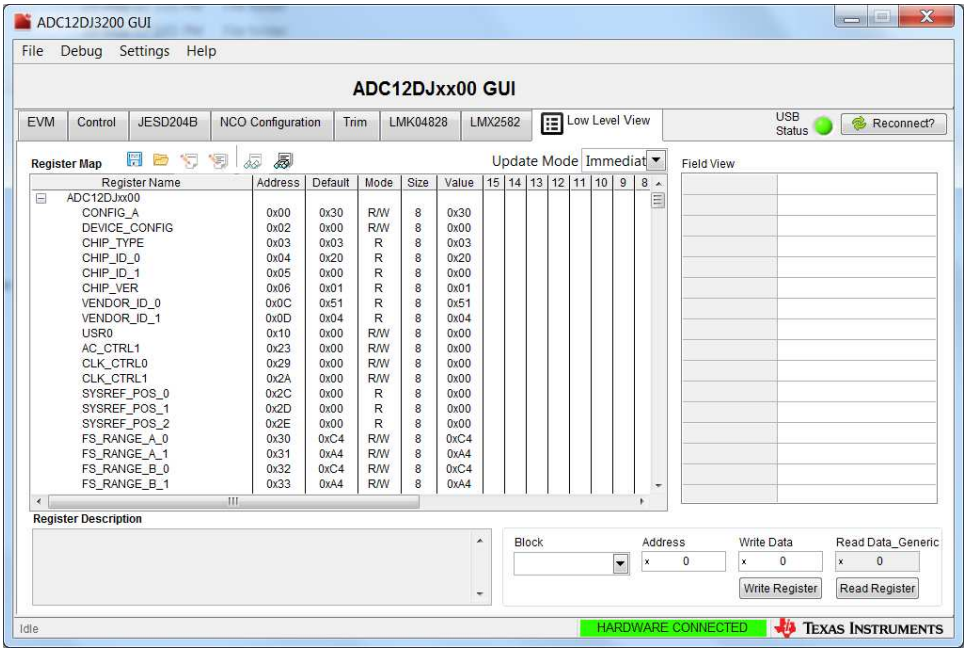


図 7. ADC12DJ3200 EVM Programming

3.1.2.3 HSDC Pro Setup

The HSDC Pro software interfaces with the TSW14J56 EVM to capture and analyze the digital data from the ADC12DJ3200 regarding SNR measurements. See *TSW14J56 JESD204B High-Speed Data Capture and Pattern Generator Card User's Guide* for the HSDC Pro setup to capture and analyze the data.

3.2 Testing and Results

3.2.1 Test Setup

図 8 shows the test setup for multiboard clock skew and 図 9 shows the test setup for ADC SNR and channel-to-channel skew measurement. In both figures, the circled number shows the clock channel number.

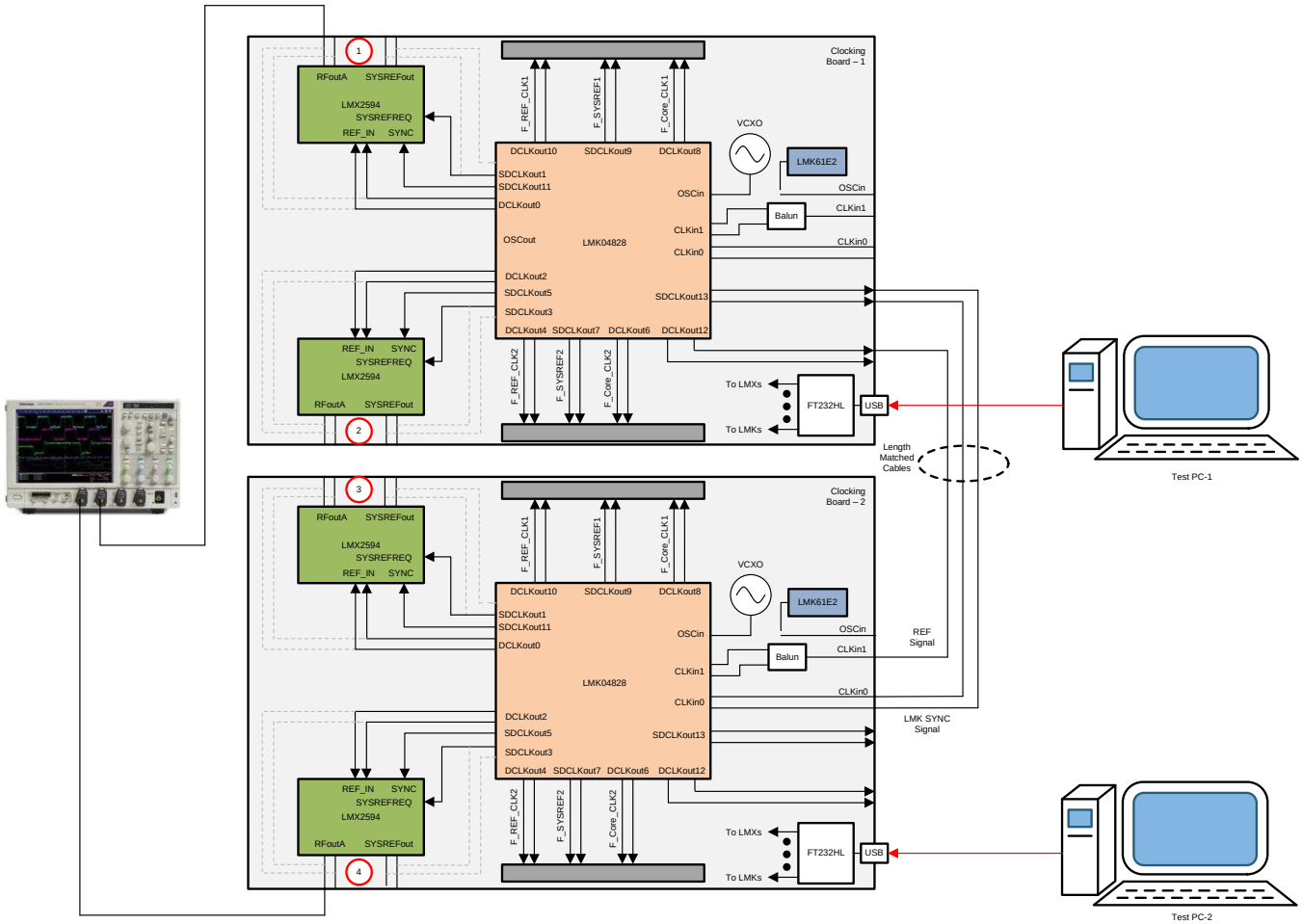


図 8. Test Setup for Multiboard Clock Skew Measurement

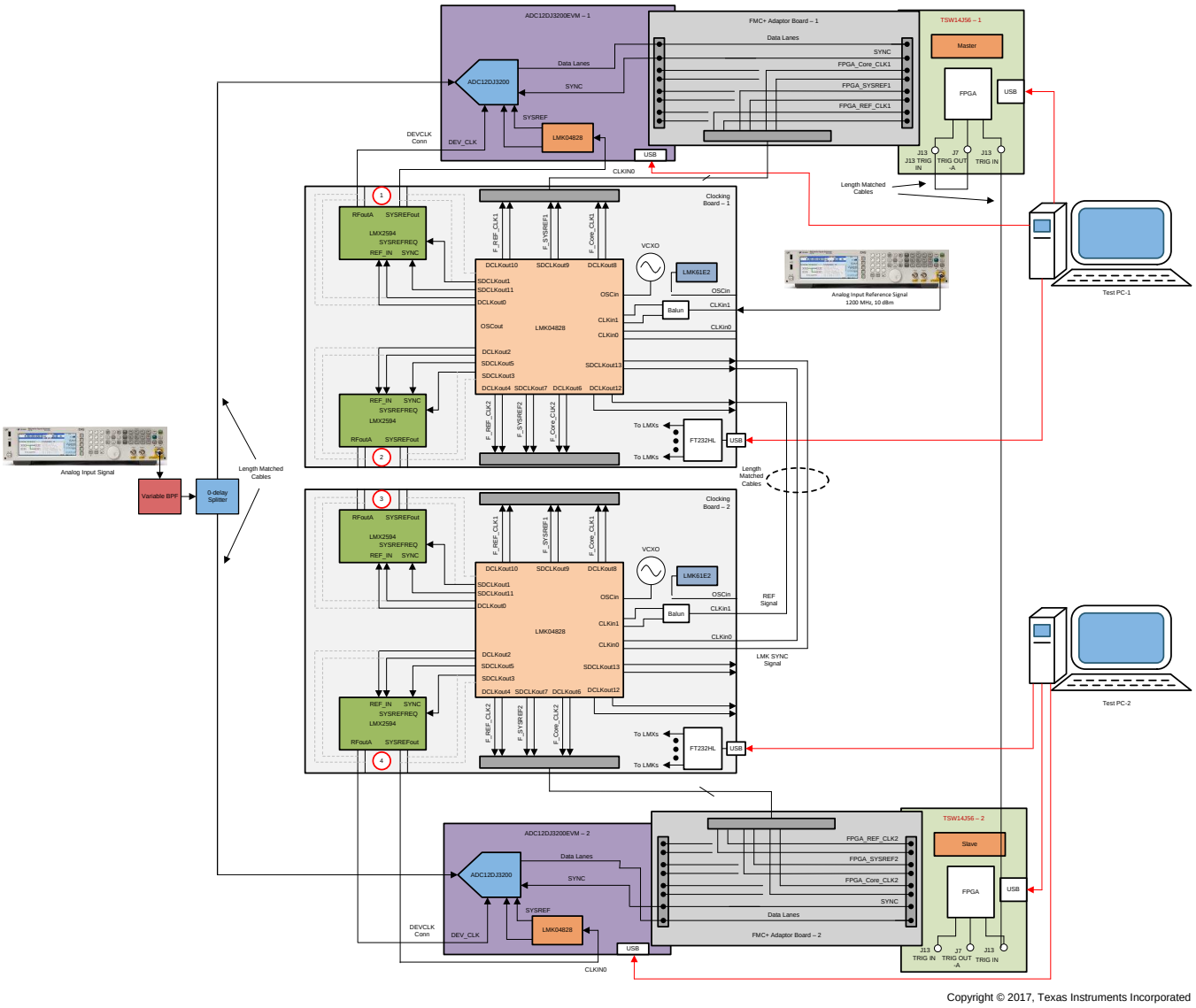


図 9. Test Setup for ADC12DJ3200 SNR and Channel-to-Channel Skew Measurement

3.2.2 Test Results

3.2.2.1 Board-to-Board Clock Phase Alignment

As explained in 2.3.1, scaling up the synchronized clocks is critical for high-channel-count systems. In this test, the clocks of the multiboard are synchronized at 3-GHz DEV_CLKs, which are generated by the LMX2594s devices. The minimum skew between the clocks reflects the minimum channel-to-channel skew in multichannel systems. 図 10 shows the clock skew between channel 1 and 4 (as shown in 図 8), which is less than 10 ps. The skew of the clocks among all channels is less than 10 ps, which the results do not show. As a result, the channel-to-channel skew in high-count multichannel systems is reduced.

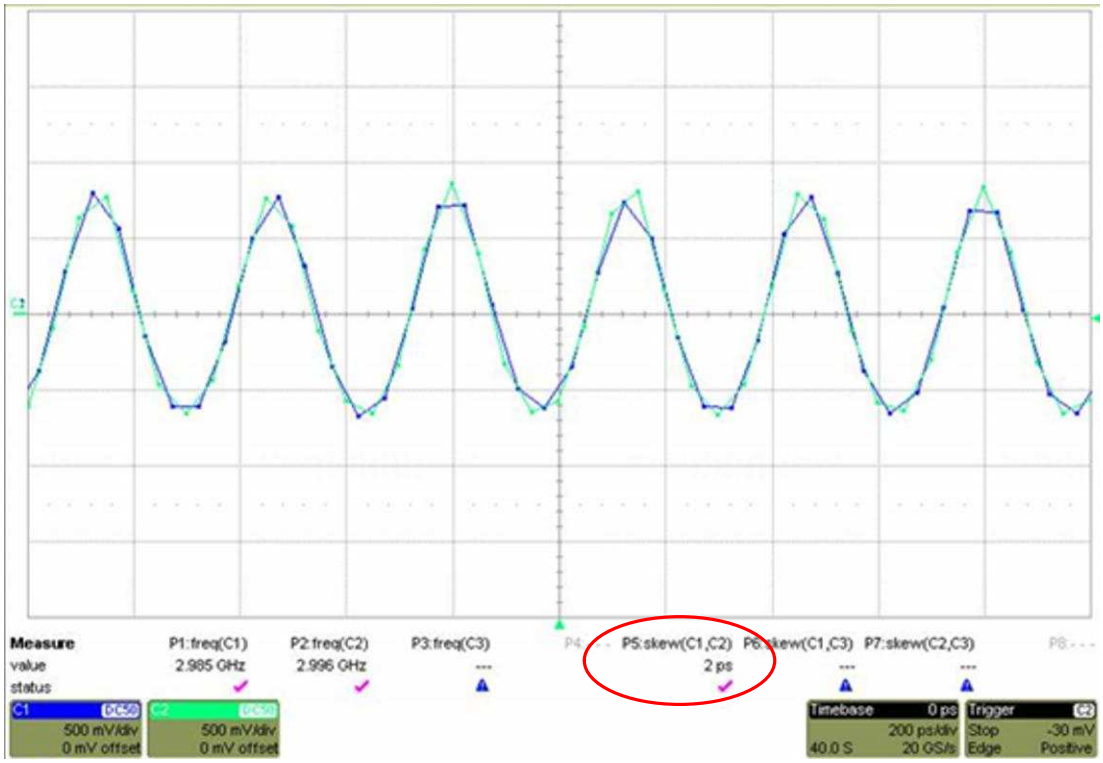


図 10. Board-to-Board Clock Measured Skew

3.2.2.2 Multichannel Signal Performance and Skew Measurement

表 3 shows the measured SNR performance of the ADC12DJ3200 EVM-1 at various frequencies for –1-dBFS differential inputs and dual-channel mode (JMODE2). The ADC12DJ3200 EVM-2 channels also show the same performance as ADC12DJ3200 EVM-1. The measured SNR of the ADC12DJ3200 with the proposed TIDA-01024 clocking solution is improved as compared to the ADC12DJ3200 EVM onboard clocks.

表 3. Measured SNR

INPUT FREQUENCY (MHz)	ADC DATA SHEET SNR (dBFS)	MEASURED SNR ON ADC12DJ3200EVM WITH ONBOARD CLOCK (dBFS)	MEASURED SNR ON ADC12DJ3200EVM WITH TIDA-01024 CLOCKS (dBFS)
997	56.3	55.25	55.4
2482	55.2	52.71	53.38

図 11 and 図 12 show the spectrum results at a 3000-MHz sampling frequency in dual-channel mode.

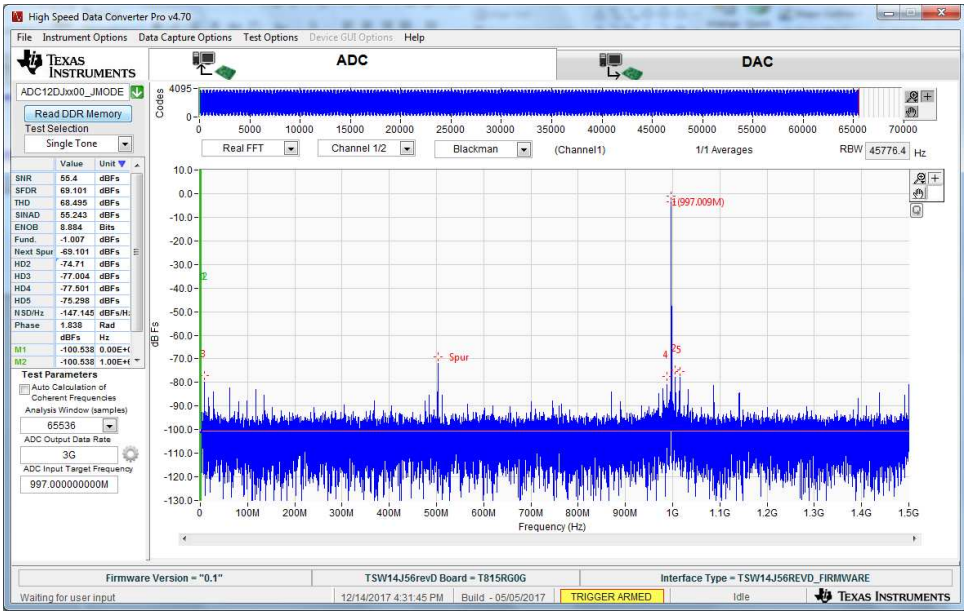


図 11. Spectrum at 997-MHz Input

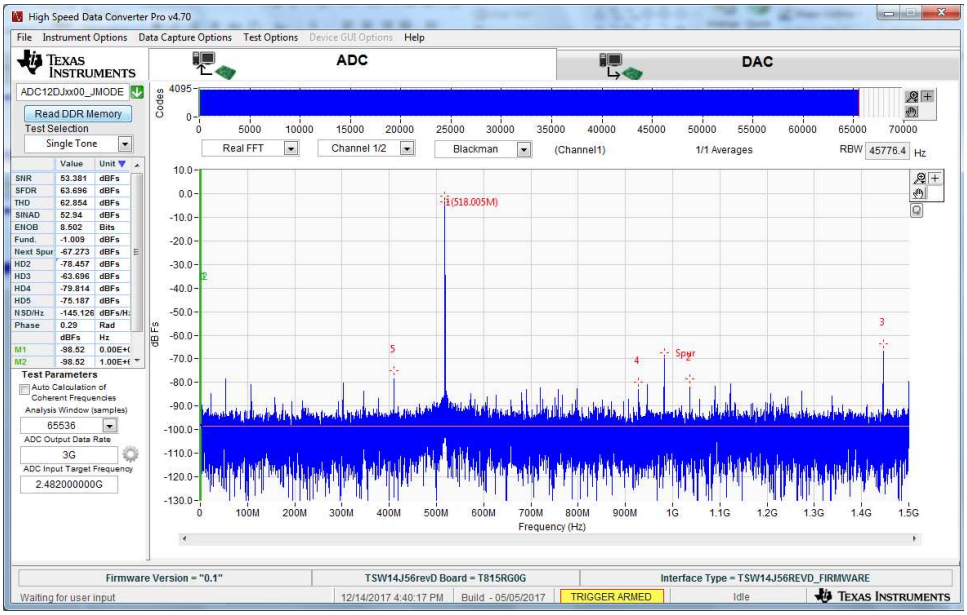


図 12. Spectrum at 2482-MHz Input

表 4 shows the time skew between two ADC12DJ3200 EVM channels at different input frequencies. Evaluate this skew by calculating the phase difference between the signals captured from each ADC using MATLAB and the example program in 8. The clocks are fed to both ADC12DJ3200 from clock channel 1 and 4, as 図 9 shows, and the measured time skew is valid for any clock channel combination. The measurements taken at a 3-GHz sampling frequency and the measured time skew was less than 50 ps for each of the input frequencies.

表 4. Measured Channel-to-Channel Skew

INPUT FREQUENCY (MHz)	MEASURED TIME SKEW (ps)
997	5.8
2482	5.4

図 13 shows a plot of the output samples of the two ADCs for a 997-MHz input, which is in the first Nyquist zone for a 3000-MHz sampling clock. 図 14 shows a plot of the output samples for a 2482-MHz input, which is in the second Nyquist zone for a 3000-MHz sampling clock. The 2482-MHz input signal aliases to 518 MHz and a phase difference of 4.7° is measured, which translates to a channel-to-channel skew of 5.4 ps for the 2482-MHz input.

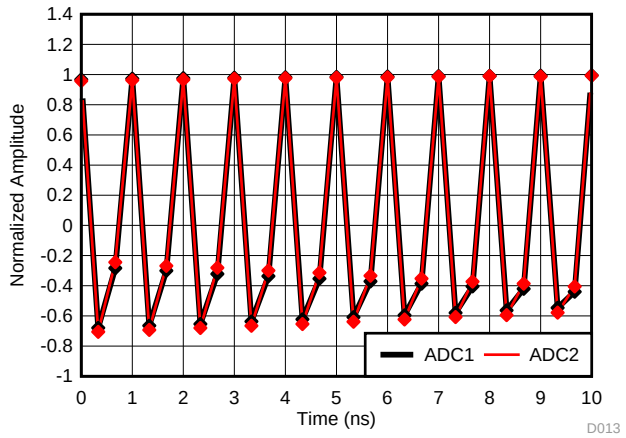


図 13. Sampled Signals at 997-MHz Input

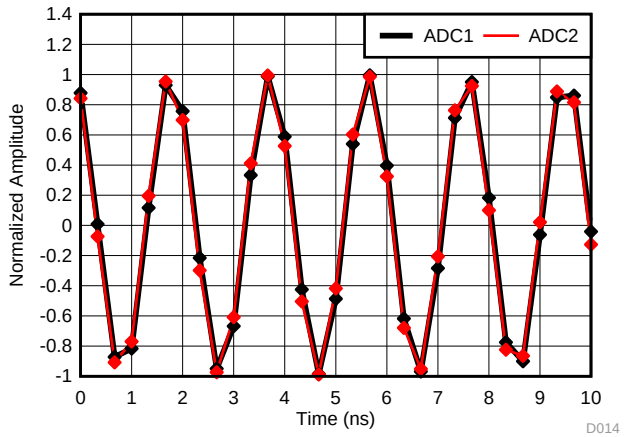


図 14. Sampled Signals at 2482-MHz Input

3.2.2.3 Summary and Conclusion

The TIDA-01024 design is a high-channel-count, JESD204B-compliant, daisy-chain clocking reference design that can be used for radar and 5G wireless testers. This reference design demonstrates multichannel, high-performance (low phase noise), phase-synchronized clock generation in a daisy-chain configuration using the LMX2594 and LMK04828 devices with a high-frequency external clock source and clock-to-clock skew of less than 10 ps. This design also demonstrates the clocking impact on the ADC12DJ3200 EVM system performance after replacing the onboard clocks with TIDA-01024 output clocks. The system SNR improves by 0.2 dB to 0.5 dB using the ADC12DJ3200EVM with the proposed clocking solution and with a clock skew of less than 10 ps. The system shows deterministic latency behavior for every power ON cycle, with the analog input channel-to-channel skew at less than 50 ps.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01024.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01024.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01024.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01024.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01024.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01024.

5 Software Files

To download the software files, see the design files at TIDA-01024.

6 Related Documentation

1. Texas Instruments, *Multichannel JESD204B 15-GHz Clocking Reference Design for DSO, Radar, and 5G Wireless Testers*
2. Texas Instruments, *ADC12DJ3200 Evaluation Module User's Guide*
3. Texas Instruments, *TSW14J56 JESD204B High-Speed Data Capture and Pattern Generator Card User's Guide*

6.1 商標

E2E is a trademark of Texas Instruments.
すべての商標および登録商標はそれぞれの所有者に帰属します。

7 About the Author

AJEET PAL is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the Test and Measurement sector. Ajeet has six years of experience in RF and wireless subsystem design for cellular and wireless systems. Ajeet earned his Bachelor of Engineering in electronics and communication engineering from the Institute of Technology & Management (ITM) University at Gwalior, and his Masters of Technology in RF and microwave engineering from the Indian Institute of Technology (IIT) in Kharagpur, India.

SANKAR SADASIVAM is a system architect at Texas Instruments, where he is responsible for architecting and developing reference design solutions for the industrial systems with a focus on Test and Measurement for the Industrial Systems Engineering team. Sankar brings his extensive experience in analog, RF, wireless, signal processing, high-speed digital, and power electronics to this role. Sankar earned his Master of Science (MS) in electrical engineering from the Indian Institute of Technology, Madras.

8 Appendix A

Example Matlab Program for Analyzing Skew

```
%-------------------------------------------------------%
% Import Data                    %
%-------------------------------------------------------%

data1 = xlsread('read_csv1.csv',1,'A1:A65536');
data2 = xlsread('read_csv2.csv',1,'A1:A65536');

Fs = 3000e6;
Fin = 997e6;
N = length(data1);
num_bits = 15;

samples_board_1 = data1;

% remove offset for board 1
samples_board_1 = double(samples_board_1);
samples_board_1 = samples_board_1 - mean(samples_board_1);
mean(samples_board_1)

samples_board_2 = data2;

% remove offset for board 2
samples_board_2 = double(samples_board_2);
samples_board_2 = samples_board_2 - mean(samples_board_2);
mean(samples_board_2)

%-------------------------------------------------------%
% Analyze Skew                                         %
%-------------------------------------------------------%

% Plot time domain data for each board.
figure(1);
plot(1:length(samples_board_2),samples_board_2,...
1:length(samples_board_1),samples_board_1);
title('Time Domain Plot');

% Get FFT of for each board.
window = blackman(N);
X=fftshift(fft(window.*samples_board_2));
Y=fftshift(fft(window.*samples_board_1));
X = X(N/2:end);
Y = Y(N/2:end);
A = 2^(num_bits-1);

figure(3);
plot((0:N/2)*(Fs/N), 20*log10(abs(X*2/N/A)));
title('FFT Plot of Board 2');

figure(2);
plot((0:N/2)*(Fs/N), 20*log10(abs(Y*2/N/A)));
title('FFT Plot of Board 1');

% Find the bin with the largest amplitude. This is the sine wave.
```

```
[mag_x index_x] = max(abs(X));
[mag_y index_y] = max(abs(Y));

% Get the phase of each signal at the appropriate bin.
phase_x = angle(X(index_x));
phase_y = angle(Y(index_y));

% Calculate the phase difference and time skew.
phase_diff = phase_y - phase_x;
phase_diff_deg = phase_diff / pi * 180;


Fin = 0.5*Fs*((index_x-1)/(length(X)-1));

skew_ps = phase_diff / (2*pi*Fin) / 1e-12;

if(skew_ps >= 0)
    fprintf('Board2 lags Board1 by %f degrees or %f ps for Fin = %f MHz',...
    phase_diff_deg, skew_ps, Fin*1e-6);
else
    fprintf('Board1 lags Board2 by %f degrees or %f ps for Fin = %f MHz',...
    -phase_diff_deg, -skew_ps, Fin*1e-6);
end
```

TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関係する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、もしくは、TIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。