参考資料

TI Designs: TIDA-01057
20ビットADCへの真の10V_{PP}差動入力で信号ダイナミック・レンジを最大化するリファレンス・デザイン

概要

この高性能データ収集(DAQ)リファレンス・デザインは、20ビット差動入力アナログ/デジタル・コンバータ(ADC)のダイナミック・レンジを拡大できます。多くのDAQシステムには、十分な信号ダイナミック・レンジを確保するために、広いフルスケール範囲での測定能力が必要とされます。従来の逐次比較型(SAR) ADC用リファレンス・デザインの多くは、THS4551完全差動アンプ(FDA)を採用していますが、THS4551は最大電源電圧が5.4Vに制限されるため、基準電圧5VでSAR ADCのダイナミック・レンジを最大化するために必要な、真の10V_{PP}差動出力(10V FSR)を実現するには十分でありません。このリファレンス・デザインでは、最大電源電圧12.6VのTIのTHS4561 FDAを実装して、真の10V_{PP}差動出力の利点を追求しました。テストの結果によれば、このリファレンス・デザインは旧デザイン(TIDA-01054)に比べて優れた性能を実現し、全体的な消費電力も削減できます。

リソース

TIDA-01057	デザイン・フォルダ
THS4561	プロダクト・フォルダ
ADS8900B	プロダクト・フォルダ
REF6050	プロダクト・フォルダ

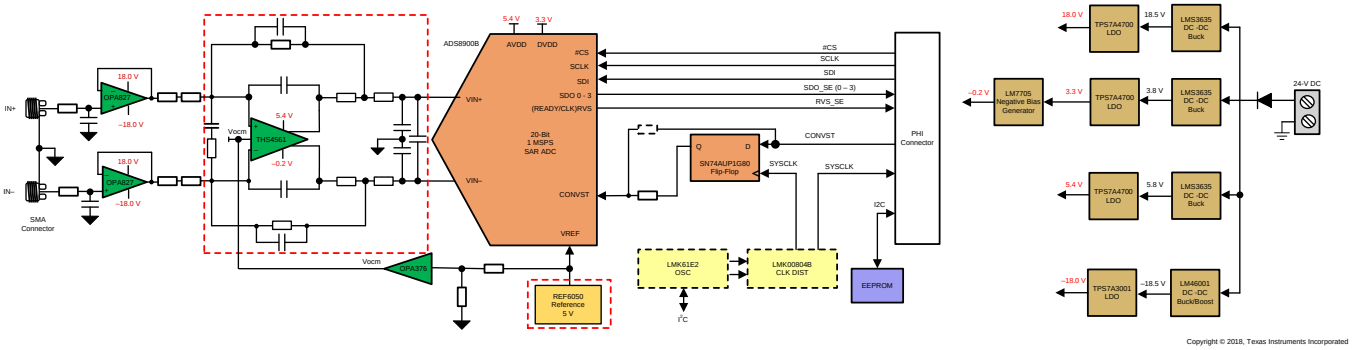
TI E2E™ Community　E2E™エキスパートに質問

特長

- 20ビットADCへの真の10V_{PP}差動アナログ・フロントエンド
- チャネル数の多いシステムを実現するモジュール式のフロントエンド・リファレンス・デザイン(反復可能)

アプリケーション

- データ収集(DAQ)
- 半導体試験用機器
- LCD試験用機器
- ラボ計測機器
- バッテリ試験装置



1 System Description

Multi-input systems that require the simultaneous or parallel sampling of many data channels present design challenges to engineers developing data acquisition (DAQ) modules and automatic testers for applications such as semiconductor tests, memory tests, liquid-crystal display (LCD) tests, and battery tests. In these systems, often hundreds or thousands of data channels are required; thus, maximizing the signal-to-noise ratio (SNR) performance while minimizing power, component count, and cost are all key design criteria. The analog front-end (AFE) signal chain often consists of a series of muxes, a scaling or programmable gain amplifier (PGA) followed by an anti-aliasing, noise limiting, low-pass filter (LPF), which is paired with the appropriate analog-to-digital (ADC) driver prior to digitization. The ADC converts the time-varying analog input to either a serial or parallel binary bit stream, which is then passed to the embedded host controller (microcontroller (MCU) or field-programmable gate array (FPGA)). Depending on the application, the ADC may contain the necessary reference or the associated buffer integrated as part of the ADC. Furthermore, the designer can also integrate portions of or the entire AFE as a single device for specific applications; however, note that this integration can also limit flexibility.

図 1 shows a block diagram of a generic AFE.

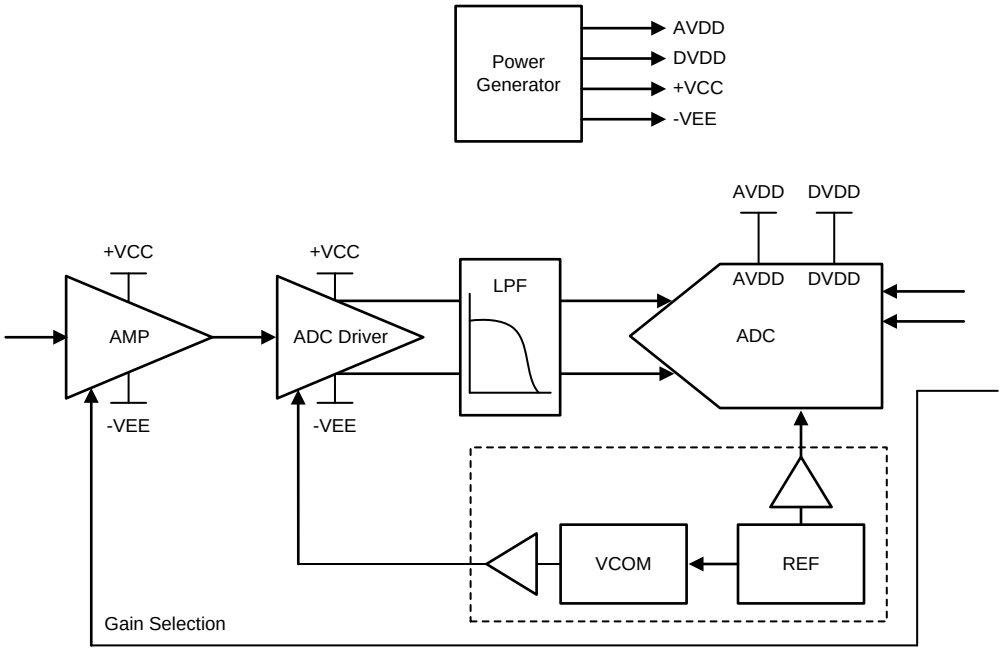


図 1. Generic AFE

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	MEASUREMENT
Number of channels	Dual	Dual
Input type	Differential	Differential

表 1. Key System Specifications (continued)

PARAMETER	SPECIFICATIONS	MEASUREMENT
Input range	10-V_{PP} fully differential	10-V_{PP} fully differential
Resolution	20 bits	20 bits
SNR	> 100.13 dB	100.95 dB
THD	< –123 dB	–124.5 dB
ENOB	> 16.34 bit	16.47 bits
System power	< 2.5 W	1.92 W
Form factor (L × W)	120 × 100 mm	112.98 × 99.82 mm

2 System Overview

2.1 Block Diagrams

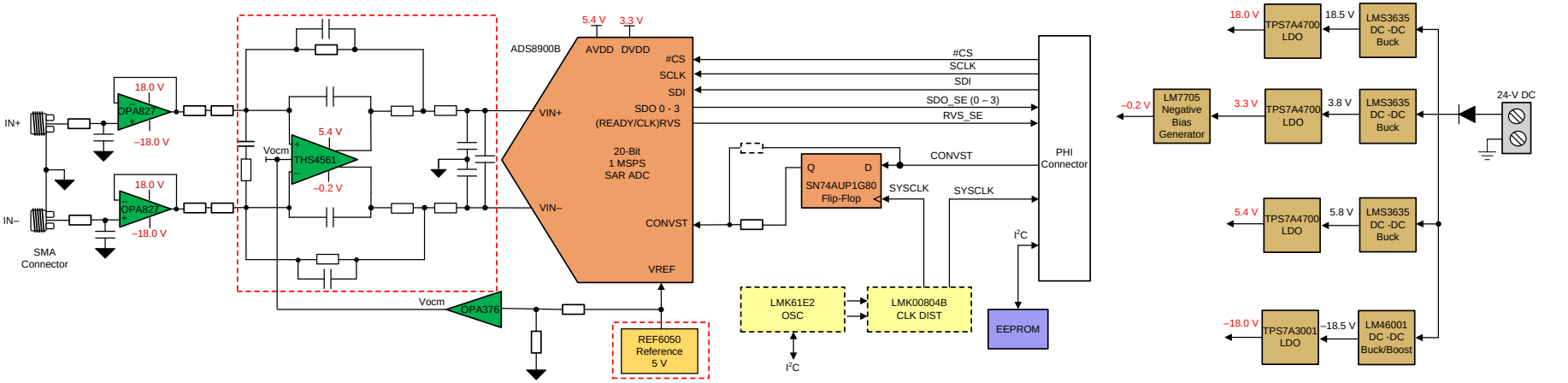


図 2. System Block Diagram

2.2 Highlighted Products

2.2.1 THS4561

The THS4561 FDA offers a simple interface from single-ended sources to the differential output required by high-precision ADCs. Designed for exceptional DC accuracy, low noise, and ultra-low harmonic distortion, the device is well suited for data acquisition systems where high precision is required with the best SNR and spurious-free dynamic range (SFDR) through the amplifier and ADC combination.

The THS4561 features the required negative rail input when interfacing a DC-coupled, ground-centered, source signal to a single-supply, differential-input ADC. Very-low DC error and drift terms support the emerging 16-bit to 20-bit SAR input requirements. A 2.85-V to 12.6-V supply range with a flexible output common-mode setting with low headroom to the supplies supports a wide range of ADC input and digital-to-analog converter (DAC) output requirements.

In this reference design, the THS4561 functions as a part of the ADC driver because it requires a high power supply range to realize the 10-V FSR.

2.2.2 REF6050

The REF6000 family of voltage references have an integrated, low-output impedance buffer that enable the user to directly drive the REF pin of precision data converters, while preserving linearity, distortion, and noise performance. Most precision SAR and delta-sigma ($\Delta\sum$) ADCs switch binary-weighted capacitors onto the REF pin during the conversion process. To support this dynamic load, the output of the voltage reference must be buffered with a low-output impedance (high-bandwidth) buffer. The REF6000 family devices are well suited, but not limited, to drive the REF pin of the ADS88xx family of SAR ADCs, ADS127xx family of $\Delta\sum$ ADCs, as well as other DACs.

The REF6000 family of voltage references are able to maintain an output voltage within 1 least significant bit (LSB), which is 18-bit, with minimal droop, even during the first conversion while driving the REF pin of the ADS8881 device. This feature is useful in burst-mode, event-triggered, equivalent-time sampling, and variable-sampling-rate data-acquisition systems. The REF60xx variants of the REF6000 family specify a maximum temperature drift of just 5 ppm/°C and initial accuracy of 0.05% for both the voltage reference and the low output impedance buffer, combined.

2.2.3 ADS8900B

The ADS8900B, ADS8902B, and ADS8904B (ADS890xB) belong to a family of pin-to-pin compatible, high-speed, single-channel, high-precision, 20-bit SAR ADCs with an integrated reference buffer and integrated LDO. The device family includes the ADS891xB (18-bit) and ADS892xB (16-bit) resolution variants.

The ADS89xxB boosts analog performance while maintaining high-resolution data transfer by using TI's Enhanced-SPI feature. Enhanced-SPI enables the ADS89xxB to achieve high throughput at lower clock speeds, which simplifies the board layout and lowers the overall system cost. Enhanced-SPI also simplifies the host's clocking-in of data, which makes it ideal for applications involving FPGAs and digital signal processors (DSPs). The ADS89xxB is compatible with a standard serial peripheral interface (SPI).

The ADS89xxB has an internal data parity feature which can be appended to the ADC data output. ADC data validation by the host, using parity bits, improves system reliability

2.3 System Design Theory

2.3.1 Power Structure

This system requires a wide variety of voltage rails to meet the specification of the reference design. The input voltage required for the system is 24-V DC. The power tree in 図 3 shows and highlights the distribution of the power into the different required rails. In this reference design, 5.4 V is generated to operate the REF6050 and THS4561 devices. The LM7705 device generates –0.2 V so that the THS4561 device can swing rail to rail without distortion. For this reason, select an ADC driver amplifier such that its power supply voltage tolerance is over 5.6 V, which is the primary reason for using the THS4561 in this reference design. For a detailed design description of the entire power system, see TIDA-01052 and TIDA-01054.

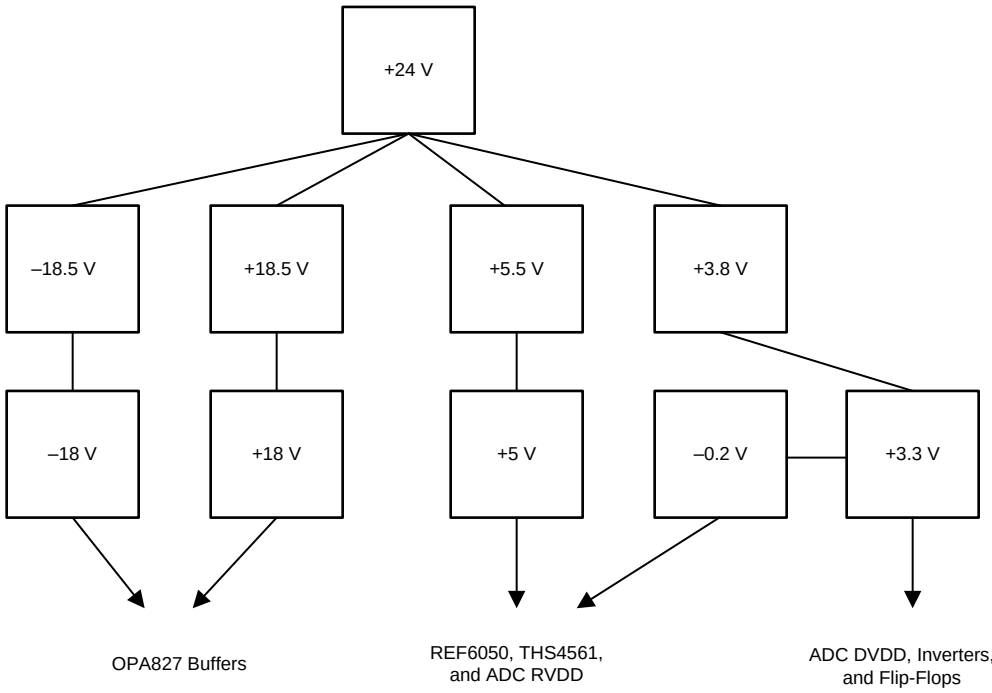


図 3. System Power Tree

2.3.2 ADC Driver Design Theory

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a flywheel RC filter. The amplifier is used for signal conditioning of the input signal and its low output impedance provides a buffer between the signal source and the switched capacitor inputs of the ADC. The RC filter helps attenuate the sampling charge injection from the switched capacitor input stage of the ADC and functions as an antialiasing filter to band-limit the wideband noise contributed by the front-end circuit. Careful front-end circuit design is required to meet the resolution, linearity, and noise performance capabilities of the ADS8900B. The input operational amplifier (op amp) must support the following key specifications:

1. Rail-to-rail input and output (RRIO)
2. Low noise
3. High small-signal bandwidth with low distortion at high frequencies
4. Low power

For DC signals with fast transients that are common in a multiplexed application, the input signal must settle within a 20-bit accuracy at the device inputs during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, the amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired 20-bit accuracy. Therefore, the designer must verify the settling behavior of the input driver within a simulator, such as the TINA-TI™ simulation software, to help select the appropriate amplifier.

Converting analog-to-digital signals requires sampling an input signal at a constant rate. Any higher-frequency content in the input signal beyond half the sampling frequency is digitized and folded back into the low-frequency spectrum of interest, which is known as aliasing. Therefore, the designer must use an analog antialiasing filter to remove the noise and harmonic content from the input signal before the ADC performs sampling. An antialiasing filter is designed as a low-pass RC filter, where the 3-dB bandwidth is optimized based on specific application requirements.

For DC signals with fast transients (including multiplexed input signals), a high-bandwidth filter is designed to allow accurate settling of the signal at the inputs of the ADC during the small acquisition time window.

For AC signals, keeping the filter bandwidth low is desirable to band-limit the noise fed into the input of the ADC, thereby increasing the system SNR. Aside from filtering the noise from the front-end drive circuitry, the filter also helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor, C_{FLT}, is connected from each input pin of the ADC to the ground (as 式 1 and 図 4 show).

This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. Generally, the value of this capacitor must be at least 15- to 20 times the specified sampling capacitor capacitance of the ADC. For example, TI's ADS8900B 20-bit SAR converter specification recommends to keep the C_{FLT} greater than 900 pF. However, the total harmonic distortion (THD) performance of the ADC driver amplifier typically degrades with high capacitive loads. Higher values of C_{FLT} also degrade the driver phase margin. Therefore, TI recommends to select the minimum required value of C_{FLT} and still maintain a good ratio between C_{FLT} and the ADC input sampling capacitance. This design uses a 1000-pF capacitor. The capacitor must be a COG– or NPO– type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time.

$$f_{-3dB} = \frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \quad (1)$$

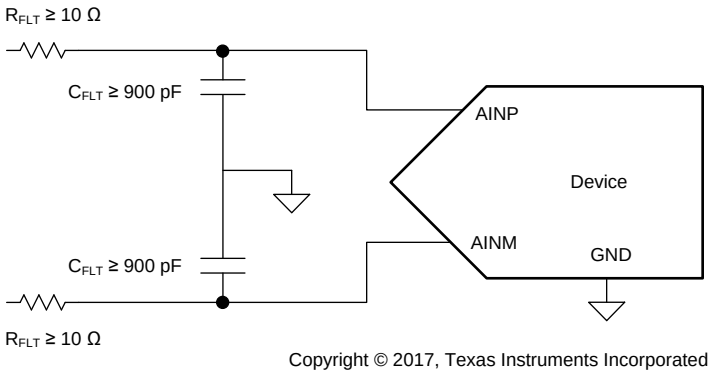


図 4. Charge Kickback Filter

Note that driving capacitive loads can degrade the phase margin of their driving amplifiers, thus making the amplifier marginally unstable. To avoid amplifier stability issues, use series isolation resistors (R_{FLT} or R_{ISO}) at the amplifier outputs. The resistor value is extremely important for many system parameters; see further discussion regarding these RC tradeoffs in *18-Bit , 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise*. A higher R_{FLT} value is helpful from the amplifier stability perspective, but adds distortion as a result of interactions with the nonlinear ADC input impedance. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of R_{FLT} requires balancing the stability and distortion. For the ADS8900B, limiting the value of R_{FLT} to a maximum of 10 Ω is recommended to avoid any significant degradation in linearity performance. The tolerance of the selected resistors must be kept less than 1% to keep the inputs balanced. The driver amplifier must be selected such that its closed-loop output impedance is at least five times less than the R_{FLT}.

2.3.2.1 THS4561 ADC Driver

Determine the values of R_{FLT} by comparing the THS4561 output impedance versus the ADC load impedance. 図 5 and 図 6 show the schematics used to simulate the ADC load impedance and the output impedance of THS4561, respectively. The simulation was done using TINA-TI.

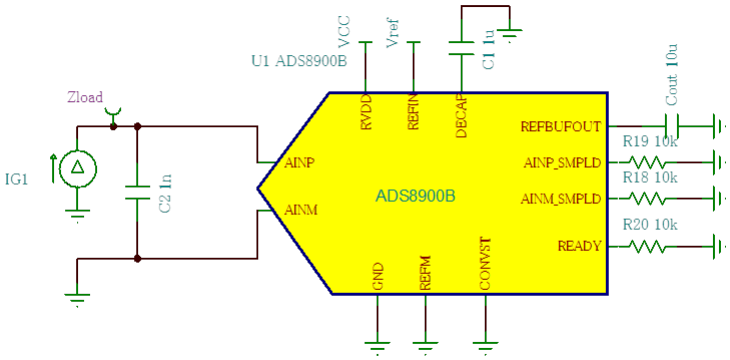


図 5. ADS8900B Load Impedance Simulation

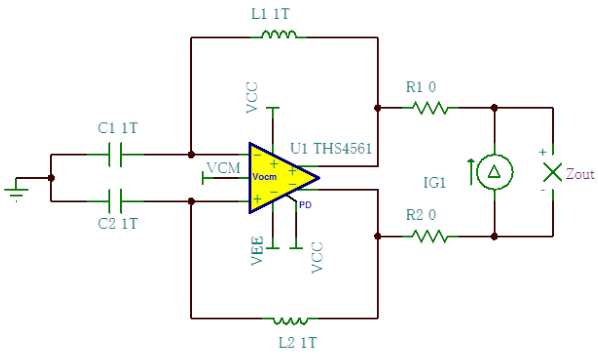


図 6. THS4561 Output Impedance Simulation

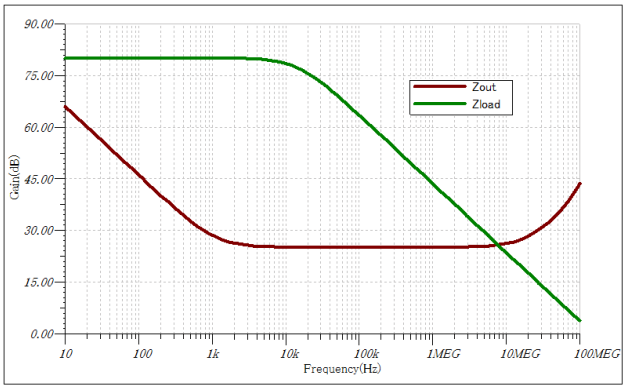


図 7. Z_{OUT} versus Zload THS4561

As the simulation results in 図 7 show, the load impedance curve is falling while the output impedance curve is rising at the point of the intersection. This intersection at a rate of greater than 20 dB per decade can cause instability (oscillation) at the THS4561 output. To flatten the output impedance response to ensure stability, add a series output isolation resistance of 20 Ω.

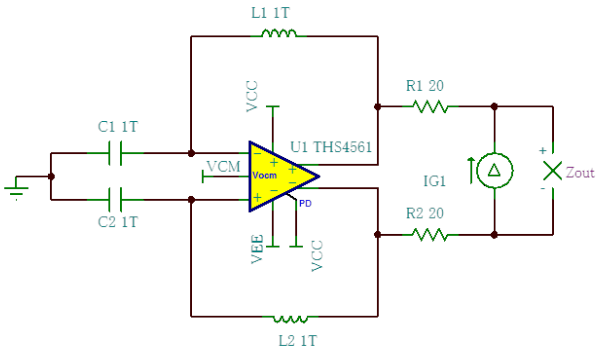


図 8. THS4561 with R_{ISO}

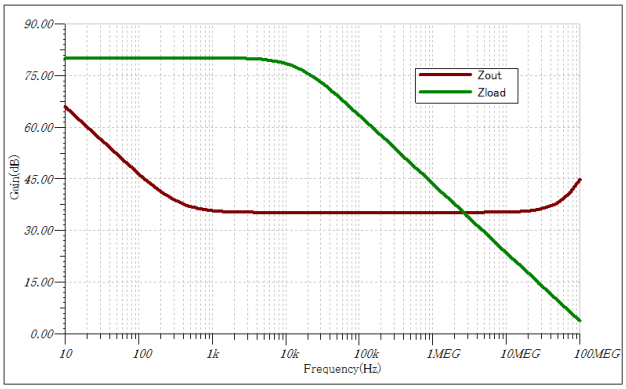


図 9. THS4561 With R_{ISO} Compensation

図 9 shows the results of simulating the THS4561 output impedance after the isolation resistance was added. The load impedance curve crosses the output impedance curve at a frequency where the impedance is constant, which improves robustness.

図 10 is used to verify the stability of the THS4561 device. When evaluating the stability of the amplifier, be sure to confirm the closed-loop gain, loaded open-loop gain, and loop gain. The phase margin of the circuit is also crucial for circuit stability operation and required settling.

図 10 features 1TF capacitors and 1TH inductors for stability simulation. When measuring loaded open-loop gain and loop gain, the feedback loop must be broken. These components are used to properly break the feedback loop. Measuring the stability without these component is difficult because the offset causes saturation. DC-wise, the inductor is a short while the capacitor is an open. AC-wise, the inductor is an open and the capacitor is a short. This configuration breaks the feedback loop and allows the designer to measure the loaded open-loop gain and loop gain.

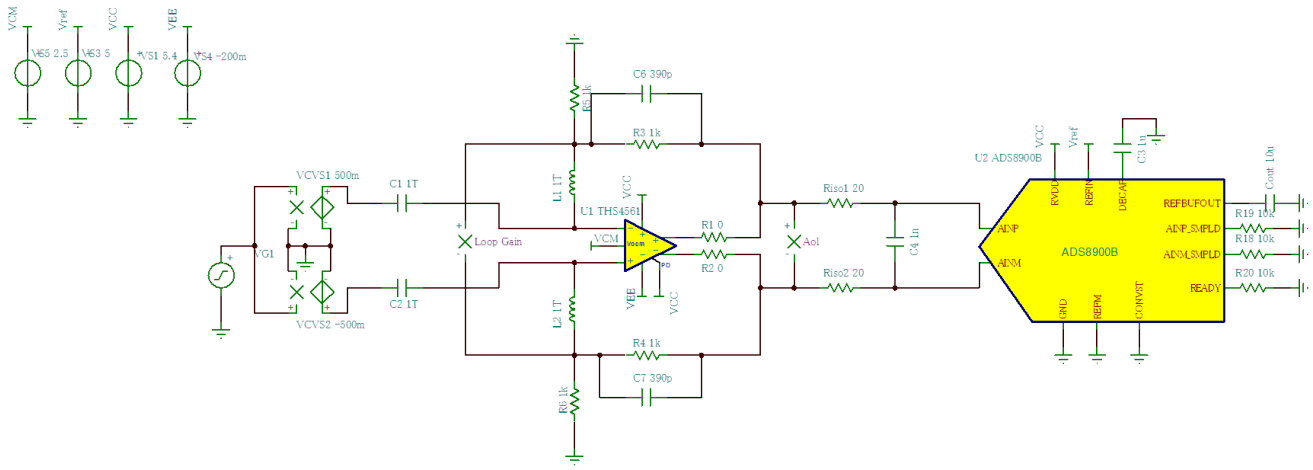


図 10. THS4561 Stability Schematic

図 11 shows a simulation result of the THS4561 stability, which indicates 43.79° of phase margin at a 38.9-MHz unity gain frequency.

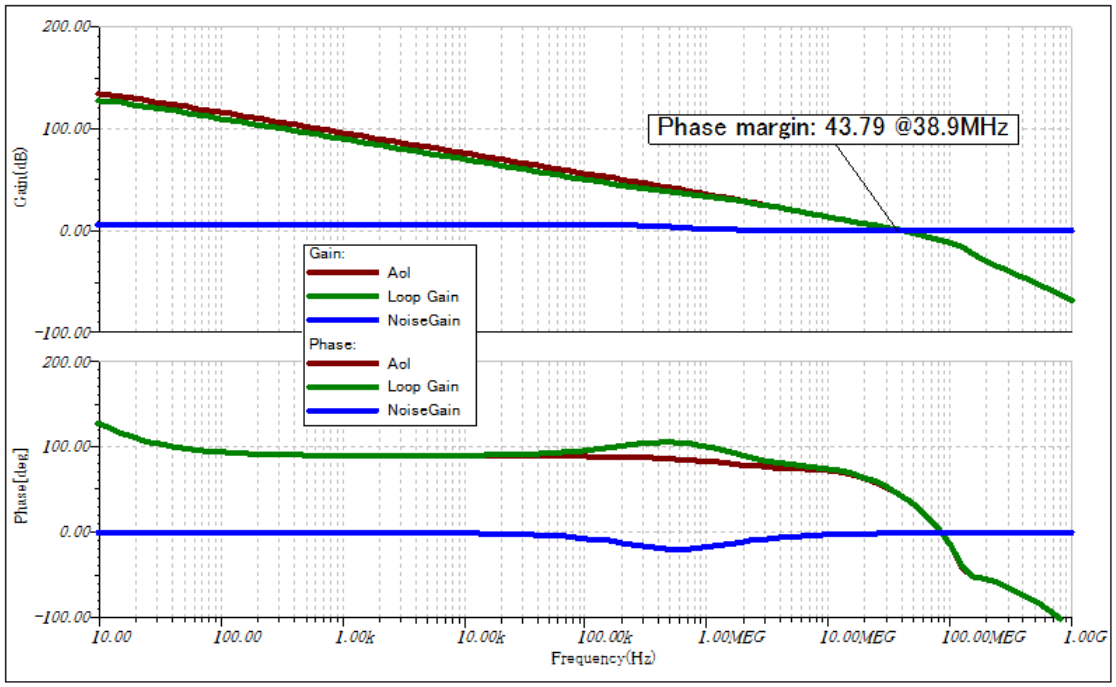
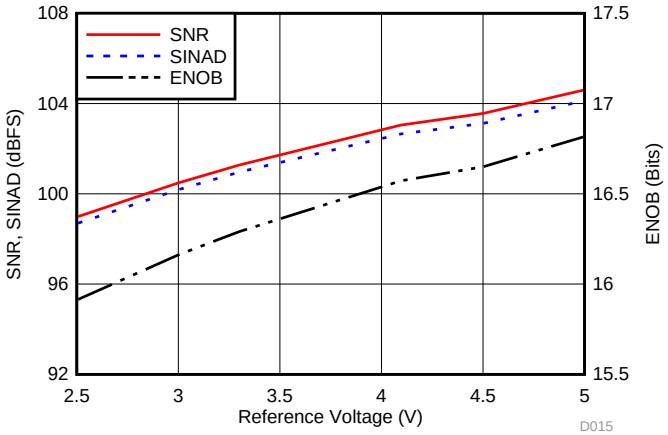


図 11. THS4561 Stability Results

2.3.2.2 Noise Analysis

This reference design focuses on an ADC driver, which ensures a 10-V_{PP} differential input to the ADC. To achieve a 10-V_{PP} differential input, use the THS4561 and REF6050. A comparison of the system (driver amplifier + ADC) noise performance with the traditional ADC driver (THS4551 and REF6041) is provided to validate the performance of this new ADC driver.

The Analog Engineer's Calculator allows the designer to calculate the system noise performance with ease. Calculating the system noise performance requires the designer to know the RMS noise of the amplifier, RMS noise of the reference voltage, and the SNR of the ADC. *REF60xx High-Precision Voltage Reference With Integrated ADC Drive Buffer* describes the RMS noise of the reference voltage and *ADS890xB 20-Bit, High-Speed SAR ADCs With Integrated Reference Buffer, and Enhanced Performance Features* describes the ADC SNR, and each values are 5 µV and 104.5 dBFS, respectively.



f_{IN} = 2 kHz

図 12. ADS8900B Noise Performance versus Reference Voltage

図 13 and 図 14 show the schematics for measuring noise performance of the THS4551 and the THS4561. In 図 13, R7 and C5 are placed for stable operation. The simulation model of ADS8900B was also placed in both schematics for further accurate results. TINA-TI was also utilized to obtain the total noise for both amplifiers. 図 15 shows the test results.

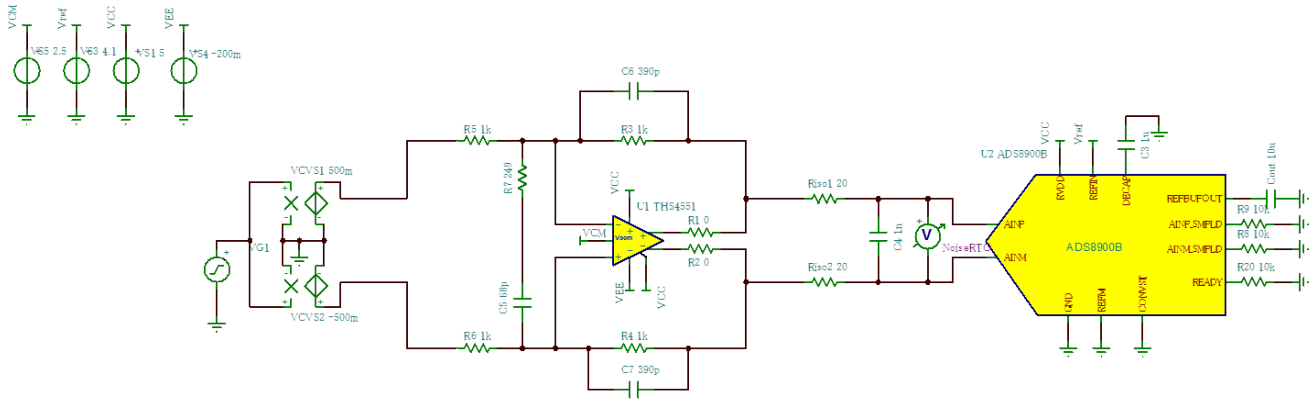


図 13. THS4551 Schematic for Noise Simulation

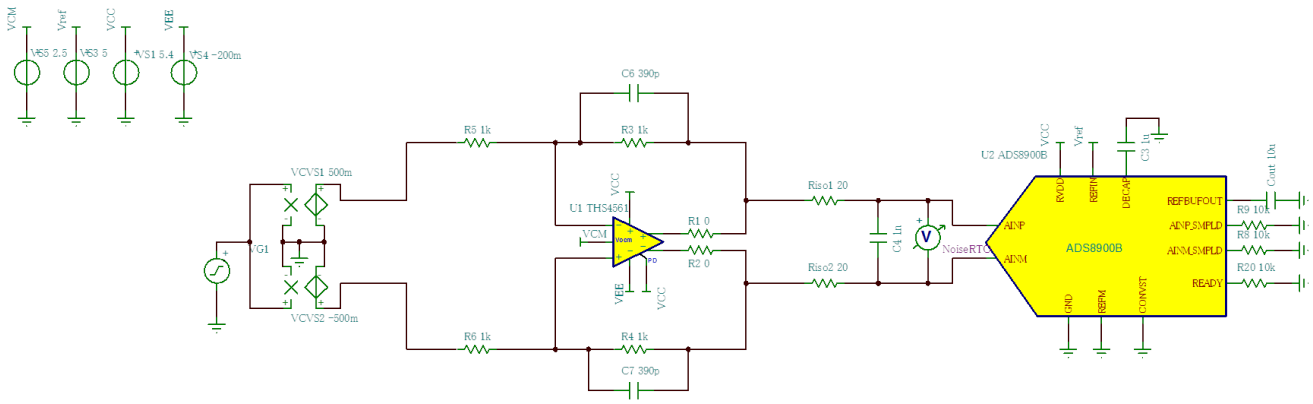


図 14. THS4561 Schematic for Noise Simulation

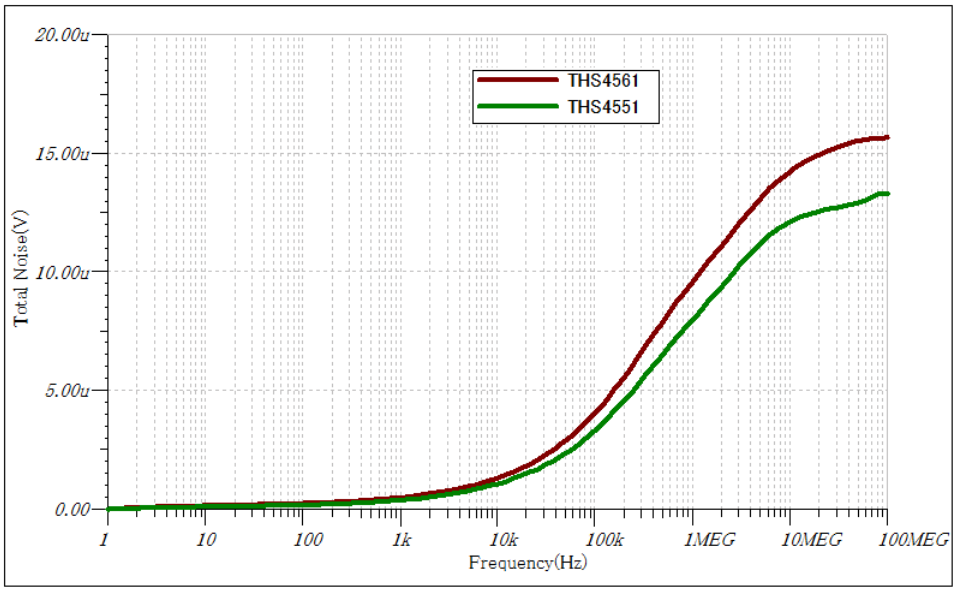


図 15. Total Noise Comparison

From 図 15, the total noise of THS4551 and THS4561 was 13.29 µV and 15.63 µV, respectively. Therefore, the THS4561 is inferior to the THS4551 when considering just the noise of the amplifier. A trade-off between the quiescent current and noise is the cause of this parameter. The THS4561 has a lower quiescent current (0.82 mA) than the THS4551 (1.35 mA).

Now, calculate the system noise performance by using the Analog Engineer's Calculator. 図 16 and 図 17 show the results for THS4551 + REF6041 and THS4561 + REF6050, respectively. Note that, because the ADS8900B has a true differential input, the FSR changes to double that of the reference voltage. Thus, the FSR from REF6041 (4.096-V output) is 8.192 V. Similarly, the FSR from REF6050 (5-V output) is 10 V. For further detail, see the section regarding ADC Transfer Function in *ADS890xB 20-Bit, High-Speed SAR ADCs With Integrated Reference Buffer, and Enhanced Performance Features*. From 図 12, the ADC SNR with reference voltages of 4.096 V and 5 V can be recognized as 103.5 dB and 104.5 dB roughly. As a result, the system noise performance of the THS4561 outperforms the THS4551 by 0.8 dB, even though the noise performance of the THS4561 itself is inferior to the THS4551.

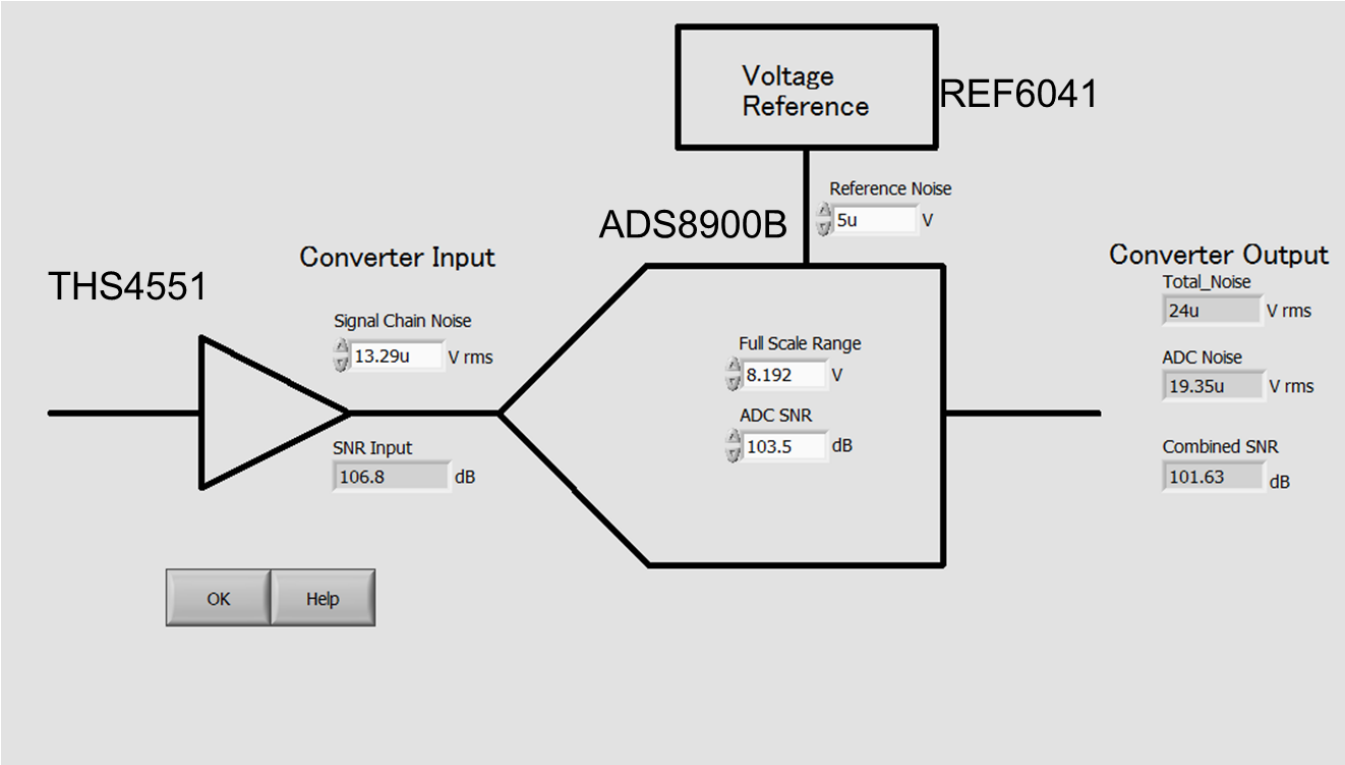


図 16. System Noise Calculation for THS4551 + REF6041

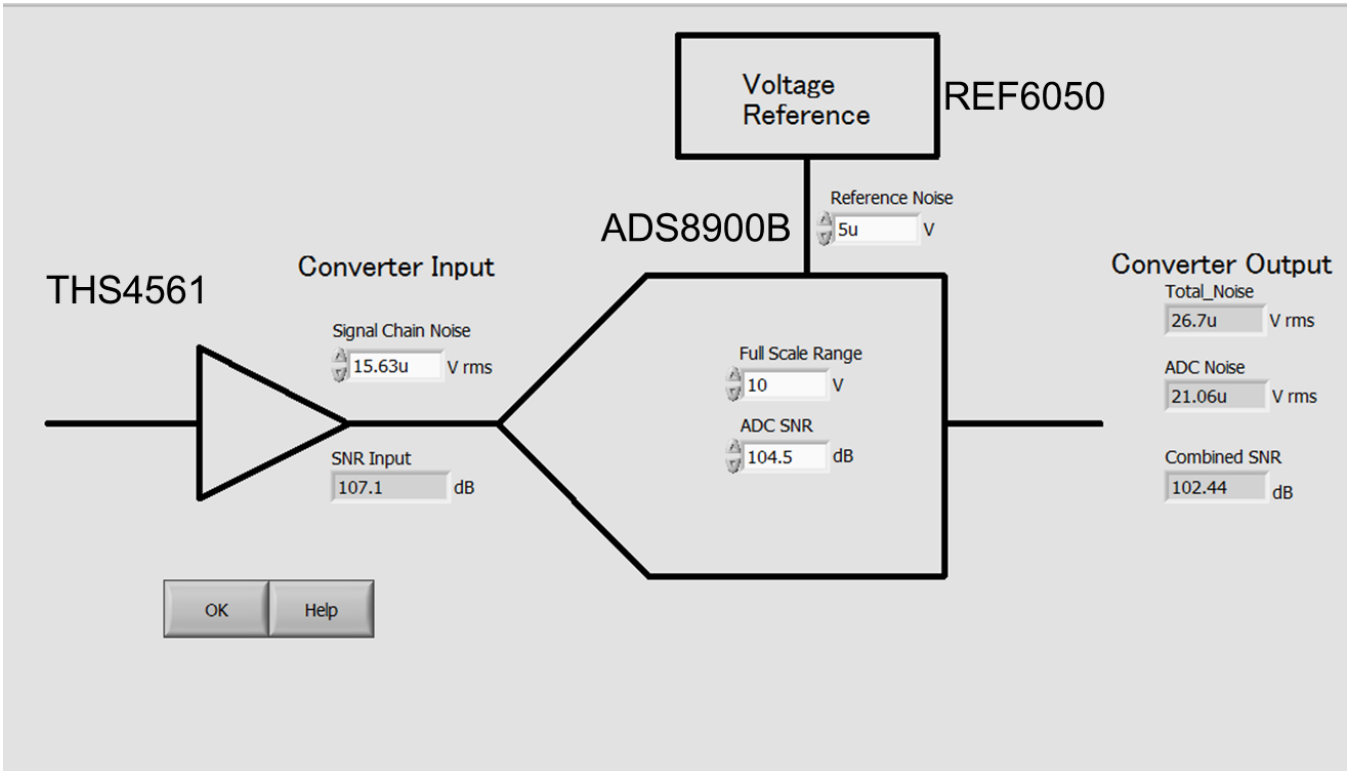


図 17. System Noise Calculation for THS4561 + REF6050

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

The following subsection outlines the information for getting the board up and running as fast as possible. To learn about the PHI board or the onboard clocking and jitter cleaner, see *Optimized Analog Front-End DAQ System Reference Design for 18-Bit SAR Data Converters*. Take care when moving the jumper pins to avoid possible damage to the components.

3.1.1 Jumper Configuration

This system has several configurable power options. These options are selectable by using two-pin and three-pin jumpers. 表 2 highlights the purpose of each jumper and assists in changing the configuration to fit the needs of the user.

表 2. Jumper Configuration

JUMPER NAME	SHORT PINS 1 AND 2	SHORT PINS 2 AND 3	DEFAULT CONFIGURATION
JSI_18V	Power to LMS3635-Q1 18-V rail	—	Short
JTI_18V	Connects LMS3635-Q1 to TPS7A700 for 18-V rail	Connects LMZ14201 to TPS7A700 for 18-V rail	Short pins 1 and 2
JSI_5V	Power to LMS3635-Q1 5-V rail	—	Short
JTI_5V	Connects LMS3635-Q1 to TPS7A700 for 5-V rail	Connects LMZ14203 to TPS7A700 for 5-V rail	Short pins 1 and 2
JSI_3.3V	Power to LMS3635-Q1 3.3-V rail	—	Short
JTI_3.3V	Connects LMS3635-Q1 to TPS7A700 for 3.3-V rail	Connects LMZ14202 to TPS7A700 for 3.3-V rail	Short pins 1 and 2
JPRI_–18V	Power to LM46001 –18-V rail	—	Short
JTI_–18V	Connects LM46001 to TPS7A3001 for –18-V rail	Connects LM5574 to TPS7A3001 for –18-V rail	Short pins 1 and 2
JMTI_–18V	Power to LM5574 –18-V rail	—	Open
JZI_18V	Power to LMZ14201 18-V rail	—	Open
JZI_3.3V	Power to LMZ14202 3.3-V rail	—	Open
JZI_5V	Power to LMZ14203 5-V rail	—	Open
J39	Connects –0.2-V rail to OPA625 and THS4561	Shorts –0.2-V rail to ground	Short pins 1 and 2

3.2 Testing and Results

An Audio Precision 2700 series signal generator is used as the signal source to test the AFE and ADC performance. The noise and THD of the AP2700 have adequate performance and do not limit measurements or system performance. Use of a quality source is crucial to avoid limiting the system's performance by the signal source. A generic DC power supply was used to generate the 18.5-V DC, –18.5-V DC, 5.8-V DC, 3.8-V DC, and –0.25-V DC. The AP2700 is set to output a 2-kHz sinusoid. A value of 2 kHz is chosen because it is the standard frequency in measuring noise and THD. The amplitude for THS4551 was chosen as 8 V_{PK-PK} to grant the full range on it. A 9.16-V_{PK-PK} amplitude was chosen for THS4561 due to the constraint of the signal generator.

A PHI controller board is used to connect the TIDA-01057 board to the host PC, where the ADS8900B EVM GUI is running. This software measures the SNR, THD, SFDR, signal-to-noise distortion ratio (SINAD), and effective number of bits (ENOB) for the ADC by running a spectral analysis.

図 18 and 図 19 show the test results for THS4551 + REF6041 and THS4561 + REF6050, respectively. 表 3 summarizes each specification. As the previous calculation in 図 16 and 図 17 show, the SNR improved by roughly 0.8 dB over the THS4551. Furthermore, the THS4561 exceeded the THS4551 in all of the other specifications, as 表 3 shows. Note that some noise components, such as phase noise, switching noise, and the first stage buffer noise were not taken into account in the previous calculation, which is why the actual measurements are slightly lower than the calculation. In conclusion, the THS4561 allows designers to improve the noise performance and power consumption of the full system due to its wider dynamic range, even though its noise performance is inferior to the THS4551.

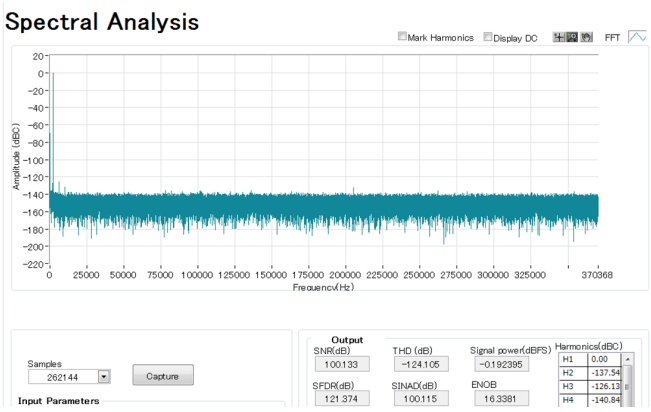


図 18. THS4551 Results

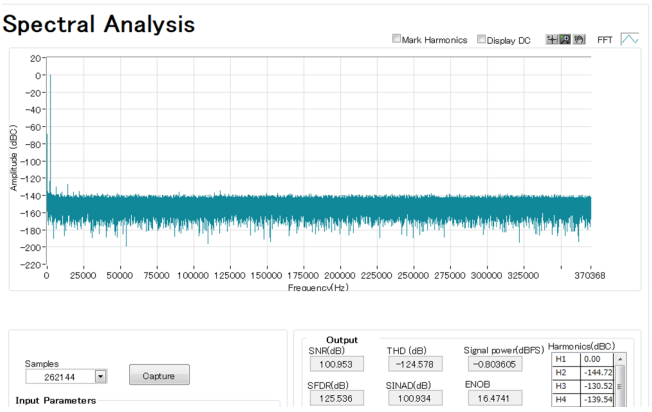


図 19. THS461 Results

表 3. Comparison of Test Results

SPECIFICATION	THS4551	THS4561
SNR	100.13 dB	100.95 dB
THD	–124.11 dB	–124.57 dB
ENOB	16.3	16.4
SFDR	121.3 dB	125.5 dB

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01057.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01057.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01057.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01057.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01057.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01057.

5 Software Files

To download the software files, see the design files at TIDA-01057.

6 Related Documentation

1. Texas Instruments, *Multi-Rail Power Reference Design for Eliminating EMI Effects in High-Performance DAQ Systems*
2. Texas Instruments, *REF60xx High-Precision Voltage Reference With Integrated ADC Drive Buffer*
3. Texas Instruments, *ADS890xB 20-Bit, High-Speed SAR ADCs With Integrated Reference Buffer, and Enhanced Performance Features*
4. Texas Instruments, *Optimized Analog Front-End DAQ System Reference Design for 18-Bit SAR Data Converters*

6.1 商標

7 About the Authors

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