参考資料

Design Guide: TIDA-01606

10kW、双方向、3 相、3 レベル (T タイプ) インバータと PFC のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインでは、双方向 3 レベル、3 相、SiC ベースのアクティブ・フロント・エンド (AFE) インバータおよび PFC 段を実装する方法の概要を紹介します。このデザインでは、50kHz のスイッチング周波数と LCL 出力フィルタを使用して、磁気素子のサイズを縮小しています。99% のピーク効率を達成しています。このデザインは、DQ ドメインに完全な 3 相 AFE 制御を実装する方法を示しています。制御とソフトウェアは、実際のハードウェアと、ループ内ハードウェア (HIL) のセットアップ上で検証されます。

リソース

TIDA-01606	デザイン・フォルダ
TMS320F28379D	プロダクト・フォルダ
C2000WARE-DIGITALPOWER-SDK	ツール・フォルダ
UCC21710、UCC5320	プロダクト・フォルダ
TMDSCNCD28379D	ツール・フォルダ
AMC1306M05、OPA4340	プロダクト・フォルダ
LM76003、PTH08080W	プロダクト・フォルダ
TLV1117LV、OPA350	プロダクト・フォルダ
UCC14240	プロダクト・フォルダ

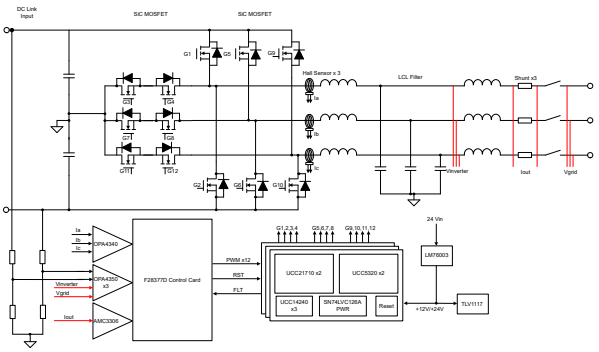
TI の TI E2E™ サポート・エキスパートにお問い合わせください。

特長

- 定格公称入力電圧 DC 800V、最大入力電圧 DC 1000V、最大電力 10kW/10kVA (400V AC L-L 50Hz または 60Hz 時)
- スイッチング周波数 50kHz のコンパクトな出力 LCL フィルタ
- 全負荷時の 2% 未満の出力電流全高調波歪み (THD)
- 強化絶縁付きの絶縁ドライバ UCC21710 により高電圧の SiC MOSFET を駆動し、UCC5320S により中電圧の SiC MOSFET を駆動
- 負荷電流制御および監視を目的とする AMC1301 を使用した絶縁型電流検出
- 三角関数演算ユニット (TMU) を使用してフェーズ・ロック・ループ (PLL) の計算を高速化するデジタル制御用 TMS320F28379D 制御カード、保護機能を実装するためのコンパレータ・サブシステム、制御ループをコプロセッサにオフロードする制御補償器アクセラレータ (CLA)

アプリケーション

- ストリング・インバータ
- セントラル・インバータ
- オンボード・チャージャ (OBC) およびワイヤレス・チャージャ
- DC 充電 (バッテリ) ステーション
- ポータブル DC チャージャ
- エネルギー・ストレージ電力変換システム (PCS)



1 System Description

Modern commercial scale solar inverters are seeing innovation on two fronts, which lead to smaller, higher efficiency products on the market:

- The move to higher voltage solar arrays
- Reducing the size of the onboard magnetics

By increasing the voltage to 1000-V or 1500-V DC from the array, the current can be reduced to maintain the same power levels. This reduction in current results in less copper and smaller power conducting devices required in the design. The reduction in di/dt also reduces the stress on electrical components. However, sustained DC voltages of > 1 kV can be difficult to design to, or even find components that can survive it.

To compensate for the voltage stresses generated by high-voltage solar arrays, new topologies of solar inverters have been designed. Traditional half bridges block the full input voltage on each switching device. By adding additional switched blocking and conduction components, the overall stress on the device can be significantly reduced. This reference design shows how to implement a three-level converter. Higher level converters are also possible, further increasing the voltage handling capability.

Additional power density in solar electronics is also being enabled by moving to higher switching speeds in the power converters. As this design shows, even a modestly higher switching speed reduces the overall size requirement of the output filter stage—a primary contributor to the design size.

Traditional switching devices have a limit in how quickly they can switch high voltages, or more appropriately, the dV/dt ability of the device. This slow ramp up and down increases conduction loss because the device spends more time in a switching state. This increased switch time also increases the amount of dead time required in the control system to prevent shoot-through and shorts. The solution to this has been developed in newer switching semiconductor technology like SiC and GaN devices with high electron mobility. This reference design uses SiC MOSFETs alongside TI's SiC gate driver technology to demonstrate the potential increase in power density.

Similarly for Onboard Chargers (OBC) higher power chargers (11 kW and 22 kW) are increasingly required. For which three phase PFC is necessary, this design shows implementation of three phase PFC using DQ control and presents the complete control loop model.

1.1 Key System Specifications

表 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Output power	10 kW	セクション 2.3
Output voltage	Three-phase 400-V AC	セクション 2.3
Output frequency	50 or 60 Hz	セクション 2.3
Output current	18 A (max)	セクション 2.3
Nominal input voltage	800-V DC	セクション 2.3
Input voltage range	600-V to 1000-V DC	セクション 2.3
Inverter switching frequency	50 kHz	セクション 2.3
Efficiency	99%	セクション 2.3.1.5
Power density	1 kW/L+	

2 System Overview

2.1 Block Diagram

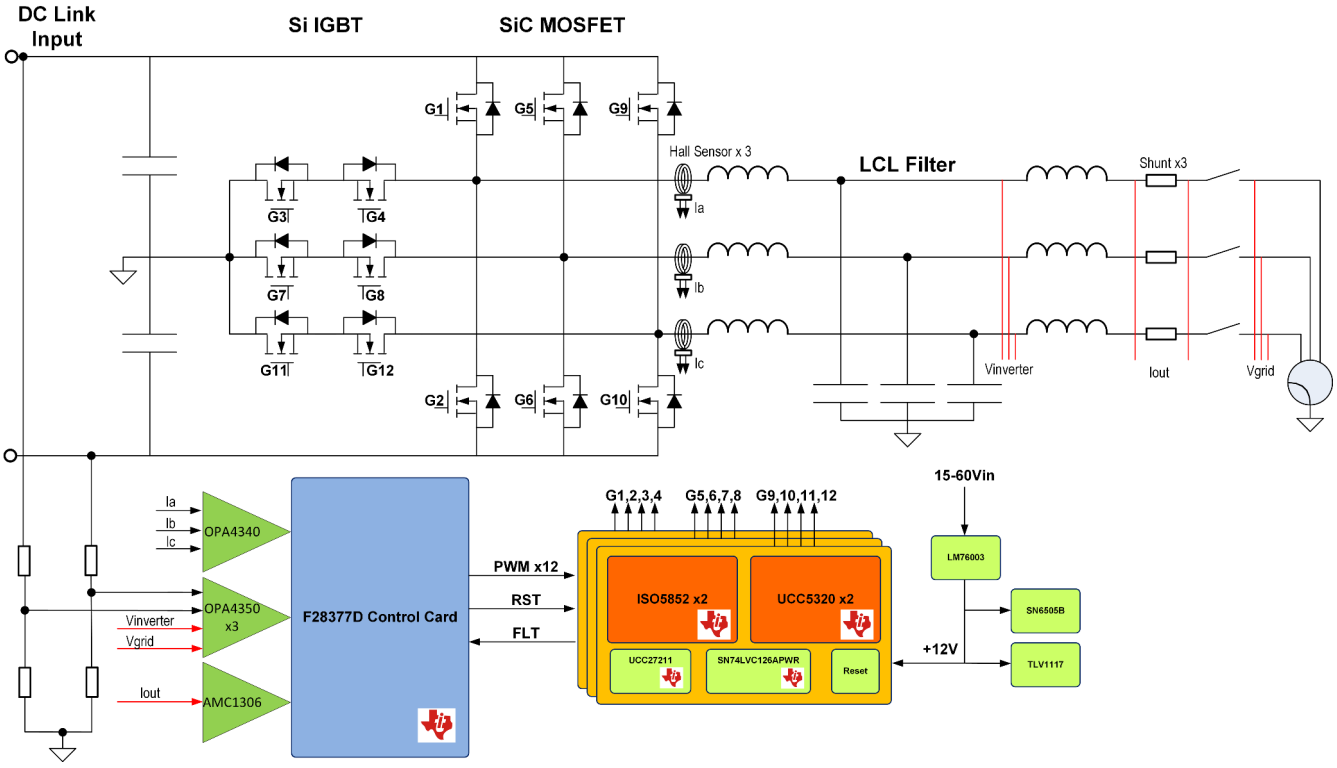


図 2-1. TIDA-01606 Block Diagram

This reference design is comprised of four separate boards that intercommunicate. The following boards work in tandem to form this three-phase inverter reference design:

- A power board, comprising all of the switching device, LCL filter, sensing electronics, and power structure
- A TMS320F28379D control card to support the DSP
- Three gate driver cards, each with two UCC21710 and two UCC5320 gate drivers
- A DC bus voltage measuring board (TIDA-01606 ISOHVCARD)

2.2 Highlighted Products

2.2.1 UCC21710

The UCC21710 device is a 5.7-kV_{RMS}, reinforced isolated gate driver for Insulated-Gate Bipolar Transistors (IGBT) and SiC MOSFETs with split outputs, providing 10-A source and 10-A sink current. The input side operates from a single 3-V to 5.5-V supply. The output side allows for a supply range from minimum 13 V to maximum 33 V. Two complementary CMOS inputs control the output state of the gate driver. The short propagation time of 130 ns provides accurate control of the output stage. UCC21710 integrates short circuit protection, detected via Overcurrent detection, with a fast response time needed to protect SiC MOSFETs.

- 150-kV/μs minimum common-mode transient immunity (CMTI)
- Split outputs to provide 10-A peak source and 10-A peak sink currents
- Short propagation delay: 90 ns (typ), 130 ns (max)
- 4-A active Miller clamp
- Output short-circuit clamp
- Soft turn off (STO) during short circuit
- Fault alarm upon desaturation detection is signaled on FLT and reset through RST
- Input and output undervoltage lockout (UVLO) with Ready (RDY) pin indication
- Active output pulldown and default low outputs with low supply or floating inputs
- 2.25-V to 5.5-V input supply voltage

- 15-V to 30-V output driver supply voltage
- CMOS compatible inputs
- Rejects input pulses and noise transients shorter than 40 ns
- Operating temperature: –40°C to +150°C ambient
- Isolation surge withstand voltage of 12800-V_{PK}

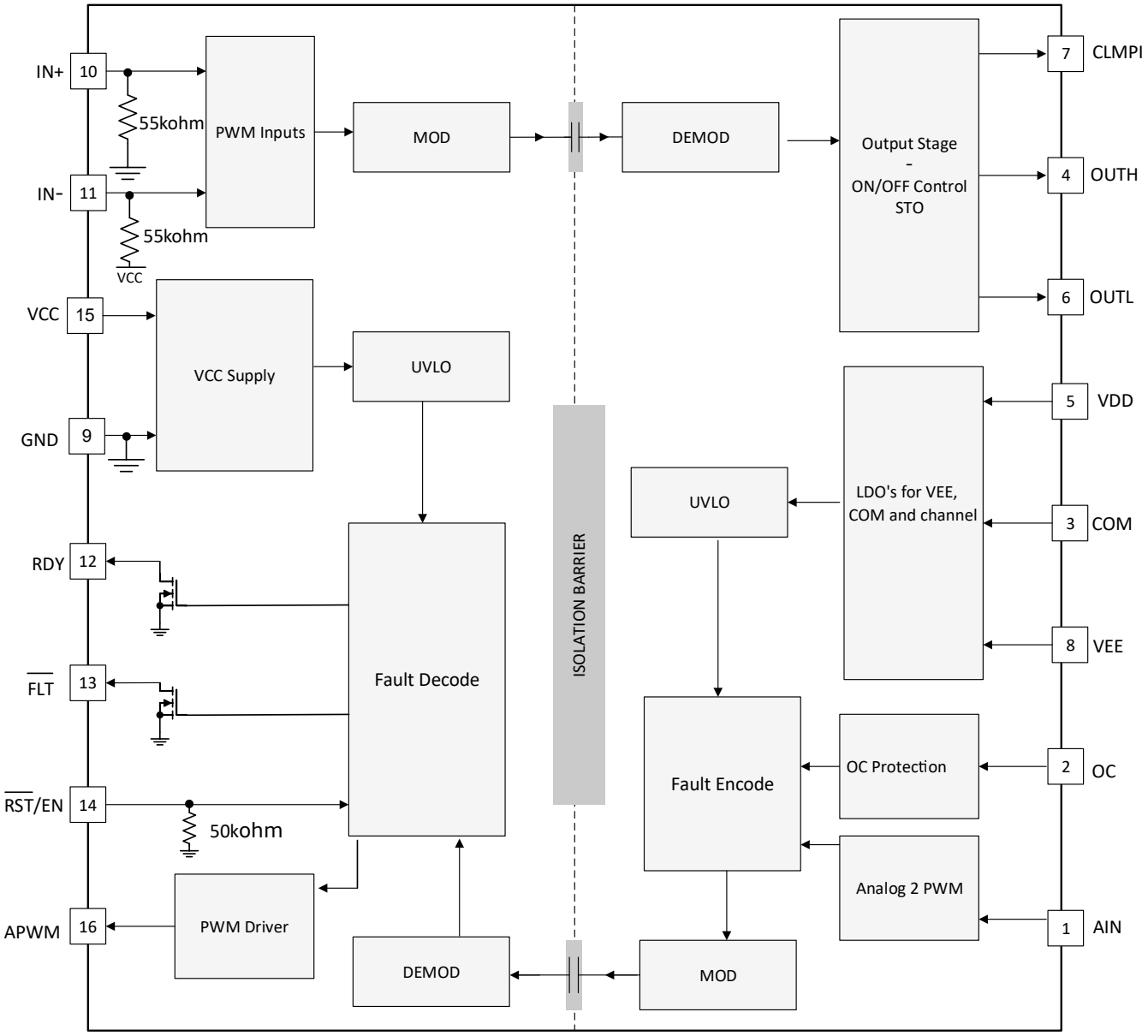


図 2-2. UCC21710 Functional Block Diagram

2.2.2 UCC5320

The UCC53x0 is a family of compact, single-channel, isolated IGBT, SiC, and MOSFET gate drivers with best-in-class isolation ratings and variants for pinout configuration, and drive strength.

The UCC53x0 is available in an 8-pin SOIC (DWV) package. This package has a creepage and clearance of 8.5 mm and can support isolation voltage up to 5 kV_{RMS}, which is good for applications where reinforced isolation is needed. With these various options and wide power range, the UCC53x0 family is a good fit for motor drives and industrial power supplies.

- 3-V to 15-V input supply voltage
- 13.2-V to 33-V output driver supply voltage

- Feature options:
  - Split outputs (UCC5320S and UCC5390S)
  - UVLO with respect to MOSFET collector (UCC5320E and UCC5390E)
  - Miller clamp option (UCC5310M and UCC5350M)
- Negative 5-V handling capability on input pins
- 60-ns (typical) propagation delay for UCC5320S, UCC5320E, and UCC5310M
- 100-kV/µs minimum CMTI
- Isolation surge withstand voltage: 4242 V_{PK}
- Safety-related certifications:
  - 4242-V_{PK} isolation per DIN V VDE V 0884-10 and DIN EN 61010-1 (planned)
  - 3000-V_{RMS} isolation for 1 minute per UL 1577 (planned)
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 End Equipment Standards (Planned)
  - CQC Certification per GB4943.1-2011 (Planned)
- 4-kV ESD on all pins
- CMOS inputs
- 8-pin narrow body SOIC package
- Operating temperature: –40°C to +125°C ambient

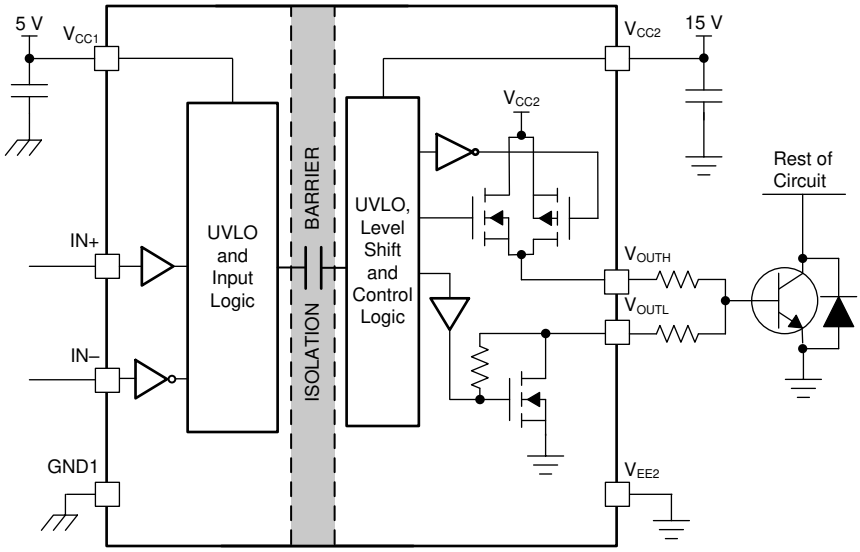


図 2-3. UCC5320 Functional Block Diagram (S Version)

2.2.3 TMS320F28379D

The Delfino™ TMS320F2837xD is a powerful 32-bit floating-point microcontroller unit (MCU) designed for advanced closed-loop control applications such as industrial drives and servo motor control; solar inverters and converters; digital power; transportation; and power line communications. Complete development packages for digital power and industrial drives are available as part of the powerSUITE and DesignDRIVE initiatives. While the Delfino product line is not new to the TMS320C2000™ portfolio, the F2837xD supports a new dual-core C28x architecture that significantly boosts system performance. The integrated analog and control peripherals also let designers consolidate control architectures and eliminate multiprocessor use in high-end systems.

- Dual-core architecture:
  - Two TMS320C28x 32-bit CPUs
  - 200 MHz
  - IEEE 754 single-precision floating-point unit (FPU)
  - Trigonometric math unit (TMU)
  - Viterbi/complex math unit (VCU-II)
- Two programmable control law accelerators (CLAs)
  - 200 MHz
  - IEEE 754 single-precision floating-point instructions

  - Executes code independently of main CPU
- On-chip memory
  - 512KB (256 kW) or 1MB (512 kW) of Flash (ECC-protected)
  - 172KB (86 kW) or 204KB (102 kW) of RAM (ECC-protected or parity-protected)
  - Dual-zone security supporting third-party development
- Clock and system control:
  - Two internal zero-pin 10-MHz oscillators
  - On-chip crystal oscillator
  - Windowed watchdog timer module
  - Missing clock detection circuitry
- 1.2-V core, 3.3-V I/O design
- System peripherals:
  - Two external memory interfaces (EMIFs) with ASRAM and SDRAM support
  - Dual six-channel direct memory access (DMA) controllers
  - Up to 169 individually programmable, multiplexed general-purpose input/output (GPIO) pins with input filtering
  - Expanded peripheral interrupt controller (ePIE)
  - Multiple low-power mode (LPM) support with external wakeup
- Communications peripherals:
  - USB 2.0 (MAC + PHY)
  - Support for 12-pin 3.3-V compatible universal parallel port (uPP) interface
  - Two controller area network (CAN) modules (pin-bootable)
  - Three high-speed (up to 50-MHz) SPI ports (pin-bootable)
  - Two multichannel buffered serial ports (McBSPs)
  - Four serial communications interfaces (SCI/UART) (pin-bootable)
  - Two I^2C interfaces (pin-bootable)
- Analog subsystem:
  - Up to four analog-to-digital converters (ADCs):
    - 16-bit mode
      - 1.1 MSPS each (up to 4.4-MSPS system throughput)
      - Differential inputs
      - Up to 12 external channels
    - 12-bit mode
      - 3.5 MSPS each (up to 14-MSPS system throughput)
      - Single-ended inputs
      - Up to 24 external channels
    - Single sample-and-hold (S/H) on each ADC
    - Hardware-integrated post-processing of ADC conversions:
      - Saturating offset calibration
      - Error from setpoint calculation
      - High, low, and zero-crossing compare, with interrupt capability
      - Trigger-to-sample delay capture
  - Eight windowed comparators with 12-bit digital-to-analog converter (DAC) references
  - Three 12-bit buffered DAC outputs
- Enhanced control peripherals:
  - 24 pulse width modulator (PWM) channels with enhanced features
  - 16 high-resolution pulse width modulator (HRPWM) channels:
    - High resolution on both A and B channels of eight PWM modules
    - Dead-band support (on both standard and high resolution)
  - Six enhanced capture (eCAP) modules
  - Three enhanced quadrature encoder pulse (eQEP) modules
  - Eight sigma-delta filter module (SDFM) input channels, two parallel filters per channel:
    - Standard SDFM data filtering
    - Comparator filter for fast action for out of range

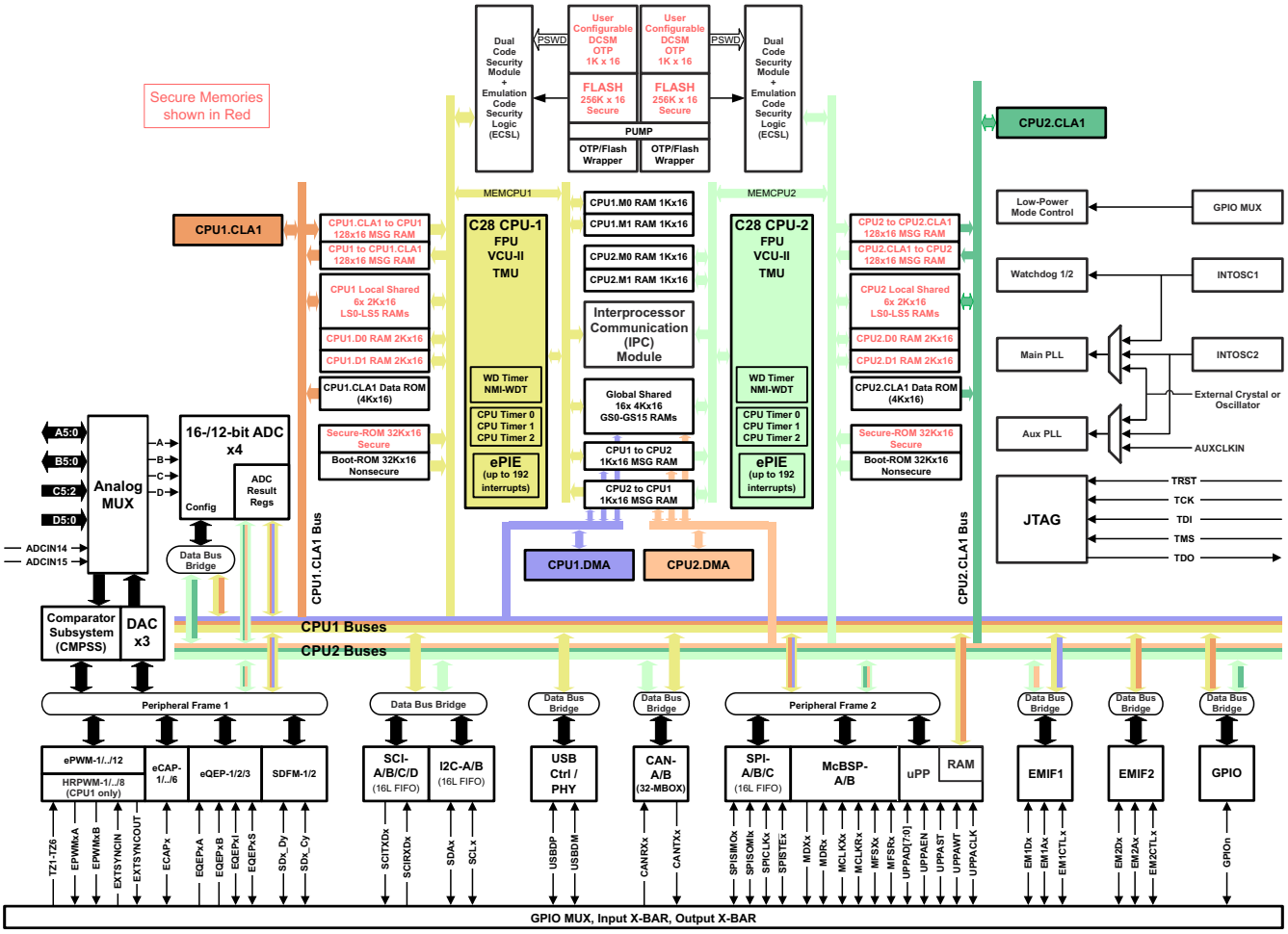


図 2-4. TMS320F28379D Functional Block Diagram

2.2.4 AMC1305M05

The AMC1305 device is a precision, delta-sigma (ΔΣ) modulator with the output separated from the input circuitry by a capacitive double isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation of up to 7000 V_{PEAK} according to the DIN V VDE V 0884-10, UL1577, and CSA standards. Used in conjunction with isolated power supplies, the device prevents noise currents on a high common-mode voltage line from entering the local system ground and interfering with or damaging low voltage circuitry.

- Pin-compatible family optimized for shunt-resistor-based current measurements:
  - ±50-mV or ±250-mV input voltage ranges
  - CMOS or LVDS digital interface options
- Excellent DC performance supporting high-precision sensing on system level:
  - Offset error: ±50 µV or ±150 µV (max)
  - Offset drift: 1.3 µV/°C (max)
  - Gain error: ±0.3% (max)
  - Gain drift: ±40 ppm/°C (max)
- Safety-related certifications:
  - 7000-V_{PK} reinforced isolation per DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
  - 5000-V_{RMS} isolation for 1 minute per UL1577
  - CAN/CSA No. 5A-Component Acceptance Service Notice, IEC 60950-1, and IEC 60065 End Equipment Standards
- Transient immunity: 15 kV/µs (min)
- High electromagnetic field immunity (see *ISO72x Digital Isolator Magnetic-Field Immunity*)
- External 5-MHz to 20-MHz clock input for easier system-level synchronization

- Fully specified over the extended industrial temperature range

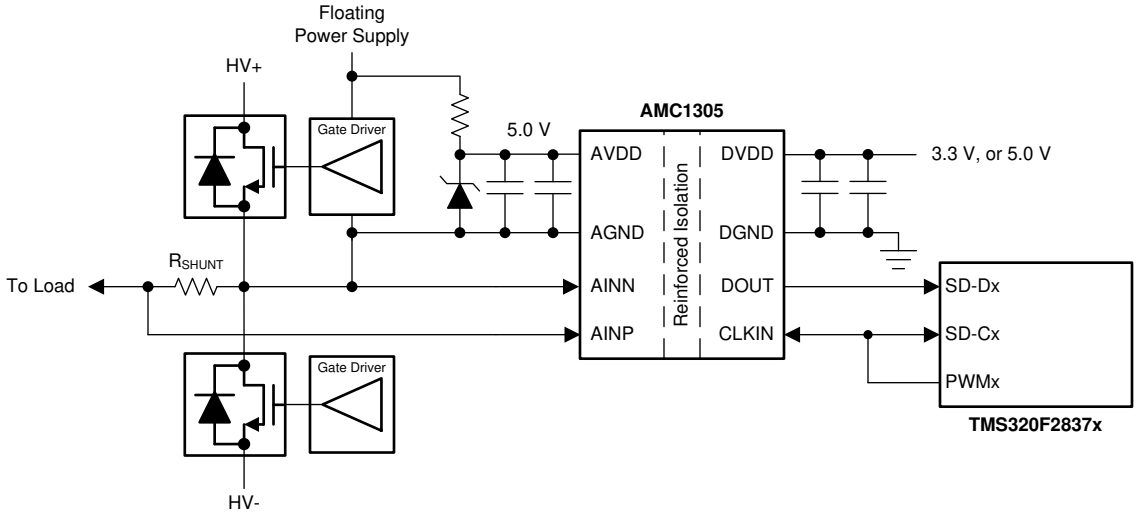


図 2-5. AMC1305M05 Simplified Schematic

2.2.5 OPA4340

The OPA4340 series rail-to-rail CMOS operational amplifiers are optimized for low-voltage, single-supply operation. Rail-to-rail input and output and high-speed operation make them ideal for driving sampling ADCs. These op amps are also well-suited for general purpose and audio applications as well as providing I/V conversion at the output of DACs. Single, dual, and quad versions have identical specifications for design flexibility.

- Rail-to-rail input
- Rail-to-rail output (within 1 mV)
- MicroSize packages
- Wide bandwidth: 5.5 MHz
- High slew rate: 6 V/µs
- Low THD + noise: 0.0007% (f = 1 kHz)
- Low quiescent current: 750 µA/channel
- Single, dual, and quad versions

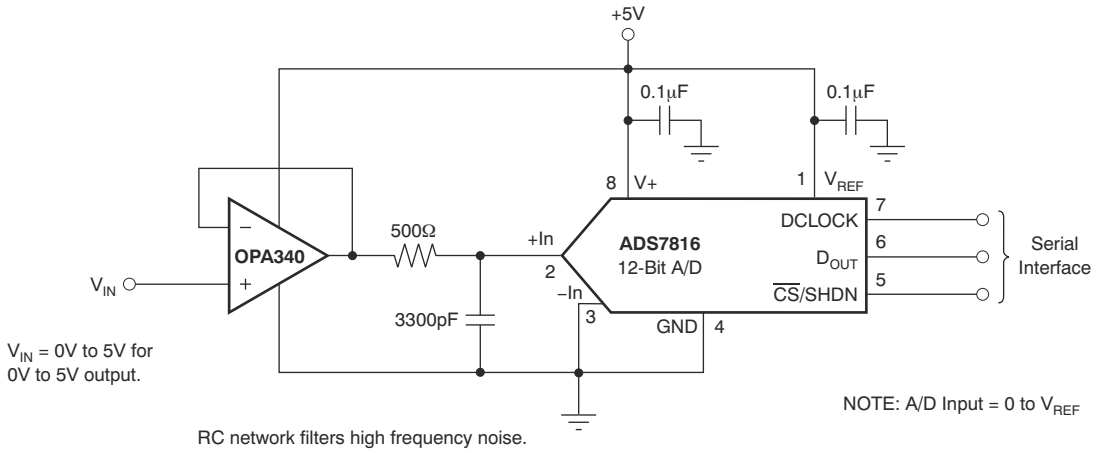


図 2-6. OPA4340 in Non-Inverting Configuration

2.2.6 LM76003

The LM76002/LM76003 regulator is an easy-to-use synchronous step-down DC/DC converter capable of driving up to 2.5 A (LM76002) or 3.5 A (LM76003) of load current from an input up to 60 V. The LM76002/LM76003 provides exceptional efficiency and output accuracy in a very small solution size. Peak current-mode control is employed. Additional features such as adjustable switching frequency, synchronization, FPWM option, power-good flag, precision enable, adjustable soft start, and tracking provide both flexible and easy-to-use solutions for a wide range of applications. Automatic frequency foldback at light load and optional external bias improve efficiency. This device requires few external components and has a pinout designed for simple PCB layout with best-in-class EMI (CISPR22) and thermal performance. Protection features include thermal shutdown, input UVLO, cycle-by-cycle current limit, and short-circuit protection. The LM76002/LM76003 device is available in the WQFN 30-pin leadless package with wettable flanks.

- Integrated synchronous rectification
- Input voltage: 3.5 V to 60 V (65 V maximum)
- Output current:
  - LM76002: 2.5 A
  - LM76003: 3.5 A
- Output voltage: 1 V to 95% V_{IN}
- 15-µA quiescent current in regulation
- Wide voltage conversion range:
  - t_{ON-MIN} = 65 ns (typical)
  - $t_{OFF-MIN}$ = 95 ns (typical)
- System-level features:
  - Synchronization to external clock

  - Power-good flag
  - Precision enable
  - Adjustable soft start (6.3 ms default)
  - Voltage tracking capability
- Pin-selectable FPWM operation
- High-efficiency at light-load architecture (PFM)
- Protection features:
  - Cycle-by-cycle current limit
  - Short-circuit protection with hiccup mode
  - Overtemperature thermal shutdown protection

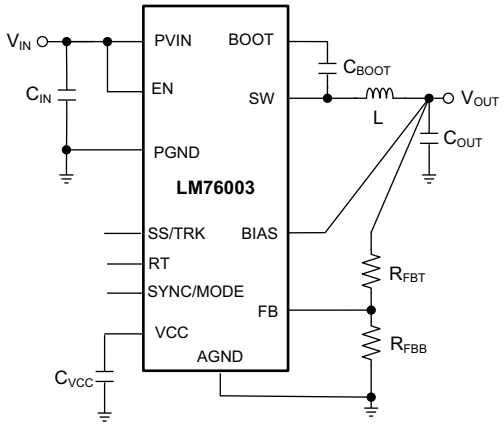


図 2-7. LM76003 Simplified Schematic

2.2.7 PTH08080W

The PTH08080W is a highly integrated, low-cost switching regulator module that delivers up to 2.25 A of output current. The PTH08080W sources output current at a much higher efficiency than a TO-220 linear regulator, thereby eliminating the need for a heat sink. Its small size (0.5 × 0.6 in) and flexible operation creates value for a variety of applications.

- Up to 2.25-A output current at 85°C
- 4.5-V to 18-V input voltage range
- Wide-output voltage adjust (0.9 V to 5.5 V)
- Efficiencies Up To 93%
- On/off inhibit
- UVLO
- Output overcurrent protection (non-latching, auto-reset)
- Overtemperature protection
- Ambient temperature range: –40°C to +85°C
- Surface-mount package
- Safety agency approvals: UL/CUL 60950, EN60950

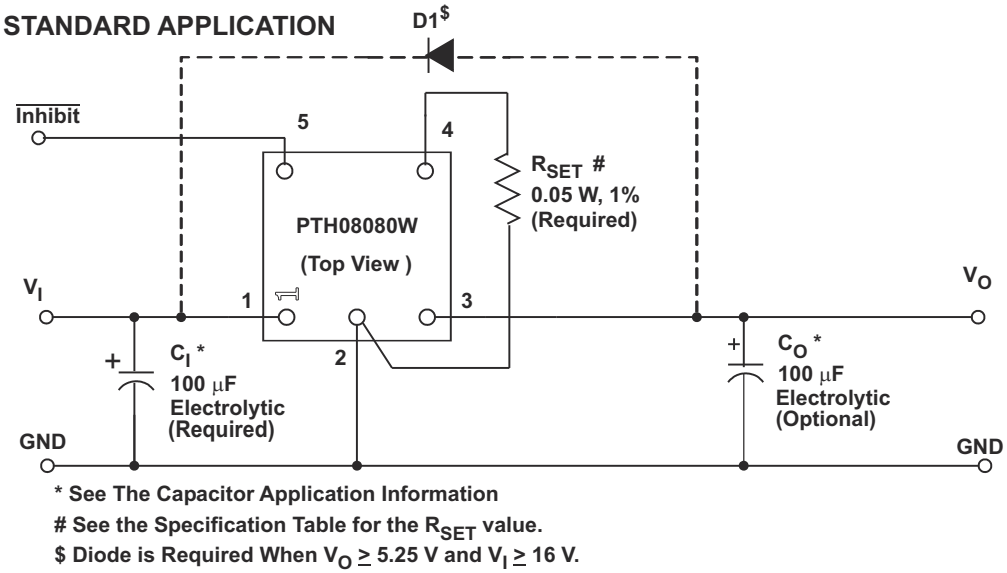


図 2-8. PTH08080W Standard Application

2.2.8 TLV1117

The TLV1117 device is a positive low-dropout voltage regulator designed to provide up to 800 mA of output current. The device is available in 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V, and adjustable-output voltage options. All internal circuitry is designed to operate down to 1-V input-to-output differential. Dropout voltage is specified at a maximum of 1.3 V at 800 mA, decreasing at lower load currents.

- 1.5-V, 1.8-V, 2.5-V, 3.3-V, 5-V, and adjustable-output voltage options
- Output current: 800 mA
- Specified dropout voltage at multiple current levels
- 0.2% line regulation maximum
- 0.4% load regulation maximum

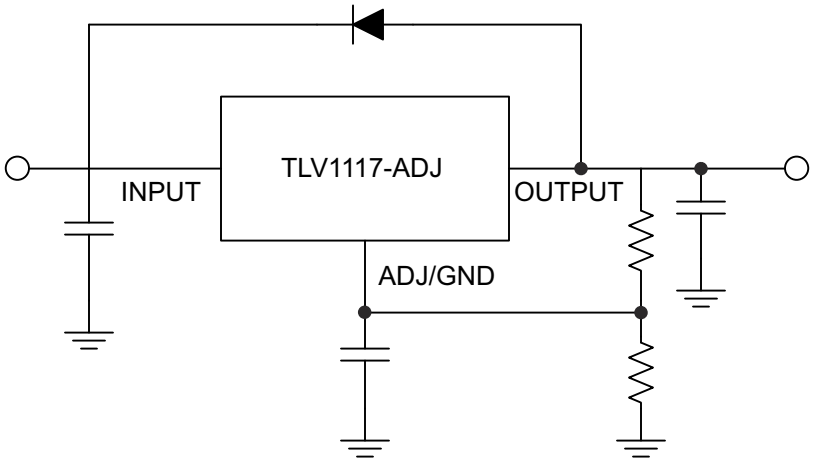


図 2-9. TLV1117 Simplified Schematic

2.2.9 OPA350

The OPA350 series of rail-to-rail CMOS operational amplifiers are optimized for low voltage, single-supply operation. Rail-to-rail input and output, low noise (5 nV/√Hz), and high speed operation (38 MHz, 22 V/µs) make the amplifiers ideal for driving sampling ADCs. They are also suited for cell phone PA control loops and video processing (75-Ω drive capability), as well as audio and general purpose applications. Single, dual, and quad versions have identical specifications for maximum design flexibility.

- Rail-to-rail input

- Rail-to-rail output (within 10 mV)
- Wide bandwidth: 38 MHz
- High slew rate: 22 V/µs
- Low noise: 5 nV/√Hz
- Low THD+noise: 0.0006%
- Unity-gain stable
- MicroSize packages
- Single, dual, and quad

2.2.10 UCC14240

The UCC14240-Q1 is a high-isolation, automotive qualified 2.0-W DC/DC module designed to provide power to SiC or IGBT gate drivers. The device integrates a transformer and DC/DC controller through proprietary architecture to achieve the smallest design size and high power density, while achieving high efficiency with very low emissions. The high-accuracy (±1.3 %), adjustable output voltages optimize gate drive voltage to provide higher system efficiency at high switching frequencies. Power-Limit and Fault Protection features maintain reliable SiC and IGBT FET operation.

- Fully integrated high-density isolated DC/DC module with isolation transformer
- Isolated DC/DC for driving: IGBTs, SiC FETs
- Input voltage range: 21 V to 27 V with 32-V absolute maximum
- 2.0-W output power at T_A ≤ 85°C and > 1.5 W at T_A = 105°C
- Adjustable (VDD – VEE) output voltage (with external resistors): 18 V to 25 V, ±1.3 % regulation accuracy over full temperature range
- Adjustable (COM – VEE) output voltage (with external resistors): from 2.5 V to (VDD – VEE), ±1.3 % regulation accuracy over full temperature range
- Low electromagnetic emission with spread spectrum modulation and integrated transformer design
- Enable, Power Good, UVLO, OVLO, soft-start, short-circuit, power-limit, under-voltage, overvoltage, and overtemperature protection
- CMTI > 150 kV/µs
- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C ≤ T_J ≤ 150°C
  - Temperature grade 1: –40 °C ≤ T_A ≤ 125°C
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Planned safety-related certifications:
  - 4243-V_{PK} basic isolation per DIN EN IEC 60747-17 (VDE 0884-17) –
  - 3000-V_{RMS} isolation for 1 minute per UL1577 –
  - Basic insulation per CQC GB4943.1
- 36-pin, wide SSOP package

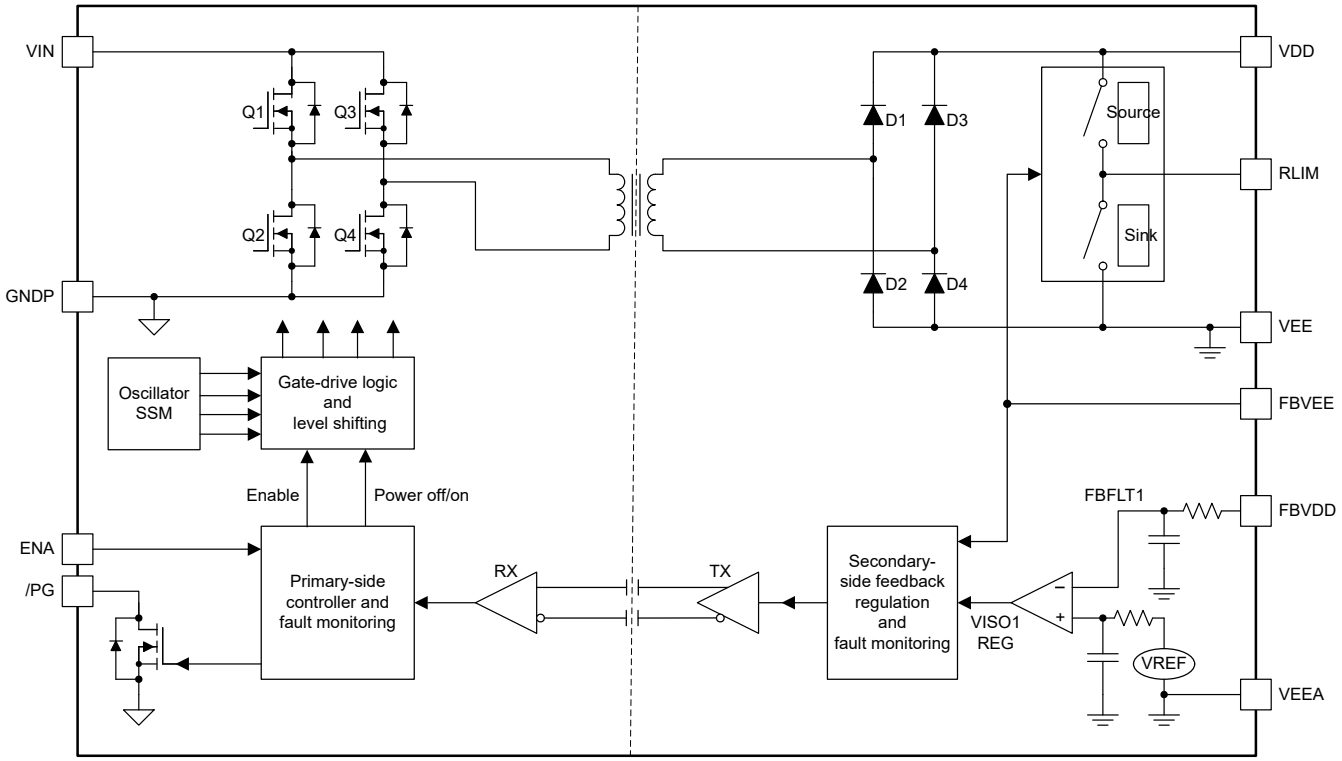


図 2-10. UCC14240 Typical Application

2.3 System Design Theory

2.3.1 Three-Phase T-Type Inverter

2.3.1.1 Architecture Overview

To understand the impetus behind a three level t-type inverter, some background on a traditional two-level inverter is required. A typical implementation of this architecture is shown in 図 2-11.

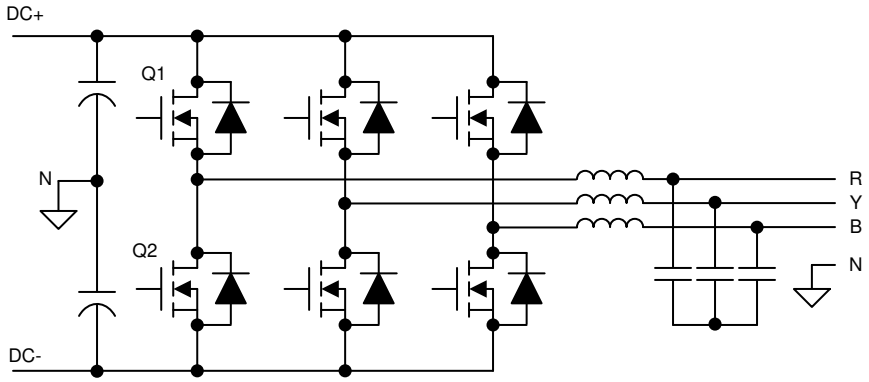


図 2-11. Two-Level, Three-Phase Inverter Architecture

To simplify the analysis, a single leg can be isolated.

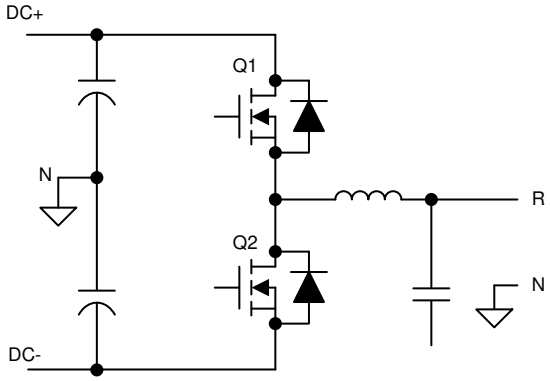


図 2-12. Two-Level, Single-Phase Inverter Leg

In this example, the two switching devices as a pair have four possible conduction states, independent of the other phases:

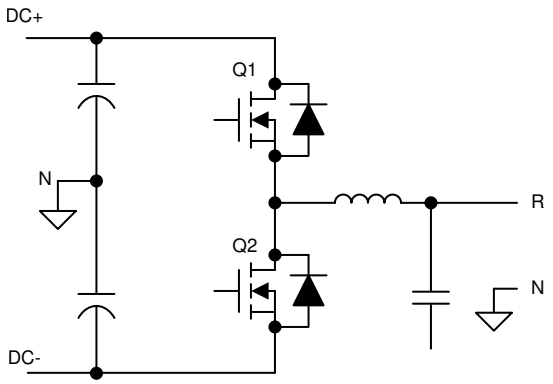


図 2-13. Q1 and Q2 off

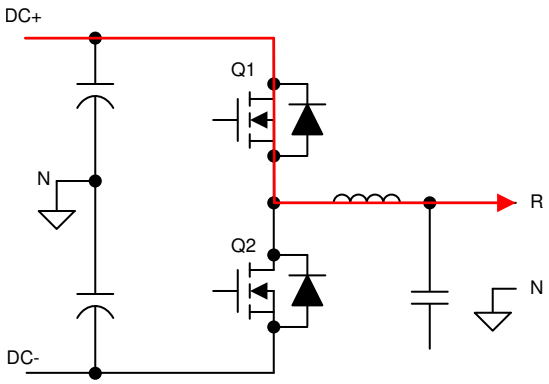


図 2-14. Q1 on, and Q2 off

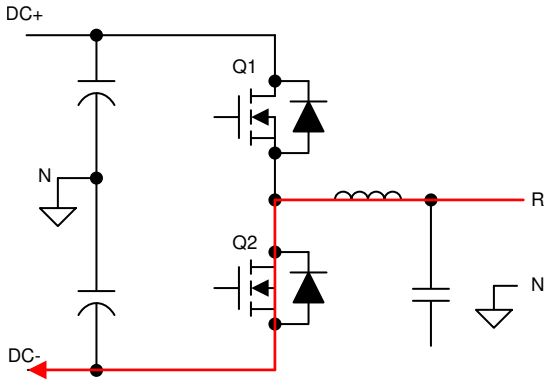


図 2-15. Q1 off, and Q2 on

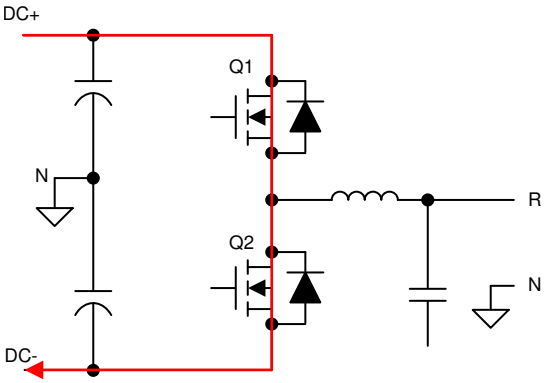


図 2-16. Q1 and Q2 on (Invalid)

By observing the current path through the inverter, each switching device must be capable of blocking the full DC link voltage present between DC+ and DC–. In traditional low-voltage systems (< 600 V), this capability is fairly trivial with common off-the-shelf IGBTs. However, if the DC link voltage is pushed higher to increase the power throughput without increasing current, as is a common trend in power electronics, this limitation puts an upper level on the supported voltage ranges.

Additionally, the increased voltage does result in increased switching losses in the traditional IGBTs. The low dV/dt exacerbates itself in these devices, even if they are able to support the higher voltages. This dV/dt is what determines how quickly one device can transition from on to off (or vice versa), thus dictating the dead time between each of these states. An elongated switch time or dead time means the switches spend less time at full conduction, resulting in decreased efficiency.

These two primary drawbacks of a two-level inverter are what drives the implementation in this design.

The next step up from a standard two-level inverter is a T-type three-level inverter. This type is implemented by inserting two back-to-back switching devices between the switch node and the neutral point of the DC link created by the bulk input capacitors. These two switch devices are placed in a common emitter configuration so that current flow can be controlled by switching one or the other on or off. This configuration also enables both of them to share a common bias supply as the gate-emitter voltage is identically referenced. 図 2-17 shows a simplified view of the implementation.

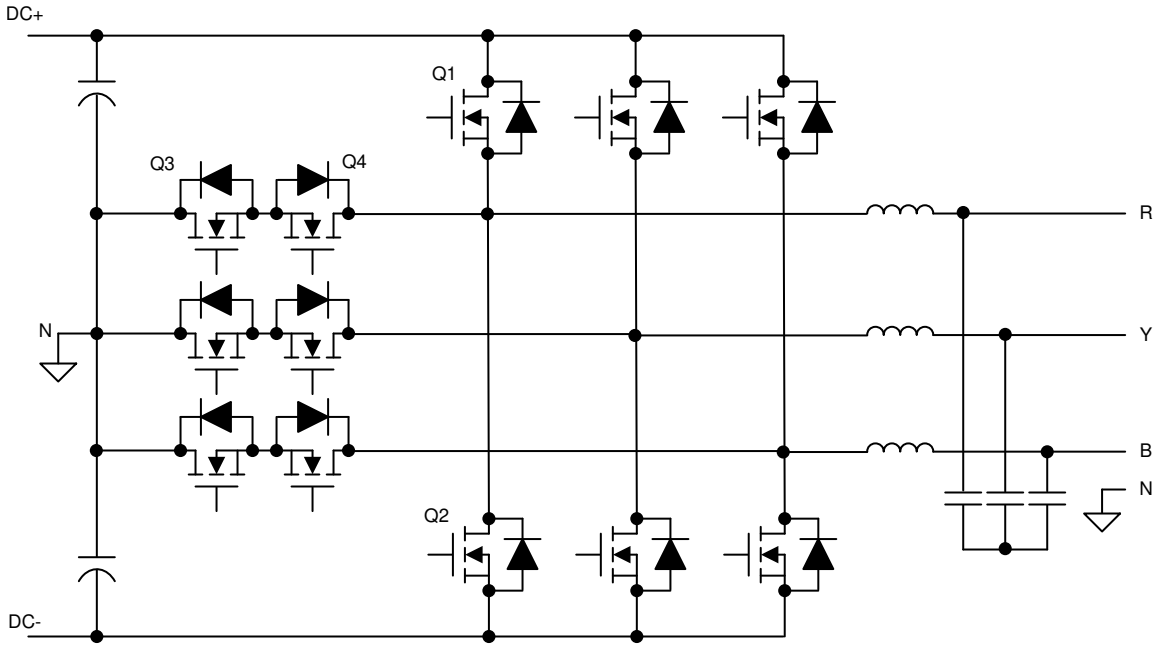


図 2-17. Three-Level T-Type, Three-Phase Inverter Architecture

To assist in understanding the benefits of the architecture, the inverter is again reduced to a single leg.

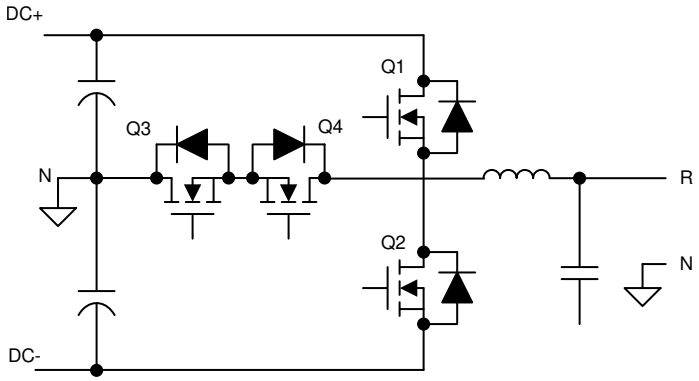


図 2-18. Three-Level T-Type, Single-Phase Inverter Leg

Adding two extra switching devices complicates the control of the system, but the same process of evaluating current flow during various modulation points illustrates the architecture benefits. Additionally, a simplified commutation scheme can be demonstrated, illustrating that control of a T-type inverter is not substantially more difficult than a traditional two-level architecture.

A single leg has three potential connection states: DC+, DC–, or N. This connection can be accomplished by closing Q1, closing Q3 and Q4, and closing Q2, respectively. However, this scheme depends on the current path in the system. Rather, for a DC+ connection, Q1 and Q3 can be closed, Q2 and Q4 for a neutral connection, and Q2 and Q4 for a DC– connection. This scheme acts independent of current direction as shown in the following figures.

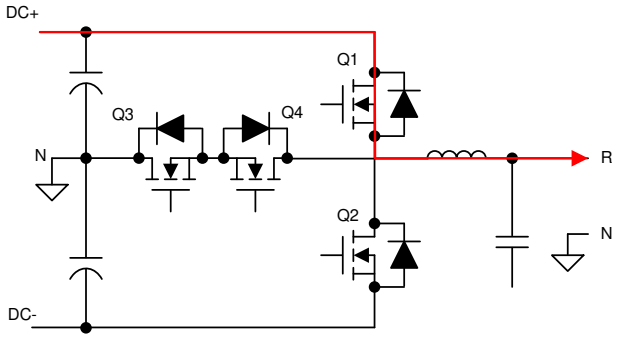


図 2-19. Q1 on, Q2 off, Q3 on, and Q4 off

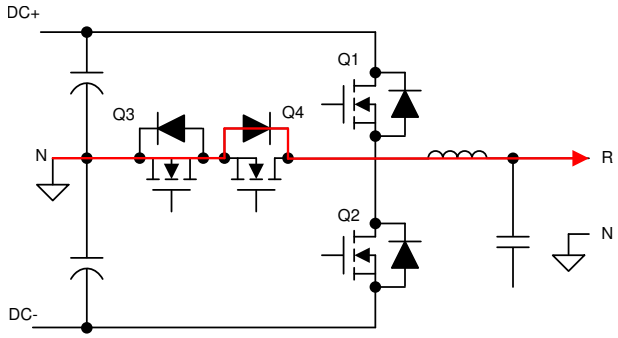


図 2-20. Q1 off, Q2 off, Q3 on, and Q4 off

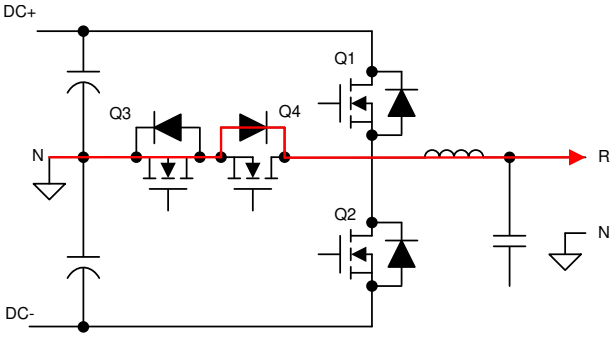


図 2-21. Q1 off, Q2 off, Q3 on, and Q4 on

This example starts with the output phase connected to DC+ by closing Q1 and Q3, resulting in current output from the system. To transition to an N connection, Q1 is opened and after a dead-time delay, and Q4 is closed. This setup allows current to naturally flow through Q3 and the diode of Q4.

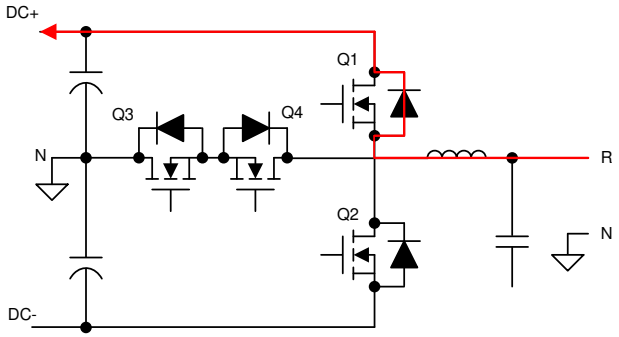


図 2-22. Q1 on, Q2 off, Q3 on, and Q4 off

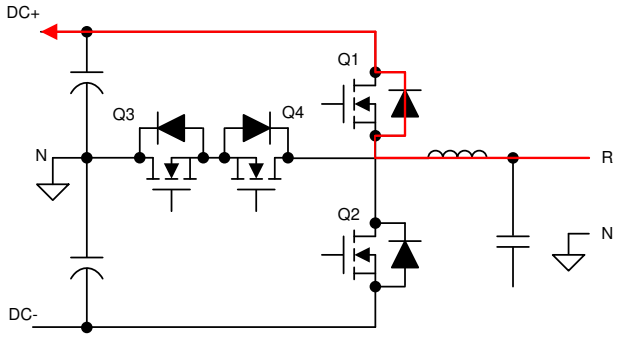


図 2-23. Q1 off, Q2 off, Q3 on, and Q4 off

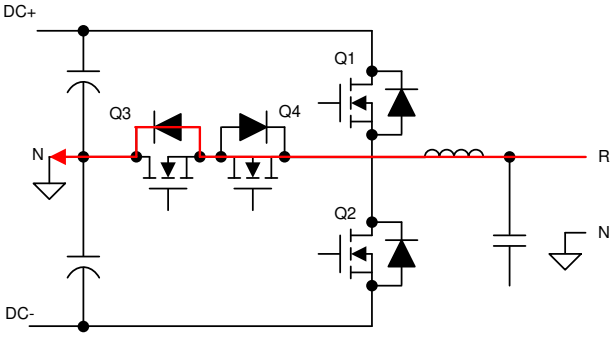


図 2-24. Q1 off, Q2 off, Q3 on, and Q4 on

For a negative current, the same sequence can be used. Once Q4 is closed, current then flows through it and the diode of Q3 rather than the diode of Q1.

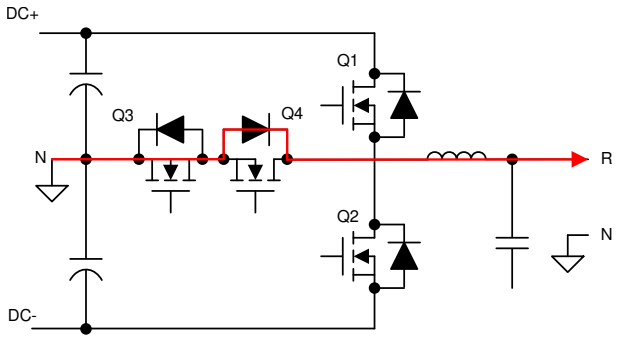


図 2-25. Q1 off, Q2 off, Q3 on, Q4 on

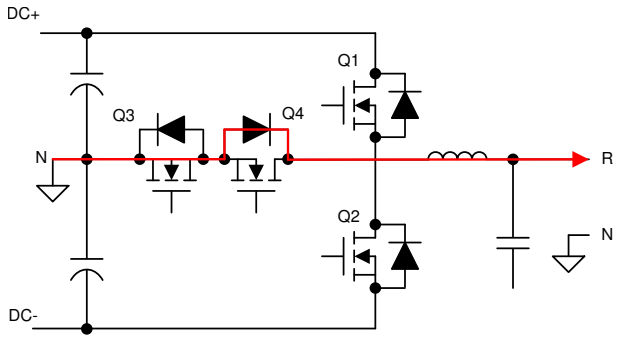


図 2-26. Q1 off, Q2 off, Q3 on, Q4 off

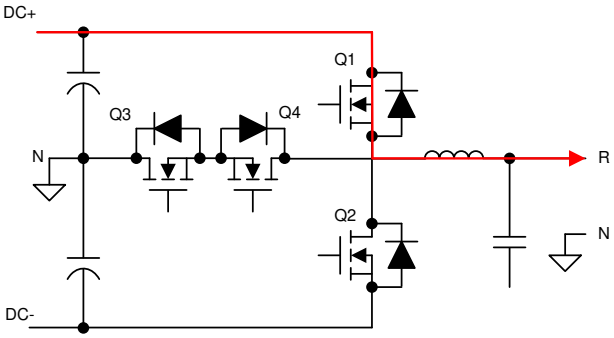


図 2-27. Q1 on, Q2 off, Q3 on, Q4 off

A similar natural current flow can be observed when connecting the output leg from N to DC+ with a positive current. Q3 and Q4 start closed with a full N connection. Q4 is switched off, but current still flows through its associated diode. Closing Q1 now naturally switches the current flow from N to DC+.

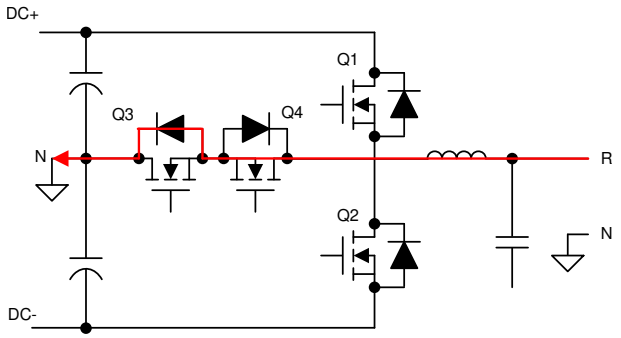


図 2-28. Q1 off, Q2 off, Q3 on, Q4 on

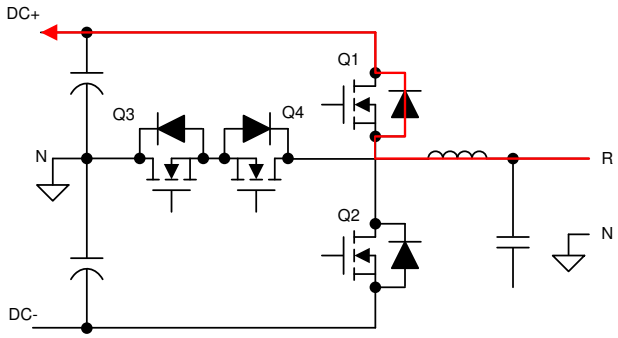


図 2-29. Q1 off, Q2 off, Q3 on, Q4 off

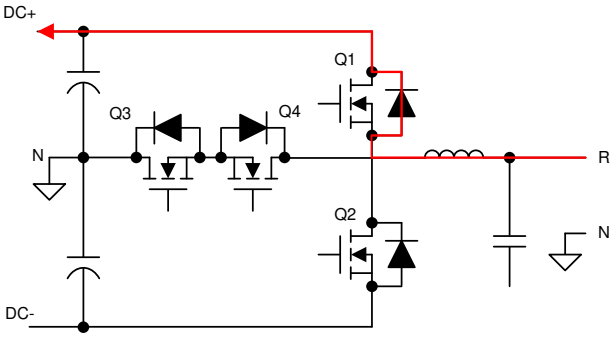


図 2-30. Q1 on, Q2 off, Q3 on, Q4 off

As in the earlier example when moving from a DC+ to N connection on a negative current, the same scheme can also be used here for a positive current. Q3 and Q4 begin closed, conducting current into N. Q4 is opened, causing current to flow through the diode of Q1. Lastly, Q1 is closed, and current remains flowing in the same direction.

All four of these transition states (DC+ to N, N to DC+, with both forward and reverse current) all share two simple switching schemes. This also holds true for transitions to and from DC– through Q2. By maintaining this scheme through all switching cycles, a simple dead-zone delay between switching events is all that is needed to avoid shoot-though; however, additional protection can be added in the control software with relative ease.

An additional benefit from this modulation scheme is that Q3 and Q4 never switch at the same time. This benefit reduces voltage stress on the devices as well as the power rating of the bias supply to drive these devices effectively. As mentioned earlier, Q3 and Q4 can share a single supply sized for one driver rather than two.

Q1 and Q2 still need to block the full DC link voltage as they would in the traditional architecture. To use a higher DC bus voltage, full-voltage FETs still need to be in place here; however, because they are back to back and do not switch at the same time, the two switches on the center leg can be at a lower rating.

2.3.1.2 LCL Filter Design

Any system of power transfer to the grid is required to meet certain output specifications for harmonic content. In voltage sourced systems like modern photo-voltaic inverters, a high-order LCL filter typically provides sufficient harmonic attenuation, along with reducing the overall design size versus a simpler filter design. However, due to the higher order nature, take some care in its design to control resonance. 図 2-31 shows a typical LCL filter.

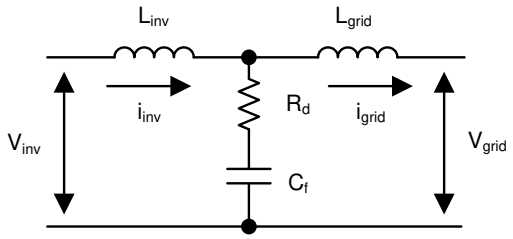


図 2-31. LCL Filter Architecture

One of the key benefits of using SiC MOSFETs (as this reference design does) is the ability to increase the switching frequency of the power stage significantly versus traditional Si-based switching elements. This increased switching frequency has a direct impact on the inverter's output filter resonant design, which needs to be accounted for. To ensure that the filter is designed correctly around this switch frequency, this known mathematical model is used in this design.

The primary component is the inverter inductor, or L_{inv}, which can be derived using 式 1:

$$L_{inv} = \frac{V_{DC}}{8 \times f_{SW} \times I_{grid\_rated} \times \%ripple} \tag{1}$$

Using re-determined system specifications, one can easily calculate the primary inductor value:

$$L_{inv} = \frac{1000\ V}{8 \times 50\ kHz \times 18\ A \times 40\%} = 347\ \mu H \tag{2}$$

The sizing of the primary filter capacitor is handled in a similar fashion using 式 3:

$$C_f = \frac{\%x \times Qrated}{2 \times \pi \times F_{grid} \times V_{grid}^{\ 2}} \tag{3}$$

Make some design assumptions to finalize the value of C_f , namely, limiting the total reactive power absorbed by the capacitor to 5%. Scaling the total system power by the per phase power results in a primary capacitor value of:

$$I_{att} = \frac{1}{\left|1 + r \times \left(1 - L_{inv} \times C_b \times \left(2 \times \pi \times f_{SW}\right)^2 \times x\right)\right|} \times 100 \tag{4}$$

$$C_f = \frac{5\% \times \frac{10\ kW}{3}}{2 \times \pi \times 50\ Hz \times \left(\frac{400}{\sqrt{3}}\right)^2} = 9.947\ \mu F \tag{5}$$

$$C_b = \frac{C_f}{x\%} = 199\ \mu F \tag{6}$$

For the remainder of the filter design, determine the values by defining the attenuation factor between the allowable ripple in grid inductor and the inverter inductor. This factor needs to be minimized while still maintaining a stable and cost effective total filter. By assuming an attenuation factor, an r value, which defines the ratio between the two inductors, is determined using 式 4:

To obtain an attenuation factor of 10%, and using the earlier derived values, the value of r can be evaluated to be:

$$r = \left| \frac{\frac{1}{10\%} - 1}{1 - 347\ \mu H \times 199\ \mu F \times \left(2 \times \pi \times 50\ kHz\right)^2 \times 5\%} \right| = 2.7\% \tag{7}$$

The resultant value for L_{grid} is then:

$$L_{grid} = r \times L_{inv} = 9.34\ \mu h \tag{8}$$

The filter design can be validated by determining its resonant frequency (F_{res}). A good criteria for ensuring a stable F_{res} is that it is an order of magnitude above the line frequency and less than half the switching frequency. This criteria avoids issues in the upper and lower harmonic spectrums. The resonant frequency of the filter is defined using 式 9:

$$F_{res} = \frac{1}{2 \times \pi \times \sqrt{\frac{L_{grid} \times L_{inv}}{L_{grid} + L_{inv}} \times C_f}} \tag{9}$$

Or, using the derived filter values:

$$F_{res} = \frac{1}{2 \times \pi \times \sqrt{\frac{9.34\ \mu H \times 347\ \mu H}{9.34\ \mu H + 347\ \mu H} \times 9.95\ \mu F}} = 16.733\ kHz \tag{10}$$

This value for F_{res} meets the criteria listed earlier and validates the filter design.

The remaining value to determine is the passive damping that must be added to avoid oscillation. Generally, a damping resistor at the same relative order of magnitude as the C_f impedance at resonance is suitable. This impedance is easily derived using 式 11:

$$R_d = \frac{1}{6 \times \pi \times F_{res} \times C_f} \tag{11}$$

$$R_d = \frac{1}{6 \times \pi \times 16.733\ kHz \times 9.95\ \mu H} = 0.316\ \Omega \tag{12}$$

For the final implementation in hardware, use real values for all of these components based on product availability and must be chosen to be appropriately close (±10% typically). When final values are determined, recalculate the resonant frequency to ensure the filter is still stable.

2.3.1.3 Inductor Design

With the filter being one of the major contributors to the size and weight of a solar inverter, ensure that the individual components are correctly sized. As seen in セクション 2.3.1.2, the increase in the system switching speed provided by the SiC MOSFETs has already resulted in an inverter inductor that is of much smaller value than normal.

In 式 1, the switching frequency is in the denominator. Any increase in switch frequency, all else being the same, results in an inverse relationship. Looking at the simplified equation for the inductance of a given inductor, there is a positive relationship between inductance and inductor cross sectional area by a number of turns. Both have a direct effect on the size of the component.

$$L = \frac{0.4 \times \pi \times \mu \times N^2 \times A \times 10^{-2}}{\ell} \tag{13}$$

where

- μ is core permeability
- N is the number of turns
- A is the cross sectional area
- l is the mean magnetic path length

The starting point for evaluating a solution to the variables in 式 13 is to determine a valid core material and subsequent permeability. The core manufacturer typically has a range of suitable materials with selection criteria based on the design inductance and the inductor current. For this design, the nominal inductor current (with an overload factor of 105%) is defined as:

$$I_{ind\_nom} = \frac{KVA_{out} \times 105\%}{\sqrt{3}\ V_{grid}} \tag{14}$$

$$I_{ind\_nom} = \frac{10\ kVA \times 105\%}{\sqrt{3} \times 400} = 15.155\ A \tag{15}$$

Using a selection guide for a toroidal inductor core manufacturer, at 347 μH, the core permeability comes to 26 μH. The core also provides a value for the inductance factor, A_L, which enables a quick path to selecting the number of turns.

$$N = \sqrt{\frac{L \times 10^3}{A_L}} \tag{16}$$

$$N = \sqrt{\frac{347\ \mu H \times 10^3}{49}} = 84 \tag{17}$$

One last piece of information required for the inductor design is the winding wire size. This size is easily computed using the nominal inductor current rating. Using copper, with a current carrying density of 4 A/mm, this inductor requires a cross sectional area of:

$$A_w = \frac{I_{ind\_nom}}{4} = \frac{15.155}{4} = 3.789\ mm^2 \tag{18}$$

This area is an equivalent to American Wire Gauge #12, which has a cross sectional area of 3.309 mm^2. This slight derating is acceptable because the switching current allows a smaller gauge to be used when compared to a static DC bias current. For this inductor, flat winding is used to increase surface area for cooling and decrease potential skin depth effects.

Using the overall design of the core, with the flat 12 AWG winding, the total length of each winding is determined to be 64.87 mm. At this point, the DC resistance of the inductor can be calculated using Pouillet's Law:

$$R_{DC} = \rho \frac{\ell}{A} \tag{19}$$

$$R_{DC} = \left(17 \times 10^{-9}\right) \frac{84 \times 64.87 \text{ mm} \times 10^{-3}}{3.309 \text{ mm}^2 \times 10^{-6}} = 0.028 \ \Omega \tag{20}$$

To determine the AC resistance, first calculate the skin depth at the inverter switching frequency:

$$S_d = 1000 \times \sqrt{\frac{\rho}{\pi \times f_{SW} \times \mu_o}} \tag{21}$$

$$S_d = 1000 \times \sqrt{\frac{17 \times 10^{-9}}{\pi \times 50 \text{ kHz} \times 4 \times \pi \times 10^{-7}}} = 0.293 \text{ mm} \tag{22}$$

R_{AC} is then determined by R_{DC}, S_d, and S_s, which is the equivalent square conductor width.

$$R_{AC} = R_{DC} \times \frac{1}{2} \times \left(\frac{S_s}{S_d}\right) \times \left(\frac{\sinh\left(\frac{S_s}{S_d}\right) + \sin\left(\frac{S_s}{S_d}\right)}{\cosh\left(\frac{S_s}{S_d}\right) - \cos\left(\frac{S_s}{S_d}\right)} \right) = 0.087 \ \Omega \tag{23}$$

This determination of R_{AC} helps determine total system losses.

2.3.1.4 SiC MOSFETs Selection

As shown in the architecture overview, the main switching device needs to support the full switching voltage. To support the 1000-V DC link voltage of this design, use 1200-V FETs; however, at this voltage, the migration to SiC is necessitated by several factors:

- The switching speed of a 1200-V SiC MOSFET is significantly faster than a traditional IGBT, leading to a reduction in switching losses.
- The reverse recovery charge is significantly smaller in the SiC MOSFET, resulting in reduced voltage and current overshoot.
- A lower temperature dependence at full load due to reduced conduction loss.

The middle switches are only exposed to half of the DC link voltage, or 500 V in this design. As such, a 650-V device is acceptable. A full SiC design provides the best performance due to these same features. For this design, the reverse recovery loss and voltage overshoot limits the device selection. As such, a 1200-V SiC MOSFET + 650-V MOSFET design is used.

Conduction loss is mainly determined by the $R_{DS(on)}$ of the 1200-V SiC MOSFET and the on $R_{DS(on)}$ of the 650-V SiC MOSFET. The 75-mΩ SiC devices have a good high-temperature performance, and the $R_{DS(on)}$ only increases 40% at 150°C junction temperature. With the high temperature I-V curve in the data sheet, calculate the conduction loss on the devices.

Switching loss is a function of the switching frequency and switching energy of each switching transient, the switching energy is related with device current and voltage at the switching transient. Using the switching energy curve in the data sheet, one can estimate the total switching loss.

Similarly, the conduction loss and switching loss can be estimated for all the devices and efficiency can be estimated. With the thermal impedance information of the thermal system design, the proper device rating can be selected. The 1200-V/75-mΩ SiC MOSFET and 650-V/60-mΩ SiC MOSFET is a good tradeoff among thermal, efficiency and cost.

2.3.1.5 Loss Estimations

The primary source of lost efficiency in any inverter is going to be a result of the losses incurred in the switching devices. These losses are broken into three categories for each device:

- Conduction loss: When the device is on and conducting normally
- Switching loss: When the device is switching between states
- Diode conduction loss: Related to voltage drop and current when in conduction

Each of these are dictated by their own equation, and can be determined from the device data sheet and design parameters that have already been set.

Conduction loss is driven by the on-time of the FET, the switched current, and the on-resistance:

$$P_{cond\_loss} = \frac{1}{T}\int_0^T V_{ce}(t) \times I_c(t) \times D_Q(t)dt \tag{24}$$

where

- V_{ce} is the conduction voltage drop
- I_c is the conduction current
- D_Q is the duty cycle
- T represents one modulation cycle

Switching loss is determined by the switching energy of the device and the switching voltage at a selected test point. Determine the value of the switching energy from the device data sheet using the value of the designed external gate resistor. The remainder of the values needed were determined earlier in the design phase.

$$P_{sw\_loss} = \frac{(E_{on} + E_{off}) \times I_{peak} \times f_{SW} \times V_{DC}}{\pi \times I_{avg} \times V_{nom}} \tag{25}$$

図 2-32 shows an example of the graph used to extract the switching energy values from the device data sheet is shown for an C3M0060065D SiC MOSFET.

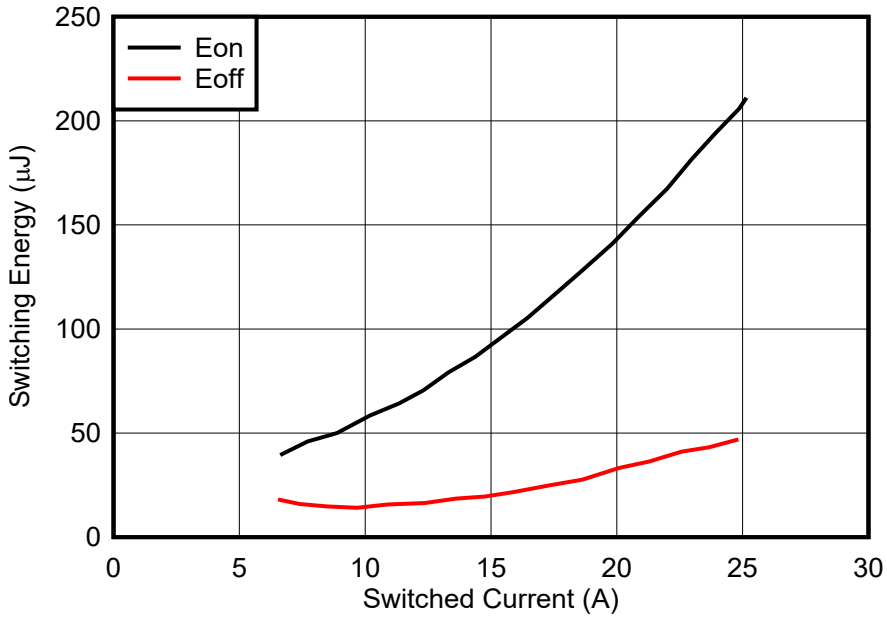


図 2-32. Switching Energy vs Switched Current for C3M0060065D

The diode conduction loss is similarly calculated using known values:

$$P_{sw\_diode} = \frac{1}{T}\int_0^T Vf(t) \times If(t) \times D_D(t)dt \quad (26)$$

where

- V_f is the voltage drop
- I_f is the diode current
- D_D is the duty cycle
- T represents one modulation cycle

Using these three equations, the expected losses of the design are computed for both the SiC MOSFETs as shown in 表 2-1.

表 2-1. Expected Losses of Switching Devices

PARAMETER	C3M0075120D (Q1)	C3M0060065D (Q3)
Conduction loss	5.76 W	4.5 W
Switching loss	1.8 W	1.13 W
Diode loss	0 W	0 W
Total	7.56 W	5.63 W

The final piece of the total system loss estimation is the inductor losses. These losses are determined using the value of the inductor DC and AC resistance and expected inductor current from セクション 2.3.1.3.

$$Pind\_loss = I_{ind\_ac\_rms}^2 \times R_{DC} + I_{ind\_ripple\_rms}^2 \times R_{AC} \quad (27)$$

$$P_{ind\_loss} = (0.81\ A)^2 \times 0.024\ \Omega + (15.155)^2 \times 0.076\ \Omega = 5.64\ W \quad (28)$$

The total major energy loss for this design is then:

$$P_{loss\_total} = 6 \times \left(P_{Q1\_total} + P_{Q3\_total}\right) + 3 \times P_{int\_loss} \quad (29)$$

$$P_{loss\_total} = 6 \times (5.631\ W + 7.56\ W) + 3 \times 5.64\ W = 96.102\ W \quad (30)$$

Use 式 30 to determine the total expected inverter efficiency. Note that this is an estimation, but the estimate allows the design to be validated up to this point.

$$\eta = \frac{P_{out}}{P_{out} + P_{loss\_total}} \times 100 \quad (31)$$

$$\eta = \frac{10\ kW}{10\ kW + 96.102\ W} = 99.048\% \quad (32)$$

2.3.1.6 Thermal Considerations

The loss estimations can also allow the heat output of the design to be characterized. Any electrical loss in the system is converted to waste heat.

Thermal simulations where performed using the physical layout of the design, as well as the expected energy losses. An off the shelf heat sink from Wakefield-Vette (OMNI-UNI-18-50) was selected to simplify the design process and provide a starting reference point for understanding the thermal performance. Use this data as a starting point for a thermal design, and not a fully-validated design.

The system was simulated using a worse-than-calculated thermal output of 10 W per switching device. This meant 120 W of total power dissipation across all three phases. 図 2-33 and 図 2-34 show the thermal simulation results with no fans.

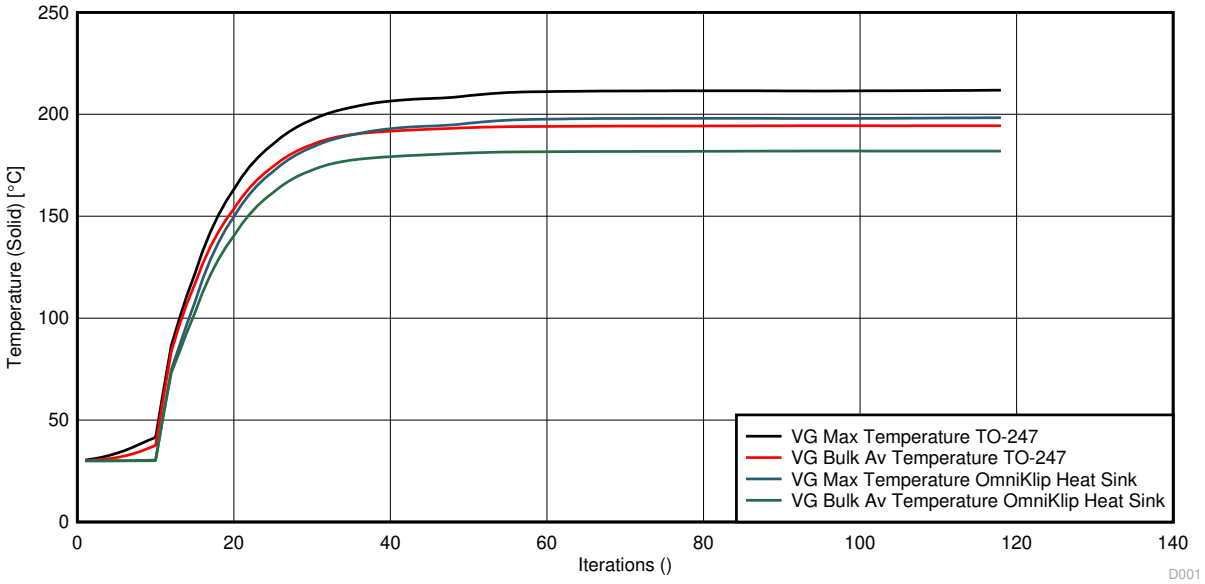


図 2-33. Simulated Temperature vs Time

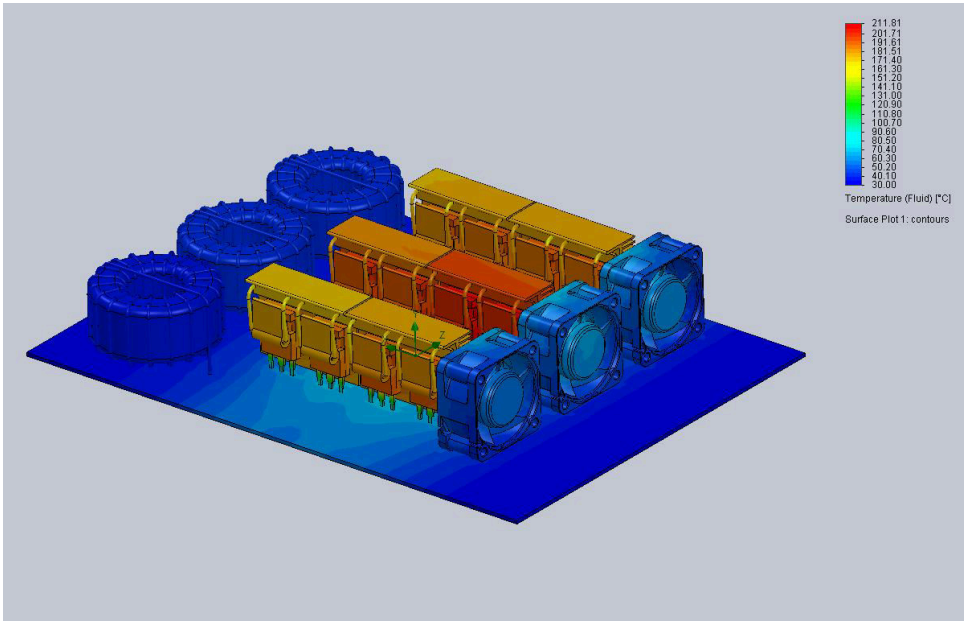


図 2-34. Passive Thermal Simulation Result

In this simulation, with only natural convection and small off the shelf heat sinks, the TO-247 package of the MOSFETs reaches a maximum temperature of 215°C, and the SiC MOSFET reaches 197°C. These temperatures are both outside the maximum allowed temperature range of the devices.

図 2-35 shows the next simulation, which includes active airflow and full ducting of the heat generating devices. This airflow reduces the maximum temperature of the MOSFET under a 130% load to be 130°C. This temperature is within the design constraint of the 175°C junction temperature of the C3M0060065D, which is the major heat generator. Please contact wakefield-Vette for details on the thermal simulation.

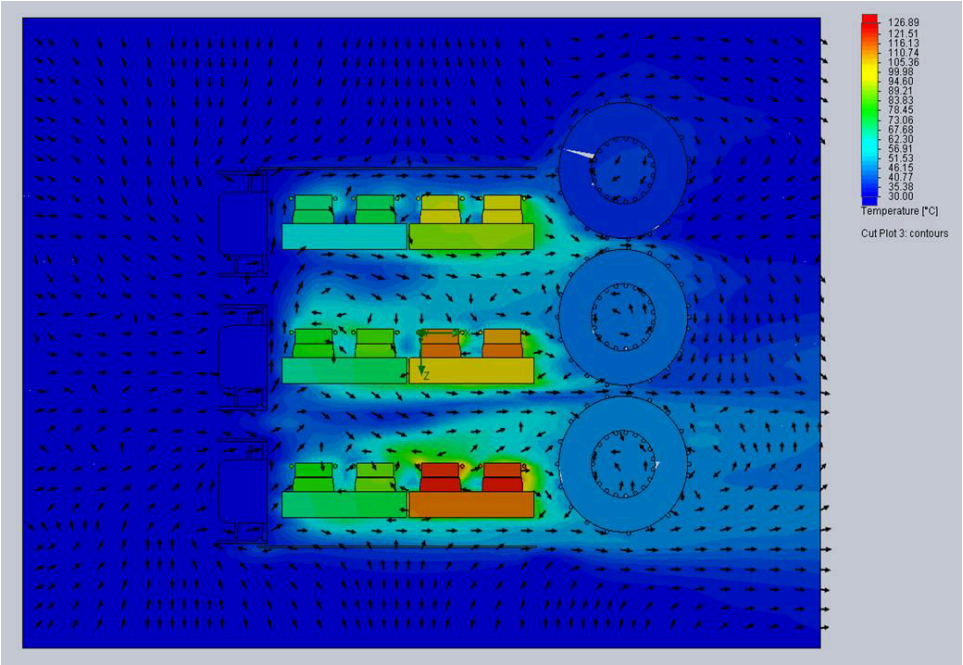


図 2-35. Active Ducted Thermal Simulation

2.3.2 Voltage Sensing

Voltage sensing happens at two points in the inverter signal path to aid in control: before and after the primary output relay. By enabling measurement on both sides of the relay, the control system can lock into the grid voltage and frequency before connecting, thus preventing any mismatch issues.

Both sensing topologies are similar. First, PGND is used as a virtual neutral using a resistor network. On the grid side of the relay, only neutral is used. The high voltage signal is attenuated using a series of large value resistances. An offset of 1.65 V is added to the attenuated neutral point to center the voltage signal in the middle of the input range of the OPA4350, and the attenuated value from the phase voltage is measured. 図 2-36 shows this sensing arrangement.

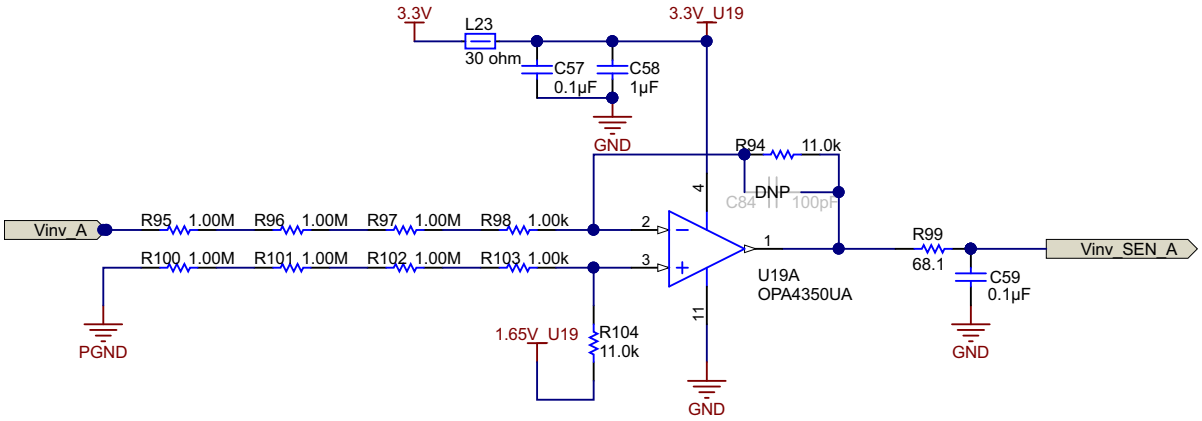


図 2-36. High-Voltage Sensing Signal Path

2.3.3 Current Sensing

Critical to attaining a closed-loop control system is accurate current measurement of the inverter. In this design, current measurement is done at two locations with different sensing technologies. The first location is on the grid output using shunt resistors. Because the output is high voltage and the controller needs to remain isolated, the AMC1306M05 reinforced modulator is used to measure the resistor voltage drop. To keep system losses low, the AMC1306M05 has a ±50-mV input range. When compared to other devices with a typical input range of ±250 mV, the total power loss across the shunt is significantly reduced.

Sizing the shunt resistor for this design is a trade-off between sensing accuracy and power dissipation. A 0.002-Ω shunt provides a ±50-mV output signal at the approximate ±25-A output inverter but also only generates 0.5 W of heat at full load. When choosing an actual device, select a high accuracy value to eliminate the need to calibrate each sensor path.

The voltage across the shunt resistor is fed into the AMC1306M05 sigma-delta modulator, which generates the sigma-delta stream that is decoded by the SDFM demodulator present on the C2000™ MCU. The clock for the modulator is generated from the eCAP peripheral on the C2000 MCU, and the AMC1306M05 data is decided using the built-in SDFM modulator.

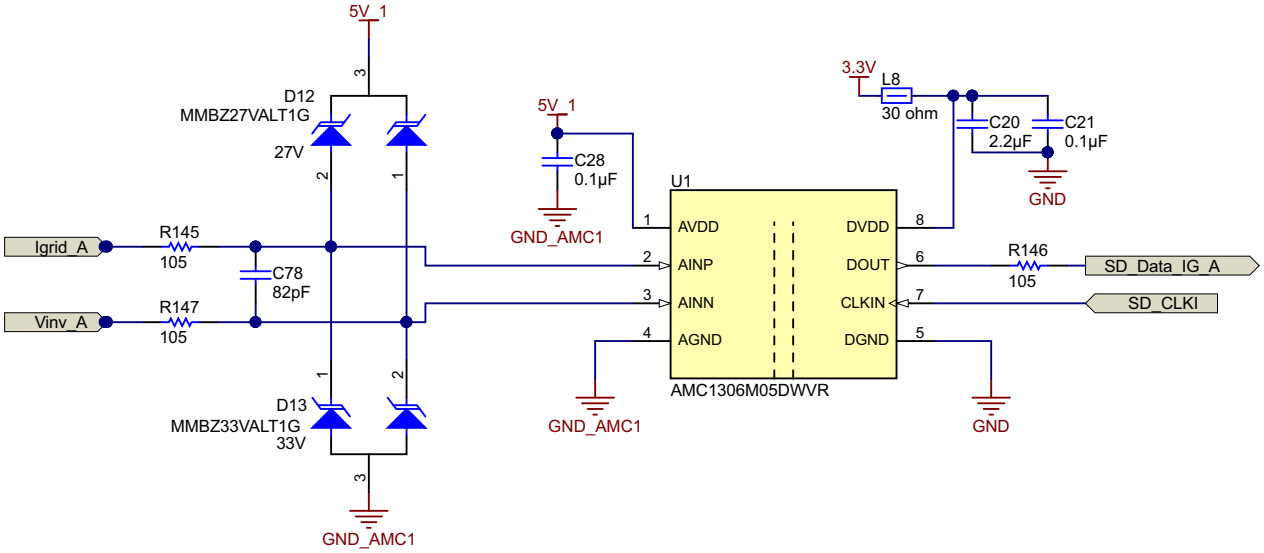


図 2-37. Isolated Shunt Sensing With AMC1305M05

The second location is a Hall-effect sensor, which is used to sense the current through the inductor. The Hall-effect sensor has a built-in offset, and the range is different than what ADC can measure. Therefore, the voltage is scaled to match the ADC range using the circuit shown in 図 2-39 and 式 33. Of note here, the OPA4340 is used over the OPA4350 in the voltage sense path due to the lower bandwidth of the former. The low bandwidth helps to reduce accidental amplification of switching noise that can be picked up by long traces in the PCB.

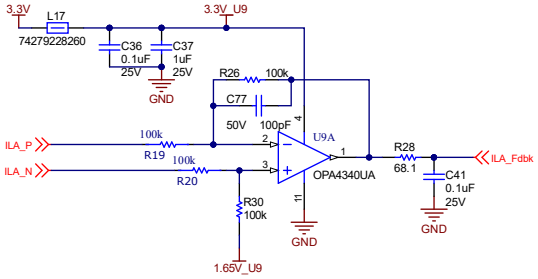


図 2-38. Isolated Hall Effect Current Sensing

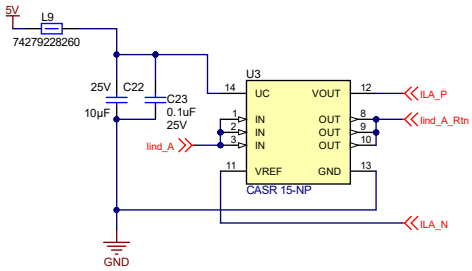


図 2-39. Hall Effect Sensor Matching

$$V_{out} = \frac{R_f}{R_e}\left(\frac{V_{nominal}}{I_{max}} + V_{offset}\right) \quad (33)$$

2.3.4 System Power Supplies

This reference design uses multiple voltage domains across the system:

- A primary high-voltage input to power the entire board (up to 24 V)
- 24 V to power the gate drive cards, further described in セクション 2.3.5
- 5 V to power the control card and drive isolated supplies
- Non-isolated 3.3 V for analog sensing
- Isolated 3.3 V for current shunt sensing

図 2-40 shows the full tree for all of these domains.

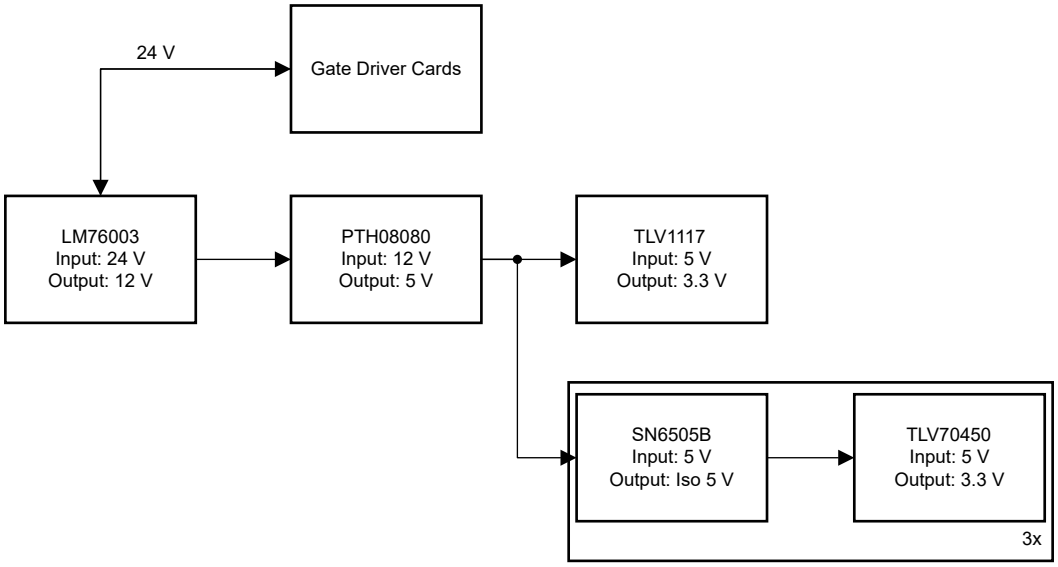


図 2-40. Power Tree

2.3.4.1 Main Input Power Conditioning

The primary voltage input for the design is rated for 15 V to 60 V. This wide V_{IN} enables the inverter to be powered from a variety of industrial voltage sources that might be used in a larger system. The range is enabled by the LM76003 synchronous step-down converter.

The converter is configured for a 12-V output using the R54 and R57 feedback resistor divider. This 12-V rail is then used to power the relays, fans, isolated gate drive bias supplies, and the remainder of the step-down converters in the system. The 3.5-A output support of the LM76003 is sufficient for this operation. The design also includes dual parallel output capacitors to reduce ESR and subsequent ripple and load transients and loads switch on an off.

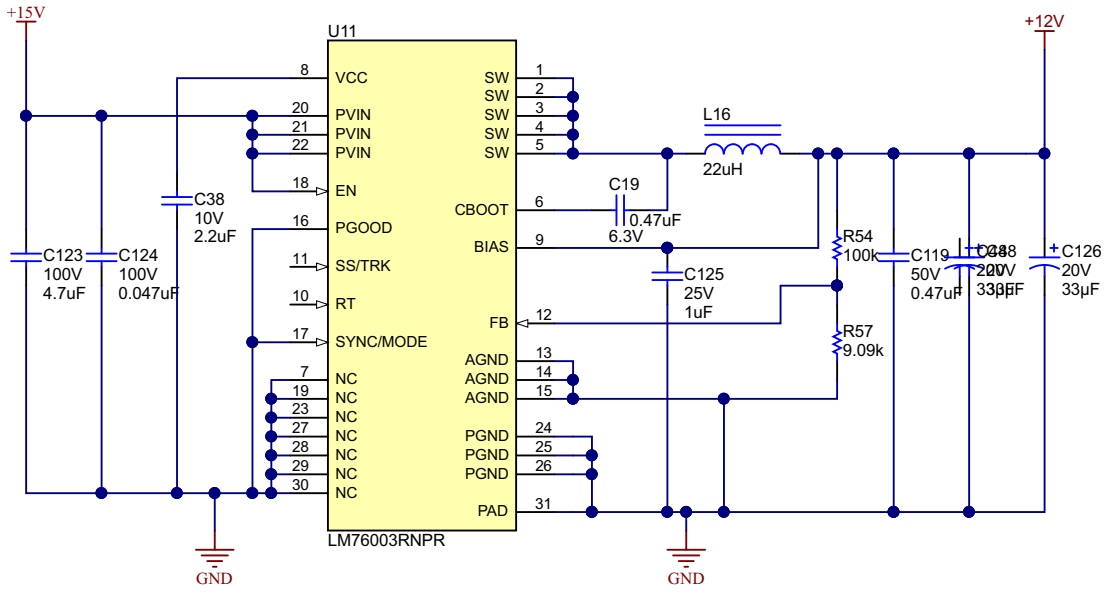


図 2-41. LM76003 12-V DC/DC Converter

2.3.4.2 Isolated Bias Supplies

To generate the isolated bias supplies for the AMC1306M05 isolated modulators, the SN6505B transformer driver is used to drive a Würth 750313638 transformer in a push-pull configuration. This is a recommended configuration from the SN6505B data sheet to build a 5-V → 6-V isolated supply.

The 6-V output is used to feed a TLV70450 LDO to generate a clean 5-V rail for the analog and digital circuitry of the AMC1306M05.

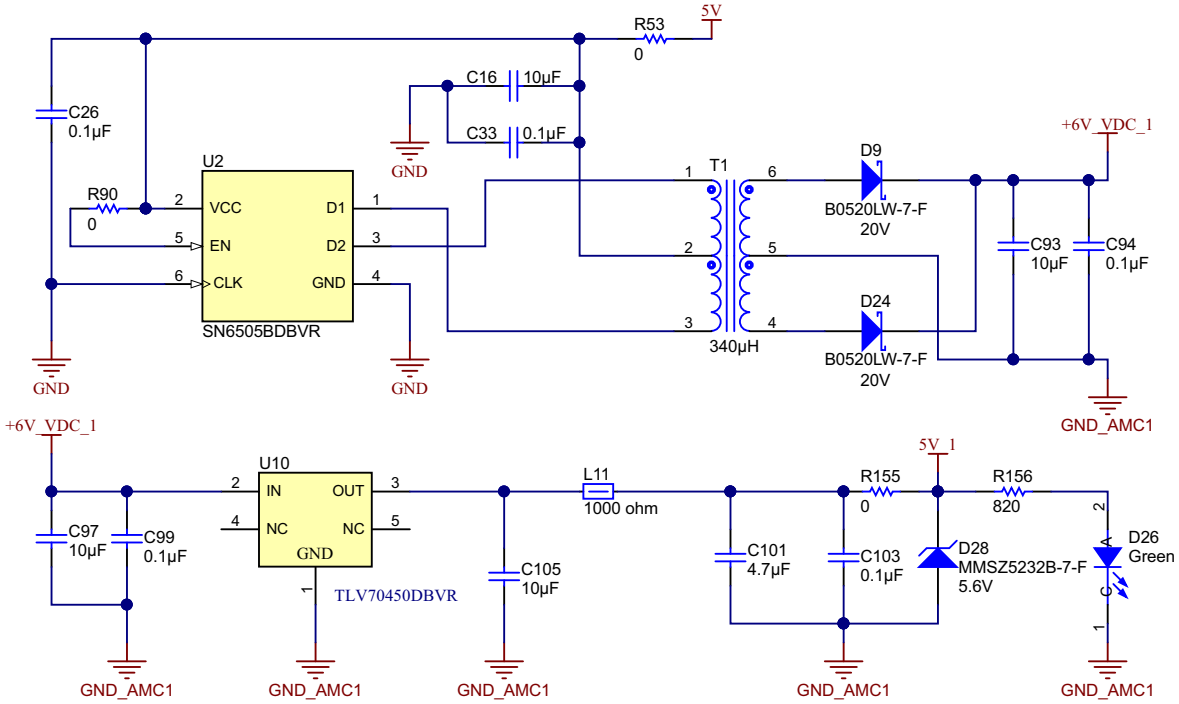


図 2-42. SN6505 Bias Voltage Supply

2.3.5 Gate Drivers

2.3.5.1 1200-V SiC MOSFETs

図 2-43 shows the schematic design of the isolated SiC MOSFET gate driver. VCC and GND are the supply pins for the input side of the UCC21710 device. The supply voltage at VCC can range from 3.0 V to 5.5 V with respect to GND. VDD and COM are the supply pins for the output side of the UCC21710 device. VEE is the supply return for the output driver and COM is the reference for the logic circuitry. The supply voltage at VDD can range from 15 V up to 30 V with respect to VEE. The PWM is applied across the IN+ and IN– pins of the gate driver.

On the secondary-side of the gate driver, gate resistors R308 and R307 control the gate current of the switching device. The DESAT fault detection prevents any destruction resulting from excessive collector currents during a short-circuit fault. To prevent damage to the switching device, the UCC21710 slowly turns off the SiC MOSFET in the event of a fault detection. A slow turnoff makes sure the overcurrent is reduced in a controlled manner during the fault condition. The DESAT diode D301 conducts the bias current from the gate driver, which allows sensing of the MOSFET-saturated collector-to-emitter voltage when the SiC MOSFET is in the ON condition.

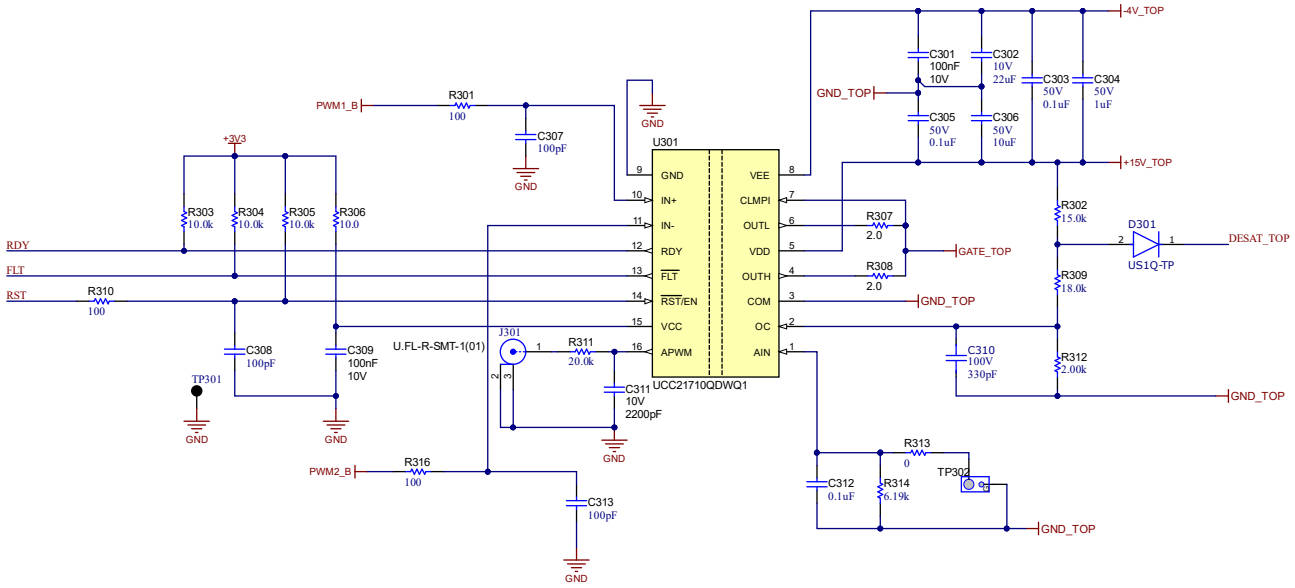


図 2-43. UCC21710 Gate Drive Circuit

2.3.5.2 650-V SiC MOSFETs

図 2-44 shows the schematic design of the isolated MOSFET gate driver. The UCC5320S primary side is powered by a 3.3-V rail. A 0.1-µF ceramic capacitor is placed close to the VCC1 pin for noise decoupling. The positive going UVLO threshold on the supply is 2.6 V and the negative going threshold is 2.5 V.

The PWM input to the gate driver is provided by the controller PWM output peripheral. Dead time must be inserted between the low-side and high-side PWM signals to prevent both switches turning on at the same time. The signal is single ended and is filtered by RC low-pass filter comprising of R417 and C410 before connecting to the gate driver input. The filter attenuates high-frequency noise and prevents overshoot and undershoot on the PWM inputs due to longer tracks from the controller to the gate driver. The inverting PWM input IN– is not used in the design and is connected to primary side ground.

The UCC5320S has split outputs that allow for controlling the turn-on rise time and turn-off fall time of the MOSFETs individually. A 3.3-Ω gate resistor R418 is used for MOSFETs turn-on. A 3.3-Ω MOSFET turn-off resistor R420 allows for strong turn-off, helping reduce turn-off losses. The low value of the turn-off resistor also increases the immunity of the gate drive circuit to Miller induced parasitic turn-on effects. A 10-kΩ resistor is connected across the MOSFET gate to collector pins close to the MOSFET on the main power board. This connection ensures that the MOSFET remains in the off state in case the gate driver gets disconnected from the MOSFET due to faults.

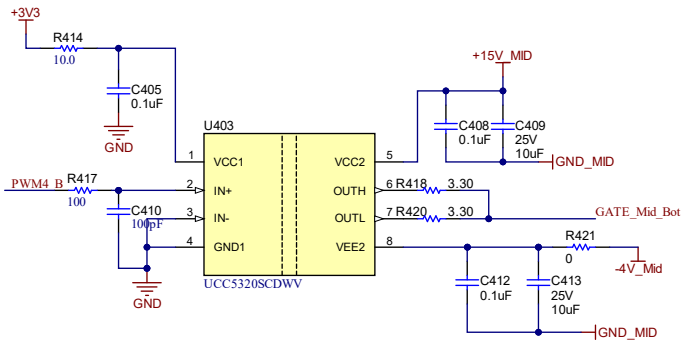


図 2-44. UCC5320 Gate Drive Circuit

2.3.5.3 Gate Driver Bias Supply

セクション 2.3.5.1 and セクション 2.3.5.2 show that the gate drivers rely on isolated bias voltages to drive the gates across the high-voltage barrier. In this architecture, there are four drivers per phase, but only three isolated domains are needed as described in セクション 2.3.1.1. These domains are:

1. +15 V and –4 V for high SiC MOSFET switch
2. +15 V and –4 V for low SiC MOSFET switch
3. +15 V and –4 V for both SiC MOSFETs in the neutral leg

The same architecture used in セクション 2.3.4.2 can generate the domains individually. However, to increase the power density of the design, the UCC1424 with integrated power supply was used. By using the following IC, this architecture decreases system complexity, cost, and size.

2.3.6 Control Design

Terminology:

V_{bus} or V_{dc}	bus voltage for the inverter
L_i and R_i	inductance of the inverter side inductor and series resistance
L_g and R_g	inductance of the grid side inductor, and series resistance
C_f and R_f	capacitance value and series resistor plus any damping resistor
v_{i_a},v_{i_b},v_{i_c}	output voltage from the three phase bridge, this voltage is what is controlled using the duty cycle control of the three phase bridge Therefore, for control purposes it is assumed now only the modulation needs to change between 2-level and 3-level inverter for the power stage and control design can remain the same. Where ,D_a, D_b, D_c, are the control variable generated such that the output voltage of the inverter can be represented as 式 34:

$$v_{i\_a} = D_a \times V_{DC}/2 \tag{34}$$

i_{i_a}, i_{i_b}, i_{i_c}	current through the inverter side inductor
v_{x_a}, v_{x_b}, v_{x_c}	voltage across the filter capacitor
i_{g_a}, i_{g_b}, i_{g_c}	voltage across the filter capacitor
v_{g_a}, v_{g_b}, v_{g_c}	grid frequency

2.3.6.1 Current Loop Design

For the inverter filter shown in 図 2-45, using KCL and KVL 式 35 can be written.

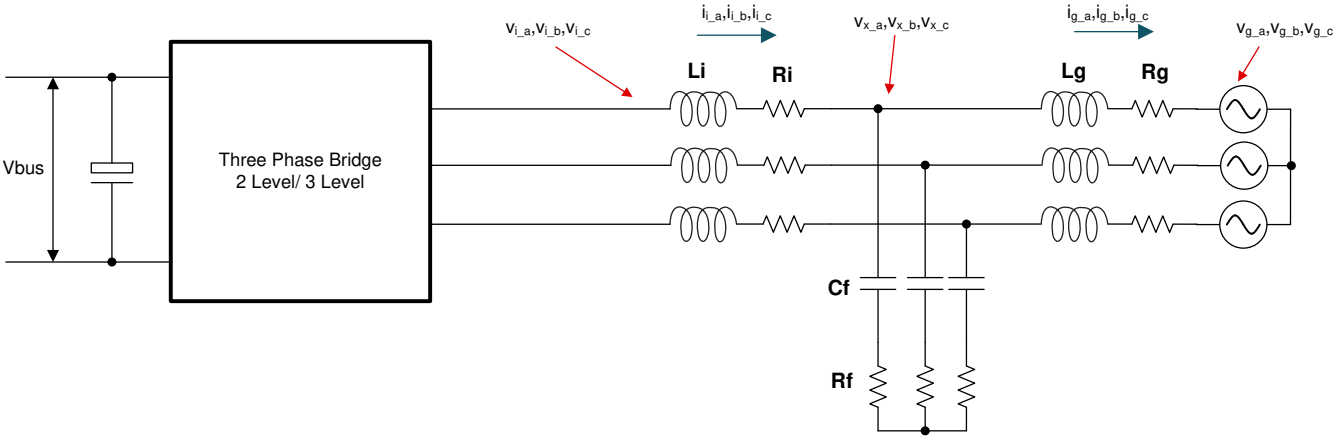


図 2-45. Inverter Model

$$v_{i\_a} - L_i \frac{di_{i\_a}}{dt} - R_i i_{i\_a} = v_{x\_a} \tag{35}$$

Upon re-arranging, 式 35 can be written as 式 36:

$$\frac{di_{i\_a}}{dt} = \frac{1}{L_i} v_{i\_a} - \frac{1}{L_i}\left(R_i i_{i\_a} + v_{x\_a}\right) \tag{36}$$

Similarly on another node, using KCL and KVL, 式 37 can be written as 式 37:

$$\frac{di_{g\_a}}{dt} = \frac{1}{L_2} v_{x\_a} - \frac{1}{L_2}\left(R_2 i_{g\_a} + v_{g\_a}\right) \tag{37}$$

Assuming R_f is negligible 式 38 can be written for the capacitor voltage:

$$\frac{dv_{x\_a}}{dt} = \frac{1}{C_f}\left(i_{i_a} - i_{g_a}\right) \tag{38}$$

Typically a synchronous reference frame control is designed, where a d_q rotating reference frame at grid frequency speed, and oriented such that the d axis is aligned to the grid voltage vector is used. Using basic trigonometric identities, i_d and i_q can be written as 式 39 and 式 40.

$$i_d = \frac{2}{3}\left(i_a \cos\omega t + i_b \cos(\omega t - 120) + i_c \cos(\omega t + 120)\right) \tag{39}$$

$$i_q = -\frac{2}{3}\left(i_a \sin\omega t + i_b \sin(\omega t - 120) + i_c \sin(\omega t + 120)\right) \tag{40}$$

Taking the derivative, and using the partial derivative theorem, 式 41 is written:

$$\begin{aligned} &\xrightarrow{\text{yields}} \frac{di_d}{dt} = \frac{2}{3}\left(\frac{di_a}{dt}\cos\omega t + \frac{di_b}{dt}\cos(\omega t - 120) + \frac{di_c}{dt}\cos(\omega t + 120)\right) + \omega i_q \\ &\frac{di_d}{dt} = \frac{2}{3}\left(\frac{di_a}{dt}\cos\omega t + \frac{di_b}{dt}\cos(\omega t - 120) + \frac{di_c}{dt}\cos(\omega t + 120)\right) - \frac{2}{3}\omega\left(i_a \sin\omega t + i_b \sin(\omega t - 120) + i_c \sin(\omega t + 120)\right) \end{aligned} \tag{41}$$

The following state equations can be written:

$$\frac{di_{i\_d}}{dt} = \frac{1}{L_i} v_{i\_d} + \omega i_{i\_q} - \frac{1}{L_i}\left(R_i i_{i\_d} + v_{x\_d}\right) \tag{42}$$

$$\frac{di_{i\_q}}{dt} = \frac{1}{L_i} v_{i\_q} - \omega i_{i\_d} - \frac{1}{L_i}\left(R_i i_{i\_q} + v_{x\_q}\right) \tag{43}$$

Hence, using these equations, and substituting in 式 44:

$$\left(sL_i\right) i_{i\_d}(s) = v_{i\_d}(s) + \left(\omega L_i\right) i_{i\_q}(s) - \left(R_i i_{i\_d}(s) + v_{x\_d}(s)\right) \tag{44}$$

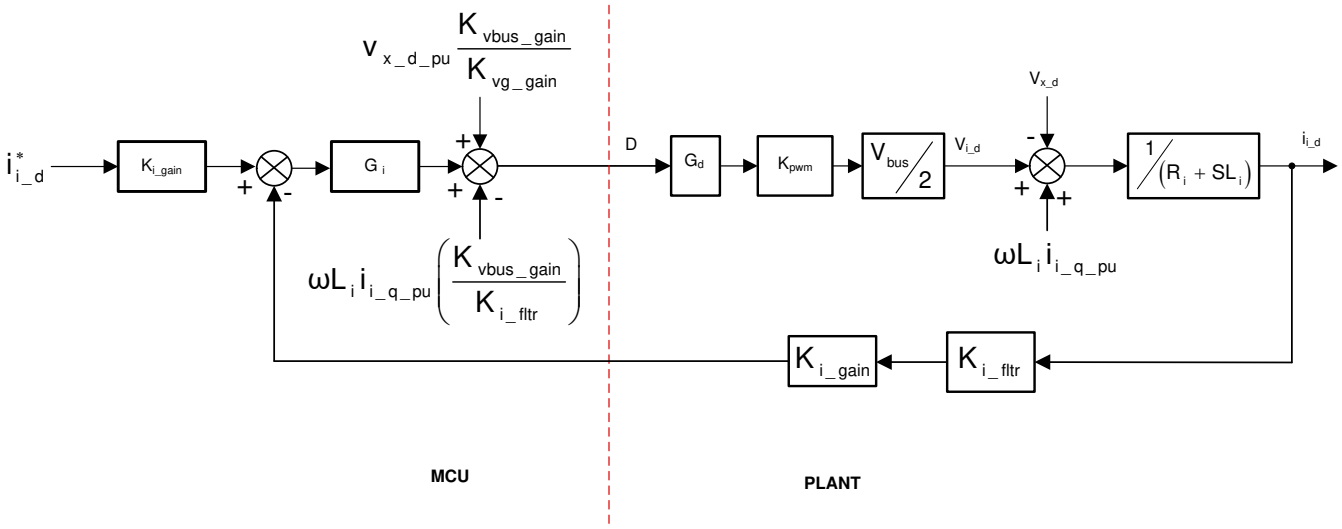
Taking the Laplace function on the previous equations:

$$\left(sL_i\right) i_{i\_q}(s) = v_{i_q}(s) - \left(\omega L_i\right) i_{i\_d}(s) - \left(R_i i_{i\_q}(s) + v_{x\_q}(s)\right) \tag{45}$$

When written in control diagram format, this looks like the following. Feedforward elements are added to remove additional sources of disturbances and errors in the model, two feedforward elements are added,

1. For the coupling term from the other axis in synchronous frame
2. For the output grid voltage

The diagram is drawn as shown in 図 2-46.



where:

- $i^*_{i\_d}$ is the current reference
- K_{i_gain} is the current sense scalar which is one over max current sense
- K_{i_fltr} is the filter that is connected on the current sense path. current sense scalar which is one over max current sense
- K_{vbus_gain} is the voltage sense scalar for the bus, which is one over max voltage sensed
- K_{vg_gain} is the voltage sense scalar for the grid voltage, which is one over max voltage sensed

図 2-46. Id Current Loop Model

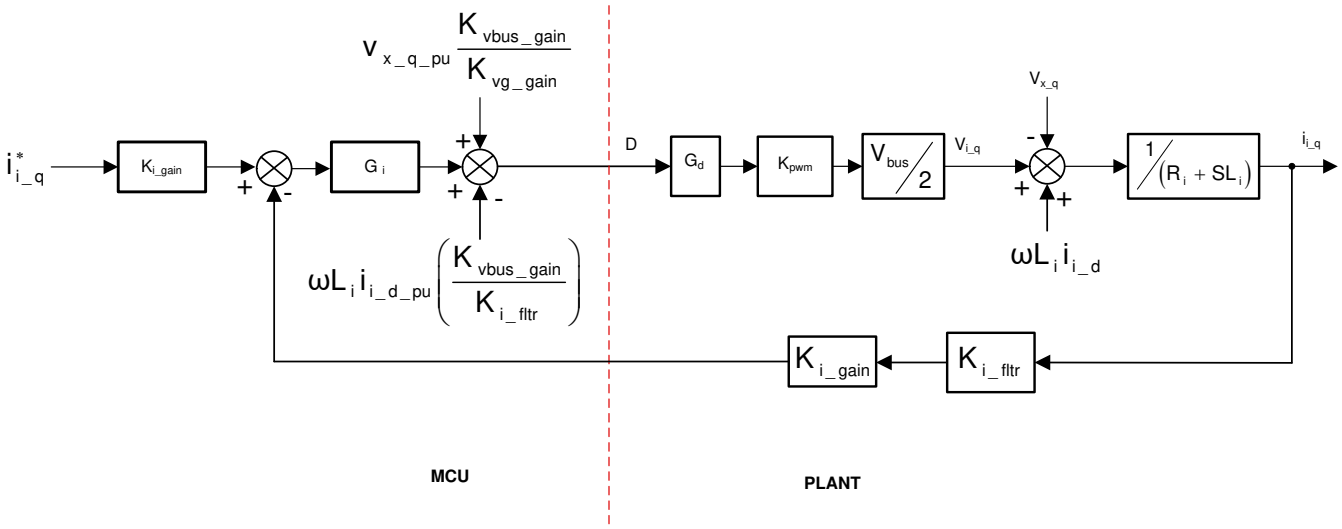


図 2-47. Iq Current Loop Model

With the feedforward elements, the small signal model can be written as 式 46(Note: Separate scaling factors are applied to bus voltage and grid voltage due to the differences in the sensing range.):

$$\frac{\hat{i}_{i\_d\_pu}}{\hat{d}} = G_d K_{pwm} \frac{1}{K_{vbus\_gain}} K_{i\_gain} K_{i\_fltr} \frac{1}{(R_i + sL_i)} \tag{46}$$

In the case of an LCL filter, the following can be assumed as a simplified model as in 式 47:

$$\frac{\hat{i}_{i\_d\_pu}}{\hat{d}} = G_d K_{pwm} \frac{1}{K_{vbus\_gain}} K_{i\_gain} K_{i\_fltr} \frac{1}{\left(Z_i + Z_c Z_f \middle/ \left(Z_c + Z_f \right) \right)} \tag{47}$$

The current loop plant is compared with the SFRA measured data for the current loop as illustrated in 図 2-48.

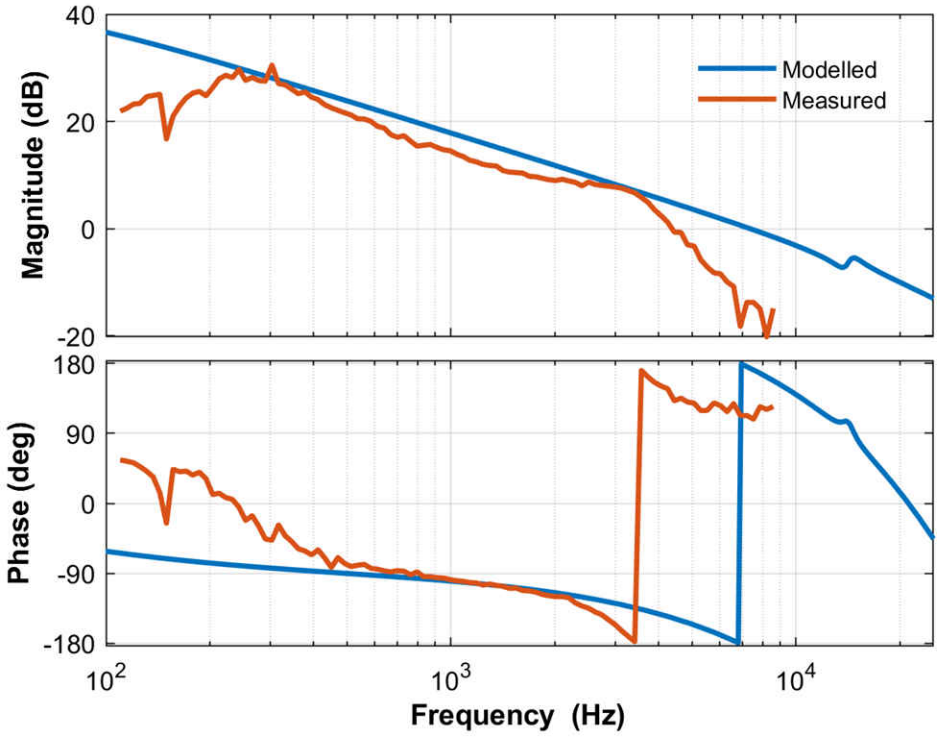


図 2-48. Current Loop Plant Frequency Response Modelled vs Measured

式 48 represents the compensator designed for the closed-loop operation:

$$G_i = 0.3 \times \frac{\left(s + 2\pi \times 95.6 \right)}{s} \tag{48}$$

With which the open loop plot in 図 2-49 is achieved, gives roughly > 1-kHz bandwidth in the I_d and I_q loop.

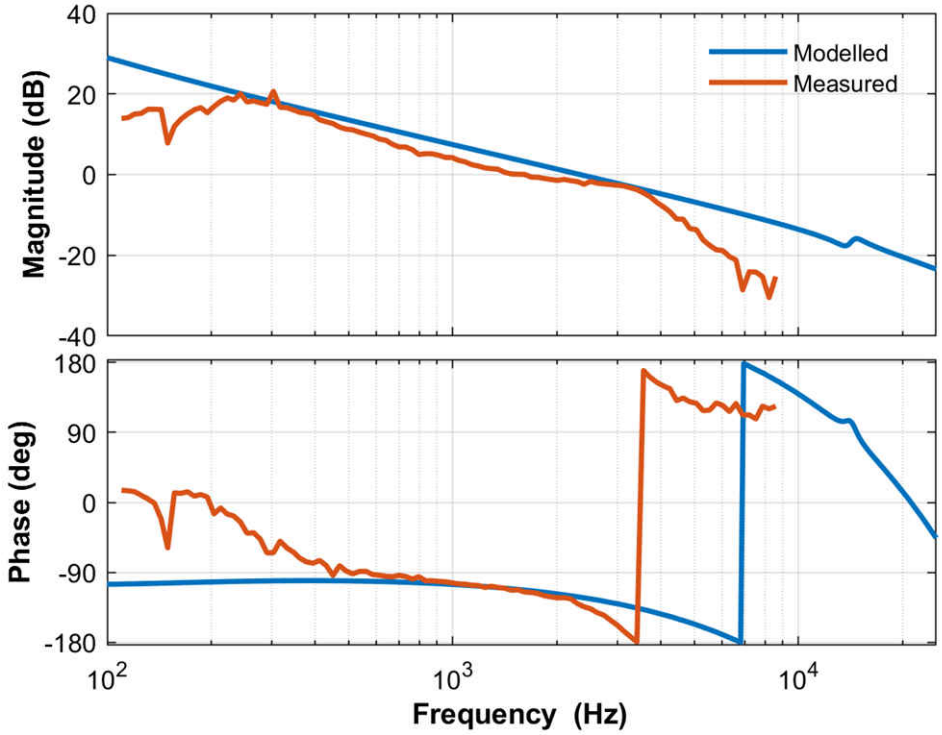


図 2-49. Current Loop, Open Loop Response Modelled vs Measured

2.3.6.2 PFC DC Bus Voltage Regulation Loop Design

Before looking at the voltage loop model, the power measurement from DQ domain can be written as:

$$P = v_a i_a + v_b i_b + v_c i_c = \begin{bmatrix} v_a & v_b & v_c \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \left(T^{-1}_{abc->dq0} \overrightarrow{v_{dq0}}\right)^T \left(T^{-1}_{dq0->abc} \overrightarrow{i_{dq0}}\right) = \overrightarrow{v_{dq0}} \left(T^{-1}_{abc->dq0}\right)^T T^{-1}_{abc->dq0} \overrightarrow{i_{dq0}} = \frac{3}{2}\left(v_{gd} i_d + v_{gq} i_q + v_{g0} i_0\right) \quad (49)$$

where

$$T_{abc->dq0} = \frac{2}{3} \begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin(\omega t) & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \\ 1/2 & 1/2 & 1/2 \end{bmatrix}$$

Hence:

$$P = \frac{3}{2}\left(v_{gd} i_d + v_{gq} i_q\right) \quad (50)$$

$$Q = -v_{gd} i_d + v_{gq} i_q \quad (51)$$

The DC Bus regulation loop is assumed to be providing the power reference, which is divided by the square of the line voltages RMS to provide the conductance. When further multiplied by the line voltage gives the instantaneous current.

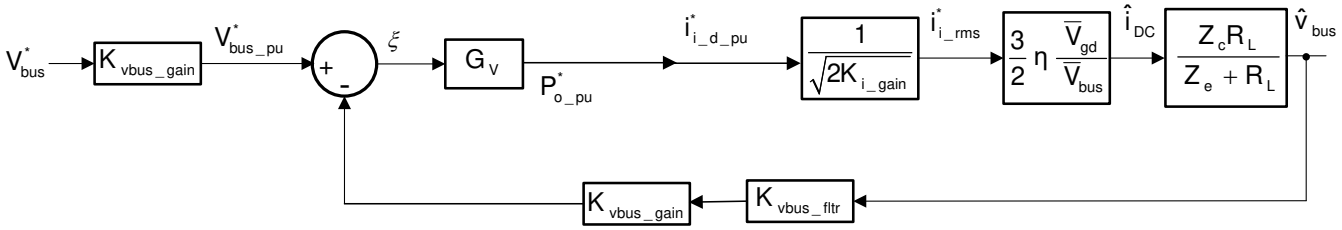


図 2-50. Voltage Loop Model

A small-signal model of the DC bus regulation loop is developed by linearizing 式 52 around the operating point:

$$i_{DC}v_{bus} = 3\eta v_{g\_rms}i_{g\_rms} \Rightarrow \hat{i}_{DC} = 3\eta\frac{\bar{V}_{g\_rms}}{\bar{V}_{bus}}\hat{i}_{g\_rms} \tag{52}$$

Because transformation is an amplitude invariant, translating from RMS to peak quantities using $\hat{i}_{g\_rms} = \frac{1}{\sqrt{2}}\hat{i}_{gd}$ and $\hat{v}_{g\_rms} = \frac{1}{\sqrt{2}}\hat{v}_{gd}$, 式 53 can be derived.

$$\hat{i}_{DC} = \frac{3}{2}\frac{\bar{V}_{gd}}{\bar{V}_{bus}}\hat{i}_{gd} \tag{53}$$

Also for resistive load on the DC Bus: $\hat{v}_{bus} = \frac{Z_c R_L}{Z_c + R_L}\hat{i}_{DC}$.

Therefore, the voltage loop plant can be written as 式 54

$$G_{v\_bus} = \frac{Z_c R_L}{Z_c + R_L} \times p \times \frac{K_{vbus_{fltr}} \times K_{vbus_{gain}}}{K_{i_{gain}}} \times \frac{1}{\left(V_{bus} \times K_{vg_{gain}}\right)} \times \frac{3}{2} \times \left(\frac{V_{g\_peak}}{V_{g\_Sense\_max}}\right) \tag{54}$$

Using the previous model the following compensator, 式 55 is designed for the voltage loop:

$$G_v = 1.8581 \times \frac{(s + 2\pi \times 35)}{s} \tag{55}$$

SFRA is used to measure the voltage loop bandwidth, and compare against the model which shows good correlation to the model. 図 2-51 shows the plant frequency response comparison and 図 2-52 shows the open-loop frequency response comparison of modelled versus measured.

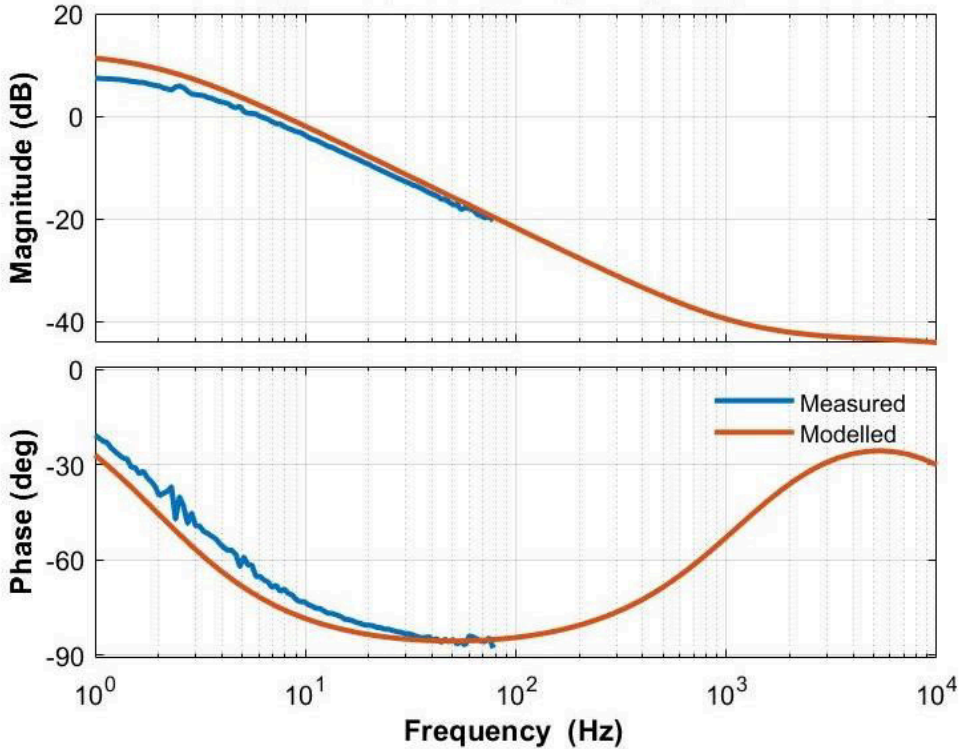


図 2-51. Voltage Loop Plant Frequency Response Measured vs Modelled

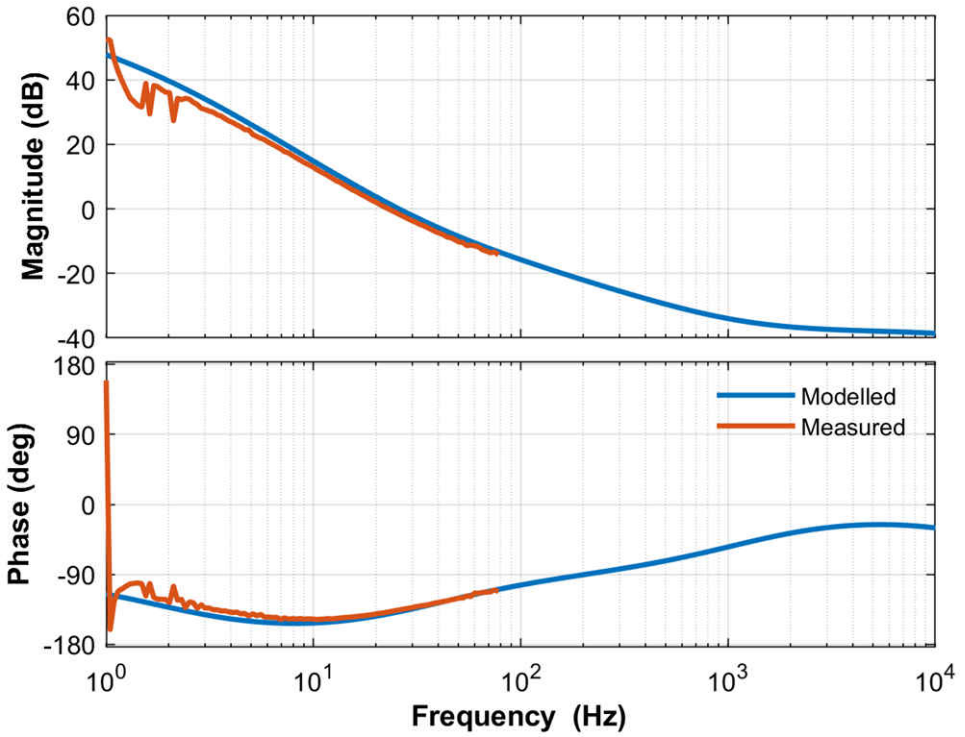


図 2-52. Voltage Loop, Open-Loop Frequency Response Modelled vs Measured

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

This section details the hardware and explains the different sections on the board and how to set them up for the experiments as outlined in this design guide.

3.1.1 Hardware

3.1.1.1 Test Hardware Required

The DUT in this design is set up and is operated in several pieces:

- One TIDA-01606 power board
- Three TIDA-01606 gate driver cards
- One TIDA-01606 ISOHVCARD
- TMS320F28379D Control Card
- Mini USB cable
- One USB isolator
- Laptop or other computer

The test equipment required to power and evaluate the design is as follows:

- 24-V, 4-A bench style supply for primary board power
- For PFC Mode
  - 400 V_{L-L} capable three-phase AC source
  - > 10-kVA resistive load to be connected at the DC output
- For Inverter Mode
  - Star connected resistive load network like the 10-kW Simplex PowerStart load bank
  - 800-V, 12-A power supply for DC link input
- Four-channel, power quality analyzer
- Oscilloscope, voltage meter, and current probes

The design follows an HSEC control card concept. This design can be scaled across multiple devices from the C2000™ MCU product family with a compatible HSEC control card. The key resources used for controlling the power stage on the MCU are listed in 表 3-1.

3.1.1.2 Microcontroller Resources Used on the Design

表 3-1 details the key controller peripherals used for control of the power stage on the board and 表 3-2 lists the key connectors and functions.

表 3-1. Key Controller Peripherals Used for Control of Power Stage on Board

Pin Number	DESCRIPTION	SOFTWARE NAME
15, 31, 28	Grid Voltage Sense Phase A, B, C	TINV_VGRID_A, B, C
21, 33, 30	Inverter Side Voltage Phase A, B, C	TINV_VINV_A, B, C
25, 37, 34	Inverter Side Current Phase A	TINV_IINV_A, B, C
42	Bus Voltage Sensing	TINV_VBUS
40	Bus Voltage Mid Point Sensing	TINV_VBUS_MID
12, 14, 18, 20	Temperature A, B, C and Ambient	TINV_TEMP_A, B, C, AMB
49, 50, 58	Q1 PWM Phase A, B, C	TINV_Q1_A, B, C
51, 52, 60	Q3 PWM Phase A, B, C	TINV_Q3_A, B, C
53, 54, 62	Q2 PWM Phase A, B, C	TINV_Q2_A, B, C
99, 103, 107	SDFM Data IG A, B, C	TINV_IGRID_A, B, C
101, 105, 109	SDFM Clock IG A, B, C	
57, 75	SDFM Clock Source	
89, 87 , 85	SiC Fault Signal A, B, C (active Low)	TINV_FAULT_A, B, C
86, 88, 90, 92	Relay on A, B, C, N	TINV_RELAY_A, B, C, N
61, 63	Gate driver supply PWM	TINV_GATE_DRIVE
59	Control GPIO for FAN	TINV_FAN

表 3-1. Key Controller Peripherals Used for Control of Power Stage on Board (continued)

Pin Number	DESCRIPTION	SOFTWARE NAME
108, 110	These pins are used to see ISR nesting and so forth, on the docking station while starting firmware debug	TINV_PROFILING1,2
95	Gate driver enable	TNV_PWM_EN
81	Gate driver Reset	TINV_R

表 3-2. Key Connectors and Functions

CONNECTOR NAME	FUNCTION
J1, J2	DC+ and DC– terminals
J3, J4, J31, J32	Phases A, B, C and neutral terminals
J33	15-V auxiliary power supply
J34	Jumper for auxiliary power supply
J5, J13	HSEC control card connector slot
J23, J7, J17, J14, J20	Phase Agate driver card connector slot
J24, J15, J21, J9, J18	Phase B gate driver card connector slot
J25, J16, J22, J12, J19	Phase C gate driver card connector slot

The following lists shows the hardware changes to TIDA-01606 - REV-6.

1. The resistors R1, R5, and R47 were changed to 2-mΩ current sense resistors.
2. The current-sense resistors along with AMC1306M05 (U1, U5, and U8) is used for current sensing in this design. The current sense out phase A LEM sensor has a noise pick-up issue and therefore is not used for current sensing and running the control loop.
3. Replaced R146, R149, R152 to 33 Ω.
4. On the TIDA-01606E4-ISOHVCARD, replaced R18 to 15-k Ω and R26 to 0 Ω.

3.1.1.3 F28377D, F28379D Control-Card Settings

Certain settings on the device control card are needed to communicate over JTAG and use the isolated UART port. The settings also provide a correct ADC reference voltage. The following are the settings required on revision 1.1 of the F28379D control card.

Refer to the information sheet located inside C2000Ware at <sdk_install_path>\c2000ware\boards\controlCARDs\TMDSCNCD28379D:

1. A:SW1 on the control card must be set on both ends to ON (up) position to enable JTAG connection to the device and the UART connection for SFRA GUI. If this switch is OFF (down), one cannot use the isolated JTAG built in on the control card nor can SFRA GUI communicate to the device.
2. A:J1 is the connector for the USB cable that is used to communicate to the device from a host PC on which Code Composer Studio (CCS) runs.
3. A 3.3-V reference is desired for the control loop tuning on this design; therefore, set the appropriate jumpers to provide a 3.3-V reference externally to the on-chip ADC. For version 1.3 of the F28379D control card, this means SW3 and SW2 are moved to the end with "." that is, to the left, which puts 3.3-V VDDA as the reference for the ADC. Refer to the information sheet for more information.

3.1.2 Software

Find related software information at the following link:

3.1.2.1 Getting Started With Firmware

3.1.2.1.1 Opening the CCS project

The software of this design is available inside C2000Ware_DigitalPower_SDK and is supported inside the powerSUITE framework. To open the project:

1. Install CCS (version 10.1 or above)
2. Install C2000Ware DigitalPower SDK from the tool page
3. Open CCS, and create a new workspace

4. Inside CCS, go to View -> Resource Explorer. Under Resource Explorer, go to Software -> C2000Ware DigitalPower SDK - <version> -> development kits and select this solution; that is, **TIDA-01606/ TIDA-010039**, and click import project.

3.1.2.1.2 Digital Power SDK Software Architecture

The general structure of the project is shown in <>. Once the project is imported, the Project Explorer will appear inside CCS.

Solution-specific and device-independent files that consist of the core algorithmic code are in "<solution>.c/h".

Board-specific and device-specific files are in "<solution>_hal.c/h". This file consists of device-specific drivers to run the solution. If the user wants to use a different modulation scheme or a different device, the user is required only to make changes to these files, besides changing the device support files in the project.

The "<solution>-main.c" file consists of the main framework of the project. This file consists of calls to the board and solution file that help in creating the system framework, along with the interrupt service routines (ISRs) and slow background tasks.

For this design, <solution> is "**tinv**" which is also referred to as the module name.

The powerSUITE page can be opened by clicking on the “main.syscfg” file, listed under the Project Explorer. The powerSUITE page generates the "<solution>_settings.h" file. This file is the only C based file used in the compile of the project that is generated by the powerSUITE page. The user must not modify this file manually, as the changes will be overwritten by powerSUITE each time the project is saved. "<solution>_user_settings.h" is included by the "<solution>_settings.h"and can be used to keep any settings that are outside the scope of powerSUITE tools such as #defines for ADC mapping, GPIOs etc.

The “Kit.json” and “solution.js” files are used internally by powerSUITE and also must not be modified by the user. Any changes to these files will result in the project not functioning properly.

The solution name is also used as the module name for all the variables and defines used in the solution.

Therefore, all variables and function calls are prepended by the **TINV** name (for example, **TINV**_vSecSensed_pu). This naming convention lets the user combine different solutions while avoiding naming conflicts.

3.1.2.1.3 Interrupts and Lab Structure

The project consists of two ISRs (ISR1 and ISR2) with ISR1 being the fastest and non-nestable ISR. ISR1 is reserved for the control loop and the PWM update. ISR1 is triggered by the PRIM_LEG1_PWM_BASE → EPWM_INT_TBCTR_U_CMPC event.

ISR2 is triggered by CPU Timer INT which is initiated by an overflow on CPU timer. It is used to run housekeeping functions such as doing a running average on the currents and voltage signals to remove noise and running the slew rate function for commanded references.

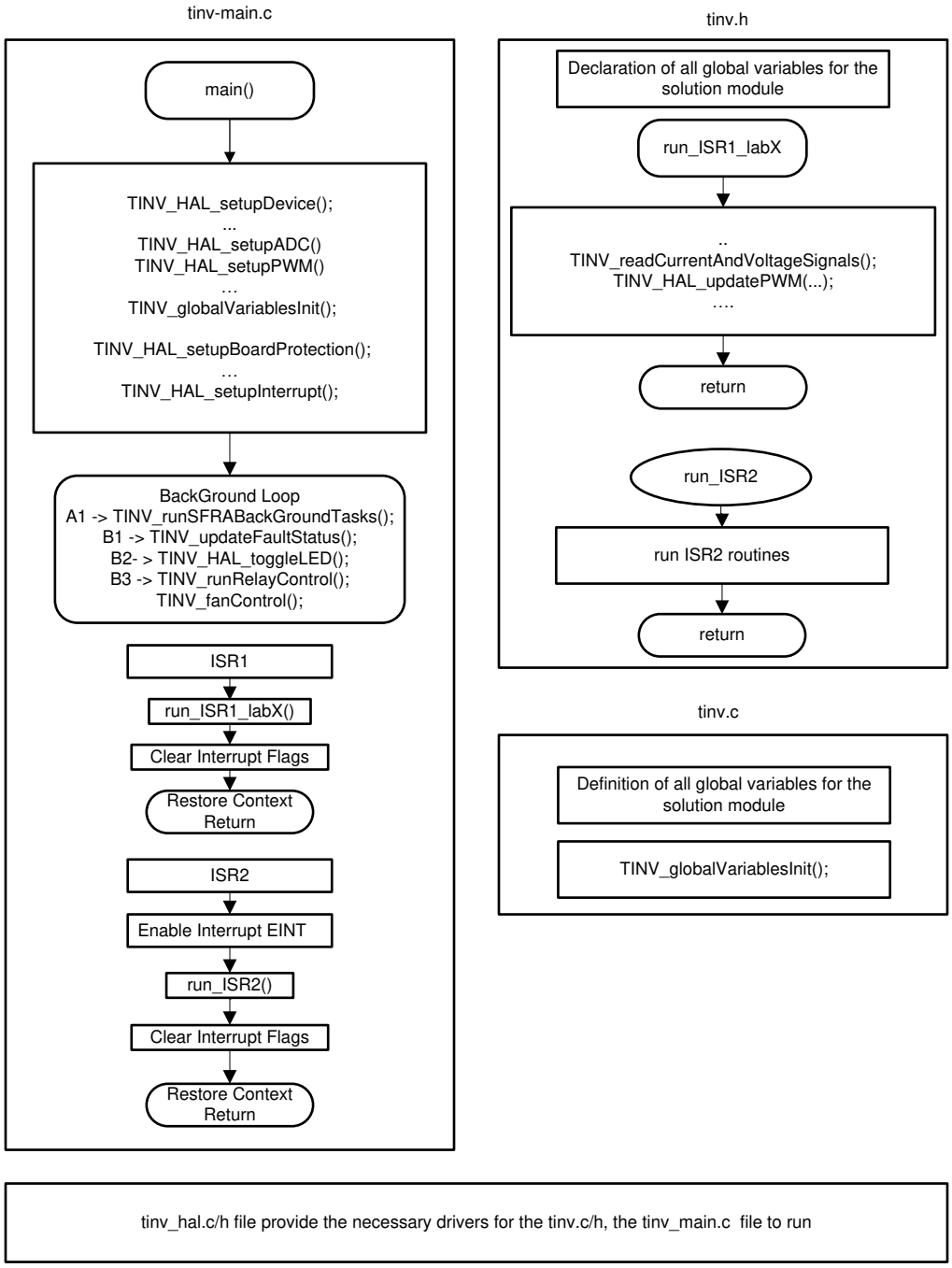


図 3-1. Software Flow Diagram

The software of this reference design is organized in seven labs, 表 3-3 lists the labs and how they have been tested. All the labs can be run on the C28x Main CPU or the *Control Law Accelerator*.

表 3-3. Overview of Labs to Test Reference Design

LAB NUMBER	DESCRIPTION	COMMENTS	TEST ENVIRONMENT
1	INV: PWM and ADC check	Test the PWM driver, ISR structure and execution rate, can be run on a control card. Unit test protection mechanisms. Test ADC mapping and reading of conversion data.	Control Card
2	INV: Open loop check	PWM Check, ADC check, Protection Check, inverter mode DC bus connected and resistive star network as load	Control Card + Power Stage Hardware
3	INV: Closed Current Loop, Resistive load connected at AC		Control Card + Power Stage Hardware
4	INV: Closed Current Loop, Grid connected test inverter mode		Control Card + Emulated power stage under Hardware In-the Loop
5	PFC: Three phase AC source , Resistive load at DC, open Loop check	1. Check if the vGridRms, iGridRms, vBus meas are correct 2. Check if PLL is locked.	Control Card + Power Stage Hardware
6	PFC: Closed Current Loop, Resistive load connected at DC, three phase AC ?		Control Card + Power Stage Hardware
7	PFC: Closed Voltage loop + Current Loop , Resistive load connected at DC, three phase AC ?		Control Card + Power Stage Hardware

3.1.2.1.4 Building, Loading and Debugging the Firmware

To build the project, right-click on the project name and click *Rebuild Project*. The project builds successfully.

To load the project, first make sure in the Project Explorer the correct target configuration file is set as Active under targetConfigs (*.ccxml file). Then, click *Run → Debug* to launch a debugging session. In case of dual-CPU devices, a window may appear for the user to select the CPU on which the debug is to be performed. In this case, select CPU1. The project will then load on the device and the CCS debug view will become active. The code will halt at the start of the main routine.

To debug the system one would monitor the variables in the watch/expressions window. To populate this window with the correct variables, click View → Scripting Console to open the scripting console dialog box. On the upper right corner of this console, click on *Open* and then browse to the “setupdebugenv_lab<Number>.js” script file located inside the project folder. This will populate the watch window with the appropriate variables needed to debug the system. Enable Continuous Refresh button on the watch window to enable continuous update of values from the controller.

Real-time emulation is a special emulation feature that allows windows within Code Composer Studio to be updated while the MCU is running. This allows graphs and watch views to updated, but also allows the user to change values in watch or memory windows, and see the effect of these changes in the system without halting the processor. To enable real-time mode click on this button on the top bar of CCS <insert image>. A message box may appear. If so, select YES to enable debug events. This will set bit 1 (DGBM bit) of status register 1 (ST1) to a “0”. DGBM is the debug enable mask bit. When the DGBM bit is set to “0”, memory and register values can be passed to the host processor for updating the debugger windows.

In different labs, sometimes the currents and voltages measured or the control variables need to be verified by viewing the data in the graph window. For this Graph window can be used which in conjunction with a piece of code that runs on the controller can show a snapshot of how the values are being sensed by the controller. The values are logged by the datalogger typically in the slower ISRs. To import the graph into the CCS view select Tools => Graph => DualTime, and click Import and point to the graph1.GraphProp file inside the project folder. Two graphs will appear in CCS. Click Continuous Refresh on these graphs. A second set of graphs can also be added by importing the graph2.GraphProp file.

CPU Loading

The main control ISR with Lab 3 and Lab 7 takes approximately 54 MIPS at 50-kHz rate when running from CPU1, that is approximately 27% of the CPU when running from 200-MHz F2837x processor. This includes the ADC drivers, abc-dq0 and dq0-abc transformation, transformation, PWM generation , two current control loops, one voltage loop, and the SFRA call.

3.1.2.2 Protection Scheme

図 3-2 explains the software functions used to setup the trip behavior on the design.

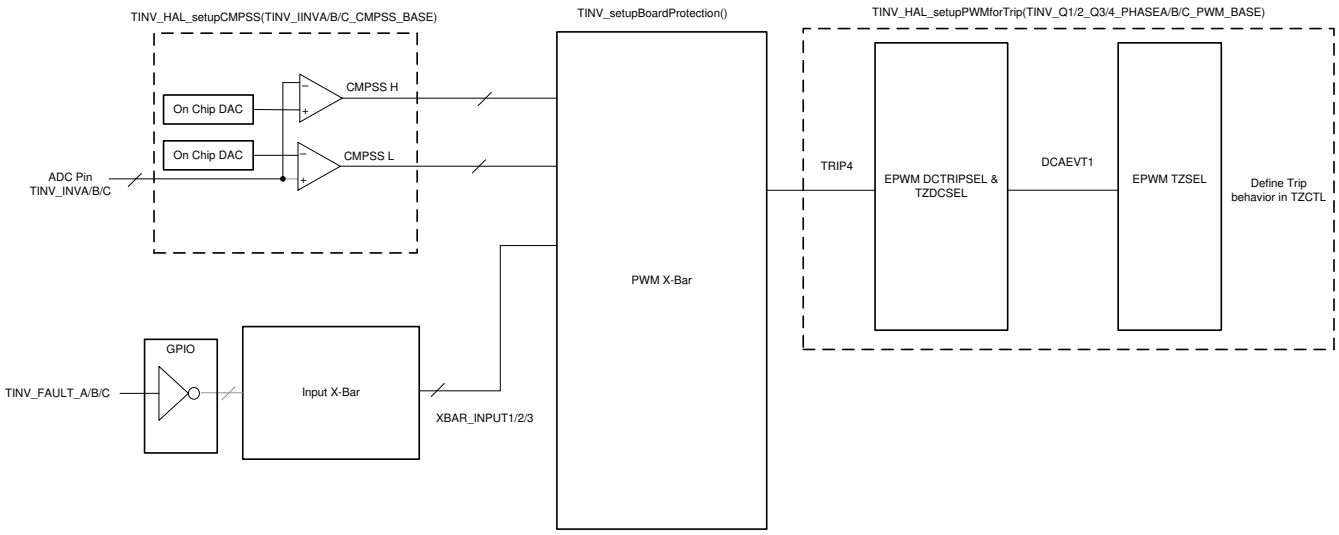


図 3-2. Software Diagram for Trip Setup

TINV_updateFaultStaus() function is called periodically in a slow background task to updating Trip Flags and also resetting the latch if needed.

If a trip event has occurred, the PWM needs Trip flags need to be cleared separately. This part is typically handled in the ISR by calling TINV_clearPWMTrips()

3.1.2.3 PWM Switching Scheme

図 3-3 is the PWM configuration used, only phase-A PWM modules time base is shown. Others are identical. EPWM11 is used for the SDFM sync on F28377.

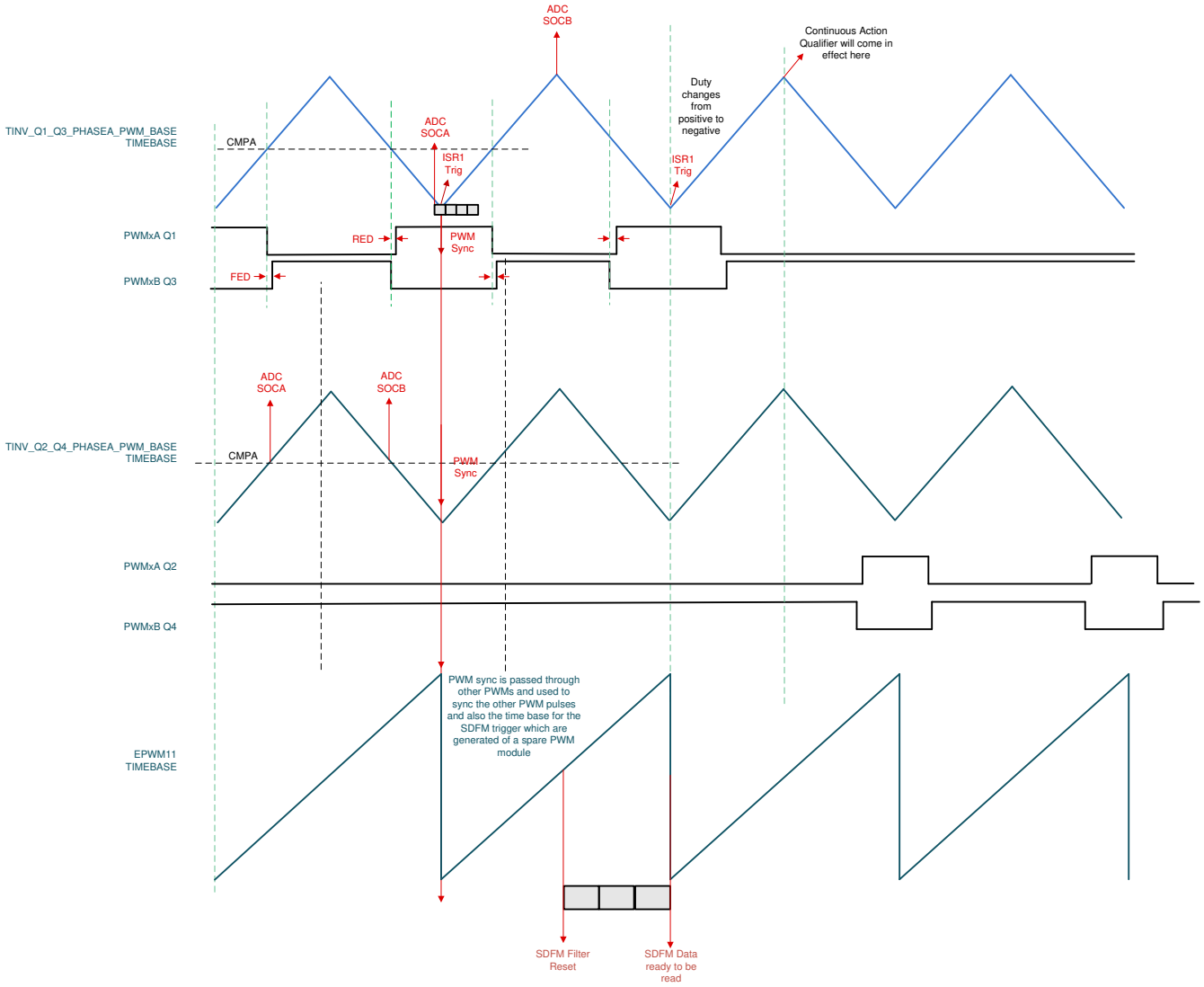


図 3-3. PWM Configuration

3.1.2.4 ADC Loading

To maintain synchronous operation all conversions are triggered as following:

TINV_Q1_Q3_A_PWM_BASE; that is, EPWM1 TBCTR_D_CMPB → EPWM1_SOCA (green), triggered every cycle,

TINV_Q1_Q3_A_PWM_BASE; that is, EPWM1 TBCTR_D_CMPB → EPWM1_SOCB (), triggered every 10th cycle,

TINV_Q2_Q4_A_PWM_BASE; that is, EPWM2 TBCTR_U_CMPB → EPWM2_SOCA, triggered every cycle

TINV_Q2_Q4_A_PWM_BASE; that is, EPWM2 TBCTR_D_CMPB → EPWM2_SOCB, triggered every cycle

TINV_Q1_Q3_A_PWM_BASE; that is, EPWM3 TBCTR_PERIOD → EPWM3_SOCA, triggered every cycle

表 3-4 shows the mapping with F2837xD on the TIDA-01606 hardware.

表 3-4. ADC Loading Architecture

	ADC-A	ADC-B	ADC-C	ADC-D
SOC0	IINV-A → ADCIN-14, CMPSS4	TEMP_A → ADC-B0	IINV-B → ADC-C4, CMPSS5	IINV-C → ADC-D2, CMPSS8
SOC1	VGRID-A → ADC-A2,	TEMP_B → ADC-B1	VGRID-B → ADC-C2	VGRID-C → ADC-D0
SOC2	VINV-A → ADC-A4	TEMP_A → ADC-B2	VINV-B → ADC-C3	VINV-C → ADC-D1
SOC3	VGRID-A → ADC-A2,	TEMP_AMB → ADC-B3	VGRID-B → ADC-C2	VBUS → ADC-D5
SOC4	VGRID-A → ADC-A2,		VGRID-B → ADC-C2	VGRID-C → ADC-D0
SOC5	VGRID-A → ADC-A2,		VGRID-B → ADC-C2	VBUS → ADC-D5
SOC6				VGRID-C → ADC-D0
SOC7				VBUS → ADC-D5
SOC8				VGRID-C → ADC-D0
SOC9				VBUS → ADC-D5

注

The ADC current reading is not used for the closed loop operation due to layout noise, instead SDFM bases sensing is employed to close the loop. Hence the grid current is used to close the current loop and the diagrams shall be interpreted accordingly for this change.

3.2 Testing and Results

3.2.1 Lab 1

This lab is meant to be run on the control card and the docking station.

Set the project to Lab 1 by changing the Lab Number in the <settings.h> file, (this will be changed by powerSUITE GUI when using powerSUITE project)

```
#define TINV_LAB 1
```

All the other options can be left at default for now in the user_settings.h file

```
#if TINV_LAB == 1
#define TINV_TEST_SETUP TINV_TEST_SETUP_RES_LOAD
#define TINV_PROTECTION TINV_PROTECTION_DISABLED
#define TINV_SFRA_TYPE TINV_SFRA_CURRENT
#define TINV_SFRA_AMPLITUDE (float32_t)TINV_SFRA_INJECTION_AMPLITUDE_LEVEL2
#define TINV_POWERFLOW_MODE TINV_INVERTER_MODE
#define TINV_DC_CHECK 0
#define TINV_SPLL_TYPE TINV_SPLL_SRF
#endif
```

図 3-4 shows the SW diagram when the code is running.

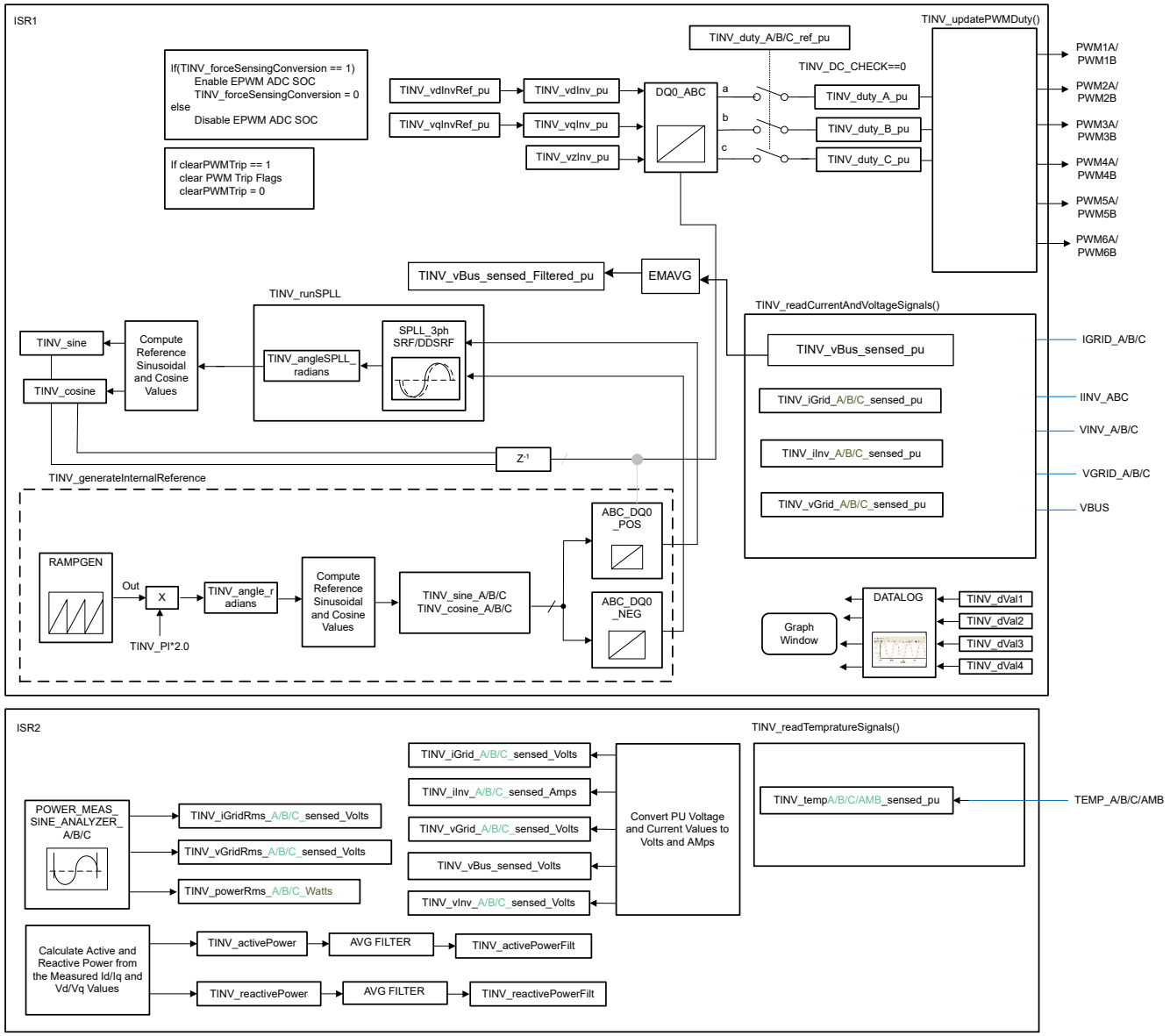


図 3-4. Lab 1 Software Diagram

3.2.2 Testing Inverter Operation

Labs 2, 3, and 4 elaborate the steps for running the power stage in the inverter mode. Lab 2 is the inverter mode of operation in open loop, Lab 3 is the inverter mode of operation with closed current loop. Lab 4 is the grid connected inverter mode of operation and this is checked only under HIL platform and not on the hardware. The high voltage (800 VDC) is applied across terminals J1 and J2. 15-V auxiliary power supply is connected to terminal J33. Three phase star connected resistive load is connected across terminals J3, J4, and J31. J32 is the neutral terminal which is left unconnected to the load.

A check for DC bus overvoltage is added to all *Inverter Labs*, Lab 1 through Lab 5, using a filtered value of the DC bus voltage. The *TINV_filterAndCheckForBusOverVoltage()* function runs from ISR1 and checks for DC bus overvoltage condition. Under OV condition this function shuts off all PWM outputs and registers the system operating state as "bus overvoltage state". Filtered DC bus voltage is calculated from instantaneous sensed DC bus voltage using the averaging function EMAVG. This is all calculated inside ISR1.

The feed-forward and decoupling function is implemented inside ISR1 and added for all Inverter Labs that use a current loop. Therefore, for the inverter mode, this is done (feed-forward and decoupling) in Lab 3 and Lab 4. For

this feed-forward and decoupling function filtered DC bus voltage is compared against a user-defined minimum bus voltage to calculate a clamped filtered DC bus voltage. This is also done inside ISR1. This clamped filtered DC bus voltage and the current controller output are finally used to implement the feed-forward and decoupling function.

For SDFM-based current sensing, overcurrent protection (OCP) is also added for all *Inverter Labs*.

3.2.2.1 Lab 2

In this lab the power stage is run in an open loop on the HW or HIL platform. 図 3-5 shows lab setup of the actual hardware.

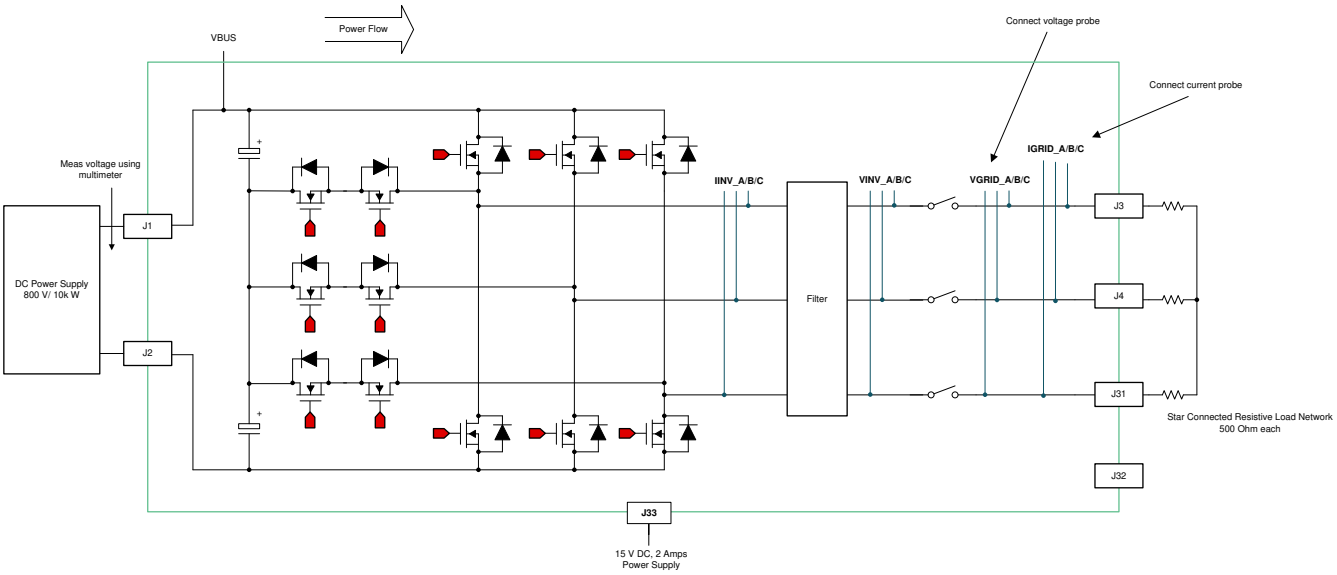


図 3-5. Inverter Mode With Resistive Load lab Setup

図 3-6 shows the SW diagram.

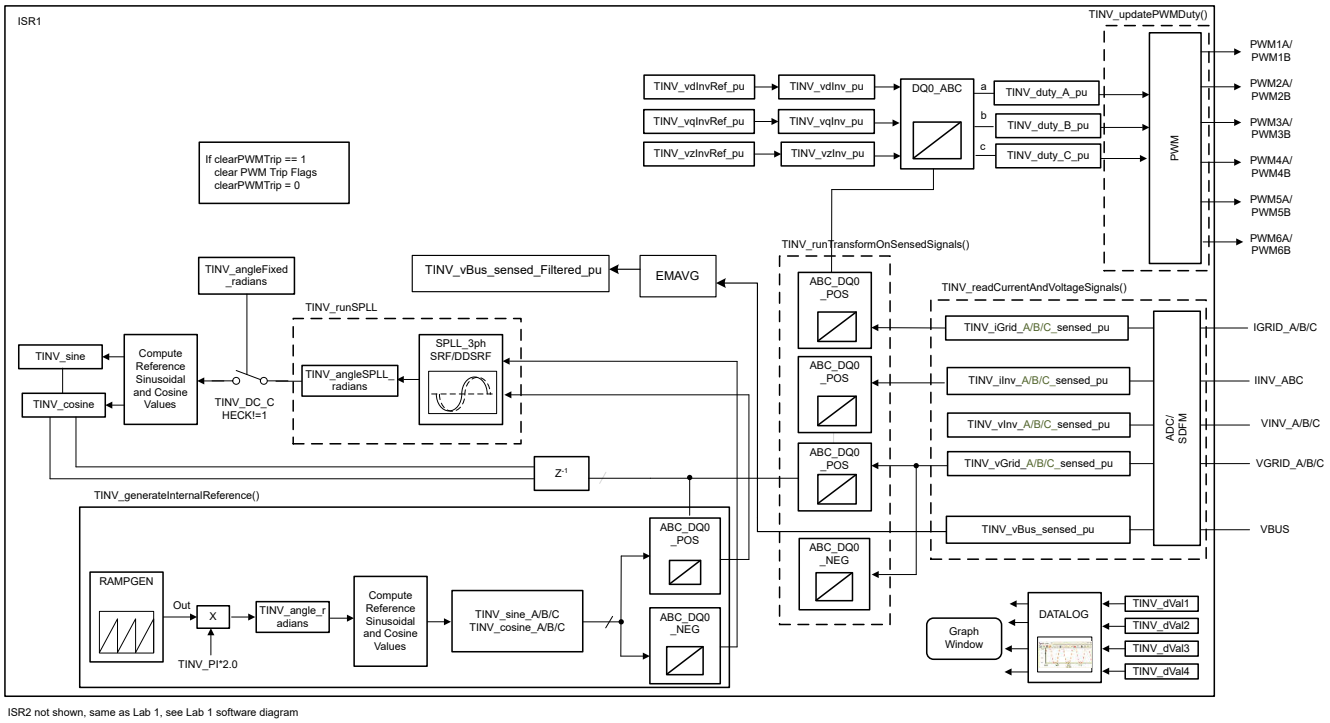


図 3-6. Lab 2 Software Diagram

Refer to the hardware test set up section for actual details of the equipment used for configuring the test. Set the project to Lab 2 by changing the Lab Number in the <settings.h> file, (this will be changed by powerSUITE GUI when using powerSUITE project).

In the user-settings.h file some additional options are available, but the following are used for the tests documented in this user guide.

```
//
// Option to use SDFM based grid sensing for the current loop
// with this option the inv current from LEM is overwritten by the grid current from SDFM
// On Revision 5 of the hardware the only option supported is the SDFM sensing
//
#define TINV_SDFM 1
#define TINV_ADC 2
#define TINV_CURRENT_LOOP_SENSE_OPTION TINV_SDFM
....
#if TINV_LAB == 2
#define TINV_TEST_SETUP TINV_TEST_SETUP_RES_LOAD
#define TINV_PROTECTION TINV_PROTECTION_ENABLED
#define TINV_SFRA_TYPE TINV_SFRA_CURRENT
#define TINV_SFRA_AMPLITUDE (float32_t)TINV_SFRA_INJECTION_AMPLITUDE_LEVEL2
#define TINV_POWERFLOW_MODE TINV_INVERTER_MODE
#define TINV_DC_CHECK 0
#define TINV_SPLL_TYPE TINV_SPLL_SRF
#endif
```

Lab 2:

In this check, the SW is run on the hardware, or the HIL platform, or both.

Build and load the code, use the lab2.js file to populate the watch variables in the CCS window.

- Turn on the relay by writing a 1 to TINV_allRelaySet. The auxiliary power supply should draw close to 530 mA.
- Set up an appropriate resistive load around 1 kΩ for the star connected load to start with, although the inverter mode can started at no load as well.
- Slowly ramp the DC bus voltage 'Vbus' to 800 V.
- Set the TINV_clearPWMTrip = 1, to clear the PWM trip signal. Now the switching action begins and sinusoidal voltages start appearing at the output. At this point the auxiliary power supply should draw close to 570 mA.
- TINV_vdInvRef_pu (default value is 0.835) is the modulation index that can be used to vary the AC output of the inverter in open-loop fashion.
- Verify the sensed voltage and current measurement data in the graph window before proceeding to close the current loop in Lab 3. 図 3-7 is the graph window for sensed grid side current by using SDFM module of C2000. The scale is shown in per unit (pu).

```
#ifndef __TMS320C28XX_CLA__
TINV_dVal1 = TINV_iGrid_A_sensed_pu;
TINV_dVal2 = TINV_iGrid_B_sensed_pu;
TINV_dVal3 = TINV_iGrid_C_sensed_pu;
TINV_dVal4 = TINV_rgen.out;
DLOG_4CH_run(&TINV_dLog1);
#endif
```

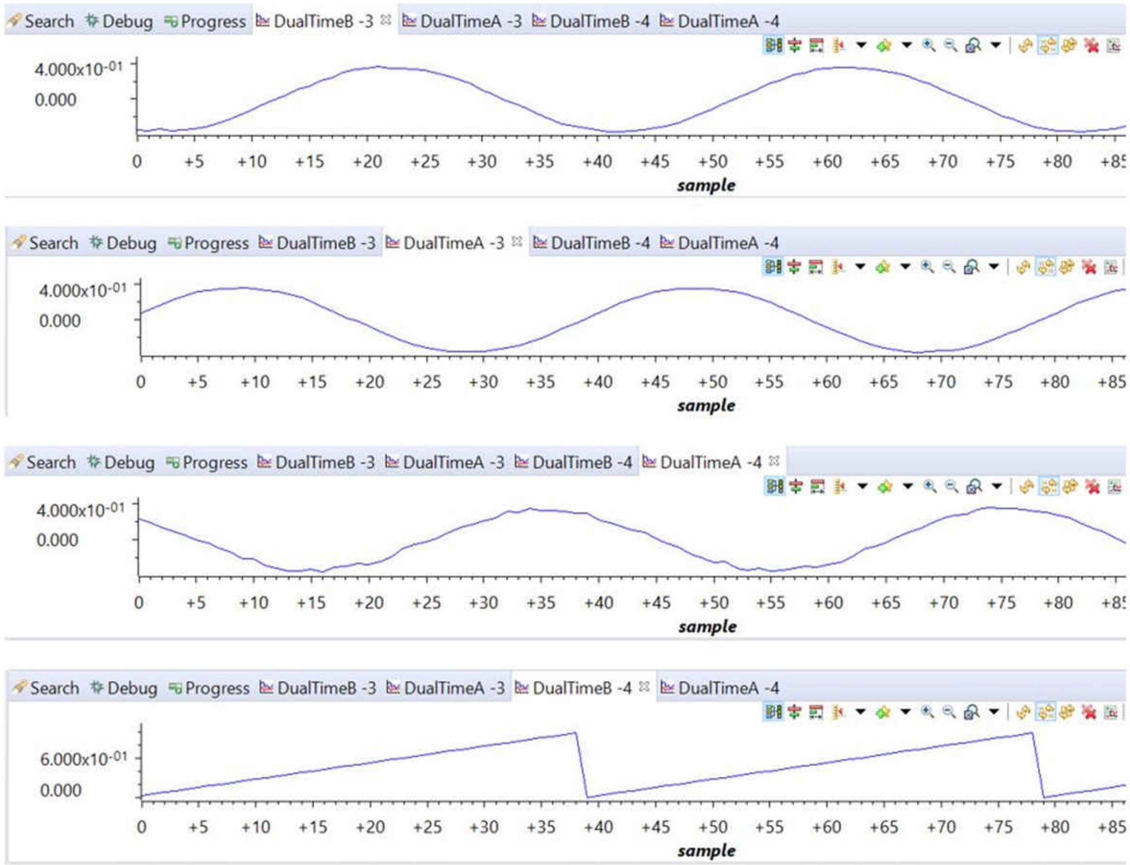


図 3-7. Sensed Grid Currents

図 3-8 shows the three grid voltages monitored from the CCS graph window. The scale is shown in per unit (pu).

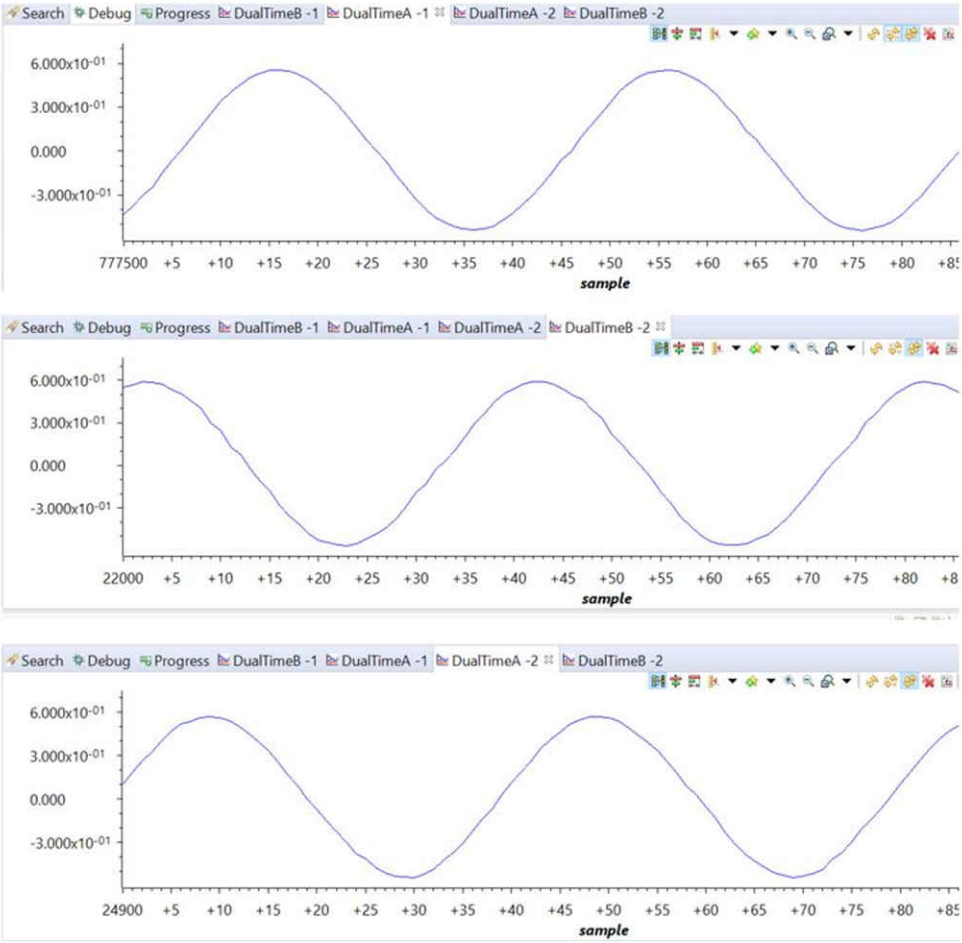


図 3-8. Sensed Grid Voltage

図 3-9 shows the captured voltage and current waveform of inverter operating in open loop at 230 VAC and 1.7 kW. Scope signals: Channel 1 - DC link voltage (light green), Channel 2 - AC voltage (blue), Channel 3 - AC current (dark green).

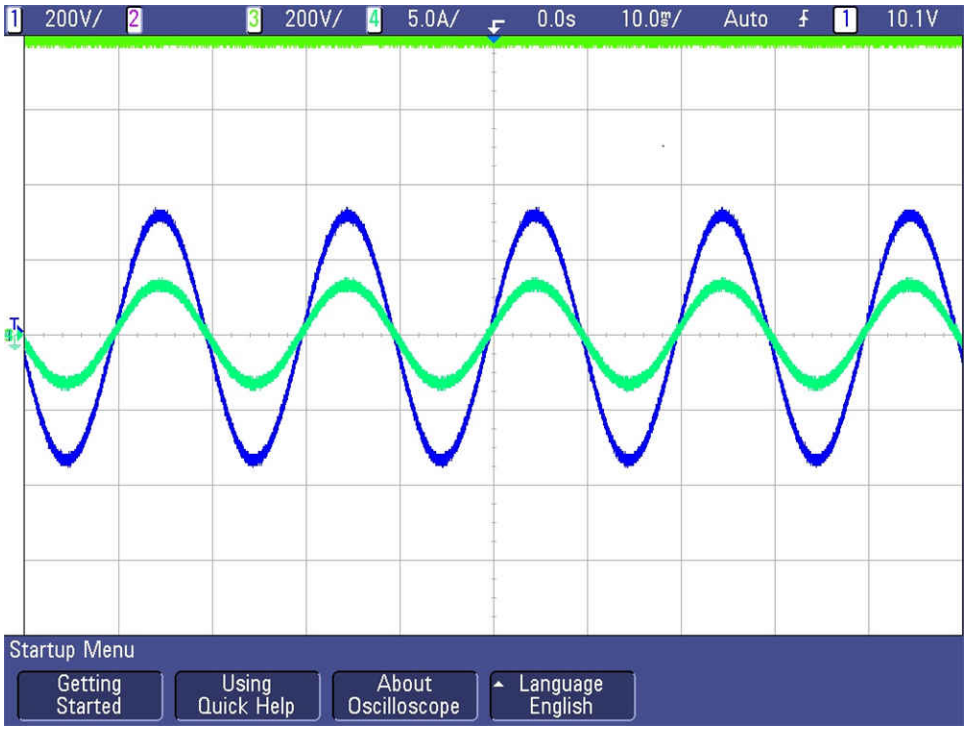


図 3-9. Open Loop Inverter Voltage and Current Waveform

3.2.2.2 Lab 3

In this lab the power stage is run in an closed loop on the real HW or HIL platform. 図 3-10 shows the SW diagram.

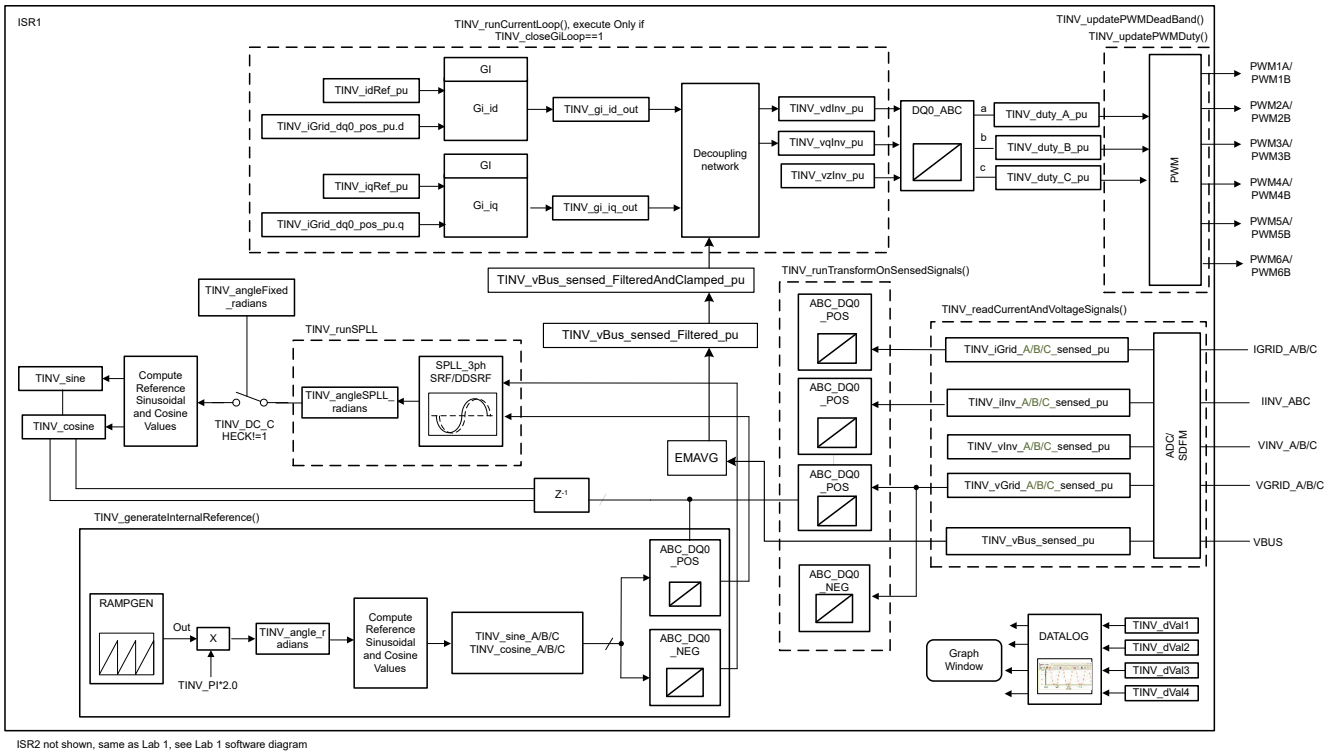


図 3-10. Lab 3 Software Diagram

Set the project to Lab 3 by changing the Lab Number in the <settings.h> file, (this will be changed by powerSUITE GUI when using powerSUITE project).

In the user settings.h file some additional options are available, but the following are used for the tests documented in this user guide.

```
#if TINV_LAB == 3
#define TINV_TEST_SETUP TINV_TEST_SETUP_RES_LOAD
#define TINV_PROTECTION TINV_PROTECTION_ENABLED
#define TINV_SFRA_TYPE TINV_SFRA_CURRENT
#define TINV_SFRA_AMPLITUDE (float32_t)TINV_SFRA_INJECTION_AMPLITUDE_LEVEL2
#define TINV_POWERFLOW_MODE TINV_INVERTER_MODE
#define TINV_DC_CHECK 0
#define TINV_SPLL_TYPE TINV_SPLL_DDSRF
#endif
```

Lab 3:

In this check, the SW is run on the hardware, or the HIL platform, or both.

Refer to the hardware test set up section for actual details of the equipment used for configuring the test. At this time, do not supply any HV power to the board.

- First launch the main.cfg and select lab3 in the project options. The compensator style (PI compensator) and the tuning loop (current loop) will be automatically populated. Now click run compensation designer icon and compensation designer tool will launch, with the model of the current loop plant with parameters specified on the powerSUITE page.
- The current compensator coefficients used for running the control loop are shown in the following code. The user can modify these coefficients to meet the necessary loop bandwidth and phase margin. The ideal coefficients with resistive load are slightly different than the one used for grid connection because the grid impedance is very low. The compensator design transfer function and response will be as shown in 図 3-11.

```
#define TINV_GI_PI_KP ((float32_t)0.3))
#define TINV_GI_PI_KI ((float32_t)0.0120860479))
```

- Once satisfied with the proportional and integral gain values, click on Save COMP. This will save the compensator values into the project. Close the Compensation Designer, and return to the powerSUITE page
- Build and load the code, use the lab3.js file to populate the watch variables in the CCS window.
- Turn on the relay by writing a 1 to TINV_allRelaySet. The auxiliary power supply should draw close to 530 mA
- Set up an appropriate resistive load around 200 Ω to start with although the inverter mode can started at no load as well.
- Slowly ramp the DC bus voltage 'Vbus' to 800 V.
- Set the TINV_clearPWMTrip = 1, to clear the PWM trip signal. Now the switching action begins and sinusoidal voltages start appearing at the output. At this point the auxiliary power supply should draw close to 570 mA.
- As soon as TINV_clearPWMTrip is set, the *TINV_closeGiLoop* variable is enabled and closed current loop action begins.
- TINV_idRef_pu is the current command reference and by default it is populated to a value of 0.005 pu at start-up. Slowly vary this to increase the output AC voltage and observe measured current tracks the commanded value.
- Verify TINV_idRef_pu and TINV_iInv_dq0_pos.d data in the watch window at low before proceeding to close the current loop in Lab 3.
- Slowly increase id_ref to 0.36 pu at 800-V input voltage to improve output power to 3.7 kW, approximately 1.25 kW per phase. 図 3-11 shows the power analyzer and scope waveform.

- 図 3-11 shows the captured voltage and current waveform of inverter operating in closed current loop at 3.7 kW. Scope signals: Channel 1 - DC link voltage (blue), Channel 2 - AC voltage (light green), Channel 3 - AC current (dark green)

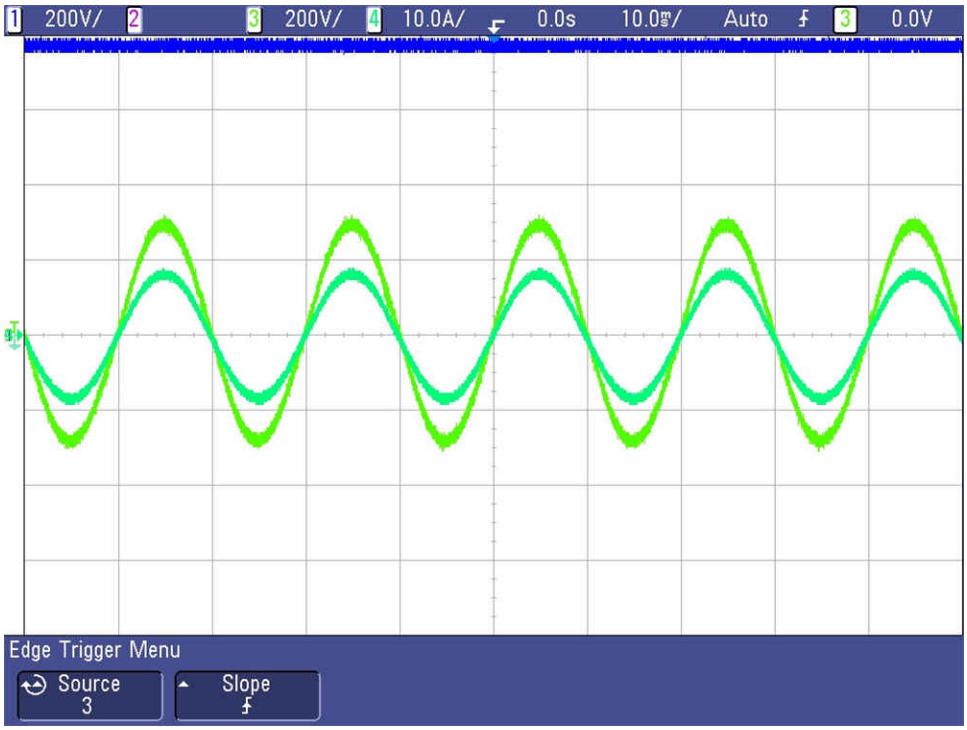


図 3-11. Inverter Closed-Loop Operation

- SFRA is integrated in the software of this lab to verify the designed compensator provides enough gain and phase margin by measuring on hardware. To run the SFRA keep the project running, and from the cfg page, click on the SFRA icon. SFRA GUI will pop up.
- Select the options for the device on the SFRA GUI. For example, for F28377D select floating point. Click on *Setup Connection*. On the pop-up window uncheck the boot on connect option, and select an appropriate COM port. Click *OK*. Return to the SFRA GUI, and click *Connect*.
- The SFRA GUI will connect to the device. A SFRA sweep can now be started by clicking Start Sweep. The complete SFRA sweep will take a few minutes to finish. Activity can be monitored by seeing the progress bar on the SFRA GUI and also checking the flashing of blue LED on the back on the control card that indicates UART activity. Once complete, a graph with the open loop plot will appear, as in 図 3-12. This verifies that the designed compensator is indeed stable. The SFRA for plant and open loop with the above coefficients is shown in 図 3-12 and 図 3-13, respectively. This action verifies the current compensator design. To bring the system to a safe stop, bring the input DC voltage down to zero.
- The above set of compensation designer coefficients are robust and stable. In case the tracking performance of current against the commanded reference and appears to oscillate, the user can use the following set of coefficients. To change the coefficients, compensation designer tool will have to be relaunched from the power suite page.

```
#define TINV_GI_PI_KP ((float32_t)0.144))
#define TINV_GI_PI_KI ((float32_t)0.112))
```

- Once satisfied with the proportional and integral gain values, click on *Save COMP*. This will save the compensator values into the project.

- The SFRA response of plant and open loop for the inverter in current mode with the new set of coefficients are shown in 図 3-12 and 図 3-13, respectively.

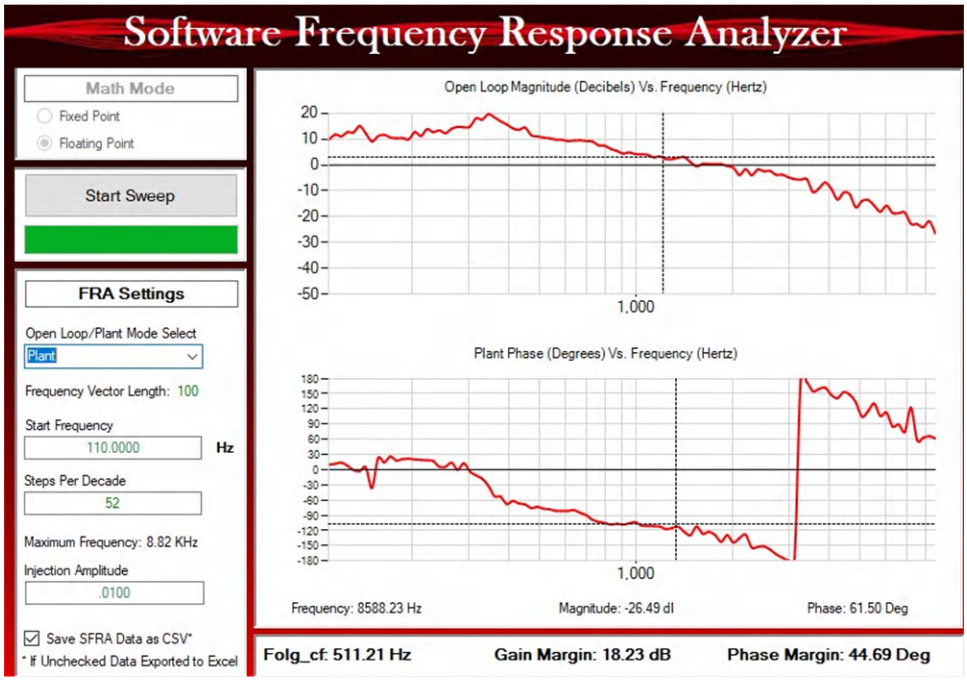


図 3-12. Inverter SFRA Plant Response for Current Loop

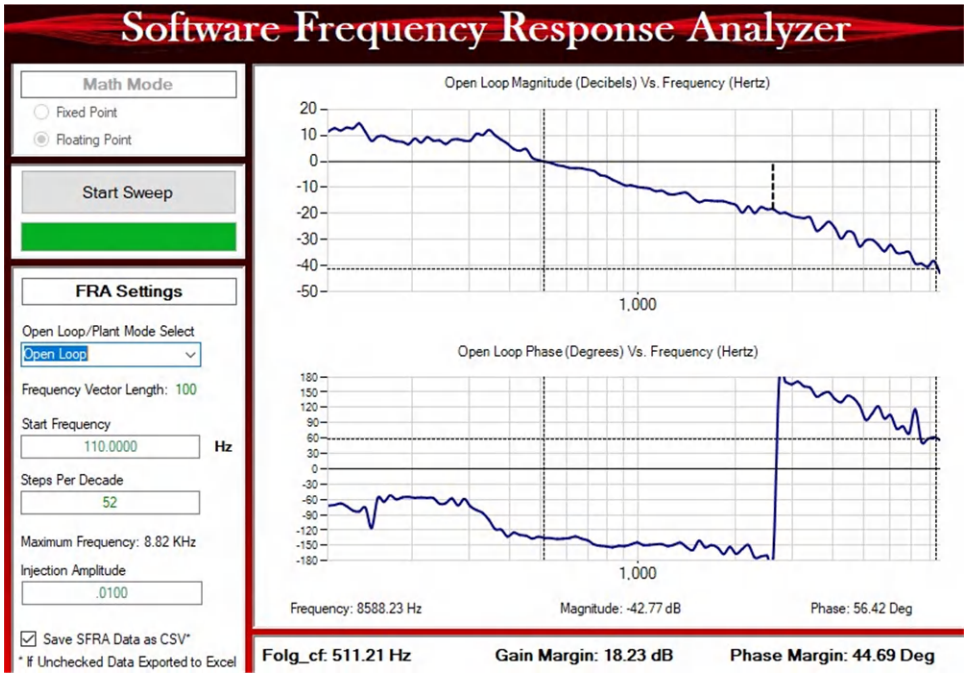


図 3-13. Inverter SFRA Loop Response for Current Loop

3.2.2.3 Lab 4

In this lab the power stage is run in a closed loop with grid connection on HIL platform. 図 3-14 shows the SW diagram.

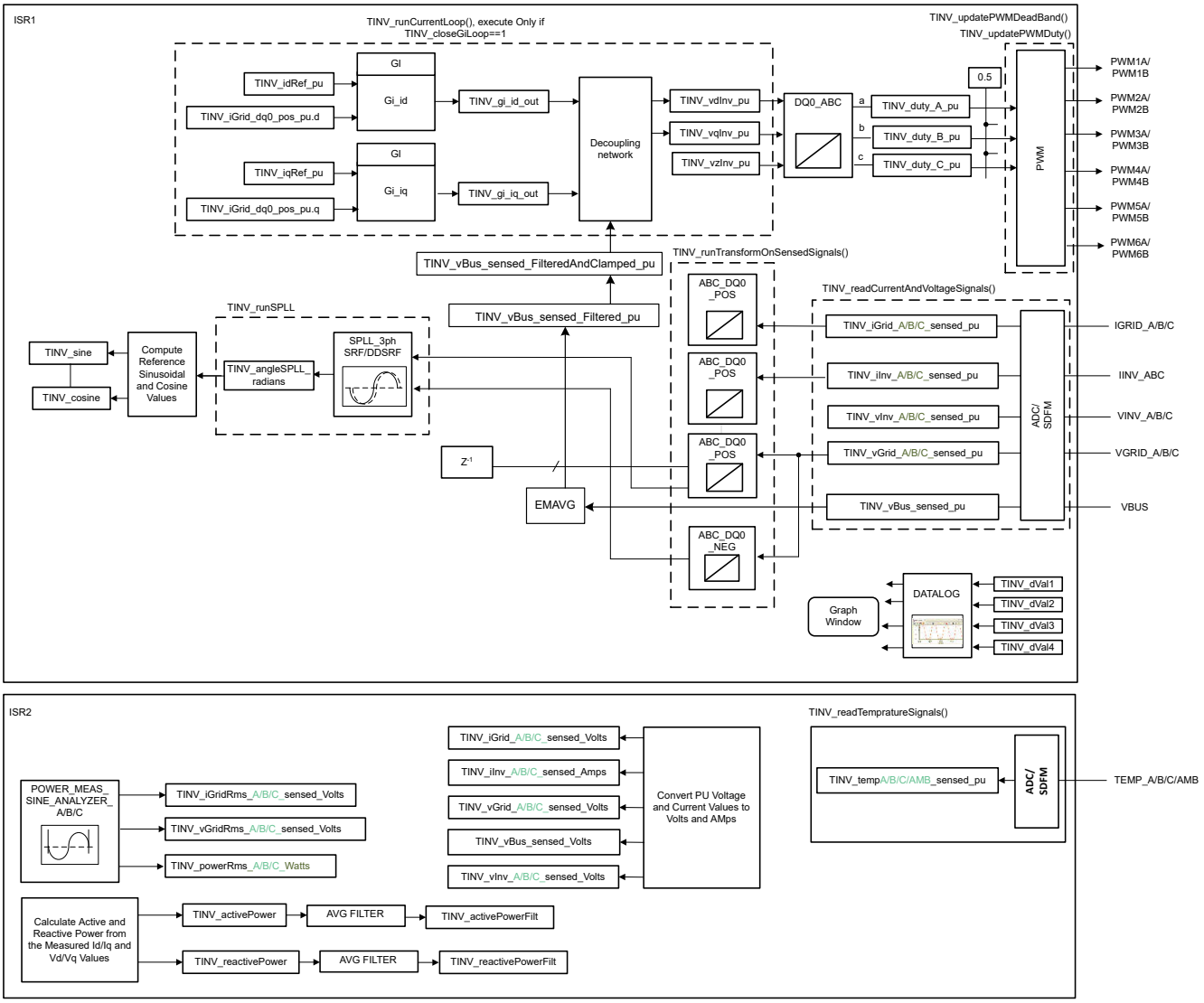


図 3-14. Lab 4 Software Diagram

注

This lab is only verified under HIL setup

Set the project to Lab 4 by changing the Lab Number in the <settings.h> file, (this will be changed by powerSUITE GUI when using powerSUITE project).

In the user settings.h file some additional options are available, but the following are used for the tests documented in this user guide.

```
#if TINV_LAB == 4
#define TINV_TEST_SETUP TINV_TEST_SETUP_GRID_CONNECTED
#define TINV_PROTECTION TINV_PROTECTION_ENABLED
#define TINV_SFRA_TYPE TINV_SFRA_CURRENT
#define TINV_SFRA_AMPLITUDE (float32_t)TINV_SFRA_INJECTION_AMPLITUDE_LEVEL2
#define TINV_POWERFLOW_MODE TINV_INVERTER_MODE
#define TINV_DC_CHECK 0
```

```
#define TINV_SPLL_TYPE TINV_SPLL_SRF
#endif
```

Lab 4

In this check, the SW is run on the HIL platform.

Build and load the code, use the lab4.js file to populate the watch variables in the CCS window.

- Slowly ramp the DC bus voltage 'Vbus' to 800 V
- Enter "1" on TINV_startPowerStage variable and ramp the AC voltage of the grid to 230Vrms, L-N; that is, 400 VL-L
- Set up an appropriate grid connection and turn on the relay by writing a 1 to TINV_allRelaySet as soon as voltage reaches 230 V_{RMS} as the inrush current limit resistors might get heated and burn out. The current should now be fed into the grid.
- Slowly increase this TINV_idRef_pu variable to be 0.6 pu, at this point the per phase power will be approximately 1.9 kW

Measure the current loop bandwidth using SFRA. 図 3-15 and 図 3-16 show plant response and loop response of inverter operating in current mode measured on the HIL platform.

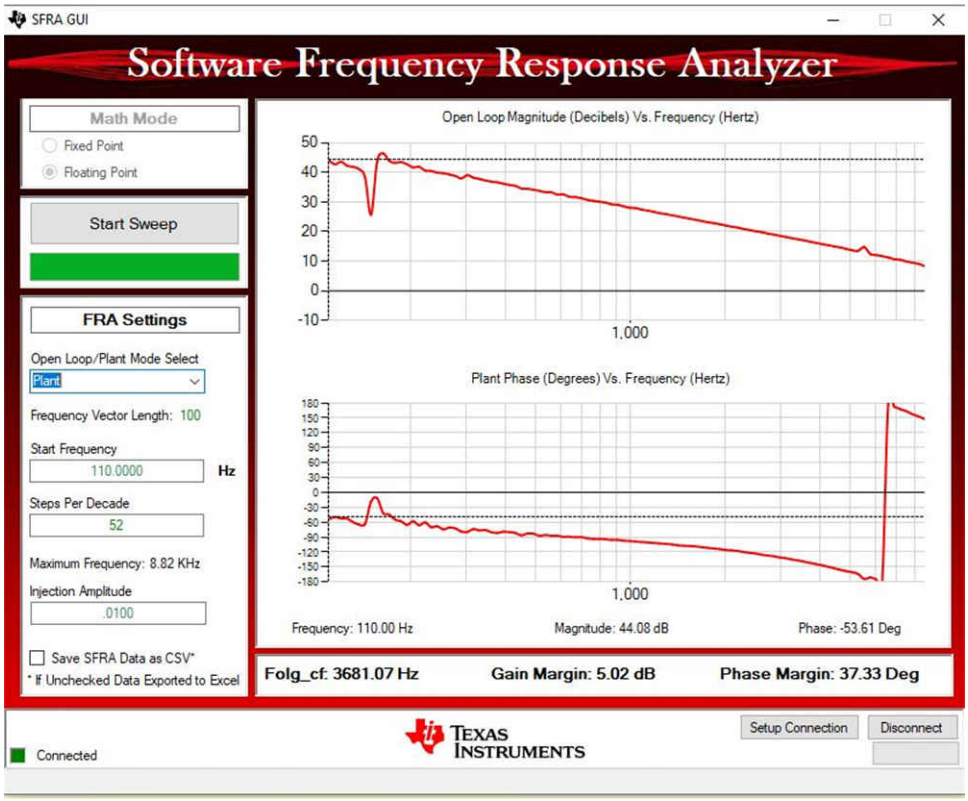


図 3-15. Inverter SFRA Plant Response Measured on HIL

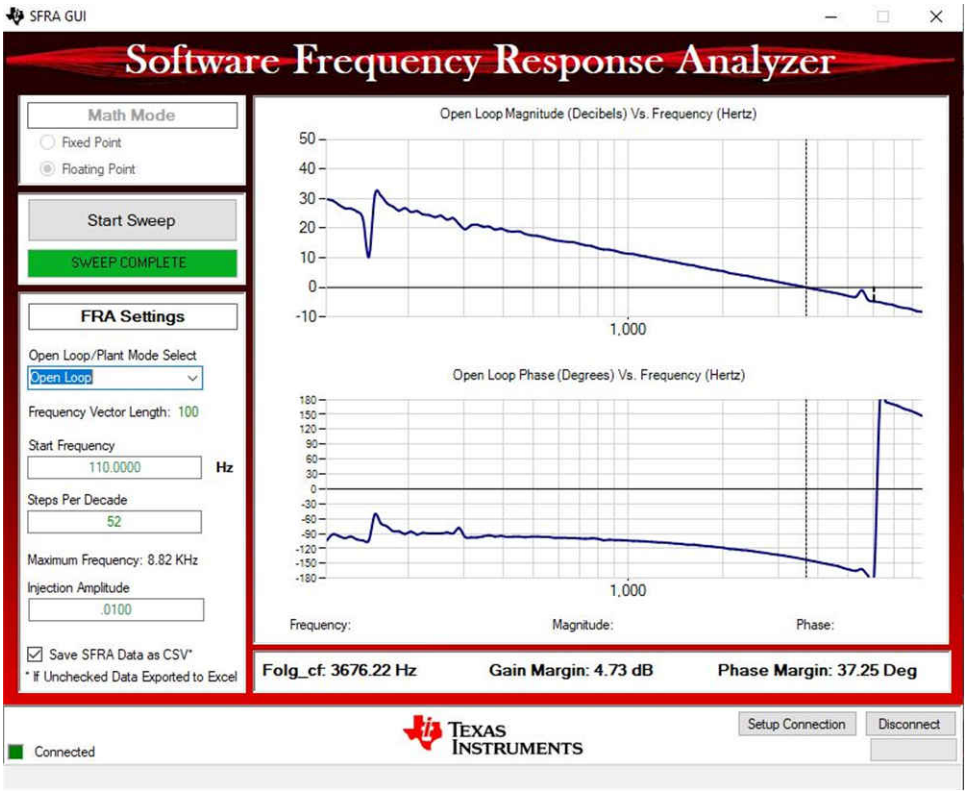


図 3-16. Inverter SFRA Loop Response Measured on HIL

3.2.3 Testing PFC Operation

Labs 5, 6, and 7 elaborate the steps for running the power stage in the PFC mode. Lab 5 is the PFC mode of operation in open loop, Lab 6 is the PFC mode of operation with closed current loop. Lab 7 is the PFC mode of operation in closed voltage and current loop and this will be checked both on the HIL platform and actual hardware.

A check for DC bus overvoltage is added to all *PFC Labs*, Lab 5 through Lab 7, using a filtered value of the DC bus voltage. The *TINV_filterAndCheckForBusOverVoltage()* function runs from ISR1 and checks for DC bus overvoltage condition. Under OV condition this function shuts off all PWM outputs and registers the system operating state as “bus over-voltage state”. Filtered DC bus voltage is calculated from instantaneous sensed DC bus voltage using the averaging function EMAVG. This is all calculated inside ISR1.

The feed-forward and decoupling function is implemented inside ISR1 and added for all *PFC Labs* that use a current loop. Therefore, for the PFC mode, this is done in Lab 6 and Lab 7. For this feed-forward and decoupling function filtered DC bus voltage is compared against a user-defined minimum bus voltage to calculate a clamped filtered DC bus voltage. This is also done inside ISR1. This clamped filtered DC bus voltage and the current controller output are finally used to implement the feed-forward and decoupling function.

For SDFM-based current sensing, overcurrent protection (OCP) is also added for all PFC labs.

図 3-17 shows the hardware setup, the DC terminals J1 and J2 are connected to a resistive load. A 15-V auxiliary power supply is connected to terminal J33. Three phase AC source is connected across terminals J3, J4, and J31 (A, B, and C). J32 is the neutral terminal which is left unconnected to the source. See the hardware test set up section for actual details of the equipment used for configuring the test.

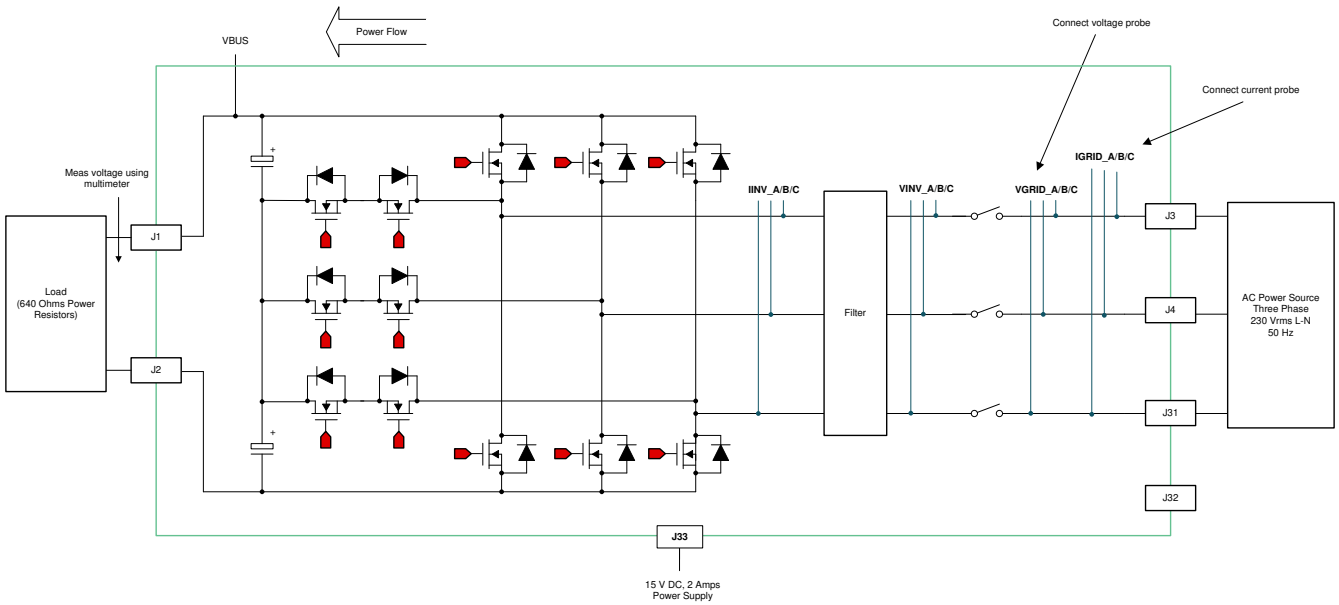


図 3-17. PFC Mode Test Setup

3.2.3.1 Lab 5

This is the first PFC lab. In this lab sensing is checked and no switching action occurs until clearPWMTrip is set to 1.

The hardware setup for the PFC mode is explained in 図 3-17. TI recommends starting the PFC at low voltage like 30 V_{RMS} and connecting a 2-kΩ resistor.

Set the project to Lab 5 by changing the Lab Number in the <settings.h> file, (this will be changed by powerSUITE GUI when using powerSUITE project).

Under this condition, the converter operates as a rectifier and rectified current can be observed being drawn without any power factor correction. SPLL locking can also be safely verified in this build.

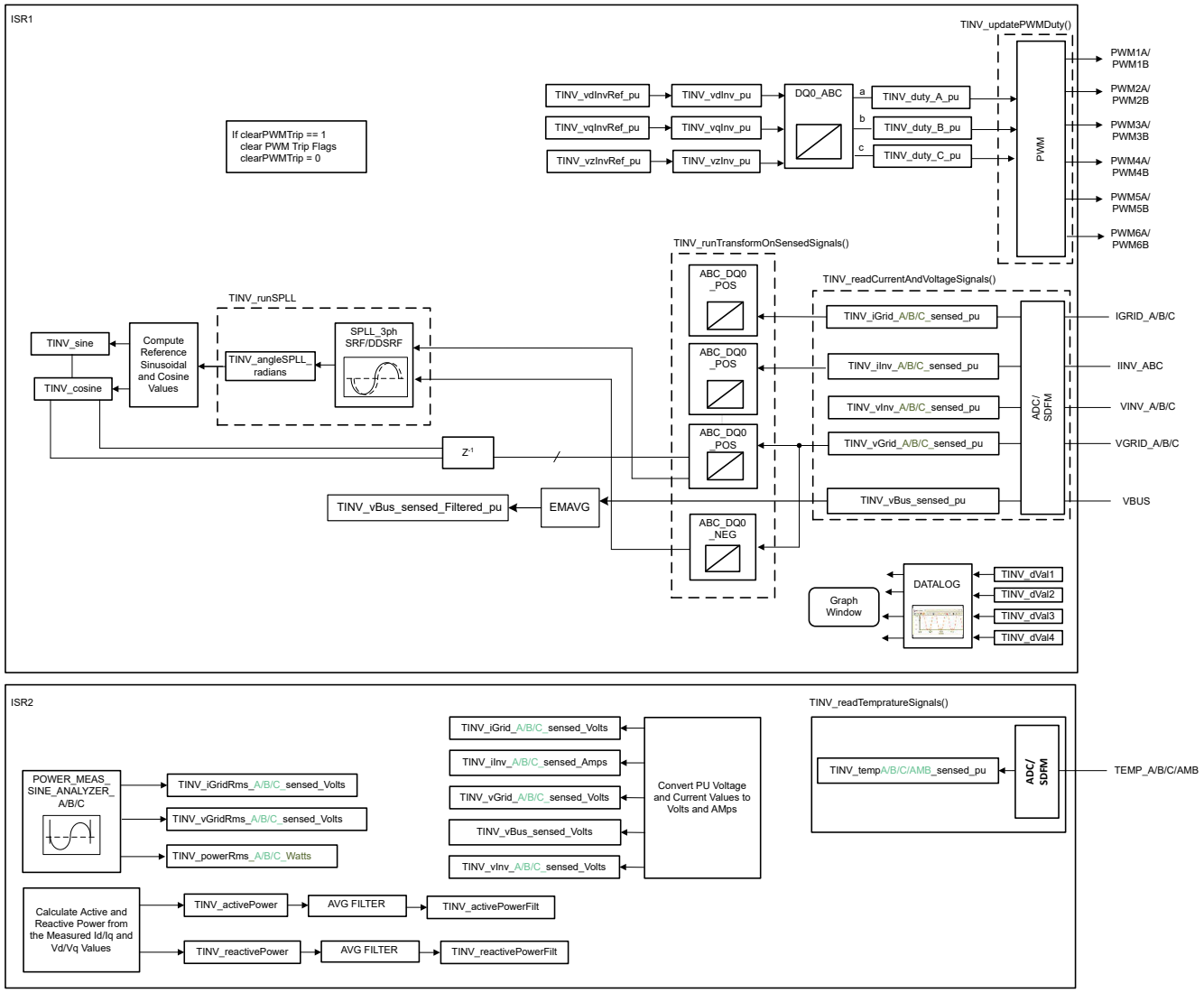


図 3-18. Lab 5 Software Diagram

Hence, the following variables are put on the datalogger:

```
TINV_dVal1 = TINV_vGrid_A_sensed_pu;
TINV_dVal2 = TINV_angleSPLL_radians / (float32_t)(2.0f * TINV_PI);
TINV_dVal3 = TINV_vGrid_A_sensed_pu;
TINV_dVal4 = TINV_iInv_A_sensed_pu;
DLOG_4CH_run(&TINV_dLog1);
```

Make sure the Grid frequency is specified correctly, the grid frequency can be changed through the sysconfig page for powerSUITE based projects. If not powerSUITE based project one can modify the tinv_settings.h file.

```
#define TINV_AC_FREQ_HZ ((float32_t)50)
```

Build and load the code, use the lab5.js file to populate the watch variables in the CCS window.

PLL lock can be checked by plotting the buffers, use the graph1.graphprop to see the buffer through Tools→ Graph → Dual Time.

Cosine transforms are used hence the angle will be 0 when the Vgrid as its peak.

First close the relay by writing a 1 to TINV_allRelaySet

Initially, the test may be run with only 30 V_{RMS} for safety, hence safely ramp the AC supply to 30 V_{RMS} and observe the graph in the CCS debug window to confirm the PLL is locking. 図 3-19 shows low voltage phase locked loop check from watch window.

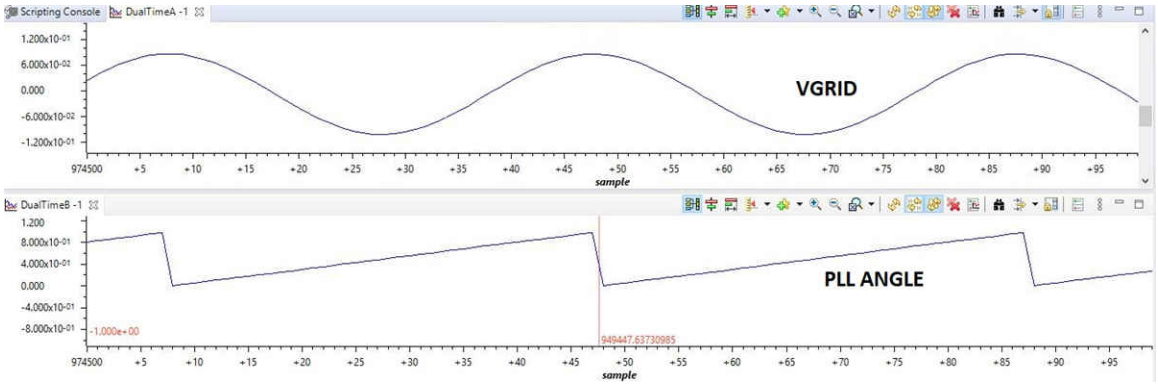


図 3-19. PLL - Grid Voltage Synchronization

If the PLL is not locking one may also issue a tinv_reset_PLL command by setting it to 1, this will initiate a task to zero out an integrated error in the module and zero all the memory elements.

Similarly, the current flowing from the grid across all phases can be checked, using the graph watch window of CCS. 図 3-20 shows the Sensed grid currents from graph windowCheck for three phase grid currents observed from the watch window.

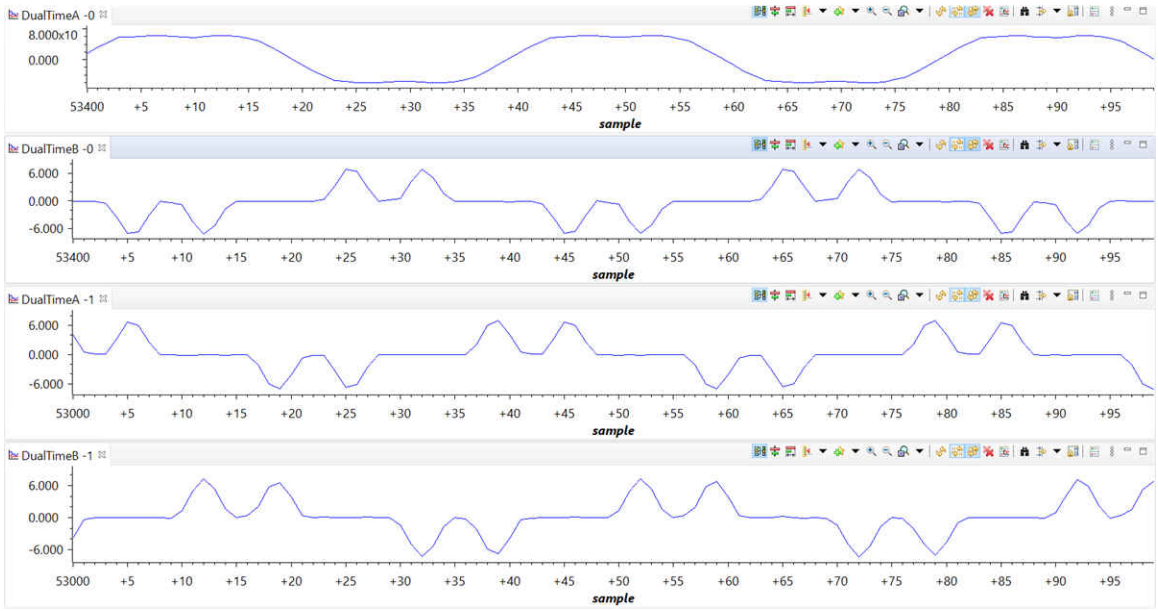


図 3-20. Sensed Grid Currents - PFC Mode

To verify boost action in Lab 5, follow the steps according to the sequence provided:

- Turn on the auxiliary power supply and set it to 15 V and then debug and run the code.
- Connect suitable load to the terminals J1 and J2. Make sure to use a high load resistance (around 2 kΩ) which otherwise can lead to high inrush currents triggering the overcurrent flag.
- Apply 30 V_{RMS} AC voltage to the three phase terminals
- Immediately turn on the relay by writing a 1 to TINV_allRelaySet. Voltage should now start to appear across the DC terminals.
- Clear the PWM trip by setting TINV_clearPwmTrip to 1 to see a slight boost in DC voltage.

Before PFC action begins, a rectified current will be drawn due to the load on the Vbus. As soon as clearPWMTrip is set to 1, a slight boost in DC voltage is seen. Note the input current has a double bump without the neutral connected to the source at light load.

注

There can be a situation in the labs for PFC (Lab 5, Lab 6, and Lab 7) where the converter operates as a rectifier and rectified current is seen being drawn without any power factor correction. But as soon as TINV_clearPwmTrip is set to 1, there is no switching action – the Gate Signals remain off.

This is because there is an overcurrent or DSAT flag (InvA_overcurrent, InvB_overcurrent,DSATA, DSATB) which is set in one of the three phases and this happens under three circumstances:

1. On closing the relays, there is an inrush current which creates an overcurrent trip in one of the three phases.
2. When TINV_clearPwmTrip to 1, the switching action causes one of the flags to be set.
3. Setting TINV_StartpowerStage to 1 for closing the current and voltage loop.

The EPWM TZFLG is set to 0X000C and under this condition no switching occurs. So make sure the load resistance is increased so that the inrush currents will not cause a trip condition and the EPWM TZFLG changes from 0x0004 to 0x0000 and switching occurs.

Once the FLG is set to 0x000C, even if we do a TINV_reset_fault_status to reset the faults, though the faults may be cleared PWM action will not be observed.

The goal is, as soon as the auxiliary power supply is started and the code debugged, all the faults – namely InvA_overcurrent, InvB_overcurrent, DSATA, DSATB; and so forth – should be set to zero so that the controller does not go into a trip state.

3.2.3.2 Lab 6

In this build level the current loop for the PFC is checked. Lab 6 is primarily meant for tuning the current loop and optimizing its performance. It is always safe to start Lab 6 at low voltage and low power as starting at higher power without a supervisory voltage loop can boost the voltage due to overcurrent events and can blow away the switches. Hence, it is very important to carefully set the TINV_idRef_pu variable so as to avoid overcurrent trips and high voltages at the DC terminals. Also the TINV_idRef_pu is defined with a negative sign for PFC mode of operation and with a positive sign for inverter mode of operation.

図 3-21 describes the software flow for running Lab 6.

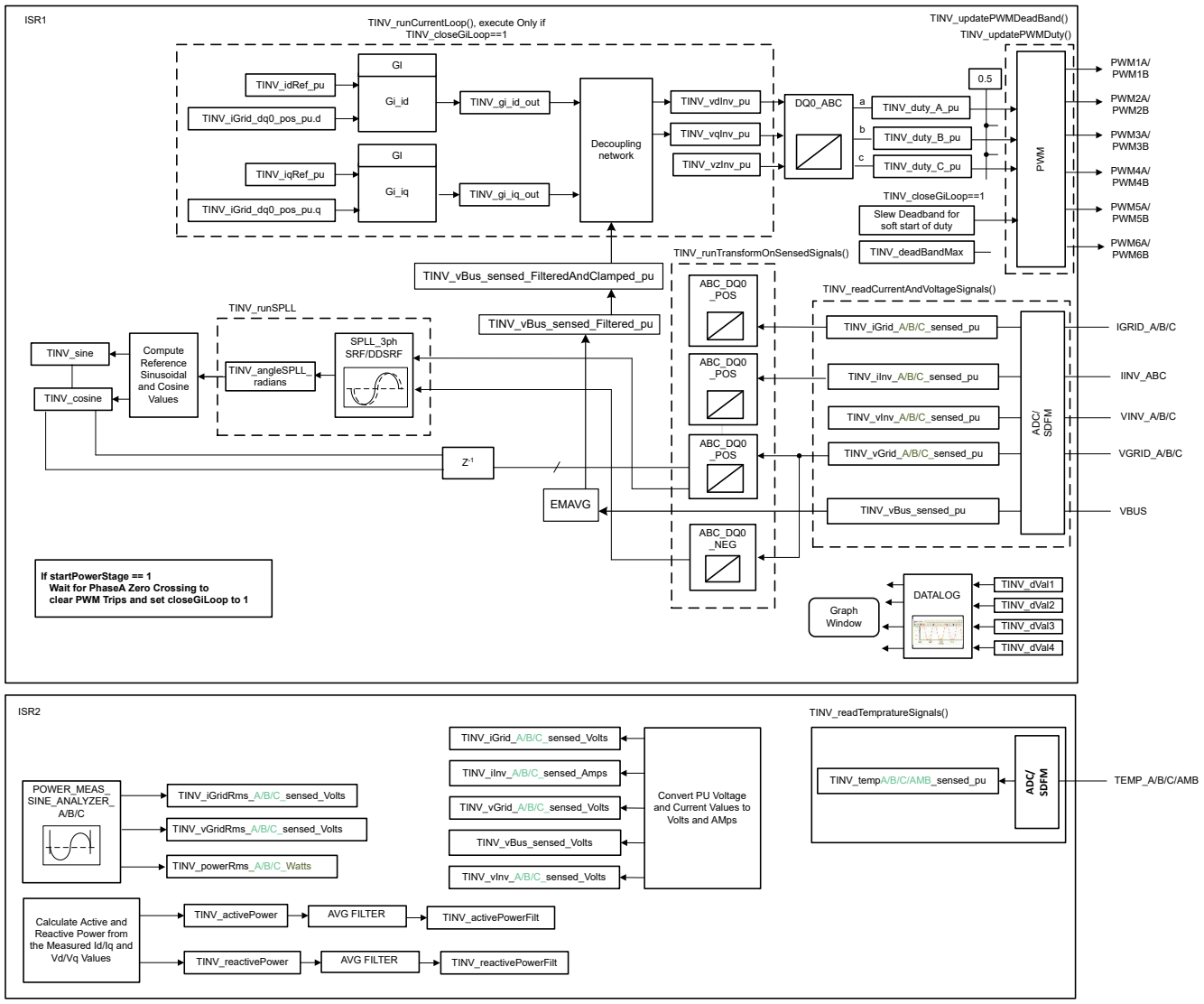


図 3-21. Lab 6 Software Diagram

Set the project to Lab 6 by changing the Lab Number in the <settings.h> file, (this will be changed by powerSUITE GUI when using powerSUITE project)

In the user settings.h file some additional options are available, but the following are used for the tests documented in this user guide.

```
#if TINV_LAB == 6
#define TINV_TEST_SETUP TINV_TEST_SETUP_RES_LOAD
#define TINV_PROTECTION TINV_PROTECTION_ENABLED
#define TINV_SFRA_TYPE TINV_SFRA_CURRENT
#define TINV_SFRA_AMPLITUDE (float32_t)TINV_SFRA_INJECTION_AMPLITUDE_LEVEL2
#define TINV_POWERFLOW_MODE TINV_RECTIFIERER_MODE
#define TINV_DC_CHECK 0
#define TINV_SPLL_TYPE TINV_SPLL_SRF
#endif
```

In this check the SW is run on the hardware, or the HIL platform, or both.

Refer to the hardware test set up section for actual details of the equipment used for configuring the test. Do not supply any HV power yet to the board.

- First launch the main.cfg and select Lab 6 in the project options. The compensator style (PI compensator) and the tuning loop (current loop) will be automatically populated. Now click run compensation designer icon

and compensation designer tool will launch, with the model of the current loop plant with parameters specified on the powerSUITE page.

- The current compensator coefficients used for running the control loop are shown in the following code. The user can modify these coefficients to meet the necessary loop bandwidth and phase margin. The ideal coefficients with resistive load are slightly different than the one used for grid connection because the grid impedance is very low. The compensator design transfer function and response are shown in 図 3-22.

```
#define TINV_GI_PI_KP ((float32_t)0.3))
#define TINV_GI_PI_KI ((float32_t)0.0120860479))
```

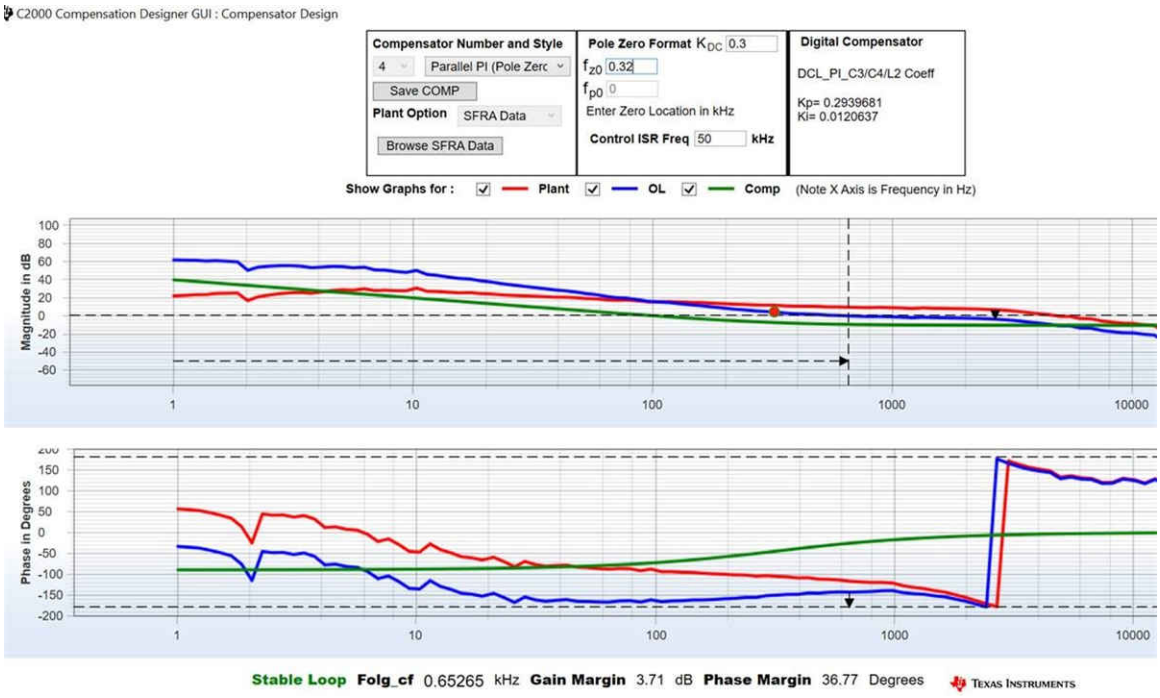


図 3-22. Compensator Design GUI - Current Loop PI Coefficients

- Once satisfied with the proportional and integral gain values, click on Save COMP. This will save the compensator values into the project. Close the Compensation Designer, and return to the powerSUITE page.
- Turn on the auxiliary power supply and set it to 15 V. Build and load the code, use the lab6.js file to populate the watch variables in the CCS window.
- Set the load resistance to a high value 3.18 kΩ.
- Set the AC input voltage to 30 V_{RMS} with appropriate current limit.
- After turning on the AC power supply, immediately turn on the relay by writing a 1 to TINV_allRelaySet. Ensure that the relay is turned on immediately (within 3-4 seconds) after turning on the ac supply.
- Set TINV_idRef_pu to –0.013 pu
- To start the PFC mode, enter "1" on TINV_startPowerStage variable, the current should now be drawn from the grid as a sinusoidal signal (with some harmonics as it is at low power) and boost action seen on the vBus. The output voltage will boost from 75 V to around 180 V as shown in 図 3-23.
- The current will become sinusoidal as the load is increased. This verifies start up of PFC at 30 V_{RMS}.
- The 図 3-23 shows PFC closed current loop start up at 30 V_{RMS}. **Scope signals**: Channel 1 - AC voltage (blue), Channel 2- DC voltage (light green), Channel 3 - AC current (dark green).

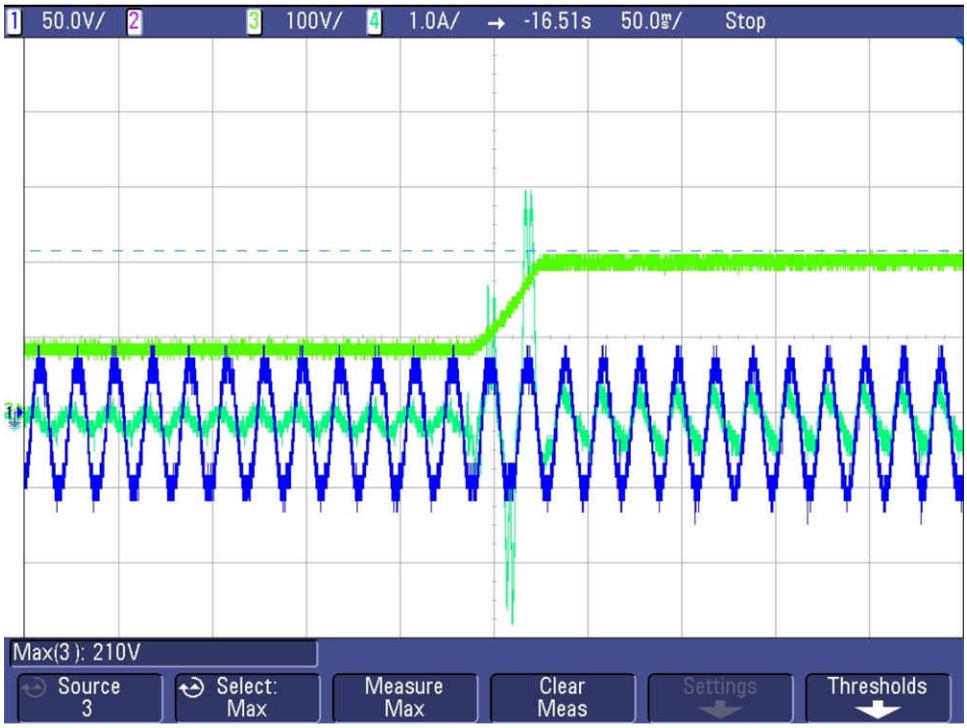


図 3-23. PFC Current Loop Start-up at 30 V_{RMS}

- Now repeat the previous steps to verify start up at 220 V_{RMS}.

  At 220 V_{RMS}, with the TINV_idRef_pu set to –0.013 pu, the bus voltage jumps from 550 V to 640 V at 155 W power as 図 3-24 shows.
- 図 3-24 shows PFC closed current loop start up at 220 V_{RMS}. **Scope signals:** Channel 1 - AC voltage (blue), Channel 2 - DC voltage (light green), Channel 3 - AC current (dark green)

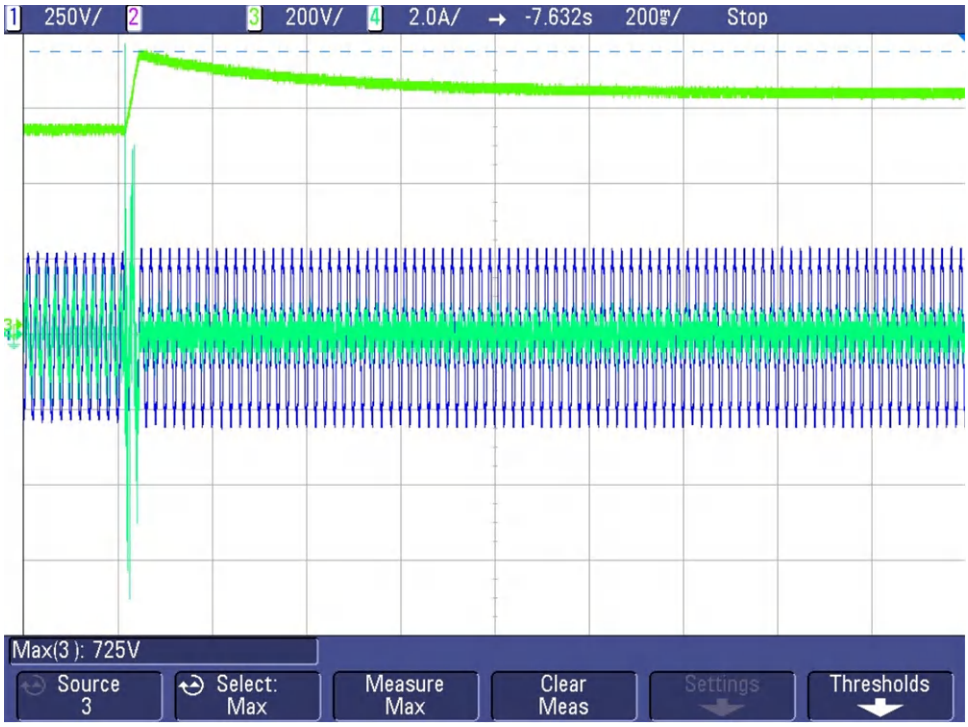


図 3-24. PFC Current Loop Start-up at 220 V_{RMS}

- As 図 3-24 shows, running this lab at higher input voltage without a supervisory voltage loop results in big overvoltage across the DC terminals. Hence it is always advisable to start this lab at low voltage and low

power as previously described for safety reasons and then slowly ramp to the desired voltage for closed current loop tuning. Starting at 230-V_{RMS} AC input voltage and boosting DC voltage to 800 V directly is shown in Lab 7.

- In case any overcurrent trip is observed which causes the PWMs to switch off, please refer the notes in Lab 5 to debug this condition.
- A soft start scheme is implemented at the start-up to ensure overcurrents are reduced at start-up. For this the duty is restricted to the PWM module by adjusting the dead band set 図 3-25 shows the PWM configuration for this setup where the dead band is set to large value and slowly reduced to the nominal value to limit the current spikes.

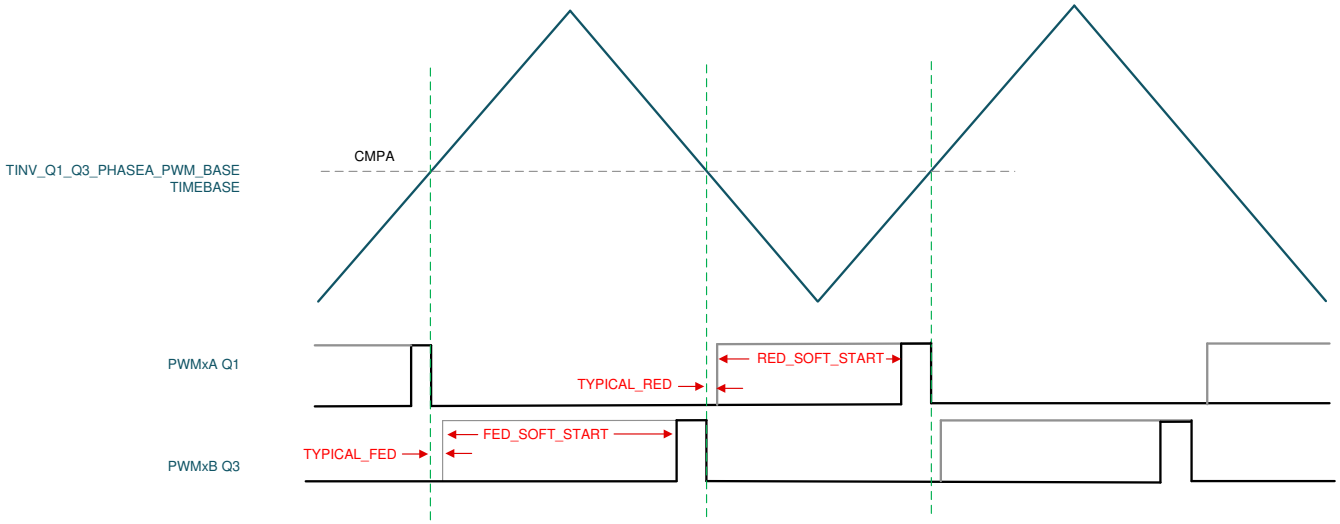


図 3-25. Dead Band Soft Start PWM Configuration

- 図 3-26 shows the effect of the start-up scheme without dead band implemented at start-up. Without soft start, a huge current spike appears which causes over current trip and the DC bus voltage also collapses. 図 3-26 shows overcurrent without soft-start implementation. Channel 1 - AC voltage (blue), Channel 2 - AC current (light green), Channel 3 - DC voltage (dark green)

図 3-26. Without Soft Start

図 3-27 shows reduced current spike with soft-start implementation. Channel 1 - AC voltage (blue), Channel 2 - AC current (light green), Channel 3 - DC voltage (dark green).

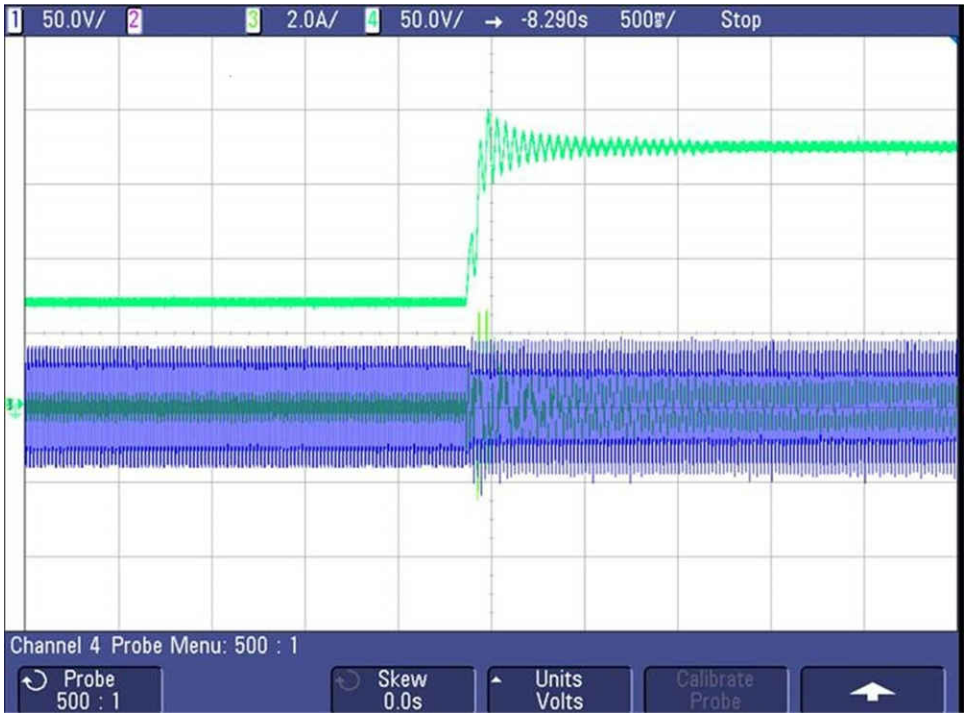


図 3-27. Soft Start With Adaptive Dead Band

- SFRA is integrated in the software of this lab to verify the designed compensator provides enough gain and phase margin by measuring on hardware. To run the SFRA keep the project running, and from the cfg page, click on the SFRA icon. SFRA GUI will pop up.
- Select the options for the device on the SFRA GUI. For example, for F28377D select floating point. Click on *Setup Connection*. On the pop-up window uncheck the boot on connect option, and select an appropriate COM port. Click *OK*. Return to the SFRA GUI, and click *Connect*.
- The SFRA GUI will connect to the device. A SFRA sweep can now be started by clicking Start Sweep. The complete SFRA sweep will take a few minutes to finish. Activity can be monitored by seeing the progress bar on the SFRA GUI and also checking the flashing of blue LED on the back on the control card that indicates UART activity. Once complete, a graph with the open loop plot will appear, as in 図 3-28 and 図 3-29 which corresponds to plant and loop response measured by SFRA GUI respectively. This verifies that the designed compensator is indeed stable

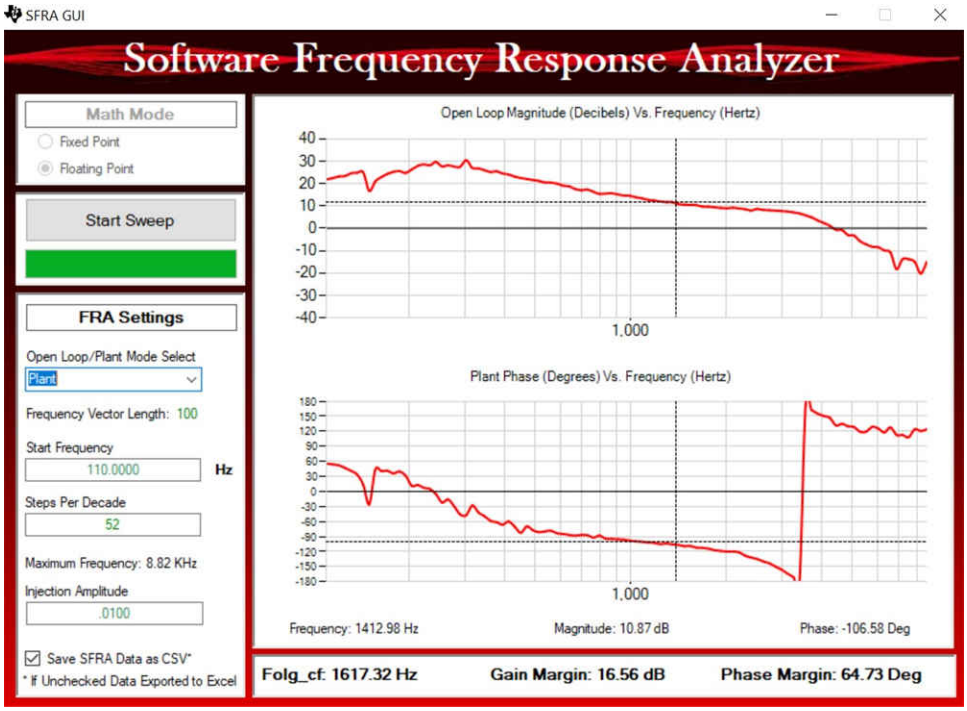


図 3-28. PFC SFRA Plant Response for Current Loop

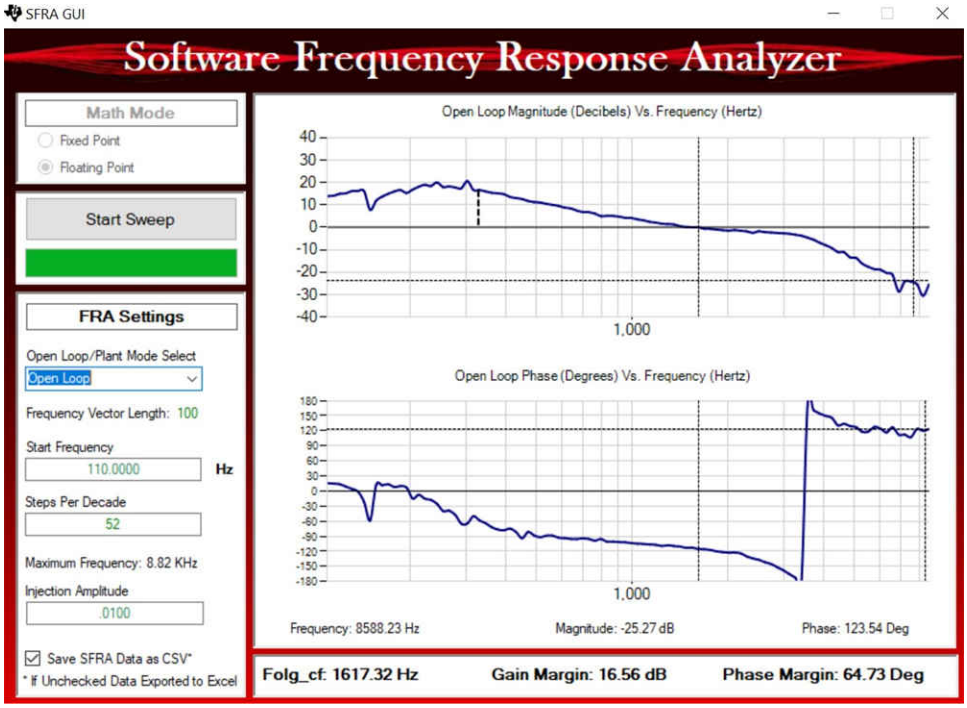


図 3-29. PFC SFRA Loop Response for Current Loop

- The frequency response data is also saved in the project folder under an SFRA data folder and is time stamped with the time of the SFRA run.
- This completes verification of Lab 6.

3.2.3.3 Lab 7

In this build level the voltage and current loop for the PFC is checked. Here the variable TINV_vBusRef_pu is defined to set the voltage at which the output DC bus voltage is to be regulated.

図 3-30 describes the software flow for running Lab 7.

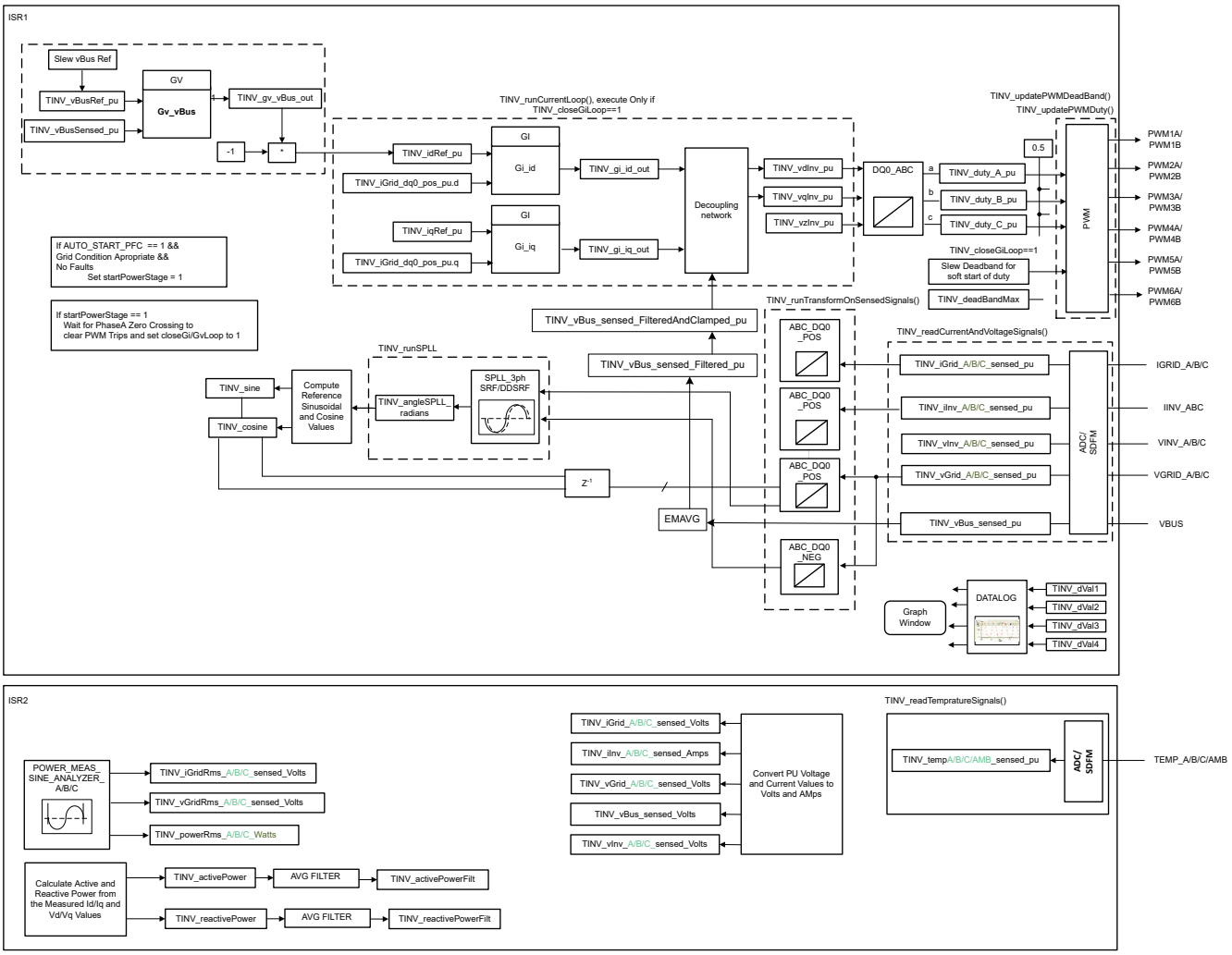


図 3-30. Lab 7 Software Diagram

Set the project to Lab 7 by changing the Lab Number in the <settings.h> file, (this will be changed by powerSUITE GUI when using powerSUITE project).

In the user settings.h file some additional options are available, but the following code is used for the tests documented in this user guide.

```
#if TINV_LAB == 7
#define TINV_TEST_SETUP TINV_TEST_SETUP_RES_LOAD
#define TINV_PROTECTION TINV_PROTECTION_ENABLED
#define TINV_SFRA_TYPE TINV_SFRA_CURRENT
#define TINV_SFRA_AMPLITUDE (float32_t)TINV_SFRA_INJECTION_AMPLITUDE_LEVEL2
#define TINV_POWERFLOW_MODE TINV_RECTIFIERER_MODE
#define TINV_DC_CHECK 0
#define TINV_SPLL_TYPE TINV_SPLL_SRF
#endif
```

In this check the SW is run on the hardware, or the HIL platform, or both.

Refer to the hardware test set up section for actual details of the equipment used for configuring the test. At this time, do not supply any HV power to the board.

- First launch the main.cfg and select Lab 7 in the project options. The compensator style (PI compensator) and the tuning loop (current loop) will be automatically populated. Now click run compensation designer icon and compensation designer tool will launch, with the model of the current loop plant with parameters specified on the powerSUITE page.
- 図 3-31 shows the current compensator coefficients used for running the control loop. The user can modify these coefficients to meet the necessary loop bandwidth and phase margin. The ideal coefficients with resistive load are slightly different than the one used for grid connection because the grid impedance is very low. The compensator design transfer function and response will be as shown in 図 3-31.

```
#define TINV_GI_PI_KP ((float32_t)1.8540138247))
#define TINV_GI_PI_KI ((float32_t)0.0081723506))
```

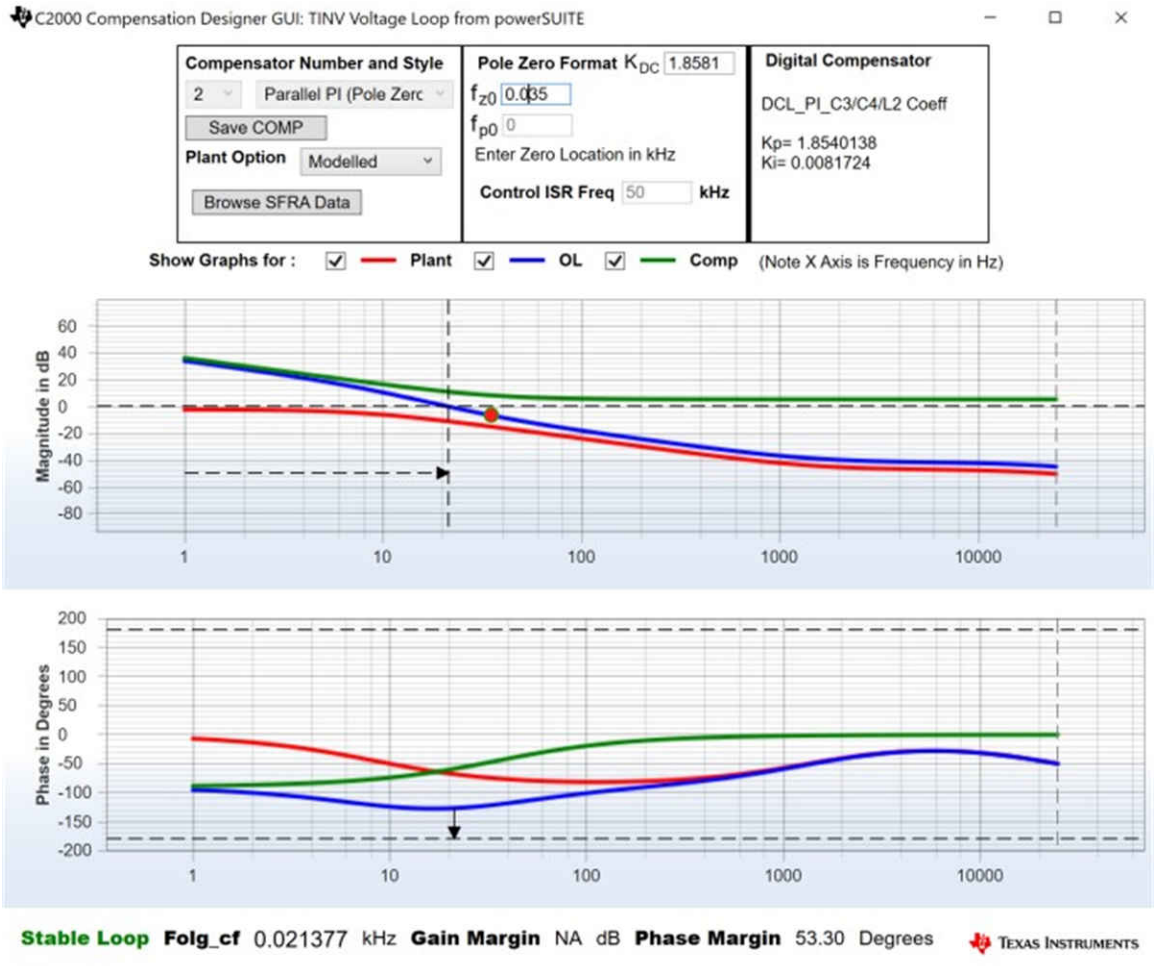


図 3-31. Compensator Design GUI - Voltage Loop PI Coefficients

- Once satisfied with the proportional and integral gain values, click on *Save COMP*. This will save the compensator values into the project. Close the Compensation Designer, and return to the powerSUITE page.
- Turn on the auxiliary power supply and set it to 15 V. Build and load the code, use the lab7.js file to populate the watch variables in the CCS window.
- Set the load resistance to a high value 3.18 kΩ.
- Set the AC input voltage to 230 V_{RMS} with appropriate current limit.
- After turning on the ac power supply, immediately turn on the relay by writing a 1 to TINV_allRelaySet. Ensure that the relay is turned on immediately (within 3-4 seconds) after turning on the AC supply.
- Now set TINV_vBusRef_pu to 0.684 pu. This corresponds to bus voltage of 800 V
- To start the PFC mode, enter "1" on TINV_startPowerStage variable, the current should now be drawn from the grid as a sinusoidal signal (with some harmonics as it is at low power) and boost action seen on the vBus. The output voltage will boost from 550 V to around 800 V drawing around 250 W power from AC supply as shown in 図 3-32. This transition happens in around 150 ms.

- The current will become sinusoidal as the load is increased. This verifies start up of PFC at 230 V_{RMS} and is shown in 図 3-32.
- In case any overcurrent trip is observed which causes the PWMs to switch off, please refer the notes in Lab 5 to debug this condition.
- The converter efficiency results and transient tests are shown in the Test Results section.
- SFRA is integrated in the software of this lab to verify the designed compensator provides enough gain and phase margin by measuring on hardware. To run the SFRA keep the project running, and from the cfg page, click on the SFRA icon. SFRA GUI will pop up.
- Select the options for the device on the SFRA GUI. For example, for F28377D select floating point. Click on *Setup Connection*. On the pop-up window uncheck the boot on connect option, and select an appropriate COM port. Click *OK*. Return to the SFRA GUI, and click *Connect*.
- The SFRA GUI will connect to the device. A SFRA sweep can now be started by clicking *Start Sweep*. The complete SFRA sweep will take a few minutes to finish. Activity can be monitored by seeing the progress bar on the SFRA GUI and also checking the flashing of blue LED on the back on the control card that indicates UART activity. Once complete, a graph with the open loop plot will appear, as in 図 3-32. 図 3-32 shows measured plant response by SFRA GUI and 図 3-33 shows measured loop response by SFRA GUI. This verifies that the designed compensator is indeed stable.

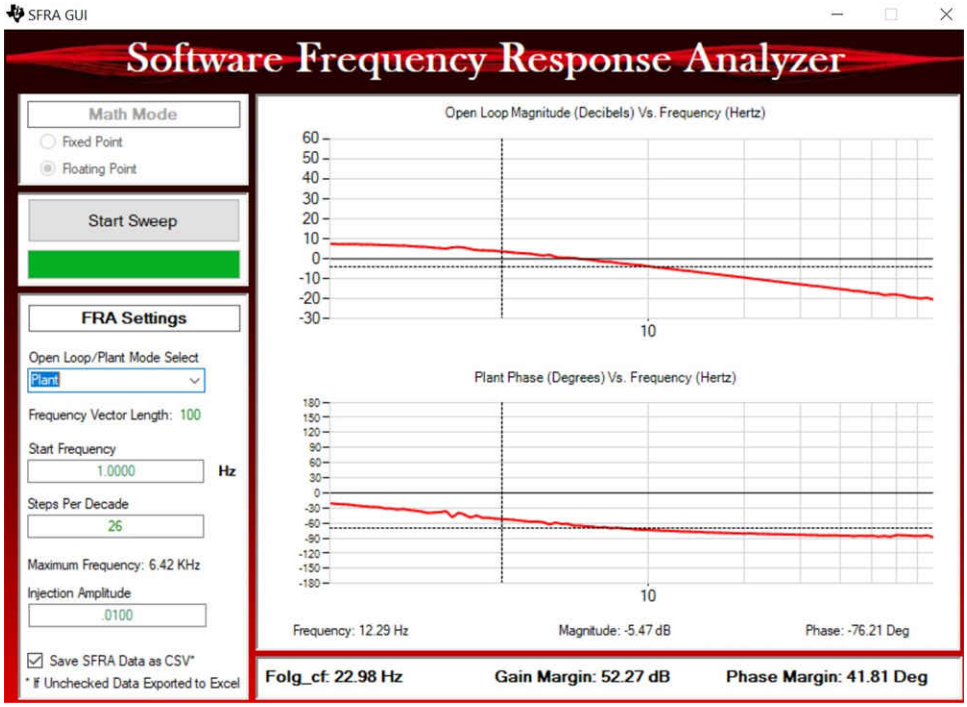


図 3-32. PFC SFRA Plant Response for Voltage Loop

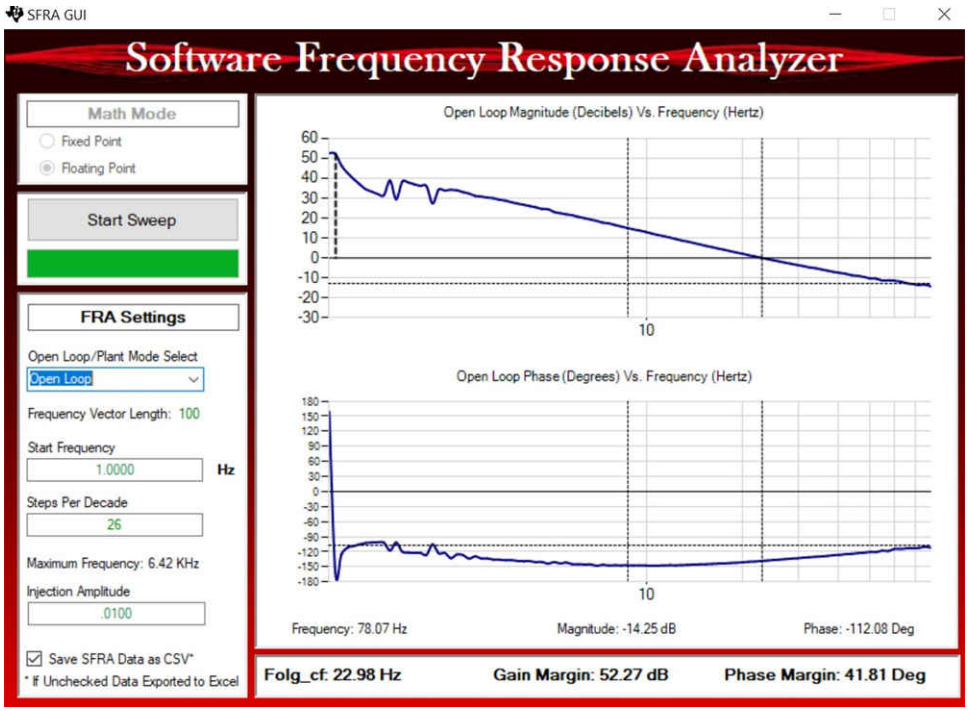


図 3-33. PFC SFRA Loop Response for Voltage Loop

- The frequency response data is also saved in the project folder under an SFRA data folder and is time stamped with the time of the SFRA run. Also, note the measured gain and phase margin are close to the modelled values as shown in the voltage loop compensator design as previously elaborated.
- This action verifies the voltage loop compensator design. To bring the system to a safe stop, bring the input AC voltage down to zero.

3.2.4 Test Setup for Efficiency

To test the efficiency of this reference design, use the following equipment as shown in 図 3-34:

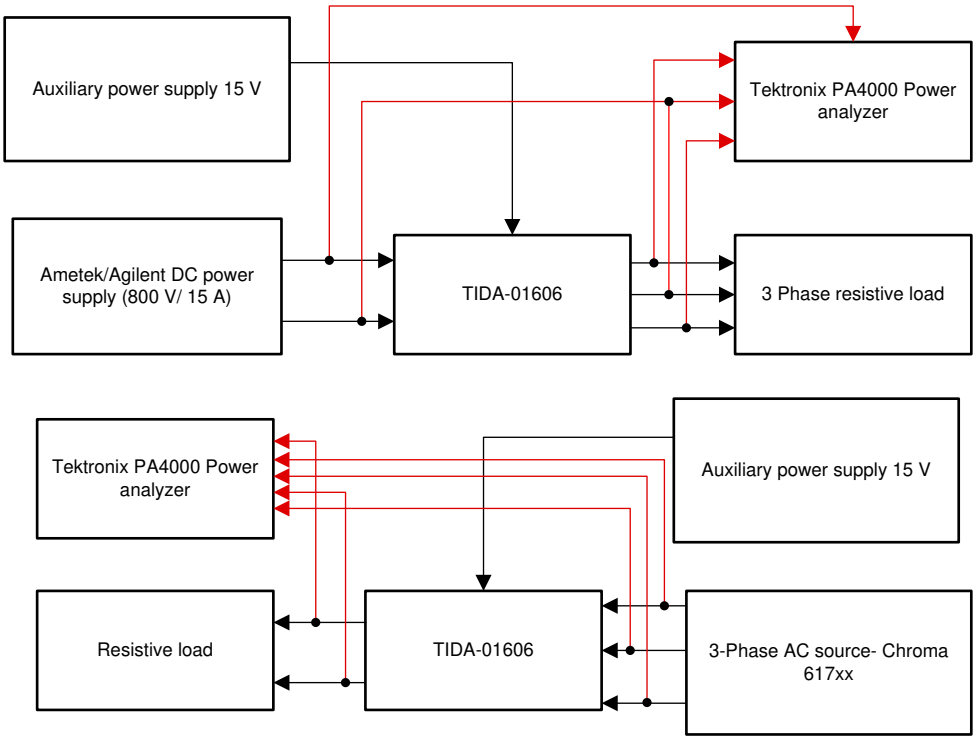


図 3-34. Test Setup for Efficiency

- A Chroma 617xx series three phase AC power supply to test PFC mode and an AMETEK, Agilent DC power supply of 800 V to support inverter mode (TIDA-01606) of operation.
- A 110-kW Simplex PowerStart (or any three-phase resistive) load bank is used as a configurable load to test the design at various set points.
- A Tektronix PA4000 Precision Power Analyzer
- An external BK precision bench power supply is used to provide a 15-V input to power the DUT.

The final design dimensions are outlined in 表 3-8 and show a total volume of 7 L. With a power rating of 10 kW, this results in a power density of 1.44 kW/L.

3.2.5 Test Results

The following sections cover the results for the inverter mode and PFC mode of operation.

3.2.5.1 PFC Mode - 230 V_{RMS}, 400 V L-L

セクション 3.2.5.1.1 shows the results when the converter is operated in the PFC mode. The applied AC input voltage is around 230 V_{RMS} and the resistive load of 3.18 kΩ is connected across DC terminals.

3.2.5.1.1 PFC Start-up – 230 V_{RMS}, 400 L-L AC Voltage

The start-up sequence of the power stage is shown in 図 3-35 with input three phase 400- VL-L and output bus regulated at 800 V and a 245-W load. The boost action from 550 V to 800 V happens in around 140 ms. 図 3-35 shows the start-up performance of PFC. **Scope signals:** Channel 1 - AC voltage (blue), Channel 2 - DC link voltage (light green), Channel 3 - AC current (dark green).

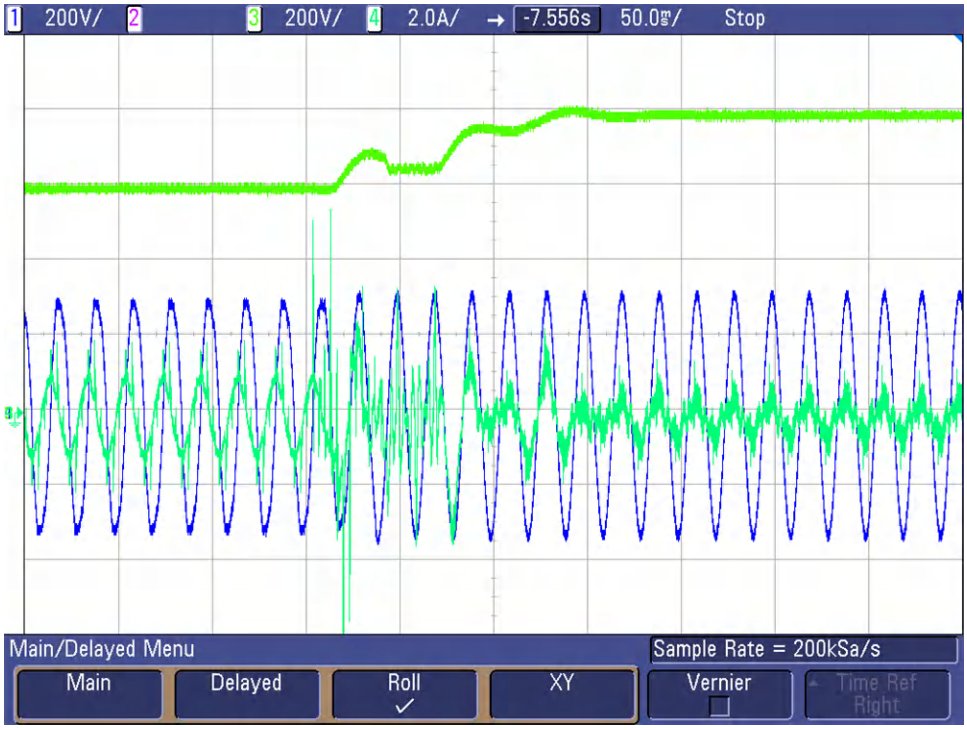


図 3-35. PFC 230 V_{RMS} Start-up

Care has been taken in the tuning of voltage loop to ensure that there is no overvoltage (above 800 V) during the ramp up of DC link voltage from 550 V to 800 V at start-up. The bumps in the DC link voltage during this period is because the current implementation of d-q based control in software is not fully optimized for this. Also, starting the PFC at high load can lead to overcurrent events which in turn can trip the PWMs. Hence it is advisable to start the PFC in the above mentioned test condition or lower output power. Refer to Lab 5 on possible causes for PWM trip and possible precautions the user needs to take to avoid this condition.

3.2.5.1.2 Steady State Results at 230 V_{RMS}, 400 V L-L - PFC Mode

The following images show the results obtained from the power analyzer as the load is slowly increased to 4.7 kW. 図 3-36 shows the steady state performance of PFC at 4.7-kW output power. **Scope signals**: Channel 1 - AC voltage (blue), Channel 2 - DC link voltage (light green), Channel 3 - AC current (dark green).

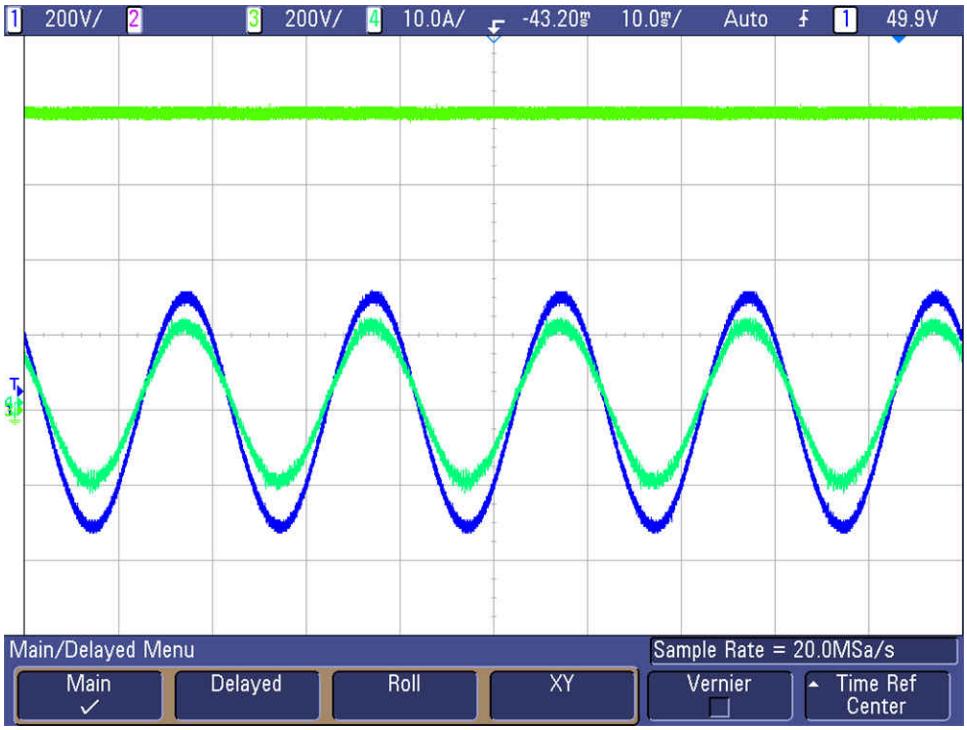


図 3-36. PFC Waveforms at Steady State - 4.7 kW

図 3-37 shows power key efficiency and THD figures captured at 4.7 kW.

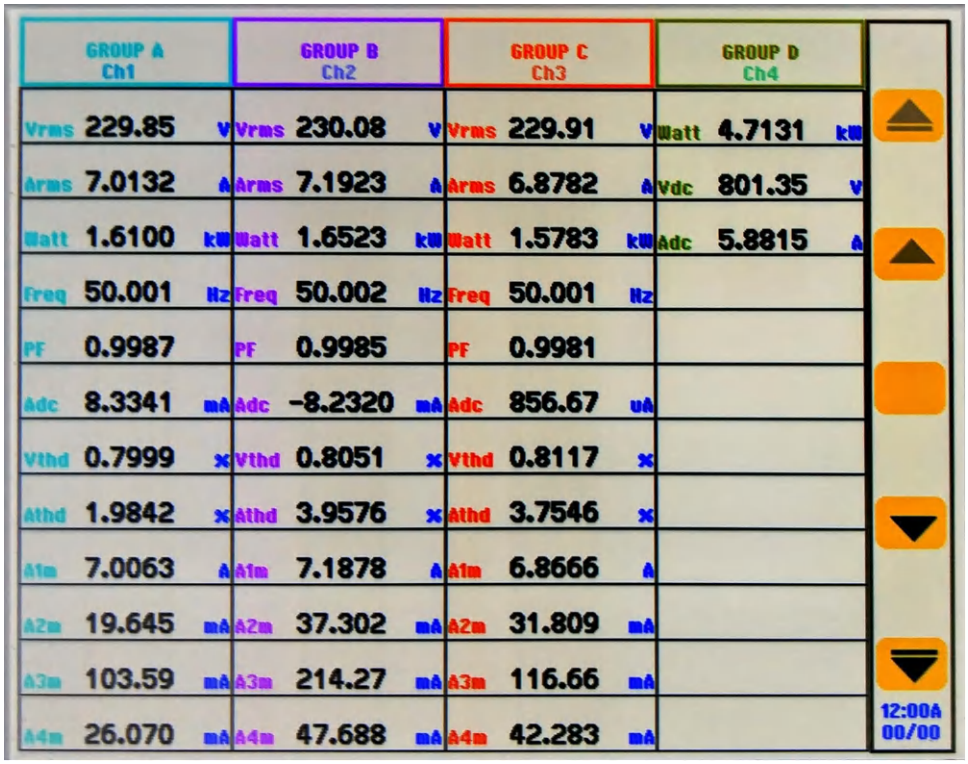


図 3-37. PFC Results at Steady State - 4.7 kW

3.2.5.1.3 Efficiency and THD Results at 220 V_{RMS}, 50 Hz – PFC Mode

This section covers the efficiency and THD results for the converter operating in PFC mode at 220 V_{RMS}. 表 3-5 summarizes the results obtained from power analyzer results when the load is varied from 200 W to 5 kW and DC bus voltage is kept constant at 800 V.

表 3-5. Detailed Test Results With 220 VAC IN, 800-V DC OUT, and Varying Power Levels

PHASE - A VOLTAGE	PHASE - B VOLTAGE	PHASE - C CURRENT	PHASE - A CURRENT (A)	PHASE - B CURRENT	PHASE - C CURRENT	OUTPUT DC CURRENT (A)	OUTPUT POWER (W)
220.3	219.94	220.15	0.398	0.573	0.405	0.25	200
220.1	219.98	220.04	0.974	1.124	0.97	0.753	600
220.09	220.02	219.98	2.55	2.64	2.48	2.018	1610
220.02	219.94	219.93	4.142	4.166	4.016	3.283	2619
220.01	219.97	219.94	5.281	5.262	5.111	4.182	3337
219.92	219.94	219.86	7.325	7.231	7.079	5.793	4624
220.01	219.97	220.03	7.89	7.81	7.76	6.278	5023

OUTPUT POWER (W)	EFFICIENCY (%)	CURRENT-THD (PHASE-A)	CURRENT-THD (PHASE-B)	CURRENT-THD (PHASE-C)	PFC- (PHASE-A)	PFC- (PHASE-B)	FC- (PHASE-C)
200	80.93	38.88	55.46	53.44	0.8098	0.8395	0.7934
600	92.06	13.22	23.44	18.54	0.9706	0.9621	0.9678
1610	96.06	5.26	9.59	6.89	0.9944	0.9923	0.9949
2619	96.9	3.09	5.63	4.53	0.9975	0.9968	0.9977
3337	97.11	2.33	4.32	3.66	0.9982	0.9978	0.9985
4624	97.29	1.724	3.034	2.712	0.9988	0.9987	0.9990

OUTPUT POWER (W)	EFFICIENCY (%)	CURRENT-THD (PHASE-A)	CURRENT-THD (PHASE-B)	CURRENT-THD (PHASE-C)	PFC- (PHASE-A)	PFC- (PHASE-B)	FC- (PHASE-C)
5023	97.37	1.47	2.76	1.98	0.9992	0.9991	0.9995

図 3-38, 図 3-39, and 図 3-40 show the efficiency, THD, and power factor under different load conditions.

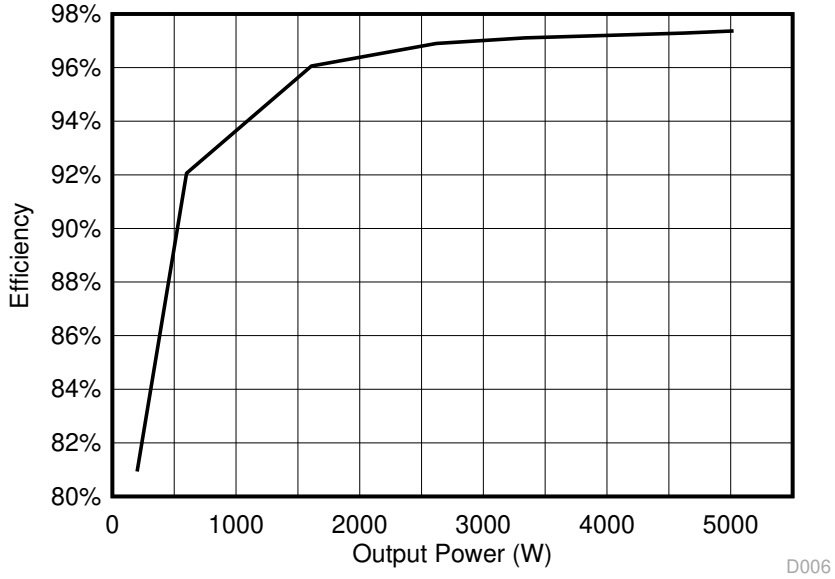


図 3-38. Efficiency Results - PFC Mode at 220 V_{RMS}

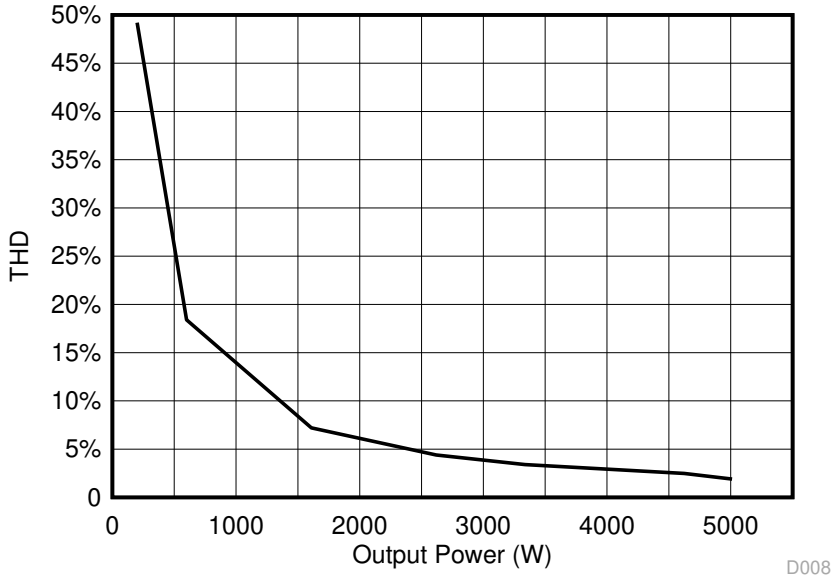


図 3-39. THD Results - PFC Mode at 220 V_{RMS}

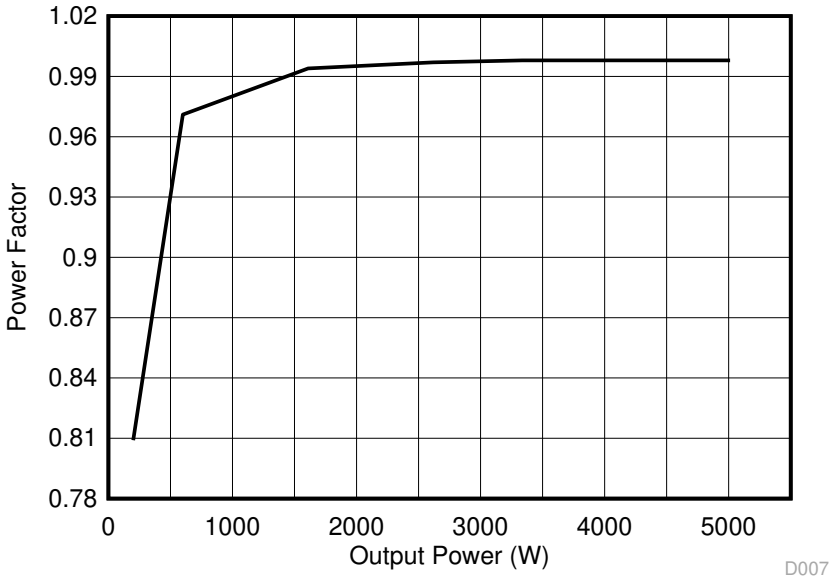


図 3-40. Power Factor Results - PFC Mode at 220 V_{RMS}

図 3-41 shows thermal performance of the board at 4.7 kW.

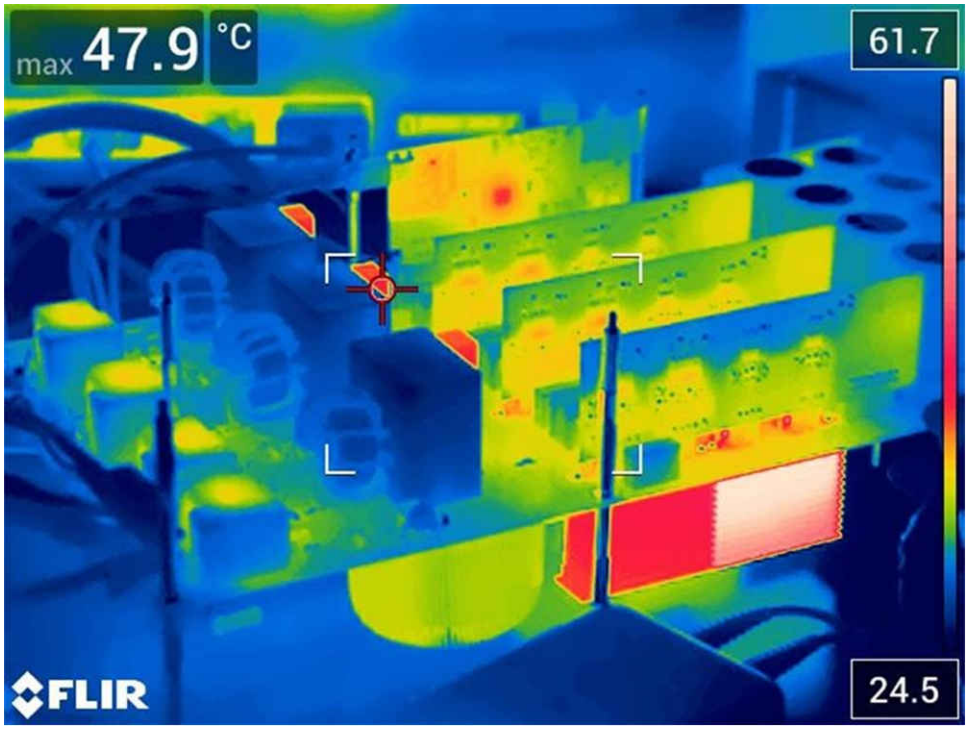


図 3-41. Thermal Image at 4.7 kW

3.2.5.1.4 Transient Test With Step Load Change

In the following section, the converter is initially operating at 800 V DC link voltage at 220 V_{RMS} AC input voltage and delivering around 400 W of output power. It is then subjected to a step load and the results are shown here for two cases. 図 3-42 shows the transient performance when the a step load of 2 kW is applied. The voltage overshoot on the DC link voltage is around 35 V. **Scope signals:** Channel 1 - AC voltage (blue), Channel 2 - AC current (light green), Channel 3 - DC link voltage (dark green).

図 3-42. Voltage Step - 400 W → 2.4 kW

図 3-43 shows the transient performance when the a step load of 4 kW is applied. The voltage overshoot on the DC link voltage is around 40 V. **Scope signals:** Channel 1 - AC voltage (blue), Channel 2 - AC current (light green), Channel 3 - DC link voltage (dark green).

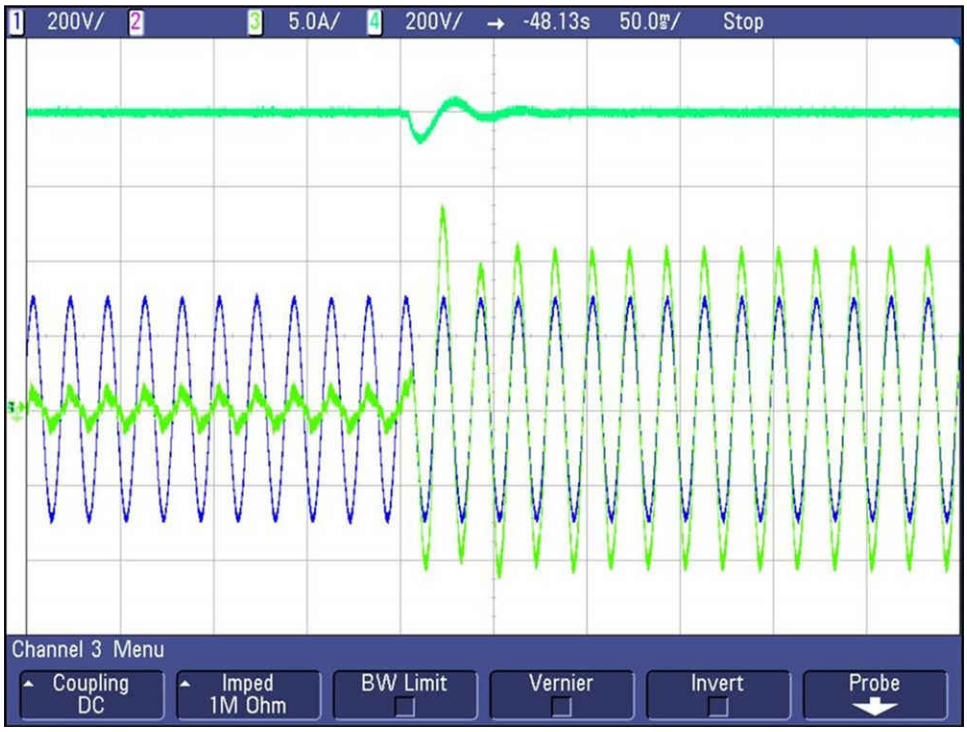


図 3-43. Voltage Step - 400 W → 4.4 kW

図 3-44 shows the transient performance when the a step down load of 2 kW is applied. **Scope signals:** Channel 1 - AC voltage (blue), Channel 2 - AC current (light green), Channel 3 - DC link voltage (dark green).

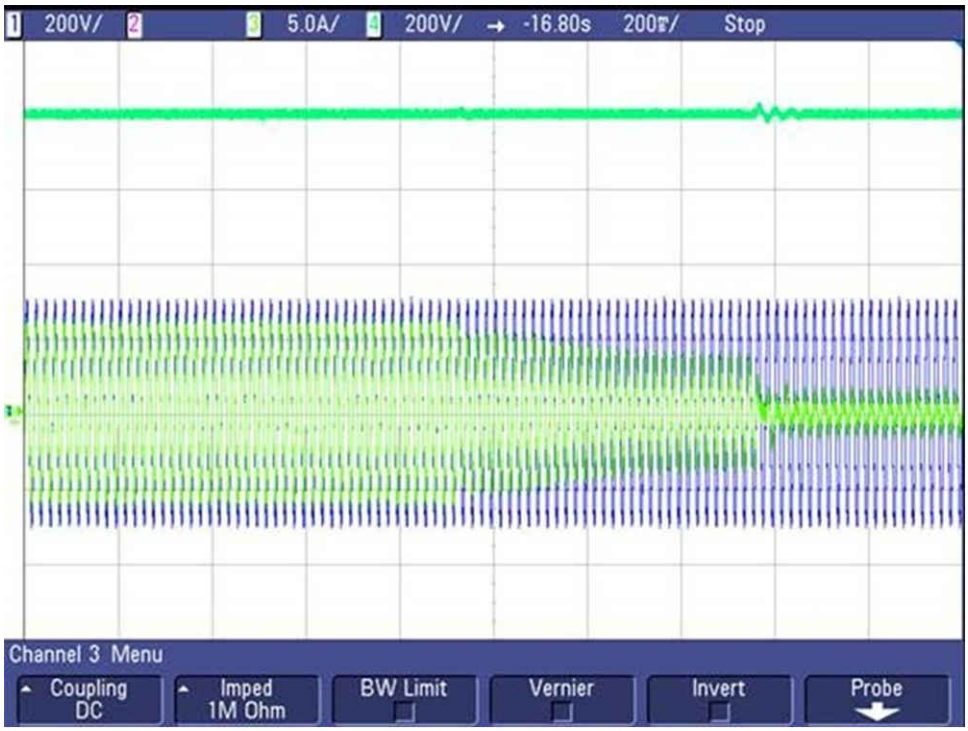


図 3-44. Step Down Load Transient - 2.4 kW → 400 W

図 3-45 shows the output voltage regulation when the input voltage is changed suddenly from 210 VAC to 175 VAC and then back to 210 VAC. **Scope signals:** Channel 1 - AC voltage (blue), Channel 2 - AC current (light green), Channel 3 - DC link voltage (dark green).

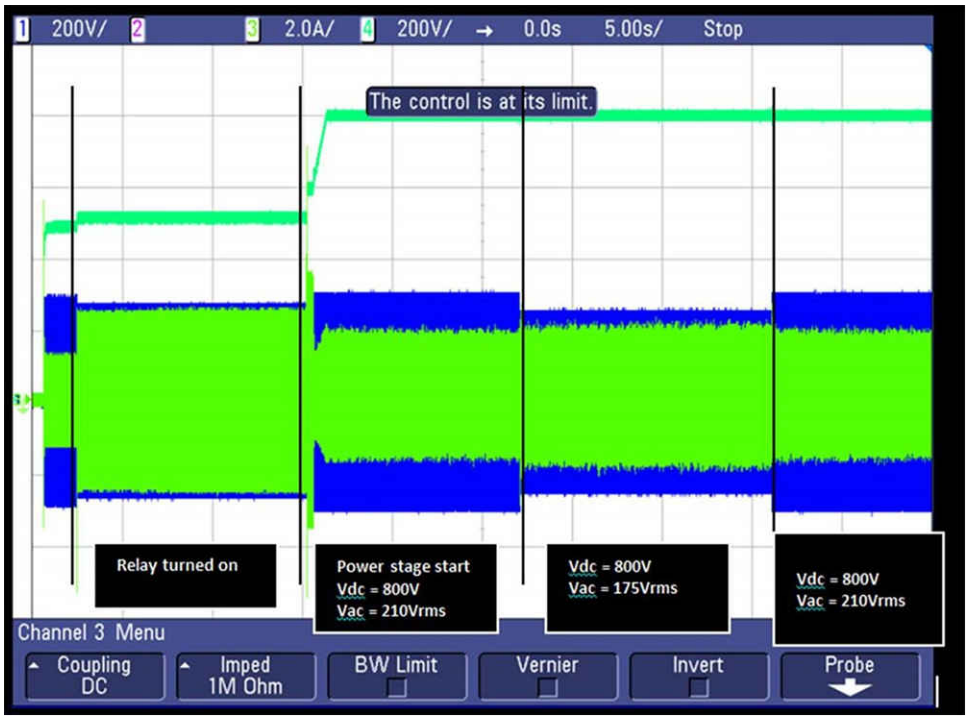


図 3-45. PFC Load Regulation to Input Voltage Change

3.2.5.2 PFC Mode - 120 V_{RMS}, 208 V L-L

セクション 3.2.5.2.1 shows the results when the converter is operated in the PFC mode. The applied AC input voltage is around 120 V_{RMS} and the resistive load of 3.18 kΩ is connected across DC terminals. Since the results for the 230-V case have been discussed in detail, only a few results for this case are shown.

3.2.5.2.1 Steady State Results at 120 V_{RMS}, 208 V-L-L - PFC Mode

This section shows the results obtained from the power analyzer as the load is slowly increased to 3.2 kW. The 図 3-46 shows the steady state performance of PFC at 3.2 kW output power. **Scope signals**: Channel 1 - AC voltage (blue), Channel 2 - DC link voltage (light green), Channel 3 - AC current (dark green).

The results in 図 3-46 are captured at 50 Hz but these can be verified at 60 Hz as well.

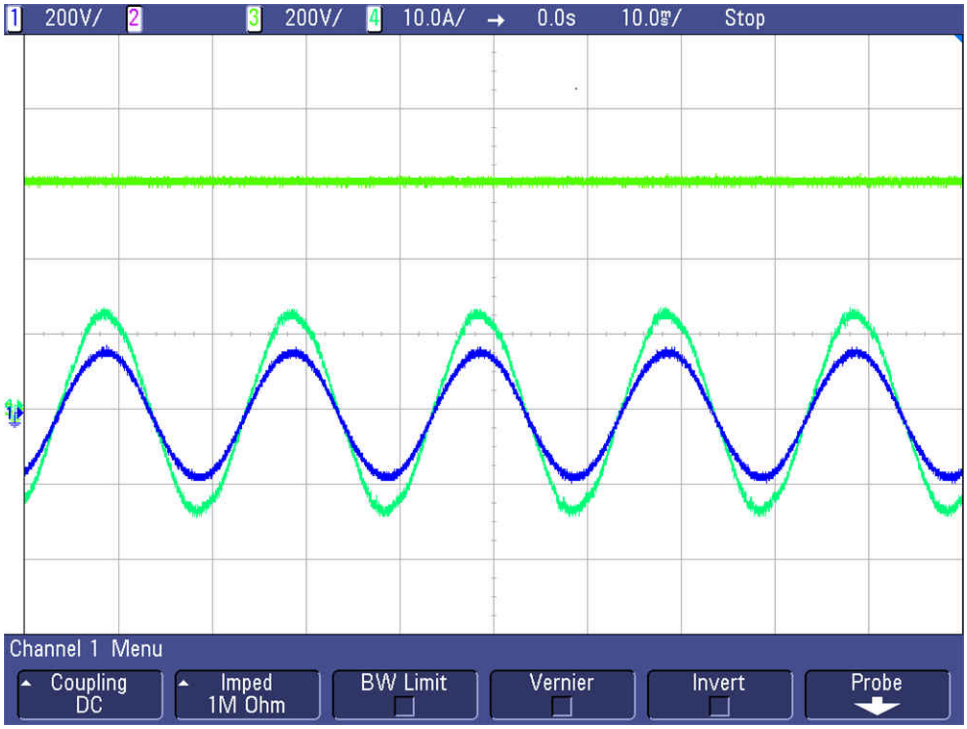


図 3-46. PFC Waveforms at Steady State - 3.2 kW

図 3-47 shows power key efficiency and THD figures captured at 3.2 kW.

GROUP A Ch1		GROUP B Ch2		GROUP C Ch3		GROUP D Ch4	
Vrms	119.76 V	Vrms	119.66 V	Vrms	119.91 V	Watt	3.1657 kW
Arms	9.2300 A	Arms	9.2741 A	Arms	9.2508 A	Vdc	608.24 V
Watt	1.1046 kW	Watt	1.1089 kW	Watt	1.1084 kW	Adc	5.2049 A
Freq	50.001 Hz	Freq	50.002 Hz	Freq	50.001 Hz		
PF	0.9992	PF	0.9993	PF	0.9992		
Adc	-66.348 mA	Adc	72.457 mA	Adc	-7.9638 mA		
Vthd	0.9989 %	Vthd	0.9987 %	Vthd	0.9754 %		
Athd	1.9572 %	Athd	1.9077 %	Athd	1.9637 %		
A1m	9.2202 A	A1m	9.2665 A	A1m	9.2367 A		
A2m	24.214 mA	A2m	16.111 mA	A2m	35.546 mA		
A3m	95.259 mA	A3m	86.576 mA	A3m	131.20 mA		
A4m	51.308 mA	A4m	44.286 mA	A4m	53.504 mA		

12:00A 00/00

図 3-47. PFC Results at Steady State - 3.2 kW

INPUT AC VOLTAGE	OUTPUT DC VOLTAGE	OUTPUT DC CURRENT	OUTPUT POWER (W)	EFFICIENCY (%)	AVERAGE THD (%)	POWER FACTOR
120	608.26	0.19	116	78.61	39.33	0.81
120	608.36	1.54	936.7	94.9	5.8	0.995
120	608.15	2.13	1295	95.39	4.35	0.997
120	608.26	3.45	2100	95.71	2.71	0.998
120	608.26	4.85	2949	95.37	1.91	0.999
120	608.24	5.2	3165.7	95.29	1.85	0.999

3.2.5.2.2 Efficiency and THD Results at 120 V_{RMS} - PFC Mode

図 3-48, 図 3-49, and 図 3-50 show the efficiency, THD, and power factor under different load conditions for the PFC operating at 120 V_{RMS}.

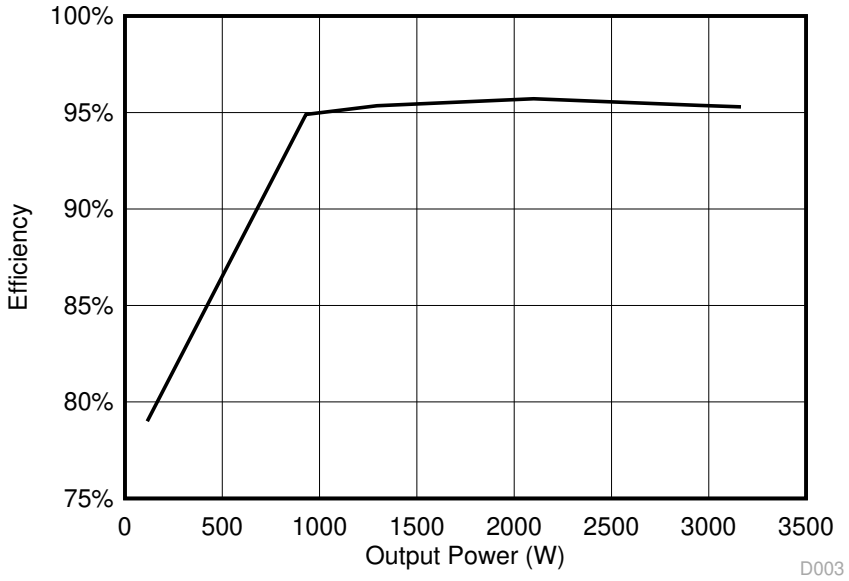


図 3-48. Efficiency Results - PFC Mode at 120 V_{RMS}

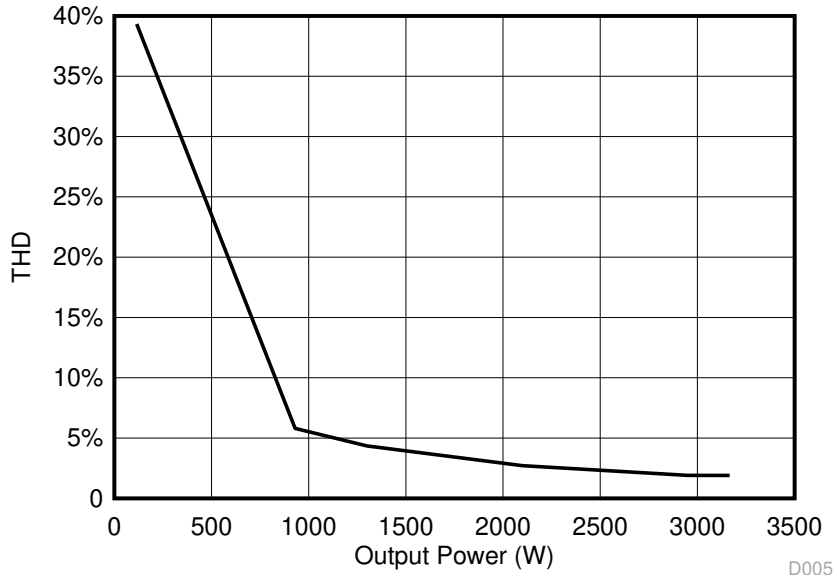


図 3-49. THD Results - PFC Mode at 120 V_{RMS}

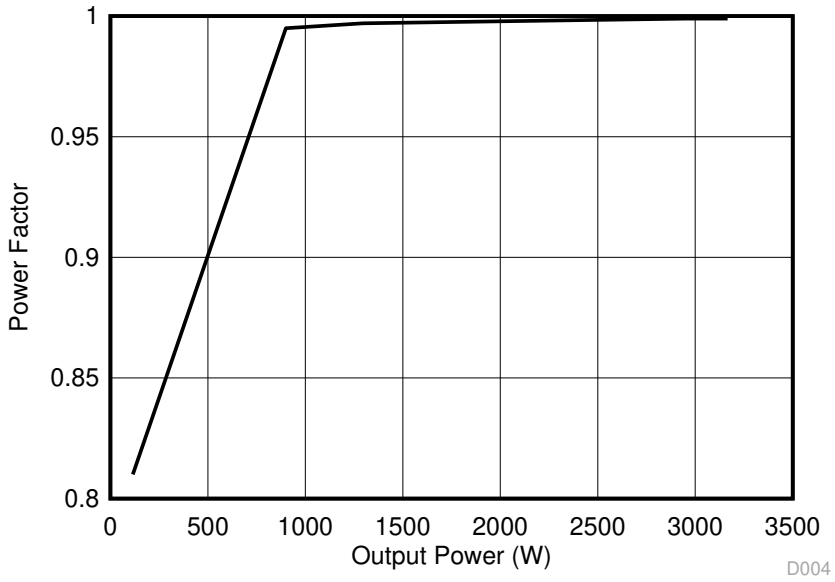


図 3-50. Power Factor Results - PFC Mode at 120 V_{RMS}

3.2.5.3 Inverter Mode

セクション 3.2.5.3.1 shows the results when the converter is operated in the inverter mode. The applied DC input voltage is 800 V and the resistive load is connected across AC terminals.

3.2.5.3.1 Inverter Closed Loop Results

The inverter is tested in the closed current loop in Lab 3 where the current reference is varied by changing the variable TINV_idRef_pu from the watch window. Setting this value to around 0.35 pu should deliver around 3.5 kW of power at the AC terminals. 図 3-51 shows closed current loop operation and the efficiency results obtained. **Scope signals:** Channel 1 - DC link voltage (blue), Channel 2 - AC voltage (light green), Channel 3 - AC current (dark green).

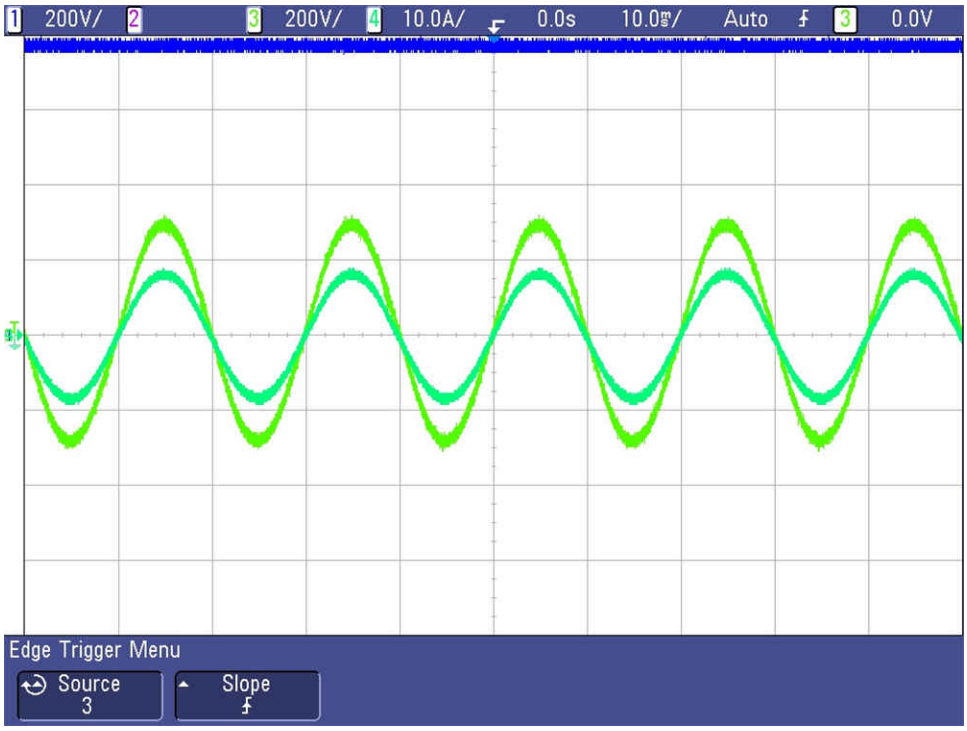


図 3-51. Inverter Closed Current Loop Waveforms

図 3-52 shows power key efficiency and THD figures captured with power analyzer at 3.8 kW.

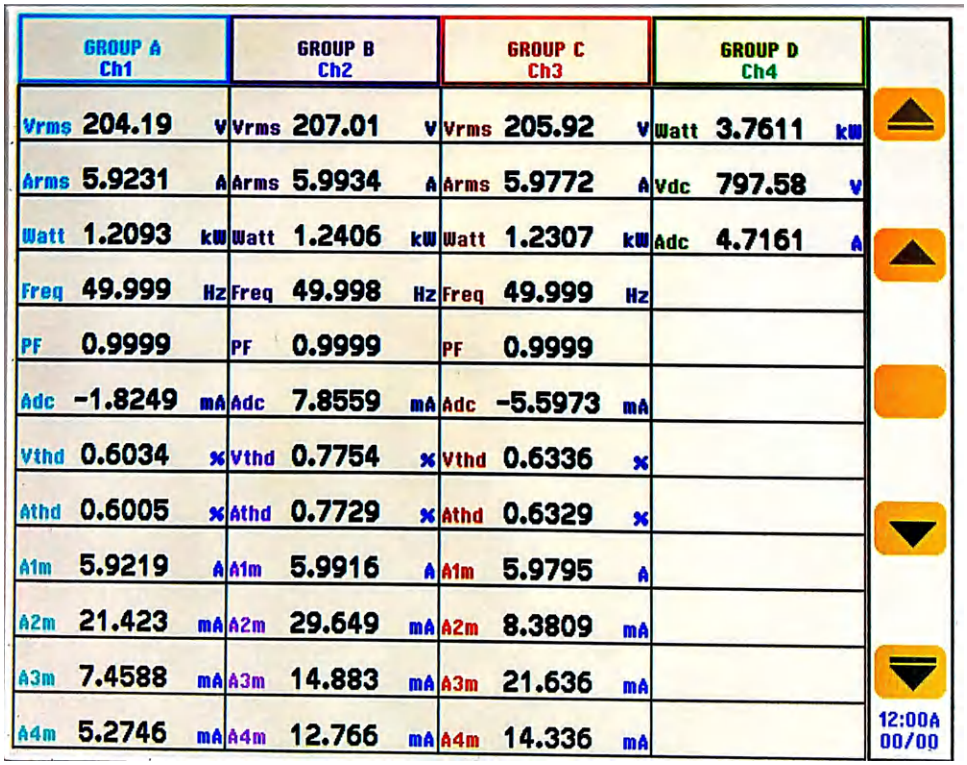


図 3-52. Inverter Closed Current Loop Results

3.2.5.3.2 Efficiency and THD Results - Inverter Mode

This section covers the efficiency and THD results for the converter operating in inverter mode at 800 V DC link. 表 3-6 summarizes the results obtained from power analyzer results when the load is varied from up to 3.8 kW.

表 3-6. Detailed Test Results With 220 VAC OUT, 800-V DC IN, and Varying Power Levels

OUTPUT POWER (WATTS)	EFFICIENCY (%)	CURRENT-THD (PHASE-A)	CURRENT-THD (PHASE-B)	CURRENT-THD (PHASE-C)	POWER FACTOR
1563	97.4	1.37	0.92	0.78	0.999
2555	97.6	1.01	0.85	0.74	0.999
3761	97.8	0.6	0.77	0.63	0.999

図 3-53 and 図 3-54 show the efficiency and THD under different load conditions for the inverter operating at 800 VDC.

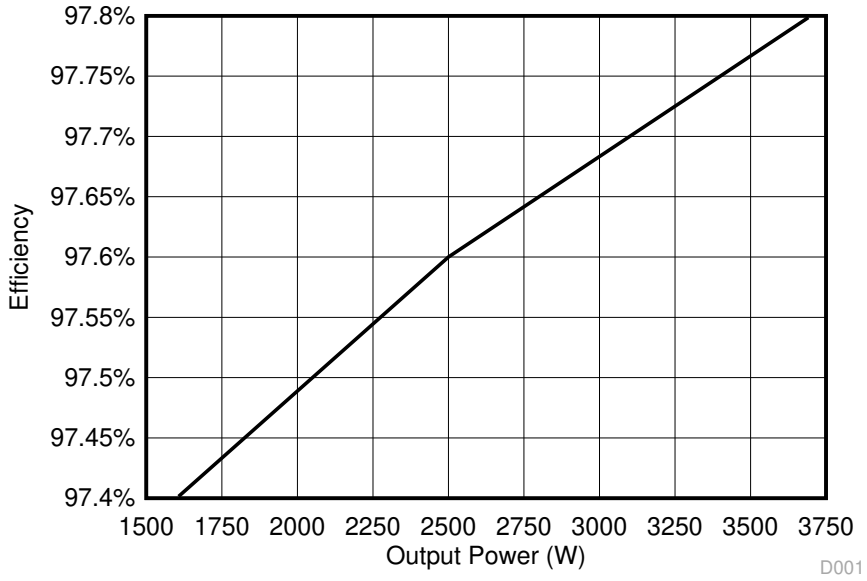


図 3-53. Efficiency Results - Inverter Mode

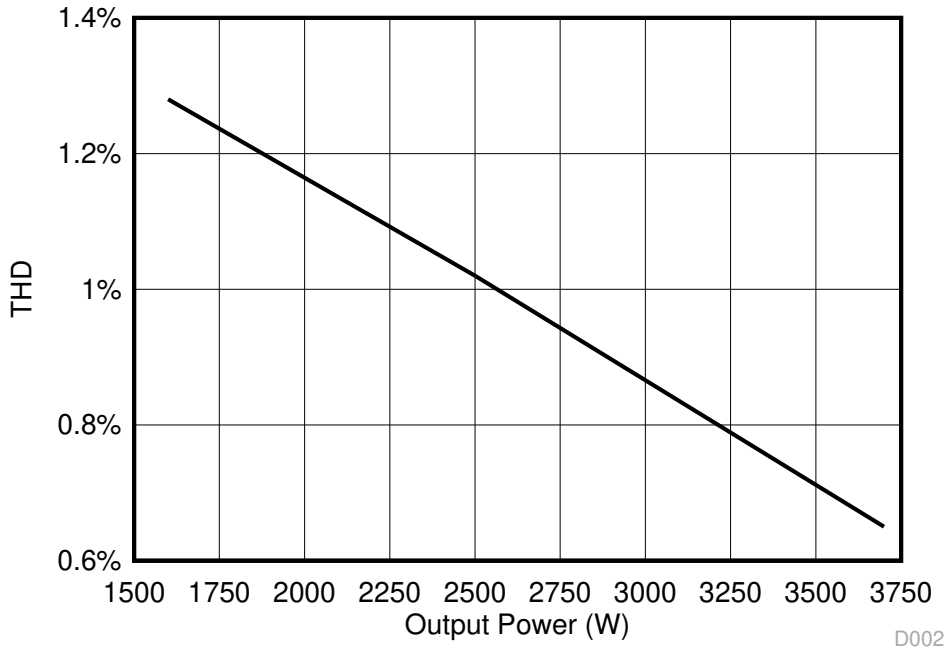


図 3-54. THD Results - Inverter Mode

3.2.5.3.3 Inverter - Transient Test

図 3-55 shows load transient performance of the inverter from no load to 3.2 kW by applying a current step in the current loop. **Scope signals:** Channel 1 - DC link voltage (blue), Channel 2 - AC voltage (light green), Channel 3 - AC current (dark green).

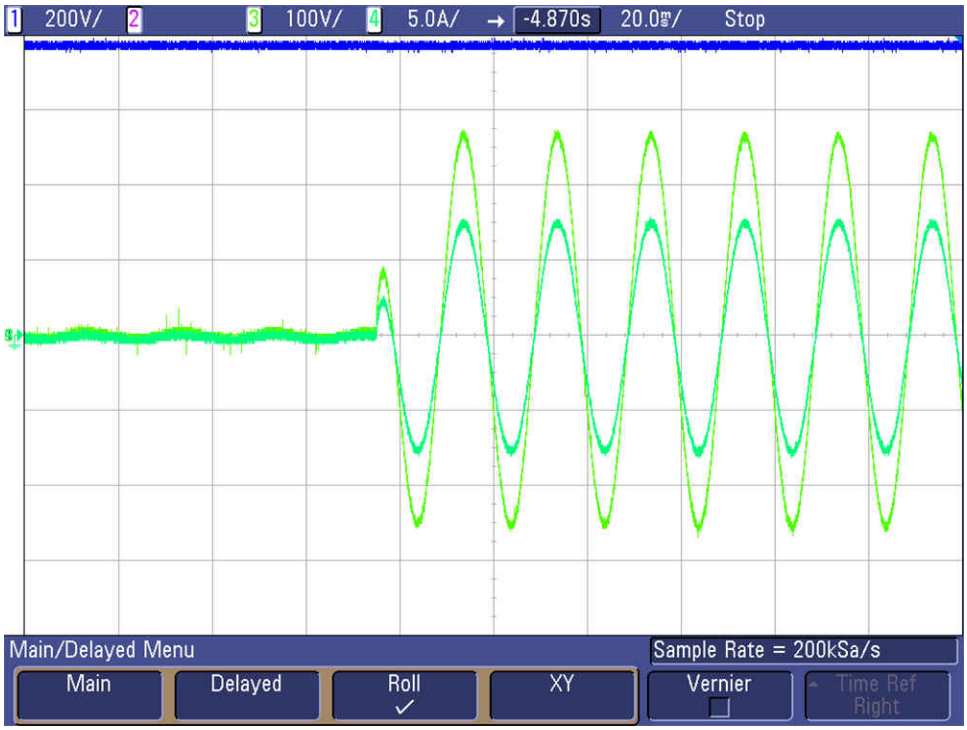


図 3-55. Inverter Current Loop Transient

3.2.6 Open Loop Inverter Test Results

The system efficiency results are detailed in 表 3-7.

表 3-7. System Efficiency Results

POWER RATING	10%	20%	30%	40%	50%	60%	70%	80%	90%	100%
600-V input	95.6%	97.43%	97.74%	97.82%	97.79%	97.79%	97.79%	97.79%		
800-V input	92.64%	96.55%	97.87%	98.31%	98.42%	98.47%	98.51%	98.54%	98.7%	98.22%
1000-V input	92.37%	96.55%	97.95%	98.52%	98.77%	98.95%	99.01%	99.06%	99.08%	99.02%

図 3-56 shows the inverter efficiency graph.

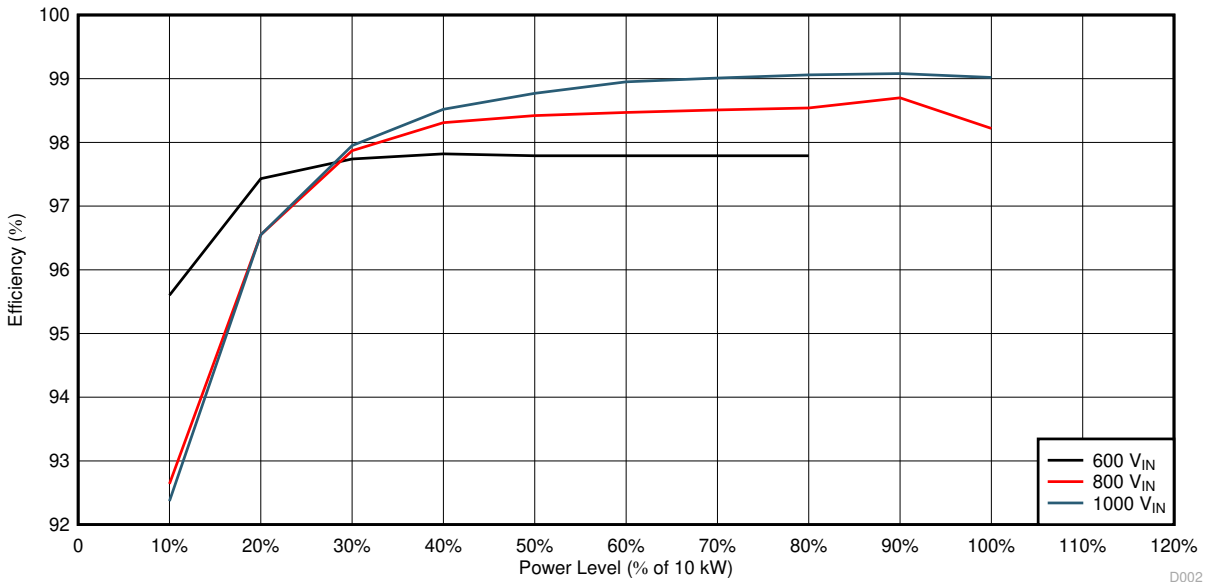


図 3-56. Inverter Efficiency

表 3-8 shows the dimensions of the system.

表 3-8. System Dimensions

AXIS	DIMENSION
X	350 mm
Y	200 mm
Z	100 mm
Volume	7 liters

The total energy density of the design is 10 kW/7L, or 1.43 kW/L.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01606.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01606.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01606.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-01606.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01606.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01606.

5 Trademarks

6 About the Authors

RUFFO RICCARDO received the Ph.D. degree in Electric, Electronics and Communication Engineering from Politecnico di Torino, Turin, Italy, in 2019. He is currently working at Texas Instruments Germany as System Engineer in the area of Grid Infrastructure, Renewable Energy. His main work includes EV charging, inductive wireless power transfer, photovoltaic, renewable energy, and energy storage applications.

KELVIN LE is a systems engineer at Texas Instruments, where he is responsible for developing system solutions for the Grid sector with a focus on EV Charging. Kelvin has been with TI since 2015. Kelvin earned his Bachelor of Science in Biomedical Engineering from the University of Central Oklahoma and his Master of Science in Electrical and Computer Engineering from the University of Texas at Austin.

The authors would like to thank **MANISH BHARDWAJ**, **BART BASILE**, **HARISH RAMAKRISHNAN**, and **MURALI KRISHNA PACHIPULUSU** for the support given for this reference design.

7 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (September 2022) to Revision H (December 2022) **Page**

- このリビジョンに対する変更は、ドキュメント全体を通して行われました。ゲート・ドライバ・ボードは、次の新しいコンポーネントを使用して変更されました。UCC21710 および UCC14240。電源ボードに実装されているパワー・スイッチが変更されました。LSIC1MO120E0080 および IKW20N60TFKSA1 の代わりに、C3M0075120D および C3M0060065D を使用しました。 1

Changes from Revision F (September 2021) to Revision G (September 2022) **Page**

- Updated all lab software diagrams: 図 3-4, 図 3-6, 図 3-10, 図 3-14, 図 3-18, 図 3-21, and 図 3-30..... 46
- Added descriptions for *check for DC bus overvoltage*, the *feed-forward and decoupling function*, and *SDFM-based current sensing, overcurrent protection (OCP)*, to the *Testing Inverter Operation* section..... 47
- Added descriptions for *check for DC bus overvoltage*, the *feed-forward and decoupling function*, and *SDFM-based current sensing, overcurrent protection (OCP)*, to the *Testing PFC Operation* section..... 60

Changes from Revision E (July 2021) to Revision F (September 2021) **Page**

- Missing TIDA-01606 ISOHVCARD board added for evaluation purposes in the *Test Hardware Required* section..... 39

Changes from Revision D (April 2021) to Revision E (July 2021) **Page**

- Updated *Voltage Loop Plant Frequency Response Measured vs Modelled* image..... 36

Changes from Revision C (March 2018) to Revision D (April 2021) **Page**

- 設計ガイドのリビジョン D を、制御設計、ハードウェアとソフトウェア、およびテストと結果の変更を反映するように更新。 1
- Added *Control Design* section..... 32
- Updated *Required Hardware and Software* section..... 39
- Updated *Testing and Results* section..... 46

Changes from Revision B (May 2020) to Revision C (August 2020) **Page**

- タイトルを「ソーラー・ストリング・インバータ用の 10kW、3 レベル、3 相 T タイプ・インバータのリファレンス・デザイン」に変更。 1

Changes from Revision A (March 2019) to Revision B (May 2020) **Page**

- Added *To obtain an attenuation factor of 10%, and using the earlier derived values, the value of r can be evaluated to be:* 18

Changes from Revision * (March 2018) to Revision A (March 2018) **Page**

- Updated block diagram Figure 1. *TIDA-01606 Block Diagram*: "F28004x Control Card" to "F28377D Control Card"..... 1

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