参考資料

デザイン・ガイド：TIDA-01605
2レベルのターンオフ保護を持つ車載用デュアル・チャネル、SiC MOSFETゲート・ドライバのリファレンス・デザイン

概要

このリファレンス・デザインは、炭化ケイ素(SiC) MOSFETをハーフ・ブリッジ構成で駆動するための、絶縁ゲート・ドライバ・ソリューションで、車載用に認定済みです。このデザインには、デュアル・チャネルの絶縁ゲート・ドライバのそれぞれで使用される、2つのプッシュプル・バイアス電源が含まれ、各電源は15Vおよび-4Vの出力電圧と、1Wの出力電力を供給します。ゲート・ドライバは、4Aのソースおよび6Aのシンク・ピーク電流を供給できます。このドライバには強化絶縁が実装されており、8kVピークおよび5.7kV RMS絶縁電圧に耐えられ、100V/nsを超える同相過渡耐性(CMTI)があります。このリファレンス・デザインには2レベルのターンオフ回路が含まれており、短絡状況において電圧オーバーシュートからMOSFETを保護します。DESAT検出スレッショルドおよび第2段ターンオフの遅延時間は構成可能です。フォルト信号およびリセット信号のインターフェイス用に、ISO7721-Q1デジタル・アイソレータが実装されています。これらの機能はすべて、40mm×40mmの小さな外形を持つ、2層PCB基板上に設計されています。

リソース

TIDA-01605	デザイン・フォルダ
UCC21530-Q1	プロダクト・フォルダ
SN6501-Q1	プロダクト・フォルダ
ISO7721-Q1	プロダクト・フォルダ
TPS7B6950-Q1	プロダクト・フォルダ
LMV762Q-Q1	プロダクト・フォルダ

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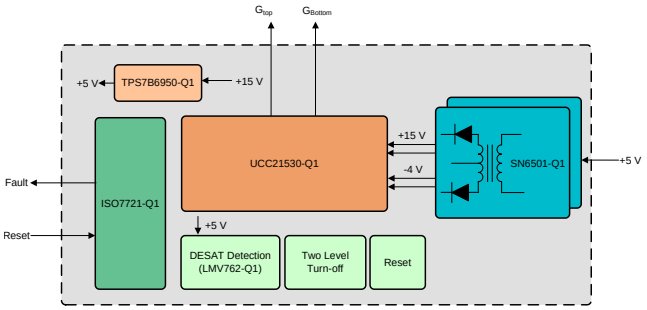
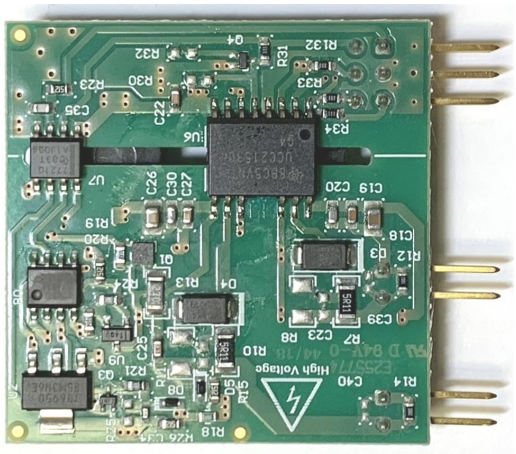


特長

- ハーフ・ブリッジ構成でSiC MOSFETを駆動するための、小型でデュアル・チャネルのゲート・ドライバ・ソリューション
- 4Aソースおよび6Aシンクのピーク電流駆動能力により、最高500kHzのスイッチング周波数でSiC MOSFET、Si MOSFET、IGBTを駆動するために好適
- 15Vと-4Vを出力する、小型、高効率の絶縁型バイアス電源を内蔵
- 柔軟で、ハーフ・ブリッジのデュアル・チャネル、パラレル、デュアル・ハイサイド、デュアル・ローサイドとして構成可能
- 2レベルのターンオフ回路を個別実装して短絡から保護し、電流制限と遅延(ブランキング)時間を調整可能
- 100V/nsを超える高いCMTIと、8kVピークおよび5.7kV RMS電圧の強化絶縁を実現

アプリケーション

- インバータとモーター制御
- オンボード・チャージャ (OBC) / ワイヤレス・チャージャ
- ガソリン / ディーゼル・エンジン・プラットフォーム
- DC/DC コンバータ



1 System Description

SiC MOSFETs are gaining popularity in many high-power applications due to their significant advantages of superior switching performance, higher dielectric-breakdown field strength, and higher ambient operating temperatures. The SiC MOSFET has been widely used in high-voltage, high-frequency, power electronic converters in the HEV/EV. Examples are high-voltage PFC converters, LLC, or phase-shifted full-bridge DC/DC converters, bidirectional DC/DC converters, high-voltage Flyback converters, and so on. Challenges are raised in the design of appropriate gate drivers. The characteristics of SiC MOSFETs require consideration of a gate-driver circuit that optimizes the switching performance of the SiC device.

- Gate voltage must be kept as high as possible, within the specified range, to operate the devices at a lower Rdson, so that the conduction losses can be minimized.
- The gate driver must have a low-propagation delay time and also a fast turn-on and turnoff slew rate. Low turn-on loss (Eon) and turnoff loss (Eoff) allow the device to operate at high-switching frequencies. SiC devices can be turned-on and turned-off within tens of nanoseconds, which largely depends on internal and external gate resistance.
- SiC MOSFETs are (normally off) voltage-controlled devices. The off and on gate voltages are normally in the range of 0 V and 20 V, respectively. A negative drive in the order of –5 V is preferred at the time of turning off the device, to ensure faster turnoff and to avoid faulty turn-on due to noise or ringing at the gate.

Considering the system requirements, many require reinforced isolation for safety reasons. A half-bridge configuration built in a compact board is usually preferred, because of ease of layout design and reduced parasitics. This reference design features the following benefits:

- Compact, dual-channel, gate-driver solution for driving SiC MOSFETs in half-bridge configuration
- 4-A source and 6-V sink peak-current driving capability suitable for driving SiC MOSFET, Si MOSFET, and IGBT, with switching frequency up to 500 kHz
- Built-in, compact, high-efficiency, isolated-bias supply, with 15 V and –4 V outputs
- Flexible and configurable as dual channel in half bridge, in parallel, dual high-side and dual low-side
- Gate-driver dead time control with shoot-through protection ensures safe operation
- Low-propagation delay ensures easy control and allows increased switching frequency
- Discrete, two-level turnoff for short-circuit protection, with adjustable current limit and delay (blanking) time
- Provide high CMTI of > 100 kV/µV and reinforced isolation of 8-kV peak and 5.7-kV RMS voltages

1.1 Key System Specifications

表 1 shows the key system specifications of this TI design. All functions are included on this board.

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	
Gate driver	Input voltage	3 V to 18 V
	Output PWM voltage	15 V and –4 V
	Drive currents	6-A peak sink and 4-A peak source
	Isolation	5.7 kVrms
		> 12.8 kV surge immunity
	CMTI	100kV /µs
Bias supply	Input voltage	5 V ±5%
	Output voltage	15 V and –4 V
Protection	Configurable DESAT detection with two-level turnoff	
	Configurable second turnoff level	
	UVLO to disable the gate driver	
Interface	Input signals	PWM, reset
	Output signals	Fault

2 System Overview

2.1 Block Diagram

図 1 shows the system block diagram. The design consists of four main functional elements:

- The isolated bias supply has integrated MOSFET switches and is based on a push-pull topology. The isolated bias supply drives the center tap transformers with approximately 50% duty cycle to transfer the power from the primary to the secondary.
- The dual-channel gate driver with reinforced isolation based on the UCC21530-Q1 device. The gate driver has the driving capability of 4-A source and 6-A sink peak current. The input side is isolated from the two output drivers by a 5.7-kV RMS reinforced isolation barrier, with a minimum of 100-V/ns CMTI.
- The short-circuit protection circuits include DESAT detection, two-level turnoff, and reset logic.
- The digital isolator is for signal isolation between the low-voltage side and high-voltage, gate-driver side. The digital isolator transfers the signals of fault and reset.

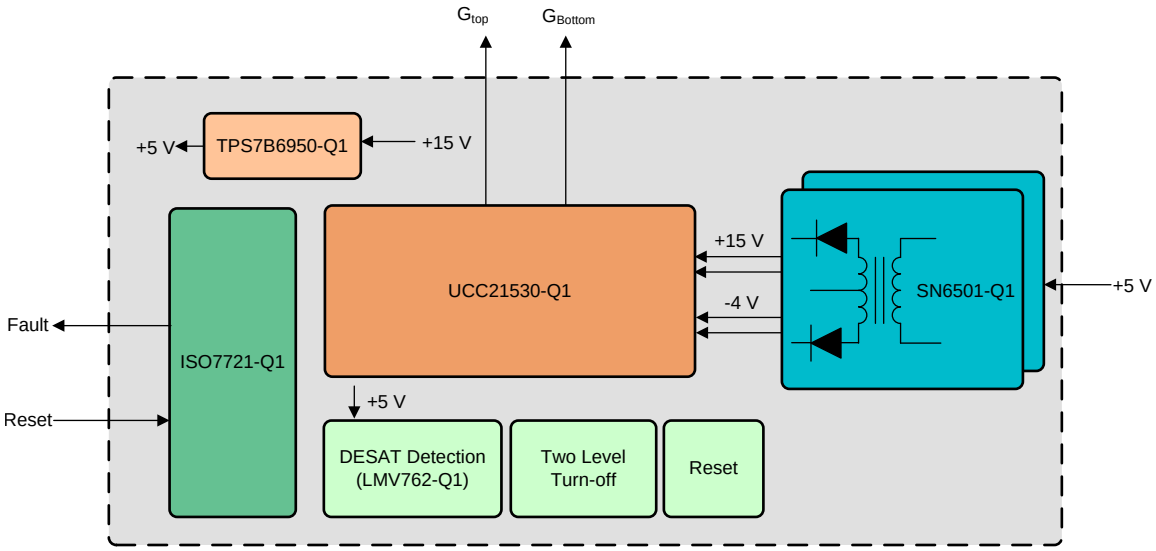


図 1. TIDA-01605 Block Diagram

2.2 Highlighted Products

The TIDA-01605 reference design features the following Texas Instruments devices.

2.2.1 UCC21530-Q1

The UCC21530-Q1 device is an automotive-grade, isolated, dual-channel, gate driver with 4-A source and 6-A sink peak current capability. The device is designed to drive power MOSFETs, IGBTs, and SiC MOSFETs. The input side is isolated from the two output drivers by a 5.7-kV RMS, 8-kV peak, reinforced, isolated barrier, with a minimum of 100-V/ns CMTI. The internal, functional isolation between the two secondary side drivers allows for a working voltage of up to 1.85-kV DC. The gate driver is also certified according to the various isolation standards of VDE, CSA, UL, and CQC. Each driver accepts VDD supply voltages up to 25 V and a wide input VCCI range from 3 V to 18 V. The UCC21530-Q1 device has programmable dead time (DT) control. A disable pin shuts down both outputs simultaneously when it is set high. The supply voltage on the secondary side has the under voltage lock-out (UVLO) protection of 12 V, which is important for driving SiC MOSFETs.

2.2.2 SN6501-Q1

The SN6501-Q1 device is a monolithic, push-pull, transformer driver, specifically designed for small factor, isolated power supplies. The device drives a low-profile, center-tapped transformer from a 3.3 V or 5-V DC power supply. The SN6501-Q1 device consists of an oscillator, followed by a gate drive circuit that provides the complementary output signals, with a 50% duty cycle to drive the ground-referenced N-channel power switches. The device includes two, 500-mA, peak MOSFET switches at 5-V input voltage, to ensure proper start-up under heavy loads.

2.2.3 ISO7721-Q1

The ISO7721-Q1 device is a dual-channel, digital isolator with 5-kV RMS isolation voltage. The device implements reinforced isolation, which is certified according to VDE, CSA, UL, and CQC standards. The ISO7221-Q1 device has an ON-OFF keying modulation scheme, to transmit the digital data across a silicon-dioxide-based isolation barrier. The device has a low-propagation delay of 11-ns typical, and a high CMTI of 100 V/ns. The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state.

2.2.4 LMV762Q-Q1

The LMV762Q-Q1 device is a precision comparator intended for applications requiring low noise and a low-input offset voltage. The device includes dual comparators in one package and features a CMOS input and push-pull output stage. The LMV762Q-Q1 device is designed to meet the demands of small size, low-power, and high-performance applications. The input offset voltage has a typical value of 200 µV at room temperature and a 1-mV limit overtemperature.

2.2.5 TPS7B6950-Q1

The TPS7B6950-Q1 is a low dropout linear regulator designed for up to 40V operations. It has typical 15 µA quiescent current at light load. The device is suitable for standby micro control-unit systems especially in automotive applications. TPS7B6950-Q1 features a thermal shutdown and an integrated short-circuit and overcurrent protection. It has an output current capability of 150 mA and offers fixed output voltage options.

2.2.6 TL431A-Q1

The TL431-Q1 device is a three-pin, adjustable, shunt regulator with specified thermal stability over applicable automotive temperature ranges. The TL431-Q1 device can be used as a single-voltage reference, error amplifier, voltage clamp, or comparator with integrated reference. The TL431-Q1 device consists of an internal reference and amplifier that outputs a sink current based on the difference between the reference pin and the virtual internal pin. The sink current is produced by the internal Darlington pair, which allows this device to sink a maximum current of 100 mA.

2.3 System Design Theory

2.3.1 Design of Push-Pull Power Supply

This section describes the steps to designing the push-pull bias supply. The push-pull converter based on the SN6501-Q1 device was selected to generate the bias power for the SiC isolated gate driver. The device has integrated MOSFET switches and drives the center-tap transformers, with approximately 50% duty cycle to transfer the power from the primary to the secondary[1].

One highlight of this part is that the positive temperature coefficient of these switches has a self-correcting effect on the V-t imbalance. During a slightly longer on time, the prolonged current flow through a MOSFET gradually heats the MOSFET, which leads to an increase in Rds(on). The higher resistance then causes the drain-to-source voltage to increase. Therefore, the voltage across the transformer winding is gradually reduced, hence the V-t balance is restored.

図 2 shows the design circuit. It consists of several discrete components: push-pull driver, transformer, rectifier diodes, as well as input and output capacitors.

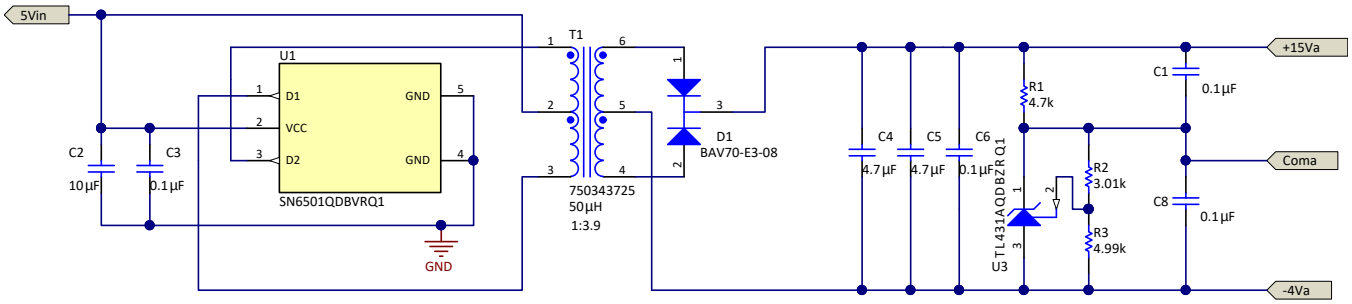


図 2. Isolated Push-Pull Power Supply Circuit

2.3.1.1 Transformer Design

The input peak current (Iin_peak) was calculated using 式 1. The factor 0.97 (η) accounts for typical transformer power-transfer efficiency.

$$I_{in\_peak} = \frac{P_{out\_max} / \eta}{V_{in\_min}} = \frac{1\,W / 0.97}{4.75\,V} = 217\,mA \quad (1)$$

Where:

- P_{out_max} is the maximum output power.
- V_{in_min} is the minimum input voltage.

The SN6501-Q1 device switches the internal dual MOSFETs with approximately 50% duty cycle each. Therefore, the AC current flowing through the transformer primary (I_{pri}) can be calculated from 式 2.

$$I_{pri} = \frac{I_{in\_peak}}{2} = \frac{217\,mA}{2} = 1108.5\,mA \quad (2)$$

The transformer turns ratio (N_{ps}) is calculated from 式 3.

$$N_{ps} = \frac{V_{prif}}{V_{sec} + V_f} = \frac{5\,V}{19\,V + 0.35\,V} = 1{:}3.87$$

Where:

- V_{sec} is the voltage across the secondary winding.
- V_f is the forward voltage of the diode.

- V_{pri} is the voltage across the primary winding. (3)

The V-t product of the transformer must be greater than Vt_{min} calculated using 式 4.

$$Vt_{min} = V_{IN\_max} \times \frac{T_{max}}{2} = \frac{V_{IN\_max}}{2 \times F_{min}} = \frac{5\ V \times 1.05}{2 \times 300\ kHz} = 8.75\ V\mu s \quad (4)$$

Where:

- V_{IN_max} is the maximum input voltage.
- F_{min} is the minimum switching frequency.

2.3.1.2 Rectifier Diode Selection

The rectifier diode at the secondary side is selected based on two criteria: low forward-voltage drop and short reverse-recovery time.

The forward current flowing through the diode is calculated using 式 5.

$$I_f = \frac{P_{out}}{V_{out}} = \frac{1\ W}{19\ V} = 53\ mA \quad (5)$$

The reverse blocking voltage of the diode (V_b) is calculated using 式 6.

$$V_b = V_{out} + V_{in} \times \frac{N_{sec}}{N_{pri}} = 19\ V + 5.5 \times \frac{3.87}{1} = 41\ V \quad (6)$$

Considering a safety margin on top, a 70 V, 250 mA diode is chosen.

2.3.1.3 Capacitor Selection

Two ceramic capacitors must be placed at the input of the SN6501-Q1 device. A ceramic bypass capacitor of 100 nF and a ripple filtering capacitor of 10 µF are connected in parallel and placed as close as possible to the Vcc pin.

The output capacitor is required for filtering the output ripple. The output ripple specification is calculated using 式 7.

$$\Delta V = V_{out} \times 10\% = 19\ V \times 1\% = 0.19\ V \quad (7)$$

The required peak current which is delivered to the gate driver is 4 A according to the UCC21521-Q1 data sheet. The required capacitance is calculated using 式 8.

$$C \geq \frac{I_{peak} \times dt}{\Delta V} = \frac{Q_g}{1.9\ V} = 184\ nF \quad (8)$$

Considering it could also be used to drive SiC MOSFETs with a higher total gate charger, a total of three 4.7-µF ceramic capacitors are connected in parallel between the supply output and gate driver.

2.3.1.4 Generation of Negative Supply

The power-supply output is separated into the positive rail of 15 V and the negative rail of –4 V. The design implements the TL431-Q1 device, which reacts at a shunt regulator. 図 3 shows the schematic.

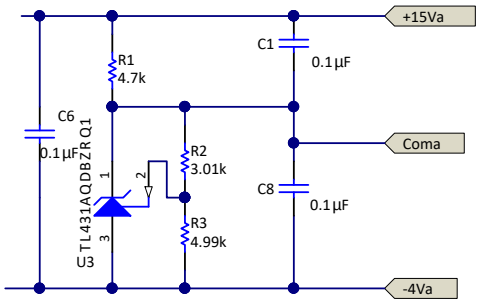


図 3. Generation of Negative Rail

To program the cathode voltage to a regulated voltage, a resistive bridge is shunted between the cathode and anode pins, with the mid-point tied to the reference pin. The cathode voltage is calculated using 式 9.

$$V_{neg} = \left(1 + \frac{R_2}{R_3}\right) \times V_{ref} = \left(1 + \frac{3.01\,k\Omega}{4.99\,k\Omega}\right) \times 2.5\ V = 4\ V \tag{9}$$

For 式 9 to be valid, the TL431-Q1 device must be fully biased, so that it has enough open loop gain to mitigate any gain error. The cathode current is set using 式 10.

$$I_{cat} = \frac{V_{out} - V_{neg}}{R_1} = \frac{19\ V - 4\ V}{4.7\ k} = 3.2\ mA \tag{10}$$

2.3.2 Design of Isolated Gate Driver

The isolated gate driver consists of a dual channel that can be configured in either two low-side gate drivers or one half-bridge gate driver. The gate driver contains 5.7-kVrms isolation capability between the primary and secondary side of the gate driver[2] . 図 4 shows the schematic of the gate driver and the associated components implemented for half-bridge configuration.

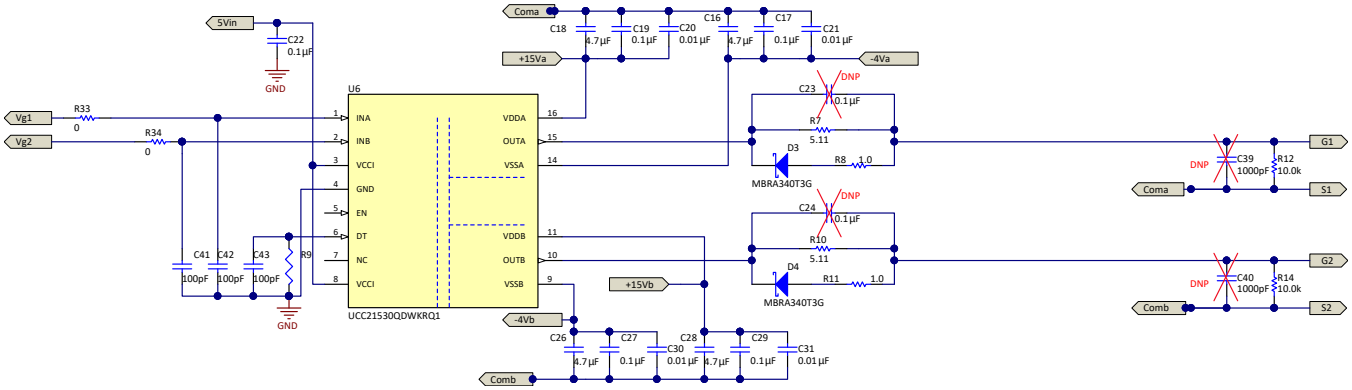


図 4. Isolated Gate Driver Circuit

2.3.2.1 Gate Driver Power Losses and Temperature Rise

The power losses of the UCC21521-Q1 device determine the thermal safety-related limits. The power losses consist of the static power loss P_{GDQ}, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. Values of the static current flowing into the V_{CCI} pin (I_{VCCI}), V_{DDA} pin (I_{DDA}), and V_{DDB} pin (I_{DDB}) are extracted from the data sheet. In this design V_{VCCI} = 5 V and V_{VDD} = 19 V. Therefore the power losses are calculated using 式 11.

$$P_{GDQ} = V_{VCCI} \times I_{VCCI} + V_{VDDA} \times I_{DDA} + V_{DDB} \times I_{DDB} = 72\ mW \tag{11}$$

From the data sheet of the C3M0065100K SiC MOSFET, the total gate charge is QG_{tot} = 35 nC. The switching frequency is assumed to be 200 kHz. The switching losses from the gate driver are calculated using 式 12.

$$P_{GSW} = 2 \times V_{DD} \times Q_G \times F_{SW} = 2 \times 24\ V \times 35\ nC \times 200\ KHz = 336\ mW \quad (12)$$

Therefore, the total losses, P_{tot}, are summed to be 408 mW. The temperature rise of the UCC21521-Q1 device is calculated using 式 13.

$$T_J = T_{Board} + R_{\theta JB} \times P_{tot} = 35°C + 32.1 \times 408\ mW = 48°C \quad (13)$$

2.3.2.2 Short Circuit Detection

The short-circuit behavior of the SiC MOSFET is similar to that of the conventional Si IGBT. Therefore, the de-sat protection circuit is similar. The main difference is that response time of the protection circuit is highly critical for the short-circuit protection of SiC MOSFETs due to the limited short circuit withstand time.

図 5 shows the schematic for the SiC MOSFET, short-circuit detection. The high-voltage diode, D6, interacts with the drain pin of the MOSFET where pulsed high voltage appears. The detection circuit functions only during the on-state of the SiC MOSFET, when the gate signal is 15 V.

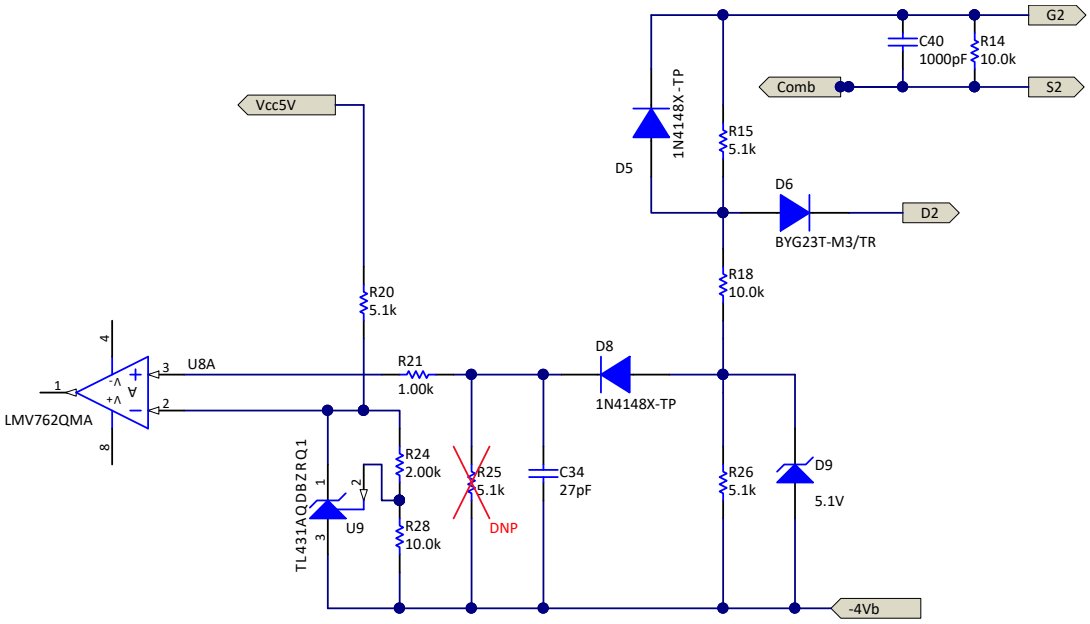


図 5. Short-Circuit Detection Circuit

The process of short-circuit protection mainly consists of three sub-periods: blanking time, delay, and two-level turnoff. At the start of the short circuit, the current flowing in the MOSFET channel increases dramatically until saturation, and the voltage from drain-to-source also increases and can reach up to the DC bus voltage. During this transient, the SiC MOSFET is turned-on, and the lower section of the resistive divider (R18 and R26) is in parallel with the drain-to-source channel. The detection circuit starts to sense the voltage of Vds + 4 V when the driver output is high (+15 V). G2 is 15-V. Refer to S2. D6 is forward biased during this period. The Anode voltage of D6 becomes Vds plus the forward voltage drop of D6. Assume that Vds is 5.2 V, hence Anode voltage of D6 is 5.9 V referring to S2 and 9.9 V referring to -4 V. Consider the resistive divider R18 and R26 (R25 is not populated), the built-up voltage across C34 (V_{sense}) is calculated as:

$$V_{sense} = 9.9\,V \times R_{26} / (R_{18} + R_{26}) - V_{fD8} = 3V \quad (14)$$

This voltage is referred to -4 Vb, and it is compared with the voltage reference, which is set as 3 V by the precision shunt regulator, TL431A-Q1. When the voltage becomes higher than the reference, the comparator, LMV762, sends the flag out and triggers the protection stage. As the result, the Vds threshold for protection is approximately 10.3 V with the designed parameters shown in 図 5.

2.3.2.3 Two-Level Turnoff Protection

In the event of a short-circuit or overcurrent in the load, a large voltage overshoot occurs across the SiC MOSFETs when it is hardly turned off. The overshoot can exceed the SiC MOSEFT breakdown voltage and destroy the switch. By introducing an additional turnoff voltage level at the gate driver output in between ON and OFF level before it is completely turned off, the SiC MOSFET channel current is limited and the drain to source voltage overshoot is greatly reduced. This process ensures that the SiC MOSFET operates at its safe region. The required timing between the first and the second voltage levels is depending on the stray inductance and the di/dt slew rate at the beginning of the interval. TIDA-01605 implements a low cost, flexible, discrete circuit to realize this function.

After a short-circuit is detected, the two-level turnoff process starts. 図 6 shows the complete circuit. When the voltage threshold is triggered, the first comparator (U8A) turns on Q2. Hence, 5 V is seen on the gate of Q1, and Q1 is conducted. The gate capacitor starts exponentially discharging through R13 and C25, and the termination voltage is calculated using 式 15.

$$V_{term} = \left(V_{gate} - V_b\right) \times \frac{R13}{R10 + R13} - V_b = \left(15\ V + 4\ V\right) \times \frac{27\ \Omega}{5.1\ \Omega + 27\ \Omega} - 4\ V = 11.9\ V \quad (15)$$

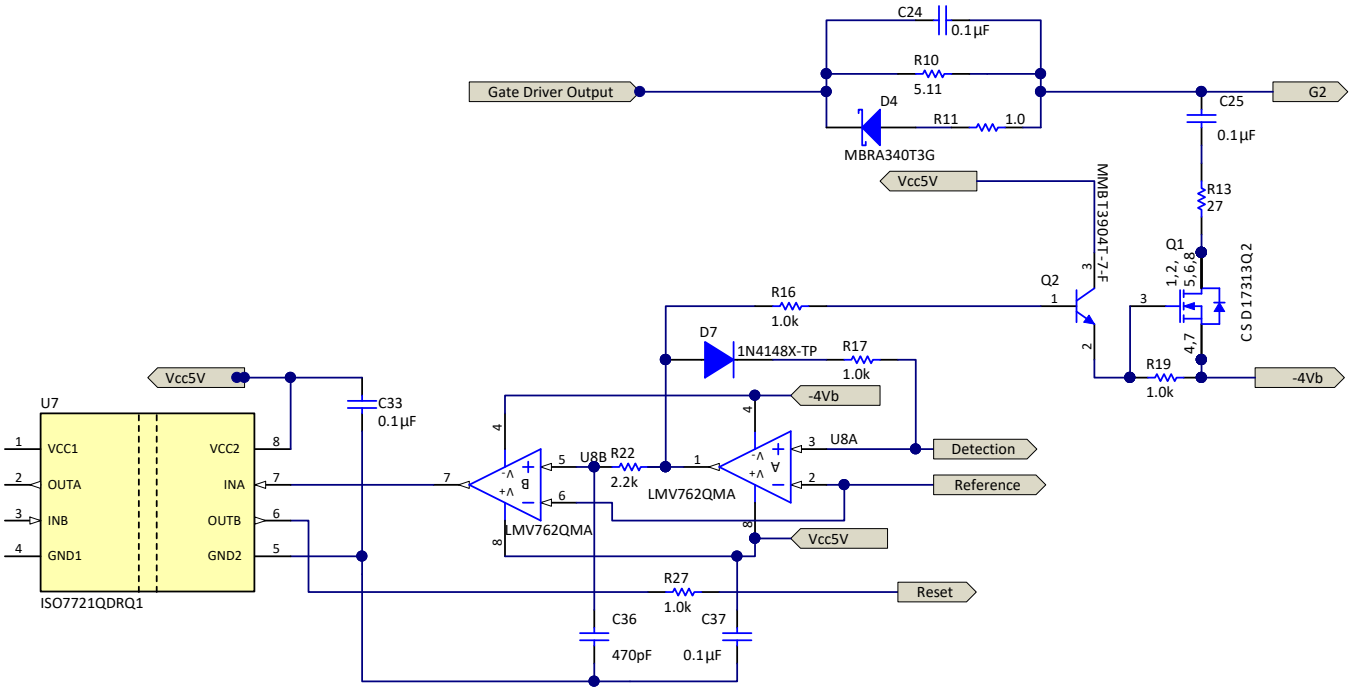


図 6. Two-Level Turnoff Schematic

After the gate voltage has reached 5.5 V, the second-level turnoff process starts. This process is triggered by the output of the second comparator, U8B. This signal first goes through a delay time which is set by R22 and C36 using 式 16.

$$T_{delay} = R_{22} \times C_{36} = 2.2\ k\Omega \times 470\ pF = 1.03\ \mu s \quad (16)$$

After the delay time, U8B is triggered. The U8B output is connected to the Enable pin of the UCC21521-Q1 gate driver. As a result, the gate driver output is pulled down to the –4 V, and the SiC MOSFET gate is discharged to the same voltage level.

The two-level turnoff circuits for the short-circuit scenario are simulated. The model of the C3M0065100k is implemented. The top graph of 図 7 shows the current flowing from the drain-to-source of the SiC MOSFET. The bottom graph of 図 7 shows the gate-to-source voltage of the SiC MOSFET. As shown, the current reaches 150-A peak in 135 ns, and the SiC MOSFET enters its desaturation region. The top graph of 図 8 shows the voltage across R26 (see 図 6), which proportionally corresponds to the drain-to-source voltage of the SiC MOSFET. As shown, the first-level turnoff occurs when the voltage reaches around –200 mV, and the second-level turnoff occurs after the 1-µs delay time, which is set by R22 and C36.

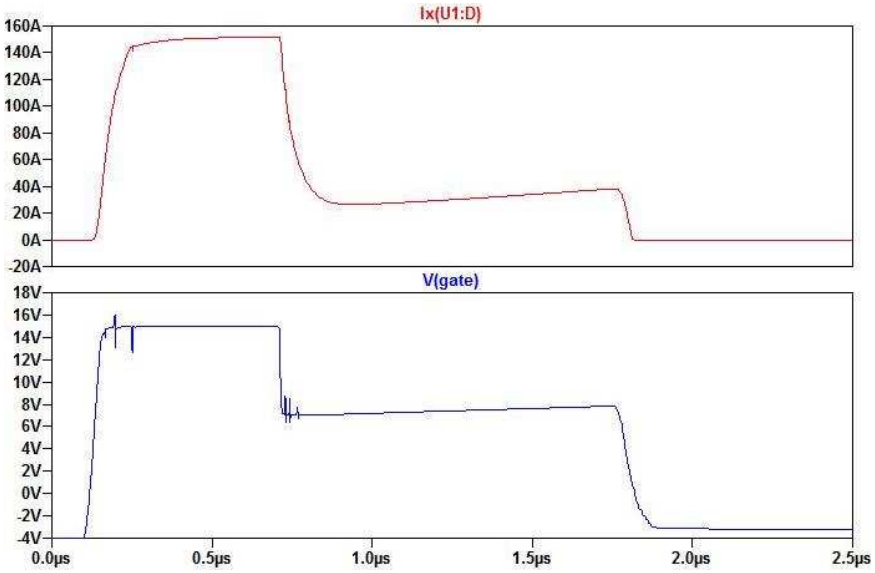


図 7. Simulated Drain-to-Source Current During Two-Level Turnoff

注: Top graph – Short-circuit current flowing from drain-to-source of the SiC MOSFET

Bottom graph – voltage at the SiC MOSFET gate

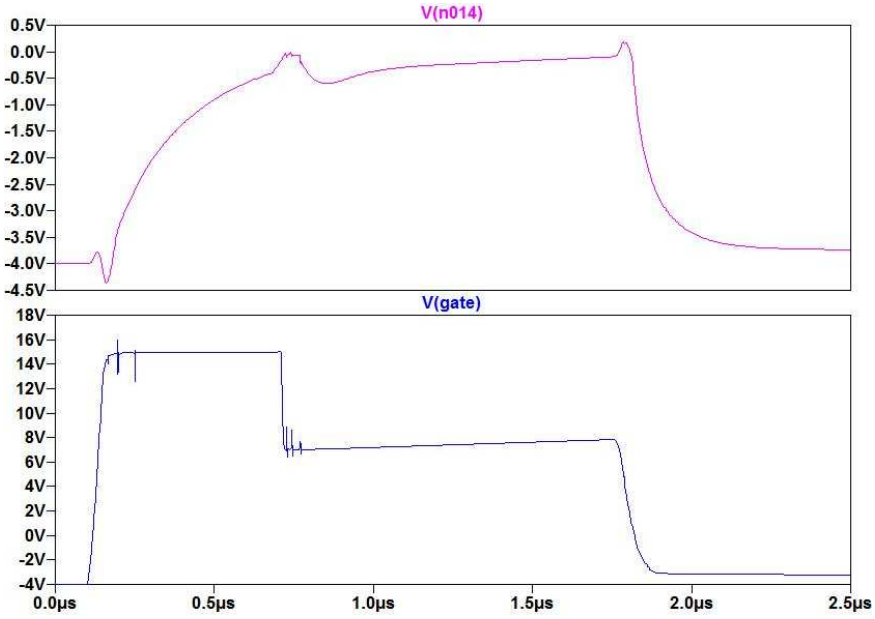


図 8. Simulated Drain-to-Source Voltage Increase During Two-Level Turnoff

注: Top graph – voltage across R26 in the detection circuit

Bottom graph – voltage at the SiC MOSFET gate

2.3.3 Digital Isolator

The digital isolator, ISO7721-Q1, is implemented for signal isolation between the low-voltage side and high-voltage side gate driver. The ISO7721-Q1 device includes one input channel and one output channel, and both transfer signals in unidirection[3]. Channel A accepts the fault signal after a short circuit happens and disables the gate driver at the primary side. Channel B accepts the reset signal from the MCU and sends it to the gate-driver secondary side. The isolator is chosen according to IEC61800-5-2 standards for reinforced isolation. The ISO7721-Q1 device can withstand 5-kV RMS voltage isolation and a CMTI of 100 V/ns.

図 9 shows the implemented circuit. A logic circuit (Q4, R30, R31, and R32) is implemented to invert the Fault flag logic, in case a gate driver with inverting Enable logic (for example, UCC21521-Q1) is used.

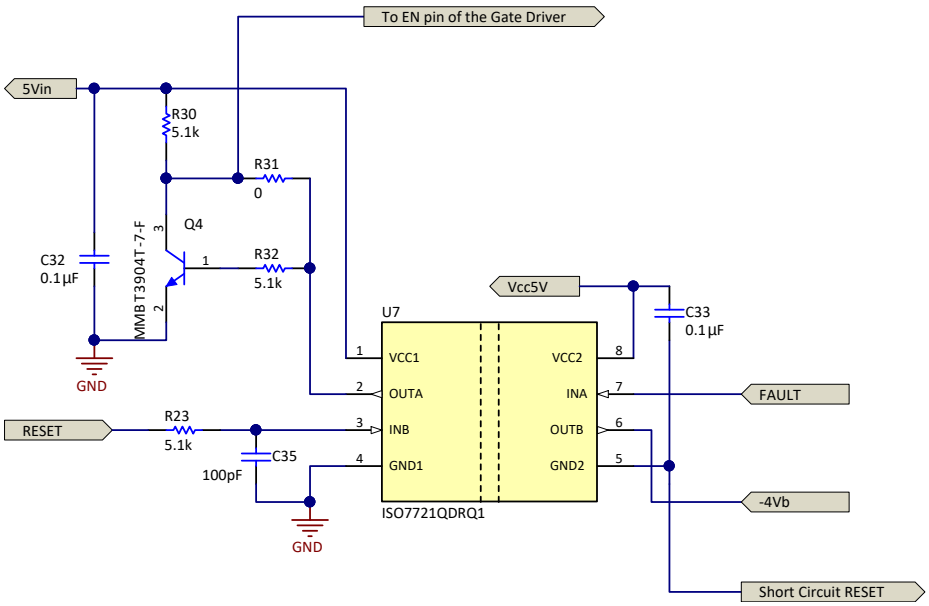


図 9. Digital Isolator Circuit

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

図 10 and 図 11 show the PCB image of the TIDA-01605 from the top side and bottomed side, respectively. Two connectors are intended for connecting the gate-to-source of the high-side SiC MOSFET and low-side MOSFET, respectively. One connector is intended for connecting the low-voltage control signals.

The isolated gate driver, digital isolator, LDO, and comparator are placed on the top side. The transformer driver and the isolation transformer are placed at the bottom side.

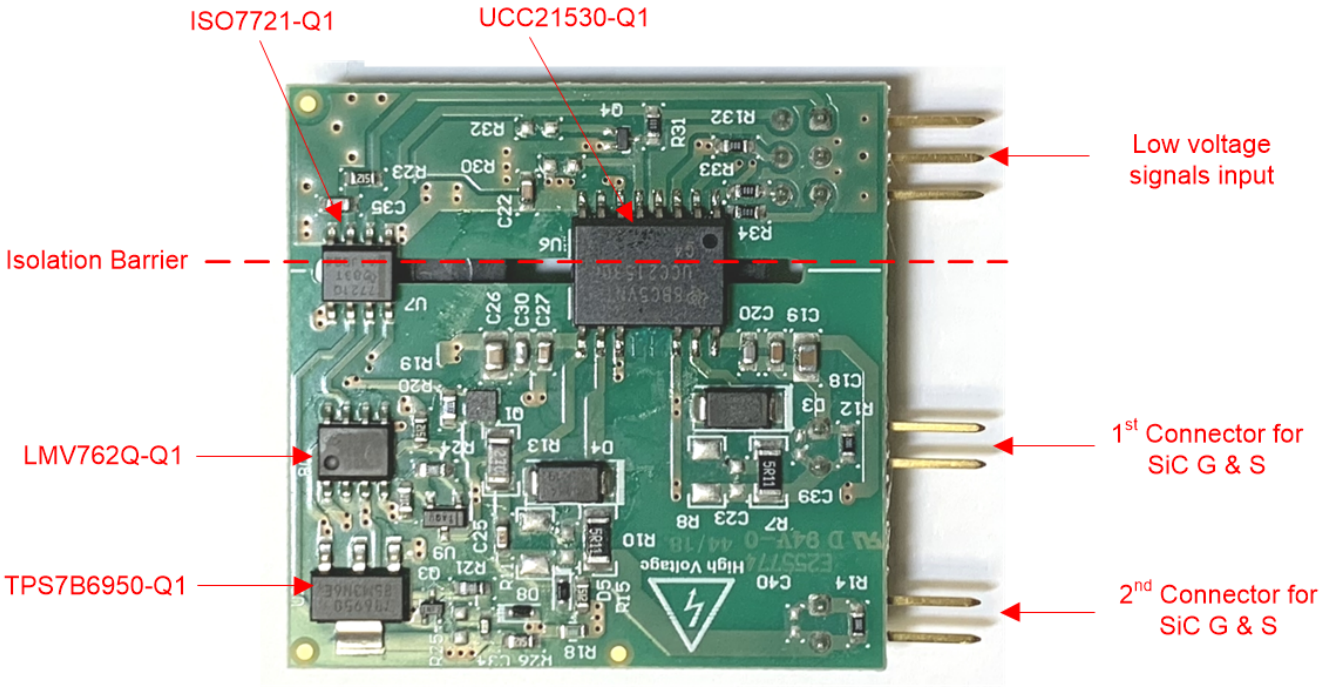


図 10. TIDA-01605 PCB Board (Top Side)

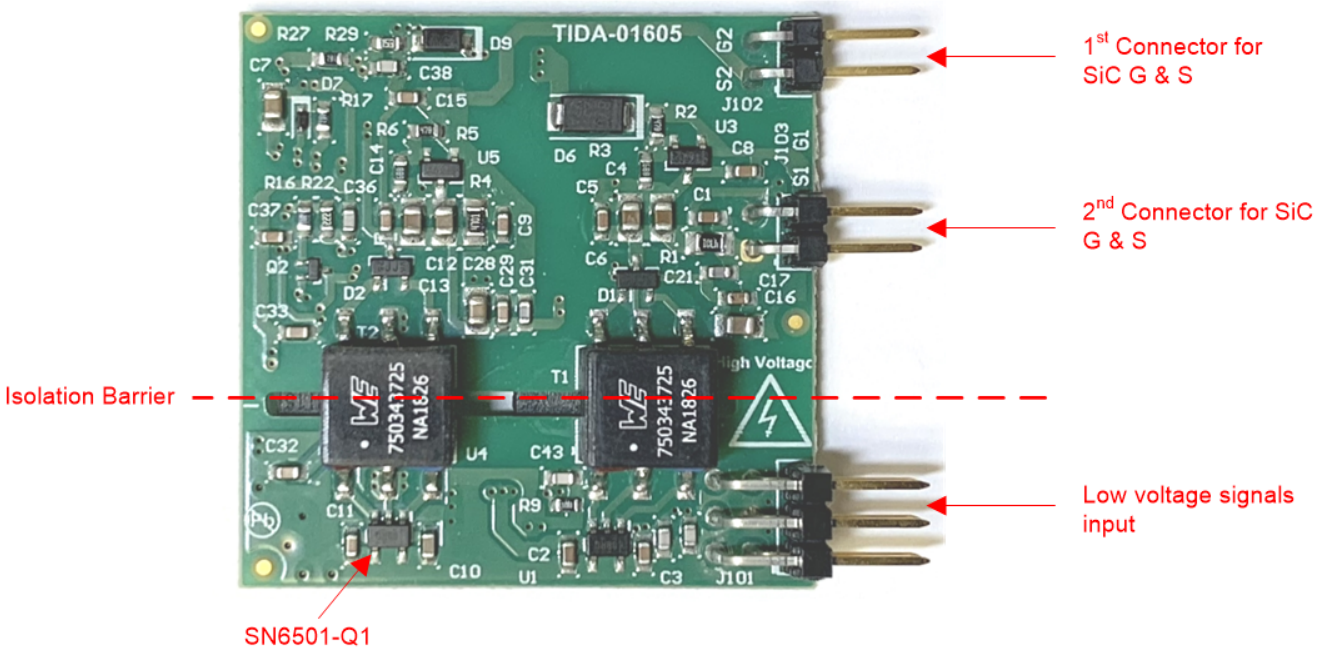


図 11. TIDA-01605 PCB Board (Bottom Side)

3.2 Testing and Results

3.2.1 Bias Supply

This section shows the measured waveforms of the isolated, gate-driver, bias supply, which is the open-loop, push-pull converter based on the SN6501-Q1 device.

3.2.1.1 Start Up

図 12 shows the start-up waveform of the 15-V power rail. The soft start takes about 140 ms.

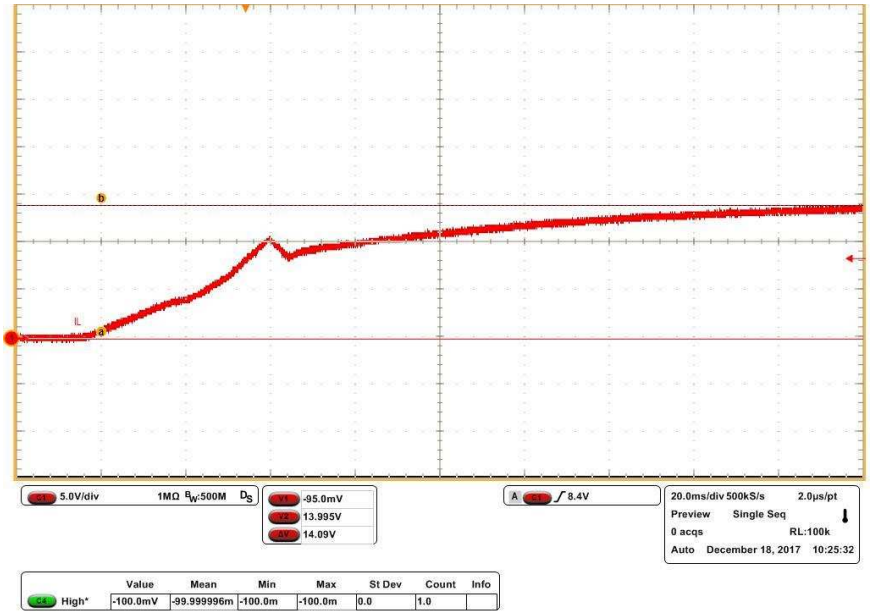


図 12. Start-Up Waveform of 15-V Power Rail

図 13 shows the start-up waveform of the –4-V power rail. The soft start takes about 20 ms.

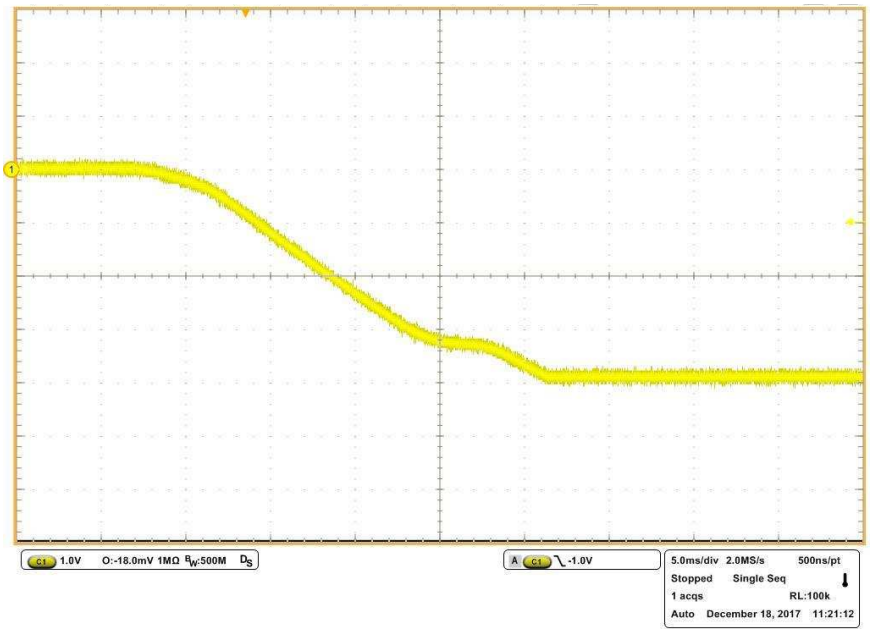


図 13. Start-Up Waveform of –4-V Power Rail

3.2.1.2 Power Down

図 14 shows the power-down waveform of the 15-V power rail. The power down takes about 300 ms.

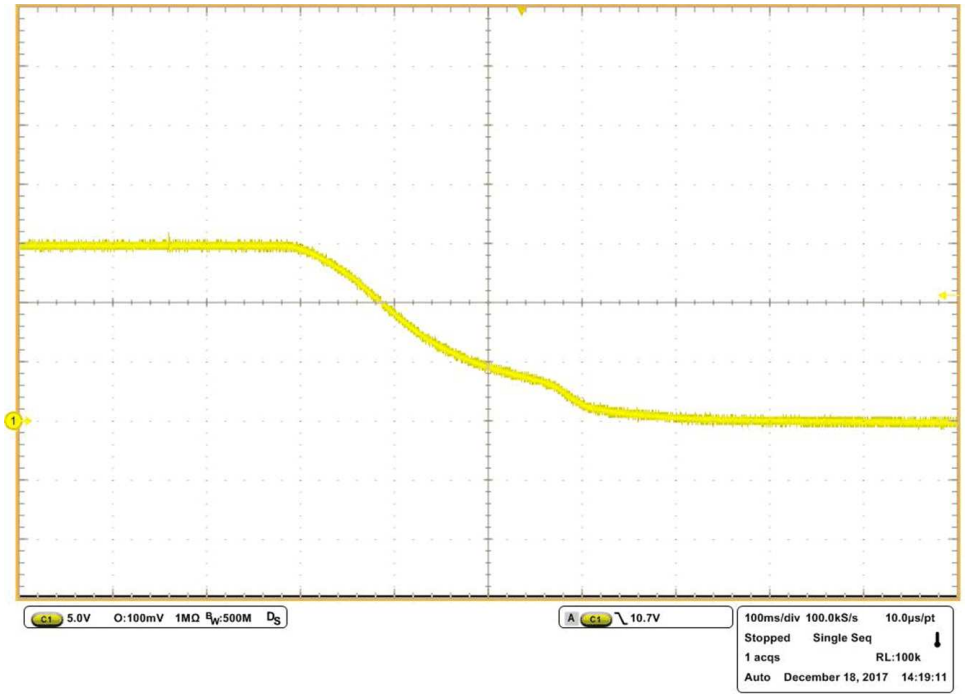


図 14. Power-Down Waveform of 15-V Power Rail

図 15 shows the power-down waveform of the –4-V power rail. The power down takes about 200 ms.

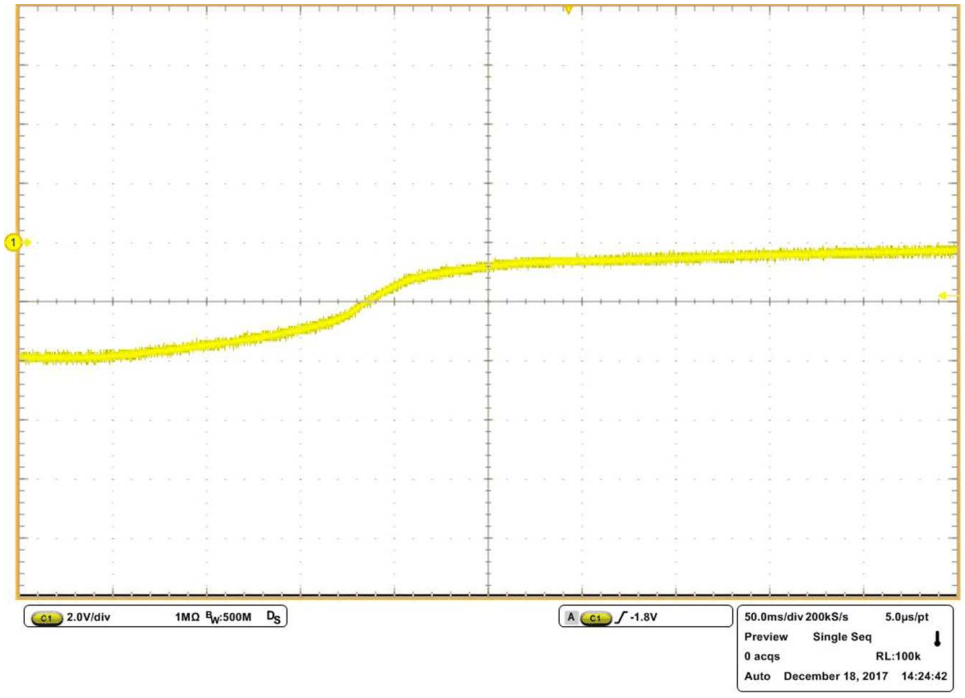


図 15. Power-Down Waveform of –4-V Power Rail

3.2.1.3 Load Transient

The load transient response presents how well a power supply copes with the changes in the load current demand. 図 16 shows the load transient response of the 15-V voltage rail. The load is switching from 0 to 5 mA, with a period of 30 ms and a 50% duty cycle. The voltage dip is around 170 mV, because the converter implements open loop control.

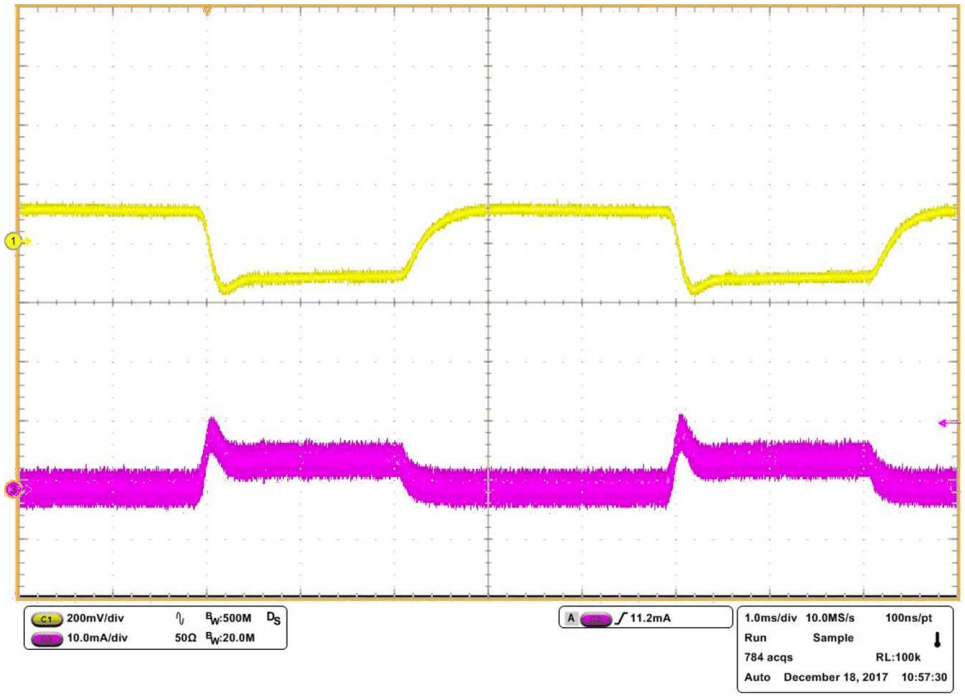


図 16. Load Transient Response of 15-V Power Rail (Load Switching From 0 to 5 mA)

3.2.2 Isolated Gate Driver

3.2.2.1 Input and Output PWM Switching

図 17 shows the PWM switching waveforms at the input and output of the isolated gate driver, UCC21530-Q1. The output voltage levels of the PWM signals follow the bias supply voltages (15 V and –4 V).

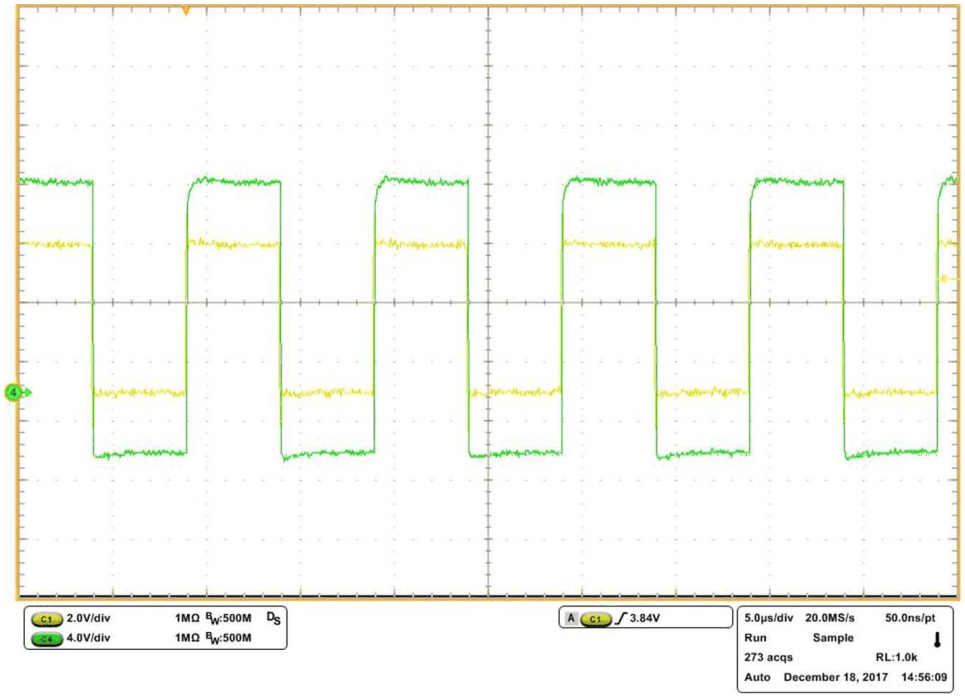


図 17. Gate Driver Input and Output PWM Switching Waveforms

注:

- CH1: PWM signal at the input of the UCC21530-Q1 device
- CH2: PWM signal at the output of the UCC21530-Q1 device

3.2.2.2 Propagation Delay Waveforms

Propagation delay is measured from the primary side to the secondary side of the UCC21530-Q1 device, as shown in 図 18. The gate driver drives the C3M0065100K SiC MOSFET, which was selected from the company Wolfspeed.

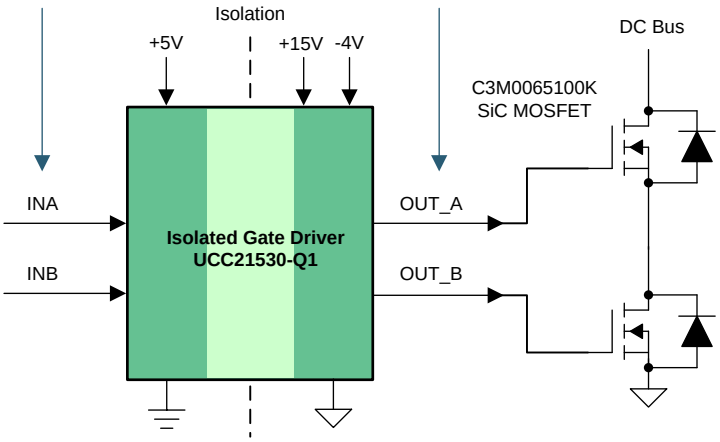


図 18. Test Circuit for Propagation Delay of UCC21530-Q1

図 19 shows the propagation delay time of the rising slope. As shown, 23-ns delay time is generated.

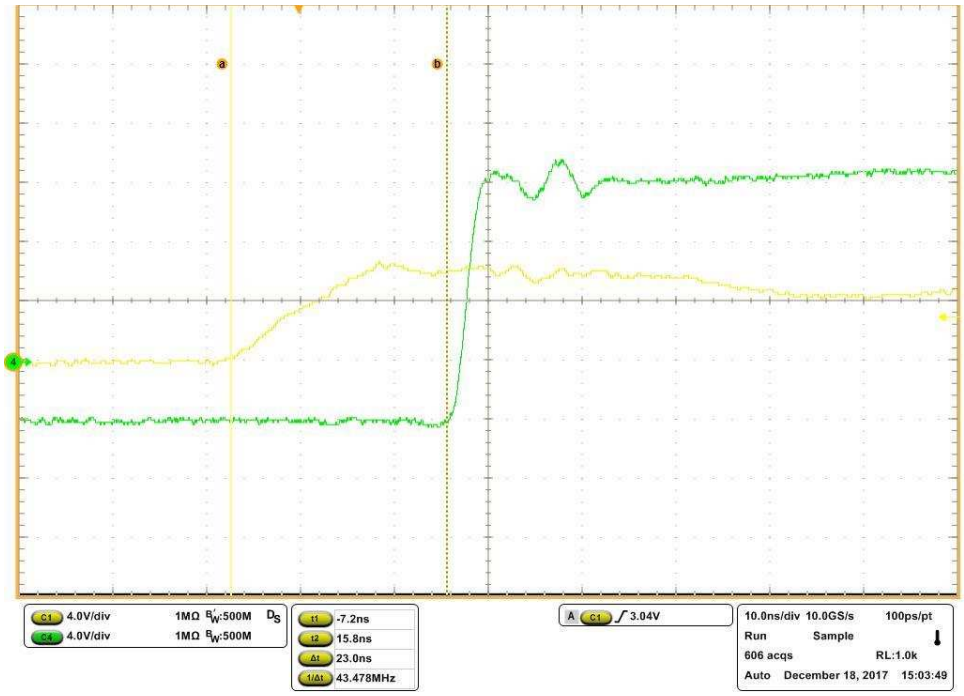


図 19. Propagation Delay of Rising Slope

注: From left to right:
- CH1: PWM signal from primary side of the UCC21530-Q1 device
- CH4: PWM signal from the secondary side of the UCC21530-Q1 device

図 20 shows the propagation delay time of the falling slope. As shown, 27.6-ns delay time is generated.

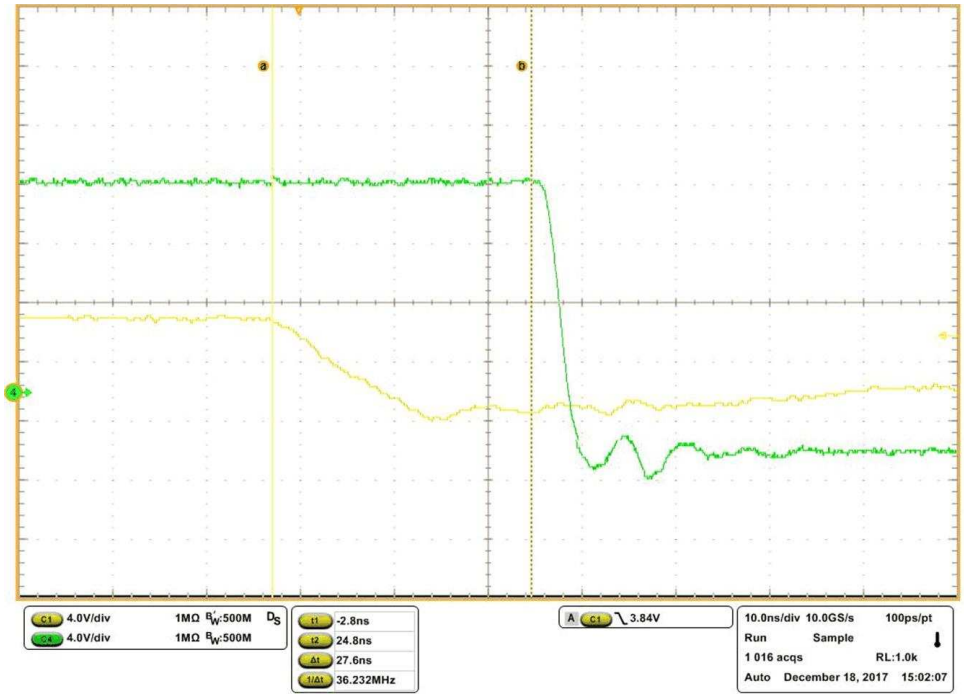


図 20. Propagation Delay of Falling Slope

注: From left to right:

- CH1: PWM signal from primary side of the UCC21530-Q1 device
- CH4: PWM signal from the secondary side of the UCC21530-Q1 device

3.2.3 Two-Level Turnoff, Short-Circuit Protection Test

The two-level turnoff circuit for short-circuit protection is tested under low voltage and with a high-voltage DC bus, respectively.

3.2.3.1 Testing Under Low Voltage

The two-level turnoff circuit is tested under low voltage for a functional check, where a 20-Ω dummy load is connected from the SiC MOSFET drain-to-source. Then from an external lab supply, a 15-V external voltage is applied from the drain-to-source. 図 21 shows the measured waveforms. After the drain-to-source voltage reaches the programmed threshold (around 7.9 V), the gate driver starts the two-level turnoff process, as shown from CH1.

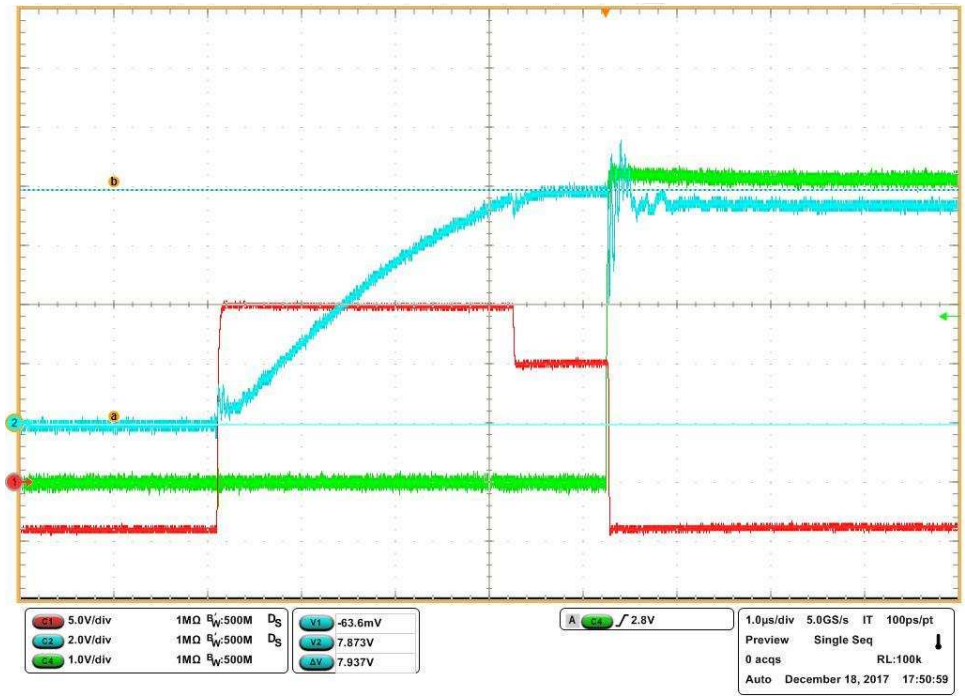


図 21. Two-Level Turnoff Waveforms Under Low-Voltage Testing

注: From the left side, top to bottom:

- CH2: Drain-to-source voltage of the SiC MOSFET
- CH4: Fault input on the Enable pin of the UCC21530-Q1 device
- CH1: Gate-to-source voltage of the SiC MOSFET

図 22 shows the duration of the first-level, turnoff process. The duration lasts for 968 ns.

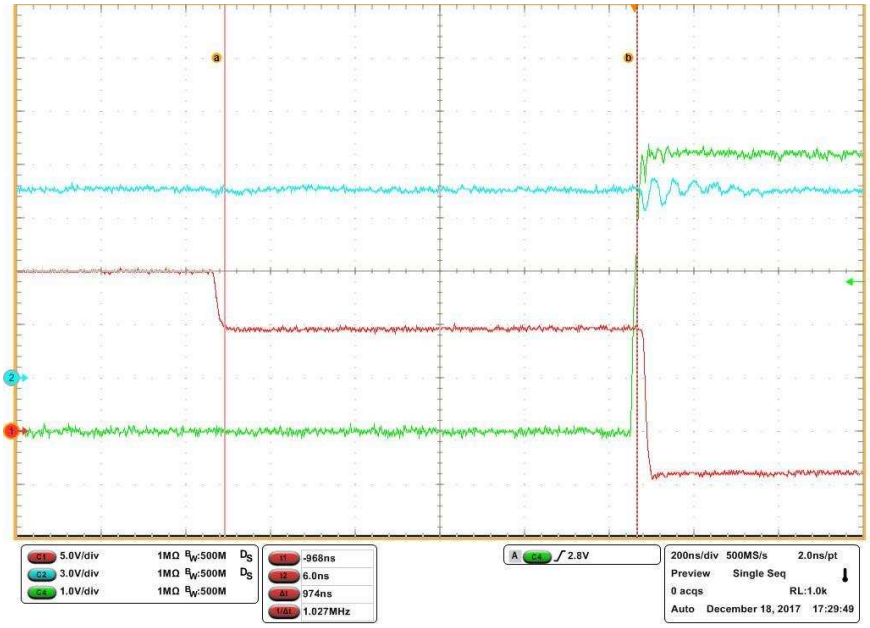


図 22. Time Period of First-Level, Turnoff Process

図 23 shows the propagation delay time from when the signal reached the Enable pin of the UCC21530-Q1 device, to when the gate starts the second-level turnoff. A 25-ns delay time is generated.

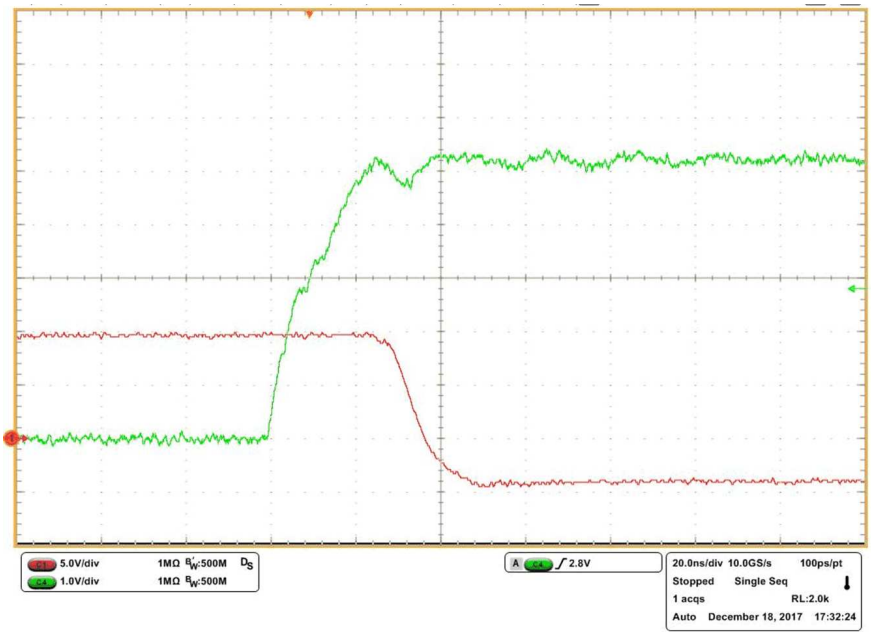


図 23. Propagation Delay From Enable Pin of UCC21530-Q1 to SiC MOSFET Gate

注:

- CH4: Enable pin of the UCC21530-Q1 device
- CH1: SiC MOSFET gate-to-source voltage

3.2.3.2 Testing Under High-Voltage DC Bus

The two-level turnoff waveforms during short circuit protection are verified at high voltages. 図 24 shows the waveforms under a 100-V input DC bus voltage. For load current the measurement is done from the voltage across a 0.1 Ohm shunt resistor, which results in 100A/div by translating it into current.

When the short-circuit failure occurs, the load current increases rapidly to around 180 A, where the SiC MOSFET enters its desaturation region. At the same time, it triggers the short-circuit detection threshold. After the programmed delay time, the gate-to-source voltage drops to its second turnoff level, which is around 12 V. Because of the two-level turnoff process, the drain-to-source overshoot at both turnoff transients has been significantly decreased. At first-level turnoff, the overshoot is suppressed to 150 V, and at the second-level turnoff it is suppressed to 170 V. The duration of the first-level, turnoff process is around 0.6 µs, and the duration of the second-level, turnoff process is 1 µs.

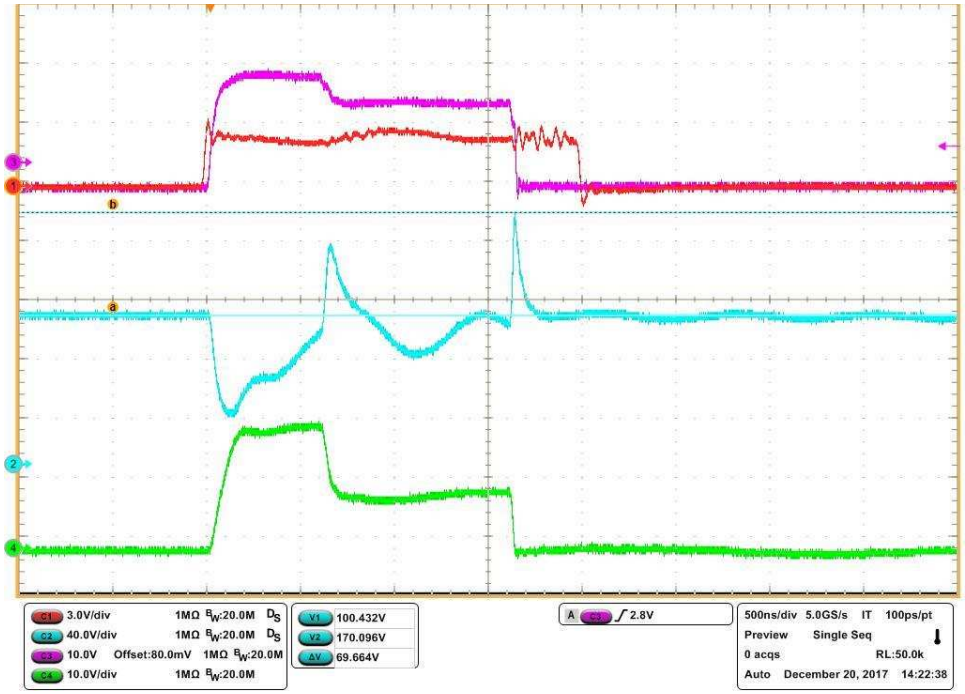


図 24. Two-Level Turnoff Waveforms Measured Under 100-V DC Bus Voltage

注: From top to bottom:

- CH3: Gate-to-source voltage
- CH1: Input PWM signal
- CH2: Drain-to-source voltage of the SiC MOSFET
- CH4: Load current scale in 100 A/div

図 25 shows the waveforms under 600-V input DC bus voltage. For load current, the measurement is done from the voltage across a 0.1-Ω shunt resistor, which results in a 100 A/div scale on the oscilloscope screen, by translating it into current.

The short-circuit current reaches 180 A, and the SiC MOSFET drain-to-source overshoot at first-level turnoff is 660 V, and at the second level the turnoff is 682 V.

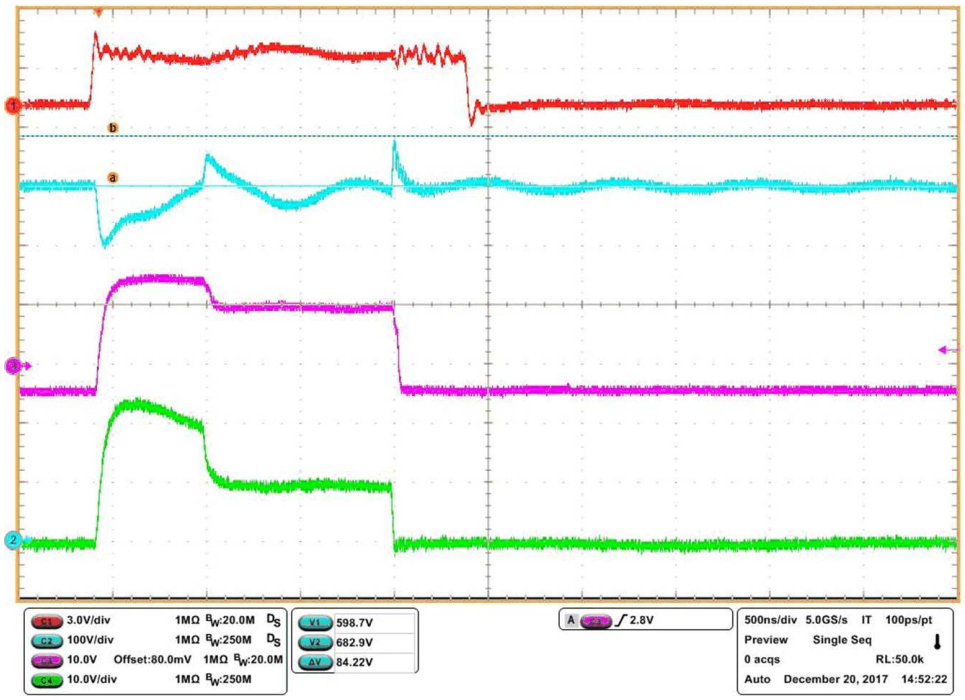


図 25. Two-Level Turnoff Waveforms Measured Under 600-V DC Bus Voltage

注: From top to bottom:

- CH3: Gate-to-source voltage
- CH1: Input PWM signal
- CH2: Drain-to-source voltage of the SiC MOSFET
- CH4: Load current

3.2.4 Reset

図 26 shows the test circuit for measuring the propagation delay of the Reset signal. The test circuit includes the main functional block diagrams in this reference design. The delay time is measured from the Reset signal sent from MCU, to the signal sent to the INB pin of the ISO7721-Q1 device, to the signal received at the Enable pin of the UCC21530-Q1 device.

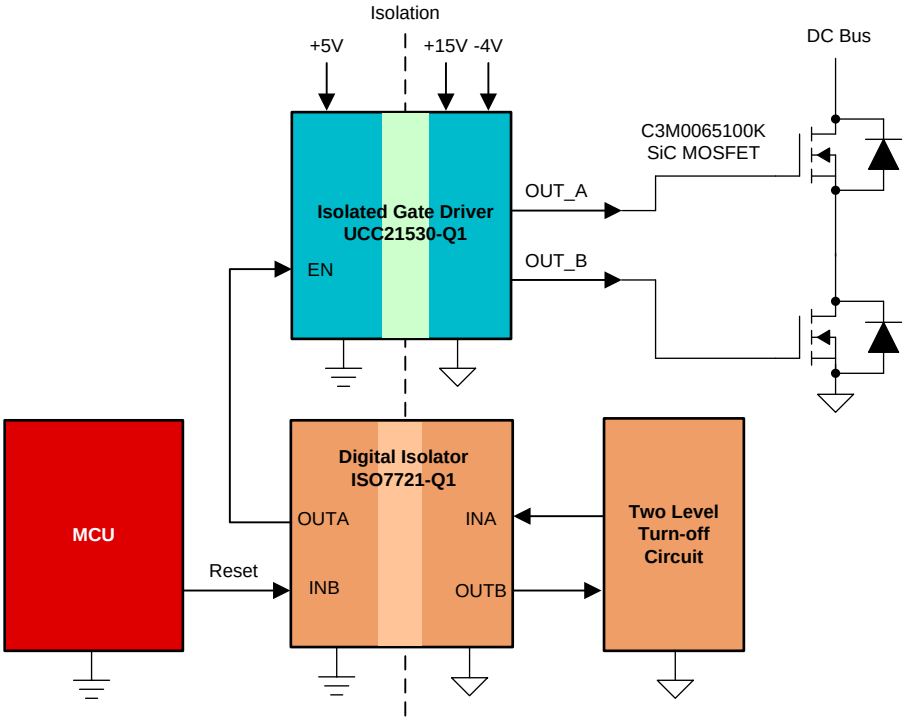


図 26. Test Circuit for Measuring Propagation Delay of Reset Signal

図 27 shows the measured waveform. A 1.26-µs delay time is generated.

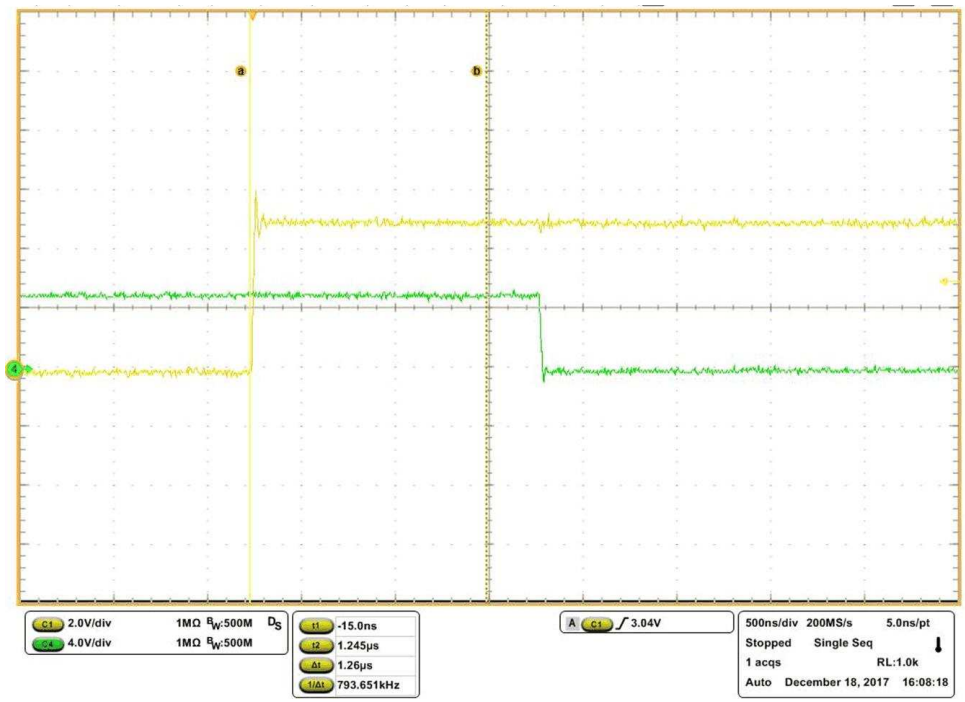


図 27. Propagation Delay of Reset Signal From MCU to Enable Pin of UCC21530-Q1

注: From top to bottom:
- CH1: Reset signal sent from MCU
- CH4: Reset signal received at the enable pin of the UCC21530-Q1 device

3.2.5 Thermal Images

The thermal image of the design board is measured under different PWM switching frequencies. The circuit runs at room temperature for 30 minutes.

3.2.5.1 200-kHz Switching Frequency

The gate driver is loaded with a 1-nF capacitor and switched at 200 kHz. 図 28 shows the thermal image of the top side of the board. The temperature of the overall board is maintained at less than 42.3°C.

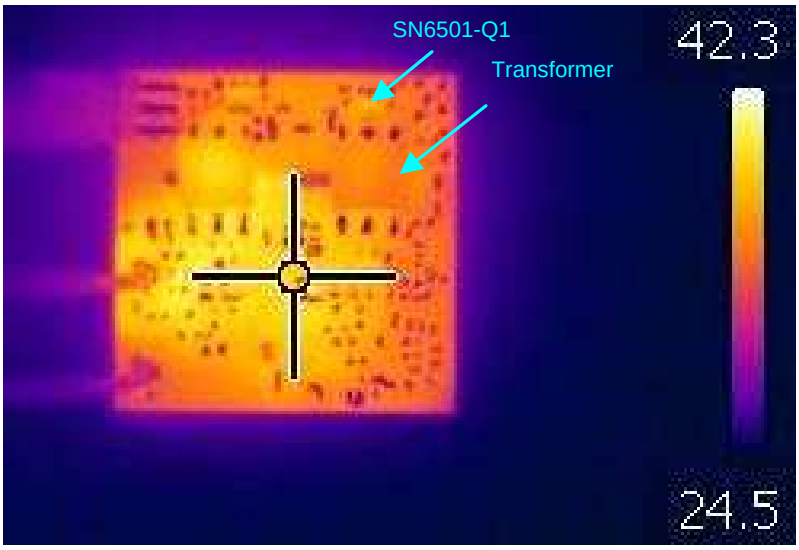


図 28. Thermal Image of Board (Top Side) at 200-kHz Switching Frequency

図 29 shows the thermal image of the bottom side of the board. The temperature of the overall board is maintained at less than 42.3°C.

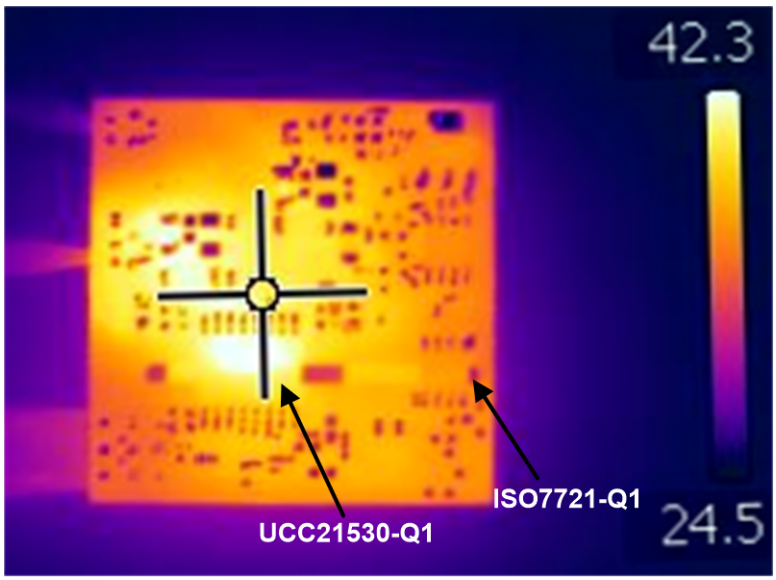


図 29. Thermal Image of Board (Bottom Side) at 200-kHz Switching Frequency

3.2.5.2 500-kHz Switching Frequency

Next, the thermal image is measured when PWM switching frequency is increased to 500 kHz. The gate driver remains loaded with 1 nF. 図 30 shows the thermal image of the top side of the board. The temperature of the overall board is maintained at less than 47°C.

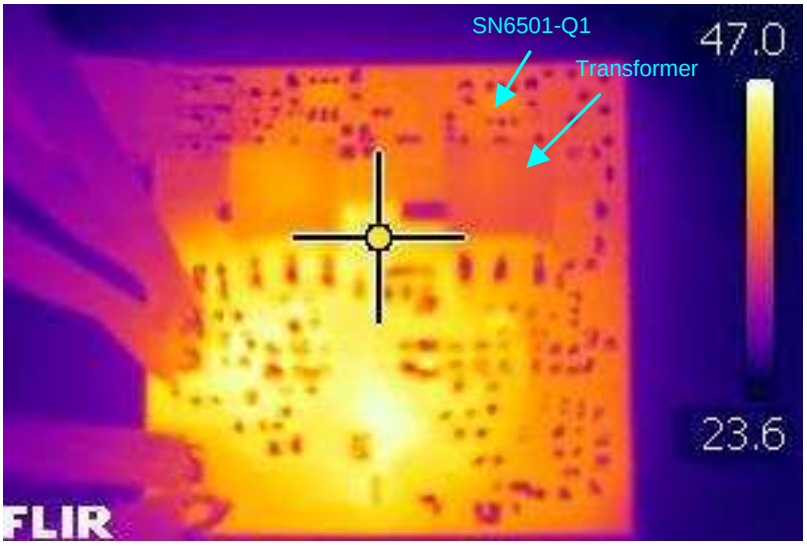


図 30. Thermal Image of Board (Top Side) at 500-kHz Switching Frequency

図 31 shows the thermal image of the bottom side of the board. The temperature of the overall board is maintained at less than 57.9°C.

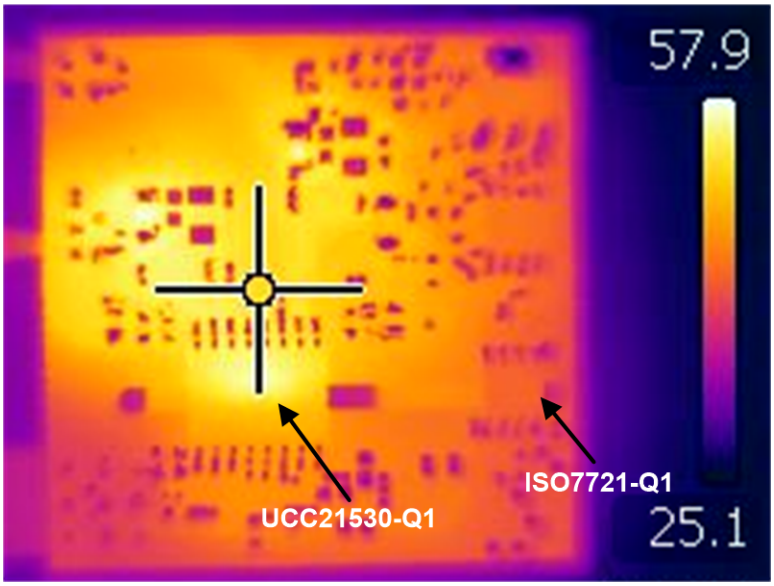


図 31. Thermal Image of Board (Bottom Side) at 500-kHz Switching Frequency

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01605.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01605.

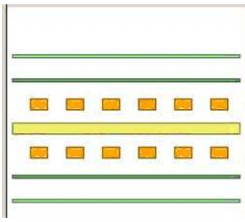
4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01605.

4.3.2 Layout Guidelines

The TIDA-01605 implements a 2-layer PCB. 図 32 shows the board material, copper thickness, and the dielectric distance in between.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation	Coverlay Expansion
Top Overlay	Overlay							
Top Solder	Solder Mask...	Surface Mat...	0.4	Solder Resist	3.5			0
Top Layer	Signal	Copper	1.4				Top	
Dielectric 1	Dielectric	Core	59.2	FR-4	4.8			
Bottom Layer	Signal	Copper	1.4				Bottom	
Bottom Solder	Solder Mask...	Surface Mat...	0.4	Solder Resist	3.5			0
Bottom Over...	Overlay							

図 32. TIDA-01605 Layer Stack

図 33 shows the component placement of the push-pull bias power supply. The input capacitor, SN6501-Q1 IC, and output capacitors are placed as close as possible to the Transformer T1, to minimize the input and output current loops. The secondary output of the push-pull power supply must be buffered to the isolated ground with low-ESR bypass capacitors. The recommended capacitor values can range from 1 to 10 µF, with X5R or X7R dielectric. The PCB clearance is kept as 8 mm for sufficient voltage isolation.

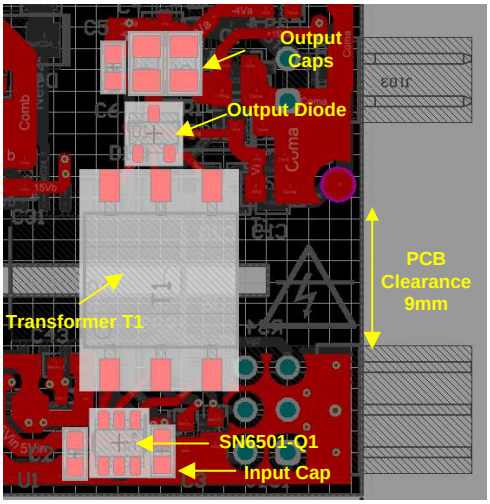


図 33. Component Placement of Push-Pull Power Supply

図 34 shows the component placement of the gate-drive loop, which includes the input capacitors for the bias supply rails, gate resistors, and gate capacitors. Low-ESR and low-ESL capacitors are selected and placed close to the UCC21530-Q1 device, between the VCCI and GND pins and between the VDD and VSS pins, to minimize the ripple and support high-peak currents when external SiC MOSFETs are being switched. The PCB traces for gate signals are kept small and compact, to minimize the noise crosstalk from the fast switching of the SiC MOSFETs.

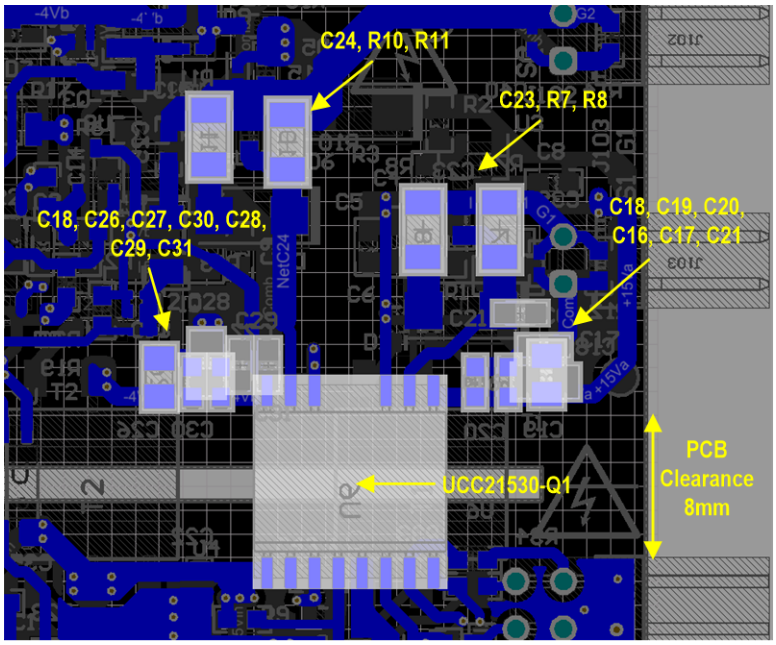


図 34. Component Placement of Gate-Drive Loop

図 35 shows the component placement for short-circuit detection. The signal-conditioning components are placed close to the SiC MOSFET drain, where pulsed, high dv/dt generates. The PCB areas are kept at a sufficient distance for voltage isolation.

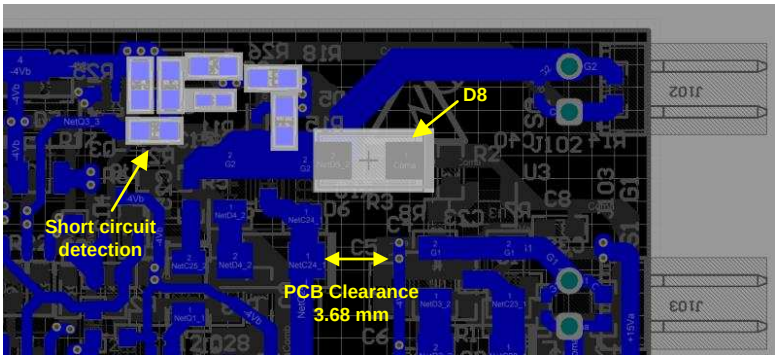


図 35. Component Placement for Short-Circuit Detection

4.3.3 General Recommendations

Apart from previous descriptions, some general layout design recommendations are listed as follows:

- Because the design contains high voltages, a PCB cutout is recommended to enhance the isolation rating between the primary and secondary. Any PCB traces or copper below the isolation devices must be avoided.
- Appropriate Creepage distances must be kept between high- and low-side PCB traces for sufficient voltage isolation.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-01605.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01605.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01605.

5 Related Documentation

1. Texas Instruments, High-Voltage Reinforced Isolation: Definitions and Test Methodologies, white paper
2. Texas Instruments, Small Form-Factor Reinforced Isolated IGBT Gate Drive Reference Design for 3-Phase Inverter, reference design (TIDA-00446)
3. Texas Instruments, Compact, Half-Bridge, Reinforced Isolated Gate Drive Reference Design, reference design (TIDA-01159)

5.1 商標

6 Terminology

AFE— Analog Front End

AEC— Automotive Electronics Council

ESR— Equivalent Series Resistance

EMI— Electromagnetic Interference

EMC— Electromagnetic Compatibility

DM— Differential Mode

CM— Common Mode

CMTI— Common Mode Transient Immunity

DCM— Discontinuous Conduction Mode

CCM— Continuous Conduction Mode

UVLO— Under Voltage Lockout

MOSFET— Metal Oxide Semiconductor Field Effect Transistor

CISPR— International Special Committee on Radio Interference

PE— Protective Earth

PSR— Primary Side Regulation

RMS— Root Mean Square

BOM— Bill of Material

OEM— Original Equipment Manufacturer

SiC— Silicon Carbide

PCB— Printed Circuit Board

HEV— Hybrid Electric Vehicle

EV— Electric Vehicle

7 About the Authors

XUN GONG is an Automotive Systems Engineer at Texas Instruments, where he is responsible for developing reference design solutions for HEV/EV powertrain applications. Xun brings to this role expertise in the fields of HEV/EV onboard charger, DC/DC Converter, and Traction Inverter based on IGBT and SiC (Silicon Carbide) power transistors. Xun achieved his Ph.D. in Electrical Engineering from Delft University of Technology in Delft, the Netherlands. Xun Gong won the 1st prize paper of the Academic Journal IEEE Transactions on Power Electronics in 2014.

GANGYAO WANG is a Systems Engineer with the High-Voltage Power Solutions Group at Texas Instruments, where he is responsible for defining high-power gate drivers and developing references design solutions for all kinds of applications using the SiC MOSFET. Before joining TI in 2017, Gangyao worked on SiC power device characterization and application. Gangyao has received his Ph.D. in Electrical Engineering from North Carolina State University in 2013, and he has published more than 40 technical papers in international journals and conference proceedings.

改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2018年3月発行のものから更新 **Page**

- ドキュメント全体を通して UCC21520-Q1 を UCC21530-Q1 に 変更 1
- 「リソース」から SN6105-Q1 を 削除 1
- 「リソース」に SN6501-Q1 を 追加 1
- ブロック図の画像を 変更 1
- ボードの画像を 変更 1
- working voltage allowed by the internal, functional isolation between the two secondary side drivers from 1.5-kV DC to 1.85-kV DC 変更 5
- information regarding under voltage lock-out (UVLO) protection 追加 5
- *Isolated Gate Driver Circuit* image 変更 10
- information in *Short Circuit Detection* 変更 12
- *Short-Circuit Detection Circuit* image 変更 12
- *TIDA-01605 PCB Board (Top Side)* image 変更 16
- *TIDA-01605 PCB Board (Bottom Side)* image 変更 17
- *Test Circuit for Propagation Delay of UCC21530-Q1* image 変更 22
- *Test Circuit for Measuring Propagation Delay of Reset Signal* image 変更 28
- *Thermal Image of Board (Bottom Side) at 200-kHz Switching Frequency* image 変更 30
- *Thermal Image of Board (Bottom Side) at 500-kHz Switching Frequency* image 変更 31
- *Component Placement of Gate-Drive Loop* image 変更 33

重要なお知らせと免責事項

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